A LOW POWER FULLY AUTONOMOUS WIRELESS HEALTH MONITORING SYSTEM FOR URINARY TRACT INFECTION SCREENING

A Dissertation

Submitted to the Faculty

of

Purdue University

by

Weeseong Seo

In Partial Fulfillment of the

Requirements for the Degree

of

Doctor of Philosophy

May 2019

Purdue University

West Lafayette, Indiana

THE PURDUE UNIVERSITY GRADUATE SCHOOL
STATEMENT OF DISSERTATION APPROVAL

Dr.Byunghoo Jung, Chair

School of Electrical and Computer Engineering

Dr.Babak Ziaie

School of Electrical and Computer Engineering

Dr.Kaushik Roy

School of Electrical and Computer Engineering

Dr.Pedro Irazoqui

School of Electrical and Computer Engineering

Approved by:

Dr.Pedro Irazoqui

Head of the School Graduate Program

For my dear parents,
my beloved wife, Yu Jin,
my loving son, Jiwan,
and my adorable daughter, Jia

ACKNOWLEDGMENTS

It has been a great honor and a privilege to be a graduate student at Purdue University. During the five years, I have been with brilliant professors and colleagues and learned so many things from them. I wish to acknowledge many people for giving me valuable lessons and joy during my life at Purdue.

First of all, I would like to thank my advisor, Prof. Byunghoo Jung for supervising my doctoral research. Throughout my graduate program, he has been a great mentor and supporter who gave me valuable advice. none of my doctoral work would have been possible without the contribution from him. I learned how to conduct a quality research from him. Whenever I encountered a problem along the way to my Ph.D., his keen insights guided me to the right direction, and his engineering expertise provided me with a new idea. I would also like to thank Prof. Babak Ziaie, Prof. Kaushik Roy, and Prof. Pedro Irazoqui for there valuable time and advice.

I would like to extend my appreciation to my colleagues for their support, discussion, and comradeship. I wish to thank Rubing Jin, Chamika M. Liyanagedera, Suchitra Mamesh, Ravi Abhishek Shankar. In particular, I thank Mohit Singh, my coffee buddy. Our discussions helped me overcome many difficulties and think wide from time to time.

Last but not least, I am truly thankful to my family for their love, support, and sacrifices. Without them, I would never have met this moment of finalizing this chapter.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

SYMBOLS

CLK	Operating frequency signal
I_{PD}	Photodiode current
V_{TH}	Threshold voltage
T_{PW}	Pulse width
C_P	Parasitic capacitance
ϵ_{SI}	Silicon dielectric constant
ϵ_0	Permittivity of free space
μ	Mobility of electrons
ρ	Resistivity of silicon
V_R	Reverse voltage of photodiode
ϕ_{bi}	Built-in junction voltage
A	Diffused Area of junction
σ_T	Standard deviation of jitter
q	Elementary charge of an electron
f	Frequency

ABBREVIATIONS

ADC	Analog-to-Degital Converter
BLE	Bluetooth Low Energy
CTS	Capacitance Touch Screen
CMOS	Complementary Metal Oxide Semicondu
DC	Direct Current
DI	Deionized
E.coli	Escherichia coli
IBIS	Input output Buffer information
IC	Integrated Circuit
LED	Light Emitting Diode
PBS	Phosphate-Buffered Saline
PCB	Printed Circuit Board
PSD	Power Spectral Density
PWM	Pulse Width Modulation
RMS	Root mean square
SPICE	Simulation program with integrated circuit emphasis
SR	Slew Rate
TI	Texas Instrument
TIA	Transimpedance amplifier
UTI	Urinary Tract Infection
VDD	Supply Voltage

ABSTRACT

Seo, Weeseong Ph.D., Purdue University, May 2019. A Low Power Fully Autonomous Wireless Health Monitoring System For Urinary Tract Infection Screening. Major Professor: Byunghoo Jung.

Recent advancements of health monitoring sensing technologies are enabling plethora of new applications in a variety of biomedical areas. In this work, we present a new sensing technology that enables a fully autonomous monitoring of urinary tract infection (UTI). UTI is the second most common infection in the human body caused by bacterial pathogens, and costs millions of dollars each year to the patients and the health care industry. UTI is easily treatable using antibiotics if identified in early stages. However, when early stage identification is missed, UTI can be a major source of serious complications such as ascending infections, loss of kidney function, bacteremia, and sepsis. Unfortunately, the limitations of existing UTI monitoring technologies such as high cost, time-intensive sample preparation, and relatively high false alarm rate prohibit reliable detection of UTI in early stages. The problem becomes more serious in certain patient groups such as infants and geriatric patients suffering from neurodegenerative diseases, who have difficulties in realizing the symptoms and communicating the symptoms with their caregivers. In addition to the aforementioned difficulties, the fact that UTI is often asymptomatic makes early stage identifications quite challenging, and the reliable monitoring and detection of UTI in early stages remain as a serious problem.

To address these issues, we propose a diaper-embedded, self-powered, and fully autonomous UTI monitoring sensor module that enables autonomous monitoring and detection of UTI in early stages with minimal effort. The sensor module consists of a paper-based colorimetric nitrite sensor, urine-activated batteries, a boost dc-dc

converter, a low-power sensor interface utilizing pulse width modulation, a Bluetooth low energy module for wireless transmission, and a software performing calibration at run-time.

To further optimize the sensor module, a new fully integrated DC-DC converter with low-profile and low ripple is developed. The proposed DC-DC converter maintains an extremely low level of output voltage ripples in the face of different battery output voltages, which is crucial for realizing low-noise sensor interfaces. Since the DC-DC converter is a part of a module embedded into a diaper, it is highly desirable for the DC-DC converter to have a small physical form factor in both area and height. To address this issue, the proposed DC-DC converter adopts a new charge recycling technique that enables a fully integrated design without utilizing any off-chip components. In addition, the DC-DC converter utilizes sub-module sharing techniques multiple modules share a voltage buffer and a recycle capacitor to reduce power consumption and save chip area. The DC-DC converter provides a regulated voltage of 1.2V and achieves a maximum efficiency of 80% with a 300Ω load resistance. The output voltage ripple is in the range of 19.6mV to 26.6mV for an input voltage ranging from 0.66 to 0.86V.

1. INTRODUCTION

1.1 Motivation

Urinary tract infection (UTI) is the second most common infection caused by bacterial pathogens, accounting for about 8.1 million hospital visits to health care providers in the US annually [1]. UTI is predominantly bacterial with coliform bacteria, in particular Escherichia coli (E.coli), being responsible for most cases [2]. It is also the most prevalent infection in the residents of long-term-care facilities with 15∼50% of the cases being asymptomatic [3], [4].

In general, UTI is considered to be easily treatable using antibiotics. However, if not found and treated early, UTI can be a major source of serious complications such as ascending infections (*e.g.*, pyelonephritis), loss of kidney function, bacteremia, and sepsis [5]. Consequently, early identification and treatment of UTI is vital to prevent major sequelae or death.

Infants and geriatric patients suffering from neurodegenerative diseases such as dementia are especially vulnerable to the deleterious effects of undetected UTI. Both groups use diapers and have difficulties understanding and/or communicating their urinary discomfort and UTI 30 associated symptoms (if not asymptomatic) to their care providers. These difficulties and the fact that UTI is often asymptomatic make early stage identification quite challenging.

Traditionally, an accurate diagnosis of UTI is made with the urine culture test in a laboratory [6]. This test allows quantification of the bacterial growth, but takes 2 to 3 days between specimen collection and final diagnosis due to the time period for cell cultivation. Furthermore, the urine culture test is not the best method for early detection of UTI. Primarily, the relatively high cost for hospital visits (to collect the specimen) and the urine culture test itself is cost0prohibitive and , in most cases,

prevents multiple and/or frequent urine culture tests from being performed. Second, a hospital visit for a urine culture test implies that the caregiver or patient already recognizes the symptoms of UTI, which often happens after serious complications have surfaced, particularly for asymptomatic patients.

For these reasons, urine dipsticks have been widely used in detecting UTI in early stages. A conventional urine UTI dipstick comprises a variety of chemical pads or reagents that react when immersed in, and then removed from, a urine sample. UTI dipsticks specifically detect the presence of nitrite, which is a surrogate of UTI. While urine dipsticks do allow for quick detection and are low-cost, this method is somewhat less accurate than conventional culture testing techniques with nitrite sensitivity falling within an 80-85% range [7]. Moreover, collecting a urine specimen for the dipstick test from an infant or a disabled elderly is often painful, time consuming, and privacy-sensitive. It becomes particularly challenging when multiple tests are required to filter out false alarms. Therefore, an alternative method for early-stage identification of UTI has been sought-after, and a better screening method that can alert caregivers about UTI with minimal effort is imperative.

1.2 Existing Approach

Several conventional UTI detection systems have been presented in the literature [8], [9]

1.2.1 Camera Based Detection System

In [8], the same chemical factors leveraged by a conventional UTI dipstick is printed on a commercial diaper using a hand-held printer which is designed to guarantee that a specific chemical factor is printed in a specific square area. When the reaction between the detection chemicals and urine occurs, a user such as a caregiver uses a camera of a smart phone to record the change in colors, process the images with a mobile application software using smartphone imaging analysis technology, and

takes further action concerning UTI. Accordingly, although this approach provides a fast detection by eliminating the time to collect urine samples, it does not offer a quantitative analysis and, more importantly, still requires an additional process to record the change in colors and process the images, thereby prohibiting completely autonomous operation. It also suffers from color fading issues because the time gap between urination and photo events is often unpredictable and the color of the sensing part fades over time when it dries up. Another issue is the contamination by stool that prohibits photo-based analysis. Both significantly affect the methodology's ability to provide accurate results.

1.2.2 CTS Based Detection System

In [9], a mutual-capacitance measurement is used to detect the presence of *E.coli* using a capacitance touch screen (CTS) with surface-electrodes modified to have *E.coli* receptors. In the case of CTS, the errors result from process variations such as the capacitance variation in the CTS and the offset variation in the charge amplifier. These errors should be compensated to improve the accuracy of the system, which normally increases the power consumption and the area of the system. Moreover, the CTS method is not autonomous because a caregiver should place the urine sample on the CTS surface manually.

In light of the shortcomings of conventional methods, an alternative, more accurate method for early-stage identification of UTI is needed, as is a better screening method that can alert caregivers about UTI with minimal manual effort. Ideally, such methods should be autonomous, automatic, minimally invasive, and provide the patient with privacy, all while being easy to implement, affordable, and capable of providing accurate and timely results.

2. UTI MONITORING SYSTEM

Fig. 2.1 shows a conceptual diagram representing the sensor module and system. As UTI dipsticks detect the level of nitrite, an indicator of UTI, the sensor module quantitatively evaluates the concentration of nitrite in the urine, and transmits the information via a Bluetooth low energy (BLE) module to a nearby BLE capable mobile device. The sensor module utilizes a flexible substrate that can either be embedded in a diaper during the manufacturing process or attached as an added unit

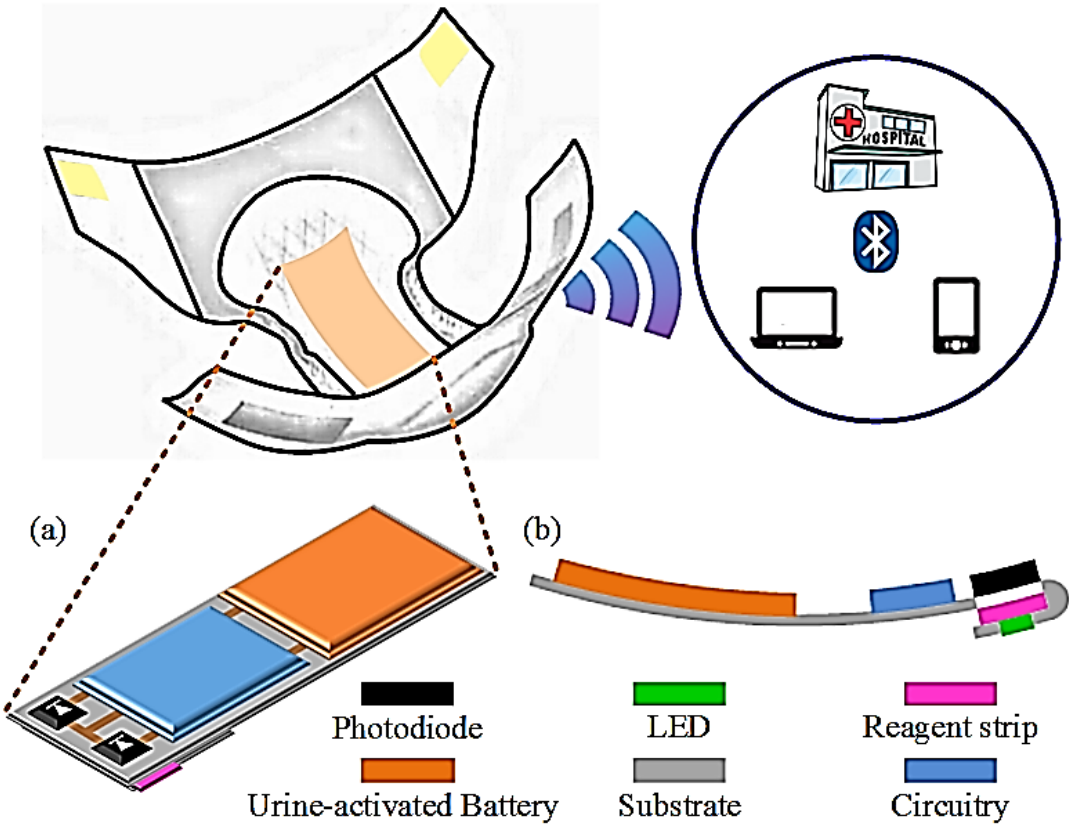


Fig. 2.1. Diaper-embedded UTI monitoring sensor module. (a) Diagonal view (b) Cross-section view

to a commercially available diaper. It is highly desirable that the disposable sensor module embedded in a diaper is self-powered because of cost and environmental issues. For this reason, the system utilized a urine-activated battery [10], which allows self-powered autonomous operations. Because of the limited amount of energy that the urine-activated battery provides, a power efficient yet accurate sensor interface circuit is crucial for successful operation.

2.1 Overview of Proposed UTI Monitoring Sensor Module

Fig. 2.2 shows a block diagram of the complete sensor module which is capable of self-wake-up, self-power, detection of UTI, and wireless transmission of information over BLE. This sensor module consists of five parts: (i) four urine-activated batteries connected in parallel (ii) a boost DC-DC converter (iii) a paper based colorimetric nitrite sensor (iv) a low-power sensor interface utilizing pulse width modulation (PWM), and (v) a BLE module for wireless transmission. Operating the sensor module utilizing urine-activated batteries simplifies the design by eliminating the need for periodic wakeup for checking the event of urination, which is required for a system that relies on a continuously powered battery. These urination-event driven automatic activation and wakeup also increase the shelf-life of the sensor module, and eliminate the color fading issue because the sensing is guaranteed to happen within a short time window after the urination-event. The output voltage provided by the batteries is not consistent and varies between 0.3V to 0.9V [10]. In order to ensure that the module functions reliably, this voltage is boosted and regulated to 2.0V with a power conversion efficiency of between 50% and 60%. Then, the boosted voltage provides power to the colorimetric nitrite sensor consisting of a light emitting diode (LED), a urine-absorbing strip, a reagent strip, an active photodiode, and a reference photodiode. It also powers the sensor interface and the BLE module. Using a regulated supply voltage is crucial to tightly control the light intensity of the LED and the performance of the sensor interface. The color of the reagent strip changes from

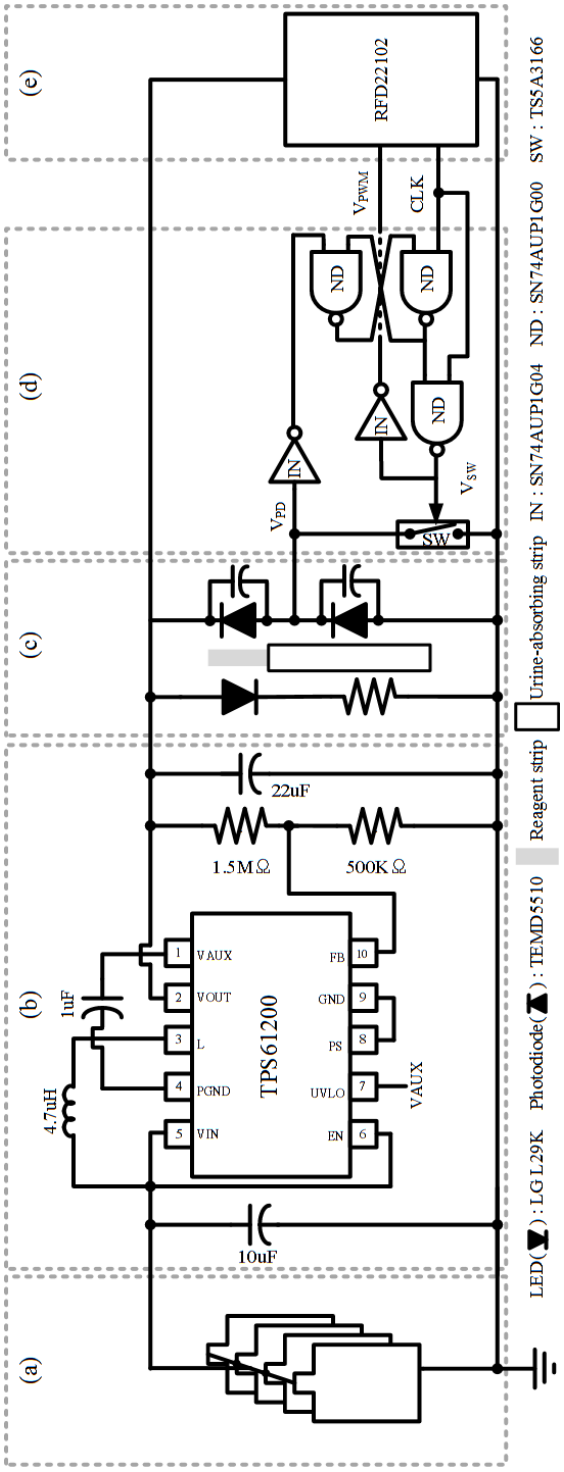


Fig. 2.2. A block diagram of the diaper-embedded UTI monitoring sensor module (a) Urine-activated batteries (b) Boost DC-DC converter (c) Colorimetric nitrite sensor (d) Sensor interface (e) BLE module

white to pink with the presence of nitrite in the urine. As in UTI dipstick, the color density of the reagent strip is a function of nitrite concentration in the urine. The color density is sensed by an LED-active photodiode pair sandwiching the reagent strip. The color density affects the intensity of the light reaching the active photodiode, and consequently affects the photocurrent generated by the active photodiode. We note that the LED light does not reach the reference photodiode. The reference photodiode is utilized to compensate the leakage dark current. Due to the weak sensitivity of the leakage dark current to the bias voltage, the leakage dark current of the two photodiodes is almost the same. Because the two photodiodes are connected in series, the balanced leakage dark currents cancel out each other and do not affect the output of the sensor interface. The series connected two photodiodes also provide a high impedance node required for charge accumulation. The sensor interface converts the photocurrent of the active photodiode into a pulse width modulated (PWM) waveform. The BLE module has a 40kHz in-built counter which digitizes the PWM signal data and transmits it to the mobile device of a caregiver, presumably connected to a centralized health monitoring network. The low-power capability of the sensor module is important because the urine powered battery has a limited power capacity, ranging from 3mW to 9mW.

2.2 Submodule Implementation

2.2.1 Urine-activated Battery

The battery is a Zn-Cu electrochemical cell providing a theoretical potential difference of 1.1V [10]. It is comprised of two half cells (Cu/CuSO4 and Zn/ZnCl2) and a salt bridge. The fabrication process starts with a laser (Universal Laser Systems, PLS6MW, 10.6m CO2 laser) machining a sheet of wax paper (Reynolds Cut-Ride, 40 m thick) into a 3cm square substrate. Then, copper and zinc (50 and 100m thick, respectively) tapes with an adhesive backing are carved into 2.5cm squares with electrical connection protrusions by the 1.06m fiber laser to create the metal electrodes.

Using the CO2 laser, filter papers (Whatman, Qualitative, 90 mm, 160 um thick) impregnated with CuSO4 are shaped into corresponding squares as electrolytes overlap the copper electrodes while those with KCl are patterned as salt-bridges as well as the electrolytes for the zinc electrodes. Afterwards, a polyimide tape is also machined by the CO2 laser. Additionally, small openings are laser cut on polyimide tape and Zn tape as access holes for urine activation of the battery. In the end, the battery is assembled through aligning and taping these patterned layers and the packaging is strengthened by high temperature lamination. Fig. 2.3 illustrates the fabrication process. When urine wets the filter papers through the predefined openings, the redox reaction starts to take place via the moist salt bridge connecting both half-cells, supplying power to the system.

2.2.2 Colorimetric Nitrite Sensor

Fig. 2.4 shows the structure of the colorimetric nitrite sensor [10]. All components are integrated onto a wax paper with great expansibility and high flexibility. In order to overlap and align the LED and the active photodiode, the sensor is folded along the dashed line in Fig. 2.4(a), and a urine-absorbing strip and a reagent strip

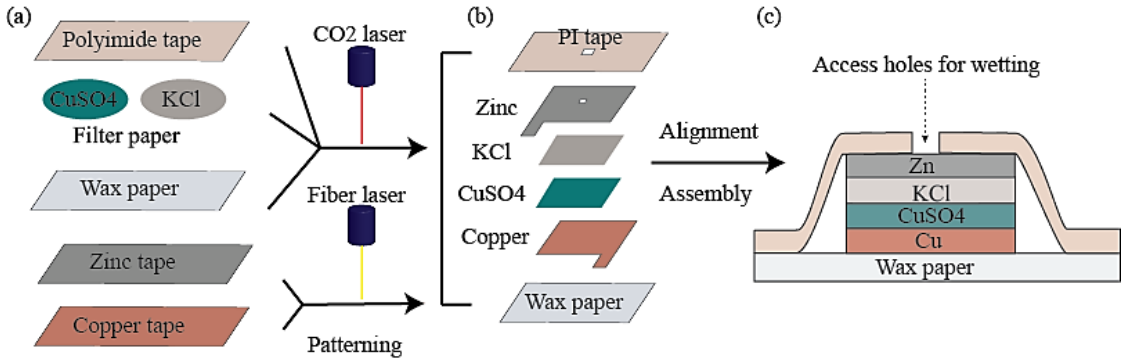


Fig. 2.3. Fabrication process of the urine-activated battery. (a) Laser-defining of the substrate, the active materials and the covering polyimide tape for the battery (b) Alignment and assembly of the battery (c) Schematic structure of the battery.

are placed between the LED and the active photodiode. The urine goes through the holes, reaches the urine-absorbing strip of the second layer, and then spreads until it arrives at the reagent strip of the third layer containing the Griess reagent. The urine reacts with p-arsanilic acid to produce a diazonium compound and to couple with N-ethylenediamine dihydrochloride in order. After the reaction chains for the detection of nitrite in acid medium, the color of the reagent strip changes from white to pink. The color density reflects the concentration of the nitrite in the urine and affects the amount of the light arriving at the active photodiode after passing through the reagent strip and consequently determines the photocurrent that the active photodiode generates. The concentration of nitrite, which indicates the level of UTI, can be quantified with the amount of the active photodiode current.

2.2.3 Sensor Interface Using Pulse Width Modulation

To convert the light intensity signal into an electrical signal, traditionally a transimpedance amplifier (TIA) converts the photodiode current into a voltage, and an analog-to-digital converter (ADC) provides digital data that represents the volt-

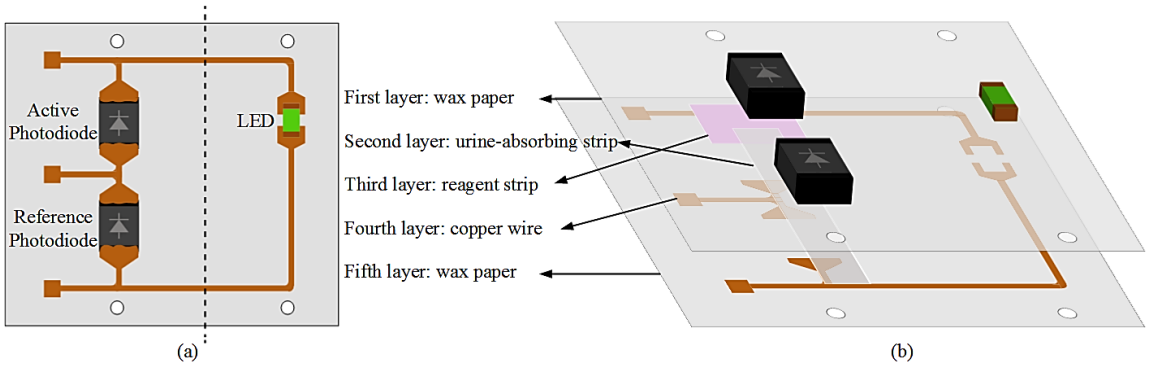


Fig. 2.4. Fabrication process of the urine-activated battery. (a) Laser-defining of the substrate, the active materials and the covering polyimide tape for the battery (b) Alignment and assembly of the battery (c) Schematic structure of the battery.

age [11]. This conventional topology increases the complexity and power consumption of the interface circuit. Because the module has a limited amount of energy available from the urine-activated battery, a power efficient sensor interface is highly desirable for reliable and self-powered operation of the sensor module. To address these issues, we developed a semi-digital PWM-based method, where the pulse width of the binary output signal is inversely proportional to the photodiode current, and a digital counter converts the pulse width into a digital signal. This PWM-based method allows to eliminate the complex and potentially power-intensive TIA and ADC. The pulse width modulated signal becomes less sensitive to the supply voltage noise because of its binary nature. It also provides a wide dynamic range because the data is represented in the time domain, measuring pulse width, rather than the voltage or current domain where its dynamic range is typically limited by the supply voltage.

Fig. 2.5 shows a block diagram of the two photodiodes in the colorimetric sensor

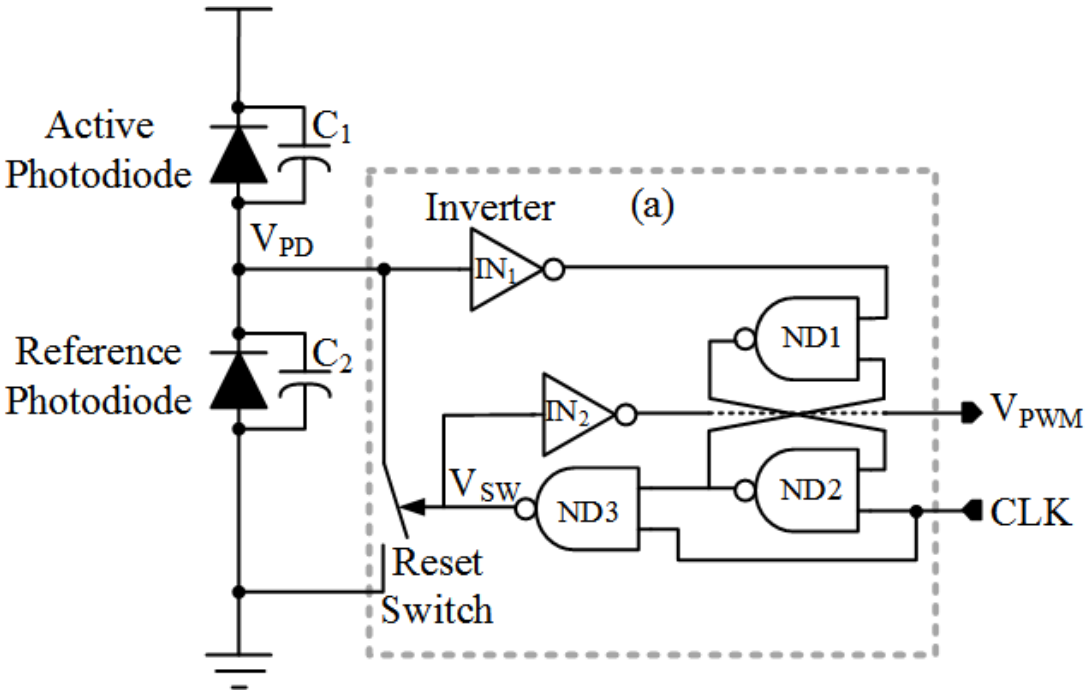


Fig. 2.5. The block diagram of photodiodes and sensor interface configuration.(a) Sensor interface circuit

and the sensor interface circuit. The sensor interface consists of two inverters, three NAND gates, and one analog switch. Two parasitic capacitors, C1 and C2, connected in parallel with the two photodiodes act as a charging capacitor.

Fig. 2.6 shows the signal response of the sensor interface operation at different stages. First, the active-high V_{SW} signal changes from *HIGH* to *LOW* at the rising edge of the *CLK* signal coming from the BLE module and turns the Reset switch off. Then, the photocurrent (I_{PD}) initiates the charging of the node V_{PD} located between the two photodiodes and the V_{PD} signal begins to increase. Once the V_{PD} signal reaches the inverter IN1 threshold voltage, V_{TH}, which is a fraction of the supply voltage, say $\alpha\,VDD$, where α is a constant smaller than 1 and should be calibrated for a reliable operation due to process variations, the IN1 output pushes the V_{SW} signal

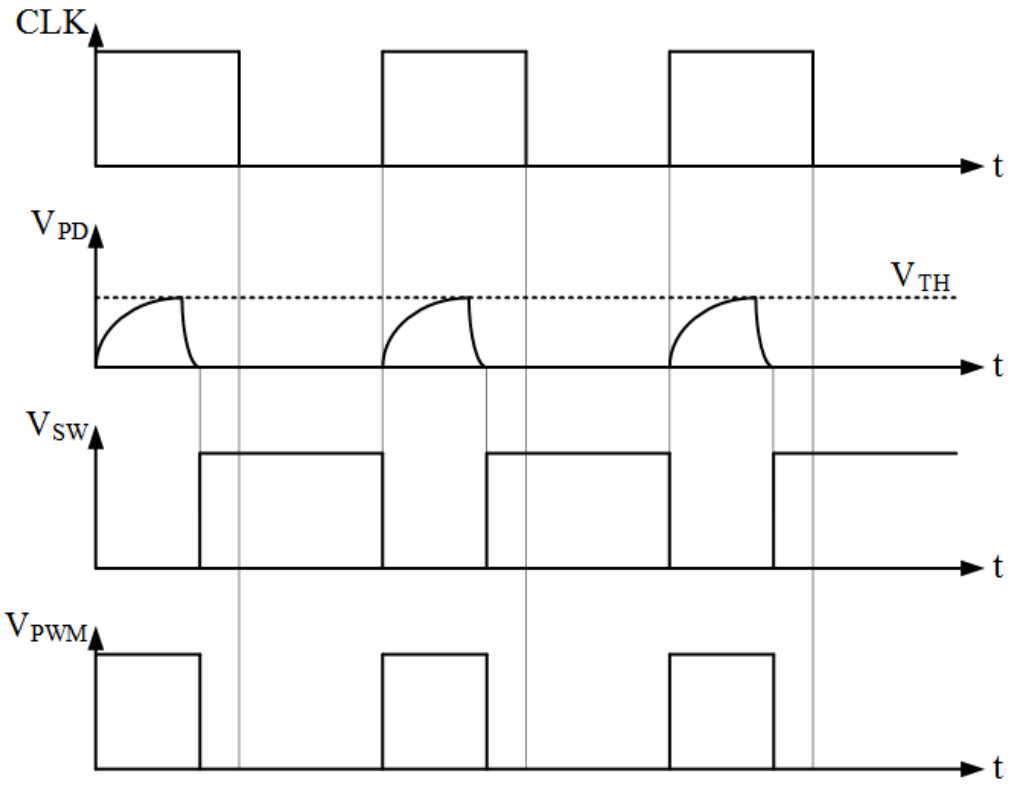


Fig. 2.6. Timing diagram for the sensor interface

to *HIGH*, resetting the V_{PD} signal to the ground. The V_{PWM} signal is the inverse of the V_{SW} signal.

If we assume that the parasitic capacitances are constant during the charging with the photocurrent I_{PD}, it is simple to analyze the relation between the pulse width T_{PW} of the V_{PWM} signal and the photocurrent I_{PD} as

$$T_{\mathrm{PW}} = \frac{(C_1 + C_2) \times \alpha VDD}{I_{\mathrm{PD}}} \tag{2.1}$$

The parasitic capacitances, however, vary significantly during the charging process due to the dependency on its reverse bias voltage as illustrated in Fig. 2.7. To obtain

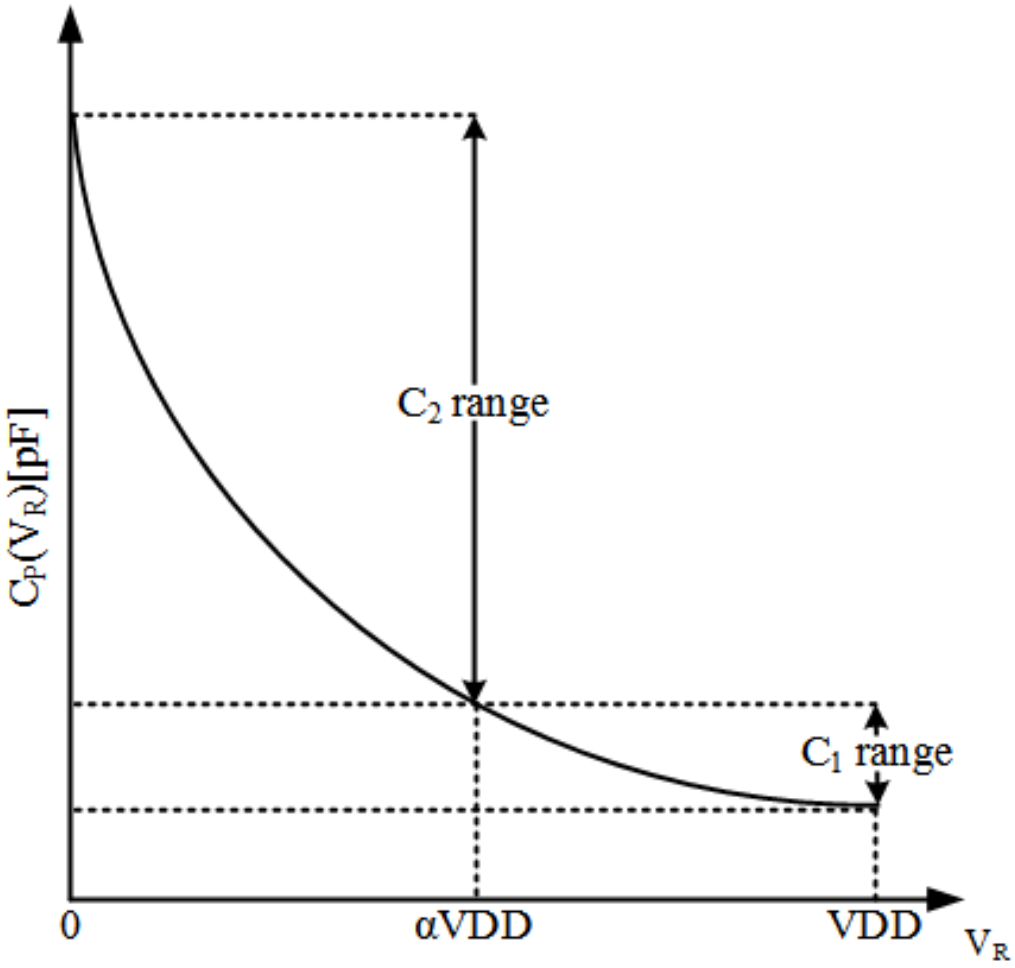


Fig. 2.7. Parasitic capacitance of a photodiode versus reverse bias voltage

the pulse width T_{PW} with voltage dependent capacitors, we use an abrupt pn-junction capacitance model and express the parasitic capacitance C_P dependent on the reverse bias voltage as follows:

$$\begin{aligned} C_{\mathrm{P}}(V_{\mathrm{R}}) &= \frac{\epsilon_{SI}\epsilon_0 A}{\sqrt{2\epsilon_{SI}\epsilon_0 A\mu\rho(V_{\mathrm{R}}+\phi_{bi})}} \\ &= \frac{K_0}{\sqrt{V_{\mathrm{R}}+\phi_{bi}}} \\ &\left(K_0 = \frac{\epsilon_{SI}\epsilon_0 A}{\sqrt{2\epsilon_{SI}\epsilon_0 A\mu\rho}}\right) \end{aligned} \tag{2.2}$$

where ϵ_{SI} is the silicon dielectric constant, ϵ_0 is the permittivity of free space, μ is the mobility of the electrons, ρ is the resistivity of the silicon, V_R is the applied reverse bias voltage, ϕ_{bi} is the built-in junction voltage, and A is the diffused area of the junction.

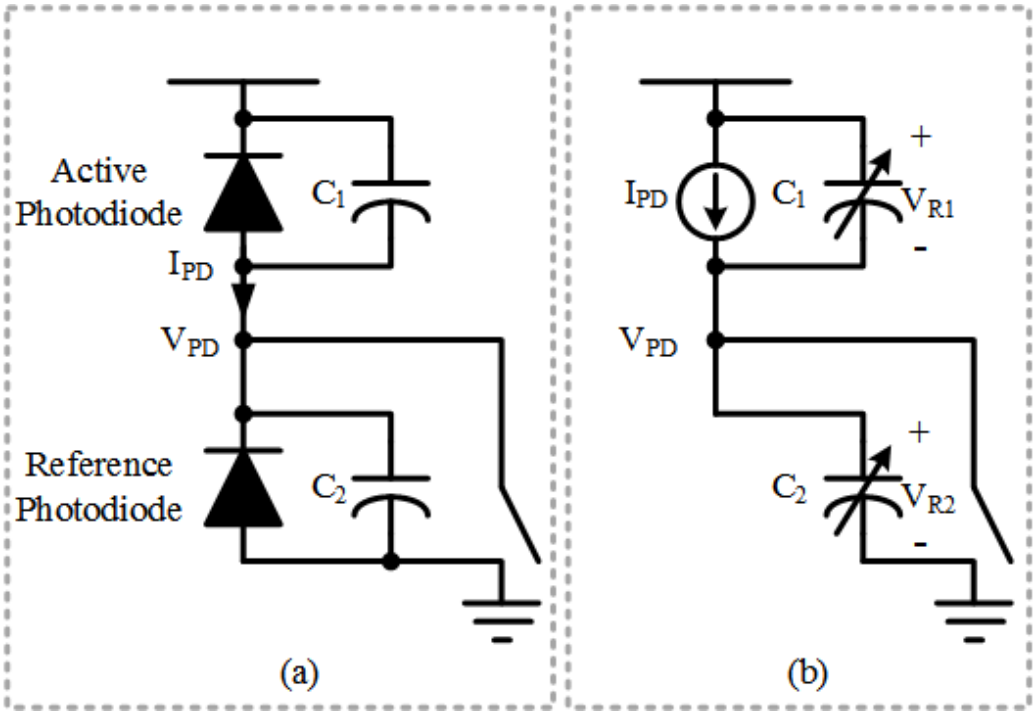


Fig. 2.8. (a) Active and reference photodiode with parasitic capacitors C_1 and C_2 (b) Circuit model with the voltage dependent parasitic capacitors.

Fig. 2.8 shows the circuit model of the two variable parasitic capacitors. To calculate T_{PW}, we add the contributions of each parasitic capacitor of the two photodiodes. From Fig. 2.8, the parasitic capacitance C_1 of the active photodiode can be described as

$$C_1(V_{R1}) = C_P(VDD - V_{PD}) \tag{2.3}$$

where V_{R1}=VDD-V_{PD}.

In addition, the parasitic capacitance C_2 of the reference photodiode can be given as

$$C_2(V_{R2}) = C_P(V_{PD}) \tag{2.4}$$

where V_{R2}=V_{PD}. Using (2.3) and (2.4), we can get

$$I_{PD} = [C_P(VDD - V_{PD}) + C_P(V_{PD})]\frac{dV_{PD}}{dt} \tag{2.5}$$

Performing an integral, we can describe the relation between the pulse width T_{PW} and the photocurrent I_{PD} as follows:

$$\begin{aligned} T_{\mathrm{PW}} &= \frac{1}{I_{\mathrm{PD}}}\int_0^{\alpha VDD}[C_P(VDD - V_{PD}) + C_P(V_{PD})]dV_{PD} \\ &= \frac{\beta}{I_{PD}} \\ &\quad (\beta = 2K_0(\sqrt{VDD + \phi_{bi}} - \sqrt{(1-\alpha)VDD + \phi_{bi}} + \sqrt{\alpha VDD + \phi_{bi}} - \sqrt{\phi_{bi}})) \end{aligned} \tag{2.6}$$

Equation (2.6) shows that the pulse width T_{PW} of the V_{PWM} signal is inversely proportional to the photocurrent I_{PD}, even with the voltage dependent parasitic capacitances.

3. DESIGN CONSIDERATION

3.1 Effects of Noise

There are various sources of noises in the sensor module. The main noise sources limiting the performance of the sensor module exist in the photodiodes and the sensor interface such as shot noise in the photodiodes, thermal noise of the constituent devices in the sensor interface, and the random fluctuation of the power supply *VDD*. Because the line and load regulation of the boost converter is 0.1% (typ.) and 0.5% (max.) with the conditions (*i.e.*, the input voltage of the boost converter changes from 0.3V to 0.8V and the load current varies from 4.58mA to 6.58mA), which is insignificant compared with other noise sources , we ignored the periodic logic threshold shifts of inverters and NAND gates by ripple in the boost DC-DC converter output. These noises introduce jitter in the edges of the output signal. Assuming a white Gaussian random distribution, the root mean square (RMS) jitter and the standard deviation of jitter, σ_{T}, can be expressed as $\mathrm{Jitter}_{\mathrm{rms}} = \sigma_{\mathrm{T}}$ and the noise μ_{N} can be defined as μ_{N} $N(0, \sigma^2{}_{\mathrm{V\ or\ I}})$ with a standard deviation σ_{V} as the voltage or σ_{I} as the current.

The rising edge of the V_{PWM} signal is only affected by the noise from the inverter and the NAND gate. The falling edge of the V_{PWM} signal is affected by the noise from the photodiodes, the power supply, the inverters, and the NAND gates. Since the inverter and the NAND gate carry digital signals with a high slew rate, the jitter generated by the inverter and the NAND gate is less significant. However, the noise voltage of the power supply and the noise current of the photodiodes significantly affect the V_{PD} signal that changes slowly and determines the falling edge of V_{PWM} signal. Consequently, more significant jitter appears at the falling edges of the V_{PWM} signal.

The pulse width of the output signal is affected by the following noise sources as shown in Fig. 3.1.

i Noise voltage from *VDD*:

$\mu_{N\_VDD} \sim N(0,\sigma^2_{N\_VDD})$.

ii Noise current from the active photodiode:

$\mu_{N\_PD} \sim N(0,\sigma^2_{N\_PD})$.

iii Noise voltage from the inverters:

$\mu_{N\_IV1} \sim N(0,\sigma^2_{N\_IV1})$,$\mu_{N\_IV2} \sim N(0,\sigma^2_{N\_IV2})$.

iv Noise voltage from the NAND gates:

$\mu_{N\_ND1} \sim N(0,\sigma^2_{N\_ND1})$, $\mu_{N\_ND2} \sim N(0,\sigma^2_{N\_ND2})$,$\mu_{N\_ND3} \sim N(0,, \sigma^2_{N\_ND3})$.

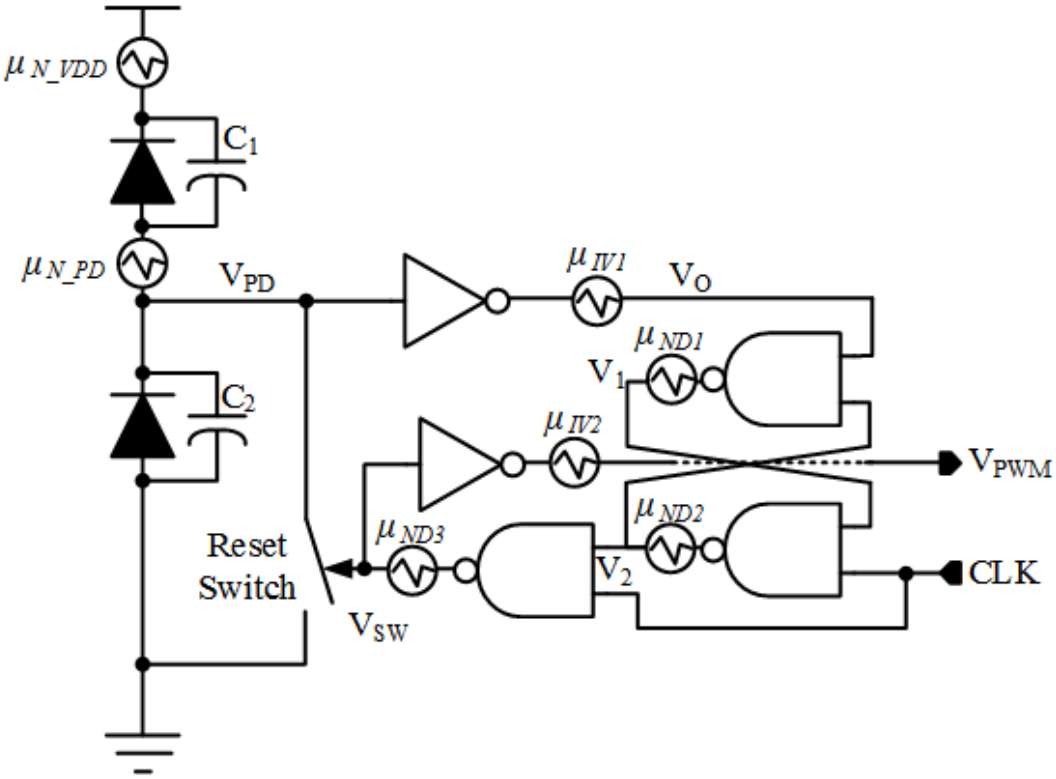


Fig. 3.1. Conceptual diagram of the noise sources

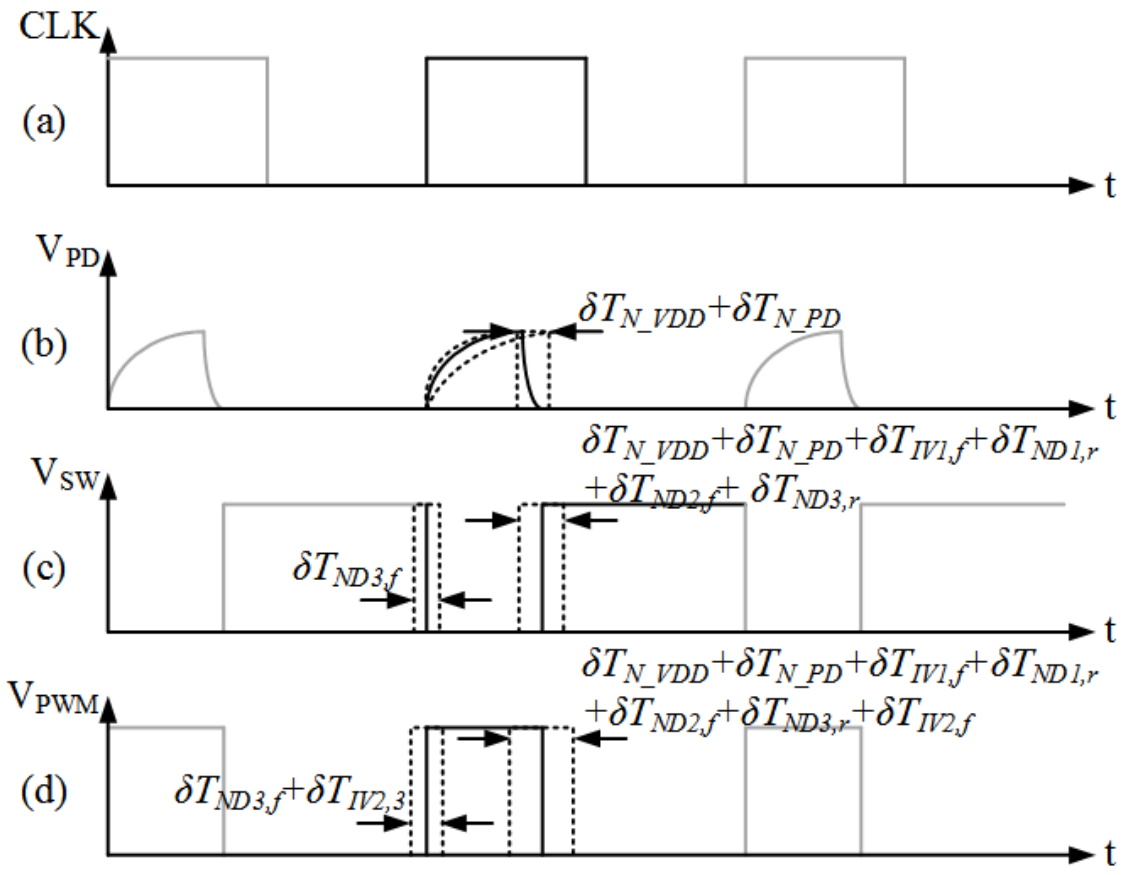


Fig. 3.2. Effect of jitter at different stage. (a) Clock signal. (b) V_{PD} signal at charging node. (c) V_{SW} signal to control the analog switch (d) Output V_{PWM} signal

Fig. 3.2 depicts the effect of each noise source to each signal stage and the output V_{PWM} signal. To find the jitter μ_{T_1st} on the output V_{PWM} signal generated by the additive noise μ_{N_PD}, and μ_{N_VDD}, we first consider the additive noise current μ_{N_PD}, superimposed on the V_{PD} signal. The dominant noise in the active photodiode is shot noise and can be modeled as the white Gaussian random noise process with a two sided power spectral density (PSD), $S_{PD1}(f)$ [12].

$$S_{\mathrm{PD1}}(f) = qI_{\mathrm{PD}}A^2/Hz \tag{3.1}$$

where q is the elementary charge of an electron. It can be expressed as $\mu_{\mathrm{N\_PD}} \sim N(0, qI_{PD}\Delta f)$. In such a noisy environment, the V_{PD} signal is the sum of a signal voltage v_{pd} and a noise voltage v_n, *i.e.*, $V_{\mathrm{PD}} = v_{\mathrm{pd}} + v_{\mathrm{n}}$. Assuming that the signal voltage is much larger than the noise voltage, we can approximate the parasitic capacitance as $C_1(VDD\text{-}V_{PD}) \approx C_p(VDD\text{-}v_{pd})$ and $C_2(V_{PD}) \approx C_p(v_{pd})$. With this approximation, we can obtain

$$\begin{aligned} T_{\mathrm{PW}} &= \frac{1}{I_{PD} + \mu_{N\_PD}} \int_0^{\alpha VDD} [C_P(VDD - v_{pd}) + C_P(v_{pd})] dv_{pd} \\ &= \frac{\beta}{I_{PD} + \mu_{N\_PD}} \end{aligned} \tag{3.2}$$

Assuming $y = I_{PD} + \mu_{N\_PD}$, the variance of jitter, σ_{T_PD}, can be derived according to the variance of noise current, $qI_{PD}\Delta f$, as

$$\begin{aligned} \sigma_{T\_PD}^2 &= Var[T_{\mathrm{PW}}] = \beta^2 \cdot Var[\frac{1}{I_{PD} + \mu_{N\_PD}}] \\ &= \beta^2 \cdot \{ \int_{-\infty}^{\infty} \frac{1}{y^2} \cdot \frac{1}{\sqrt{2\pi q I_{PD} \Delta f}} \cdot e^{-(y - I_{PD})^2 / 2qI_{PD}\Delta f} dy \\ &\quad - [\int_{-\infty}^{\infty} \frac{1}{y^2} \cdot \frac{1}{\sqrt{2\pi q I_{PD} \Delta f}} \cdot e^{-(y - I_{PD})^2 / 2qI_{PD}\Delta f} dy]^2 \} \end{aligned} \tag{3.3}$$

In addition, σ_T can be approximately expressed using the equation derived in [13] and [14]

$$\sigma_T = \frac{\sigma_V}{SR} \tag{3.4}$$

where SR is the slew rate of the signal. Because the V_{PD} signal is not linear, the slope of the V_{PD} signal needs to be calculated when the V_{PD} signal reaches αVDD as follows:

$$\begin{aligned} \frac{dV_{\mathrm{PD}}}{dt}|_{V_{PD}@\alpha VDD} &= \frac{I_{PD}}{C_P(VDD - V_{PD}) + C_P(V_{PD})}|_{V_{PD}@\alpha VDD} \\ &= \gamma \cdot I_{\mathrm{PD}} \\ &\quad (\gamma = \frac{\sqrt{(1-\alpha)VDD + \phi_{bi}} + \sqrt{\alpha VDD + \phi_{bi}}}{K}) \end{aligned} \tag{3.5}$$

Using (3.2), (3.3), and (3.4), the jitter σ_{T_1st} can be obtained as

$$\begin{aligned} \sigma_{T\_1st} &= \sqrt{\sigma_{T\_PD}^2 + (\frac{\sigma_{N\_VDD}}{\gamma I_{PD}})^2} \\ &= (\delta T_{N\_PD} + \delta T_{N\_VDD})_{\mathrm{rms}} \end{aligned} \tag{3.6}$$

Due to the slow change in the V_{PD} signal, the σ_{T_1st} becomes the main jitter which is inversely proportional to the photodiode current.

The jitter added onto the V_{PWM} by the inverters are

$$(\delta T_{IV1})_{rms} = \frac{\sigma_{IV1}}{SR_{IV}} \tag{3.7}$$

$$(\delta T_{IV2,r})_{rms} = \frac{\sigma_{IV2,r}}{SR_{IV}}; (\delta T_{IV2,f})_{rms} = \frac{\sigma_{IV2,f}}{SR_{IV}} \tag{3.8}$$

where SR_{IV} is the slew rate at the output of the inverter.

The jitter introduced by the NAND gates are

$$(\delta T_{ND1,f})_{rms} = (\delta T_{ND3,f})_{rms} = \frac{\sigma_{ND1,f}}{SR_{ND}} \tag{3.9}$$

$$(\delta T_{ND2,r})_{rms} = (\delta T_{ND3,r})_{rms} = \frac{\sigma_{ND2,r}}{SR_{ND}} \tag{3.10}$$

where SR_{ND} is the slew rate at the output of the NAND gate.

From equation (3.5) (3.10), it is important to note that the rising edge jitter is smaller than the falling edge jitter and the falling edge jitter is inversely proportional to the photodiode current.

By adding the independent jitter sources, we can estimate the time deviation from the ideal output pulse width of the V_{PWM} signal as

$$\begin{aligned}\sigma_{T,total} = [&(\delta T_{N\_VDD} + \delta T_{N\_PD})^2 + (\delta T_{IV1})^2 + (\delta T_{IV2,r})^2 \\ &+ (\delta T_{IV2,f})^2 + 2(\delta T_{ND1,f})^2 + 2(\delta T_{ND2,f})^2]^{1/2}\end{aligned} \tag{3.11}$$

Using the total jitter $\sigma_{T,total}$ and by differentiating (2.6), we can estimate the photodiode current resolution $I_{PD,res}$ as

$$I_{PD,res} = |\sigma_{T,total} \cdot \frac{{I_{PD}}^2}{\beta}|_{@MaximumI_{PD}} \tag{3.12}$$

where the nitrite concentration of 0mg/L provides the maximum photodiode current. Equation (3.12) shows that photodiode current resolution $I_{PD,res}$ can be improved by either reducing the photodiode current I_{PD} or the jitter $\sigma_{T,total}$. However, the photodiode current I_{PD} determines the detection range of the sensor module, hence to increase photodiode current resolution $I_{PD,res}$, reducing the jitter $\sigma_{T,total}$ is a better

option. The dominant sources of jitter $\sigma_{T,total}$ are the noise voltage of power supply and the shot noise of the photocurrent, which are white and can be reduced by averaging samples [15]. For the proposed system, a photocurrent resolution of 30nA is required for the targeted nitrite concentration detection sensitivity, 1.35ms/(mg/L). Without averaging, the photocurrent resolution of the system is about 117nA, which does not meet the target. We achieved the target resolution by averaging over 100 consecutive pulse width data.

3.2 Process Variations

Process variations are unavoidable during the manufacturing processes of the LED, the photodiodes, the urine-absorbing strip, the reagent strip, inverters, and NAND gates, and become a critical concern in the system design. With the presence of large variations contributed by the consisting elements, a reliable operation of the sensor module would be almost impossible. To mitigate this problem, we present a differential reading technique and an effective on-line calibration method.

We note that the process variations would impact the output pulse width for the dry reagent strip (before reacting with urine) and for the wet reagent strip (after reacting with urine) in the same manner. Consequently, the differential reading between the pulse width (T_{PW1}) for the dry reagent strip and the pulse width (T_{PW2}) for the wet reagent strip would suffer significantly less from process variations.

To measure the difference, we use a time lapse reading technique. The sensor module is designed in such a way that the urine reaches the urine-activated batteries first, and the reagent strip later. As soon as the urine-activated batteries become active, the sensor module measures T_{PW1} while the reagent strip is dry. The following readings use T_{PW1} as a reference, and the sensor module registers the differential pulse width, $T_{DPW} = T_{PW1}$ - T_{PW2}, rather than T_{PW1}. Although the effect of process variations can be partially mitigated by this time-lapse based differential reading

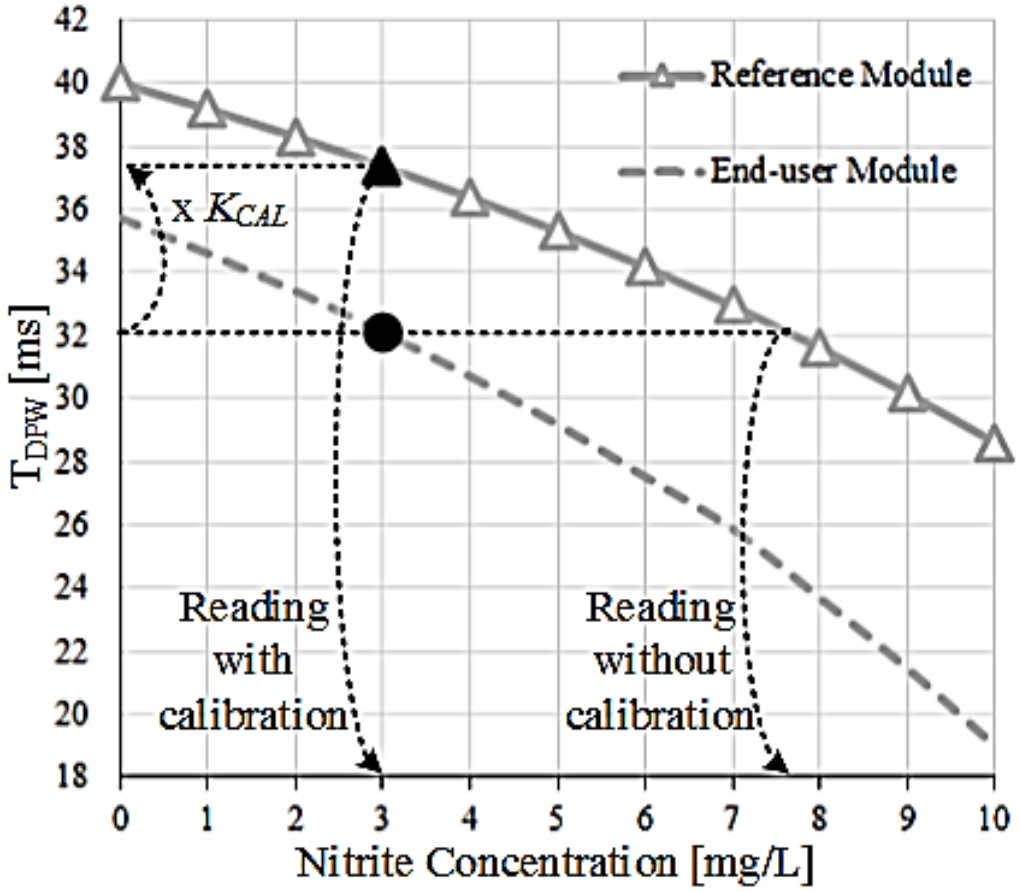


Fig. 3.3. Calibration for process variations.

technique, the sensor module is still vulnerable to process variations, requiring further calibrations.

The proposed on-line calibration finds a process variation constant number K_{CAL} using a known reference and corrects the measured differential pulse width by multiplying the constant K_{CAL}. In this method, we use one arbitrarily selected sensor module as a known universal reference. An end-user sensor module has the performance deviation from the reference module and shows a different output pulse width at the same nitrite concentration. The measured differential pulse width of an end-user sensor module can be annotated back to the differential pulse width of the reference module by multiplying the constant K_{CAL}, as shown in Fig. 3.3.

First, we measure the nitrite concentration versus the differential pulse width curve using the known reference module as shown in Fig. 3.3. We can express the reference pulse widths ($T_{DPW,REF}$) by visiting the familiar formula (2.6) and using the differential reading technique

$$T_{DPW,REF} = \beta_{REF}(\frac{1}{I_{DRY,REF}} - \frac{1}{I_{WET,REF}}) \tag{3.13}$$

where $I_{DRY,REF}$ is a reference photocurrent when the reagent strip is dry and $I_{WET,REF}$ is a reference photocurrent when the reagent strip is wet. The data for the reference module is stored in the mobile device that performs the calibration operation. Because each end-user module has a different constant β, each sensor module should be able to find its own value of β unless the constant value is measured for each module during the production stage, which is challenging because the module is intended for one-time use and to be disposable. In the developed system, each sensor module finds the value of β autonomously utilizing the dry condition measurement. For the time lapse based differential measurement, the sensor module first measures the pulse width T_{PW1}. Because the nitrite concentration in the urine should not affect the constant β, we can calculate the constant K_{CAL} using the measured T_{PW1} and the known value of $T_{PW1,REF}$ from the known reference.

$$K_{CAL} = \frac{T_{PW1,REF}}{T_{PW1}} = \frac{\beta_{REF}}{\beta} \cdot \frac{I_{DRY}}{I_{DRY,REF}} \tag{3.14}$$

As the process variations would impact the output pulse width for the dry reagent strip and for the wet reagent strip in the same manner, we can express the relationship between the two reference currents and the two end-user currents as

$$I_{DRY} = \epsilon I_{DRY,REF}, I_{WET} = \epsilon I_{WET,REF} \tag{3.15}$$

where I_{DRY} is an end-user photocurrent when the reagent strip is dry and I_{WET} is an end-user photocurrent when the reagent strip is wet. The calibrated differential pulse width $\mathrm{T_{DPW,CAL}}$ can be obtained by multiplying the calculated constant $\mathrm{K_{CAL}}$ to the measured differential pulse width and using (3.16):

$$T_{DPW} = \beta(\frac{1}{I_{DRY}} - \frac{1}{I_{WET}}) \tag{3.16}$$

$$
\begin{aligned}
T_{DPW,CAL} &= K_{CAL} \cdot T_{DPW} \\
&= \beta_{REF}\left(\frac{1}{I_{DRY,REF}} - \frac{I_{DRY}}{I_{DRY,REF}}\frac{1}{I_{WET}}\right) \\
&= \beta_{REF}\left(\frac{1}{I_{DRY,REF}} - \frac{1}{I_{WET,REF}}\right)
\end{aligned}
\tag{3.17}
$$

4. IMPLEMENTATION AND MEASUREMENT RESULTS

Implementation and measurement were performed in three versions of the sensor module. The first version sensor module focuses on the implementation of the proposed technology and the characterization of the each sub-modules. The results generated from the first version was used to redefine one or more of the problems established in the initial phase, and to build a more robust understanding of the problems. The second version focused on making the sensor module practical and economical. The third version focused on improving the power efficiency and accuracy of the sensor module.

4.1 First sensor module

Fig. 4.1 shows the implementation of the first UTI sensor module. The first version has four separate modules connected through wires: a urine activated battery module, a circuit module, a sensor module, and a BLE module. The first sensor module focused on the implementation of the proposed technology and the characterization of the each modules The measurement setup used for the sensor module is shown in Fig. 4.2. The boost DC-DC converter and the PWM sensor interface are mounted on a custom printed circuit board (PCB). During measurements, the colorimetric nitrite sensor is placed in a box to make sure that the active photodiode only responds to the LED light, but not to the ambient light. An LED with the peak emission wavelength of 572nm is chosen because of its high sensitivity to pink color. Two photodiodes with the peak sensitivity wavelength of 540nm are used. The LED bias current is set to 0.5mA while the PWM sensor interface draws 0.008mA from the regulated 2V supply. The microcontroller in the BLE module (RFD22102 from RFDuino) provides the *CLK* signal and converts the pulse width output of the PWM sensor interface

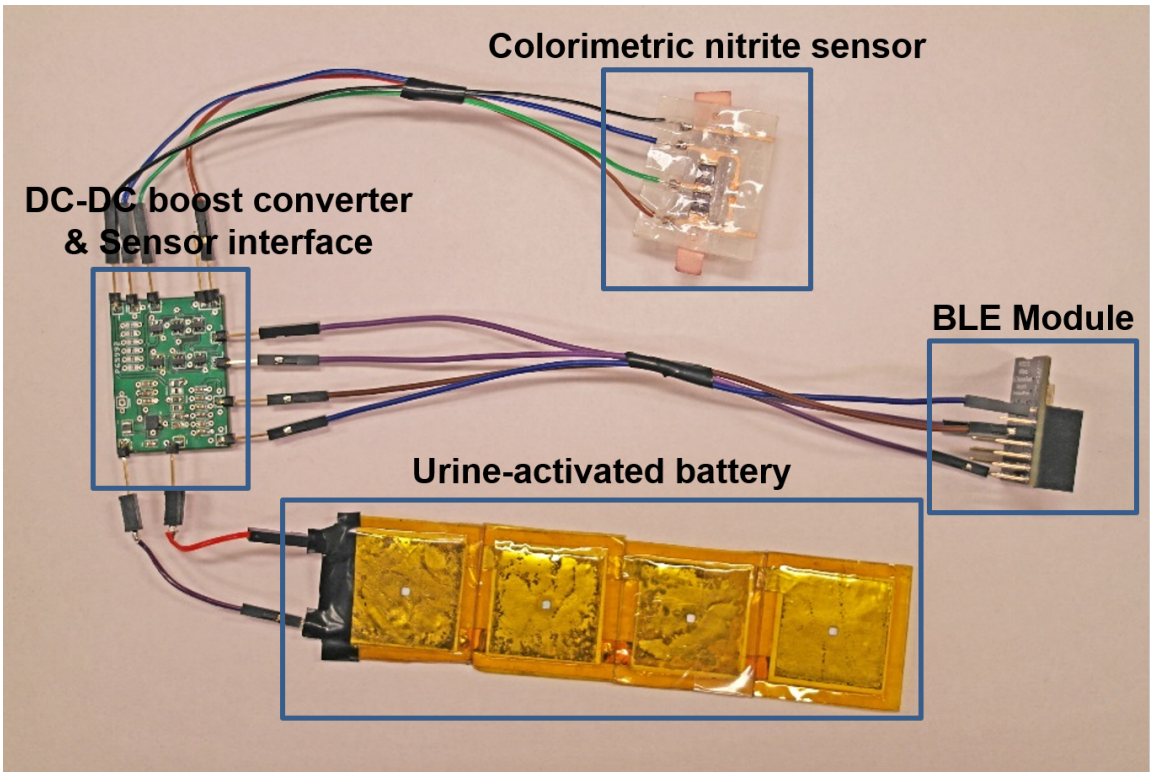


Fig. 4.1. The first version sensor module

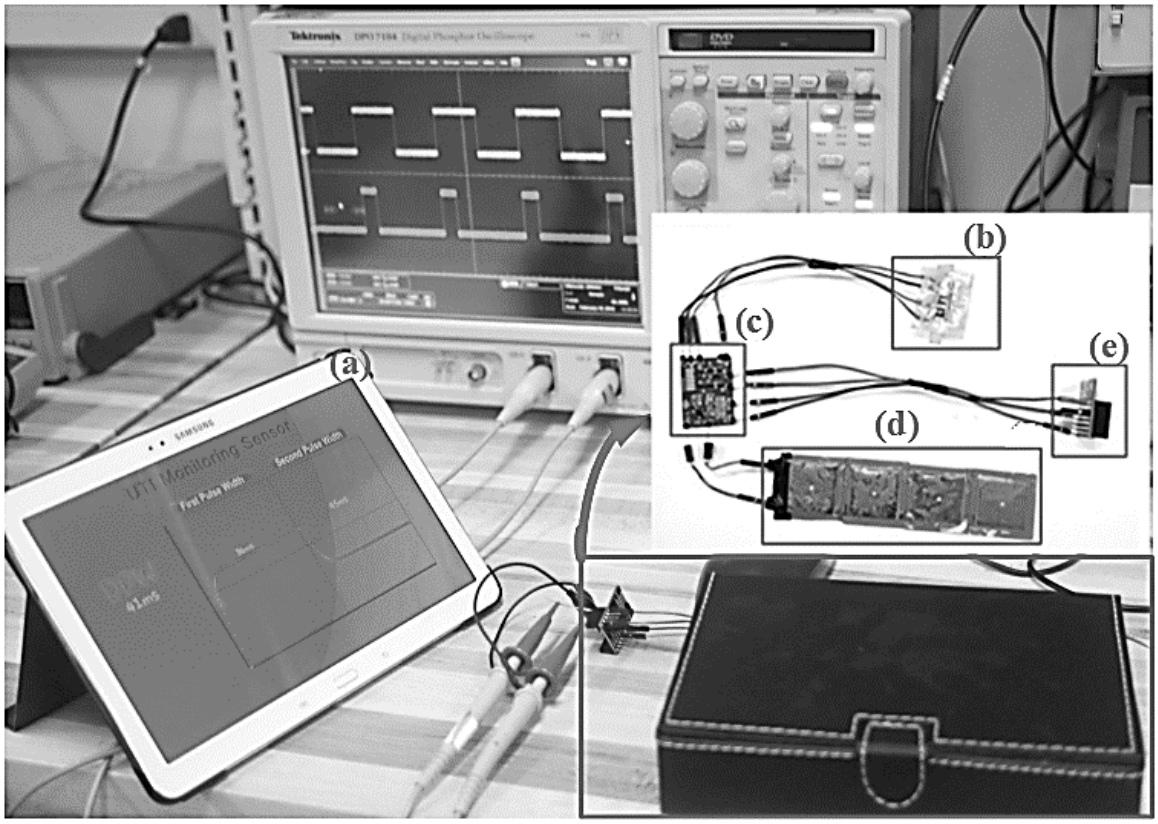


Fig. 4.2. Measurement set-up. (a) Mobile APP displaying nitrite concentration in real time (b) Colorimetric nitrite sensor (2.5cm x 3.5cm, 3g) (c) DC-DC boost converter and sensor interface (2.7cm x 3.6cm, 6g) (d) Urine-activated batteries (15cm x 3.5cm, 6g) (e) BLE module (RFD22101) (2.3cm x 2.9 cm, 5g)

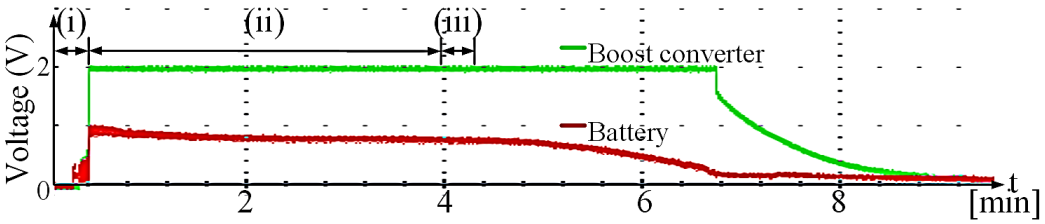


Fig. 4.3. Measured the battery voltage and the boost converter voltage: (i) Initial urine exposure and battery activation, (ii) DC-DC boost convert start and sensor reading (iii) BLE transmission

into digital data using the built-in counter that is transmitted to a paired mobile device (an Android tablet). The BLE module draws 6mA in transmission mode.

Synthetic urine samples with nitrite concentrations of 0mg/L, 4mg/L, 6mg/L, 8mg/L, and 10mg/L are used for the measurements. To perform the tests, urine samples were dropped onto the sensors and the urine-activated batteries at the same time. Fig. 4.3 shows the voltage variation of the urine-activated batteries and the regulated voltage of the boost DC-DC converter. The batteries are activated in 10 seconds after initial urine exposure and the boost DC-DC converter starts operation when the voltage of batteries reaches a start-up voltage of 0.5V, at which time the colorimetric sensor starts reading. The PWM signals for the dry reagent strip and

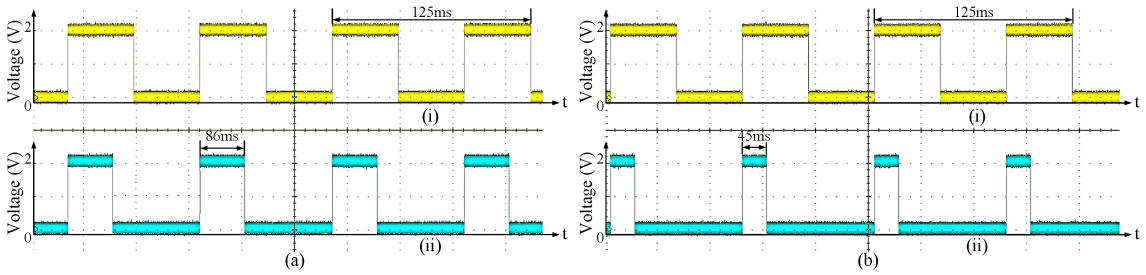


Fig. 4.4. Measured PWM signal (a) Pulse width for the dry reagent strip: (i) Clock signal, (ii) Output V_{PWM} signal, and (b) Pulse with for the wet reagent strip: (i) Clock signal, (ii) Output V_{PWM} signal.

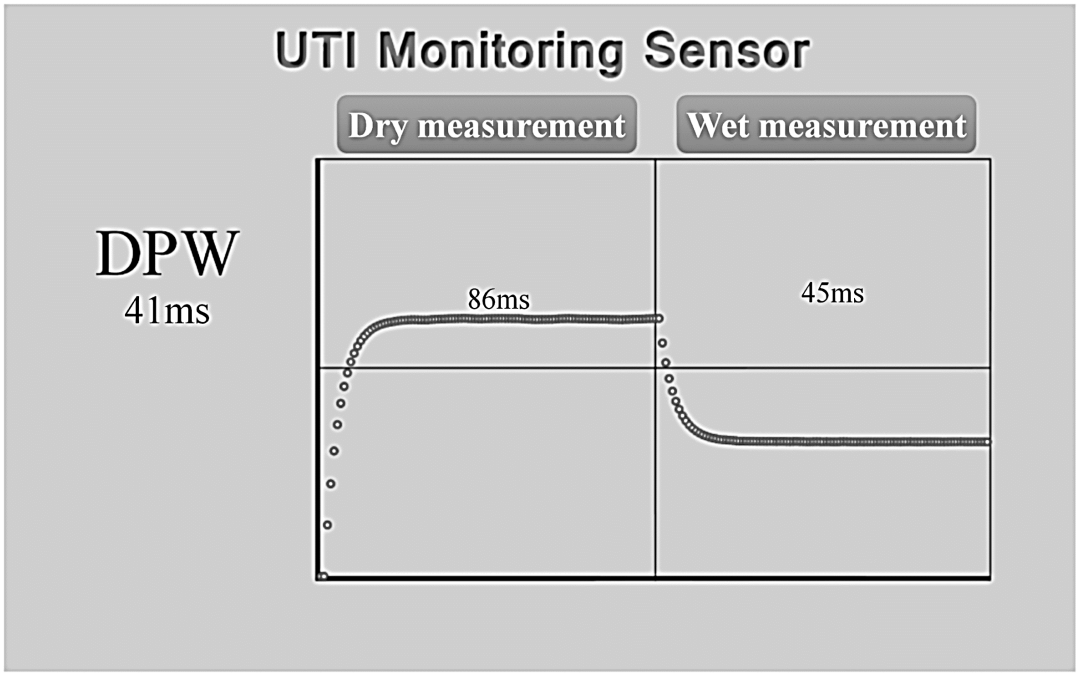
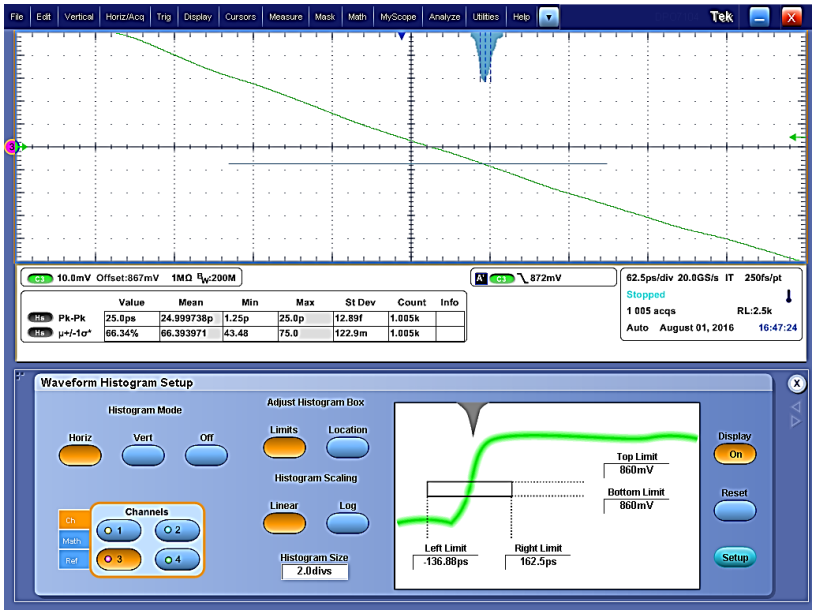


Fig. 4.5. Displayed result on the mobile device.

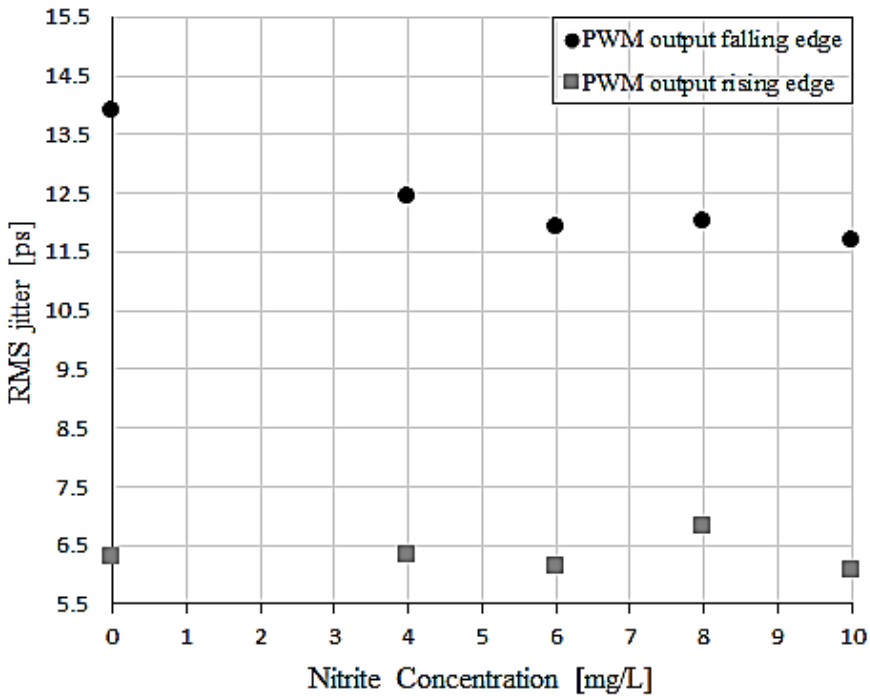
for the wet reagent strip were measured as shown in Fig. 4.4. The BLE module digitizes the PWM signals and transmits them. Fig. 4.5 shows T_{PW1}, T_{PW2}, and the differential pulse width displayed on the mobile device at real-time.

The jitter on rising and falling edge of PWM output signal were measured using a high-speed oscilloscope as shown in Fig. 4.6(a). Fig. 4.6(b) shows the measured jitter on the rising and falling edges of PWM signal in the presence of different nitrite concentrations. As described by equations from (3.6) to (3.11), the falling edge jitter is bigger than the rising edge jitter, and the falling edge jitter is inversely proportional to the nitrite concentrations becasue the active photodiode currents decreases while the rising edge jitter remains constant.

Fig. 4.7 illustrates the differential pulse width versus nitrite concentrations curves for an ideal case simulation and measurements before and after the calibration. We used SPICE simulator to get the simulation results shown in Fig. 4.7. The Inverters and NAND gates of the sensor interface are modeled based on IBIS model provided

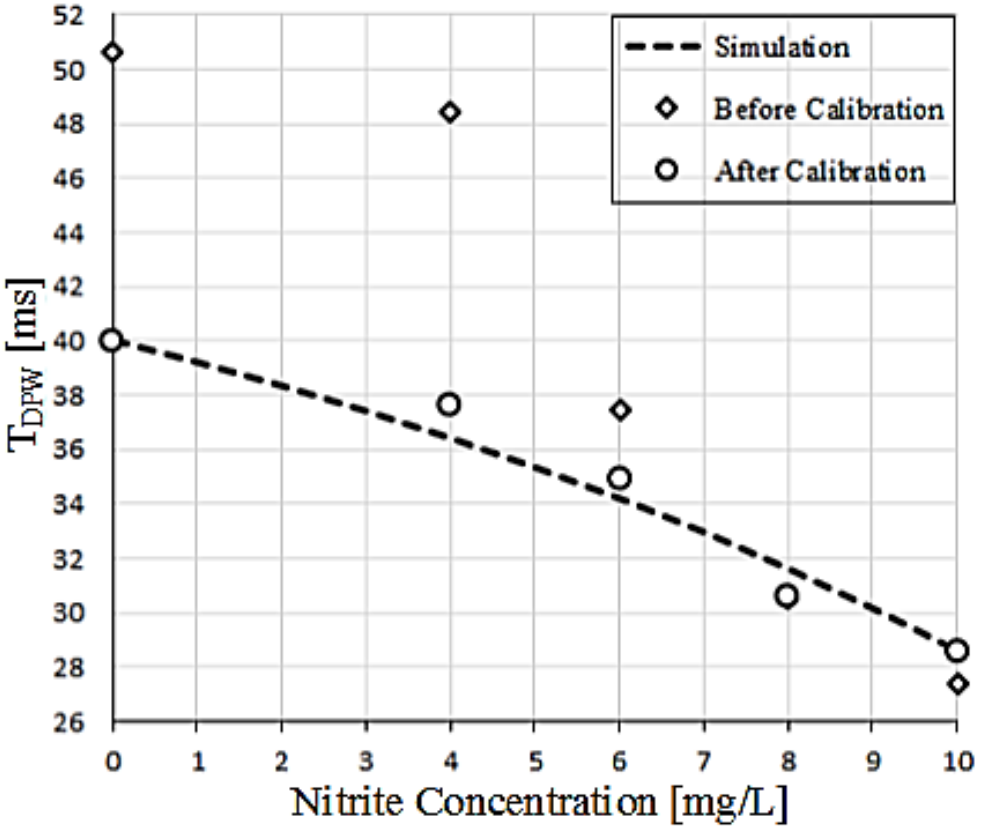


(a)



(b)

Fig. 4.6. (a) Jitter measurement of the PWM output signal falling edge. (b) RMS jitter of rising and falling edges of the PWM output signal versus nitrite concentration.



(a)

(b)

Fig. 4.7. (a) Measured differential pulse width versus nitrite concentrations (b) Conventional dipstick color chart.

by the manufacturer (Texas Instruments). The active photodiode is replaced with a current source and a voltage dependent capacitor connected in parallel. The current which is previously performed studies in [16] is used to model the photodiode current, and the voltage dependent capacitor is implemented using a Verilog-A. As a

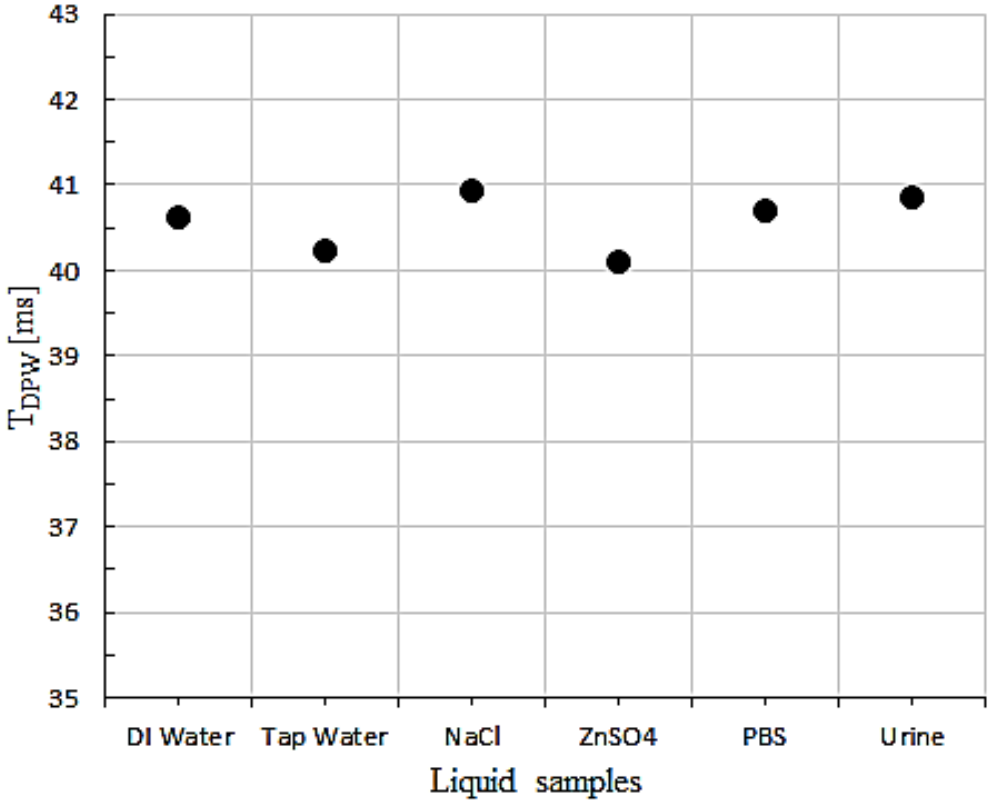


Fig. 4.8. Measured differential pulse width versus liquid samples.

simplification , we assume that the dark current of the active photodiode is canceled out by that of the reference photodiode, and the reference photodiode is modeled as a voltage dependent capacitor. For the measured differential pulse width T_{DPW} before the calibration, the maximum error from the ideal case simulation reaches up to 33%, while the T_{DPW} after the calibration shows a maximum error of 3.5%, which corresponds to almost 10 folds of improvement. The sensor module achieves a sensitivity of 1.35 ms/(mg/L) and a detection limit of 4 mg/L for nitrite. Because nitrite is never found naturally in urine, and many species of gram-negative bacteria convert nitrate to nitrite, the T_{DPW} of urine from a person without UTI will show 40ms. Accordingly, the T_{DPW} of the urine of a person with UTI will be smaller than 40ms, and the difference will increase with increasing amount of nitrite in the urine.

Fig. 4.7(b) shows a reference color chart of typical urine dipsticks designed for nitrite detection. To the untrained eyes, a quantitative analysis on nitrite concentration, beyond the decision on positive or negative, is not feasible for dipsticks. This additional quantitative information can be beneficial for a health information technology. The comparison demonstrates the effectiveness of the proposed autonomous sensing utilizing the developed sensor module.

Fig. 4.8 presents the measured differential pulse width with liquid samples, showing that the differential pulse width changes by 2.03%. Although the urine composition varies among patients, the sensor module should correctly detect only nitrite for UTI. In order to verify the sensor module specificity to nitrite, different types of solutions such as deionized (DI) water, tap water, NaCl of 500mg/L, ZnSO4 of 500mg/L, phosphate-buffered saline (PBS), and fresh urine were used. These experimental results prove that the sensor module can detect nitrite reliably regardless of liquid samples.

4.2 Second sensor module

The second version focused on making the sensor module practical and economical. Fig. 4.9 shows the implementation of the second UTI sensor module. The second sensor module comprises a disposable module and a reusable module due to cost and the environment issue. The disposable module is configured for single-use application and includes a colorimetric sensor module and a battery module. The disposable module may either be embedded in a diaper during the manufacturing process or attached as an added unit to a commercially available diaper. The disposable module is positioned within the diaper at a location conductive to receiving urine. The disposable module is in wired communication with the reusable module placed outside the diaper. The BLE module and the circuitry module are combined into the reusable module on one PCB. The reusable module can removably affixed to the exterior of the diaper either by a user or the patient wearing the diaper.

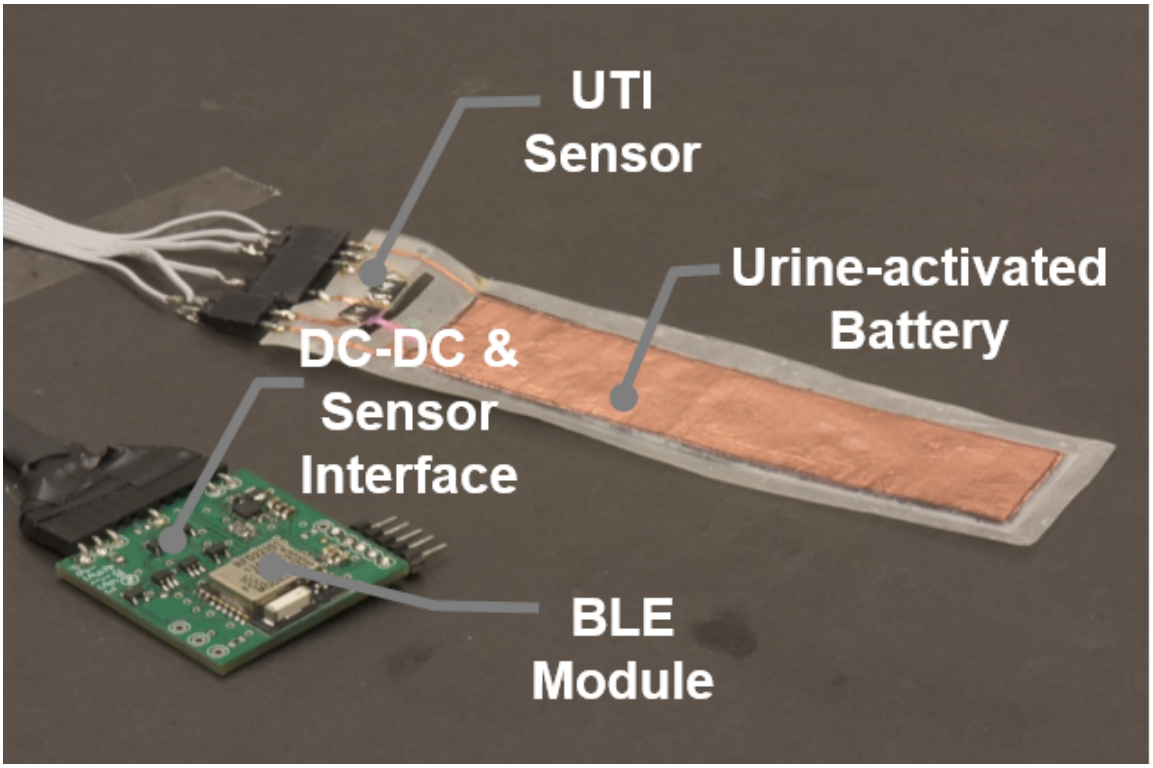
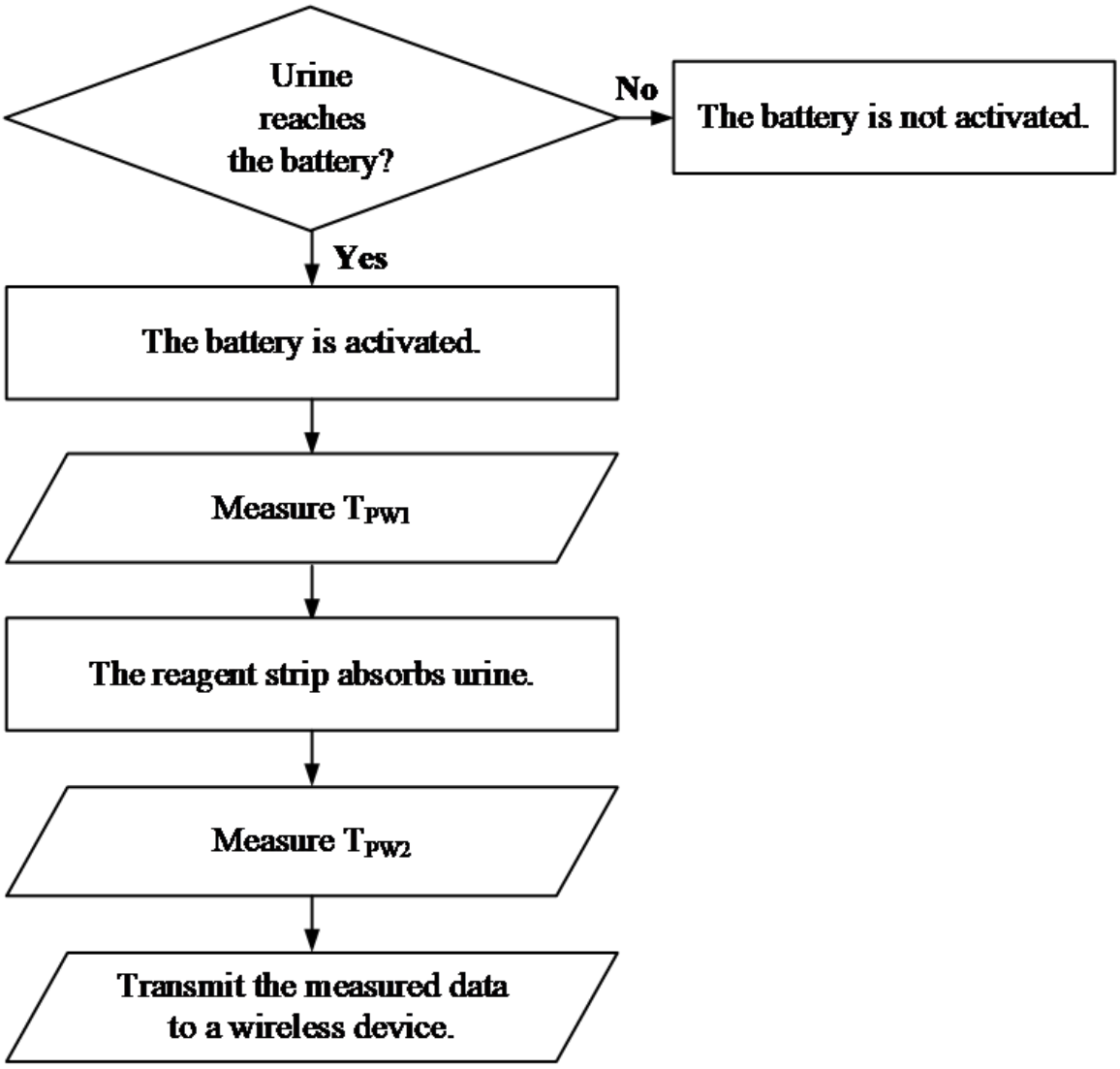
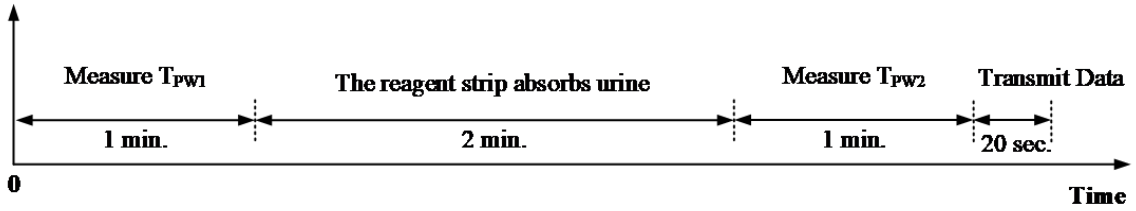


Fig. 4.9. The Second version sensor module



(a)



(b)

Fig. 4.10. (a) Operation flow chart (b) Timing diagram.

There are two main design shortcomings in implementation for this sensor module. The first one is power management. Fig. 4.10(a) shows the flow charts depicting the steps of the operation applied for this module and Fig. 4.10(b) shows a timing diagram associated with the operation. In operation, as soon as urine reaches the urine-activated battery, the battery is activated and provides power to drive performance of the steps in Fig. 4.10(a). The sensor module measures the pulse width T_{PW1} for one minute while the reagent strip is dry. The sensor module waits for two minutes until the urine reaches the reagent strip of the colorimetric sensor and finishes the reaction between urine and the chemical/reagent within the reagent strip. Then, the sensor module measures the pulse width T_{PW2} for one minutes. After 4 minutes, the BLE module transmits the measured data to a nearby mobile device. To calculate the nitrite concentration, both T_{PW1} and T_{PW2} are necessary. In the operation of this sensor module, the sensor module works for four and half minutes to measure two pulse widths and to send data. This method is inefficient in terms of power consumption because during the reaction between urine and the chemical/reagent, the data are unnecessary and the sensor module does not need to work. To solve this problem, the sleep mode function is added to the third version sensor module. Another issue with this sensor module was that the BLE connection in the software was unstable and the mobile app lost some data. This is because the Processing code used in the software is not fully compatible with Android BLE library. This has also has been fixed by moving from Processing code to Android.

4.3 Third sensor module

The third version focused on improving the power efficiency, enhancing the accuracy of the colorimetric sensor module, and stabilizing BLE connection between the sensor module and the mobile device. Fig. 4.11 shows the implementation of the third UTI sensor module. This sensor module comprises a reusable module and a disposable module as in the second version. However, when compared with previ-

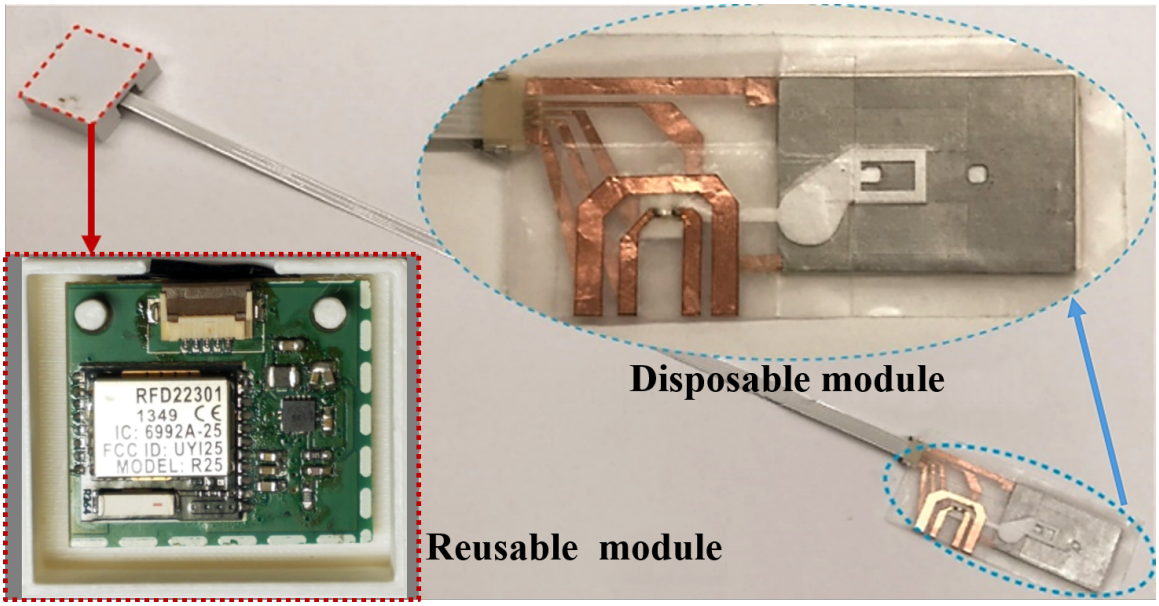


Fig. 4.11. The third version sensor module

ous implementations, the sleep mode is added to this sensor module to reduce power consumption. Fig. 4.12 shows flow charts depicting the steps of the operation applied for this module. When in a sleep mode, the sensor module's functionality is disabled except for the timing controller, which significantly reduces power consumption. Thereafter, the timing controller of the microprocessor is periodically wake the sensor module up between predefined sleep mode intervals to measure the output signal and ensure operation if the reagent strip absorbs urine. Accordingly, where sleep mode is activated, instead of measuring the sensor output signal frequently, the sensor module measures the sensor output at a reduced speed. Between when the measurements are taken, the sensor module is in sleep mode so that only small amounts of power are drawn from the urine-activated battery. With the sleep mode operation, the battery size reduced from 15x3.5cm^2 to 3.5x3.2cm^2.

In previous implementations, the colorimetric sensor module used the reagent strip developed in the lab. The some of the reagent strip changes from white to pink, but the other remains white because the reagent chemicals does not distribute evenly

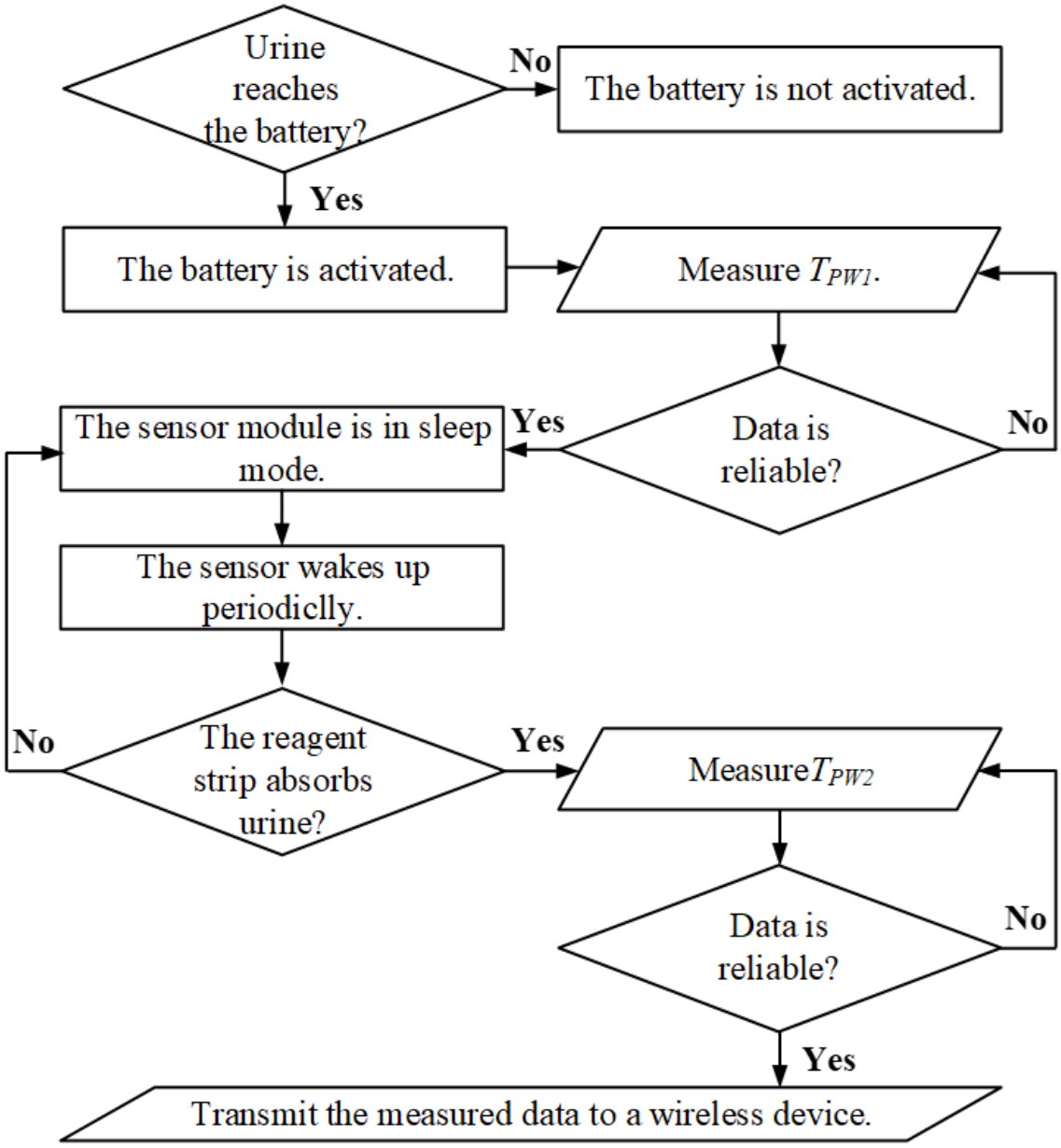
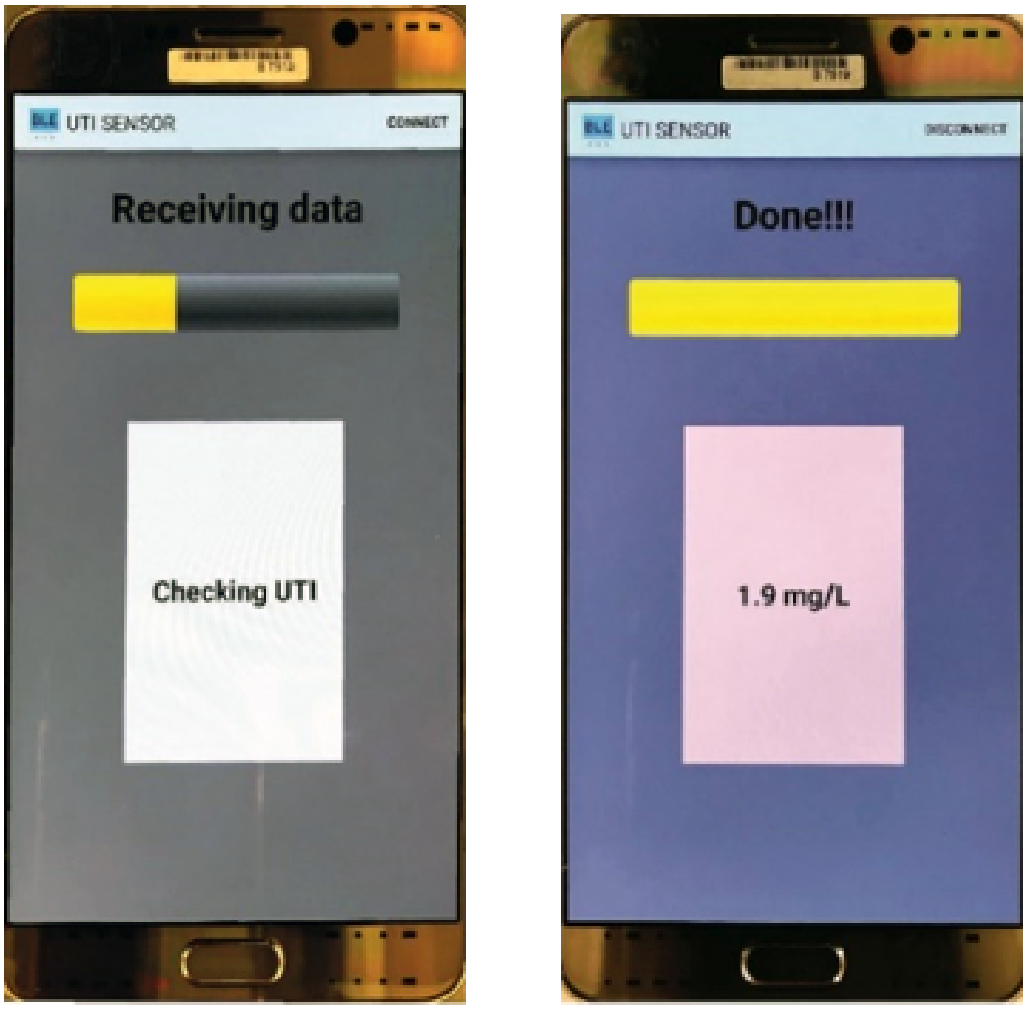


Fig. 4.12. Operation flow chart.

over the strip. The white region in the reagent strip affects the current which the active photodiode generates and causes less accuracy of the sensor module. To solve this issue, from a commercial urine dipstick, the pad containing chemicals that reacts with urine is stripped. The reagent area is replaced with the pad and it improves the accuracy of the colorimetric sensor module.

In addition, a new software is developed with Android to improve BLE connectivity between BLE module and the mobile device. The software installed in a mobile



(a) (b)

Fig. 4.13. Displayed result on the mobile device (a) Receiving data. (b) Nitrite concentration after the calibration.

device performs quantitative analysis and shows the final results in real time as shown in Fig. 4.13. Fig. 4.13(a) displays the progress of the sensor module's operation and Fig. 4.13(b) exhibit the final nitrite concentration after calibrating the received data.

The measurement setup used for the sensor module is shown in Fig. 4.14. The disposable module wrapped with a black insulation tape to block the ambient light source is embedded into a diaper as shown Fig. 4.14(a). The reusable module is placed on the outside of the diaper and connected to the disposable module through a flexible flat cable (FFC). Fig. 4.14(b) displays the data which the mobile device receives and Fig. 4.14(c) exhibit the nitrite concentration after calibration.

Fig. 4.15 illustrates the reading nitrite concentration versus synthetic urine samples with nitrite concentrations of 0mg/L, 2.5mg/L, 5mg/L, 7.5mg/L, 10mg/L, and 12.5mg/L for an ideal case, this work, HI96708 [17], HI-764 [18]. We used HI96708 for high range nitrite concentration and HI-764 for low range nitrite concentration. For the measured nitrite concentration of HI96708, the maximum error reaches up to 60%, while this work shows a maximum error of 27%, which corresponds to almost 2.2 folds of improvement. Dipstick test can tell only positive or negative based on the changes in the color, and cannot provide a quantitative UTI data.

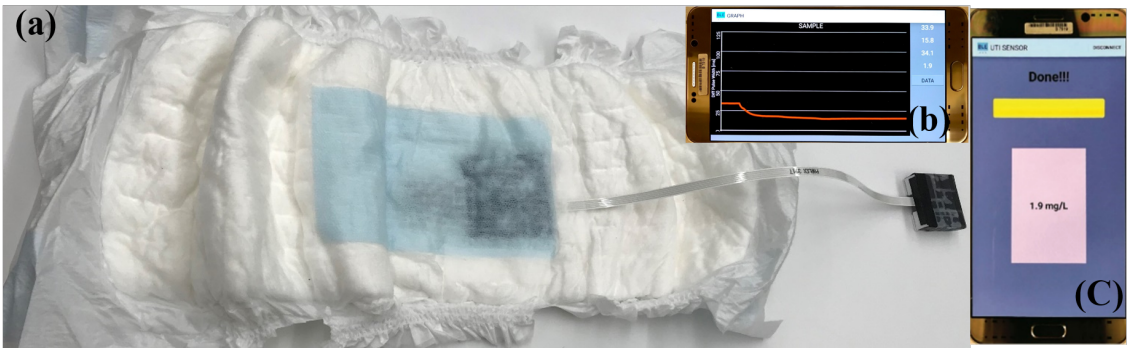


Fig. 4.14. Measurement set-up. (a) The reusable module embedded into the diaper and disposable module placed on the outside of the diaper (b) Measured data (c) Nitrite concentration after the calibration

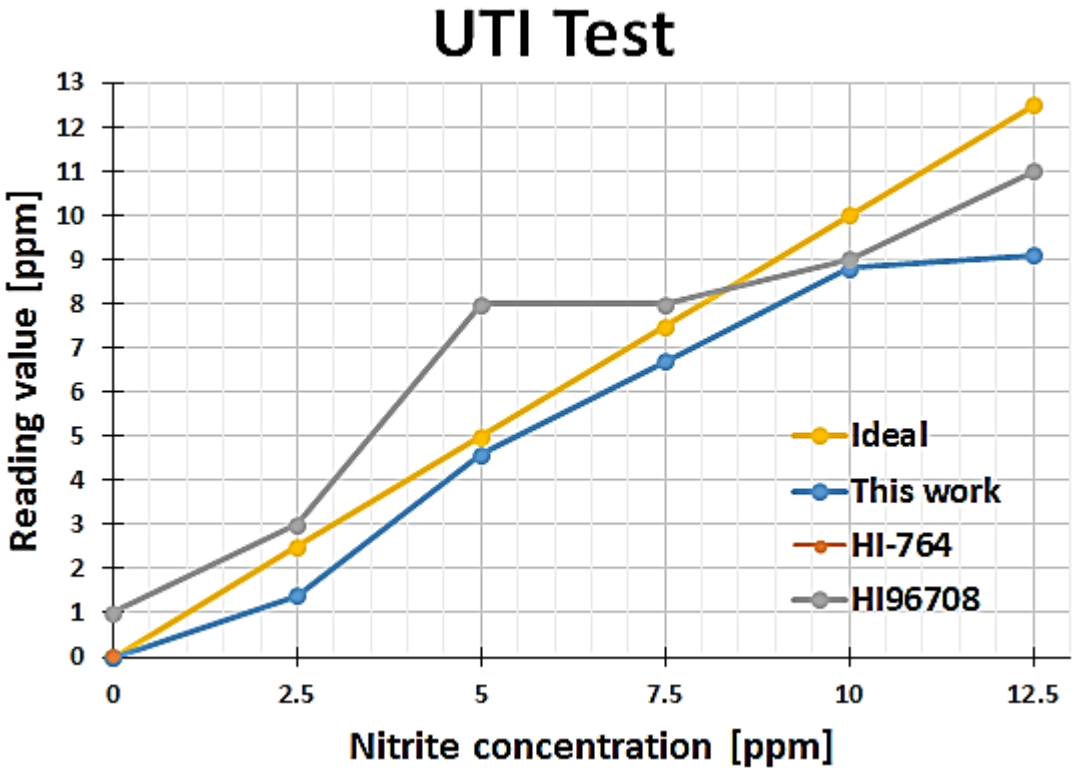


Fig. 4.15. Measured nitrite concentration versus nitrite concentrations.

Nitrite [ppm]	0	2.5	5	7.5	10	12.5
This work [ppm]	0	1.4	4.6	6.7	8.8	9.1
HI96708 [ppm]	1	3	8	8	8	11
HI-764 [ppm]	0.13					
Dipstick	-	+	+	+	+	+

Table 4.1.
Performance comparison

Table 4.2 shows a comparison of this sensor module with other system. This work achieves the lower detection limit of 0.6ppm, which is slightly defective compared to other systems. However, this work can be fully embedded in a diaper without

	This work	Dipstick	Camera-assisted system
Lower detection limit	< 0.6[ppm]	0.5[ppm]	0.5[ppm]
Time	Instant	two minutes	Unpredictable time
Diaper embedding	Inside	NA	On the diaper skin
User intervention	None	Collect urine sample. Dip, wait, and read color chart	Check wet diaper Image capture and send it
Privacy issue	No	Yes	Yes
Production cost	Low	Very low	Low

Table 4.2.
Comparison with other systems

hindering accurate sensing. Camera-based system requires the sensor to be attached to the skin of a diaper. When it is attached to the human body side, it can be easily contaminated (ex: by stool). When it is attached to the outside, the urine must leak to outside of the diaper. When it is embedded in a diaper, a de-embedding step is required before tacking pictures.In addition, other systems are time-sensitive and their test has to be processed timely to be diagnostically significant.

4.4 Summary

This work reports a diaper-embedded UTI monitoring sensor module self-powered by urine-activated batteries. The sensor module can detect UTIs autonomously and transmit the data to a caregivers mobile device that is presumably connected to a health care network, allowing a reliable early detection and screening of UTI with minimal efforts. The sensor module consists of a paper-based colorimetric nitrite sensor, urine-activated batteries, a boost DC-DC converter, a low-power PWM sensor

interface, and a BLE module. The urination-event driven wakeup method allows the proposed sensor module to be compact, power efficient and reliable. The sensor interface utilizing the PWM method significantly reduces the circuit complexity and the power consumption, which is attractive for self-powered applications with a limited power budget. The binary two level nature of the PWM sensor interface output is also attractive for wireless transmission over noisy environment. The time lapse based differential reading technique and the on-line calibration utilizing a known reference significantly mitigate the adverse effects of process variations in the components without increasing the system complexity and power consumption. With the calibration, the maximum error in nitrite concentration estimation has improved from 33% to 3.5%. When compared to the commercial device of HI96708, the performance of this work has improved from 60% to 27%. The sensor module achieves a lower detection limit of 0.6 ppm for nitrite concentration.

5. A FULLY INTEGRATED AND REGULATED CHARGE PUMP

Recent advancements in health monitoring and sensing technologies have enabled a plethora of new biomedical applications utilizing a variety of wearable and implantable devices. One example is a diaper-embedded urinary tract infection (UTI) monitoring device presented in [19] and Fig. 5.1 shows a block diagram of the UTI sensor module that utilizes a urine-activated battery. The diaper-embedded UTI sensor module consists of a urine-activated battery, a DC-DC converter, a voltage doubler, a paper-based colorimetric UTI sensor, a low-power sensor interface utilizing pule width modulation (PWM), and a wireless data transmission module. Like many other wearable biomedical devices, self-powering is crucial for autonomous operation, and the UTI sensor module utilizes a thin disposable urine-activated battery fabricated on a flexible substrate [10]. The same battery can be activated by sweat for band-aid-like disposable sensor patch devices [10].Once activated by urine, the battery powers the UTI sensor module for a few minutes, but its output voltage drops from 0.86V to 0.66V over a period of about five minutes [10]. In order to ensure that

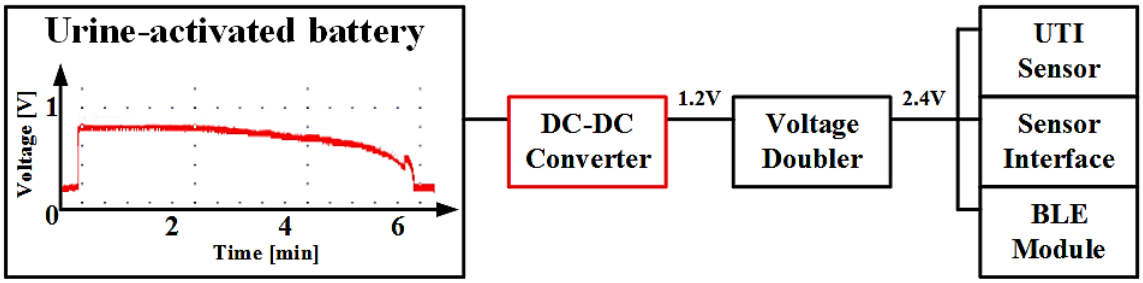


Fig. 5.1. A UTI sensor module

the UTI sensor module functions reliably, a DC-DC converter is required to boost the battery voltage and provide a regulated output voltage to its load. In addition to a high conversion efficiency, the DC-DC converter should provide a low output voltage ripple and ripple variation in the face of varying battery voltages. Low output voltage ripple and ripple variation is particularly important for an analog sensor interface circuitry with a relatively poor power supply rejection ratio (PSRR), and it is not uncommon that analog sensor interfaces, such as the PWM-based interface used in [19], compromise PSRR for low-power. Another important design parameter for wearable biomedical devices is form factor. The UTI monitoring module presented in [19] utilized an off-the-shelf inductive DC-DC converter with off-chip inductors, which is not suitable for a fully diaper embedded design because of its relatively large footprint and high profile. This work presents a fully integrated DC-DC converter optimized for the urine- or sweat-activated batteries presented in [10]. The converter that provides a low output voltage ripple and ripple variation can be used without any off-chip capacitor or with just one optional off-chip load capacitor to further suppress its output ripple if required. Its small foot-print and low-profile makes it suitable for wearable applications such as diaper-embedded and band-aid-like patch devices.

5.1 Existing Designs and Proposed Design

There are two methods of implementing fully integrated DC-DC converters. One is a fully integrated inductive converter [20], [21] and the other one is a fully integrated capacitive converter [22]. Inductor based fully integrated DC-DC converters require costly additional fabrication steps involving thick metals and integrated magnetic materials [20], [23]. They also suffer from the high series resistance and low energy density, thereby increasing chip area and reducing the efficiency of the DC-DC converters [24]. On the other hand, integrated capacitive DC-DC converters can potentially achieve a low series resistance and high energy density without any additional fabrication steps in the current CMOS process [25]. Many wearable biomedical

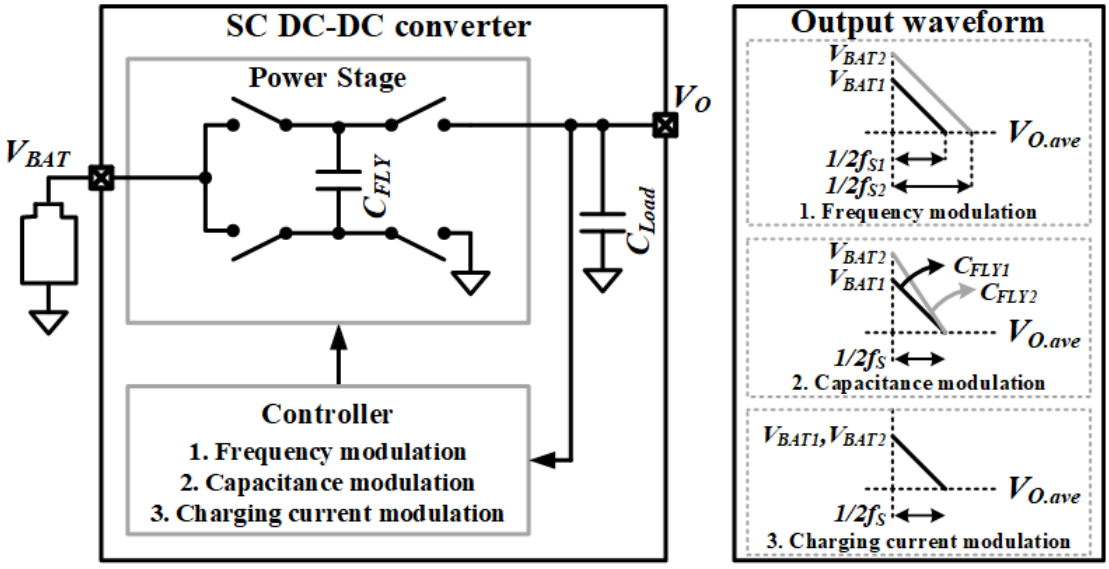


Fig. 5.2. A block diagram and output waveform of a regulated capacitor converter

sensing devices, including the aforementioned diaper-embedded UTI sensing module, are disposable where low-cost is one of the most important design parameters. For this reason, this work focuses on fully integrated capacitive DC-DC converters

Although fully integrated capacitive DC-DC converters have certain advantages, a relatively large output voltage ripple and ripple variation, among others, largely remains as a challenge. Fig. 5.2 shows a block diagram of a typical regulated switched-capacitor (SC) converter which consists of a power stage and a controller. Adaptively controlled by the controller unit, the power stage provides a regulated output voltage V_O, over a certain range of the battery voltage V_{BAT}. A few different output voltage regulation techniques have been proposed including frequency modulation [26], [27], [28]], capacitance modulation [29], [30]], and charging current modulation [31], [32], [33]. The frequency modulation and the capacitance modulation utilize a similar mechanism which controls the output voltage ripple to regulate the output voltage. The former modulates the switching frequency f_S and the latter modulates the capacitance of the flying capacitor C_{FLY} in the face of the varying battery voltage

V_{BAT}. In both cases, the average output voltage $V_{O.ave}$ and the output voltage ripple ΔV_O are given by

$$V_{O.ave} = CG \cdot V_{BAT} - \frac{\Delta V_O}{2} \tag{5.1}$$

$$\Delta V_O = \frac{I_O}{(C_{LOAD}+C_{FLY})f_S} \tag{5.2}$$

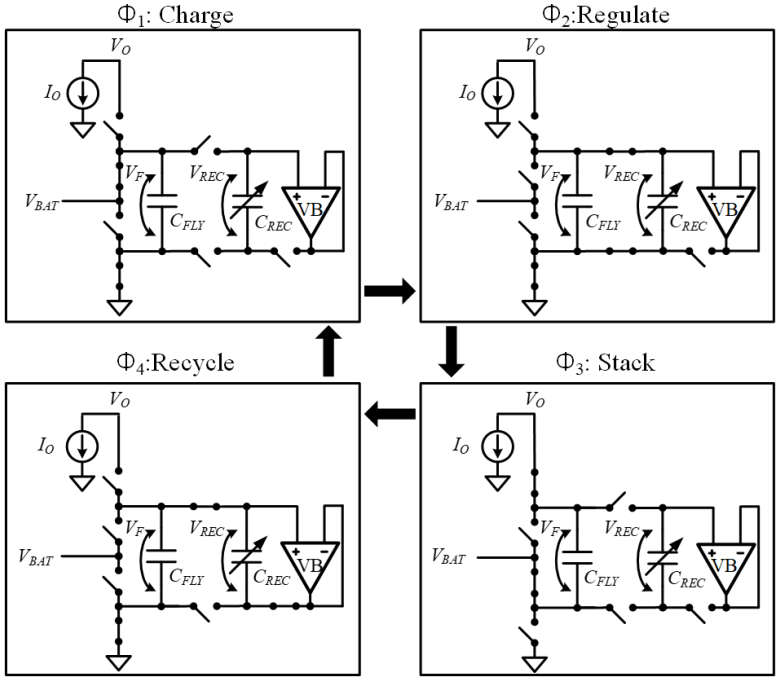
where CG is the conversion gain, C_{LOAD} is the output load capacitor, and I_O is the output current. Although these approaches provide a regulated average output voltage, the main disadvantage of controlling the output voltage through f_S and C_{FLY} is that the output voltage ripple is dependent on V_{BAT}.For example, if V_{BAT} increases, f_S and C_{FLY} should be decreased to to generate the targeted constant average output voltage $V_{O.ave}$ by increasing ΔV_O as shown in equations (5.1) and (5.2), and in the output waveforms of Fig. 5.2. This variation in the output voltage ripple is detrimental for many sensor interface applications, and often results in a stringent requirement on the power supply noise rejection. To mitigate this voltage ripple variation issue, the load capacitor C_{LOAD} must be selected based on the worst-case output voltage ripple and usually occupies a large area. Increasing C_{LOAD} is particularly challenging for fully integrated capacitive DC-DC converters because of limited die area. Another proposed approach is charging current modulation [31], [32], [33].This method regulates the amount of charge that is transferred from the battery V_{BAT} to the flying capacitor C_{FLY}. This is achieved by controlling the capacitor-charging current using a voltage-controlled-current-source (VCCS). Although the charging current modulation provides a fixed output voltage ripple as shown in Fig. 5.2, this technique requires a high-performance amplifier to generate an accurate intermediate voltage for the VCCS [32], [33]. Also, the high-precision amplifier typically has a multistage topology that increases the power consumption of the controller unit [34]. In addition, this design is prone to instabilities due to the multiple poles of the control loop [35].

This dissertation proposes a new fully integrated and regulated charge pump incorporating an adaptively controlled auxiliary capacitor C_{REC} and a charge recycling technique. The proposed charge pump utilizes the charge redistribution between the flying capacitor C_{FLY} and the adaptively controlled recycling capacitor C_{REC} to

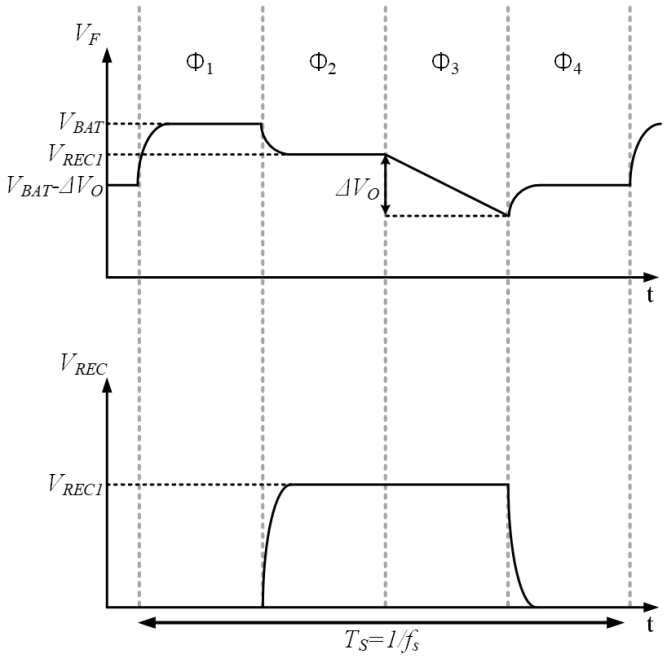
regulate the output voltage. Because the switching frequency f_S and the flying capacitor size C_{FLY} are fixed, unlike the existing frequency or capacitance modulation approaches, the proposed design can provide an output voltage ripple independent of the input battery voltage C_{BAT}. Also, because the switching frequency f_S can be independently selected, it can be easily optimized to minimize the output ripple without using an excessively large load capacitor C_{LOAD}. Although the extra switching operation required for the charge redistribution results in an extra loss, the charge recycling operation compensates the loss and the core conversion efficiency of the proposed design does not degrade compared with the existing designs. To achieve a minimal output voltage ripple, the proposed design adopts a time interleaving technique utilizing sixteen sub-converters that are grouped into four switched-capacitor (SC) sub-modules where each sub-module has four sub-converters. Exploiting the fact that the charge redistribution and recycling sequences of the four sub-converters in each sub-module do not overlap in the interleaved operation, the recycling capacitor and control circuit are shared among the four sub-converters. The sharing technique allows to further reduce the chip area and the power consumption in the controller unit.

5.2 Operation Principle, Efficiency, And Ripple

Fig. 5.3 depicts the operation sequence of the proposed charge pump and the voltage waveforms of the flying capacitor C_{FLY} and the recycle capacitor C_{REC} in steady state. The proposed charge pump sequentially and repeatedly operates in four phases: charge regulate stack recycle. The key concept of the proposed charge pump is regulating the charge stored in the flying capacitor C_{FLY} through a charge redistribution utilizing an adaptively controlled auxiliary capacitor C_{REC} to obtain regulation of the output voltage V_O, and then, instead of dumping the charge stored in the auxiliary capacitor C_{REC}, recycling the remaining charge stored in C_{REC} for the next charge phase.



(a)



(b)

Fig. 5.3. (a) Operation of the proposed technique at each phase (b) voltage waveforms of the flying capacitor and the recycle capacitor

During the charge phase Φ_1, C_{FLY} is connected between the battery and the ground. C_{FLY} is fully charged to the battery voltage V_{BAT} at the end of this phase. C_{REC} does not store charge and thus the voltage V_{REC} across C_{REC} shows 0V during this phase. To regulate the output voltage against the varying battery voltage V_{BAT}, during the regulate phase Φ_2, C_{FLY} and C_{REC} are connected in parallel with initial voltages V_{BAT} and 0V, respectively. Once connected, the charge is redistributed between C_{FLY} and C_{REC}. The excess charge of C_{FLY} is transferred to C_{REC}, therefore the voltage V_F across C_{FLY} decreases and V_{REC} increases. The capacitance of C_{REC} is adaptively controlled based on the output voltage V_O to determine the amount of excess charge transferred to C_{REC} and thus regulate V_F during Φ_2. After the charge redistribution between C_{FLY} and C_{REC} completes, V_F and V_{REC} becomes the same as V_{REC1}

$$V_{REC1} = V_F = V_{REC} = \frac{C_{FLY} V_{BAT}}{C_{FLY} + C_{REC}} \tag{5.3}$$

which is a function of C_{REC}. During the stack phase Φ_3, C_{FLY} is connected between V_{BAT} and V_O, and the proposed charge pump provides a boosted and regulated output voltage. The maximum output voltage $V_{O.max}$ and the average output voltage $V_{O.ave}$ can be described as follows:

$$\begin{aligned} V_{O.max} &= V_{BAT} + V_F \\ &= V_{BAT} + \frac{C_{FLY}}{C_{FLY} + C_{REC}} V_{BAT} \\ &= (1 + \frac{C_{FLY}}{C_{FLY} + C_{REC}}) V_{BAT} \end{aligned} \tag{5.4}$$

$$\begin{aligned} V_{O.ave} &= V_{O.max} - \frac{\Delta V_O}{2} \\ &= (1 + \frac{C_{FLY}}{C_{FLY} + C_{REC}}) V_{BAT} - \frac{I_O}{8 f_S C_{FLY}} \end{aligned} \tag{5.5}$$

Equation (5.4) shows that the voltage conversion gain of the proposed charge pump is $1+C_{FLY}/(C_{FLY}+C_{REC})$ which can be modulated by adaptively controlling C_{REC} against the varying V_{BAT}. For example, if V_{BAT} decreases, C_{REC} decreases and the conversion gain increases, which allows the output voltage regulation through a simple capacitance tuning based negative feedback. Dumping the charge transferred to

C_{REC} during phase Φ_2 would deteriorate its power conversion efficiency significantly. Instead, the charge stored in C_{REC} is transferred to C_{FLY} during the recycle phase Φ_4 using a voltage buffer VB and is recycled during the next charge phase. The proposed technique regulates the charge stored in C_{FLY} in the face of different V_{BAT} regardless of the switching frequency f_S and the flying capacitance C_{FLY}. By adopting a constant switching frequency f_S and a constant flying capacitance C_{FLY}, the design can provide a fixed and regulated amount of charge delivered to the load, and also a regulated output voltage ripple in the face of the varying input battery voltage V_{BAT}.

Compared with conventional topologies, the proposed charge pump requires two additional phases to regulate and recycle the charge, and the switching loss during the additional switching operations would adversely affect its conversion efficiency. To quantitatively estimate the effect of the charge redistribution and the charge recycling, the intrinsic switched-capacitor loss of the proposed charge pump is compared with that of a conventional charge pump utilizing switching frequency modulation. The voltage waveform of the flying capacitor in the conventional charge pump is illustrated in Fig. 5.4 where ΔV_{O_con} is modulated according to the varying V_{BAT} to regulate the output voltage. The flying capacitor is discharged to V_{BAT}-ΔV_{O_con} at the beginning

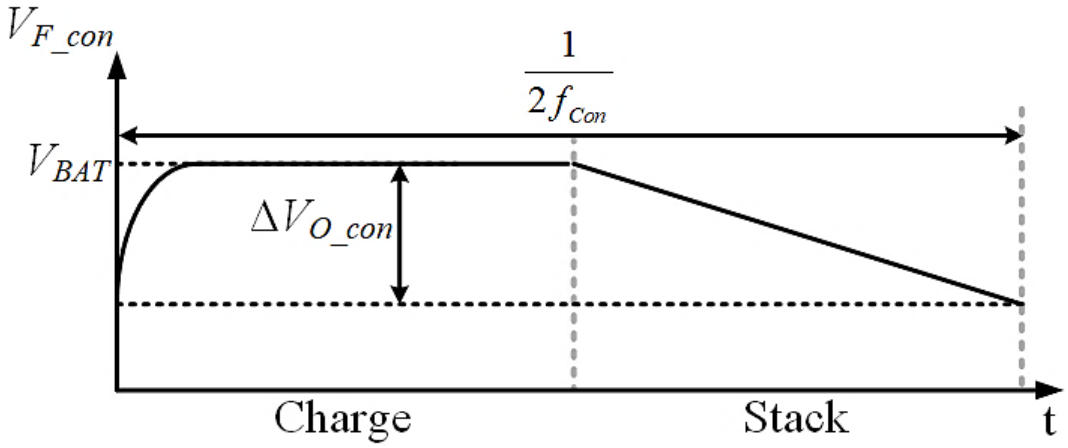


Fig. 5.4. Waveform of the flying capacitor in the voltage doubler with the adaptive control of the switching frequency

of the charge phase and is eventually charged to V_{BAT} at the end of the charge phase. The average output voltage of the proposed charge pump and the conventional charge pump are the same and is given as

$$\begin{aligned} V_{O.ave} &= (1 + \frac{C_{FLY}}{C_{FLY} + C_{REC}})\, V_{BAT} - \frac{\Delta V_O}{2} \\ &= 2\, V_{BAT} - \frac{\Delta V_{O\_con}}{2} \end{aligned} \tag{5.6}$$

Solving equation 5.6 gives

$$\Delta V_{O\_con} = \frac{2 C_{REC}}{C_{FLY} + C_{REC}} V_{BAT} + \Delta V_O \tag{5.7}$$

During the charge phase of the conventional charge pump, the intrinsic switched-capacitor loss P_{L_con} can be written as

$$\begin{aligned} P_{L\_con} &= \frac{C_{FLY} \Delta {V_{O\_con}}^2}{2} \cdot 2 f_{con} \\ &= (\frac{C_{REC}}{C_{FLY} + C_{REC}} V_{BAT} + \frac{\Delta V_O}{2}) I_O \end{aligned} \tag{5.8}$$

For the proposed design, we need to consider the losses in three phases: charge, regulate, and recycle phases. The flying capacitor of the proposed charge pump is discharged to V_{BAT}-ΔV_O at the end of Φ_4 and is eventually charged to V_{BAT} at the end of Φ_1 as illustrated in Fig. 5.3. The power P_1 dissipated during the charging of the flying capacitor in Φ_1 is given as

$$P_1 = \frac{1}{2} C_{FLY} \Delta {V_O}^2 \cdot 4 f_S \tag{5.9}$$

To regulate the output voltage, the proposed charge pump regulates the amount of the charge in the flying capacitor during Φ_2 through charge redistribution and the switching loss P_2 during this charge redistribution is

$$P_2 = \frac{1}{2} (C_{FLY} \parallel C_{REC})\, {V_{BAT}}^2 \cdot 4 f_S \tag{5.10}$$

At the beginning of Φ_4, the energy $E_{initial}$ of C_{FLY} and C_{REC} is

$$E_{initial} = \frac{1}{2} C_{FLY} (V_{REC1} - \Delta V_O)^2 + \frac{1}{2} C_{FLY} {V_{REC1}}^2 \tag{5.11}$$

At the end of Φ_4, the energy E_{final} is

$$E_{final} = \frac{1}{2} C_{FLY} (V_{BAT} - \Delta V_O)^2 \tag{5.12}$$

, and the dissipated power P_3 during Φ_4 is

$$\begin{aligned} P_3 &= (E_{initial} - E_{final}) 4 f_S \\ &= (\frac{C_{FLY} C_{REC}}{C_{FLY} + C_{REC}} V_{BAT} \Delta V_O - \frac{1}{2} \frac{C_{FLY} C_{REC}}{C_{FLY} + C_{REC}} {V_{BAT}}^2) 4 f_S \end{aligned} \tag{5.13}$$

The intrinsic switched-capacitor loss P_L of the proposed charge pump is the sum of P_1, P_2, and P_3, and is given as

$$\begin{aligned} P_L &= P_1 + P_2 + P_3 \\ &= (\frac{C_{REC}}{C_{FLY} + C_{REC}} V_{BAT} + \frac{\Delta V_O}{2}) I_O \end{aligned} \tag{5.14}$$

Equations (5.8) and (5.14) show that the intrinsic switched-capacitor losses of the proposed design and the conventional design are the same despite the fact that the proposed charge pump has additional power losses during the regulate and the recycle phases. This is because the flying capacitor of the proposed charge pump is charged in two steps: partially charged during the recycle phase and fully charged during the charge phase. This two-step charging has a less power loss than the one-step charging of the conventional charge pump. The reduced loss during the charge phase compensates the additional losses and the total loss becomes the same with that of the conventional designs. The conversion efficiency η of the proposed design can be described as

$$\begin{aligned} \eta &= \frac{P_O}{P_O + P_L} \\ &= \frac{V_{O.ave} I_O}{(V_{O.ave} + \frac{\Delta V_O}{2} + \frac{C_{REC} \cdot V_{BAT}}{C_{FLY} + C_{REC}}) I_O} \\ &= \frac{V_{O.ave}}{2 V_{BAT}} \end{aligned} \tag{5.15}$$

[36] presented the conversion efficiency of a conventional converter utilizing frequency modulation, and the formula is identical with equation (5.15). Despite the need for additional switching operation, the proposed charge pump can achieve the same level

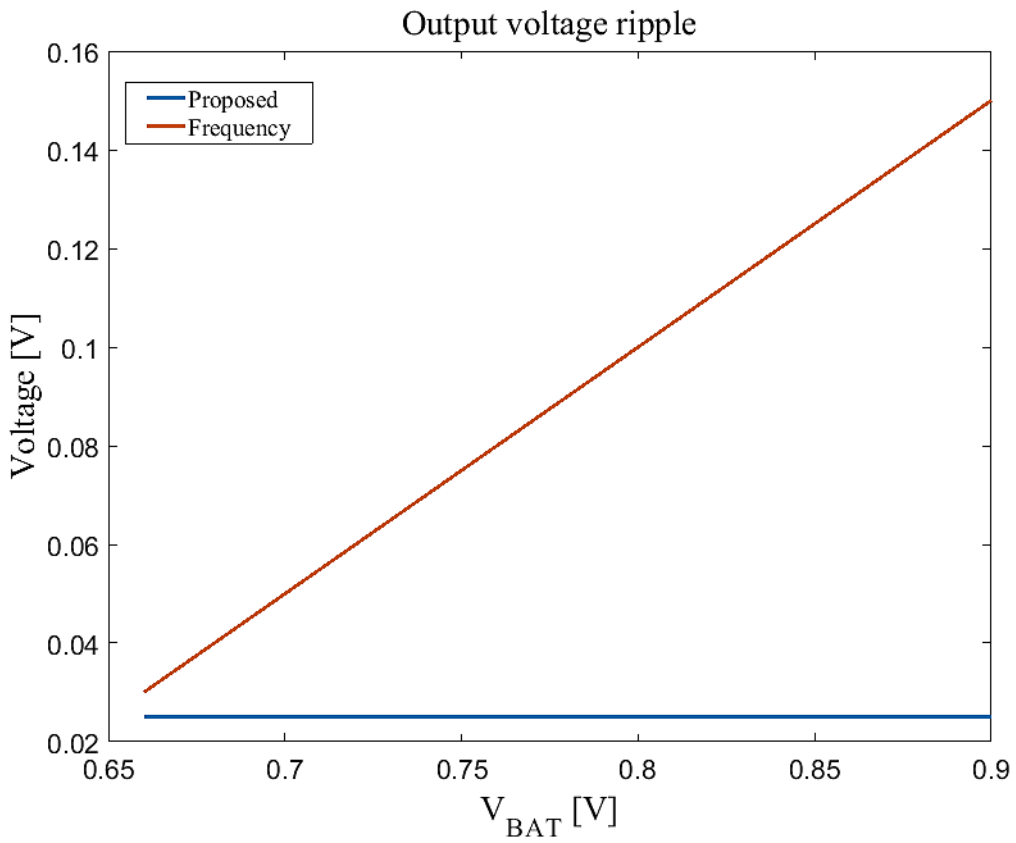


Fig. 5.5. Output voltage ripple

of conversion efficiency compared with conventional designs largely because of the proposed charge recycling scheme.

Because the proposed charge pump uses a fixed switching frequency, equation (5.2) can be used as it is to describe its output voltage ripple ΔV_O. The flying capacitor C_{FLY} of the conventional switching frequency modulation based charge pump is shorted to the load capacitor C_{LOAD} at the beginning of the stack phase and the charge redistribution between C_{FLY} and C_{LOAD} occurs. The relationship of the charge redistribution can be written as

$$\begin{aligned} C_{Load}V_O + C_{FLY}V_{BAT} = C_{FLY}(V_O + \Delta V_{O\_con} - V_{BAT}) \\ + C_{Load}(V_O + \Delta V_{O\_con}) \end{aligned} \tag{5.16}$$

Solving equation (5.16), The output voltage ripple of ΔV_{O_con} can be shown as

$$\Delta V_{O\_con} = \frac{C_{FLY}}{C_{FLY} + C_{Load}}(2 V_{BAT} - V_O) \tag{5.17}$$

Fig. 5.5 shows the simulated output ripples of the proposed charge pump and the conventional switching frequency modulation based charge pump. For fair comparison, the same flying capacitor C_{FLY} of 2.5nF and the same load capacitor C_{LOAD} of 0.5nF are used for both. The proposed design uses an extra capacitor C_{REC} of 1.2nF. The load current and the output voltage used for the simulation are 5mA and 1.2V, respectively. The switching frequency of the proposed charge pump is fixed at 5MHz while the switching frequency of the converntional design varies from 4.2MHz to 0.8MHz depending on the input battery voltage. The proposed charge pump provides a constant output voltage ripple, but the output voltage ripple of the conventional charge pump shows a strong dependency on V_{BAT}. For the conventional design, because of the large output voltage ripple variation, the size of the load capacitor C_{LOAD} must be selected based on the worst-case output voltage ripple. Equation (5.17) shows that, to reduce the worst-case output voltage ripple of the conventional design to the level of the proposed design, the load capacitor C_{LOAD} must be about four times larger than the flying capacitor C_{FLY}. In other words, the proposed design can provide a small worst-case output voltage ripple by adding a small auxiliary recycle capacitor C_{REC} instead of using an excessively large output load capacitor. This high area-efficiency of the proposed design makes it attractive for the implementation of fully integrated DC-DC converters.

5.3 Implementation

The proposed fully integrated and regulated charge pump was implemented in a TSMC 65nm CMOS technology with a MIM option. Fig. 5.6 shows a chip microphotograph of the implemented charge pump. The total flying capacitance is 2.2nF, the total recycle capacitance is 1nF, and the total load capacitance is 380pF. The flying, recycle, and load capacitors occupy most of the area, and the die area including all

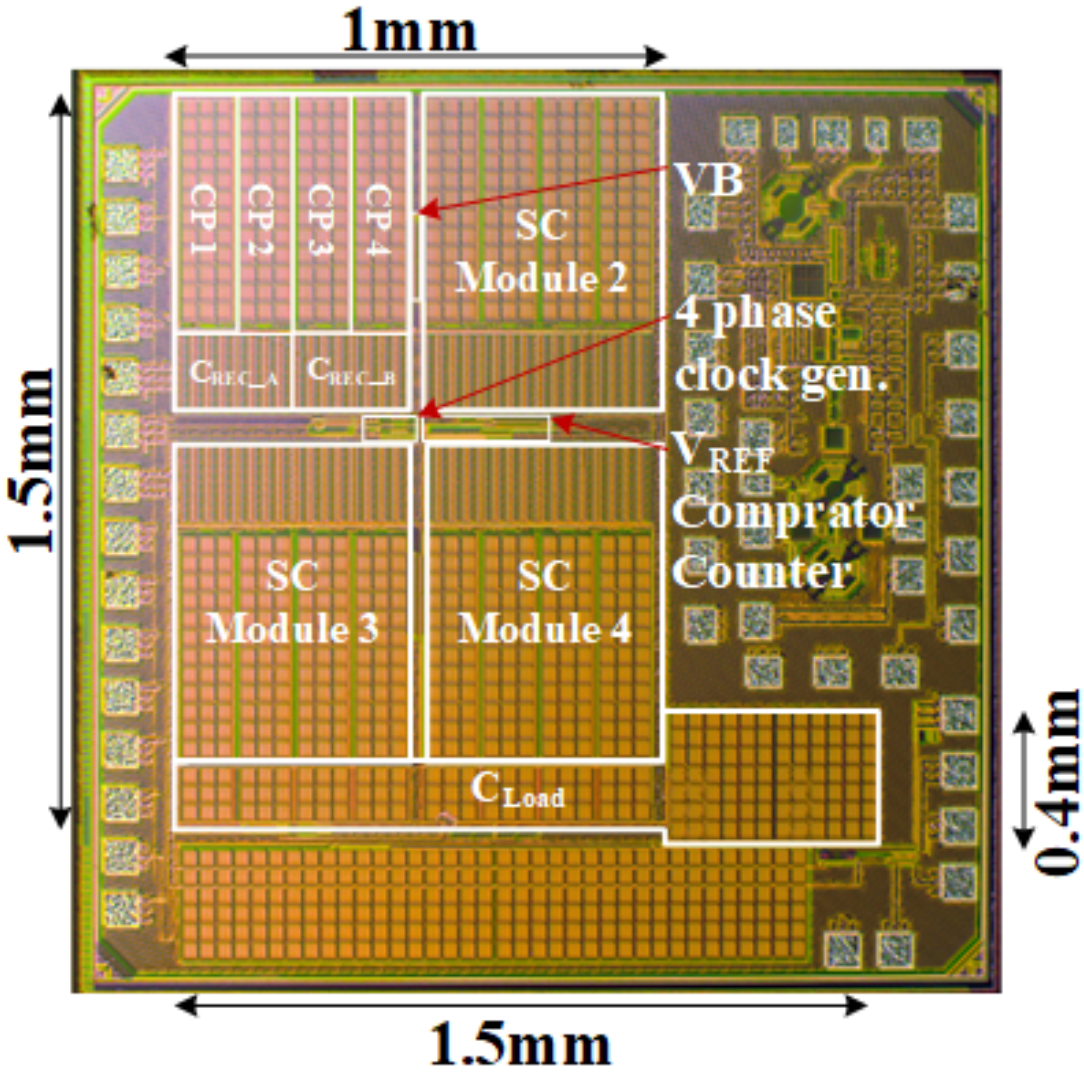


Fig. 5.6. Microphotograph of the proposed charge pump

capacitors is 1.7mm^2. The capacitors were implemented using MIM and MOS transistors. The die area can be further reduced using dual-MIM capacitors if required.

5.3.1 Sharing sub-blocks

To reduce the output voltage ripple, the proposed charge pump uses a sixteen time interleaving topology utilizing sixteen flying capacitors. Nominally, each flying capacitor needs to be paired with its own recycle capacitor and a voltage buffer (VB) requiring sixteen recycles capacitors and sixteen voltage buffers for a sixteen interleaving operation. To reduce the number of recycle capacitors and the voltage buffers, and hence reduce the chip area and the power consumption, the proposed design utilized sub-module sharing techniques.

Since the operation of the proposed design repeats four phases, four interleaved unit-converters can be grouped as a sub-module, and the four phases of the four unit-converters can be shifted to avoid overlapping. Because the voltage buffer is active only during the recycle phase and the recycle phases of the four unit-converters do not overlap, the four unit-converters can share a voltage buffer. Fig. 5.7 shows a configuration where four unit-converters with non-overlapping phases share a voltage buffer used for charge recycling. Consequently, for the proposed sixteen interleaving design, only four voltage buffers are required instead of sixteen, which reduces power consumption and area.

We also note that since the recycle capacitors are required only during the regulate and the recycle phases and the phases of the four unit-converters in a sub-module do not overlap, the charge stored in a recycle capacitor C_{REC} during a regulate phase of a unit-converter can be transferred to the C_{FLY} of another unit-converter during its own recycle phase. Fig. 5.8 shows a configuration designed to share two recycle capacitors C_{REC_A} and C_{REC_B} among four unit-converters. Fig. 5.9 depicts the switching sequence of C_{REC_A} and its voltage waveform in steady state during one cycle. C_{FLY} of unit-converter 1 is connected to C_{REC_A} and the excess charge in C_{FLY}

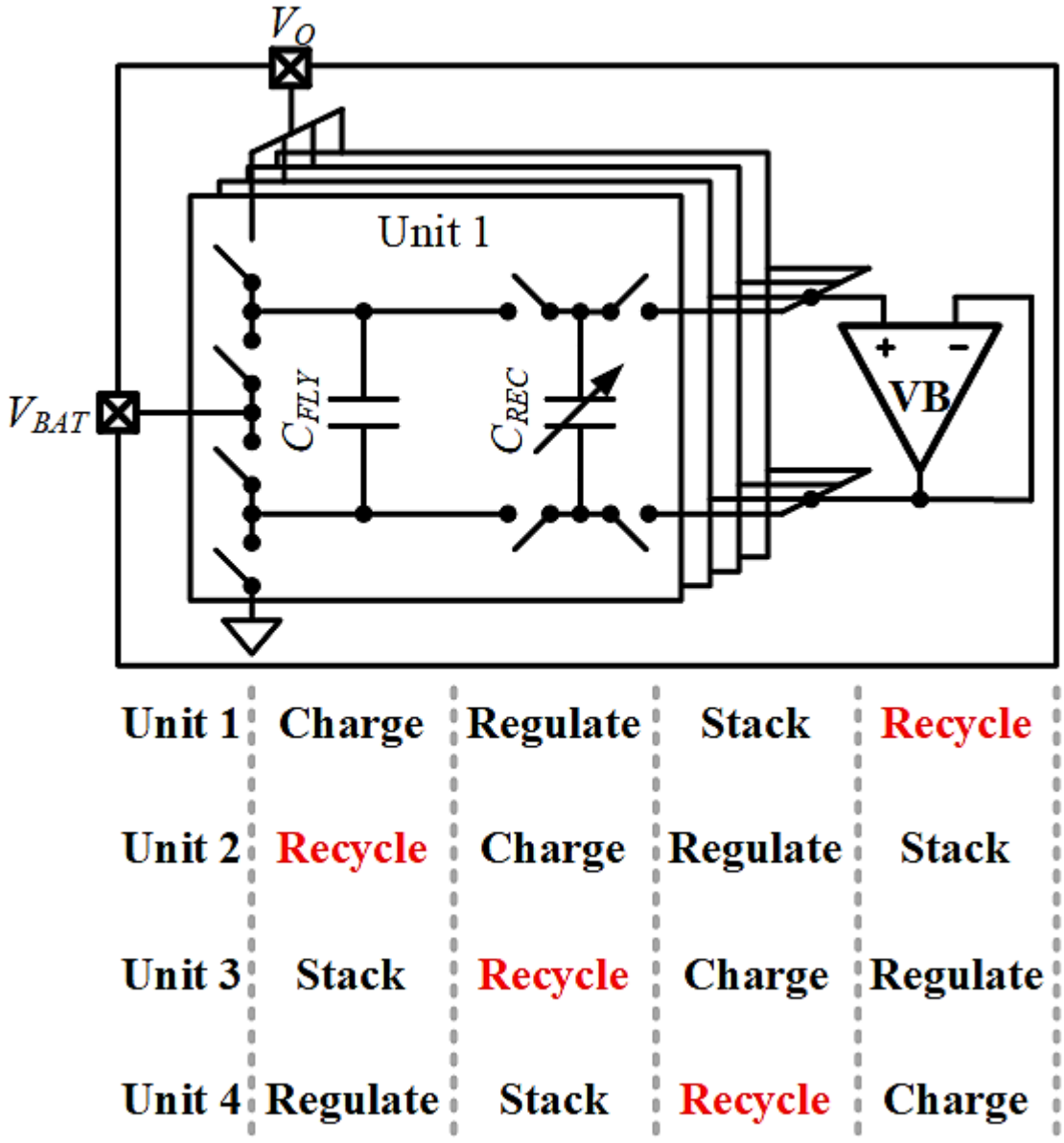


Fig. 5.7. Configuration sharing one VB and its phase diagram

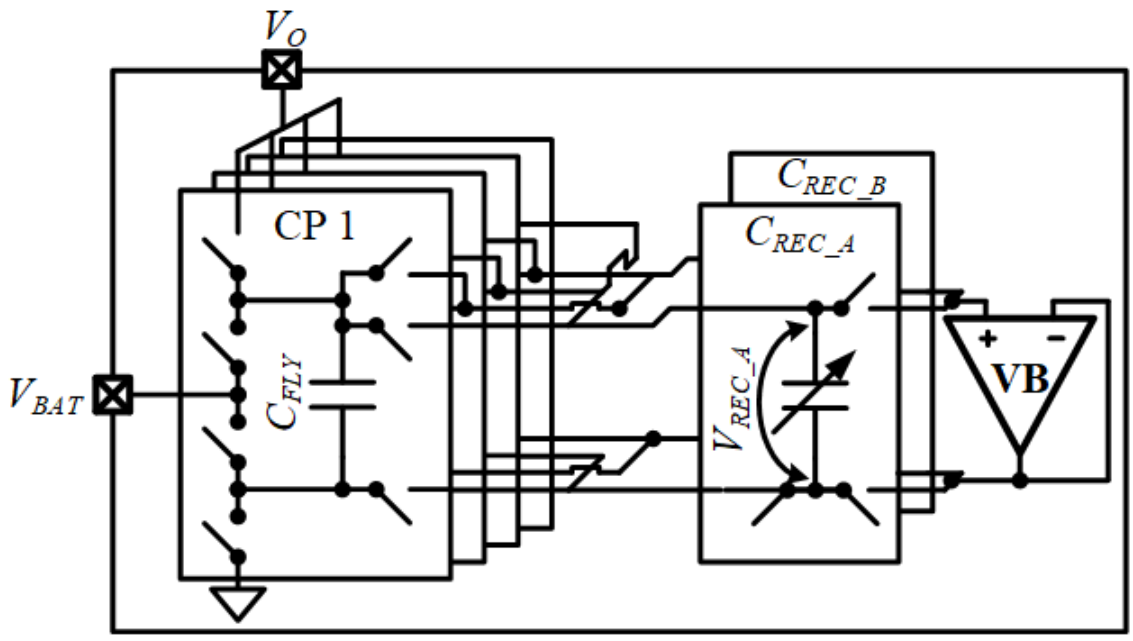


Fig. 5.8. Configuration sharing C_{REC_A} and C_{REC_B}

of unit-converter 1 is transferred to C_{REC_A} during Phase II. Without the recycle capacitor sharing, C_{REC_A} would simply hold the stored charge during the stack phase of unit-converter 1. Instead, the charge stored in C_{REC_A} is transferred to C_{FLY} of unit-converter 4, which is in the recycle phase during Phase III. After the recycle phase of unit-converter 4, C_{REC_A} is depleted out of charge and can be used to regulate C_{FLY} of unit-converter 3 during Phase IV. Then, the newly stored charge in C_{REC_A} during Phase IV is transferred to C_{FLY} of unit-converter 2 during Phase I. Fig. 5.10 illustrates the switching sequence of C_{REC_B} and its voltage waveform during one cycle. C_{REC_B} works in a similar manner, but with a shifted phase compared to C_{REC_A}. In this way, we can reduce the number of required recycling capacitors from four to two for each sub-module. For the proposed sixteen interleaving design, the number of required recycle capacitors reduces to eight from sixteen, which is significant for area efficiency and fully integrated implementation.

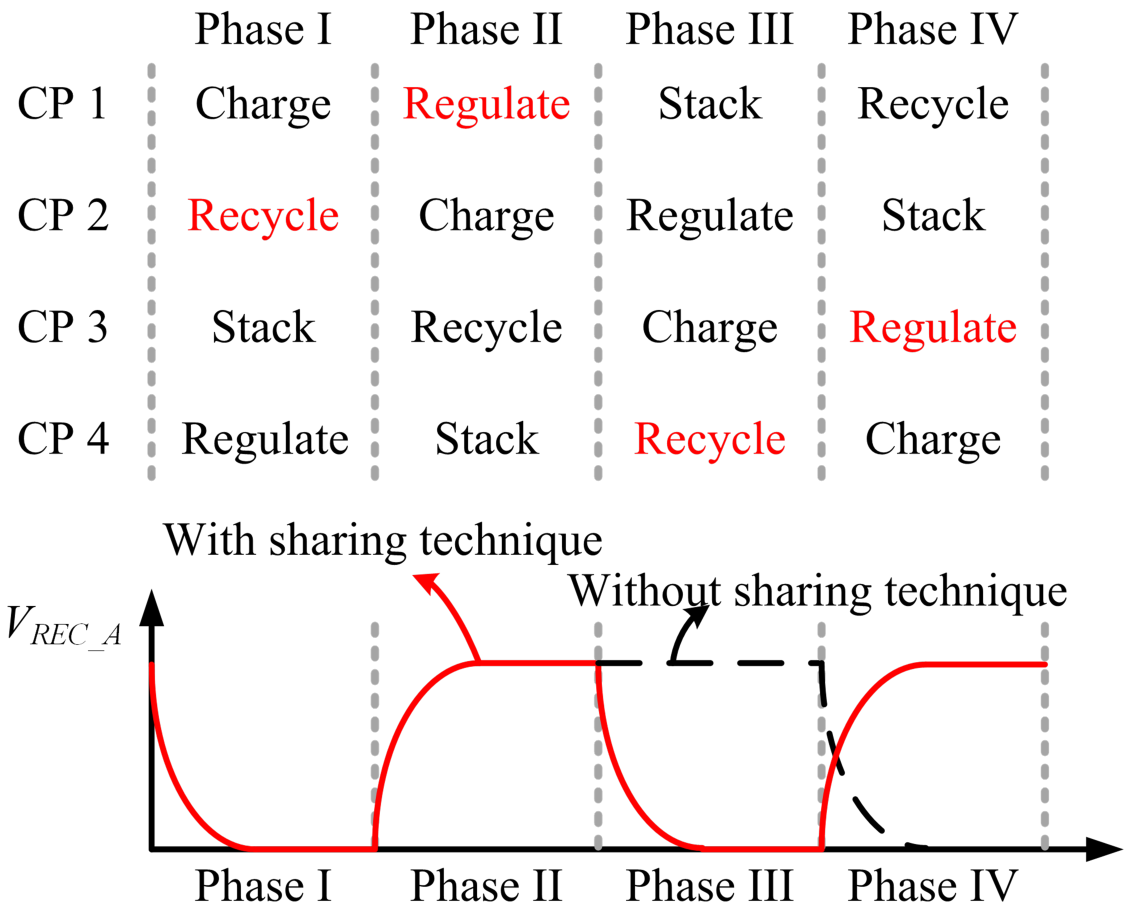


Fig. 5.9. C_{REC_A} connection and its waveform

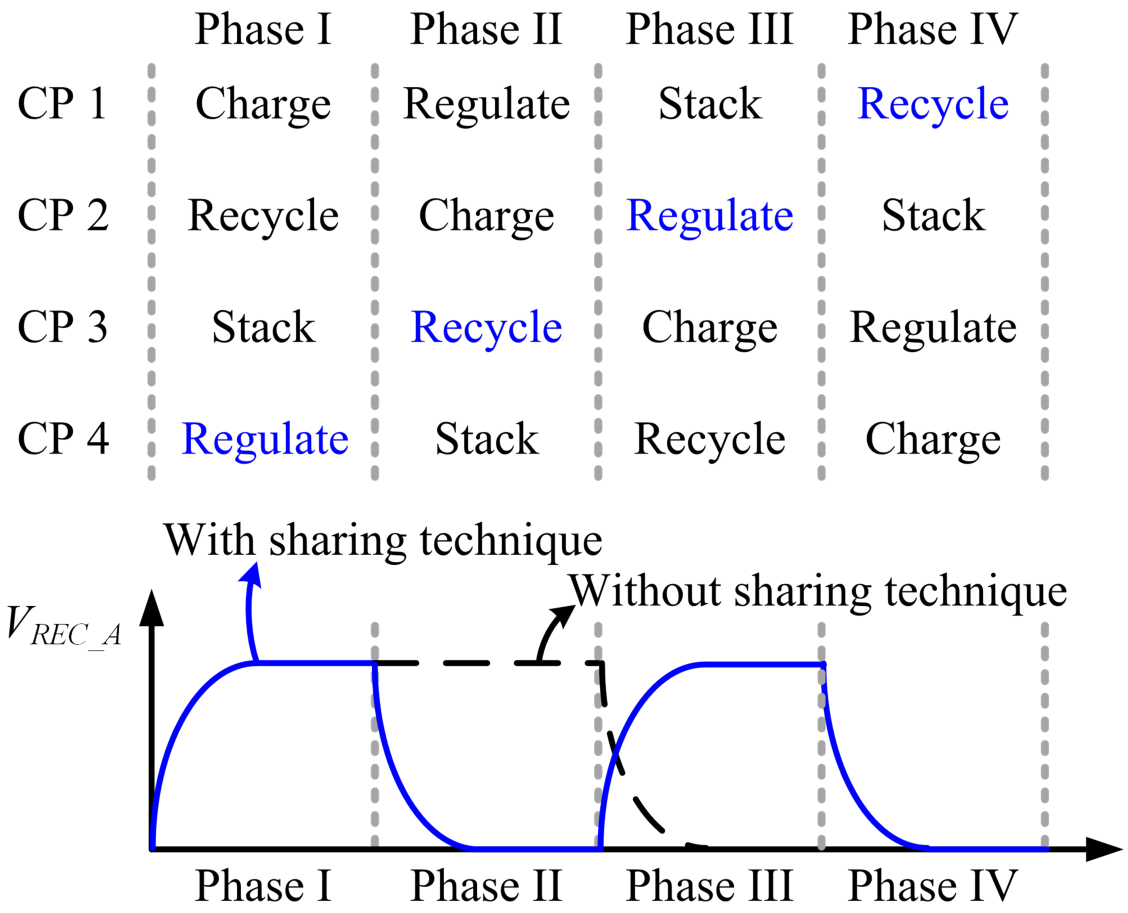
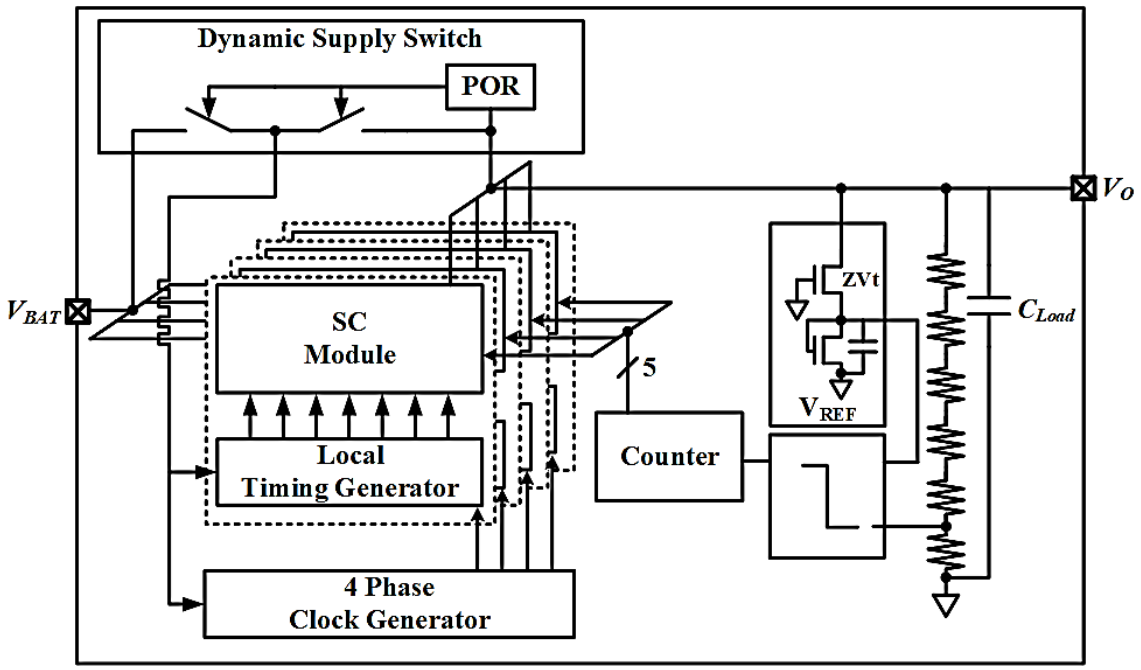


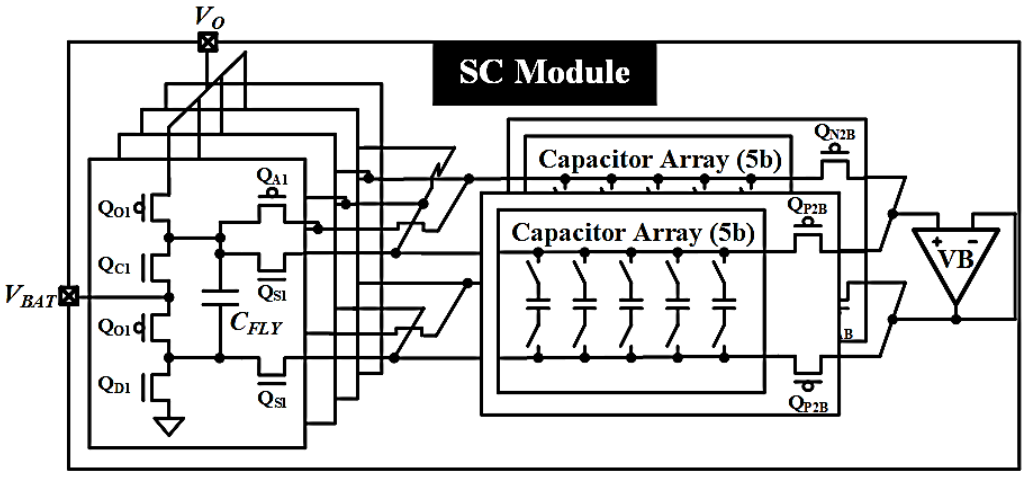
Fig. 5.10. C_{REC_B} connection and its waveform

5.3.2 Overall Architecture

Fig. 5.11 shows a block diagram depicting the overall architecture of the proposed charge pump. The proposed charge pump consists of four switched-capacitor



(a)



(b)

Fig. 5.11. (a) Overall system architecture (b) switch capacitor (SC) module

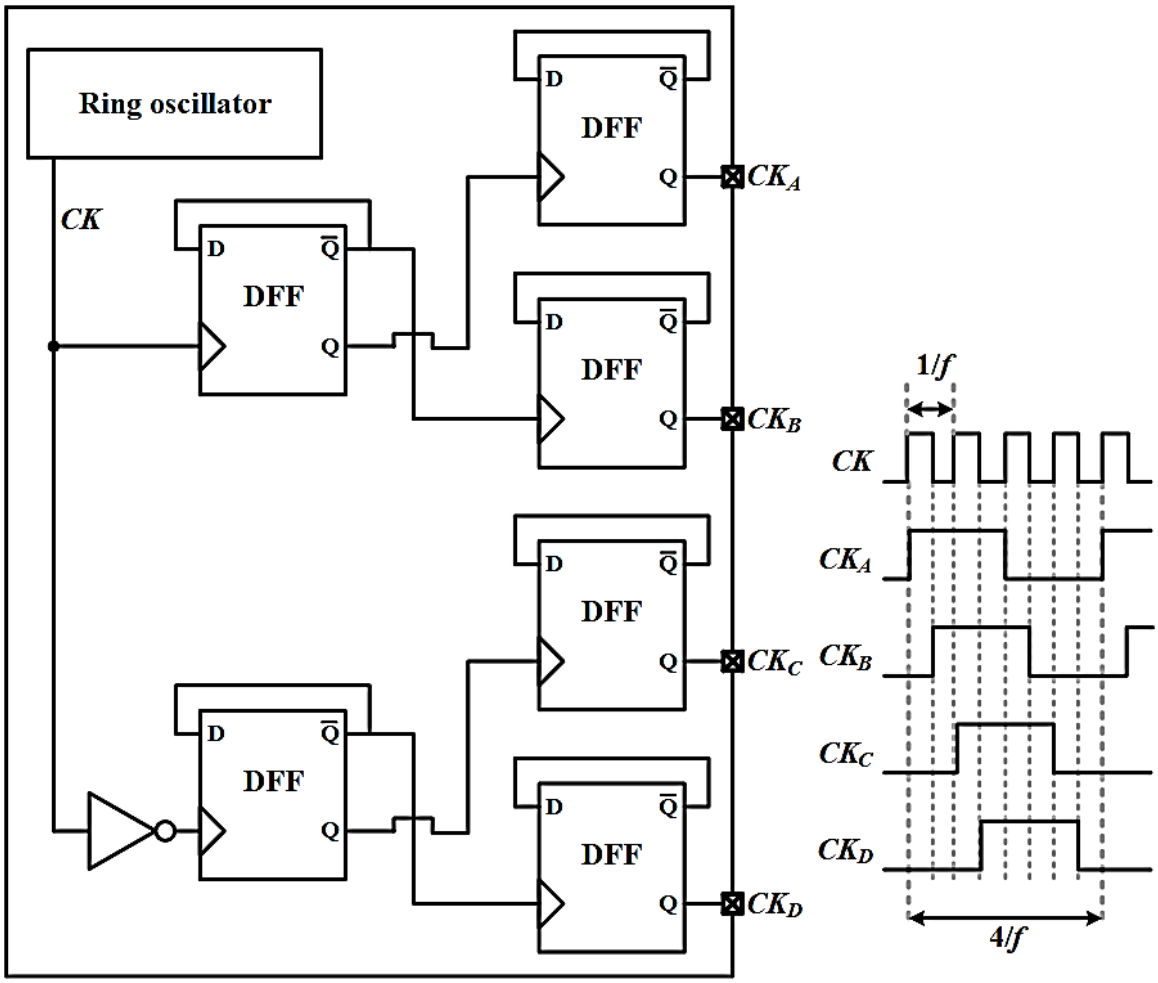


Fig. 5.12. Four phase clock generator and its timing diagram

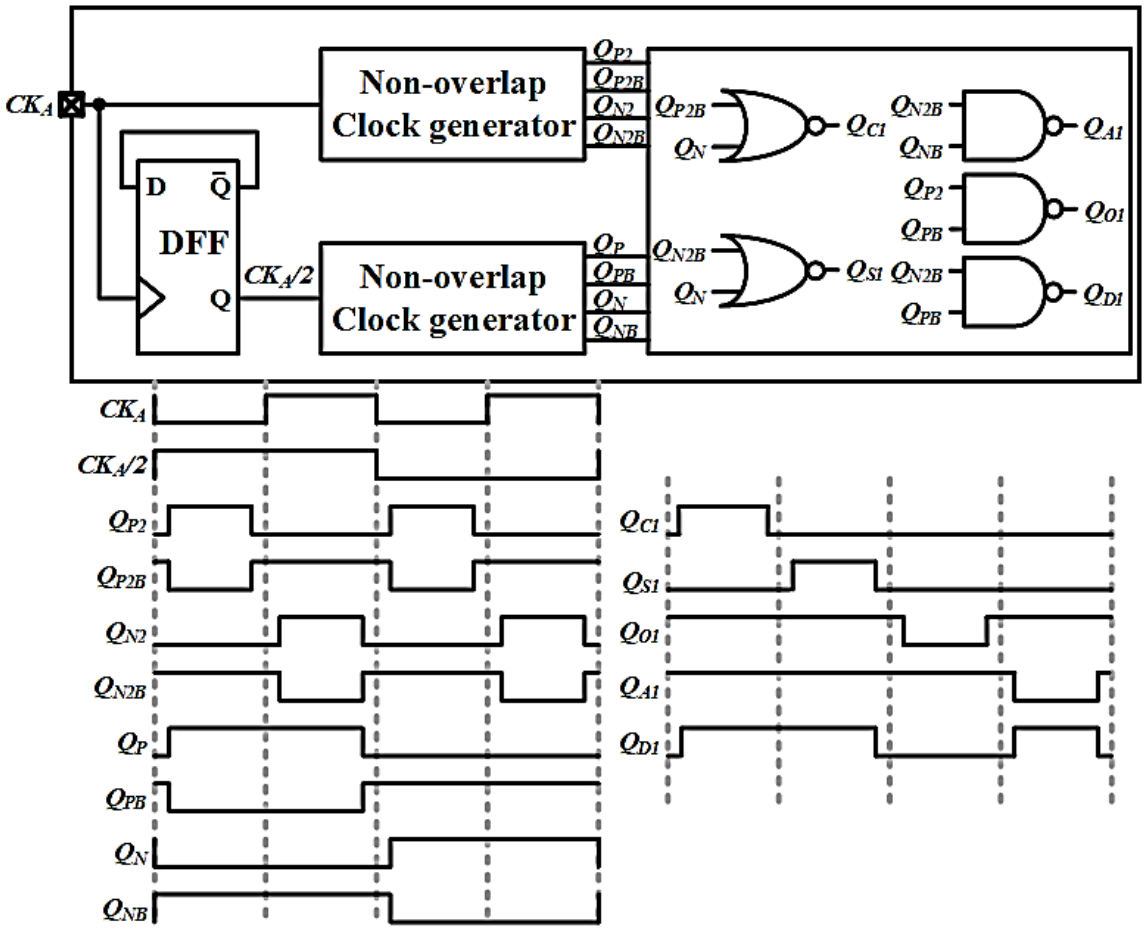


Fig. 5.13. Local timing generator and its timing diagram

(SC) sub-modules with its own local timing generator, a dynamic supply switch, a shared four phase clock generator, and an adaptive recycle capacitor controller. Each switched-capacitor (SC) sub-module has four sub-converters sharing two recycle capacitor arrays and one voltage buffer, and the system has total sixteen sub-converters working in an interleaved manner. The adaptive recycle capacitor controller includes a reference voltage V_{REF} generator of 0.2V, a comparator, and a 5-bit counter. The reference voltage generator presented in [37] is adopted in this design. The comparator compares V_{REF} with a divided output voltage and its output is used to increment or decrement the bits of the counter. The counter output determines the number of capacitors in the array to be connected in each SC sub-module and thus adaptively setting the capacitance of the recycle capacitor C_{REC}. This digital counter-based adaptive capacitance control makes the adaptive closed-loop control simple and robust. A dynamic supply switch is used to sense and select the higher voltage between the battery voltage V_{BAT} and the output voltage V_O. Initially, V_{BAT} supplies power to the local timing generator and the four-phase clock generator. When the output voltage V_O is higher than 1V, the output voltage V_O supplies power to the control circuitry so that all switches in the module are driven with the maximum voltage minimizing their on-resistance and parasitic capacitance. The dynamic supply switch design presented in [38] is adopted in this design. The four-phase clock generator, shown in Fig. 5.12, is implemented using a set of cascaded D-flip flops which divide the input clock CK provided by the local ring oscillator. The D-flip flops produce four clocks with a frequency of $fs = f/4$, each shifted by 45° in phase. The local timing generators use the four phase clocks to generate the switch control signals required for the sixteen interleaving operation as shown in Fig. 5.13.

5.3.3 Measurements

Fig. 5.14 shows the measured voltage waveforms of the flying capacitor C_{FLY}, the voltage across it V_F, the top node voltage TOP, and the bottom node voltage BOT.

The battery voltage V_{BAT} and the load resistance were 0.8V and 300Ω, respectively. The charge pump regulates the output voltage to 1.2V. During the charge phase Φ_1, C_{FLY} is charged to V_{BAT} and V_F increases. During the regulate phase Φ_2, the excess charge stored in C_{FLY} is transferred to C_{REC} through charge redistribution and V_F decreases. C_{FLY} provides power to the load during the stack phase Φ_3 and V_F decreases. Finally, during the recycle phase Φ_4 the charge stored in C_{REC} moves to C_{FLY} and V_F increases. As described in the previous section, V_F increases toward V_{BAT} in two steps: first partially charged during the recycle phases Φ_4 and then fully charged during the charge phase Φ_1.

The conversion efficiency of the charge pump with a 300Ω load resistance is measured with an input voltage varying from 0.66V to 0.86V, which is the output voltage range of the urine-activated batteries presented in [19]. Fig. 5.15(a) shows the

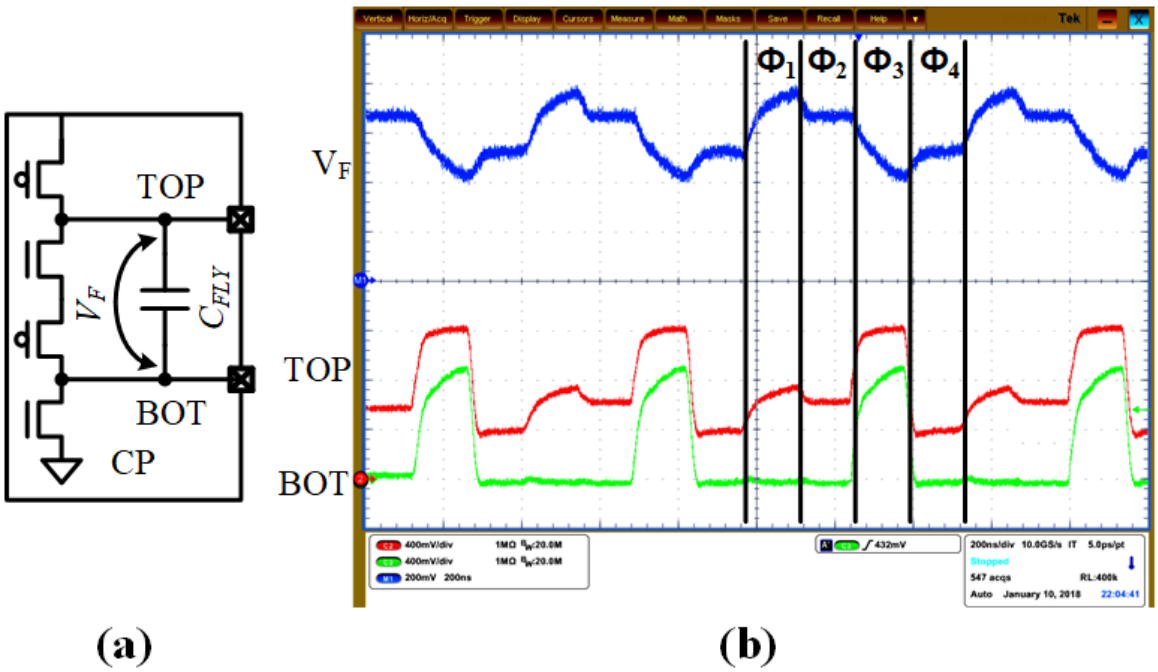
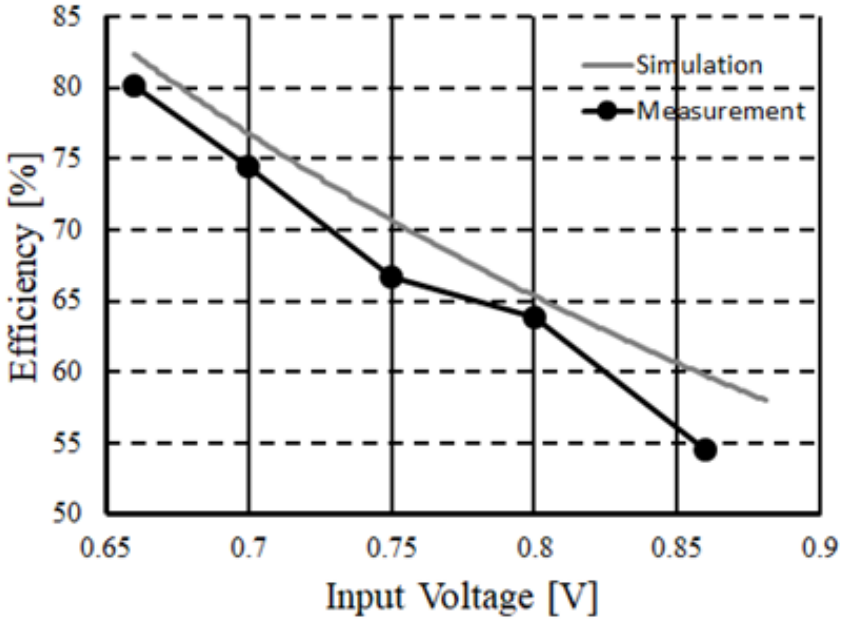
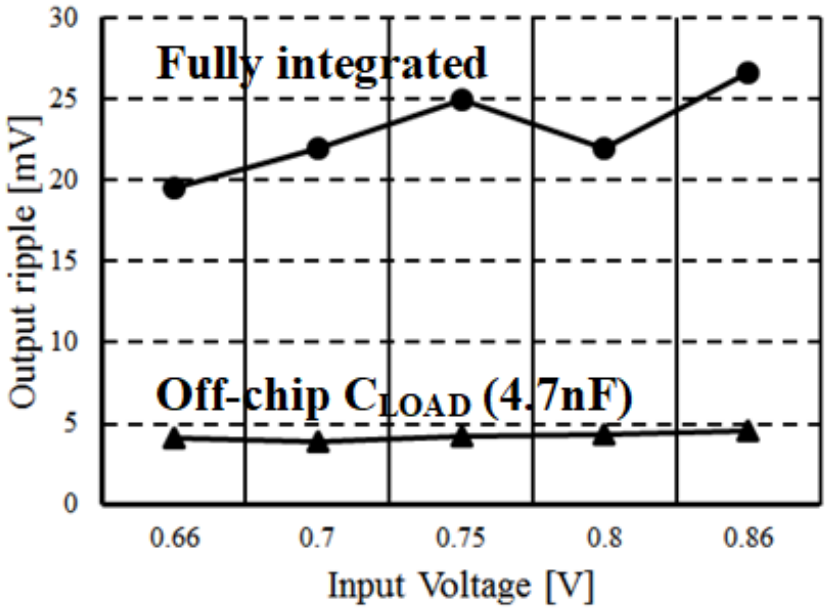


Fig. 5.14. (a) Probe points (b) Measured waveforms of V_F, TOP, and BOT at V_{BAT}=0.8V (Φ_1 charge Φ_2 regulate Φ_3 stack Φ_4 recycle)

measured efficiency. The charge pump achieves a maximum efficiency of 80% when V_{BAT}=0.66V. Fig. 5.15(b) shows the measured output voltage ripple. Over the input



(a)



(b)

Fig. 5.15. (a) Measured efficiency (b) Measured output ripple

voltage range, the output voltage ripple remains around 23mV with a peak-to-peak variation of about 7mV. The variations in the output voltage ripple largely stems from the voltage dependent parasitic capacitance. Adding an additional off-chip load capacitor of 4.7nF, which is much bigger than the on-chip parasitic, reduces the output voltage ripple to 4.3mV with an almost negligible variation. As described in the precious section, using a fixed switching frequency and a fixed flying capacitor size is the key factor for the consistent output voltage ripple.

Table 1 compares the performance of the proposed design with previously published designs. This proposed design achieves a peak-efficiency of 80% as compared to 70% of the fully integrated design presented in [39]. The relatively high switching frequencies and the wide switching frequency range of the fully integrated design in [39] are responsible for the relatively low conversion efficiency and the wide output voltage ripple variation. The total capacitance of the design in [39] is 1.5 times bigger than that of the proposed fully integrated design, yet the worst-case output ripple of the proposed design is about 1.5 times smaller than that of the design in [39]. We note that the proposed design occupies a larger area than the design in [39] despite a smaller total capacitance. This is because the design in [39] used dual-MIM capacitors which have a much higher energy density. The designs presented in [40] and [41] utilize large off-chip flying and load capacitors which allows switching frequencies as low as 200KHz to 600KHz making the switching frequency losses insignificant compared to the proposed design where the switching frequency is 5MHz. Although the design presented in [40] shows a smaller output voltage ripple than the proposed fully integrated design due to its large off-chip capacitors, the proposed design shows a smaller output ripple variation. When an additional off-chip load capacitor of 4.7nF is added, the proposed design shows a much smaller output voltage ripple compared with the designs presented in [40] and [24]. Although the output currents of the designs presented in [40] and [41] are 7.5-times and 40-times bigger than that of the proposed design respectively, the designs in [40] and [41] utilize 50-times and 7-times bigger off-chip load capacitors with considering the output current difference. Even

without any off-chip capacitors, the ripple and ripple variation of the proposed design is better than or comparable with that of the designs with big off-chip capacitors.

	[39]	[40]	[41]	This work	
Technology	130nm	600nm	130nm	65nm	
Fully integrated	Yes	No	No	Yes	No
Topology	Step-down 1/2	Step-up 2/1	Step-up 2/1	Step-up 2/1	
Capacitor	MOS Dual-MIM	Off-chip	Off-chip	MOS MIM	Off-chip C_{LOAD}
# of Interleaving	2	1	1	16	
C_{FLY}	936pF	1μF	330nF	2.2nF	2.2nF
C_{LOAD}	5nF	2.2μF	2μF	378pF	378pF
C_{REC}	NA	NA	NA	1nF	1nF
C_{TOTAL}	5.936nF	3.2μF	2.33μF	3.578nF	8.278nF
I_O	4mA	30mA	160mA	4mA	4mA
Chip area [mm^2]	0.97	5.48	0.25	1.7	
V_{BAT} [V]	1.2	1.5$\sim$3.2	3.3	0.66$\sim$0.86	
V_O [V]	0.3$\sim$0.55	2.7,3.3	4.5$\sim$5.55	1.2	
$V_{O.ripple}$[mV]	20 $\sim$40	10 $\sim$20	26 $\sim$45	19.6 $\sim$26.6	3.9 $\sim$4.6
η_{peak} [%]	70	87	75	80	80
Frequency [MHz]	33$\sim$100	0.2$\sim$0.5	0.4$\sim$0.6	2.5	

Table 5.1.
Performance comparison

5.4 Summary

In this work, we presented a fully integrated and regulated charge pump implemented in a standard 65nm CMOS technology. The charge pump utilizes the charge redistribution between the fixed flying capacitor and the adaptively controlled recycle capacitor to regulate the output voltage and charge recycling to compensate the charge redistribution loss. The unique topology allows to use a fixed switching frequency and a fixed flying capacitance. Consequently, the design can provide an output voltage ripple with a small variation over a wide input voltage range without sacrificing conversion efficiency, and achieve a small worst-case ripple without using a large load capacitor which is crucial for area-conscious applications. The design also utilizes voltage buffer and recycling capacitor sharing technique to further reduce power consumption and to save chip area. The implemented charge pump occupies an area of 1.7mm^2. The design achieves a maximum efficiency of 80% with a 300Ω load resistance, and a constant output voltage of 1.2V. The output voltage ripple ranges from 19.6mV to 26.6mV for an input voltage varying from 0.66 to 0.86V.

6. SUMMARY AND CONCLUSION

Health monitoring sensing technologies have evolved rapidly and have the potential to provide timely and qualified assistance for people. Continuous health monitoring can save human's lives through timely detection of serious disease. The health monitoring system can be applied to urinary tract infection (UTI) diagnosis. UTI is one of the most common infections in humans. UTI is easily treatable using antibiotics if identified in early stages. However, without early identification and treatment, UTI can be a major source of severe complications. This is more severe for infants and geriatric patients suffering from neurodegenerative diseases since they have difficulty in describing their symptoms.

This work presents a diaper-embedded, self-powered, and fully autonomous UTI monitoring sensor module that enables detection of UTI in early stages with minimal effort. For this sensor module, several unique techniques are developed, which are the urination-event driven automatic activation, the low power sensor interface using pulse width modulation (PWM), the time lapse based differential reading technique, and the on-line calibration. The proposed urination-event driven automatic activation increases the shelf-life of the sensor module and eliminates the color fading issue. The sensor interface based on PWM remarkably simplifies the circuit design, reduces the power consumption, and provides better noise immunity. The time lapse based differential reading technique and the on-lice calibration offer robustness to process variation. With the proposed methodologies, the developed sensor module shows a better detection of nitrite, an indicator of UTI, than existing other systems. This sensor module achieves a detection limit of 0.6 ppm for nitrite concentration.

A compact fully integrated DC-DC converter is highly desirable for wearable and implantable biomedical devices that rely on a small size battery with a limited power capacity. This paper presents a fully integrated and regulated charge pump developed

for urine-activated battery applications. The proposed design utilizes charge redistribution between fly and recycle capacitors and an adaptive recycle capacitance control to regulate the output voltage. The charge recycling compensates the loss during the charge redistribution. The design maintains a constant switching frequency and a fixed flying capacitance in the face of varying input voltages, and thereby provides an almost constant output voltage ripple over a wide input voltage range. In the proposed charge pump, multiple sub-blocks share a voltage buffer and a recycle capacitor to reduce power consumption and save chip area. Implemented in a 65nm CMOS technology, the chip that has a 2.2nF flying capacitor, a 1nF recycle capacitor and a 380pF output capacitor occupies 1.7mm^2. Connected to a urine-activated battery with an output voltage ranging from 0.86V to 0.66V, the design delivers a regulated voltage of 1.2V to a load. The fully integrated and regulated charge pump achieves a maximum efficiency of 80% with a 300Ω load resistance, and the measured output voltage ripple varies from 19.6mV to 26.6mV.

REFERENCES

REFERENCES

[1] S. M. Schappert and E. A. Rechtsteiner, "Ambulatory medical care utilization estimates for 2006," *National Health Statistics Reports*, no. 8, pp. 1–29, Aug. 2008.

[2] B. Foxman, "Epidemiology of urinary tract infections: incidence, morbidity, and economic costs," *The American Journal of Medicine*, vol. 113 Suppl 1A, pp. 5S–13S, Jul. 2002.

[3] L. E. Nicolle and T. T. Yoshikawa, "Urinary Tract Infection in Long-Term-Care Facility Residents," *Clinical Infectious Diseases*, vol. 31, no. 3, pp. 757–761, Sep. 2000.

[4] H. J. Woodford and J. George, "Diagnosis and management of urinary tract infection in hospitalized older people," *Journal of the American Geriatrics Society*, vol. 57, no. 1, pp. 107–114, Jan. 2009.

[5] J. Winberg, H. J. Andersen, T. Bergstrm, B. Jacobsson, H. Larson, and K. Lincoln, "Epidemiology of symptomatic urinary tract infection in childhood," *Acta Paediatrica Scandinavica. Supplement*, no. 252, pp. 1–20, 1974.

[6] B. Foxman, "The epidemiology of urinary tract infection," *Nature Reviews. Urology*, vol. 7, no. 12, pp. 653–660, Dec. 2010.

[7] N. Sharief, M. Hameed, and D. Petts, "Use of rapid dipstick tests to exclude urinary tract infection in children," *British Journal of Biomedical Science*, vol. 55, no. 4, pp. 242–246, Dec. 1998.

[8] C. Chen, Y. Wu, and T. Dong, "Dipsticks integrated on smart diapers for colorimetric analysis of urinary tract infections in the field," *in Proc. 2014 16th Int. Conf. Mechatron.-Mechatronika*, pp. 423–427, 2014.

[9] C. Barbosa and T. Dong, "Modelling and design of a capacitive touch sensor for urinary tract infection detection at the point-of-care," *in Proc. 36th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, pp. 4995–4998, 2014.

[10] W. Yu, W. Seo, T. Tan, B. Jung, and B. Ziaie, "A diaper-embedded disposable nitrite sensor with integrated on-board urine-activated battery for uti screening," *in Proc. 38th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, pp. 303–306, 2016.

[11] J. H. L. Lu, M. Inerowicz, S. Joo, J. K. Kwon, and B. Jung, "A Low-Power, Wide-Dynamic-Range Semi-Digital Universal Sensor Readout Circuit Using Pulsewidth Modulation," *IEEE Sensors Journal*, vol. 11, no. 5, pp. 1134–1144, May 2011.

[12] A. V. D. Ziel, *Noise in Solid State Devices and Circuits*. New York: USA:Wiley, 1986.

[13] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: USA:McGraw-Hill, 2001.

[14] M.-T. Tan, J. S. Chang, and Y.-C. Tong, "A process-independent threshold voltage inverter-comparator for pulse width modulation applications," *in Proc. 6th IEEE Int. Conf. Electron. Circuit Syst.*, vol. 3, pp. 1201–1204, Sep. 1999.

[15] R. J. Baker, *CMOS Circuit Design Layout and Simulation*. New York: USA:Wiley, 2005.

[16] W. Yu, T. Tan, R. Rahimi, B. Jung, and B. Ziaie, "Optical nitrite sensor and urine-activated electrochemical power source on paper through laser-assisted patterning and lamination," *MicroTAS 2014 Conference*, pp. 2277–2279, Oct. 2014.

[17] Nitrite high range portable photometer. [Online]. Available: https://hannainst.com/hi96708-nitrite-high-range-portable-photometer.html

[18] Saltwater aquarium ultra low range nitrite colorimeter. [Online]. Available: https://hannainst.com/hi764-nitrite-ulr-for-marine.html

[19] W. Seo, W. Yu, T. Tan, B. Ziaie, and B. Jung, "Diaper embedded urinary tract infection monitoring sensor module powered by urine-activated batteries," *IEEE Transactions on BioCAS*, vol. 11, no. 8, pp. 681–691, Jun. 2017.

[20] J. Wibben and R. Harjani, "A high efficiency dc-dc converter using 2nh integrated inductors," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 8, pp. 844–854, Aug. 2008.

[21] S. Kudva and R. Harjani, "Fully integrated on-chip dc-dc converter with a 450 output range," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1940–1951, Aug. 2011.

[22] R. Balczewski and R. Harjani, "Capacitive voltage multipliers: A high efficiency method to generate multiple on-chip supply voltages," *Proc. ISCAS*, pp. 508–511, 2001.

[23] D. S. Gardner, G. Schrom, P. Hazucha, F. Paillet, T. Karnik, and S. Borkar, "Integrated on-chip inductors with magnetic film," *IEEE Trans. Magn.*, vol. 43, no. 6, pp. 2615–2617, 2007.

[24] J. Lee, G. Hatcher, L. Vandenberghe, , and C. K. Yang, "Evaluation of fully integrated switching regulators for cmos process technologies," *IEEE Trans. VLSI*, vol. 15, no. 9, pp. 1017–1117, 2007.

[25] C. Pei, R. Booth, H.Ho, N. Kusaba, X.Li, M.-J.Brodsky, P. Parries, H.Shang, R. Divakaruni, and S. Iyer, "A novel, low-cost deep trench decoupling capacitor for high-performance, low-power bulk cmos applications," *Proc. 9th Int. Conf. Solid-State Integr.-Circuit Technol.*, pp. 1146–1149, 2008.

[26] T. V. Breussegem and M. Steyaert, "A fully integrated gearbox capacitive dc/dc-converter in 90nm cmos: Optimization, control and measurements," *Proc. IEEE Workshop Control Modeling Power Electron*, pp. 1–5, 2010.

[27] T. V. Breussegem and M. Steyaer, "A fully integrated 74% efficiency 3.6v to 1.5v 150mw capacitive point of load dc/dc converter," *Proc. IEEE Eur. Solid-State Circuit Conf.*, pp. 434–437, 2010.

[28] T. V. Breussegem and M. Steyaert, "A 82% efficiency 0.5% ripple 16- phase fully integrated capacitive voltage doubler," *Proc. IEEE Symp. VLSI Circuits*, pp. 198–199, 2009.

[29] T. D. Cook, T. Akhter, and J. C. Cunningham, "Variable load, variable output charge-base voltage multipliers," U.S. Patent 7 889 553 B2, Feb., 2011.

[30] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A fully-integrated switched-capacitor step-down dc-dc converter with digital capacitance modulation in 45 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec. 2010.

[31] B. Gregorie, "A compact switched-capacitor regulated charge pump power supply," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1944–1953, Aug. 2006.

[32] C. L.Wei, C. H.Wu, L. Y.Wu, and M. H. Shih, "An integrated step-up/step-downdc-dc converter implemented with switched-capacitor circuits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, pp. 813–817, Oct. 2010.

[33] C. L.Wei, L.Y.Wu, H. H. Yang, C.H.Tsai, B. D. Liu, and S. J.Chang, "A versatile step-up/step-down switched-capacitor-based dc-dc converter," *IEICE Trans. Electron*, vol. E91-C, pp. 809–812, May 2008.

[34] M. Tan and W. Ki, "A cascode miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 440–449, Feb. 2015.

[35] P. D. P. Favrat and M. Declercq, "A high-efficiency cmos voltage doubler," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 410–416, Mar. 1998.

[36] W. Ki, F.Su, and C. Tsui, "A versatile step-up/step-down switched-capacitor-based dc-dc converter," *IEICE Trans. Electron*, vol. E91-C, pp. 809–812, May 2008.

[37] M. Seok, D. Blaauw, D. Sylvester, and G. Kim, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5v," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.

[38] J. Curty, N. Joehl, C. Dehollain, and M. Declercq, "Remotely powered addressable uhf rfid integrated system," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2193–2202, Nov. 2005.

[39] S. Kudva and R. Harjani, "Fully integrated capacitive dc-dc converter with all-digital ripple mitigation technique," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1910–1920, Aug. 2013.

[40] J. Lee, S. Kim, S. Song, J. Kim, S. Kim, and H. Yoo, "A regulated charge pump with small ripple voltage and fast start-up," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 425–432, Feb. 2006.

[41] H. Lee and P. Mok, "An sc voltage doubler with pseudo-continuous output regulation using a three-stage switchable opamp," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1216–1229, Jun. 2007.

VITA

VITA

Weeseong Seo received his B.S. degree in electrical engineering from Korea University, Soeul, South Korea, in 2006 and his M.S degree in electrical and computer engineering from the University of California at San Diego, La Jolla, CA in 2009. From 2010 to 2014, he worked at Samsung Electronics, Hwasung, Korea where he was involved in designing data converters. From 2014 to 2019, he worked to pursue his Ph.D degree in electrical and computer engineering at Purdue University. From May in 2018 to August un 2018, he was a design intern at Texas Instruments, Dallas, TX , investigating the issues of a negative charge pump and a power transfer over a capacitive isolatoin boundary.