APPLICATIONS OF MICROHEATER/RESISTANCE TEMPERATURE DETECTOR AND ELECTRICAL/OPTICAL CHARACTERIZATION OF METALLIC NANOWIRES WITH GRAPHENE HYBRID NETWORKS

by

Doosan Back

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THE PURDUE UNIVERSITY GRADUATE SCHOOL
STATEMENT OF COMMITTEE APPROVAL

Dr. David B. Janes, Chair
School of Electrical and Computer Engineering
Dr. Dimitrios Peroulis
School of Electrical and Computer Engineering
Dr. Peter Bermel
School of Electrical and Computer Engineering
Dr. Alexandra Boltasseva
School of Electrical and Computer Engineering

Approved by:

Dr. Dimitrios Peroulis
Head of the Graduate Program

For my family and my fiancée, Eunjoo,

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ABSTRACT

Author: Back, Doosan. PhD
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Title: Applications of Microheater/Resistance Temperature Detector and Electrical/Optical Characterization of Metallic Nanowires with Graphene Hybrid Networks
Committee Chair: David B. Janes

A microheater and resistance temperature detector (RTD) are designed and fabricated for various applications. First, a hierarchical manifold microchannel heatsink with an integrated microheater and RTDs is demonstrated. Microfluidic cooling within the embedded heat sink improves heat dissipation, with two-phase operation offering the potential for dissipation of very high heat fluxes while maintaining moderate chip temperatures. To enable multi-chip stacking and other heterogeneous packaging approaches, it is important to densely integrate all fluid flow paths into the device. Therefore, the details of heatsink layouts and fabrication processes are introduced. Characterization of two-phase cooling as well as reliability of the microheater/RTDs are discussed. In addition, another application of microheater for mining particle detection using interdigitated capacitive sensor. While current personal monitoring devices are optimized for monitoring microscale particles, a higher resolution technique is required to detect sub-micron and nanoscale particulate matters (PM) due to smaller volume and mass of the particles. The detection capability of the capacitive sensor for sub-micron and nanoparticles are presented, and an incorporated microheater improved stable capacitive sensor reading under air flow and various humidity.

This paper also introduces the characterization of nanomaterials such as metallic nanowires (NWs) and single layer graphene. First, the copper nanowire (CuNW)/graphene hybrid networks for transparent conductors (TC) is investigated. Though indium tin oxide (ITO) has been widely used, demands for the next generation of TC is increasing due to a limited supply of indium. Thus, the optical and electrical properties of CuNW/graphene hybrid network are compared with other transparent conductive materials including ITO. Secondly, silver nanowire (AgNW) growth technique using electrodeposition is introduced. A vertically aligned branched AgNW arrays is made using a porous anodic alumina template and the optical properties of the structure are discussed.

1. INTRODUCTION

1.1 Motivation

Microheaters and resistance temperature detectors (RTD) have been used in a variety of fields and has evolved with diverse needs. The basic principle of the microheater is that electrical energy is transformed into thermal energy using a Joule-heating effect. Microheaters are used in the field where controlled heating is necessary in microscale. For instance, the fuel cell system requires a threshold temperature for the catalytic reaction of source material. On-chip microheaters are popularly used in combination with MEMS/RF applications [1]–[3]. The microheater is also a key component of the miniaturization of instruments for drug vaporization, miniaturized mass-spectroscopy, and polymerase chain reaction (PCR) systems [4]–[8]. Together with the thermocouple, RTD is one of the most common thermometers. While the thermocouple uses two dissimilar conductors to create a junction of different temperatures, RTD uses metals' temperature coefficients to track temperature change. Since RTD is more resistant to signal noise than the thermocouple, it is often used in noisy environments such as electric motors, generators, and other high voltage equipment [9].

Given the recent development of microelectronics, the requirements for the microheater are becoming more elaborate. For instance, most microheaters are designed in a very limited space, and the scale of the heating area is shrinking. The estimated power consumption of the microheater should be consistent with their application requirements. For example, the priority parameters of hand-held PCR devices include low power consumption and portability [10]. Microheaters must have high reliability, as they often run at an elevated temperature and are exposed to high humidity environments; accordingly, degradations such as electromigration and oxidation must be considered.

The key parameters to satisfy these requirements are: i) electrical resistances, ii) material types, and iii) microheater/RTD dimensions. In other words, electrical resistance determines the required input power and current density. Resistance relates to the electrical resistivity of the material and heater dimensions. The materials should be highly resistant to heat and oxidation. Since such parameters are highly correlated, they must be simultaneously considered in heater and RTD design.

Nanowire (NW) is a one-dimensional nanostructure with a diameter of tens of nanometers and its length ranges from a few microns (μm) to tens of μm. Semiconductor NWs have been studied extensively in the development of electronic components like nanoscale transistors and p-n junction diodes. Metallic NWs have been studied as transparent conductors (TC), solar cell electrodes, and high sensitivity bio-sensing applications [11]–[14]. Graphene was first introduced in 2004 and gained significant attention due to its superior electrical, mechanical, and optical properties [15]–[18]. Graphene has been utilized in the development of transistors, supercapacitors, touch-screen displays, and other research applications [19]–[21].

Although NW and graphene have demonstrated promising properties, there are still challenges for commercialization such as mass fabrication, sheet resistance, and oxidation. A recent effort attempted to integrate NW and graphene in a hybrid structure. One popular TC application uses the NW/graphene hybrid network with promising results [22]–[24]. Moreover, graphene is an excellent oxidation/corrosion barrier that prevents NW oxidation from air or moisture [25], [26]. Researchers seek to utilize this hybrid structure in plasmonic applications, which has led to studies on surface plasmon polariton (SPP) tuning of hybrid structures and exciton-plasmon interaction [27]–[29].

1.2 Outline

This work will broadly focus on two topics: i) applications of microheater/RTD and ii) metallic NW and graphene characterization. The first topic involves the application of the microheater and RTD in microfluidic studies, which will be the focus of Chapter 2. A compact hierarchical manifold microchannel (MMC) design is presented for two-phase cooling. It utilizes an integrated multi-level manifold distributor to feed coolant to an array of microchannel heat sinks. The heat source is simulated via Joule heating using platinum microheaters and on-chip spatial temperature measurements are made using RTDs. A very high volumetric heat density (W/m^3) is dissipated using the heatsink showing a promising cooling approach for high-power electronics. Continuing from Chapter 2, Chapter 3 will focus on the reliability of the platinum microheater and RTD. The effect of electromigration and temperature on device failure is discussed, and the failure mechanism is studied quantitatively using Black's equation. The current factors of platinum are extracted in two different temperature levels for the first time and they have compared each other. Chapter 4 will introduce another application of the microheater

on a mining particle detection. This technique uses an interdigitated capacitive sensor and the sensor is designed for monitoring sub-micron and nanoparticles in mining environments. The results present the detection capability of sub-micron and nanoparticle as well as stable sensor reading with a microheater integration approach.

Chapter 5 and 6 will focus on the metallic NW and graphene. In Chapter 5, the copper nanowire (CuNW) and graphene hybrid networks are explained. The concept of NW/graphene co-percolation networks is introduced, and a TC fabricated using the CuNW/Graphene hybrid networks is presented with its optical and electrical properties. Finally, Chapter 6 will introduce a branched silver nanowire (AgNW) array made by electrodeposition. The fabrication process of the vertically-aligned branched AgNW array is presented and the optical properties of the NW array including waveguiding effect is discussed.

2. MICROHEATER AND RESISTANCE TEMPERATURE DETECTOR (RTD) USE IN HIERARCHICAL MANIFOLD MICROCHANNEL HEAT SINK

2.1 Introduction

The continuing miniaturization of electronic devices and increasing die-level heat fluxes requires thermal management technologies that can provide the necessary cooling capacity while maintaining chip temperatures within allowable limits. High-power computing, switching, and radar electronics have reached power densities above 100 W/cm², with future systems projected to reach 1000 W/cm² [30]. Optical devices such as laser diodes and photovoltaic systems also need proper thermal management to perform at design specifications and to achieve their desired reliability [31]–[33]. Traditional heat dissipation has relied on heat spreaders; however, heat spreading is not a solution in cases where heat is generated over a large fraction of the chip surface area. Furthermore, volumetric heat density becomes a concern with increasing levels of integration, such as 3D stacking of devices in data centers [34], which requires a more compact cooling system. Integrated motor drives offer higher power density but similarly raise operating temperature concerns [35].

Microchannel heat sinks have been shown to dissipate high heat fluxes at moderate chip temperatures for electronics cooling applications. In their pioneering work, Tuckerman and Pease [36] experimentally tested a silicon microchannel heat sink. The 50 μm-wide and 302 μm-deep channels were wet-etched using potassium hydroxide (KOH) and the simulated heat load was applied to the base of the channels using thin-film tungsten silicide (WSi_2) resistors. The silicon heat sink was bonded to a glass top cover using anodic bonding. Heat fluxes up to 790 W/cm² were dissipated over a 10 mm × 10 mm area using single-phase water as the working fluid at pressure drops up to 214 kPa. Many studies have since shown that microchannel heat sinks are a viable technology for electronics cooling applications [37], [38].

The performance of microchannel heat sinks can be improved by allowing the working fluid to undergo phase change in the channels. For most fluids, the latent energy absorbed during evaporation is orders of magnitude larger than the specific heat capacity associated with moderate temperature rises. Two-phase microchannel heat sinks yield more uniform temperature along the channel length because evaporation is an isothermal process at a given pressure. Achieving

complete evaporation of the coolant in heat sinks is unfeasible because local dryout—when vapor is in contact with the channel wall—results in extreme temperature spikes. To support extremely high heat fluxes, high fluid flow rates are required to prevent dryout but may lead to exorbitant pressure drops. One heat sink design approach to overcome this challenge is to use a manifold which delivers the flow to the channels at multiple locations along their length thereby reducing the effective flow length—this design is termed a manifold microchannel (MMC) heat sink.

Harpole and Eninger [39] developed a numerical model to solve for the temperature distribution in MMC heat sinks during single-phase operation. The model was used to optimize the geometric parameters for the dissipation of high heat fluxes over a 10 mm × 10 mm area using a water/methanol mixture as the working fluid. The design called for small-diameter, high-aspect-ratio channels fed by a manifold that distributed the flow to the channels at multiple locations along the flow length. The optimal design had channels between 7 μm and 15 μm-wide and ~167 μm-deep, and a manifold with 200 μm-wide inlets and outlets spaced by a center-to-center distance (i.e., the effective flow length) of ~333 μm. The design was demonstrated by wet-etching microchannels (9 μm-wide and 334 μm-deep) and manifold features in silicon using KOH. The manifold and microchannels were joined and sealed using diffusion bonding. Since this initial demonstration, many numerical and experimental studies have shown that MMC heat sinks are a high-performance heat sink design for single-phase operation [40]–[43]. Two-phase cooling is more efficient than single-phase cooling because it exploits the latent heat of vaporization, resulting in a higher heat dissipation per fluid mass. Although less commonly studied than single-phase approaches, two-phase cooling in MMC heat sinks has been successfully demonstrated [44].

In addition to investigating and optimizing the channel geometries, a number of studies have demonstrated the importance of manifold designs and dimensions on the overall performance of MMC heat sinks [45]–[50]. Proper manifold design is required to prevent significant flow maldistribution to the channels; this is a concern for all microchannel heat sinks but is especially important in MMC heat sinks due to the large number of parallel flow paths. Flow maldistribution can cause drastic performance differences between channels which can result in large temperature gradients across the chip surface. During two-phase operation, intrinsic flow instability mechanisms can lead to exacerbated flow maldistribution [51]–[53].

Hierarchical manifolds distribute the flow from a single inlet/outlet to the heat sink using a series of branching flow paths. This allows the manifold to be designed such that the hydraulic

resistance of each flow path is similar, which results in an even flow distribution. Brunschwiler et al. [54] demonstrated a direct liquid-jet-impingement cold plate with a nozzle array. They designed a vertical hierarchical manifold structure to minimize the hydraulic resistance of the flow path from the top inlet to the bottom 30 μm-diameter nozzle array and achieved a pressure drop of 35 kPa from single phase operation. Calame et al. [55] designed horizontally hierarchical branched microchannels with different levels of hierarchies and achieved an average heat flux dissipation of 960 W/cm2 using water. Dang et al. [56] and Schultz et al. [57] designed an embedded radially expanding hierarchical microchannel heat sink for two-phase cooling of 3D stacked chips.

Advancements in microelectromechanical systems (MEMS) fabrication methods have allowed more flexibility in microchannel heat sink design. Deep reactive ion etching (DRIE) techniques have been used to fabricate high-aspect-ratio microchannels having complex channel/manifold flow profiles [58]–[60]. Hermetic sealing throughout the system has been achieved using a variety of bonding techniques including fusion [61], anodic [62], eutectic [63], and thermocompression [64]. Alternative bonding materials such as photoresist [65] and adhesive tapes [66] have also been used to achieve fluidic sealing.

Recently, we demonstrated fabrication and testing of a hierarchical manifold microchannel heat sink in two-phase operation [67]. Heat fluxes up to 1020 W/cm² were dissipated over a 5 mm × 5 mm area by flowing the dielectric working fluid HFE-7100 through a 3 × 3 array of embedded, high-aspect-ratio microchannel heat sinks. Despite this extreme level of heat flux dissipation based on the heat input footprint area, the manifold was attached to the heat sink as a separate component that increased the system size. In the current work, a manifold microchannel heat sink is developed with an embedded, compact hierarchical manifold that significantly reduces the envelope of the flow features. Fabrication of all flow features in silicon using DRIE allows a dense 9 × 9 array of embedded microchannel heat sinks to be aligned and thermocompression-bonded to the hierarchical manifold layers. Microheaters and resistance temperature detectors (RTDs) are patterned directly on the microchannel wafer; these individually addressable devices provide heating and local temperature sensing. Hydrodynamic and thermal performance of the heat sink is characterized for a range of flow rates; the efficacy of the design is evaluated based on the volumetric heat dissipation within the system envelope.

This work was done in collaboration with Kevin P. Drummond in School of Mechanical Engineering, Purdue University under the guidance of Professor Justin A. Weibel and Professor

Suresh V. Garimella, and with Michael Sinanis in School of Electrical & Computer Engineering under the guidance of Professor Dimitrios Peroulis. Drummond and Sinanis contributed to the fabrication of the hierarchical manifolds/microchannels and wafer bonding, which were done in Birck Nanotechnology Center. Drummond conducted the thermal characterization of the heat sink and this work was done in Garimella's laboratory.

2.2 Device Fabrication

2.2.1 Hierarchical manifold microchannel heat sink array design

In a hierarchical manifold microchannel heat sink array, fluid is delivered to an array of microchannel heat sinks using a multi-level manifold, as shown schematically in Figure 1(a). The manifold consists of multiple layers that split the flow into gradually finer features. Maximum granularity occurs at the channel inlet/outlet plenum where flow is delivered to the individual microchannel heat sinks, each having an effective flow length that is significantly shorter than the overall length of the channel. In this work, a 9 × 9 array of microchannel heat sinks is etched into a single silicon die with a total heated area of 5 mm × 5 mm. Each of the 81 heat sinks consists of 18 high-aspect-ratio microchannels that are 19 μm-wide and 150-μm deep. The detailed dimensions of the plenum and microchannels are shown in Table 1. The base thickness is the thickness of the silicon substrate at the bottom of the microchannels.

A three-dimensional drawing of the hierarchical MMC heat sink array used in this work is shown in Figure 1(b). The manifold comprises four silicon wafers (A-D), each etched from both sides, for a total of eight feature levels (1-8), as labeled in the figure. Fluid enters the manifold at Level 1 (Wafer A) where there is a single inlet; as the fluid travels through Levels 2 through Level 8 (Wafers A-D), it is gradually split into finer flow paths. After reaching Level 8, where there is a distinct inlet plenum feature for each of the 81 microchannel heat sinks, the fluid enters the microchannels (Wafer E) and turns 90 degrees, i.e. flows parallel to the wafer surface. The fluid is heated by microfabricated heaters (top surface of Wafer E) as it flows through the microchannels. After traveling along the length of the channels, the fluid turns 90 degrees and exits back through the manifold where the fluid is recollected from the channel outlet plenums (Level 8) into a single fluid exit (Level 1).

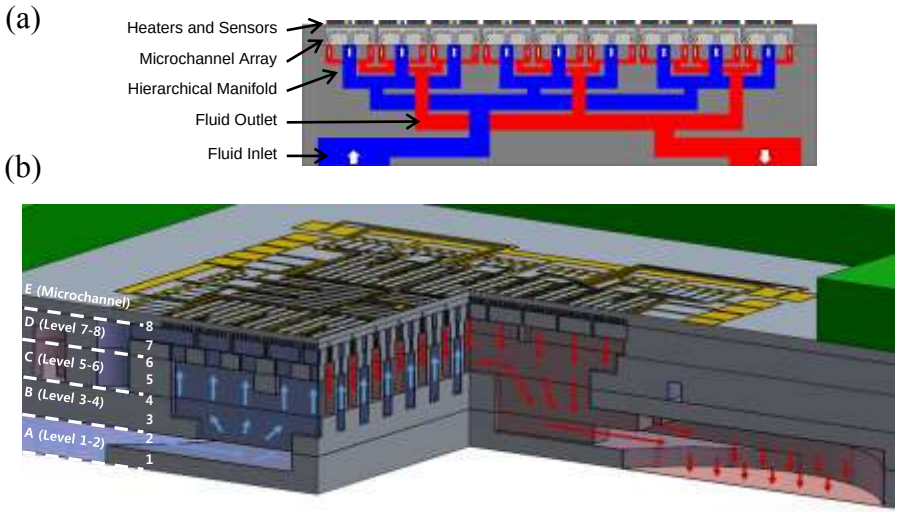

Figure 1. (a) Schematic diagram showing a hierarchical manifold microchannel heat sink array (not to scale), and (b) three-dimensional drawing of the specific design used in this work with sections removed to show the internal flow features (all features are to scale except the microchannels). [68]

Table 1. Summary of plenum and microchannel dimensions. [68]

Parameter	Value	Units
Channel width	19	μm
Channel height	150	μm
Aspect ratio	7.9	
Fin width	11	μm
Base thickness	50	μm
Plenum inlet length	100	μm
Plenum outlet length	50	μm
Effective flow length in channels	175	μm

2.2.2 Heater and sensor layout

The heater and RTD sensor layout are designed to provide a uniform background heat flux and local temperature measurements over the 5 mm × 5 mm die area. For ease of fabrication, the heaters and RTDs are deposited and patterned at the same time. Because all the features are constrained to the same plane, the heaters and RTDs—and their traces—cannot overlap. The heater consists of a 3 × 3 array of individually addressable heaters; All traces have the same width and are equally spaced across the entire heated area as shown in Figure 2. In addition, metal pads of low resistivity are periodically patterned on top of the heaters to achieve a more uniform heat flux

by creating heating elements that are periodic in both horizontal and vertical directions. RTDs are placed between the lines of the heaters; each heater footprint area contains two RTDs for a total of 18 temperature measurements across the die surface. All RTDs are connected using the four-wire technique to eliminate the lead wire resistance from the measured resistance.

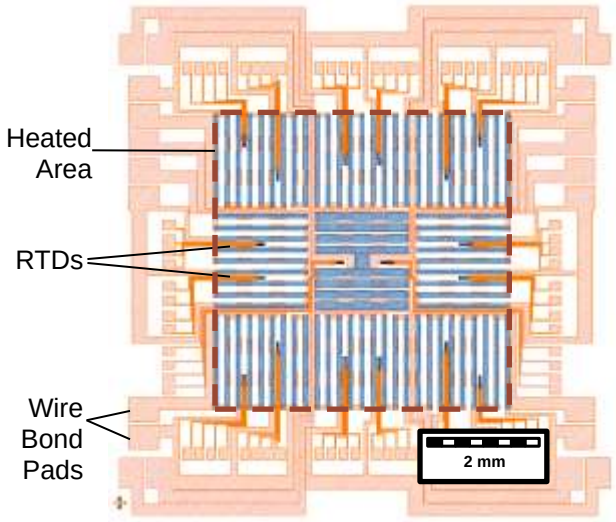

Figure 2. Heater and RTD layout. The 3×3 heater array covers a 5×5 mm^2 area (blue) and each heater is individually addressable. Each section has two four-wire RTDs for local temperature sensing. [68]

Electromigration has been shown to create voids and hillocks on metals due to the movement of ions under bias, and is likely to happen at large current densities and high temperatures [69]. Electromigration can be avoided by increasing heater resistance, which results in lower current densities for a given power. However, higher resistance will require a higher voltage and this may cause dielectric breakdown. Therefore, the resistances of the heaters are designed based on both the electromigration limit (10^7 A/cm^2) and breakdown voltage limit of the dielectric layer (200 V for 200 nm SiO_2). An individual heater of 333 Ω satisfies these requirements, as both the current density and the voltage are below the limits at the heater design flux of 1 kW/cm^2. Platinum (Pt) is chosen as the heater/sensor material as it has strong resistance to oxidation and other chemical reactions. In addition, the electrical resistance of Pt is linear with respect to temperature over the expected operating range, making it a good candidate for RTDs [70]. Gold (Au) is chosen as the lead wire material to minimize heat generation in the leads and for robust connections to printed circuit board (PCB) using Au wire-bonding.

2.2.3 Microchannel plate and manifold plate fabrication

The overall fabrication processing flow is as follows: i) bottom-side etching of the microchannel plate and manifold plates, ii) top-side heater and RTD patterning on the microchannel plate and etching of the manifold plates, and iii) metallization and bonding, as shown in Figure 3. The microchannel wafer fabrication process, which is outlined in Figure 4(a), begins by etching the microchannel features into the bottom side of a 300 μm-thick, 4 inch-diameter silicon wafer. A single wafer yields 12 dies, each 20 mm × 20 mm in size. The channels occupy the center 5 mm × 5 mm footprint area of the die, with the remaining area available for top-side traces, wire-bond pads, and mounting of the wafer to a PCB. The wafer is cleaned using piranha solution and a 2 μm-thick silicon dioxide (SiO_2) hard mask layer is thermally grown on the wafer. Photolithography was with hexamethyldisilazane (HMDS) adhesion promoter and AZ9260 positive photoresist layer throughout, unless otherwise stated. HMDS/AZ9260 are coated using a spin coater (Specialty Coating Systems G3). The photoresist layer is exposed using a mask aligner (Karl Suss MA6) and developed in a diluted AZ400K solution (DI water:AZ400K = 3:1). The SiO_2 layer is removed from the open areas using a plasma dry etch (Surface Technology Systems-Advanced Oxide Etch). The microchannels are then etched to the desired depth using the Bosch process (STS-Advanced Silicon Etch). For the etching of high-aspect-ratio microchannels, the photoresist provides the soft mask after microchannel patterning while the SiO_2 provides sharper edges and more vertical sidewalls. The key DRIE parameters are listed in Table 2. Once the channels are etched, the photoresist and SiO_2 layers are removed using PRS2000 and buffered oxide etch (BOE), respectively.

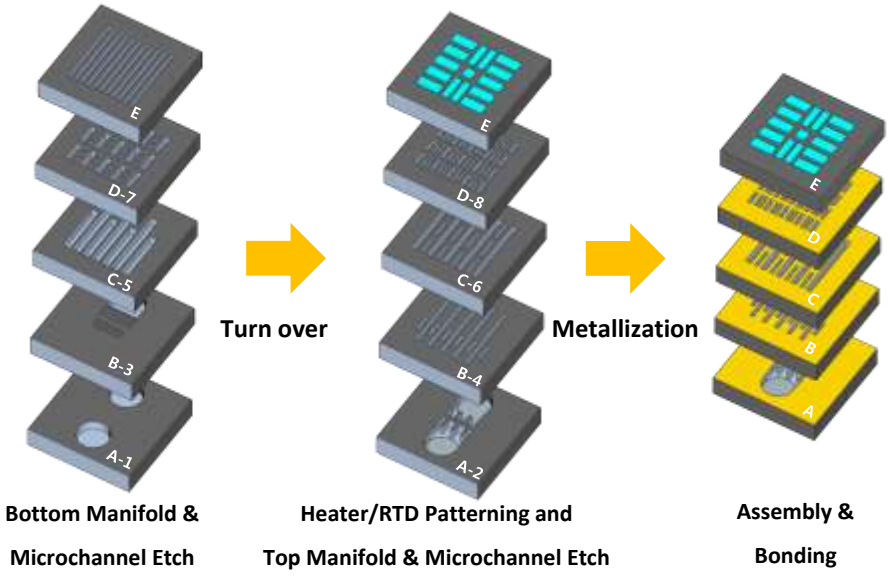

Figure 3. Overall fabrication flow: i) bottom manifold and microchannel etch, ii) top manifold and microchannel etch and heater/RTD patterning, iii) interface metallization, assembly and bonding of all chips (not to scale, refer to Figure 1(b) for wafer labels A-E and level numbers 1-8). [68]

Heater and RTD patterns are fabricated directly on the top side of the microchannel wafer. After the microchannel etch process, a 200 nm-thick layer of SiO_2 is thermally grown on the wafer as a dielectric barrier. The same photolithography procedures as for the microchannel patterning are employed, and backside alignment was used to align the heater and RTD patterns with respect to the microchannels. Once the patterns are defined, 5 nm of Titanium (Ti) and then 20 nm of Pt are deposited via electron beam evaporation (CHA Industries, Inc.). This was done at a pressure level of 2.0×10^{-6} torr and the deposition rate was 1.0 Å/s. A lift-off process is performed by stripping off the photoresist using PRS2000. To fabricate the heater and RTD lead wires, this lithography procedure is repeated with two differences: the trace locations are defined using a new mask and the metal depositions are 10 nm of Ti and then 400 nm of Au.

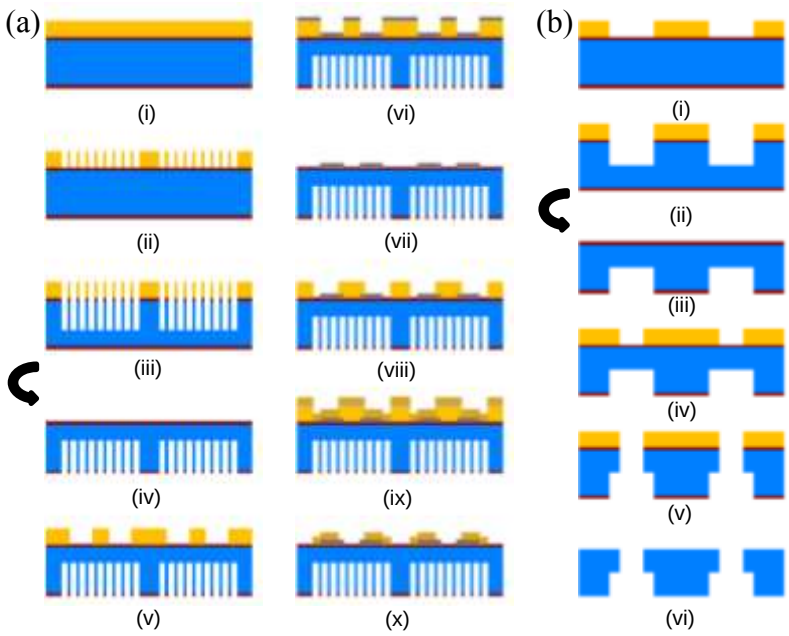

Figure 4. Cross-section of the fabrication process. a) microchannel and heater/RTD bottom side: (i) HMDS and photoresist (PR) coating; (ii) microchannel lithography; (iii) SiO_2 and Si etch; Top side: (iv) PR removal, BOE & re-oxidation; (v) heater/RTD backside lithography; (vi) Ti and Pt deposition; (vii) lift-off; (viii) lead wires lithography; (ix) Ti and Au deposition; (x) lift-off. b) manifold bottom: (i) PR coating and bottom side lithography; (ii) SiO_2 & Si etch. Top side: (iii) PR removal, BOE & re-oxidation; (iv) PR coating and top side lithography; (v) SiO_2 & Si etch; (vi) PR removal and BOE. [68]

Table 2. Key parameters using for deep reactive ion etching (DRIE) of the high-aspect-ratio microchannels. [68]

Parameter	Value	Units
Etch rate (approx.)	3	μm/min
Etch step time	10	s
Passivation step time	10	s
RF power	1000	W
Platen power	10	W
C_4F_8 flow rate	100	SCCM
SF_6 flow rate	250	SCCM
O_2 flow rate	30	SCCM

Because the hierarchical manifold requires a large number of layers for flow distribution, etching features into both sides reduces the required number of wafers and bonding interfaces, while also mitigating risk for misalignment between layers. Two Levels are fabricated in each wafer, by etching from the bottom side and then from the top side, with the patterns from the two Levels meeting at the middle of the wafer. The processing steps in manifold wafer fabrication are

shown in Figure 4(b). The 500 μm-thick wafers are cleaned and oxidized with a 2 μm-thick SiO_2 layer. The fabrication procedure follows that used for the microchannel etch and the same procedure is repeated on the opposite side of the wafer. Backside lithography is used to align with the features already etched in the wafer.

Figure 5(a) shows a microscope image of the heaters and RTDs deposited on the opposite side of microchannel wafer (Level E). Heating elements are clearly patterned in the 5 × 5 mm^2 area, and RTDs are located in between the heaters. Each heater is connected to Au traces for wirebonding. Figure 5(b) shows a scanning electron microscope (SEM) image of the cross section of the etched microchannels. Straight walls are achieved, and all channels have consistent width; the side walls and bottom surfaces are smoothly finished.

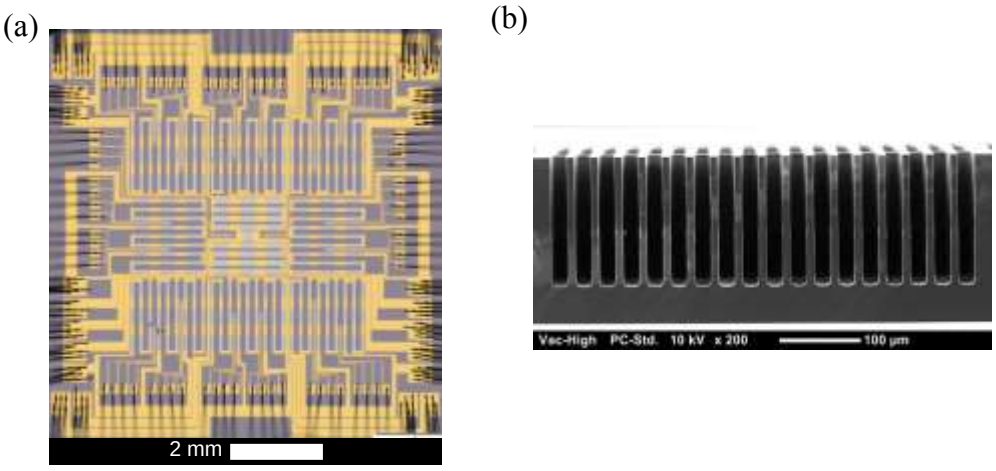

Figure 5. (a) Microscope image of fabricated heater/RTD layer. Heating elements (Pt) are located in a 5 × 5 mm^2 area and 18 RTDs are placed in between the heaters. (b) SEM image of the microchannel cross-section. The width and depth of each channel is 19 μm and 150 μm, respectively. [68]

2.2.4 Assembly and Integration

All layers of the manifold and microchannels are joined to seal surfaces between the fluid routing features and prevent fluid from bypassing the microchannels. An evaluation of thermocompression bonding was performed using two dummy silicon wafers, one containing through plenum features and another with etched microchannels (nominally 15 μm × 150 μm). The samples were thermocompression bonded, diced, and the open plenum features sealed to evaluate the leakage rate of helium. The leakage rate was measured to be <1.3×10-7 atm-cc/sec

across 4 samples. The bonds were also subjected to 500 temperature cycles (MIL-STD-883, Condition B, -55 to +125°C) without failure. Based on these hermiticity results and visual inspection, thermocompression bonding was selected as the sealing method for the test samples used in this work.

Prior to bonding, the microchannel and manifold wafers are cleaned using piranha solution. After cleaning, 50 nm of Ti and 500 nm of Au are deposited on both sides of the manifold wafers using a magnetron sputtering system (MANTIS Deposition CUSP-Series); the Ti layer is used to increase adhesion of the subsequent Au layer. The sputtering system pressure during deposition is held at 7.3 $\times 10^{-3}$ Torr and the DC deposition current is 0.1 A. The sample is rotated during deposition to improve uniformity across the wafer. The microchannel wafer is coated using the same deposition process on the channel side. The wafers are then diced into 20 mm × 20 mm dies for bonding (Disco DAD-2H/6 Dicing Saw). Figure 6(a-e) shows the metallized and diced dies.

A custom-made, Macor ceramic assembly fixture is used to align the microchannel die and manifold dies during thermocompression bonding. The assembly and alignment is completed in a cleanroom to prevent any contamination at the interfaces. Once the manifold and microchannel dies are stacked in order, as shown in Figure 6(a-e), the fixture is installed in the vacuum chamber of a bonding facility. Bonding is performed by heating the assembly stack to 350 °C while compressing at a pressure of 500 kPa for 1 h. The assembled fluid features, including the hierarchical manifold (dies from Wafers B-E), are confined to a 5 mm × 5 mm × 2.3 mm working envelope. After thermocompression bonding, the die assembly is attached to the underside of a custom-designed PCB using adhesive tape. The heaters and RTDs are then electrically connected to the PCB bond pads using gold wire bonds as shown in Figure 6(f). Each of the background heaters and RTDs are wirebonded (West Bond 7400A Ultrasonic Wedge Bonder) separately such that they can be addressed and monitored individually. A dummy chip is prepared to confirm the reliability of the custom heaters and RTDs at the maximum operating temperature. A constant current density (4.8×10^{6} A/cm^2) was applied to the base heater and the chip temperature was monitored by the central RTD. The temperature recorded by the RTD was initially at 155 °C but decreased rapidly within the first few hours as the heater resistance decreased. Because the heater resistance would be expected to increase if degraded by electromigration, this reduction in the heater resistance is attributed to an annealing effect caused by Joule heating. Afterward, the temperature remains stable at 138 ± 2 °C and the resistance of heater slowly increases by 1% over

a period of 378 h, which causes a slight temperature increase due to the increased heating power at constant current density; no failure was observed. To calibrate the heater resistance before testing, heaters are annealed at 180 °C in a laboratory oven for 24 h.

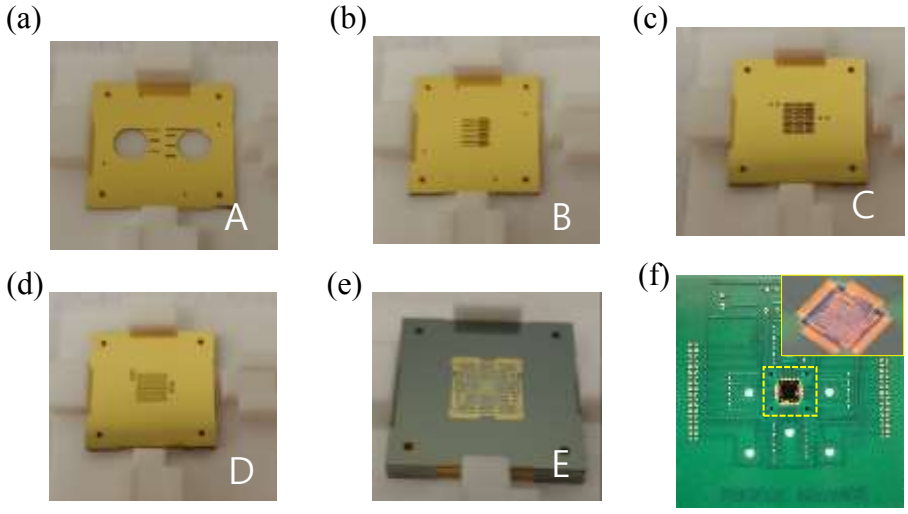

Figure 6. (a-d) Top view of the metallized manifold dies and (e) microchannel die after stacking. (f) Photograph of the fully assembled hierarchical manifold microchannel heat sink array test vehicle, with inset showing the wirebonded chip. [68]

To characterize the manifold feature alignment, one sample was diced normal to the flow direction in the microchannels, polished, and imaged using a microscope, as shown in Figure 7. The arrows indicate the inlet fluid path through the manifolds. The results reveal that there are no gaps between the plates and that the flow features are aligned within a few microns.

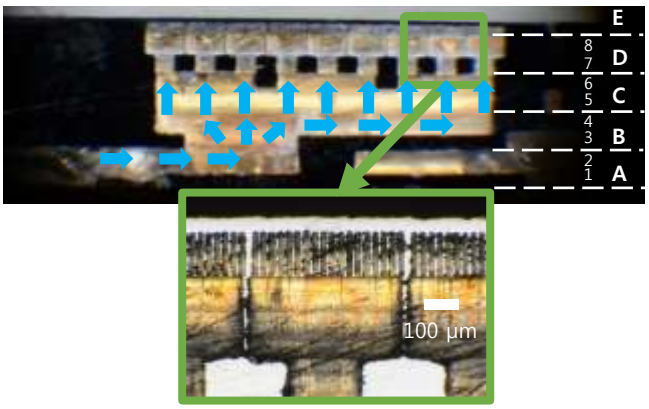

Figure 7. Cross-section image of the bonded manifold and microchannel test chip assembly with a magnified inset image of the top plenum and microchannel features (refer to Figure 1(b) for wafer labels A-E and level numbers 1-8). [68]

2.3 Experimental Methods

2.3.1 Electrical measurement and calibration details

A wiring diagram of the electrical components used to measure the voltage and current to each of the heaters, and to adjust the power to each of the heaters, is shown in Figure 8. A single DC power supply (Sorensen XG100-8.5) is used to power all of the heaters. While the design of each individual heater element on the test chip is identical, slight differences in metal deposition thickness, trace length, wire bond resistance, lead wire length, and operational temperature can lead to small differences in their resistance. To ensure uniform heat flux across the chip surface throughout testing, a potentiometer (Ohmite RES25RE) is added in series with each of the heaters; this provides a variable resistance that is used to adjust the voltage drop of each parallel branch and thus equalize the power applied by each heater. A voltage divider circuit (TE Connectivity 1622796-6, 10 kΩ ± 0.1%; TE Connectivity 8-1879026-9, 499 kΩ ± 0.1%) is wired in parallel to each heater of the test chip, which is used to step down the voltage below the 10 V limit of the data acquisition hardware (National Instruments cDAQ-9178). For instance, as shown in the Figure 8, the voltage across R_1 (V_1) is calculated using $V_1 = V_{meas,1} * ((R_{div1} + R_{div2})/R_{div2})$, where $V_{meas,1}$ is acquired from the data acquisition hardware and R_{div1} and R_{div2} are known. The voltage drop (V_{shunt}) across a shunt resistor (R_{shunt}) (Vishay Y14880R10000B9R, 0.1 Ω ± 0.1%) wired in series to each heater is used to calculate the current through each heater: $I_N = \left(V_{shunt,N}/R_{shunt}\right)$. The total voltage drop and current are measured using the same techniques and are used to verify the individual measurements.

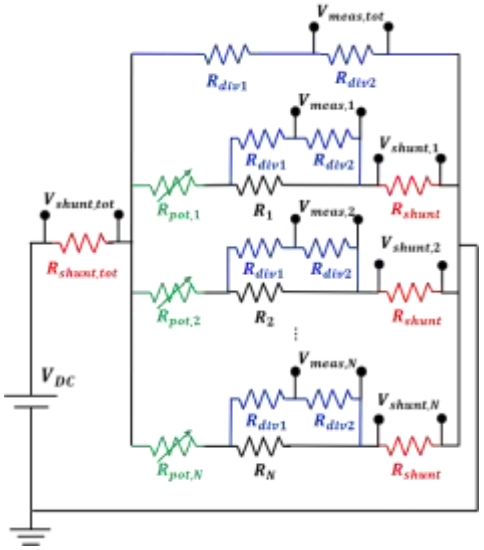

Figure 8. Electrical wiring diagram showing the components used to measure heater power to the test vehicle. The voltage divider circuits (blue) consist of two resistors (R_{div1} = 499 kΩ, R_{div2} = 10 kΩ) and each shunt resistor (red, R_{shunt} = 0.1 Ω, $R_{shunt,tot}$ = 0.2 Ω) is used for current measurement. The potentiometers (green, R_{pot} = 0-25 Ω) are added to adjust and equalize power to each heater. [68]

To calibrate the on-chip RTDs, the test chip is placed in a laboratory oven along with a Pt100 RTD (PR-10-3-100, Omega) that is used as the known reference temperature. The electrical resistance of the on-chip RTDs was measured at two different temperature levels: 50 °C and 100 °C. A linear fit is used to determine the relationship between electrical resistance and temperature for each of the 18 RTDs across the chip surface.

2.3.2 Thermal and hydrodynamic testing procedure

Prior to testing, the working fluid HFE-7100 is degassed via vigorous boiling and subsequent capture of the vapor; noncondensable gases escape during this process, leaving pure working fluid to be used for testing. HFE-7100 was chosen because of its high dielectric strength and low attenuation of RF signals; its boiling point is 61 °C at 100 kPa. A two-phase flow loop is used to deliver fluid to the test section at a constant and known flow rate, inlet temperature, and outlet pressure. The magnetically-coupled gear pump (GB-P23, Micropump) provides a constant flow rate that is independent of the system pressure drop; the flow rate is measured using a Coriolis mass flow meter (CMF010M, Micromotion). The differential pressure drops across the entire chip and across the microchannels are measured (PX2300, Omega) using pressure taps located in the

inlet/outlet of manifold and microchannels, respectively. A detailed description of this flow loop is available in Ref. [71]. To characterize the two-phase heat sink performance under boiling conditions, the fluid temperature at the inlet to the test section was set to achieve a constant, relatively small subcooling below the saturation temperature. Experimental testing was performed at a fixed inlet temperature of 59 °C (~6 °C below the saturation temperature at the outlet pressure), fixed absolute outlet pressure of 121 kPa, and fluid flow rates ranging from 150 to 350 g/min. During testing, the heat input to the test chip heaters begins at 0 W and is incremented in steps until a maximum chip temperature of 120 °C is reached, with the steady-state data (temperatures, pressures, voltages, currents, and flow rate) being recorded at each heat input level. The fluid pressure drop is measured between the inlet and outlet streams at Level 1 and Level 8 (Figure 1(b)); the measurement at Level 1 provides the total pressure drop while the measurement at Level 8 provides the channel pressure drop.

2.3.3 Data reduction

Electrical power supplied to each heater is calculated using P = V×I, where V is electrical voltage and I is electrical current. The total power supplied to the heaters, P_{total}, is then calculated by summing the power to each of the heaters. Most of the applied heat is absorbed into the fluid via convective and boiling heat transfer; however, some of the heat is conducted into the test fixture and lost to the ambient. This heat loss was estimated prior to testing using the method outlined in Ref. [38] and was found to be $Q_{loss}=0.02768*(T_{(chip,avg)}-T_{amb})$. The net heat input is calculated by subtracting the calibrated heat loss, Q_{loss}, from the supplied electrical power as $Q_{in} = P_{total} - Q_{loss}$. The base heat flux is calculated by dividing the net heat input by the base footprint area, A_b. Pressure drop is measured at the inlet and outlet to the manifold as well as the inlet and outlet to the channels.

2.4 Results

2.4.1 Thermal performance

Figure 9 shows the average chip temperature as a function of base heat flux at four different fluid flow rates. Fluid enters the test chip at 59 °C and is heated as it flows along the length of the channels. At low heat fluxes (< 100 W/cm2 approx.), the surface temperature rise is not sufficient to initiate boiling of the liquid. In this single-phase region, convective heat transfer results in a

linear chip temperature increase with heat flux at each flow rate. At higher heat fluxes, the fluid transitions to boiling, resulting in a lower temperature rise for a given increase in heat flux in the two-phase region compared to the single-phase regime; the slope of the curves in the two-phase regime is insensitive to flow rate, indicating that the boiling process governs heat transfer to the fluid. At some critical heat flux, the surface temperature experiences a sudden increase past the 120 °C limit and the heater power is cutoff; the last steady-state data point before this threshold terminates each curve in Figure 9. There is a slight degradation in performance (increasing slope) in each curve as the critical heat flux is approached. The critical heat flux is highly dependent on the fluid flow rates and as flow rate increases, higher heat fluxes can be dissipated before critical heat flux is encountered. The highest heat flux dissipated at a flow rate of 150 g/min is 305 W/cm² and at 350 g/min is 660 W/cm², an increase of 116 %. A more thorough analysis of performance trends in MMC heat sinks during two-phase operation is available in [67], [71].

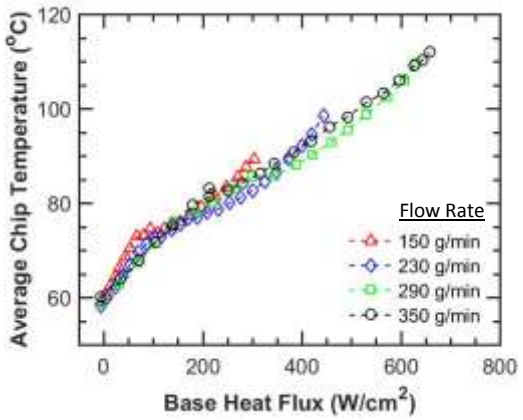

Figure 9. Average chip temperature as a function of base heat flux at flow rates of 150, 230, 290, and 350 g/min. [68]

2.4.2 Pressure drop

Figure 10(a) shows the measured total pressure drop across the entire test chip, which includes pressure drop in the inlet and outlet manifold as well as the microchannels. For each flow rate, the pressure drop is relatively constant in the single-phase region. Upon boiling incipience, the bulk fluid density decreases causing an increase in fluid velocity and hence pressure drop. The two-phase pressure drop increases with heat flux due to the increase in vapor generation with increasing heat flux at a given flow rate. The pressure drop increases with increasing flow rate in

both the single- and two-phase regions, as expected. Figure 10(b) plots both the total pressure drop across the test chip and the pressure drop across the microchannels for the highest flow rate of 350 g/min. A majority of the total pressure drop occurs in the manifold flow features; the channel pressure drop accounts for only 20 % to 27 % of the total pressure drop, depending on the heat flux. This is important to note because thermal performance is governed by the channel size; due to the discretization of the heat sink into a 9 × 9 array with very short flow paths, the pressure drop across the channels can be maintained at only 27 kPa for the maximum heat flux dissipation of 660 W/cm². In the current design, the large maximum total pressure drop of 138 kPa is caused by the restriction of the manifold flow features to a compact envelope of only 5 mm × 5 mm × 2.3 mm such that the observed volumetric heat dissipation of 2870 W/cm^3 can be achieved.

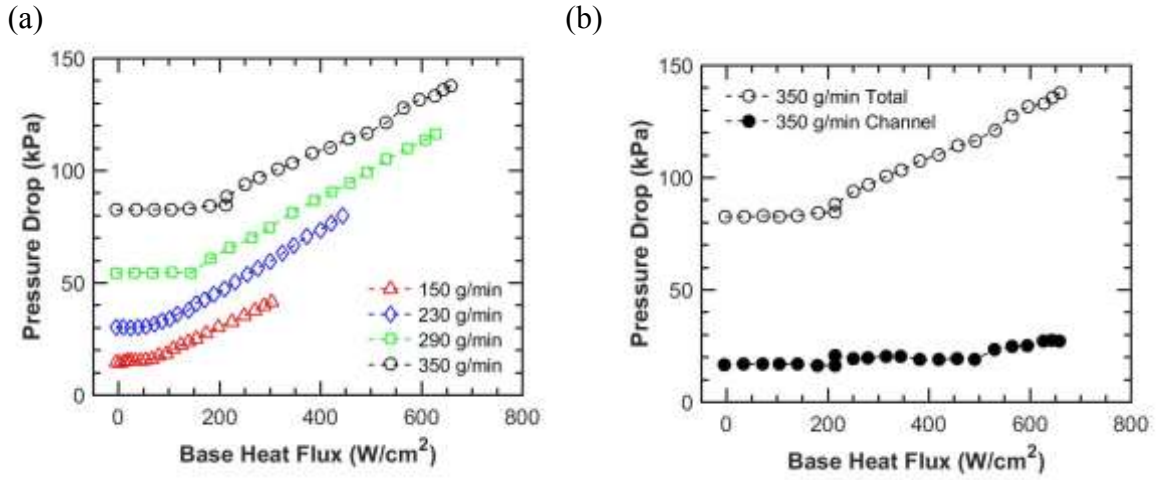

Figure 10. (a) Total pressure drop as a function of base heat flux at flow rates of 150, 230, 290, and 350 g/min and (b) comparison of the total pressure drop (open symbols) versus microchannel pressure drop (closed symbols) at a flow rate of 350 g/min. [68]

2.4.3 Discussion

To illustrate the compactness of the 9 × 9 heat sink array, its thermal and hydraulic performance are compared with our previous work. Figure 11(a) shows the 350 g/min data from the current test vehicle having a 9 × 9 heat sink array compared to data from Drummond *et al*. [71] for a 3 × 3 array at a similar flow rate of 360 g/min. The samples have similar nominal channel geometries of approximately 15 μm × 150 μm. Overall, the thermal performance is very similar for the two different test vehicles. While the flow length and number of parallel flow paths differ significantly, thermal performance is known to be largely governed by channel size and fluid

quality during two-phase operation in confined microchannels, which are essentially the same across these data sets. Even though the thermal performance is very similar between the designs on a heat flux basis, the primary advantage of the 9 × 9 heat sink array is the small volumetric envelope of the compact integrated manifold, which is significantly reduced compared to the 3 × 3 array manifold. All functional flow features could be confined into a 5 × 5 × 2.3 mm^3 for the 9 × 9 manifold in the current work compared to an envelope of 25 × 8 × 10 mm^3 for the 3 × 3 manifold in our prior work. This translates to a maximum volumetric heat dissipation of 2870 W/cm^3 for the 9 × 9 array compared to a maximum of only 285 W/cm^3 for the 3 × 3 array. However, this compact manifold design requires smaller manifold flow features that increase the total pressure drop; Figure 11(b) shows the total pressure drop for the 9 × 9 array compared to that the 3 × 3 array. The channel pressure drop for the 9 × 9 array is also shown for reference. Even though the 3 × 3 array would be expected to have a higher channel pressure drop (it was not measured), the 9 × 9 array still has a notably higher total pressure drop at a given heat flux, due to the dominant contribution of the manifold flow resistance to the overall pressure drop.

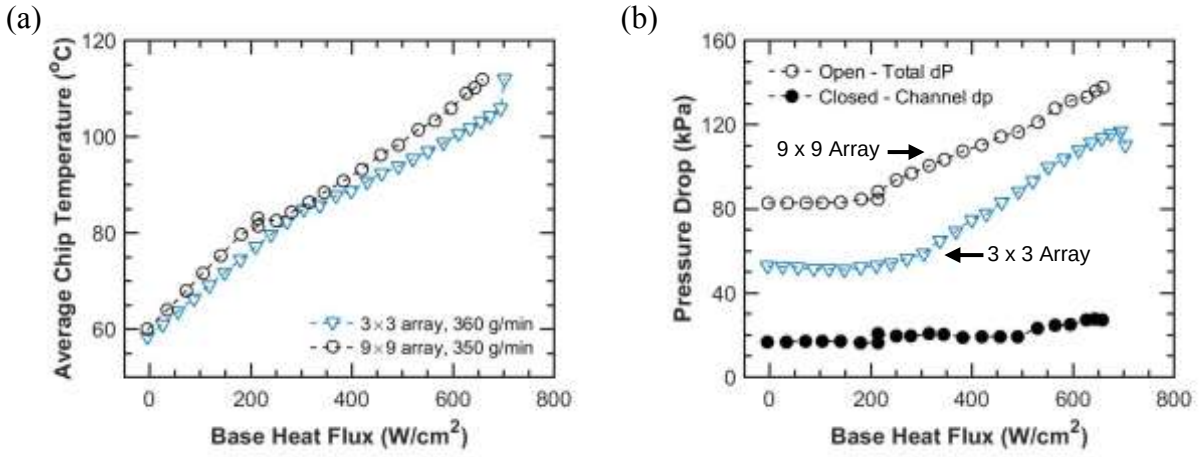

Figure 11. (a) Average chip temperature and (b) pressure drop for the 3 × 3 array and the 9 × 9 array. A similar nominal microchannel size of approximately 15 μm × 150 μm was used in both array designs. (Channel pressure drop for 3 × 3 array test vehicle was not available. [68]

2.5 Conclusion

A compact hierarchical manifold microchannel heat sink was fabricated and tested. The hierarchical manifold consists of 8 fluid routing levels which distribute fluid uniformly to a dense 9 × 9 array of embedded microchannel heat sinks. All fluid features are fabricated using photolithography and DRIE processes. The individually addressable heaters and 4-wire RTDs are

patterned directly on top of the microchannel wafer to provide heating and local temperature sensing. The fabricated dies are aligned using a custom-designed assembly fixture and thermocompression bonded. With stringent size constraints on most heat sinks, this compact, robust manifold design provides a functional manifold within a total envelope volume of 5 × 5 × 2.3 mm3.

The thermal performance of the 9 × 9 array heat sink at a given flow rate is very similar to previous work that investigated 3 × 3 arrays. However, due to the integration of a compact manifold, a volumetric heat density of up to 2870 W/cm3 is dissipated from the 9 × 9 array, an order of magnitude higher than that with the 3 × 3 array. While the microchannel pressure drop was only 27 kPa for the maximum heat flux dissipation of 660 W/cm2, a majority of the pressure drop (80% of the total) occurs in the manifold for these extremely small fluid flow features, resulting in a total pressure drop of 138 kPa at this heat flux.

4. ELECTROMIGRATION STUDY ON THIN FILM PLATINUM

4.1 Introduction

All electronic devices age over time. Reliability has been an important issue in industries as it is directly related to the lifetime of devices and manufacturing cost. The reliability becomes more critical as the devices are scaled down. There are many parameters which can change the device lifetime: temperature, oxidation, and voltage/current, etc. For instance, high power devices such as lasers, radars, and server systems could degrade faster as they are running in relatively high temperature. In addition, high voltage and current density often contribute to system breakdown due to electromigration. Electromigration is a diffusion phenomenon in solids due to driving forces such as electric fields and momentum transfer. In other words, high electric fields or higher current densities cause ion transfers that manifest as voids and hillocks in solids as shown in Figure 12. When such voids and hillocks accumulate, devices eventually fail. Electromigration is different from thermomigration; the ion movement occurs as a result of electric effect, rather than temperature effect.

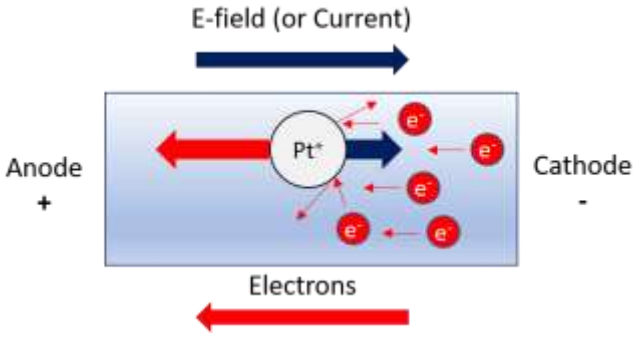

Figure 12. Schematic of electromigration. Ions are migrated to the anode due to collision of electrons flows.

Early studies showed that bulk metals are limited to 10^4 A/cm^2 due to the Joule-heating effect. For thin film metals, such as films deposited on semiconductors, heat dissipation is faster so that the films can carry current density in the range of 10^5 – 10^6 A/cm^2 at below half of the melting temperature [69]. However, electromigration is likely to happen when the current density reaches $10^7 A/cm^2$. One of the requirements for the microheater in chapter 2 is to generate power density up to 1 KW/cm^2 (5 KW/cm^2 for hotspot heater). Given the current heater design,

the current density should increase up to $8 \times 10^6 A/cm^2$ to obtain such a power density and this will increase the probability of electromigration. Also, RTDs should not degrade during thermal tests as the failure of RTDs could provide incorrect temperature information. Therefore, it is necessary to study the reliability of microheater and RTDs to estimate device failure as well as to design reliable thermal test conditions.

One of the most popular methods is to estimate the mean time to failure (MTTF) using Black's equation:

$$MTTF = AJ^{-n}e^{(\frac{E_a}{k_B T})}. \quad (1)$$

where A is constant, J is the current density, n is the current factor, E_a is the activation energy of metal, k_B is the Boltzmann constant, and T is the temperature. Black introduced this equation in 1968 to explain the mass transport of aluminum via momentum transfer and the key parameters of "E_a" and "n" [72]. It is believed that E_a, which is related to thermal diffusion of atoms, is highly influenced by fabrication methods such as type of metallization, pressure, patterning, etc. On the other hand, there have been many discussions about "n". In Black's initial study, he assumed "n" is a constant number and arrived at "2" after theoretical calculation. In 1970, however, Hofman and Breitling argued that the "n" should be "1" instead of "2". They translated the electron arrival rate to atom differently, where it is not a factor of the current density [73]. In addition, they argued that the match between Black's theory and experimentation could have been the result of inaccurate film temperature measurement. In 1971, Blair suggested that "n" is not a constant number and should be defined by the experiment [74]. And in 1991, Lloyd argued that the current factor depends on the failure mechanism such that it is close to 1 if the void nucleation is a dominant failure mechanism. On the other hand, it is close to 2 if the void growth is dominant [75]. Thus, people who have used Black's equation to estimate MTTF, referred the "n" in one of the three ways: i) use of the original Balck's parameter, 2, ii) Referring to numbers from similar works, and iii) extraction of the parameter from experimental results [76]–[79].

In Black's study, aluminum (Al) is used to study electromigration because it is one of the most popular metals in industry. Copper (Cu) and its alloy have been studied as well since they are the major materials for electronic components such as interconnects. Platinum (Pt) is a noble material that is popularly used for heaters, sensors, and electrodes due to its high resistance to temperature and oxidation. Though its reliability for heat and oxidation is well proven, however,

there are very few studies on Pt electromigration. Courbat et al. studied the improvement of reliability by testing different metal adhesion layers [80]. Eliasson et al. used a Pt microwire to study the effect of a DC/AC current on electromigration [81]. Neither study mentioned a current factor using Black's equation. Rusanov et al. did reliability experiments on Pt films made with different adhesion layers and fabrication process [82]. They obtained both "E_a" and "n" by extrapolation of data which are 1.36 ± 0.27 eV and 6.05 ± 1.7 respectively.

In this work, the reliability of thin-film Pt is studied using Black's equation and key parameters are characterized. Although there has been extensive research on electromigration, few studies carefully considered the "n" in terms of temperature. To the author's knowledge, no studies to date have presented empirical "n" for Pt in different temperature levels. Therefore, two different temperature regimes are used for the extraction of "n" and the results are compared. The thin film channel tested in this work consists of 20 nm of Pt and 5 nm of Ti, and four Au electrodes are used for four-probe measurement. The reliability tests are performed in various temperature and current densities and the voltage across the Pt channel is monitored. The resistance of all tested devices increased by 17 - 30 % after tests but it saturated over time. Only a few devices failed after tests. Optical inspection found voids and hillocks on the contact areas where current density is highest. In order to extract parameters, results are plotted with respect the inverse of temperature (1/T). While the result shows a weak correlation when referring to background temperature, the linearity between MTTS and 1/T is significantly improved when the effect of self-heating is included. The extracted "E_a" is 1.47 eV and the relatively higher E_a could be related to the melting point of Pt as well as the adhesion layer. The "n" which is extracted at 180 °C appeared to be 8.6 while it reduces to 6.3 when extracted at 220 °C. The 2.3 of difference could be related to the thermal effect but it is difficult to draw a strong conclusion due to lack of data.

This work was done in collaboration with Andrea Montes in School of Electrical Engineering, National University of Colombia. Montes contributed to the design of current source and voltage readout circuit.

4.2 Experimental Methods

4.2.1 Device layout & fabrication

Figure 13(a) shows the SEM image of device under test (DUT) made of Pt thin-film and Au electrodes. The Pt has U-shaped channel whose width is 20 μm and the bottom contact area has 12 μm width. Current enters the film via one of the bottom electrodes, flowing through the U-shaped channel and finally exits via another bottom electrode. The additional electrodes in the middle are designed for four-probe measurement such that it eliminates the voltage drop from the electrodes and provide accurate voltage across the DUT. While the DUT is running, a nearby device can monitor temperature during tests as it works as resistance temperature detector (RTD). Microheaters have serpentine shapes surrounds the DUT and the heaters allows tests to be run at desired temperature. Both DUTs and background heaters are microfabricated on a silicon substrate with 200 nm of thermally-grown silicon dioxide. The main fabrication steps are: i) DUT and background heater patterning by photolithography, 2) metallization of 5 nm of Ti and 20 nm of Pt, 3) lift-off metals by photoresist removal, 4) contact patterning by photolithography, 5) metallization of 20 nm of Ti and 400 nm of Au, and 6) metal lift-off by photoresist removal. The fabricated chip is bonded to a custom-designed printed circuit-board (PCB) and wirebonded using Au wires for electrical interfaces. Figure 13(c) and (d) show the finalized test chip and PCB. A detailed information is described in Chapter 2.2.

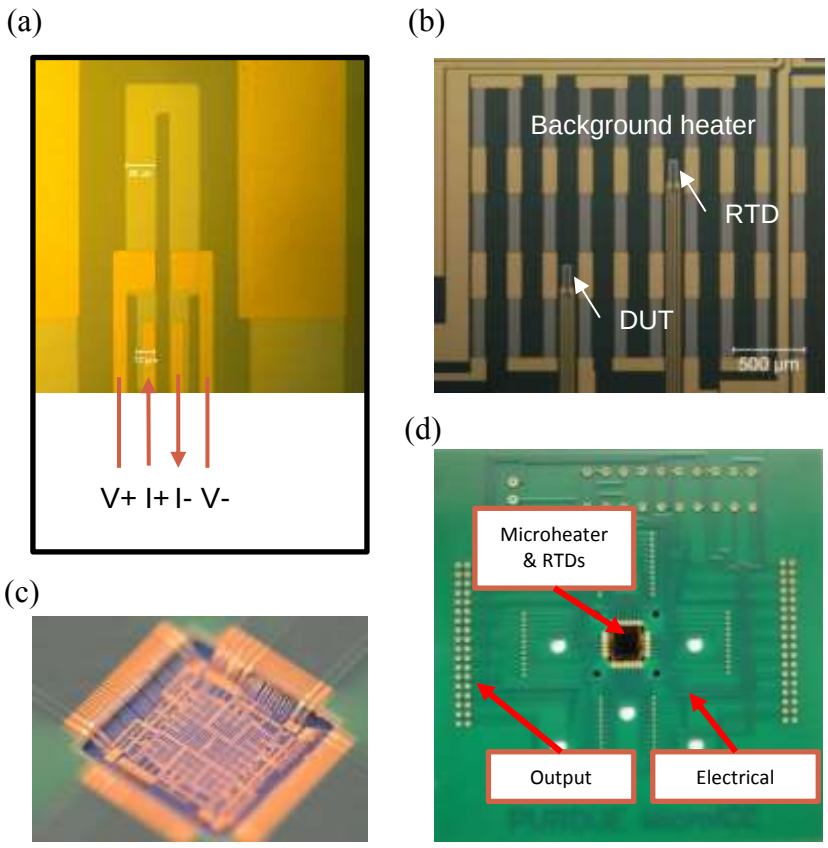

Figure 13. (a), (b) Microscope image of test chip. The U-shaped channel and heater (gray) are made of Pt and the electrodes (yellow) are Au. Background temperature is controlled by heater activation and RTD is placed nearby to monitor DUT temperature. (c) Wirebonded test chip and (d) Assembled chip and PCB

4.2.2 Test setup

The test setup consists of three parts; i) current source, ii) voltage readout, and ii) control & monitoring of temperature. The current source is designed to provide constant current to the DUT during tests. A linear voltage regulator (LT3083, Linear Technology) is used to build a current source and the output current level is determined by an output resistor (R_{out}) and feedback resistor ($R_{control}$) as shown in Figure 14. Since voltage across the load (DUT) changes during tests, a simulation study was done to evaluate the stability of current level with respect to change in load resistance. Table 3 shows the output current at different DUT resistance and current level is stable up to 50 mA when DUT resistance is 400 Ω (nominal DUT resistance: 200

Ω). The list of test current densities is shown in Table 4. An additional power supply is used for current level higher than 55 mA and a constant 5 mA is applied for RTDs.

The DUT voltage is read through the USB interface (NI USB 6215) but the voltage needs to be adjusted due to the limitation of voltage reading (10 V maximum). Therefore, the voltage signal is first amplified by addition of a reference voltage which is provided by a Zener diode (1N4734, Digi-Key) and the added signal is reduced using a voltage divider circuit at a known ratio. The adjusted signal is recorded in real-time using LabVIEW and converted into original signal. The device temperature is monitored by RTD and the background heater is controlled by an individual power supply.

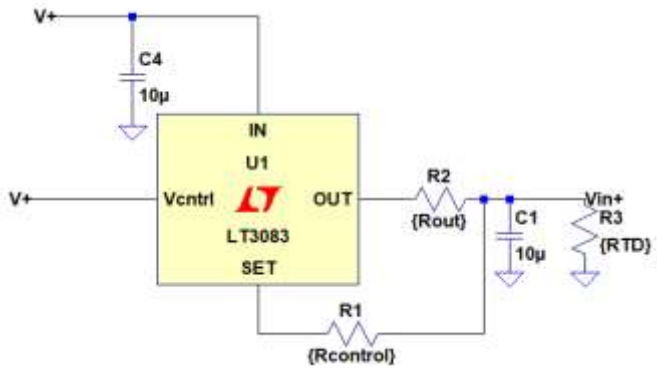

Figure 14. Circuit diagram of current source. The current range is determined by R1 and the precise control is done by changing R2. R3 represents both DUT and RTD.

Table 3. Calculated current levels at various DUT resistances.

Load (DUT) Resistance (Ω)	Current (mA) R_{out}=10 Ω, $R_{control}$=10 KΩ	Current (mA) R_{out}=15 Ω, $R_{control}$=10 KΩ	Current (mA) R_{out}=10 Ω, $R_{control}$=5.1 KΩ	Current (mA) R_{out}=20 Ω, $R_{control}$=5.1 KΩ	Current (mA) R_{out}=10 Ω, $R_{control}$=2 KΩ	Current (mA) R_{out}=20 Ω, $R_{control}$=2 KΩ
100	49.86	33.46	25.47	12.81	9.97	5.03
200	49.91	33.47	25.47	12.81	9.97	5.03
300	49.98	33.48	25.48	12.81	9.97	5.03
400	49.79	33.49	25.48	12.81	9.97	5.03
500	40.49	33.49	25.48	12.81	9.98	5.03

Table 4. List of test current level and current density

Current (mA)	Current density (A/cm^2)
7.5	1.4×10^6
14.3	2.8×10^6
29	5.8×10^6
55.4	1.1×10^7
63	1.26×10^7
70	1.4×10^7

4.2.3 Calibration

Prior to tests, all devices are annealed and calibrated. The as-fabricated chip is first annealed using microheater for 8 hours at 150 °C. A clear decrease in resistance is observed from all devices after annealing and the post-anneal resistance remained stable. The annealed chip is then calibrated using laboratory oven and the resistance of each device is recorded at different temperature. A thermocouple is placed nearby the device to track oven temperature. Figure 15 shows the resistance shifts with respect to temperature at 20, 40, 69, and 96 °C respectively. The linearly extrapolated curve matched well with the measured resistance value such that it can provide the corresponding temperature information during tests with an accuracy of ± 1 °C.

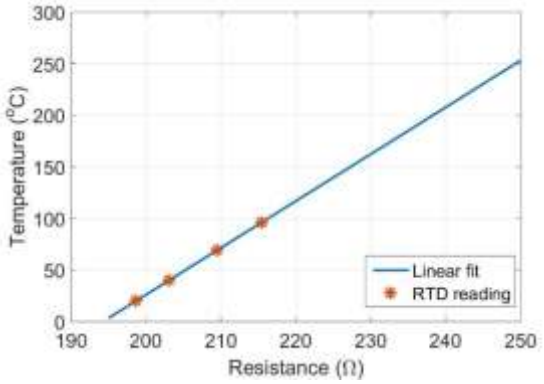

Figure 15. Calibration results of RTDs. The linearly extrapolated curve (blue) matches well with the resistance of RTDs. Temperature is estimated by monitoring the resistance shift of RTD.

4.2.4 Test method

The initial DUT voltage is recorded at the start of test at room temperature (21.3 °C, relative humidity: 33 %). After 5 minutes of recording, the microheater is turned on with desired power level and held constant for 20 minutes for the saturation of temperature. Once the temperature saturates, the current source starts to provide current to DUT at a desired level and

the DUT is monitored for minimum 5 hours or until there is no change in voltage reading. After running tests, both current source and the microheater are turned off and the DUT is allowed to cool down for 20 minutes. Once the device temperature reaches room temperature, the DUT voltage is measured again in order to determine a “final” resistance. Finally, the tested devices are inspected using optical microscope.

4.3 Results & Discussion

4.3.1 Effect of current & temperature

Figure 16(a) shows the resistance response for the first 15 hours at different current density when chip temperature is 180 °C. Since temperature instantly increases with current source initiation, the chip temperature is referred from temperature after 5 minutes of current source initiation. Once the current source starts providing current, the DUT resistance increased correspondingly. The difference in initial resistance is because of both temperature variation as well as fabrication nonidealities. It is interesting to note that the resistance saturates over time for all devices. And the saturation time is reduced as either current or temperature increases. For instance, the resistance saturated in about 30 minutes when current is 70 mA, but it takes more than 5 hours until saturation when current density is 63 mA or lower. At T = 220 °C, the saturation happens faster as shown in Figure 16(b). Once the resistance saturates, no more increase in resistance is observed from all devices and only a few devices failed abruptly. The spikes from the 29 mA result is due to artifacts from measurement. No data is recorded after 9 hours for the test with 63mA at 220 °C.

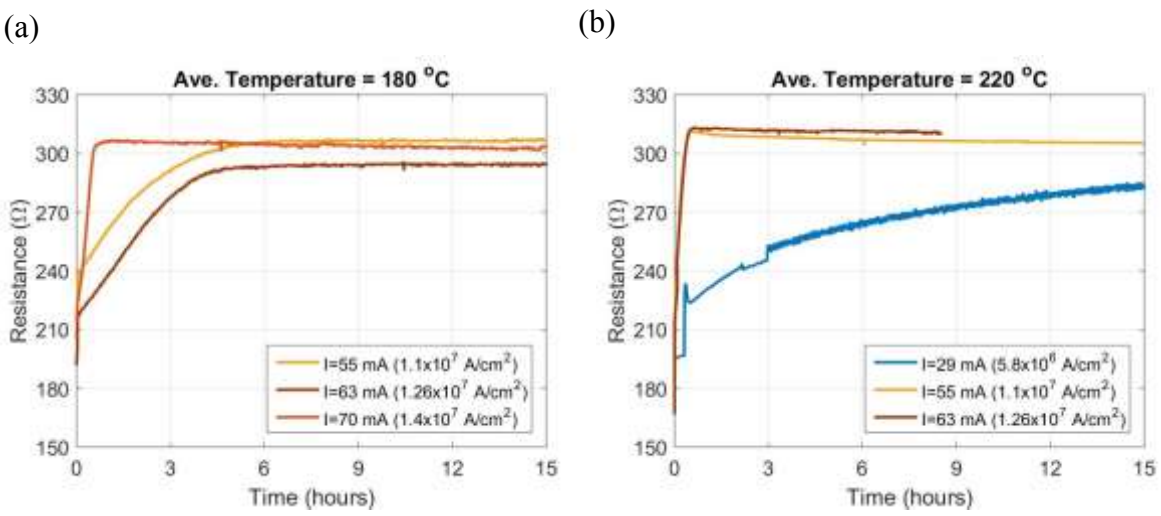

Figure 16. First 6-hour resistance change of DUTs at (a) 180 ± 5 °C and (b) 220 ± 5 °C. Each curve represents data from individual device which are tested at different current densities.

Table 5 shows the experimental results for all tested devices at various current densities and temperatures. All devices showed increased resistance by 17 – 31 % compared to the initial resistance. Figure 17(a) shows the microscope image of DUT after test. While no clear damages are observed on the 20 μm-width Pt channel area, a black chunk of hillock is formed at the left contact area. Since the channel width is reduced from 20 μm to 12 μm at the bottom contact, the local current density is higher in this region than in the overall DUT. Thus, the migrated ions are likely to piled up at this bottleneck. Figure 17(b) shows a void formed at the bottom right contact of the failed device. Although the recorded voltage includes the 20 μm-channel via the middle electrodes, the void/hillock made beyond the electrodes will not be reflected on the voltage measurement, explaining sudden failure of DUT without increased resistance. A higher resolution imaging analysis like SEM will be necessary to understand the failure mechanism on the device.

Table 5. Summary of reliability tests. ΔR/R refers to the fractional change in resistance before and after test.

Current (mA)	Background temperature (°C)	RTD temperature (after current on) (°C)	Saturation time (hour)	ΔR/R (%)
7.5	156	241	125.9	21
14.3	164	249	107.2	21
29	140	225	36.64	Failed in 102 hours
55.4	158	152	90	23
	123	184	5.94	26
	135	218	0.55	17
	167	220	0.50	27
	200	251	0.11	Failed in 7 hours
63	101	180	4.67	31
	131	217	0.37	23
70	21	124	17.05	31
	80	177	0.77	24

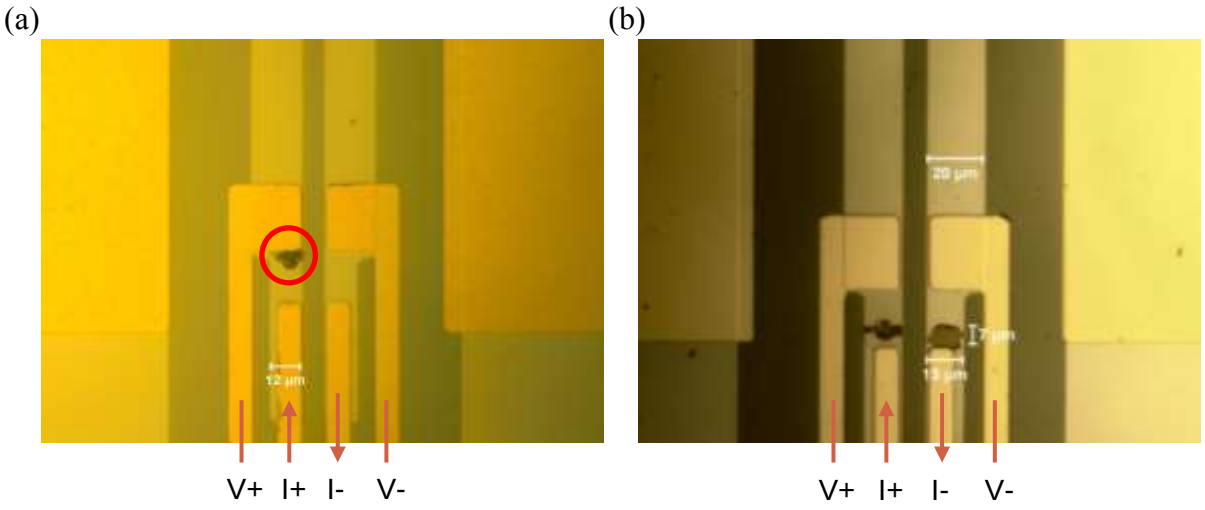

Figure 17. Microscope images of DUT after tests. (a) Atoms are accumulated on the bottleneck of Pt channel. (b) A void on the failed device. It is made in the cathode side and hillocks are formed on the anode side as a result of electromigration.

4.3.2 Failure time estimate

To quantitatively understand the effect of current and temperature, the Black's equation is used. Two parameters, "n" and "E_a" must be known to estimate the mean time to failure (MTTF). Taking the logarithm to the Equation (1) yields:

$$\ln(MTTF) = \ln A - n \ln J + \frac{E_a}{k_B T}. \quad (2)$$

In other words, "E_a" is the slope of the linear equation with respect to $1/k_BT$ for a known current density, J. On the other hand, "n" is the slope of the linear equation with respect to ln J when the temperature (T) is constant. Though the MTTF generally refers to the "failure time" of DUT as a result of open circuit or permanent resistance increase by allowable limit, there is no standard criteria for defining failure. In this work, all devices showed 17 – 31 % of increased resistance after test but measuring accurate failure time is challenging as the degradations are likely to happen beyond voltage measurement range. To make all results consistent, therefore, the MTTF here is defined as the "mean time to saturate" (MTTS) where it measures the time for DUT voltage to saturate and become constant as shown in Table 5.

Regarding the estimation of temperature, two approaches are used. The first method is to refer to the temperature surrounding the device; it is popularly used when the Joule heating from the DUT is negligible such that the temperature change from DUT is negligible. The second method is to refer to DUT temperature; For devices tested with high current densities, Joule heating is not negligible anymore and additional temperature monitoring method is necessary. For instance, thermocouple or IR-camera can be used to monitor DUT temperature during tests. Figure 18(a) shows the MTTS when the background temperature is used. When linearly extrapolating results, it shows a weak correlation with respect to data. This indicates that the Joule heating from DUT is not negligible. A separate thermal test without background heating is performed to estimate temperature change due to DUT. About 1.15 W of heat (I = 70 mA) from DUT increases the chip temperature by 100 °C which is equivalent to the temperature increase from the background heating. Thus, Figure 18(a) is replotted with respect to the RTD temperature, where heating is included by both background heater and DUT. Figure 18(b) clearly shows the effect of temperature and current on the MTTS of the device. The extrapolated line (red) using the results with 55mA indicates that the MTTS decreases exponentially with

increasing temperature. Also, the vertically extrapolated lines (black) show the decreasing MTTS with increasing current density.

(a) (b)

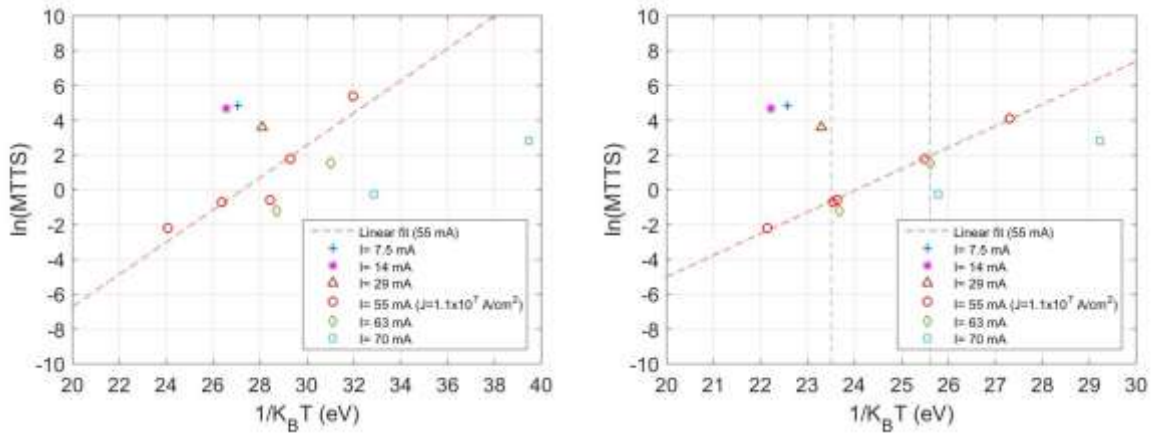

Figure 18. Logarithmic plots of MTTS with respect to $1/k_BT$. Two different temperature are used: (a) background temperature only and (b) sum of background and DUT temperature.

The activation energy "E_a" and "n" are extracted from the experimental results. According to the Equation 2, the E_a is the slope of the linear extrapolation of MTTS from a constant current density (red) as shown in Figure 18. Thus, the E_a is calculated using the results with the current density of 1.1×10^7 A/cm^2 and it becomes 1.47 eV. To calculate the "n", the MTTS which were tested at 180 ± 5 °C and 220 ± 5 °C are replotted with respect to lnJ and extrapolated as shown in Figure 19. The calculated "n" becomes 8.6 for 180 ± 5 °C and 6.3 for 220 ± 5 °C. It should be noted that the data points are not at exactly same temperature; because the MTTS changes exponentially with respect to temperature, the slope could change correspondingly. If exactly fitting to T = 220 °C, for instance, the MTTS of 29 mA (Δ) increases while that of 63 mA (◊) decreases. Finally, the MTTS of DUT can be estimated based on the extracted parameters.

$$MTTS = A \times J^{-6.3\ or -8.6} \times e^{\frac{1.47}{k_B T}} \quad (3)$$

where the constant "A" can be obtained by calculation the y-intercept of the extrapolated line in Figure 18. Table 6 listed MTTS for various current densities and temperature. The MTTS varied by 10 - 100 hours depending on the "n".

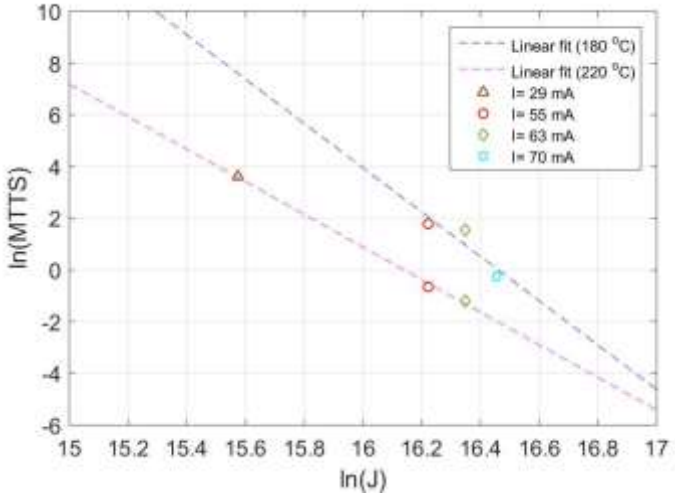

Figure 19. Logarithmic plots of MTTS with respect to lnJ. "n" is the slope of the linearly extrapolated curve. Two "n" are calculated at different temperature: 180 ± 5 °C and 220 ± 5 °C.

Table 6. Saturation time estimate using Black's equation.

Current (mA)	Current density (A/cm^2)	Temperature (°C)	MTTS (hours)
55	1×10^7	150	378-478
55	1×10^7	175	40-50
82.5	1.5×10^7	150	15-29

4.3.3 Comparison of activation energy and current factor

The extracted parameters are also compared with other studies. It is known that the "E_a" heavily depends on materials, the quality of film such as evaporation and pressure, etc. Comparing with the "E_a" of other materials, which are 0.48-0.6 eV for Al and 0.77-0.81 eV for Cu respectively, the "E_a" is higher than others [82]. This is because of the relatively higher melting point of Pt. For instance, Ascoli et al. extracted the activation of Pt using Pt microwire and reported 1.23 eV [83]. In addition, the Ti adhesion layer which hold Pt atoms against electromigration may results in a higher "Ea" than the previous study.

Regarding the "n", the absolute numbers are higher than previously reported numbers which varied from 1 to 2.4. Rusanov et al. reported experimental results on Pt films made with 300 nm of Pt and 15 nm of Ti [82]. They obtained "n" by extrapolation of data which is 6.05 ± 1.7. This higher "n" could be the effect of Joule heating, type of degradation, and plasticity etc. [84]. While the difference of 2.3 in the two extracted "n" could also be the results of such effects,

it is difficult to draw strong conclusions about the “n” due to the lack of data at various current densities and temperature.

4.4 Conclusion

The reliability of thin-film platinum is studied under various conditions. The resistance of tested devices increased by 17 – 31 % over time and becomes saturated. The saturation time highly depends on the applied current density and device temperature. Only a few devices failed in the given times and voids and hillocks are observed on the narrow contact area where current density is highest. Since the most degradations happen beyond the voltage measurement area, abrupt failures are observed on the voltage reading rather than continuous increase in resistance. It appeared that self-heating from device is not negligible compared to background temperature and the linearity between MTTS and 1/T is greatly improved when the self-heating is accounted on temperature. The extracted activation energy is 1.47 eV for 20 nm of Pt with 5 nm of Ti adhesion layer. The current factors are extracted in two different temperature regimes (180 ± 5 °C and 220 ± 5 °C) and they are 8.6 and 6.3 respectively. While temperature effect such as Joule heating could be a reason for the variation in the current factors, more experiments at diverse current densities and temperature will be necessary for clear understanding.

5. DEVELOPMENT OF INTERDIGITATED CAPACITIVE SENSOR AND MICROHEATER INTEGRATION FOR REAL-TIME MONITORING OF SUB-MICRON AND NANOSCALE PARTICULATE MATTERS

5.1 Introduction

Particulate matter (PM) is a mixture of particles and droplets in air consisting of various compounds. PM exists everywhere in various sizes and some of the particles are toxic and respirable to human. Some work environments have more dangerous respirable particles than others and can cause harmful effects to human through inhalation. Miners in the mining environment are often exposed to higher level of hazardous particles such as coal, silica (SiO_2) and diesel exhaust, and continuous exposure to such particles can cause severe damage to the human respiratory system. For instance, exposure to mine dust can cause coal workers' pneumoconiosis (CWP), also known as black lung disease, which is very common in coal miners; it is reported that about 4,800 people in U.S. died because of CWP from 2005 to 2014 [85]. Workers mining minerals are at high risk for silicosis as they are exposed to mine dust containing high amount of silica. Accordingly, the National Institute for Occupational Safety and Health (NIOSH) recommends that workers' exposure to respirable coal mine dust should be limited to 1 mg/m^3 and crystalline silica should be limited to 0.05 mg/m^3 (up to 10 hours per day over a 40-hour work week) [86].

Some devices have been commercially developed to monitor air quality or collect airborne particles in the mining environments. The two broad approaches are: i) gravimetric filter sampling for particle collection and ii) direct reading of particle mass concentration. The gravimetric sampling is one of the oldest and most popular methods, since it was first introduced in 1950s. Higgins and Dewell first designed a personal sampler consisting of cyclone, filter holder and a small pump and workers wore the apparatus during work hours [87]. The concentration of dust is calculated by the average mass gain over the sampling time. The filter is then analyzed via electron microscopy and x-ray diffraction spectroscopy (XPS) to examine the accurate concentration and components of the collected particles such as silica [88], [89]. However, the gravimetric method requires several hours to collect enough particles and the samples are sent out for accurate analysis of the particles. On the other hand, direct reading of particle concentrations has been developed with various monitoring techniques. In 1973, Gravati

presented a light scattering method to measure size distribution of PM in real time. This method has been developed to monitor PM concentrations by translating the sampler's light scattering into the corresponding concentration [90], [91]. Personal/DataRAM (pDR) is one of the commercial devices which use the light scattering method and it is often used in underground gassy mines for making rough relative measurements [92]. Personal dust monitor (PDM) is another type of real-time instrument that uses a tapered-element oscillation microbalance (TEOM) to monitor the coal-dust concentration in the mining environment. TEOM was first introduced by Wang et al. where a replaceable filter cartridge is mounted to the tip of the tapered element, which oscillates like a tuning folk during operation [93]. The oscillation frequency changes in real-time with respect to the mass collected on the filter and the integrated particle mass can be analyzed by gravimetric method after measurement. The TEOM-based PDM is now a mandatory instrument to monitor dust exposure for workers in underground coal mines [94].

The advancement of nanotechnology naturally brought attention to the hazard of nanomaterials and the necessity for higher resolution monitoring systems. This concern is now raised to work places handling nanomaterials as well as underground mines [95], [96]. According to Heyder et al., particle deposition efficiency in the human respiratory track varies with particle diameter; while the highest efficiency (~90 %) is at particle diameter of 10 μm and reduces to 15 % with decreased diameter, the efficiency starts increasing again when the diameter is 0.2 μm. The efficiency reaches almost 80 % with particle diameter of ~0.01 μm [97]. Moreover, such particles can penetrate deep into the lung or other organs by circulating through the body. However, due to the smaller volume of particles as well as their smaller mass, detecting sub-micron and nanoparticles using current methods is challenging since it requires orders of magnitude higher sensitivity compared to detecting microscale particles. Moreover, the effect of temperature and humidity becomes more critical as higher precision is required. For instance, commercially available PM sensors are difficult to detect ultra-fine particles due to noise from temperature and humidity. The use of pDR is inhibited as it is impacted by moisture in the mine air and calibration using gravimetric measurement is necessary [92]. Therefore, it is not recommended for environments where accuracy is the topmost concern. In addition, NIOSH reported in 2013 that TEOM technique is not suitable for monitoring nanomaterials in the mining environment [98]. Mine dust contains a portion of respirable particles in nanometer sizes as well

as in microscale. However, current devices are mainly affected by larger particles while the response from smaller particles are masked by the response of the larger particles.

Several studies have shown the possibilities of high-resolution particle detection sensors using advanced technologies such as microelectromechanical systems (MEMS). Sensors made with microfabricated cantilevers [99] or acoustic resonator [100], [101] allow the detection of airborne particles whose masses are from pico-gram (pg) to nano-gram (ng). Hajjam et al. designed a micromechanical acoustic resonator and detected individual particles of 1μm diameter (1-2 pg) using a table-top network analyzer [102]. On the other hand, Techniques using optical scattering has also developed to detect smaller particles. Commercial optical particle counters (OPC) have detection limit around 0.3 μm by analyzing the scattered light. Particles with tens of nanometers are difficult to detect due to the limitation of wavelength; Rayleigh scattering occurs when particle are much smaller than the wavelength of light (i.e. ~ 1/10 of the wavelength). The state-of-the-art technology such as scanning mobility particle sizer (SMPS) detects such nanoparticles by enlarging them using condensation in a supersaturated gas, reaching a detection resolution of few nanometers [103]. In addition, detection of single nanoparticle can be achieved using optical microcavities [104] and nanofiber arrays [105]. In spite of the improved sensor sensitivity, there are limitations on the miniaturization of system; the optical scattering technique requires a laser source, multiple photodetectors, and a closed chamber to minimize environmental effect [106]. This may be overcome with advanced semiconductor technologies such as laser diodes, but nanoparticle detection with condensation needs additional equipment such as condenser and alcohol reservoir [107]. MEMS cantilevers and microcavities could be portable but it is still difficult to detect ultra-fine particles without laboratory equipment due to noise [108], [109].

Unlike the methods mentioned above, capacitive sensors detect particles by capacitance shift due to the dielectric properties of deposited particles. Evans and York first demonstrated a sensor chip for particle detection using interdigitated capacitive sensor [110]. The sensor chip includes a sensor array and readout circuit, and they showed 60 atto-farad (aF) of capacitance shift for a 50 μm particle deposited on the sensor. Ciccarella et al. demonstrated a capacitive sensor with low noise readout circuitry and measured 10 aF capacitance shift with a 5 μm diameter mineral talc particle [111]. Both works used custom-designed readout circuits to avoid the use of laboratory equipment and integrated with sensor in a single board. Due to electrical

interface of capacitive sensor, it allows an easy integration with readout circuits. Therefore, it has more potential for miniaturization than other techniques such that the capacitive sensor can be integrated with generic air sampling cassette, or pocket-sized sensor and smartphone-embedded sensor can be made [112].

While the previous capacitance sensing approaches demonstrated microscale particle detection, sensor response on sub-micron and nanoscale regimes were not studied. In this work, we aimed to design and fabricate a capacitive sensor for respirable nanoparticles. The proposed interdigitated capacitance sensor has detection capability of sub-micron and nanoscale particles in 1 mm × 1.5 mm sensing area. This miniaturized sensor enables an easy integration with standard sampling cassettes minimizing the interference of air flow for particle collection. The readout board utilizes resistance-capacitance (RC) delay time constant to monitor capacitance shift due to particle deposition in real-time and it is separately designed for re-use. The sensor showed a clear response with respect to particle deposition; and the positive capacitance shift is consistent with the increased sensor counting. Among the collected particles on the sensor, about 77 % are sub-micron particles with diameter below 1 μm and 23 % are microparticles. Most of the microscale particles appeared to be agglomerates of sub-micron particles. A comparison with simulation study shows that the capacitance shift is proportional to the volume of particles. The concentration of the collected particles on sensor is compared with a standard gravimetric method, and less than three orders of magnitudes of particle mass is responsible for sensor response. The added microheater allows the sensor temperature to be maintained at constant temperature above dew point. Finally, the sensor response is represented as standard airborne particle concentration expression showing a prototype of a real-time personal particle monitoring system.

This work was done in collaboration with Daniel Theisen in Department of Environmental & Radiological Health Sciences, Colorado State University under the guidance of Professor Candace Su-Jung Tsai, and with Weeseong Seo in School of Electrical and Computer Engineering, Purdue University. Theisen contributed to the design of personal sampling cassette and gravimetric measurement, which were done in Colorado State University. Seo contributed to the design and characterization of readout circuitry.

5.2 Device Fabrication

5.2.1 Sensor design & fabrication

The capacitive sensor was designed to be directly integrated with standard air sampling cassettes which use 25 - 37.5 mm filter. To demonstrate the capacitive sensor response, a custom-designed sampling cassette (Tsai Diffusion Sampler, TDS) is used [113]. The sampling cassette allows the selection of sub-micron particles while rejecting larger particles: the mass median aerodynamic diameter (MMAD) is 3.8 μm. The layout of sensor was determined such that it minimizes the air flow interference when integrated with the sampling cassette and facilitates easy connection with the readout board. Thus, the sensor has a rectangular shape with dimensions of 2 mm × 20 mm, as shown in Figure 20. The interdigitated patterns provide maximum sensitivity in a given area where electrodes with different polarities are interchanged. The width of metal electrodes is 2 μm and two different electrodes spacings are designed which are nominally 2 μm and 3 μm respectively. The electrodes spacings are chosen based on projected fabrication yield. The sensor is located at one end of the strip, and the actual sensing area is 1 mm × 1.5 mm. The calculated nominal capacitances are 6.23 pF for 2 μm-spacing and 4.98 pF for 3 μm spacing, according to the equation of interdigitated capacitor [114].

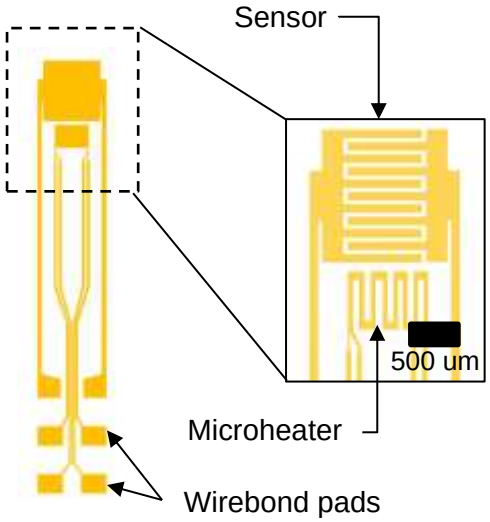

Figure 20. Interdigitated capacitive sensor strip layout.

The sensor strip also includes a resistance-based microheater suitable for maintaining the sensor at an elevated temperature; this capability provides a means to mitigate the effects of

condensation/water droplets and enhances the stability of the capacitance. In addition, direct integration of microheater on sensor reduces the complexity of installing a heater inside the sampler, avoiding extra interfaces for heaters. The serpentine pattern is used in order to maximize the resistance (minimize the current) in the limited area, and four electrodes enable accurate temperature measurement as well. While silicon substrate provides solid and high fabrication yields, its high parasitic capacitance reduces the effect of capacitance change from the sensor. Polyimide has lower relative dielectric constant ($\varepsilon_{polyimide}$: 3.4) than silicon (ε_{Si}: 11.68) such that it minimizes the parasitic capacitance from the substrate.

The cross-section of sensor fabrication is drawn in Figure 21(a). A 127 um-thick polyimide film (Kapton HN, CS Hyde Company) was first degassed under vacuum oven for 8 hours to remove any remaining bubbles from the film. It is then cut into square pieces and solvent-cleaned in the cleanroom facility. MCC Primer adhesion promotor (80/20, Microchem) was applied onto the polyimide substrate using a spin coater (Specialty Coating Systems G3) followed by AZ 1518 positive photoresist. The photoresist layer is exposed using a mask aligner (Karl Suss MJB-3) and developed in MF-26A developer (Dow Electronic Materials MEGAPOST). Once the patterns are defined, 20 nm of Titanium (Ti) and 400 nm of Aluminum (Al) are deposited via electron beam evaporation (Airco Temescal, System Control Technologies). This was done at a pressure level of 2.0×10^{-6} torr and the deposition rate was 1.0 – 2.0 Å/s. A lift-off process is performed by stripping off the photoresist using acetone. Figure 21(b) shows the sensors fabricated on polyimide substrate and 24 sensor strips in a 3 cm × 4.5 cm area. Figure 21(b) and (c) shows the sensors fabricated on polyimide substrate.

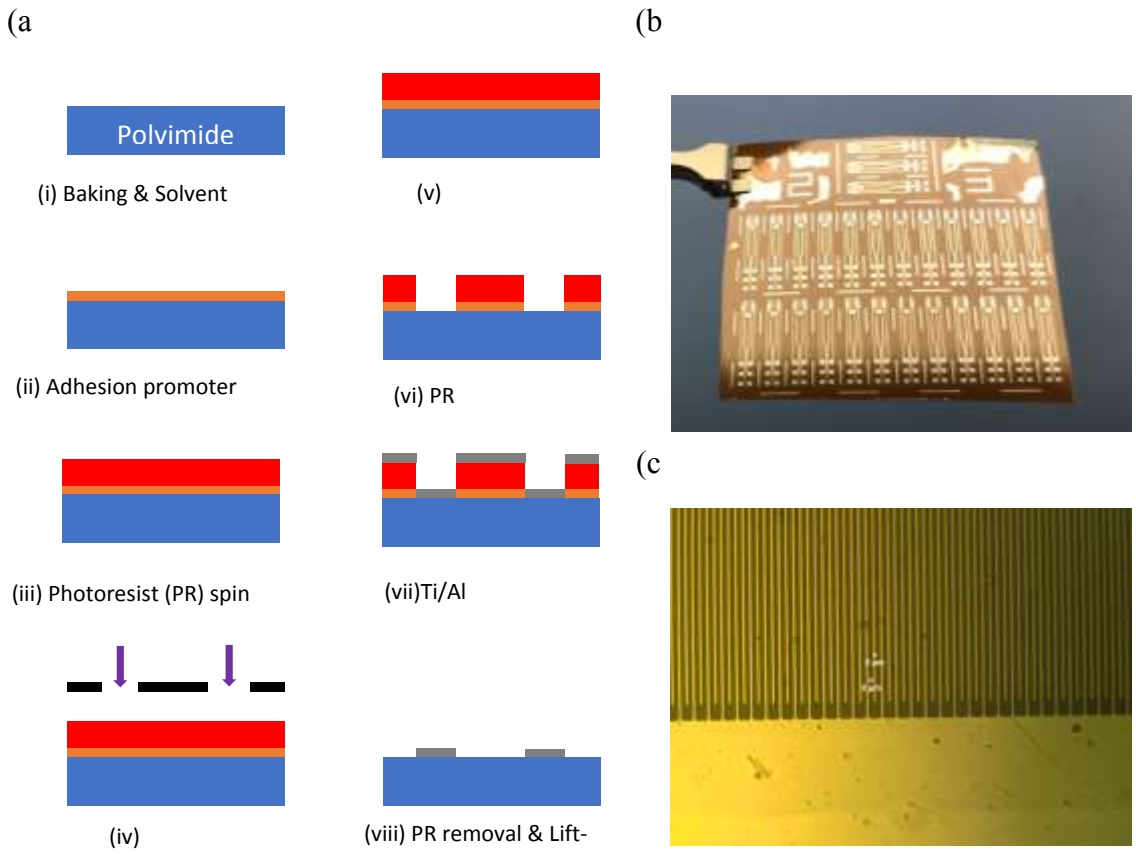

Figure 21. (a) Cross-section of sensor fabrication process, (b) photograph of polyimide substrate containing sensor strips, (c) Microscope image of the interdigitated capacitive sensor.

5.2.2 Interface PCB

To facilitate integration with the sampling cassette as well as the readout board, a custom-designed interface printed circuit board (PCB) is made. The interface PCB enables robust electrical and mechanical connections to the readout board, via the pin header connections. Figure 22(a) shows the interface PCB with sensor strip mounted. The sensor and microheater are wirebonded to the PCB using gold wires. Like batch-fabricated sensor strips, low-cost interface PCBs are also disposable.

5.2.3 Integration with sampling cassette

The top portion of the sampling cassette was also modified from the original design so that the sensor could be inserted into the cassette. A detailed description of the original sampling

cassette design was previously published [113]. The modification includes a 10 mm-long stand to support the sensor chip and an opening of 2.5 mm-height and 10 mm-width. To measure particle concentration after test, a polycarbonate filter covering the entire cross-section of air flow is placed on the bottom portion. The sensor is then inserted through the opening and located on the filter surface. A simulation study using a computational fluid dynamic program proved that particle distribution inside the sampling cassette depends on the particle size; whereas particles smaller than 3 μm are uniformly distributed over the filter area, particles larger than 3 μm are preferentially located in the center area. To avoid contributions from large particles, the sensor is located approximately 2.5 mm away from the center as shown in Figure 22(b). After the sensor placement, the opening was sealed using paraffin wax film to avoid air leakage. The assembled sensor (Figure 22(c)) is finally installed into the readout board as shown in Figure 22(d). The whole system has a dimension of 12 cm × 3 cm × 4 cm with total weight of 37 g.

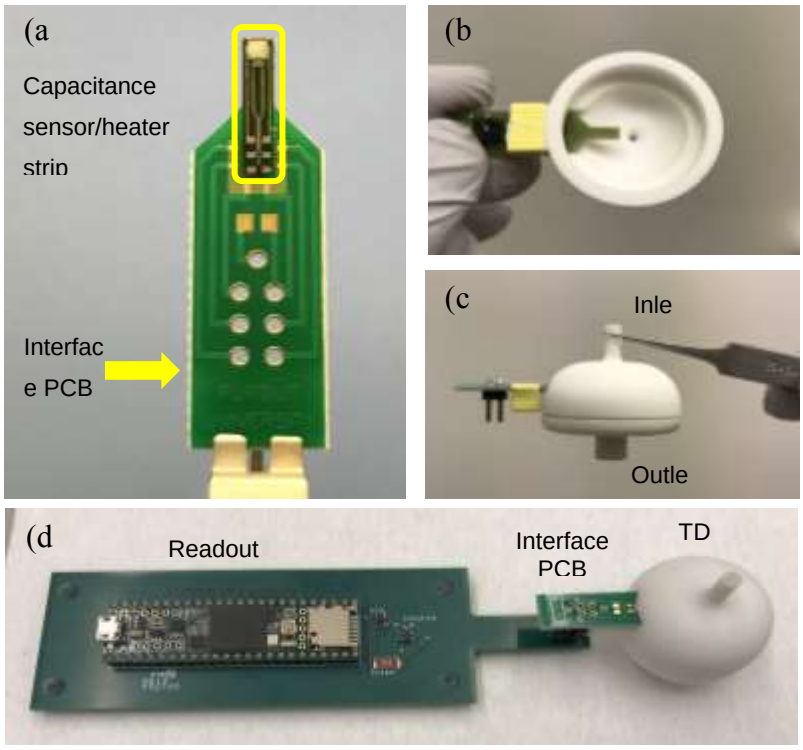

Figure 22. Photographs of (a) capacitance sensor/heater strip mounted on interface PCB; (b) and (c) strip/interface PCB assembly mounted in a modified sampling cassette, showing bottom and side views, respectively; and (d) a fully assembled system. The sensor/cassette assembly is electrically connected to the separately designed readout board. The readout board can be re-used.

5.2.4 Readout circuit

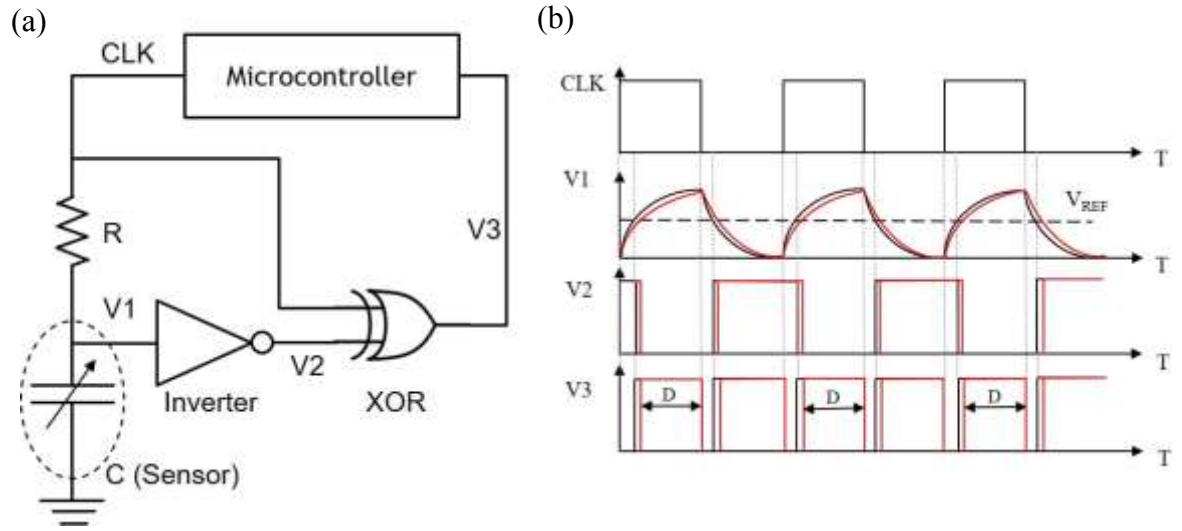

Figure 23 shows an ideal response of the circuit and a block diagram of the sensor and readout circuit. The integrated readout approach measures the time constant of an electrical circuit consisting of the capacitance sensor and an external resistor (100 MΩ ± 5%, Bourns Inc.). The operation procedure is as follows: i) The microcontroller (Teensy 3.6, PJRC) generates a clock signal (CLK) of 100 Hz (square wave, 50 % duty cycle), ii) the resistance-capacitance delay (RC delay) influences the clock signal depending on the RC time constant (V1), iii) it is then transformed into a square wave signal (V2) after passing the inverter (SN74AUP1G04DBVT, Texas Instrument), iv) the output of the inverter is fed into the XOR gate (74HC1G86GV, Nexperia USA Inc.) and compared with the initial clock signal, v) the final XOR output (V3) is then sent back to the microcontroller. The duration of each output pulse is counted by the microcontroller and the counting results of 500 pulses are averaged. Counting interval (minimum detectable pulse width) is set to 1 microseconds (μS) and the switching threshold of the inverter is set to 0.5 V_{DD}. The "rise" pulse in V3 appeared to be more sensitive than the "fall" pulse and this could be related to the value of V_{REF}. Therefore, only the "rise" pulses are chosen for counting. As the capacitance of the sensor increases due to particle deposition, the corresponding increase in the time constant of the RC circuit is converted into a shift in counts in a sampling circuit, realized by the microcontroller. The data from the microcontroller can be downloaded through a USB port.

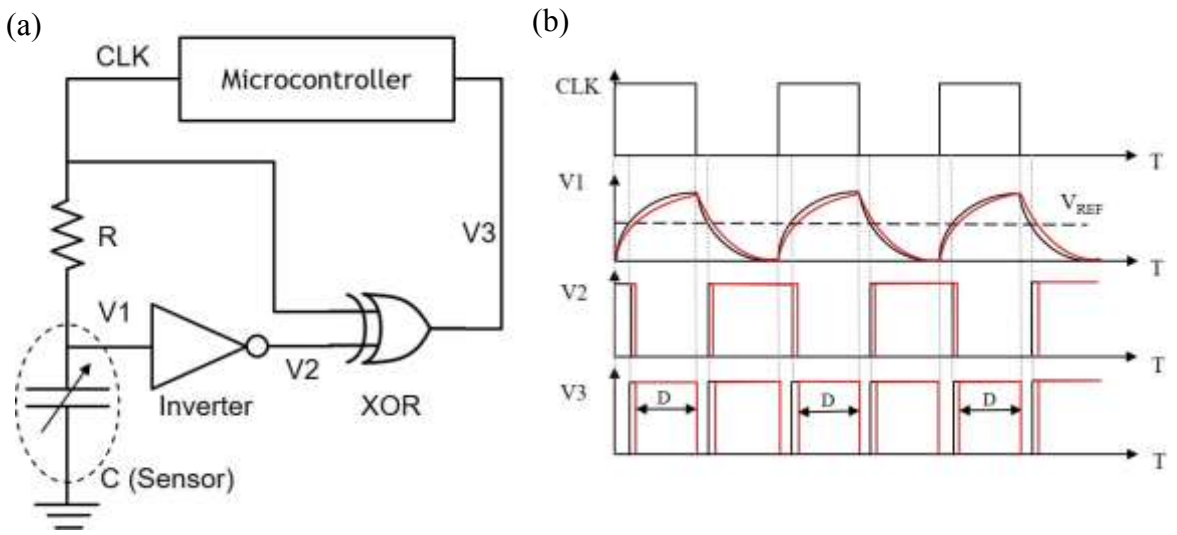

Figure 23. (a) The block diagram of capacitive sensor and readout configuration and (b) ideal response of sensor readout.

5.3 Results & Discussions

5.3.1 Calibration & test set up

The integrated sensor and readout board were calibrated before testing. To confirm the capability of sensor reading, fixed capacitors with known capacitance values are used, as shown in Figure 24. Because the readout board itself has a fixed resistance and parasitic capacitance, the initial counting does not begin from zero. The results showed that counting increased linearly with increasing capacitance. After calibration with the fixed capacitors, the actual capacitive sensor chips were compared. For the 2 µm-spacing sensor chips, the measured capacitances ranged from 11 to 12 pF and the 3 µm-spacing sensor chips have capacitance of 7 - 8 pF. Comparing with the nominal capacitances of 2 µm and 3 µm-spacing sensors, which are 6.23 pF and 4.98 pF respectively, the higher measured values should originate from the parasitic capacitance of the interface PCB as well as fabrication nonidealities. The counting of two sensor chips (8.03 pF and 11.54 pF) matched well with the linearly extrapolated curve whose inverse of the slope is about 15 femtofarad (fF)/count. The measured capacitance values with a tabletop capacitance meter has an accuracy of ± 0.02 picofarad (pF) and the counting accuracy is ± 0.5.

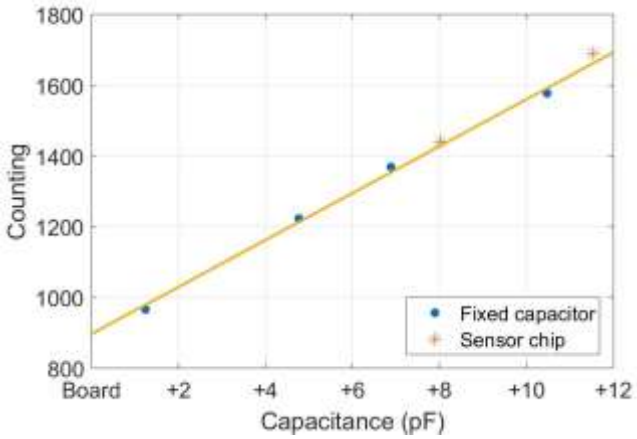

Figure 24. Readout circuit calibration using fixed capacitors. Fixed capacitance values are 1.24 pF, 4.76 pF, 6.88 pF, and 10.47 pF respectively. The tested sensor chips fit to the linearly extrapolated curve (yellow).

5.3.2 Test with road dust

The capacitance sensing approach was demonstrated with test dust, with the capacitance sensor mounted in the sampler. A custom-designed test chamber (20 cm × 20 cm × 20 cm) is prepared and two openings are made on the side wall and the top side respectively. The assembled modified sampler was installed on the outside of wall, and the inlet of the sampler was inserted through an opening. The outlet of the sampler was connected to an air pump for constant air flow (0.3 L/min), and test dust (Arizona Test Dust, ISO12103-1, Powder Technology Inc.) was sprayed periodically through the top opening of the chamber. The readout PCB was connected to a computer via a USB port for real-time sensor monitoring.

Figure 25(a) shows the time-response of a sensor device during two tests: one using road-dust and the other with the same airflow but without particles. At the beginning of each test, the stability of the sensor was monitored via measurement during 5 minutes without airflow and 15 min of airflow without particles. After 60 minutes of tests, an additional 10 min of measurement without air flow was performed. While the sensor reading was stable during dry test (no particles generated), a clear differential response was observed when particles are generated showing a counting shift of 3.24. The sub-integers of counts are the results of averaging as described in the readout circuit section as well as 2 minutes of window averaging from the recorded data. The sensor capacitance was measured before/after test for comparison and Figure 25(b) shows an

increase in sensor capacitance after testing, in agreement with positive shifts in counting from the readout circuit. The readout calibration using fixed capacitors estimated a resolution of ~15 fF/count, however, the calculated resolution from the test results using road dust appeared to be ~42 fF/count. One possibility is that the actual capacitance shifts due to particles could be masked under continuous air flow which causes dried condition, resulting the reduced capacitance shifts during tests.

(a) (b)

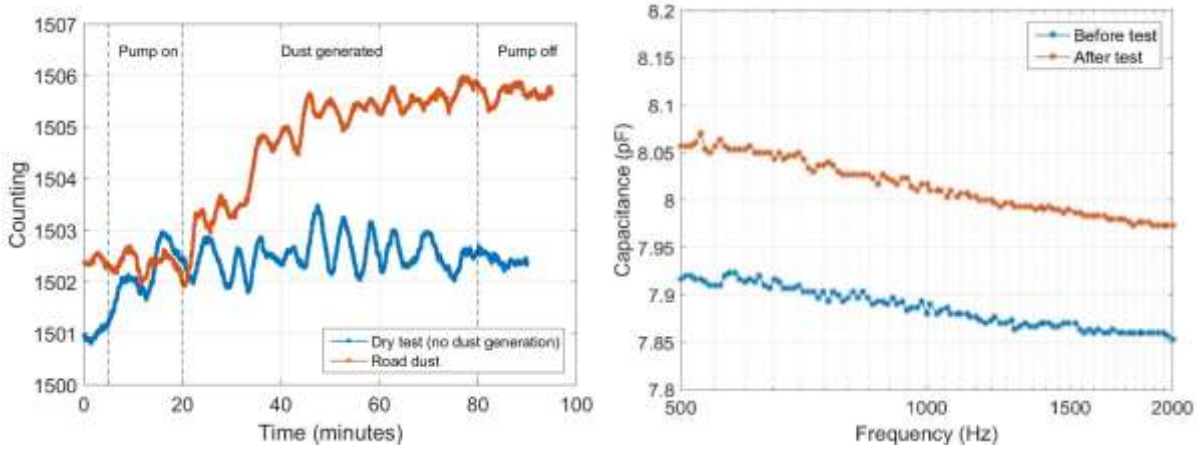

Figure 25. (a) Time-response of an integrated sampler, comparing i) test with road dust and ii) a "dry" test, without particle generation. A clear differential response was observed for the case in which particles were generated in the chamber volume. (b) Capacitance shift before/after testing, as measured by a laboratory capacitance meter. The positive shift in capacitance is consistent with increased counting.

5.3.3 Correlation of sensor response to total particles estimated from post-test imaging

The tested sensor was inspected with a scanning-electron microscope (SEM) for post-analysis. Five representative SEM images with a fixed magnification are inspected, and the average number of particles are calibrated with respect to the entire size of sensor. Figure 26(a) shows one of the SEM images of a capacitance sensor exposed to a comparable flux of particles. The collected particles are categorized by size based on SEM images: i) sub-micron particles with diameter below 1 μm and ii) microparticles larger 1 μm. And the microparticles are again partitioned by 1 μm. The effective diameter (D_{eff}) is individually defined for each group using the mode of diameter. Table 7 shows the post-analysis results using SEM images. About 77 % of

particles are smaller than 1 um while 23 % are larger than 1μm. Whereas most particles had sub-micrometer diameters, a few larger particles were observed, and they are counted as a single particle due to a limited resolution. Particles are assumed as spheres with D_{eff} of each group and the total volume of particles on sensor is calculated, which is 1.15×10^{4} μm^3. Since the test dust mostly consists of silica, the density of silica (2.65 g/cm^3) is used for the calculation of the effective mass. The calculated total particle mass on sensor becomes 3.04×10^{-8} g. The calculation indicates that the positive capacitive sensor response corresponds to the volume/mass of particles collected on sensor. The result also shows that a large portion of volume and mass fraction comes from the microparticle groups, nevertheless most of particles are sub-micron.

To understand the sensor response with volume, the total volume is converted into a layer of particles with effective thickness. Assuming it is uniformly deposited over the sensing area, the effective thickness becomes 7.77 nm. It is then compared with a simulation result. A COMSOL simulation is performed with two electrodes as a unit and the spacing between the electrodes is 2 μm. The result is then normalized with respect to the entire sensor area. It appears that the capacitance shift is linear with respect to the deposited silica up to 1 μm and it becomes saturated. Since the estimated thickness is 7.77 nm, sensor response is in the regime where the dielectric change is linearly proportional to the volume of each particle. This result indicates that the effect of larger particles is still dominant as shown in Table 7. It should be noted that a magnified SEM image shows that those larger particles were the agglomerates of sub-micron particles rather than single particles as shown in Figure 26(b). Nucleation of particles after landing on sensor could result in such agglomerations, but a comparative study with aerosol size distribution of test dust is necessary to understand the agglomerations.

(a) (b)

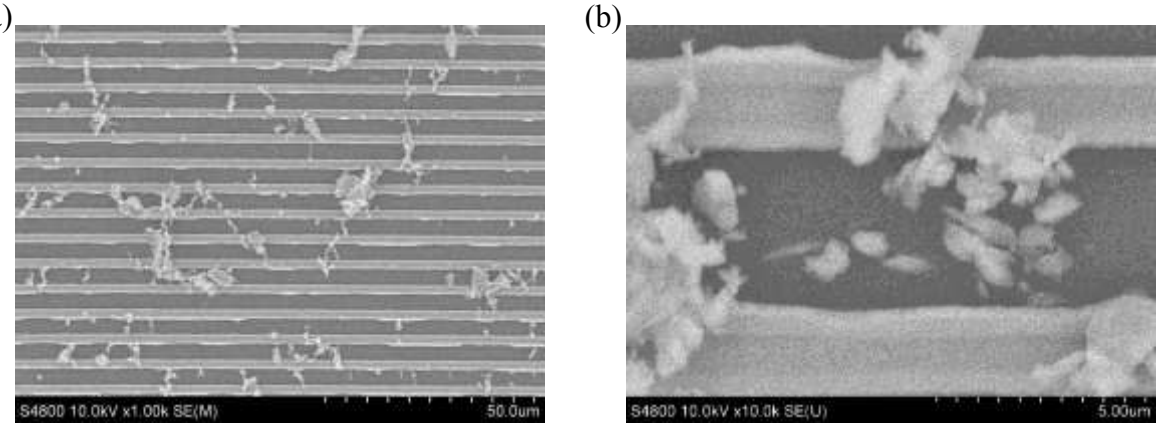

Figure 26. SEM image of (a) particles deposited on a capacitance sensor after exposure to comparable particle flux. For reference, the lines and spaces in the image are approximately 3 microns. (b) A magnified SEM image showing agglomerates of sub-micron particles.

Table 7. Post-analysis of particle information using SEM

Group	Size range	D_{eff} (μm)	# of Particles	V_{eff} (μm^3)	m_{eff} (g)	Fraction (%)
A	≤ 1 μm	0.5	10,005	6.50×10^{2}	1.72×10^{-9}	5.7
B	$1 < D \leq 2$ μm	1.5	2,728	4.83×10^{3}	1.28×10^{-8}	42.1
C	$2 < D \leq 3$ μm	3	140	1.98×10^{3}	5.25×10^{-9}	17.3
D	$3 < D \leq 4$ μm	4	120	4.02×10^{3}	1.06×10^{-8}	34.9
Total			12,993	1.15×10^{4}	3.04×10^{-8}	100

5.3.4 Effective particle concentration

The collected mass on the sensor is compared with a standard gravimetric method. The 25 mm polycarbonate filters were desiccated for a minimum of 48 hours prior to pre and post weighing. Filters were weighed on a microbalance (Mettler Toledo MX5) until two consecutive measurements were within 0.005 mg. The two measurements were averaged to determine the final mass of deposited particles, which is 4×10^{-5} g. Comparing with the collected mass on sensor (3.04×10^{-8} g), the average mass on filter (sampler) is more than three orders of magnitude higher than that on sensor. Considering that the sensing area (1 mm × 1.5 mm) takes about 0.3 % of the filter area (13 % including interface PCB), the larger mass ratio than the area ratio indicates non-uniform distribution of particles inside the sampler. Figure 27(a) shows a clear image wherein a

high portion of particles was collected at the center area, and the concentration decreased with distance from the center. This is mainly due to the location of inlet where the center area has direct airflow. It also shows that the sensor and interface board do not interfere with particle collection, except the relatively clean area at the lower side of the filter indicating the sensor and interface board location.

A simulation study using a computational fluid dynamic program showed that particle distribution inside the sampling cassette depends on the particle size; particles smaller than 3 μm are relatively uniformly distributed over the filter area, while particles larger than 3 μm are concentrated in the center area. Figure 27(b). shows the simulation results with three representative particles; while particles of 11.5 nm-diameter (red) is uniformly distributed, both 5.8 um-diameter (blue) and 9.0-um diameter (green) are collected preferably in the center. The sensor is located about 2.5 mm away from the center. According to the simulation result, the sensor rejects most of particles larger than 9 μm while some of 5 μm-diameter particles could land on the sensor. This result agrees with our post-analysis on Table 7 where a small portion of microparticles are observed on the sensor. Therefore, placing the sensor away from the center increases the probability of sensing sub-micron particles rather than microparticles.

With all given information, we can convert our results into the standard airborne particle concentration expression; g/m^3. Using the chain rule,

$$\frac{mass\ (g)}{Volume\ (m^3)} = \frac{Count}{min} \times \left(\frac{mass\ (g)}{Count} \times \frac{1}{Flow\ rate\ \left(\frac{L}{min}\right)} \times mass\ calibration\ factor\right) \quad (4)$$

where the mass calibration factor is the ratio of particle mass on filter to particle mass on sensor, which are obtained by gravimetric method and post-analysis respectively. While the terms in the parenthesis are known, only the rate of change in count will vary with respect to the environment. For instance, the rate of change in Figure 25(a) is about 1 count/10 minutes for the first 30 minutes. Therefore,

$$4.11\ \frac{mg}{m^3} = \frac{1\ Count}{10\ min} \times \left(\frac{3.04\times10^{-8}\ (g)}{3.24\ Count} \times \frac{1}{0.3\ (L/min)} \times \frac{10^3 L}{m^3} \times 1{,}316\right). \quad (5)$$

The calculation result shows that under the given test conditions using road dust, the particle concentration is □4 mg/m^3 for 10 minutes of sampling. On the other hand, the rate decreases after 30 minutes of particle sampling with the ratio of 0.33 count/10 minutes. That is,

$$1.36\,\frac{mg}{m^3} = \frac{0.33\ Count}{10\ min} \times \left(\frac{3.04\times10^{-8}\ (g)}{3.24\ Count} \times \frac{1}{0.3\ (L/min)} \times \frac{10^3 L}{m^3} \times 1{,}316\right). \quad (6)$$

By monitoring the rate of change in counts, the airborne particle concentration can be calculated at intervals on the order of 10-20 minutes.

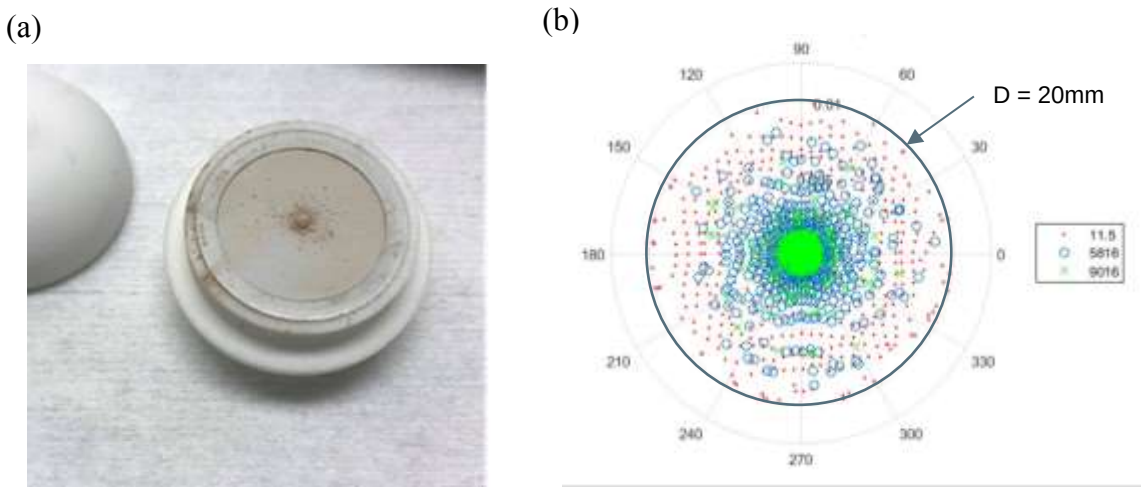

Figure 27. (a) Photograph of the filter after testing. A high proportion of particles was collected at the center area, and the concentration decreased with increasing radius. (b) Radial particle distribution by size. Small dots (red) represent particles with 11.5 nm diameter, circles (blue) represent particles with 5.8 μm, and crosses (green) represent particles with 9.0 μm.

5.3.5 Microheater characterization

The microheater integrated on the sensor strip allows heating of the strip to a controlled elevated temperature. This is intended to mitigate effects of high and variable ambient humidity as well as temperature-based drift in capacitance under constant air flow. Figure 28(a) shows the capacitance reading without and with the heater activated in ambient condition (Temperature: 19 °C, Relative humidity: 38 %). Under constant air flow (no particles generated), the use of heater resulted in a more stable sensor capacitance where the variation reduced from ±40 fF to ±20 fF, thus enabling stable detection of a smaller quantity of deposited particles. The absolute capacitance decreased after heater is activated and one possibility is that thermal expansion of substrate effectively widened electrodes spacing causing lower capacitance. Figure 28(b) shows the stability of the capacitance signal as a function of relative humidity (RH) at room temperature. To control the RH, air was bubbled through a beaker of water inside the test

chamber and the RH was measured using hygrometer. No sampling cassette is used to eliminate the effect of air flow. While capacitance increased with higher RH, the use of the on-board resistance heater significantly decreased the variation in capacitance over the range of 43–64 % RH (dew point of 5.6 °C to 12 °C). Like Figure 28(a), the absolute capacitance decreased again as heater is activated but remained stable during operation. This result indicates that the capacitance sensor can operate over a range of ambient dew points.

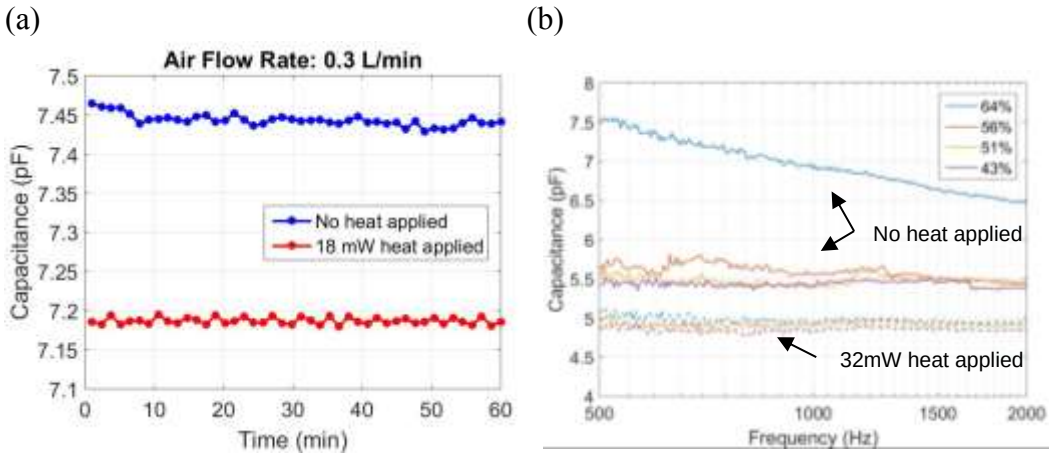

Figure 28. (a) Capacitance sensor test without and with heating via a resistance heater. Tests were performed at constant flow rate and capacitance fluctuation is reduced with the activation of heater. (b) Capacitance response at different relative humidity levels without a heater and with an activated heater. The stability of capacitance improved specifically at higher relative humidity (or dew point) when heater is activated.

5.4 Conclusion

A sub-micron and nanoscale particulate matters detection system is made. The interdigitated capacitive sensor strip is designed for the integration with standard personal sampling cassettes and the readout board enables continuous monitoring of capacitance shifts due to particles. Sensor response with respect to test dust showed differential behavior from tests without dust and good agreement with positive capacitance shift. Most of the collected particles are sub-micron particles with diameter below 1 µm, and microparticles are agglomerates of smaller particles. A simulation study showed that capacitance shift is linearly proportional to the particle volume. Due to radial dependence of particle deposition as well as sensor location, the

particle mass concentration on sensor appeared to be three orders of magnitudes less than the concentration on sampler measured by standard gravimetric method. The incorporated heater improved stable capacitance sensor reading by mitigating variations from surroundings such as air flow and relative humidity. The current generation of device has an envelope of 12 cm × 3 cm × 4 cm and its weight is 37g including sensor chip, readout circuit, and personal sampler. This real-time, miniaturized, and lightweight particle monitoring system could be utilized for workers in diverse workplaces who are exposed to hazardous nanoparticles.

6. COPPER NANOWIRE/GRAPHENE HYBRID NETWORK FOR TRANSPARENT CONDUCTOR

6.1 Introduction

Transparent conductors (TCs) are thin layers of material which are optically transparent and electrically conductive. TCs are used in displays, photovoltaic systems, and antistatic shielding. Given the development of the display market, the demand for TC is steadily increasing. It is expected for the market size to reach $5 billion within a few years [115]. The most popular materials are transparent conducting oxides (TCO) where it has both large bandgaps enough to avoid the absorption of visible wavelength, and reasonable electrical conductivity with high levels of doping. Tin-doped indium oxide or indium tin oxide (ITO) is the most popular among TCs and features over 80 % transmittance with 10-100 Ω/□ of sheet resistance (R_{sh}). Though ITO has been widely used for transparent conducting electrodes, fabrication is expensive because indium is a rare material. In addition, the poor mechanical properties of ITO make it difficult to use in flexible electronics [116].

Other materials, including nanostructured approaches, could provide improved flexibility and more earth-abundant materials. Carbon nanotube (CNT) and graphene were first introduced in the 1990s and 2004, respectively. Both have received attention as potential TCs because of their high transmittance and conductivity [117]. However, the fabrication costs of both CNT and graphene are currently more expensive than that of ITO. Metal mesh or conductive polymers have a cost advantage, but metal mesh causes interference fringes between metal grids and display panels (i.e. the Moiré effect). Conductive polymers have so far shown poor conductivity compared to other metallic materials. Metal nanowire (NW) networks can provide low R_{sh} at moderate transparency (< 90 %) as well as flexibility. However, NW conductance in the high transparency is limited by percolation.

Co-percolation networks consist of NW networks covered with a single-layer of graphene. While the NW networks has the highest resistance at its junctions, the high resistance of single-layer graphene is a result of its grain boundaries. Such properties make it difficult to substitute NW networks for ITO, despite their transparency and flexibility. In the co-percolation networks, however, R_{sh} is greatly reduced as it avoids high resistance paths such as NW junctions and grain

boundaries, as shown in Figure 29. Chen et al. made a silver NWs and graphene hybrid network and showed improved R_{sh} with respect to ITO at same transparencies (88 %, λ= 550 nm) [22].

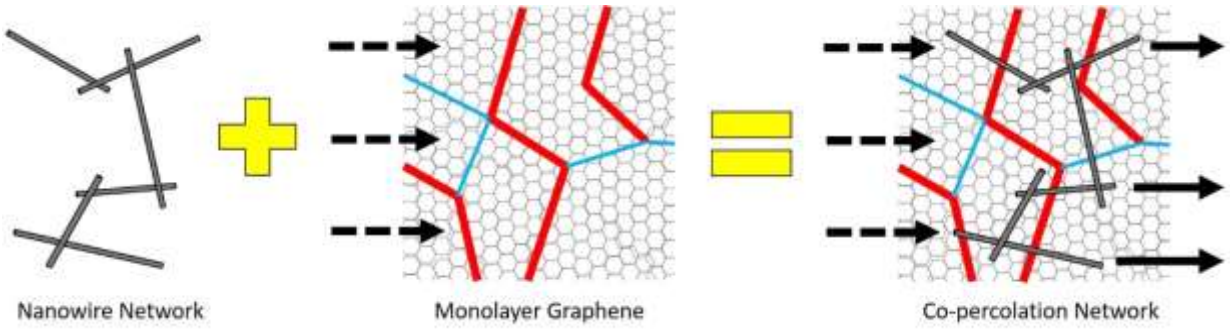

Figure 29. Schematic of nanowire/graphene hybrid network. A co-percolation network is formed in the hybrid network and it reduces sheet resistance significantly.

Most NW and hybrid networks studies have employed silver nanowires (AgNWs). Recently, NWs of other materials, including copper (Cu), are of interest due to their low cost as well as varying properties. First, Cu is an inexpensive material whose conductivity (ρ_{Cu}: 16.8 Ω·nm) is similar to silver (ρ_{Ag}: 15.9 Ω·nm). Thus, a similar performance is achieved at a much lower cost. Secondly, Cu has different optical properties than silver. As shown in Figure 30, Cu has a plasmonic effect in the visible wavelength range (550-600 nm), while silver has the same effect in the ultraviolet wavelength range (300-350 nm). Therefore, Cu may be useful for applications like optical limiting and photoconductivity as the wavelength range of interest overlaps. In addition, a different contact work function control will be available with Cu.

In this study, copper nanowire (CuNW)/graphene hybrid networks were fabricated and their optical/electrical properties were characterized. A detail of CuNW cleaning process to remove surfactants and the Fourier-transform infrared spectroscopy (FTIR) characteristics of CuNW are presented. The processed CuNW were drop-casted on glass substrate and graphene was transferred on top of CuNW. The transmittance was measured before/after the graphene transfer and the results were compared. The circular electrical contacts were patterned via photolithography for transfer length measurement (TLM). The lowest R_{sh} is 92 ± 8 Ω/□ at 81 % transmittance (λ=550nm).

This work was done in collaboration with Yuki Mori in the Institute of Scientific and Industrial Research, Osaka University, Japan, under the guidance of Professor Kazuhiko

Matsumoto. Mori contributed to the fabrication of CuNW/graphene hybrid networks, which were done in Birck Nanotechnology Center, Purdue University.

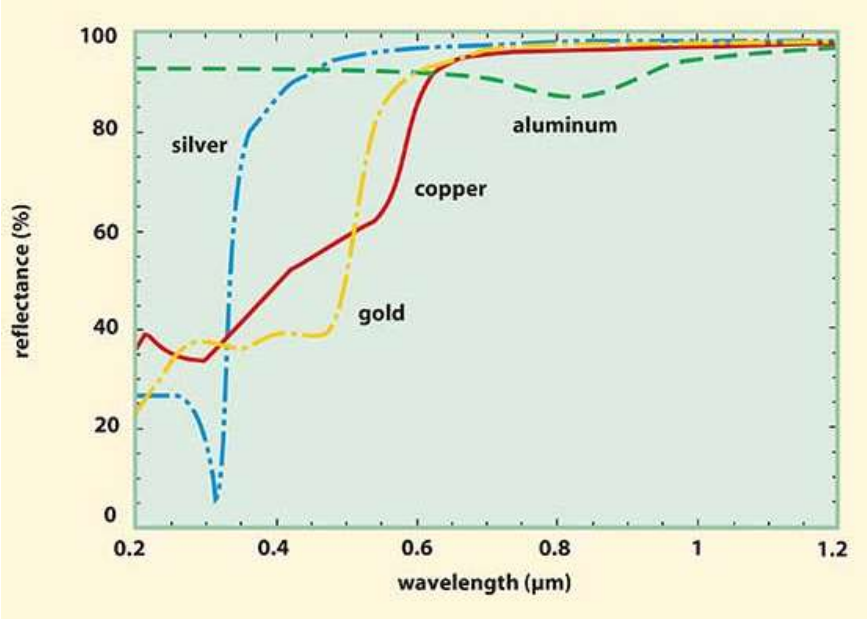

Figure 30. Reflectance of bulk metals [118].

6.2 Device Fabrication

6.2.1 Copper nanowire preparation

Commercially available CuNWs (Novarials. Co. LTD.) and single-layer CVD graphene (ACS Materials) are used to make a CuNW/graphene hybrid network. The average diameter of CuNW is 100 nm and length is 50 - 200 μm. Figure 32(a) shows the un-treated CuNWs drop-casted on glass substrate and agglomerated CuNWs and Cu flakes are observed. To spread the NWs, the CuNWs are transferred into ethanol and 2 wt% polyvinylpyrrolidone (PVP, 9003-39-8, Sigma Aldrich) is added into the solution. The solution is stirred overnight for complete separation. It is then centrifuged at 4000 rpm for removing PVP and repeated three times for 10 minutes. Various types of solvents were investigated to remove the surfactant. Figure 31 shows the results of the FTIR transmittance on CuNW solution before and after treatment. Four major peaks were observed for the un-treated CuNW solution at 2953, 1676, 1421, and 1286 cm^{-1}, and it appears that these peaks match the PVP-iodine complex, which exhibited peaks at 2952, 1677, 1421, and 1421 cm^{-1}, as shown in the inset of Figure 31. After the three rounds of cleaning, the solvent is switched

back to IPA and drop-casted again on a KBr card for transmittance measurement. As shown in Figure 31(b), the four peaks found for the un-treated solution were greatly reduced after all type of cleaning. The noisy peaks at around 3800, 2400, and 1700 cm^{-1} were due to vibrational modes of water (H_2O) and carbon dioxide (CO_2) in the air.

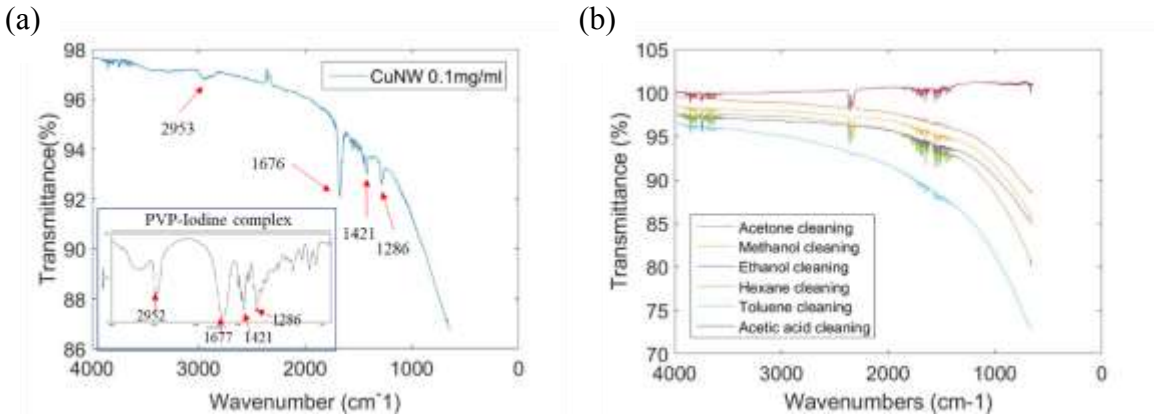

Figure 31. FT-IR Spectroscopy results on CuNWs. Transmittance of diluted (0.1mg/ml) CuNW solution. The inset is the FT-IR transmittance of PVP-iodine complex. (b) Transmittance results after solvent cleaning.

The solution is then filtered to remove the flakes of Cu using a 5 μm-diameter polyester track etch (PETE) membrane filter. This process is repeated several times until the flakes are minimized. After filtering, the remaining CuNWs on the filter are transferred to the prepared isopropanol (IPA) and drop-casted on glass substrates. Figure 32(b) shows the microscope image of CuNW after treatment and no flakes are observed. Various sample densities are made by controlling the number of drops, as shown in Figure 32(c). For better adhesion to the substrate, the samples are annealed in 300 °C for 1 hour using forming gas.

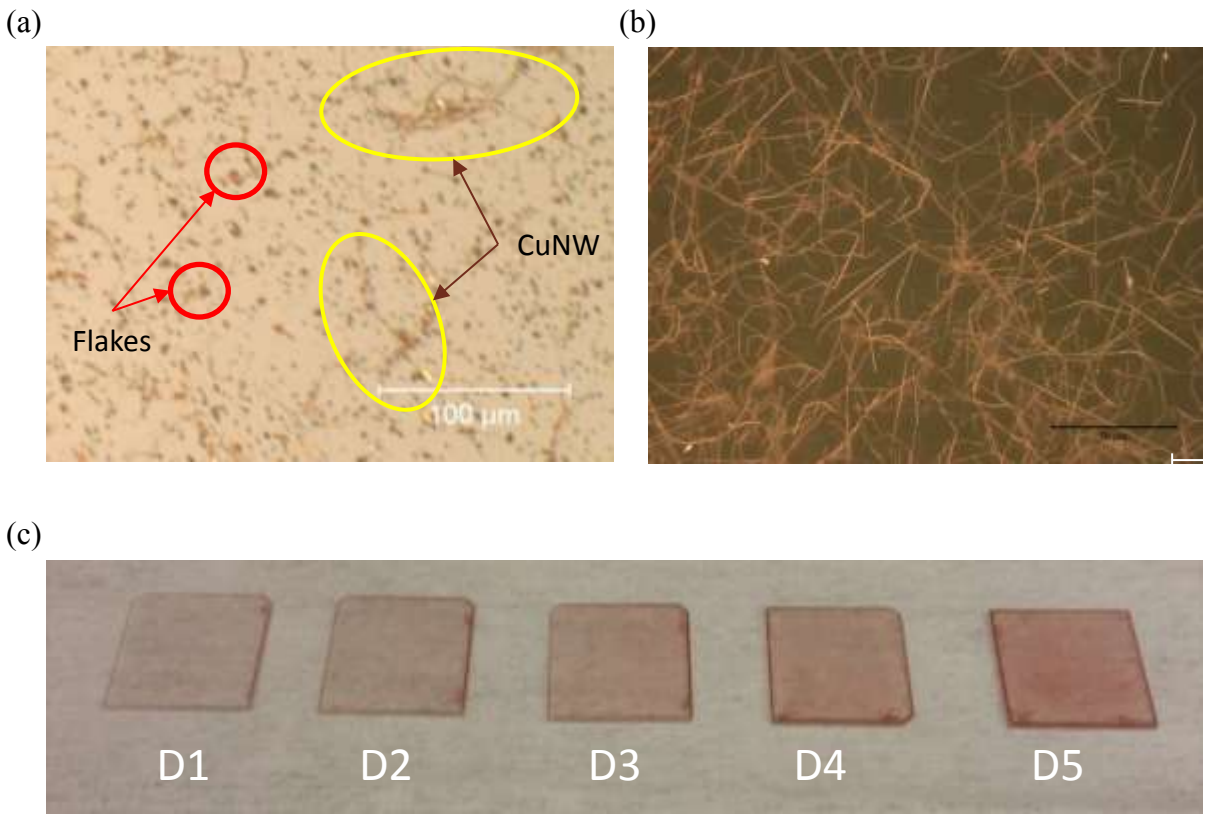

Figure 32. Commercial CuNW (a) before treatment and (b) after treatment. Several times of filtering process was conducted to remove copper flakes. (c) CuNW on glass substrate. D1 has lowest NW density and D5 has highest NW density.

6.2.2 Graphene transfer & contact fabrication

The graphene transfer process is illustrated in Figure 33. It began with spin-coating of polymethyl methacrylate (PMMA, MicroCHEM 950 A4) on one side of the graphene. After the spin-coating, the other side of the graphene is removed using dry-etch. 50 sccm of O_2 plasma (Plasmatech RIE) is applied for 30 seconds and the pressure is 50 mtorr. The Cu foil is then etched using a diluted iron nitrate solution (5 g of Iron(III) nitrate nonahydrate, Sigma Aldrich, in 100 ml DI water). The PMMA/Graphene is cleaned using pure DI water several times and transferred on top of the CuNW sample. The PMMA is removed using acetone for 1 hour at 70 °C, and the sample was annealed again at 350 °C for 1 hour under the forming gas.

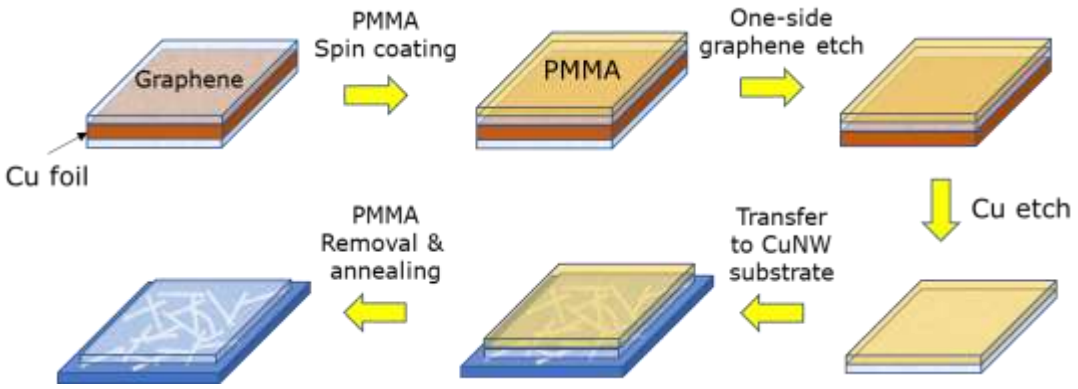

Figure 33. Schematic of graphene transfer process. i) Spin coating of PMMA, ii) oxygen plasma etch, iii) Cu etch, iv) transfer to CuNW substrate, v) PMMA removal & annealing

Photolithography is used to make metal contacts on the CuNW/graphene sample as shown in Figure 34. Hexamethyldisilazane (HMDS) adhesion promotor and AZ 1518 positive photoresist are applied, and the sample was exposed using a mask aligner (SUSS MJB3). The mixture of AZ developer and deionized water (AZ:DI Water = 1:1) is used to develop patterns. 5 nm of titanium (Ti) and 100 nm of gold (Au) is evaporated using an e-beam evaporator (CHA Industries). The deposition rate for Ti and Au was 1.0 Å/s, and the pressure was 2.0×10^{-6} torr. The metal contacts were finally made with the lift-off process using acetone. Figure 35 shows the finalized circular patterns on the samples.

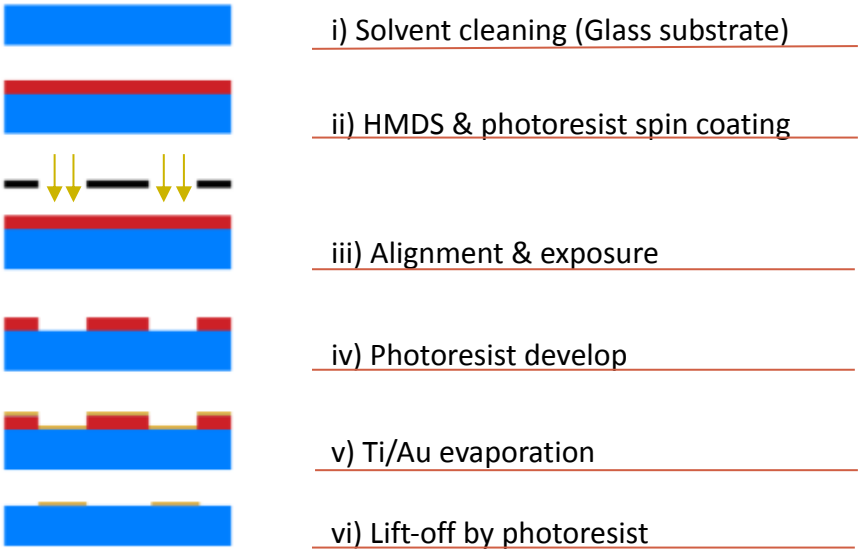

Figure 34. Cross-section of contact fabrication.

(a) (b)

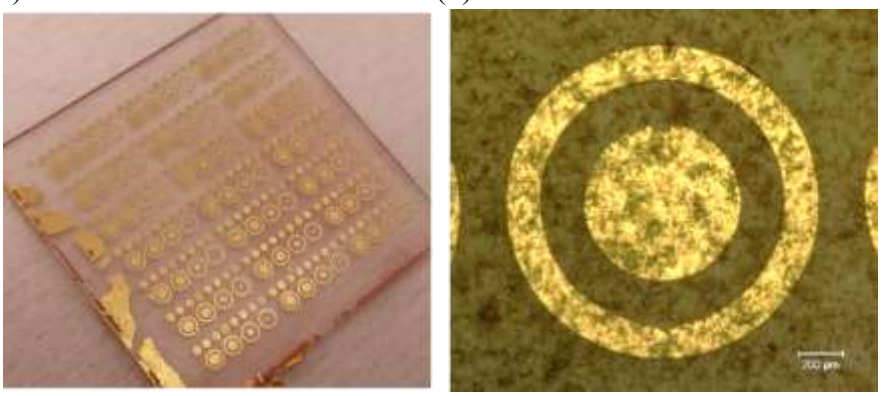

Figure 35. (a) Optical image of hybrid sample after contact fabrication and (b) Microscope image of hybrid network with circular electrodes.

6.3 Experimental Methods and Results

6.3.1 Optical properties of CuNW and hybrid network

The optical transmittance was measured before and after the graphene transfer. A spectrophotometer (PerkinElmer Lambda 950 UV-VIS-NIR) was used to measure the diffusive transmittance. For each sample, the measurements were conducted three times at different spots and averaged. The averaged data was normalized with respect to the transmittance of the glass substrate. The transmittance of the CuNW and hybrid network was measured from 300 nm to 1200 nm. Figure 36(a) shows the transmittance of CuNW before graphene transfer and the transmittance steadily decreased as the NW density increased. While the transmittance was flat in the UV and IR regions, there is a decreased transmittance below 600 nm, and it is more pronounced in the higher NW density samples. These effects are attributed to plasmonic effects of Cu, while Ag showed a peak in the shorter wavelength range (350 nm) [119], [120].

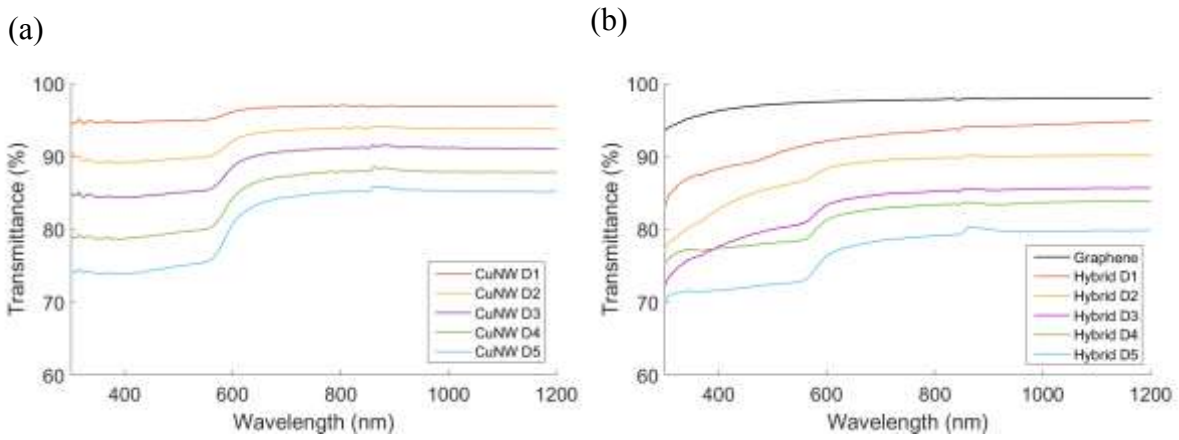

Figure 36. Optical transmittance of (a) CuNW and (b) CuNW/Graphene hybrid network.

The transmittances of the hybrid network and single-layer graphene are shown in Figure 36(b). When each sample was compared, the overall transmittance decreased post-graphene transfer. However, the magnitude of change varied by sample. For instance, while the transmittance of graphene was mostly constant except the region below 400 nm, a decreased transmittance was observed in lower NW density samples (D1-D3). This data was replotted with respect to NW density at specific wavelengths, as shown in Figure 37. The transmittance decreased after the graphene transfer, and the rate was consistent for longer wavelength ranges such as 700 nm and 1100 nm. Considering that the transmittance of graphene is about 97 % in this range, the rate of decrease generally matches with expected transmittance of hybrid networks. On the other hand, despite the non-uniform transmittance of graphene, the ratio was not consistent for D1-D3 in the 350 nm range. The transmittance rather increased as NW density increased from D3 to D4.

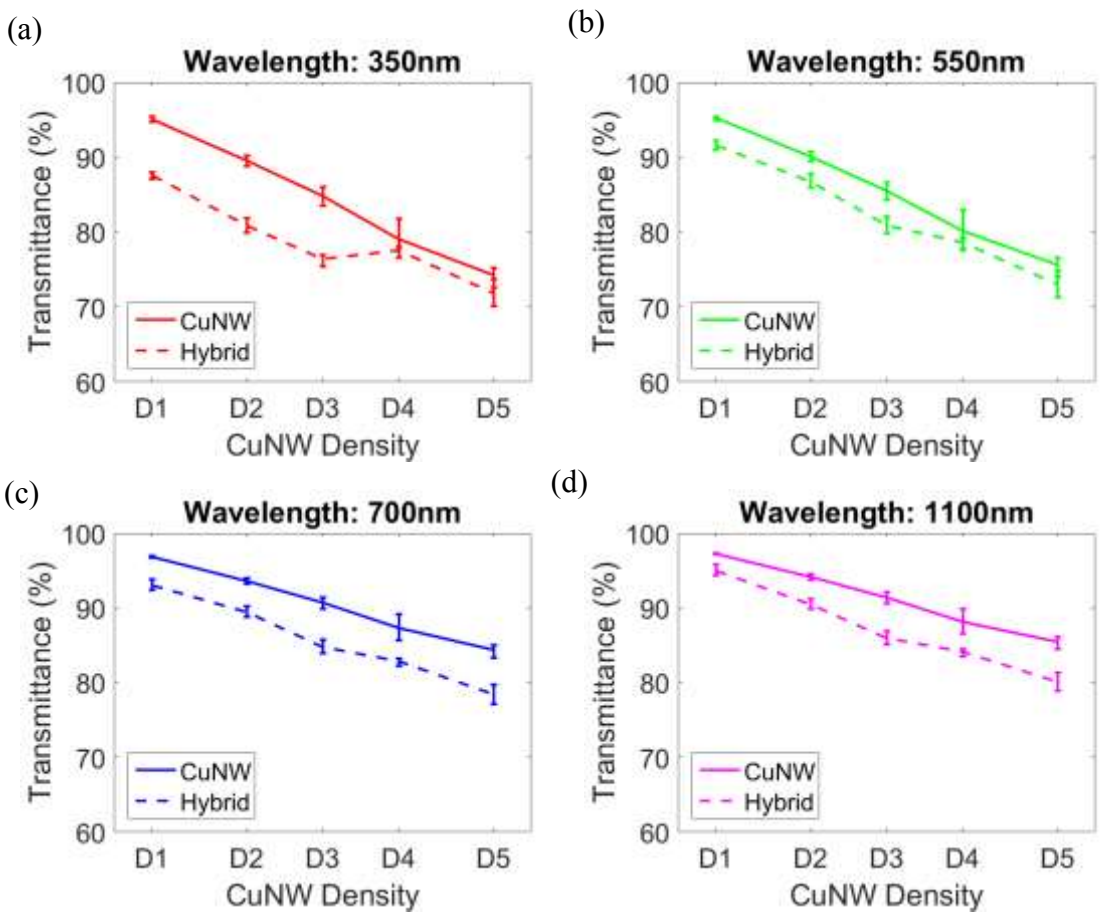

Figure 37. Optical transmittance with respect to NW density. (a) 350nm, (b) 550nm, (c) 700nm, and (d) 1100 nm.

6.3.2 Electrical properties

The electrical measurement was conducted using circular transmission line patterns of four different channel lengths (150 µm, 250 µm, 350 µm, and 450 µm). Each average data point was collected after 3-5 measurements of different spots. Figure 38 shows that the measured resistance of CuNW D1 (lowest NW density) is in the 10^9 Ω range, but the resistance was reduced to a few hundred ohms post-graphene transfer. When compared to single-layer graphene, the hybrid resistance was lowered by a factor of two. Considering the resistance of CuNW D1 is similar to that of dielectric materials, this improved conductance indicates the effect of the co-percolation network between the CuNW and single-layer graphene.

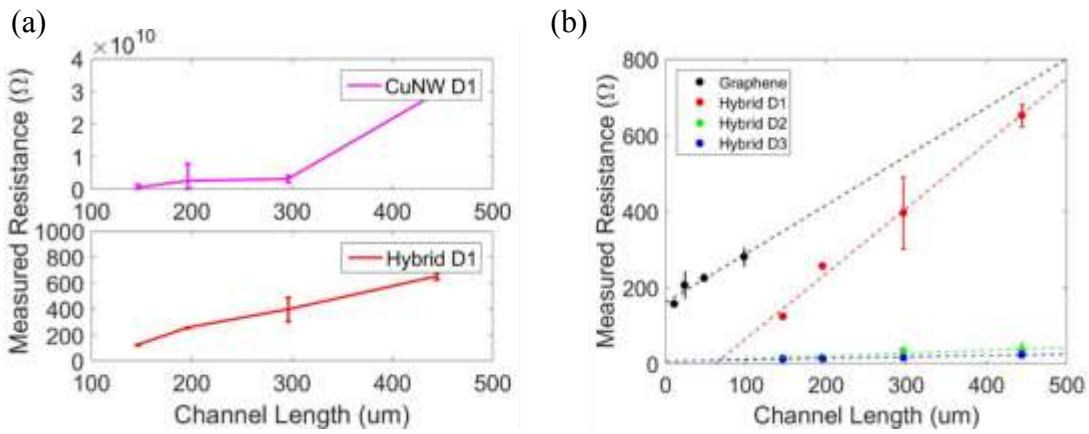

Figure 38. Electrical measurement of CuNW D1 and Hybrid network. (a) Measured resistance of CuNW and hybrid network at same NW density. (b) Comparison of resistance of graphene and hybrid network with various densities.

To extract the R_{sh}, the resistance in the circular transmission line pattern is,

$$R = \frac{R_{sh}}{2\pi} \times \left[\ln\left(\frac{r_1+s}{r_1}\right) + L_T\left(\frac{1}{r_1} + \frac{1}{r_1+s}\right)\right] \quad (7)$$

where r_1 is the radius of the inner electrode, r_2 is the radius of outer electrode, s is the channel length, L_t is the transfer length, and R_{sh} is the sheet resistance. If $r_2 \gg$ s, then the equation will reduce to

$$R \approx \frac{R_{sh}}{2\pi r_2}(s + 2L_T). \quad (8)$$

Since such an assumption is not valid, it is rearranged with respect to s. Thus,

$$\frac{R}{C} = R_{corrected} = \frac{R_{sh}}{2\pi\, r_2}(s + 2L_T) \quad (9)$$

where the correction factor C is,

$$C = \left[\ln\left(\frac{R_1+s}{R_1}\right) + L_T\left(\frac{1}{R_1} + \frac{1}{R_1+s}\right)\right] \times \frac{R_1}{(s+2L_T)}. \quad (10)$$

R_{sh} can be obtained by calculating the slope of the linear equation.

$$R_{sh} = \text{slope} \times 2\pi r_2. \quad (11)$$

The transfer length (L_T) must be known to calculate C. Thus, L_T is extracted by calculating the x-intercept of the linearly extrapolated lines in Figure 38(b). Figure 39 shows the corrected resistance with respect to the channel length and R_{sh} was extracted from the slope. For Hybrid D3, R_{sh} is

92±8 Ω/□ the transmittance is 81 % (λ=550 nm) and the error comes from the transfer length assumption.

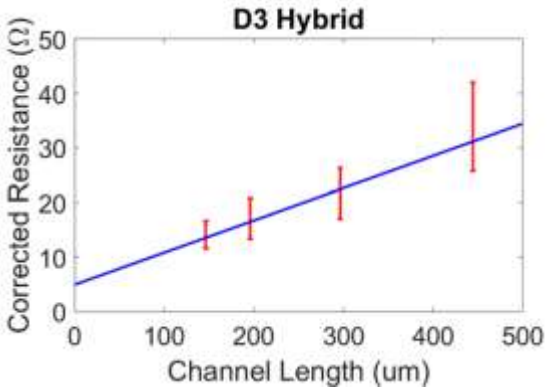

Figure 39. Corrected resistance of Hybrid D3 network. Linear extrapolation was used to extract sheet resistance (blue line).

6.3.3 Discussion

Figure 40 shows the figure of merit from previous studies and the CuNW/graphene hybrid networks (Hybrid D3). While the transmittance is 81 % at 550 nm (yellow star) but it increases to 84 % in 610 nm (orange star) because of the strong plasmonic resonance of Cu in the 550 nm. Currently, the CuNW/graphene's figure of merit is close to that of CNT but still there is a gap between ITO and this study. Two things must be addressed to improve the conductivity of CuNW and its hybrid networks. First, Cu is one of the materials which is easily oxidized, and the oxidized CuNW may increase R_{sh} as the oxidized surface prevents NW-NW or NW-graphene junctions. Recent studies that use graphene as an oxidation barrier may be beneficial not only for the co-percolation network but also for the protective layer.

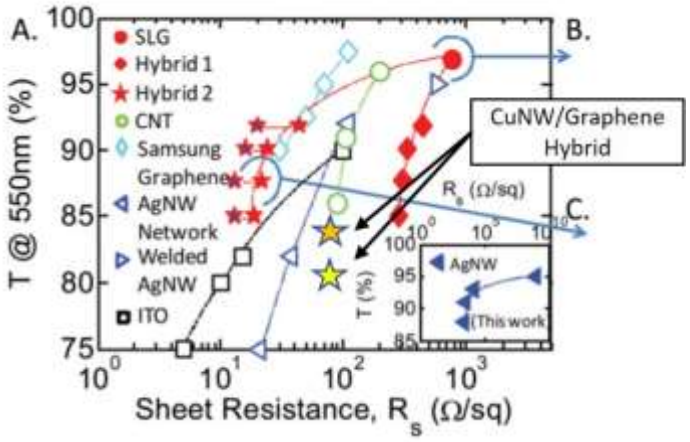

Figure 40. Optical transmittance vs. sheet resistance data for previous works and this work (CuNW/Graphene hybrid). The transmittance is 81 % at 550 nm (yellow star) but it increases to 84 % in 610 nm (orange star) because of the strong plasmonic resonance of Cu in the 550 nm. The previous works are reprinted from Chen's work [22].

Secondly, the use of surfactant may increase the R_{sh} due to the presence of surfactant on NWs. Though Figure 31 showed no signs of PVP after the cleaning process, the PVP could still exist on the NW surface. PVP is a popular surfactant that helps NWs to separate in solution but is difficult to remove completely. Since PVP separates NWs by wrapping around the NW surface, good electrical contact may not be achieved if PVP is not completely removed. Figure 41 shows the measured resistance of CuNW and its hybrid samples without the cleaning process. CuNW D1 has the lowest NW density and CuNW D5 has the highest NW density. CuNW D1 and Hybrid D1 are assumed to have the same NW density. As shown in Figure 41(a), the resistance increased as NW density increased. The overall resistance decreased on the hybrid device as expected, however the resistance increased again with increasing NW density. This result is counterintuitive because the higher NW density should reduce resistance as more NW networks are formed. Considering that the other conditions were maintained, this result may be due to residual surfactant on the NW networks. Therefore, further studies on removing the surfactants are necessary.

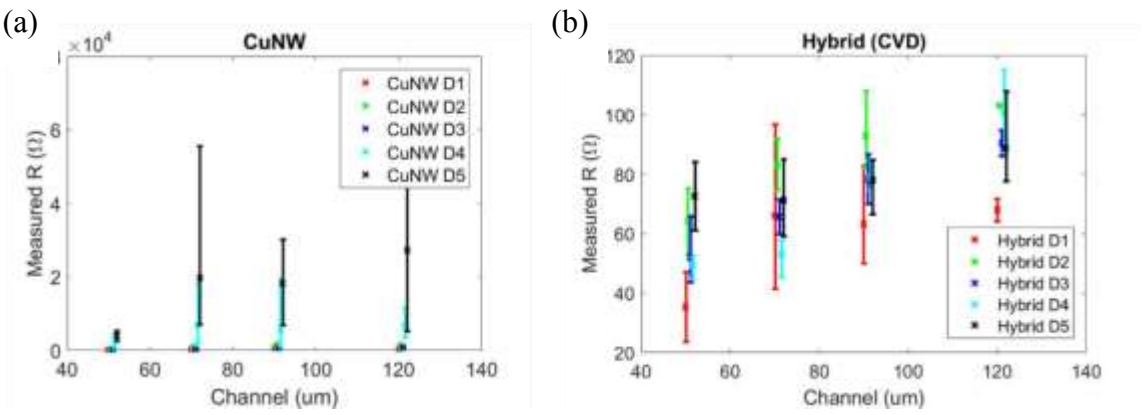

Figure 41. Measured resistance (a) CuNW and (b) hybrid network without cleaning process. The resistance increases with higher NW density.

6.4 Conclusion

A transparent conductor using CuNW and graphene hybrid network is made. This co-percolation network significantly reduces the sheet resistance while minimizing the loss of optical transmittance. It provides additional conducting path each other such that bottlenecks like NW-NW junctions and grain boundaries on graphene could be avoided. The optical transmittance of the hybrid network showed sharp decrease in the visible range due to the plasmonic effect of Cu and a different ratio of decreased transmittance is observed between shorter wavelength and longer wavelength range. The hybrid network showed improved conductivity compared to NWs and graphene samples respectively and the lowest R_{sh} is 92±8 Ω/□ when the transmittance are 81 % (λ=550 nm) and 84 % (λ=610 nm), respectively. Prevention of Cu oxidation and complete removal of surfactant could improve the figure of merit of this hybrid networks.

7. VERTICALLY ALLIGNED NANOWIRE ARRAYS BY ELECTRODEPOSTION

7.1 Introduction

Metal and semiconductor nanostructures have generated significant interest in the scientific community and been scrutinized for their material, electrical, and optical properties. Metallic nanostructures show selective photo-absorption when embedded in matrices of transparent dielectrics [121]. The selective absorption of metallic nanoparticles at a particular frequency has been attributed to surface plasmon resonance (SPR) [122]. The structure, shape, size, and crystallinity of the nanostructures are crucial factors that ultimately determine their characteristics.

AgNWs and nanostructures are of particular importance due to their optical, electrical, and plasmonic properties. For instance, AgNW mesh forms a percolating network that may be prepared by coating a solution to flexible substrates. These structures are known to have high transmittance and low sheet resistance that rival the optical and conducting properties of well-established TC such as indium tin oxide (ITO) [123]. Also, Ag's branched or nanodendritic structures have great potential as plasmonic routers or chemical sensors [22], [124]–[126].

The fabrication and deposition of Ag nanoparticles (AgNPs) and nanostructures have been achieved via various methods, including, but not limited to thermal evaporation and electron beam lithography [121], [122]. Template assisted growth and fabrication of NWs are quite popular due to the variety of NWs realized with various materials such as metals and semiconductors. Compared to the vapor-liquid-solid (VLS) growth process, template assisted growth provides control of the NW structure. The templates allow the NW growth to be anisotropic with a fixed size, distribution, and geometry. Among the diverse types of templates available, the porous anodic aluminum (PAA) templates are hard templates whose pore size, pitch, regularity, and template thicknesses can be controlled during the anodization of aluminum. PAA templates have very low absorption in the visible (vis) and near infrared (NIR) spectrum of light; therefore, these templates form an excellent matrix for analyzing and studying the optical properties of vertically aligned NWs. The actual diameter and length of NWs depend on the pore size of the templates and the time of deposition in the PAA membrane nanochannels.

Some studies have examined the optical properties of straight AgNW arrays [122], [127]. While bulk Ag has a higher reflectance (lower absorbance) in the visible range of the spectrum,

straight AgNW arrays have lower reflectance (higher absorbance) within the same wavelength range. This result has been attributed to the plasmonic effect of the AgNW arrays. On the other hand, the optical properties of vertically branched AgNWs (Ag BNWs) has not been reported.
In this work, vertically aligned, randomly branched AgNWs were electrochemically deposited within the pores of a branched porous anodic aluminum (BPAA) template (Anodisc 13 from Whatman Co.). A nanostructure made of thin metallic nanowires (like the Ag BNWs) in a matrix of an isolating dielectric material (such as the alumina in a BPAA template) is expected to have an extremely low plasma frequency [127]. The samples were inspected via scanning electron microscopy (SEM) and x-ray diffraction (XRD). Finally, the optical reflectance, transmittance, and absorbance of the Ag BNWs were characterized. This work was done in collaboration with Asaduzzaman Mohammad in electrical engineering under the guidance of Dr. David. B. Janes, and Jieran Fang in electrical engineering under the guidance of Dr. Alex Kildeshev. Mohammad contributed equally to the electrodeposition of AgNW and optical measurement. Mohammad also contributed to the generation of SEM images of BPAA and Ag BNWs. Fang contributed to the numerical calculation of optical transmittance and reflectance of Ag BNWs using FDTD simulation.

This work was done in collaboration with Asaduzzaman Mohammad in Electrical and Computer Engineering under the guidance of Dr. David B. Janes, and with Jieran Fang in Electrical and Computer Engineering under the guidance of Dr. Alex Kildeshev. Mohammad contributed to electrodeposition of nanowire and optical measurement, which were done in Birck Nanotechnology Center. Fang contributed to the simulation of optical response of the BPAA and Ag BNWs.

7.2 Electrodeposition of Branched Silver Nanowires

The BPAA templates had a thickness of about 60 μm and were divided into two different layers. The top layer of the templates had branches of varying diameters, which covered a depth of approximately 1-1.5 μm. The remaining layer of the BPAA consisted of unconnected, parallel, cylindrical pores with an average diameter of 150 nm and a thickness of about 58-59 μm. The branches of the top layer were interconnected and hierarchically stacked so that the diameter increased as the top branches gradually merged to form intermediate branches of higher diameter.

For the simplicity of analysis and understanding, the entire template can be considered to have three distinct regions, as seen in Figure 42. The top branched layer cross-section has been observed to have distinct regions whose average diameters (spacing) have been determined to be approximately 20 (40) nm and 100 (220) nm [128]. The bottom layers that form the lower branches or trunks of the branched structures have average diameters of 150 nm with a pitch of 440 nm. It should also be noted that the branches within each specific region have slightly varied diameters and spacing.

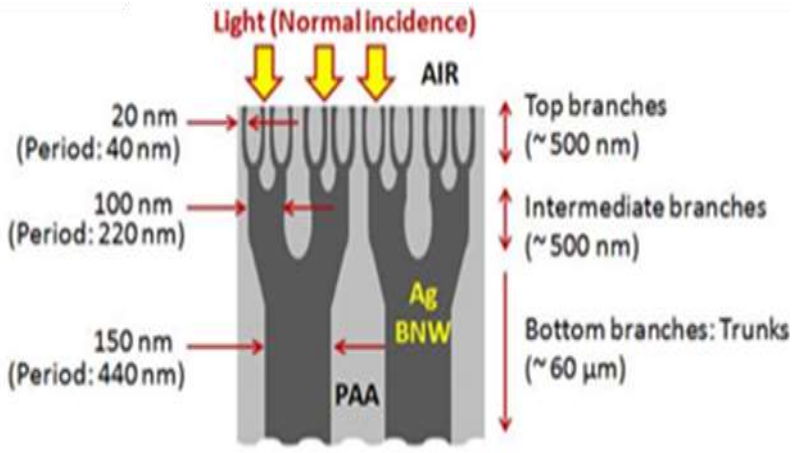

Figure 42. Schematic of the silver Branched Nanowires (Ag BNWs) in the Branched Anodic Alumina (BPAA) template [119].

The Ag BNWs were deposited within the pores of the BPAA template by potentiostatic electrodeposition of Ag. The deposition was performed in a three-electrode setup using a PAR (Princeton Applied Research) 273A potentiostat. Using an e-beam evaporator, the working electrode was formed by evaporating a 100 nm thick gold (Au) film on the "top" branched side of the BPAA template (containing the smallest diameter pores). Platinum (Pt) gauze was used as the counter electrode. An Ag/AgCl (3 M NaCl) reference electrode was employed and all deposition potentials mentioned in this work refer to this electrode. The Ag BNW deposition was carried out in an electrolyte solution of 0.05 M silver nitrate (AgNO3) and 0.57 M boric acid (B(OH)3) without agitation and at room temperature [129]. Prior to the deposition, the solution was purged with nitrogen to reduce the amount of dissolved oxygen. The exposed Au film, on the back of the working electrode, and the edges of PAA were carefully covered with a layer of an insulating material to facilitate the deposition of Ag within the confines of the BPAA template nanochannels. The DC electrodeposition was conducted at a constant deposition potential of 0.04 V. This method

avoided the use of extremely poisonous cyanide-based electrolytes typically used for depositing and electroplating Ag.

To study the optical properties of the Ag BNWs in the alumina matrix, it was crucial to remove the highly reflective and opaque Au layer. Due to the higher reactivity of Ag compared to Au, any wet chemical etching would preferentially attack the Ag BNWs at a rate faster than the Au film, thereby destroying the sample. Therefore, a dry plasma etching technique was employed in this work. The Au layer was etched using argon (Ar) plasma (Plasma Tech reactive ion etching (RIE) system) at 200 W with a flow rate of 50 sccm and a pressure of 100 mtorr for 9 minutes. Only the surface of the Au layer was exposed to the plasma. The sample was later inspected and analyzed to ensure the removal of Au. The regions containing Ag BNWs were visibly distinct from the regions devoid of them.

7.3 FE-SEM and Optical Characterization of Branched Silver Nanowire Arrays

The material composition of the BNWs was confirmed to be Ag by XRD measurements. Field emission scanning electron microscopy (FESEM) was used to observe the branching of the AgNWs. From the cross section of the BPAA matrix containing Ag BNWs, as seen in Figure 43 (a), the BNWs appear to be vertically aligned and hierarchically stacked with relatively clear distinctions between the regions of different Ag BNW diameters. The FESEM image also confirms that the Ag BNWs are independently branched, nominally parallel, and continuous.

To better understand the filling factor, an FESEM image of the branched surface of the sample with the Au layer etched off was obtained, as shown in Figure 43 (b). The average packing density of the branched side of the BPAA template was found to be ~33 %. The actual filling factor may be higher, as the possibility remains that some of the topmost branches of the Ag BNWs may have been removed during the Ar plasma etch process required for the removal of the Au layer. Many factors could negatively affect the filling factor of the pores, for example microscopic cracks in the BPAA template. Packing density may also be influenced by contaminants or debris inside the nanochannels or on the template surface that could effectively block the deposition path. The non-uniformity of the electrical resistance channels in each pore may also contribute to the varying BNW growth rates in different template regions.

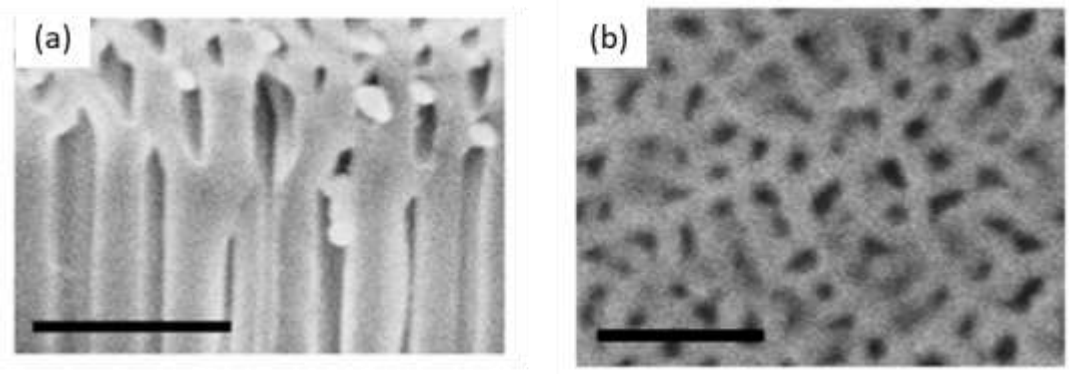

Figure 43. (a) cross-sectional FESEM image of vertically aligned randomly branched AgNW arrays (scale bar- 1µm); (b) Top surface of the BPAA template containing the Ag BNWs, after Au removal. (Scale bar- 200 nm) [119].

On the bottom side (trunk section), most of the nanochannels of the BPAA template appeared to be empty. A small percentage of the BNWs filled the entire cross-sectional length (~60 µm) of the template, and subsequently served as nucleation sites for Ag nanostructures on the other surface. The length of the Ag BNWs ranged from a few microns to about 60 µm.

The reflectance (R) and transmittance (T) of the Ag BNWs in the BPAA matrix were measured using a PerkinElmer UV-vis-NIR spectrometer (Model Lambda 950) with an integrating sphere arrangement. R and T were measured by illuminating a region of about 1 mm^2 of the bare branched BPAA surface containing the BNWs without the Au layer. The measurements were performed at normal incidence ($\theta = 0°$), and the wavelength ranged from 320 nm to 2000 nm (UV to NIR range). A standard white reflector from Perkin Elmer was used to calibrate each set of measurements. The absorbance of the Ag BNWs in the BPAA matrix was calculated from the R and T spectra of the sample. The absorbance of a blank BPAA template was also measured for comparison.

7.4 Results and Discussion

The measured R and T spectra of the Ag BNWs, with light incident of the top branched surface of the sample, are shown in Figure 44 (a). As observed in the figure, the R increases sharply, from 5 % to about 25 %, as the wavelength of the incident light increases from 320 nm to 800 nm. The minimum value of R is observed near 300 nm. The R of the Ag BNWs stabilizes at around 25 - 30 % as the wavelength of the incident light reaches the NIR range of the spectrum. The spike observed at 850 nm arise due to the switching of detectors in the spectrometer.

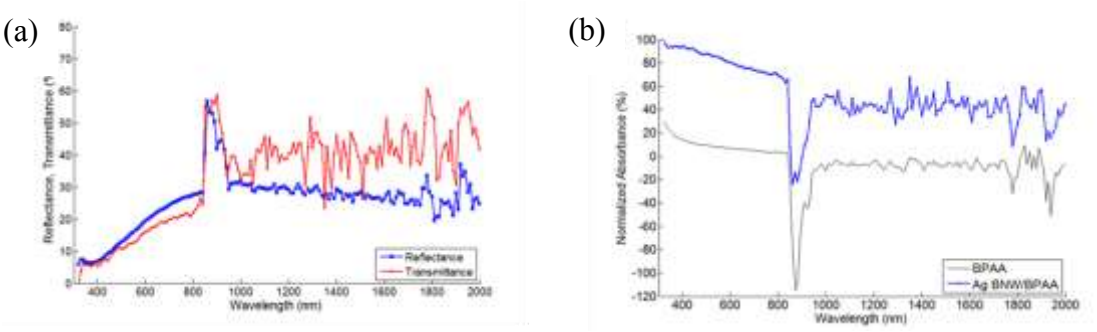

Figure 44. (a) Reflectance (R) and transmittance (T) of Ag BNWs with normal incidence on the branched side; (b) Normalized absorbance (A) of Ag BNWs and blank BPAA with respect to wavelength [119].

The measured R and T spectra exhibit the same general trend observed in the straight Ag nanowire structures when the incident light was perpendicular to the surface of the templates containing NWs [127]. In bulk Ag, a sharp reflectance minimum at around 320 nm is attributed to plasmonic effects in Ag. In a prior study, silver-alumina composite material also showed a clear dip in the reflectance spectra of the sample at around 320 nm [127]. While the decreases in R and T at the lowest measurement wavelengths in the current study may correspond to plasmonic effects, it is difficult to draw strong conclusions from this region due to the lack of data below 300 nm.

As demonstrated by Lee et al., the T of Ag thin film drops rapidly as the film thickness increases from 3 nm to 30 nm. The T is less than ~5 % for Ag films 30 nm thick in the wavelength range of 900-2000 nm [121]. Ag BNWs, which have more Ag along the light pathway than the thin film Ag (30 nm), display higher T. The T of the Ag BNWs increases steadily from about 4 % to 27 % as the incident wavelength rises from 320 nm to 800 nm. For the NIR range of the spectrum, the T stays near 40 %, which is higher than the T of Ag thin films of thickness as low as 9 nm.

The absorbance of the Ag BNWs in the BPAA template was calculated from the measured R and T spectra. To measure the absorption taking place in the BPAA template, R and T measurements for an empty BPAA template were conducted. While the actual absorption taking place in the empty template was 15-30 % in the UV region, the absorption almost reaches zero in the vis and NIR spectrum ranges, as can be seen in Figure 44 (b). The negative absorption of BPAA after the switching detectors in the spectrometer may be attributed to the uncertainty of measurement.

To better understand the fraction of light absorbed in the sample versus the light reflected from the sample, a normalized absorbance (A) was defined by:

$$A = \frac{1-R-T}{1-R}.$$

As observed in Figure 44 (b), A was very high (100-70 %) in the UV-visible range. While a plasmonic peak is observed at 350-400 nm for Ag nanowire arrays, the peak is hidden in our branched structure because of plasmonic peak shift depending on the nanowire diameters. As the diameter increases, the plasmonic peak shifted toward a longer wavelength (redshift) [122]. It should be noted that direct comparison of absorbance between BPAA and Ag BNW/BPAA must be avoided; plasmonic resonance and wave-guiding modes are subject to the changes in their surroundings [130].

In contrast to Ag thin film thickness as low as 9 nm, which exhibited significant decreases in wavelength absorbance above 1 μm [121], the A of Ag BNWs remained at approximately 40 % for this wavelength range. The light that was not absorbed into the top branches of the Ag BNWs with the smallest diameters reached the regions with larger diameters and was absorbed in the lower branches having higher diameters.

It is interesting to note that the volume filling fractions of the pores in these BPAA templates were determined to be ~19.6 % for the topmost branches, ~16.2 % for the middle branches, and ~9.1 % for the bottom trunk regions of the template [128]. This is the reverse of the typical tapered transition one would employ to achieve a low R. The relatively small reflectance in the UV-visible range and the high transmittance despite the high impedance mismatch indicates a wave-guiding effect in the structure.

The optical properties of Ag BNWs and BPAA composites were numerically calculated using the spectral averaging of the FDTD data from indiscriminately selected frames. Simulations were completed for a number of frames until a convergent set of averaged spectra was obtained [131]. For simplicity, the BNWs were split into three layers whose diameters (and lengths) were 20 nm (500 nm), 100 nm (500 nm), and 150 nm (4 μm), respectively. The packing density of Ag BNW was considered in this calculation as well. As shown in Figure 45, R, T, and A were all in general agreement with our quantitative experimental data. R and T were slightly higher in numerical calculation, by 15 – 20 %; as a result, A in the wavelength range of 900 nm – 2 μm remained at 30 %. Considering that the experimental data showed 40 % absorption, the increased absorption in the experiment is because the actual length of Ag BNWs varies up to 60 μm. This

provides another indication that the packing density of Ag BNWs may be higher than our estimation (33 %).

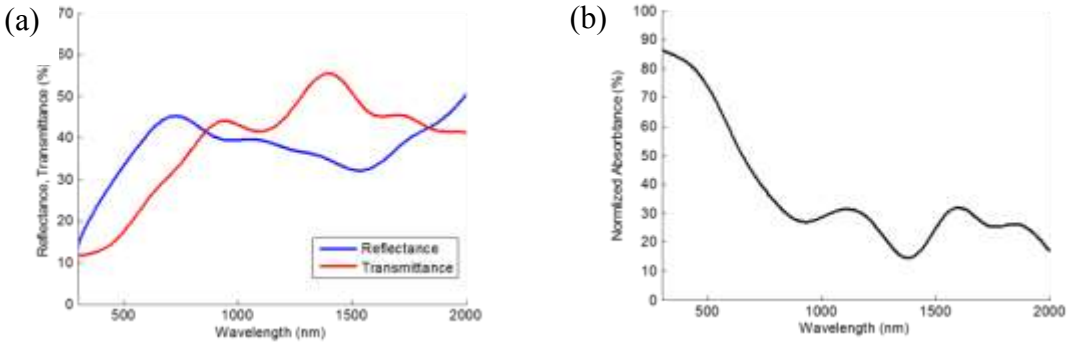

Figure 45. Numerically calculated (a) reflectance, transmittance, and (b) Normalized absorbance of Ag BNWs and BPAA composite when incident light is perpendicular to the surface of AgBNWs/BPAA structure [119].

7.5 Conclusion

In this work, vertically aligned, hierarchically stacked, and randomly branched AgNWs were grown in a template-assisted process by electrodeposition. The BNWs were found to be independently branched, continuous and parallel. The low reflectance and transmittance of the sample appears to be due to the presence of the vertical arrays of Ag BNWs. The normalized absorbance of the Ag BNWs was higher (100-70 %) in the UV-visible part of the spectrum and decreased around ~40 % for the wavelengths in the NIR range. The appreciable transmittance in the structure along with the lower reflectance (UV-visible) is thought to be due to the structure's wave-guiding effect.

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VITA

EDUCATION

PURDUE UNIVERSITY — West Lafayette, IN
Ph.D. candidate in Electrical and Computer Engineering — Aug 2019
Advisor: Prof. David B. Janes

COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK — New York, NY
M.S. in Electrical Engineering — Feb 2012
Concentration: *Solid State Science and Engineering*

SUNGKYUNKWAN UNIVERSITY (SKKU) — Suwon, Korea
B.S. in Physics (with distinction) — Feb 2010

RESEARCH EXPERIENCE

DIRECT SENSING SAMPLER FOR SUBMICRON MINING PARTICLES (FUNDED BY ALPHA FOUNDATION) — West Lafayette, IN

- Designed & fabricated capacitive sensors for sum-micron and nanoparticles detection and microheater integration for humidity control.
- Developed personal sampler that can measure respirable particles on the scale of submicron and nanometer.
- Developed a pulse width modulation (PWM) readout circuit for real-time monitoring of capacitive sensing.

MICROCOOLING FOR INTENSELY CONCENTRATED ELECTRONICS (MICROICE) (FUNDED BY DARPA, Press release by Purdue**:** https://goo.gl/wdw5pF**)** — West Lafayette, IN

- Fabricated a compact hierarchical manifold microchannel heat sink array with an envelope of 5×5 mm^2 for evaporative intrachip cooling.
- Designed and fabricated thin film platinum micro-heater capable of heat generation up to 5 kW/cm^2.
- Developed platinum resistance temperature detector (RTD) for monitoring of local chip temperature.

RELIABILITY OF THIN-FILM MICRO-HEATER AND RESISTANCE THERMOMETER — West Lafayette, IN

- Studied reliability on platinum micro-heater reaching electromigration limit and thermal stability on resistance thermometer (RTD).
- Characterized activation energy & current factor on Black's equation for thin-film platinum.
- Built data acquisition system using LabVIEW and current source/voltage regulation circuity for electromigration test.

1D-2D HYBRID TRANSPARENT CONDUCTORS & NANOWIRE GROWTH (FUNDED BY NSF) — West Lafayette, IN

- Fabricated copper nanowire/graphene hybrid network for transparent conductors.

- Characterized hotspots on nanowire networks analyzed surface properties using thermoreflectance imaging and Fourier-transform infrared spectroscopy (FT-IR).
- Electrodeposited vertically aligned nanowire arrays on single-layer graphene for infrared detector and studied its optical properties.

COLUMBIA LABORATORY FOR UNCONVENTIONAL ELECTRONICS (CLUE) New York, NY

- Developed organic solar cell with single-layer graphene as transparent electrode.
- Studied functionalization of polydimethylsiloxane (PDMS) for graphene transfer.
- Studied theoretical limit of single/tandem solar cell efficiency and characterization of materials using MATLAB simulation.

TEACHING EXPERIENCE

IC FABRICATION LABORATORY (ECE 557 - GRADUATE LEVEL COURSE) West Lafayette, IN

Teaching Assistant

- Performed training about fume hoods safety and cleanroom.
- Taught comprehensive microfabrication skills such as photolithography and etching.
- Taught basic electrical characterization skills using MOS capacitor and MEMS cantilever.

HONORS & SCHOLARSHIPS

- Best Paper Award in the Emerging Technologies Track at IEEE ITherm Conference
- Sungkyunkwan University (SKKU) Academic Excellence Scholarship
- Distinguished Service Medal by the President of SKKU

PUBLICATIONS

- Doosan Back, Kevin P. Drummond, Michael D. Sinanis, Justin A. Weibel, Suresh V. Garimella, Dimitrios Peroulis, and David B. Janes, "Design, Fabrication, and Characterization of a Compact Hierarchical Manifold Microchannel Heat Sink Arrays for Two-Phase Cooling", *IEEE Transactions on Component, Packaging, Manufacturing Technology* (DOI: 10.1109/TCPMT.2019.2899648)

- Kevin P. Drummond, Doosan Back, Michael D. Sinanis, David B. Janes, Dimitrios Peroulis, Justin A. Weibel, and Suresh V. Garimella, "Characterization of Hierarchical Manifold Microchannel Heat Sink Arrays Under Simultaneous Background and Hotspot Heating Conditions", *International Journal of Heat and Mass Transfer*, 126 (2018) 1289–1301

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- Doosan Back, Yuki Mori, Kazuhiko Matsumoto, and David B. Janes, "Optical and electrical characterization of CuNW/Graphene hybrid structure for transparent conductor", *59th Electronic Materials Conference*, South Bend, IN, June 2017

- Kevin P. Drummond, Justin A. Weibel, Suresh V. Garimella, Doosan Back, David B. Janes, Michael D. Sinanis, Dimitrios Peroulis, "Evaporative intrachip hotspot cooling with a hierarchical manifold microchannel heat sink array", *IEEE Thermal and Thermomechanical Phenomena in Electronic Systems Conference, 2016 15th IEEE Intersociety Conference on*, p307-315

- Suprem R. Das, Qiong Nian, Mojib Saei, Shengyu Jin, Doosan Back, Prashant Kumar, David B. Janes, Muhammad A. Alam, Gary J. Cheng, "Single-layer graphene as a barrier layer for intense UV laser-induced damages for silver nanowire network", *ACS Nano*, 2015, 9(11), pp 11121-11133

- Kevin P. Drummond, Justin A. Weibel, Suresh V. Garimella, Doosan Back, David B. Janes, Michael D. Sinanis, and Dimitrios Peroulis, "Fabrication and Characterization of a Hierarchical Microchannel Heat Sink Array for Evaporative Intrachip Cooling", *40th Annual Government Microcircuit Applications & Critical Technology (GOMACTech) Conference*, St. Louis, MO, 2015

- Asaduzzaman Mohammad*, Doosan Back*, Jieran Fang, Alex Kildishev, and David B. Janes, "Optical Characteristics of Vertically Aligned Arrays of Branched Silver Nanowires", *Proceedings of the 14th IEEE International Conference on Nanotechnology (IEEE-NANO)*, Toronto, Canada, August 18-21, 2014, 563-566