DEVICE-CIRCUIT CO-DESIGN EMPLOYING PHASE TRANSITION MATERIALS FOR LOW POWER ELECTRONICS

by

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Dedicated to my wife and my parents for their unconditional love and support.

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ABSTRACT

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Phase transition materials (PTM) have garnered immense interest in concurrent post-CMOS electronics, due to their unique properties such as - electrically driven abrupt resistance switching, hysteresis, and high selectivity. The phase transitions can be attributed to diverse material-specific phenomena, including- correlated electrons, filamentary ion diffusion, and dimerization. In this research, we explore the application space for these materials through extensive device-circuit co-design and propose new ideas harnessing their unique electrical properties. The abrupt transitions and high selectivity of PTMs enable steep (< 60 mV/decade) switching characteristics in Hyper-FET, a promising post-CMOS transistor. We explore device-circuit co-design methodology for Hyper-FET and identify the criterion for material down-selection. We evaluate the achievable voltage swing, energy-delay trade-off, and noise response for this novel device. In addition to the application in low power logic device, PTMs can actively facilitate non-volatile memory design. We propose a PTM augmented Spin Transfer Torque (STT) MRAM that utilizes selective phase transitions to boost the sense margin and stability of stored data, simultaneously. We show that such selective transitions can also be used to improve other MRAM designs with separate read/write paths, avoiding the possibility of read-write conflicts. Further, we analyze the application of PTMs as selectors in cross-point memories. We establish a general simulation framework for cross-point memory array with PTM based *selector*. We explore the biasing constraints, develop detailed design methodology, and deduce figures of merit for PTM selectors. We also develop a computationally efficient compact model to estimate the leakage through the sneak paths in a cross-point array. Subsequently, we present a new sense amplifier design utilizing PTM, which offers built-in tunable reference with low power and area demand. Finally, we show that the hysteretic characteristics of unipolar PTMs can be utilized to achieve highly efficient rectification.

We validate the idea by demonstrating significant design improvements in a *Cockcroft-Walton Multiplier,* implemented with TS based rectifiers. We emphasize the need to explore other PTMs with high endurance, thermal stability, and faster switching to enable many more innovative applications in the future.

1. INTRODUCTION

1.1 Device-Circuit Co-design for Exploratory Technologies

Relentless evolution of modern electronics has motivated diverse exploratory research on computing and date storage. For decades, periodic downscaling of transistors, dictated by Moore's law [1]–[4], has fueled progress of electronic technologies. To cope with the stupendous growth of the computation complexity in digital systems, it is necessary to keep shrinking the transistors to enhance integration density. However, concerns about the end of the golden age of scaling is building up as the transistor sizes are approaching atomic dimensions. Shorter channel length invokes quantum effects, short channel effects and fabrication challenges [4]. In addition, the fundamental *Boltzmann limit* [4]–[6] (stemming from statistical distribution of free carriers) has become a major hindrance against continued improvement of device and circuit performance [4], [5]. Hence, the quest for alternative device structures, physical phenomena and novel circuit topologies is garnering interest. To satiate the need for superior performance and throughput, design of high-speed transistors has been a perpetual research field. However, due to the surge in interest for portable, wearable and implantable electronic systems, the design of ultra-low power devices/circuits/architectures has also received a major impetus in the recent decades.

Several device structures are being explored to harness sub-kT/q (sub-60 mV/decade) switching to enable ultra-low power circuit operation [5]–[14]. These novel exploratory devices offer unique opportunities and challenges, which need to be thoroughly examined before striding towards industrial realization. Tunnel FET (TFET) [11], [15]–[17], Negative Capacitance FET (NCFET) [14], [18]–[20] and Hyper-FET [6], [21]–[24] are few such examples of steep switching devices. TFETs use modulation of quantum tunneling through a barrier [15] to achieve sharper switching characteristics. However, the design of p-type TFETs with ON currents comparable to the n-type TFETs is still a challenge [8], [16]. In contrast to the TFET, an NCFET achieves steep switching by utilizing the negative capacitance exhibited by the ferroelectric material introduced as an extra layer in the gate stack [14], [19]. A voltage-step-up action is achieved due to the

negative capacitance of the ferroelectric, which yields lower sub-threshold swing and higher ON current (I_{ON}) [25], [26]. However, the voltage step-up action is accompanied by an increase in the gate capacitance, which may offset the benefits of higher I_{ON} [18], [25]–[27]. Hyper-FET utilizes the insulator-metal transitions of an augmented phase transition material (PTM) [22], [28]–[30] to achieve steep switching. The PTM, by virtue of its current driven abrupt switching from the insulating state to the metallic state and vice versa, assists in transistor switching. However, being a hysteretic device, it leads to a complex design space for digital applications. All these examples hint at the necessity to co-design devices and circuits, while dealing with exploratory technologies.

In addition to the devices that make up the logic and computational components of a system, storage elements also mandate rapid reformation. The humungous boost in creation of digital data across the world has led to an unprecedented need for storage. Rapid growth of social networks, large-scale scientific experiments and the internet-of-things (IoT) are some of the major contributors to this overwhelming trend. Design and development of memory technology has become more vital than ever before. There is need for memory devices and architectures that allow faster access. In addition, there is huge demand for non-volatile memory systems, which are appropriate for energy-constrained systems such as portable electronics and energy harvesting platforms. Several non-volatile memory devices have been developed over the past few decades. Resistive RAM [31]–[34], Phase Change Memory [35]–[38], Ferroelectric RAM [39]–[43], NAND/NOR Flash [44]–[48] and Magnetic RAM [49]–[54] are some of the major variants. However, each of these devices have their own limitations and overheads [32], [40], [55]–[58] and there is a strong need to continue the exploration of innovative design approaches to complement or replace the existing design methodologies. Similar to the innovations in the device and circuit level, incorporation of novel architectures is also vital to harness greatest benefit out of the emerging technologies.

Electronics, as we know it, is going through a major paradigm shift. This revolutionary transformation to the post-CMOS era necessitates exploration of unique materials, devices, circuits and systems to cater to the growing demands. Silicon based technology has served

its purpose successfully for decades and has attained maturity. However, even with well-developed process technologies, Si based transistors are under-equipped for next generation challenges. A strong need to search for post-CMOS technologies is being echoed across the semiconductor industry. By dint of the research thrust provided by this buzzing interest, new materials and device structures are being proposed and studied. 'Phase transition material' is one of the most promising families of emerging post-Si materials. The unique electrical properties of these materials can be utilized to design novel logic/memory devices and circuits, to facilitate next-generation electronics. This thesis presents some exclusive ideas and techniques regarding potential uses for phase transition materials in designing low-power logic and memory. Comprehensive device-circuit co-design has been carried out for each of these ideas and techniques to analyze the possible implications and feasibility.

1.2 Phase Transition Materials (PTM)

Phase transition materials (PTM) are entities that exhibit abrupt change in resistance due to insulator-metal and metal-insulator transitions triggered by electrical [59][60], thermal [61], mechanical (pressure, strain) [62], [63] or optical stimuli [64]. The phase transitions can be attributed to diverse physical mechanisms (electron-electron correlation [65], [66], filamentary ion diffusion [21], [67], dimerization [68] etc.) in different materials. The

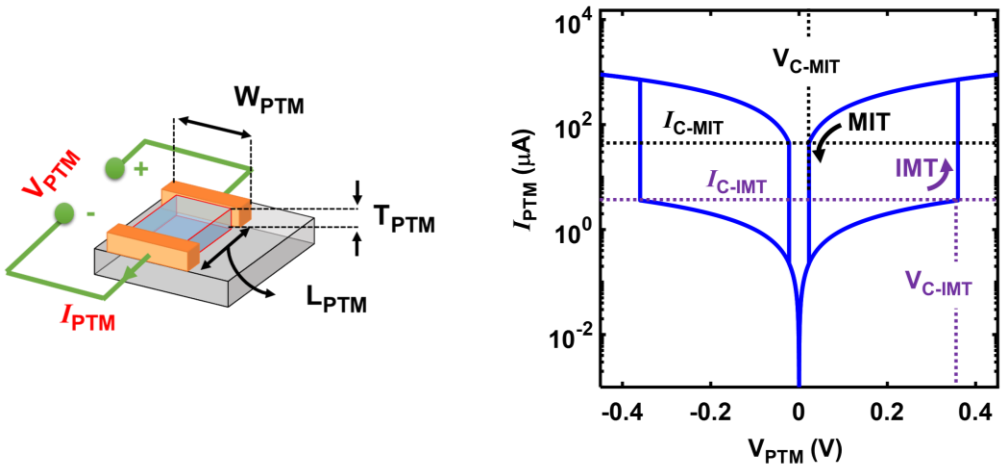


Fig. 1.1 Current-Voltage (*I-V*) Characteristics of a typical phase transition material. The critical voltage/current levels corresponding to phase transitions have been marked.

family of PTMs is quite rich with materials (e.g. VO_2, V_2O_3, V_2O_4, TiO, Ti_2O_3, $SmNiO_3$, Cu-doped HfO_2, doped chalcogenide etc. [22], [67], [69]–[74]), exhibiting a wide range of resistivity, hysteresis and thermal stability. Moreover, new PTMs are being extensively explored and novel approaches, such as using strain, have been reported to tailor their properties [75]. Such techniques and a wide spectrum of PTMs show promise to down select and optimize the PTMs, as per the needs of specific applications. Note, the materials that undergo such transitions due to having strongly correlated electrons are known as 'Correlated Materials (CM)' [76], [77]. The high and low resistance states of all these transitioning materials are abruptly separated by transition threshold levels. Therefore, they are often referred to as 'Threshold Switches (TS)' [21], [78], [79]. In literature, they are also mentioned as- 'Insulator-Metal Transitioning (IMT) Material' [80]–[83]. Depending on the application, most appropriate acronym will be used for these materials in different chapters of this thesis. However, irrespective of the underlying physical phenomenon, the electrical characteristics of these materials can be behaviorally generalized as follows.

PTMs exist in two phases - metal and insulator, with the resistance of the insulating phase (R_{INS}) usually being orders of magnitude higher than the resistance of the metallic phase (R_{MET}). Fig. 1.1 shows the current-voltage (I-V) response and device geometry for a typical PTM. W_{PTM}, L_{PTM} and T_{PTM} are the width, length and thickness (respectively) of the PTM. In absence of the electrical stimuli, PTMs remain in the insulating phase. In response to a sufficiently high current ($I_{C\text{-}IMT}$) (or voltage $V_{C\text{-}IMT}$) flowing through (applied across) the material, insulator-to-metal transition (IMT) occurs. Conversely, reduction of current/voltage below a critical level ($I_{C\text{-}MIT}$ or $V_{C\text{-}MIT}$) triggers metal-to-insulator transition (MIT). Such transitions lead to an inherently hysteretic behavior in these materials. The IMT and MIT have been shown to be abrupt (but not instantaneous) [84]–[86]. The critical current density for IMT and MIT transitions ($J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$) and the resistivity of metallic and insulating states (ρ_{MET} and ρ_{INS}) are device/geometry independent material parameters. The device specific parameters ($I_{C\text{-}IMT}$, $I_{C\text{-}MIT}$, R_{MET} and R_{INS}) can be expressed in terms of material level parameters (and geometric dimensions) as shown below.

$$I_{C\text{-}IMT} = J_{C\text{-}IMT} \times W_{PTM} \times T_{PTM} \tag{1.1}$$

$$I_{C\text{-}MIT} = J_{C\text{-}MIT} \times W_{PTM} \times T_{PTM} \quad (1.2)$$

$$R_{MET} = \rho_{MET} \times L_{PTM} / (W_{PTM} \times T_{PTM}) \quad (1.3)$$

$$R_{INS} = \rho_{INS} \times L_{PTM} / (W_{PTM} \times T_{PTM}) \quad (1.4)$$

An important point to note is that some materials, especially those that exhibit filamentary conduction [21], [67], may not exhibit linear dependence of resistance on area (A_{PTM} = $W_{PTM} \times T_{PTM}$). Similarly, the relationship between resistance and length (L_{PTM}) may be non-linear. For such materials with a complex dependence of the resistance on the geometry, the effective resistivities, ρ_{MET} and ρ_{INS} are defined as R_{INS} (A_{PTM}, L_{PTM}) $\times A_{PTM} / L_{PTM}$ and R_{MET} (A_{PTM}, L_{PTM}) $\times A_{PTM} / L_{PTM}$, respectively. Here, $R_{INS\ /\ MET}$ (A_{PTM}, L_{PTM}) are insulating/metallic resistances of the selector with non-linear dependence on A_{PTM} and L_{PTM}. It can be observed that, the effective resistivities, in general, can be functions of geometry and may not be just a constant parameter. The effective resistivities can also be functions of the voltage across the selector. In addition, by virtue of similar effects, $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$

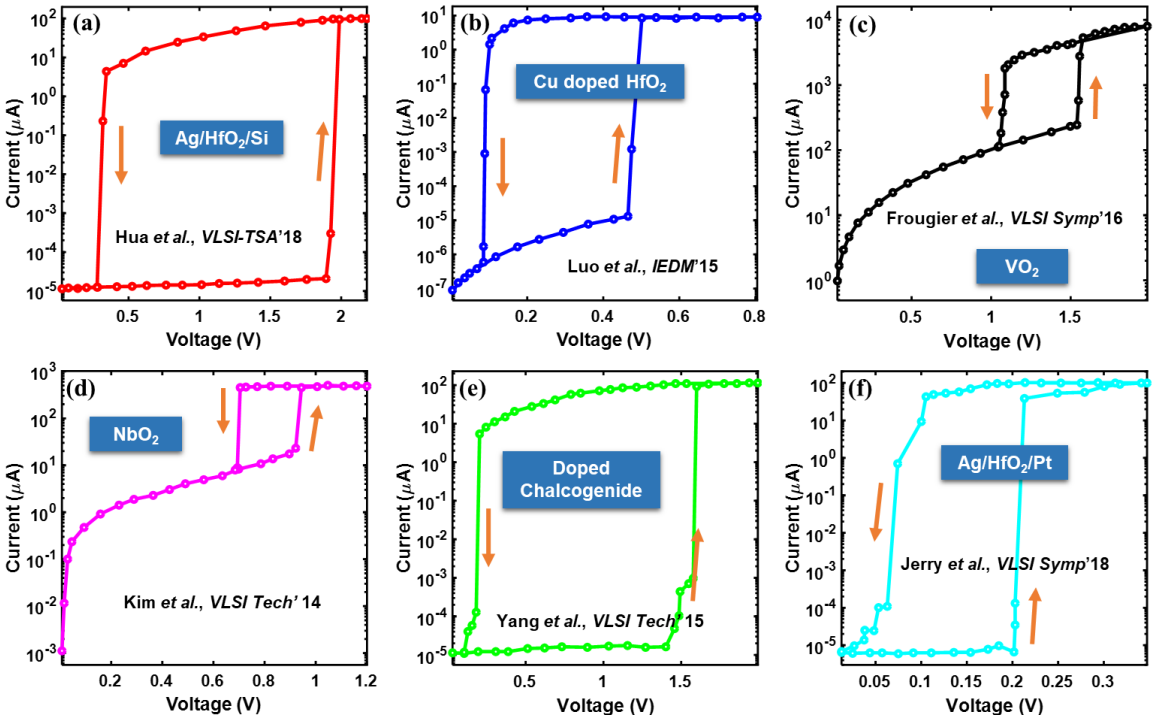


Fig. 1.2 Compilation of measured current-voltage (*I-V*) characteristics of a few phase transition materials reported in literature. (a) Ag/HfO_2/Si (b) Cu-doped HfO_2 (c) VO_2 (d) NbO_2 (e) doped chalcogenide (f) Ag/HfO_2/Pt.

may also be functions of area. Furthermore, some PTMs can exhibit unipolar (responding to only positive/negative polarity of voltage) electrical characteristics. To summarize, the prime features of the electrical characteristics of PTMs are: (a) abrupt transitions (b) high resistance ratio and (c) hysteresis. Fig. 1.2 presents the *I-V* characteristics of a few PTMs reported in literature ([21], [22], [67], [73], [78], [87]). Noticeably, all these materials have the signatures of the three major features of PTM, even though the transition mechanisms may be different.

1.3 Contributions of this Dissertation

The prime target of this dissertation is to analyze the unique properties of phase transition materials and explore their applications at the device and circuit levels. We utilize a simulation-based approach to propose and verify several unique techniques to improve logic and memory designs. We establish compact models and frameworks to perform device, circuit and array level simulations. A brief overview of the major contributions and the contents of the subsequent chapters is as follows

(a) We first explore PTM-augmented MRAM, which utilizes selective transitions of PTMs to enhance the read performance of Spin Transfer Torque (STT) MRAMs. Chapter 2 covers the details of this proposed technique.

(b) In chapter 3, we propose a different variant of PTM augmented multi-port MRAM that utilizes separate read/write paths and provides a unique set of advantages including high sense margin and better read stability.

(c) Chapter 4 presents a comprehensive analysis and establishes the design methodology, biasing constraints and optimization procedure for cross-point memory array with PTM based selectors.

(d) Chapter 5 complements our extensive work on cross-point array design by directing special focus on sneak path leakage analysis. We present a computationally efficient compact modeling approach to estimate leakage in a cross-point array with PTM based threshold-switching selectors.

(e) Chapter 6 analyzes the device-circuit co-design space for the PTM augmented steep switching transistor, called Hyper-FET. We investigate the impact of its unique device level characteristics on circuit level performance and provide directions for material down selection.

(f) In chapter 7, we present a novel sense amplifier design with built-in reference, utilizing unique properties of phase transition materials. In addition to analyzing the performance benefits, we discuss the process to tune the reference dynamically to counter the effect of variation.

(g) In chapter 8, we explore a unique design of using the inherent hysteresis and unipolar phase transitions in $Ag/HfO_2/Pt$ threshold switch for efficient rectification. We implement a Cockcroft-Walton voltage multiplier using $Ag/HfO_2/Pt$ based rectifiers to validate the idea and illustrate the benefits.

(h) Chapter 9 concludes this dissertation and provides a brief discussion on some possible future directions for PTM based designs.

2. THRESHOLD SWITCH AUGMENTED STT MRAM

2.1 Introduction

Spin Transfer Torque (STT) MRAM has drawn immense attention as a non-volatile memory device due to several promising features including high retention time, thermal stability, impressive reliability and CMOS compatibility [51], [58], [88], [89]. STT MRAM comprises of a magnetic tunnel junction (MTJ) and an access transistor (Fig. 2.1 (a)). The MTJ stores data in the form of relative magnetization between its two magnetic layers called pinned layer (PL) and free layer (FL). These two layers are separated by an oxide (usually MgO) layer, which acts as a tunnel barrier. If the FL possesses a magnetization parallel to the PL, the MTJ exhibits low resistance state (LRS) which is also referred to as parallel (P) state. On the contrary, if the magnetization of the FL is opposite to that of the PL, the MTJ presents high resistance state (HRS) or anti-parallel (AP) state.

The relative difference between resistances of P and AP states of the MTJ (R_P and R_{AP} respectively) is called tunneling magneto resistance (TMR). The TMR, defined as (R_{AP} - R_P) /$R_{P,}$ is a direct measure of the distinguishability of the stored data in an MTJ. Despite having several favorable characteristics, a big challenge for STT MRAMs is the low inherent TMR (~ < 200 %) of the MTJ [58]. In addition, the resistance of the access transistor (R_{FET}) sullies the TMR of the overall memory cell. Hence, the overall distinguishability of stored data in a STT MRAM is represented by its cell TMR (CTMR), defined as (R_{AP} - R_P) / (R_P + R_{FET}). Low CTMR of the STT MRAM yields low sense margin (SM) making it challenging to design sensing circuits [90], [91]. Thus, improving the CTMR and SM is amongst the most important needs for STT MRAM design. In addition to high distinguishability, robust read operation demands high stability of the stored data, which is measured by read disturb margin (RDM). It is necessary to ensure sufficiently high RDM and SM (or CTMR) in a memory cell [79], [92], [93]. However, the SM and RDM in a STT MRAM typically have conflicting requirements [93], [94]. In addition, the write operation shares the current path with read which results in read-write conflict and aggravates the design challenges. This is because in STT MRAMs, the MTJ undergoes

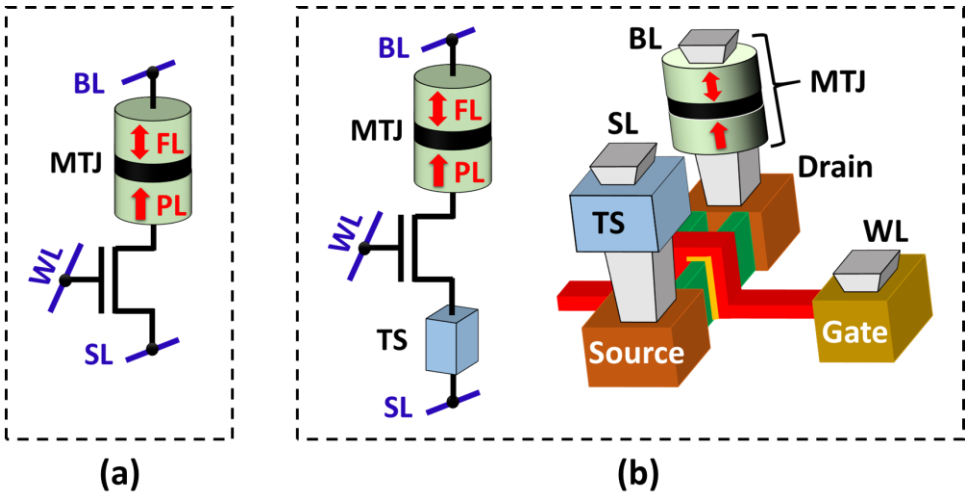


Fig. 2.1 (a) Schematic diagram of a spin transfer torque (STT) MRAM cell. (b) Schematic and 3D structure for a threshold switch augmented MRAM.

P→AP and AP→P transitions driven by *spin transfer torque* [95], [96] induced through bi-directional current flow. Write current (I_{WRITE}) in STT MRAM needs to be larger than critical values ($I_{CRIT:\ AP\rightarrow P}$ and $I_{CRIT:\ P\rightarrow AP}$) to achieve desired switching in MTJ. The read stability and write speed have conflicting current requirements, making it challenging to improve the read performance without degrading the write performance (and *vice versa*).

Various efforts have been directed towards mitigating the design conflicts of STT MRAM [97]–[99]. Conjoining MTJ with physical phenomena like *Spin Hall effect* [97], [100], *Seebeck effec*t [98] and *Rashba effect* [99] have been explored as means to overcome limitations of standard STT MRAMs. While useful in several aspects, these approaches have their own challenges in terms of fabrication complexity, variability and area impact [89]. With the emergence of new materials with unique properties, it becomes important to explore novel opportunities of designing spin-memories by employing such materials in conjunction with the MTJs. In this chapter, we present a unique approach to optimize the read operation of STT MRAM. The idea is to employ correlated material, such as VO_2 [22], [30] with the STT MRAM cell (Fig. 2.1 (b)) and obtain selective phase transition in VO_2 to boost the SM as well as RDM. This approach shows promise to significantly improve the read operation and moderately reduce write power with no area penalty and minimal

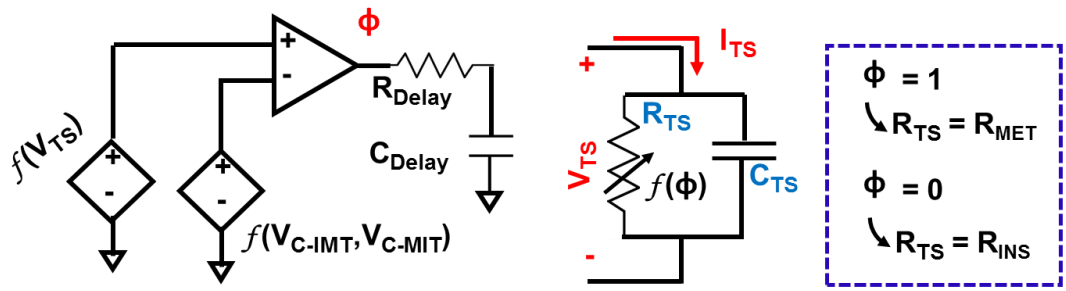


Fig. 2.2 Behavioral representation of the phenomenological model for threshold switch / phase transition materials.

adverse effect on write speed [79], [93]. With such advantages, it is crucial to also explore the proper design space of this novel approach and establish a proper optimization methodology. Besides, analysis to assess impact of variations is also vital. Here, we provide a comprehensive evaluation of the design space and degree of variation tolerance for this technique. Note, we first evaluated this technique using VO_2, which has strong electron-electron correlation (hence, the name correlated material). But there are other physical processes like filamentary ion diffusion or dimerization [21], [67] that yield similar insulator ↔ metal switching behavior. This family of materials is often referred to as *Threshold Switch (TS)*. Any of such bi-directional TS can be used to realize the technique proposed in [93]. To ensure generality of discussion, we will henceforth use the name-Threshold Switch Augmented STT MRAM (TSA MRAM) to refer to the proposed technique.

2.2 Modeling and Simulation Framework

We use a phenomenological circuit-compatible SPICE model [28], [79] to simulate characteristics of TS. The model assumes constant resistance of the TS in the insulating and metallic states. The voltage across the TS (V_{TS}) is compared to the critical levels ($V_{C\text{-}IMT}$ and $V_{C\text{-}MIT}$) to decide on the *phase* (and thereby its resistance, R_{TS}). Hence, the resistance switching behavior of the TS is invoked self-consistently in correlation with the biasing scenario. Fig. 2.2 shows the behavioral representation of this model. We calibrate this model with *I-V* characteristics of epitaxial VO_2 films reported in [6]. In addition to the

TS model, we use a physical model for the MTJ from [101]. We choose an MTJ with perpendicular magnetic anisotropy [102]. We use 20 nm predictive technology model [103] for the access transistor. The relevant parameters have been summarized in Table 2.1.

Table 2.1 List of Parameters Used for Simulation of STT and TSA MRAMs

	Parameters	Value
TS	R_{MET}, R_{INS}	0.5 KΩ, 100 KΩ
	$I_{C\text{-}IMT}$, $I_{C\text{-}MIT}$	3.6 μA, 45 μA
	T_{IMT}, T_{MIT}	500 ps, 1 ns
	L, Area, Intrinsic capacitance	45 nm, 4500 nm^2, 1fF
MTJ	Diameter, Oxide thickness ($T_{OX\text{-}MTJ}$)	40 nm, 1.1 nm
	Thickness of free layer	1.5 nm
	Saturation magnetization	700 KA/V
	Energy barrier, Gilbert Damping	56 K_BT, 0.028
Transistor	Technology node, # of Fins	20 nm, 4
	Fin height and Fin width	28 nm, 15 nm

2.3 Principle of Operation

TSA MRAM has a TS connected in series with the standard STT MRAM structure (Fig. 2.1). The TS and the MTJ are connected to opposite terminals (*source* and *drain*) of the access transistor (reason discussed later). Fig. 2.3 illustrates the principle of operation for the TSA MRAM. The target is to trigger selective phase transitions in the TS during read, depending on the stored data in MTJ. The bit line (BL) is pre-charged to read voltage (V_{READ}) and kept floating during read. After this, word line (WL) is asserted. The resulting increase in current through the cell (I_{CELL}) triggers IMT and drives the TS to metallic state (irrespective of the stored data in MTJ). The BL voltage (V_{BL}) starts to discharge through the memory cell. With the TS in the metallic state, the resistance of the cell is mainly governed by the MTJ. An MTJ storing P state presents less resistance in discharge path and allows larger current flow compared to an AP MTJ. Hence, the TS can remain in metallic state with an MTJ in P state throughout the entire read time span (T_{READ}). Conversely, the MTJ with AP state produces much lower I_{CELL}. Hence, I_{CELL} in AP state can quickly fall below $I_{C\text{-}MIT}$, triggering MIT in the TS (by design). Eventually, throughout

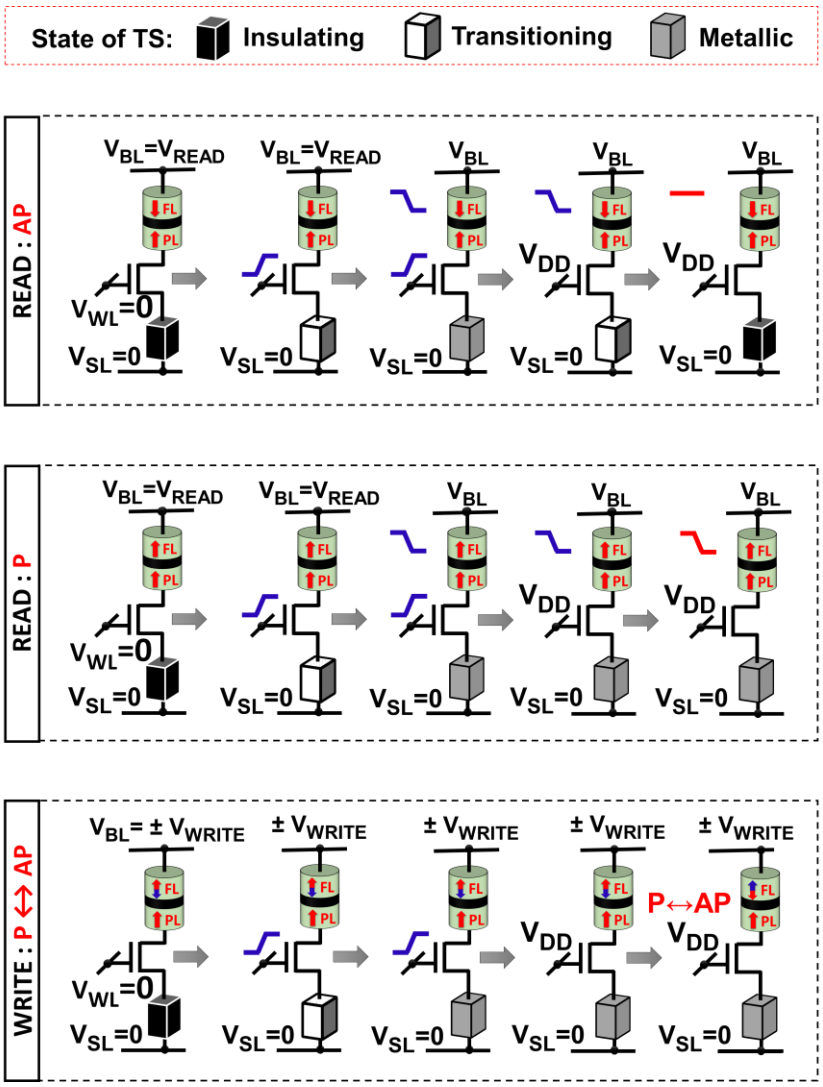


Fig. 2.3 Principle of operation for TSA MRAM.

most part of the read operation, TS exhibits its metallic state with a P MTJ and insulating state with AP MTJ. As a result, effective resistance in HRS of the cell becomes, $R_{HRS\text{-}TS} \approx (R_{AP} + R_{FET} + R_{INS})$ and in LRS of the cell becomes, $R_{LRS\text{-}TS} \approx (R_P + R_{FET} + R_{MET})$. In a standard STT MRAM, $R_{HRS\text{-}STD} \approx (R_{AP} + R_{FET})$ and $R_{LRS\text{-}STD} \approx (R_P + R_{FET})$. Since, $R_{INS} >>$ max [R_{MET}, R_P, R_{AP}] the TSA MRAM exhibits significantly high (quantified later) relative resistance difference compared to standard STT MRAM, yielding high CTMR and SM. In addition, an immense increase in cell resistance during AP read leads to reduction in corresponding read current ($I_{READ\text{-}AP}$). This reduction in read current (I_{READ}) can be utilized to reduce

accidental data flipping. We choose a biasing polarity for read, which restricts P→AP switching [93][104]. Hence, only AP→P flipping is possible and the RDM can be defined by: 1-($I_{READ\text{-}AP}$ /$I_{CRIT:\ AP\rightarrow P}$). As, $I_{READ\text{-}AP}$ is significantly less, TSA MRAM can achieve much higher RDM compared to STT MRAM. For the write operations, the TS needs to be triggered and maintained in metallic state throughout AP→P and P→AP write to avoid incurring much write penalty due to TS resistance. As $|I_{WRITE}| > I_{READ,}$ this can be ensured by designing the cell to achieve $|I_{WRITE}| > I_{C\text{-}MIT}$. During write, the TS undergoes IMT on assertion of the WL (as during read) and then remains in metallic state with a sufficiently high write voltage (V_{WRITE}).

2.4 Design Approach for TSA MRAM

The above description conceptually conveys the idea behind TSA MRAM. However, to achieve the desired selective phase transitions in TS, a meticulous design approach needs to be followed, which we discuss next.

Table 2.2 Design Space Related Terminologies for TSA MRAM

Term	Significance	Figure
$V_{CELL\text{-}MIT\text{-}(AP)\ /\ (P)}$	The V_{CELL} at which the metallic TS in a TSA MRAM with AP / P MTJ undergoes MIT.	3 (a): (V_1) 3 (a): (V_2)
$V_{CELL\text{-}IMT\text{-}(AP)\ /\ (P)}$	The V_{CELL} at which the insulating TS in a TSA MRAM with AP / P MTJ undergoes IMT.	3 (b): (V_3) 3 (a): (V_4)

2.4.1 Biasing Constraints

An important step to design a TSA MRAM is to deduce appropriate ranges for V_{READ} and V_{WRITE}, which enable the aforementioned phase transitions in TS. In Table 2.2, we define important threshold points of the cell voltage (V_{CELL}). Let us consider the read operation first. Fig. 2.4 (a) shows the I_{READ} versus V_{READ} plot for TSA and STT MRAM. Recall, after the initial IMT (due to assertion of WL), the TS should remain in metallic state for P MTJ and revert to insulating state for AP MTJ. Hence, V_{READ} needs to be less than $V_{CELL\text{-}MIT\text{-}(AP)}$ and greater than $V_{CELL\text{-}MIT\text{-}(P).}$ Therefore, the first condition to fulfil is,

$$V_{CELL\text{-}MIT\text{-}(P)} < V_{READ} < V_{CELL\text{-}MIT\text{-}(AP)} \quad (2.1)$$

On a different note, the TSA MRAM needs to be able to trigger IMT in TS (after assertion of the WL) at the chosen V_{READ}. So, another condition for V_{READ} is-

$$V_{READ} > V_{CELL\text{-}IMT\text{-}(P)} \quad (2.2)$$

Note, the above condition is defined for P MTJ since triggering the WL driven initial IMT is not a requirement for AP MTJ (as the TS will eventually revert to insulating state). For the case of P MTJ, the TS needs to be stable (non-oscillatory [30]) in metallic state throughout the read operation. Such stable operation demands,

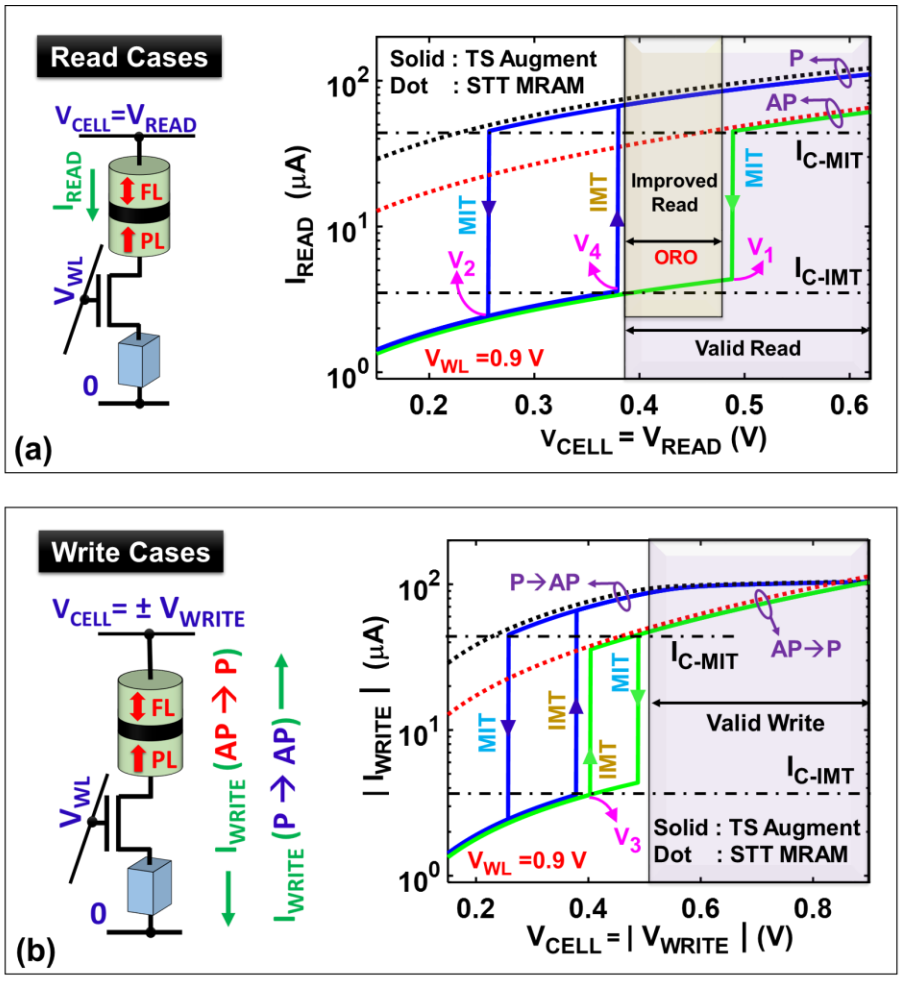


Fig. 2.4 Feasible range of bias voltage to ensure desired phase change in the threshold switch during (a) read and (b) write operations.

$$V_{CELL\text{-}IMT\text{-}(P)} > V_{CELL\text{-}MIT\text{-}(P)} \quad (2.3)$$

On the contrary, oscillatory mode may arise while reading AP MTJ. In such a scenario, voltage distribution among the series connected AP MTJ, transistor and TS yields $V_{CELL\text{-}IMT\text{-}(AP)} < V_{CELL\text{-}MIT\text{-}(AP)}$ (Fig. 2.4 (b)) and thereby results in oscillations [82], [105]. It is important to mention, this oscillatory mode is not mandatory for the TSA MRAM design and it may or may not occur depending on the relative resistance of the TS, MTJ and the access transistor. In fact, the discharging BL suppresses the oscillation in TS (if present) due to I_{CELL} reduction, which drives and keeps TS into the insulating state. Hence, $V_{CELL\text{-}IMT\text{-}(AP)}$ can be greater or less than $V_{CELL\text{-}MIT\text{-}(AP)}$. Combining, (2.1), (2.2) and (2.3) we get the condition that yields the desired operation as –

$$V_{CELL\text{-}IMT\text{-}(P)} < V_{READ} < V_{CELL\text{-}MIT\text{-}(AP)} \quad (2.4)$$

The range of V_{READ} that complies with (2.4), will be referred to as the optimum range of operation (ORO) hereafter (marked in Fig. 2.4 (a)). This represents the region in which TSA MRAM exhibits improved read over STT MRAM. Another point to mention is that, for $V_{READ} > \max [V_{CELL\text{-}MIT\text{-}(AP)}, V_{CELL\text{-}IMT\text{-}(AP)}]$, the TS will be in metallic state for both P and AP states of MTJ. Since metallic TS incurs only a small increase in the resistance, the TSA MRAM will still be able to achieve read functionality with mildly degraded performance compared to STT MRAM. Since, in this scenario the read functionality is maintained, this range has been marked as region for *valid read* in Fig. 2.4 (a). Note, the DC response (Fig. 2.4 (a)) shows an abrupt boundary between ORO and *valid read* regions. But due to transient effects (discussed later), TSA MRAM may exhibit benefits over the STT MRAM even when it is biased within *valid regio*n close to the ORO boundary. However, to ensure the desired benefit from the TSA MRAM, it is necessary to choose the V_{READ} from within the ORO (complying with (2.4)). Similarly, it is also necessary to establish a range for V_{WRITE}. Fig. 2.4 (b) shows I_{WRITE} versus V_{WRITE} characteristics for TSA and STT MRAMs. Clearly, if the TS can be maintained in metallic state with AP MTJ, it will be metallic with P MTJ. Hence, the following constraint is enough to enforce the TS to be in metallic state during write-

$$V_{WRITE} > \max[\, V_{CELL\text{-}IMT\text{-}(AP)}, V_{CELL\text{-}MIT\text{-}(AP)} \,] \quad (2.5)$$

The constraints described so far are based on DC considerations. We next evaluate the transient operation of the TSA MRAM and present additional design insights.

2.4.2 Transient Aspects of TSA MRAM Operation

Simulated transient waveforms for the read/write operation of STT and TSA MRAM have been illustrated in Fig. 2.5. Note, standard STT MRAMs may employ sensing mechanisms other than the one depicted here [57], [106], [107]. But, to understand the impact of TS on

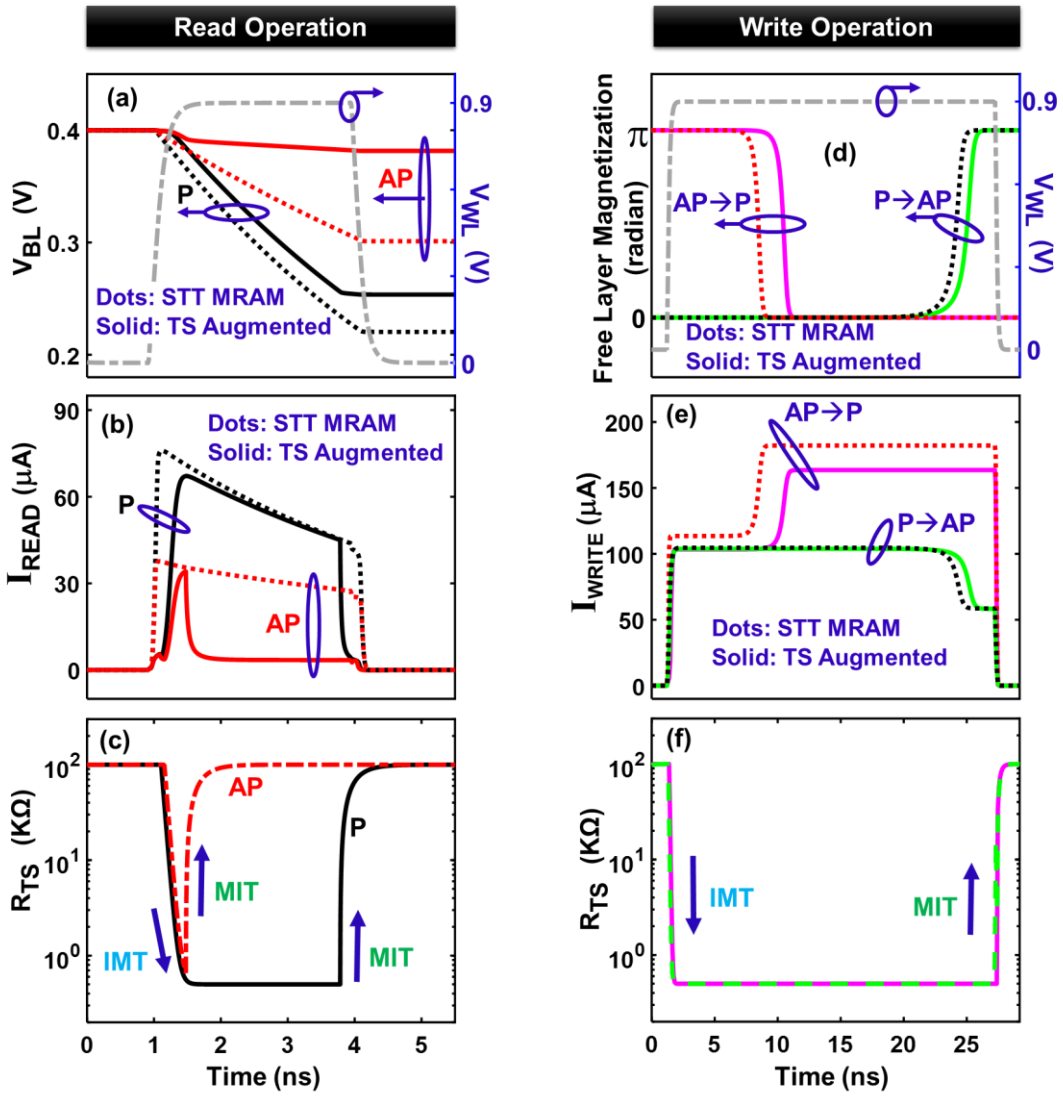


Fig. 2.5 Simulated transient response for (a-c) read and (d-f) write operations.

the read operation of the TSA MRAM, we compare STT and TSA MRAMs considering a similar sensing scheme. V_{BL} starts discharging after assertion of the WL (Fig. 2.5 (a)). For STT MRAM, a difference in the extents of BL discharge occurs solely due to the difference between R_P and R_{AP}. However, for TSA MRAM, the discharge for AP MTJ drastically reduces after TS undergoes MIT (as R_{INS} is large). Fig. 2.5 (b) shows the discharge current during the read operation. The TSA MRAM initially shows almost similar levels of discharge current as in a STT MRAM for both P and AP cases. That occurs due to the TS being in metallic state for both cases in the beginning of the read cycle. Note, V_{READ} has been chosen based on constraint (2.4). Therefore, after the initial IMT, the TS undergoes MIT for AP case (Fig. 2.5 (c)). During the major part of the read operation, the AP MTJ is accompanied with an insulating TS and the discharge becomes very low. But, the TS with P MTJ supports almost as high discharge current as in a standard STT MRAM storing P. Thus, for TSA MRAM, a larger voltage differential (ΔV_{BL}) is developed between BLs for P and AP cases. Note, due to the discharging BL, the voltage across the TS with P MTJ will also reduce below $V_{C\text{-}MIT,}$ if the WL is kept asserted for sufficiently long period. In that scenario, the TS with P MTJ will also exhibit MIT and ΔV_{BL} will get saturated (Fig. 2.5 (a)). Hence, ideally, the WL can be de-asserted prior to reaching this saturation condition.

The write operation of TSA MRAM does not impose any additional design constraints in terms of the transient response. The write time (T_{WRITE}) for the TSA MRAM is slightly (~3%) larger than that of the STT MRAM (Fig. 2.5 (d)). The reason is the slight reduction of I_{WRITE} due to the resistance of the metallic TS (Fig. 2.5 (e, f)). Such minute write penalty is observed for low R_{MET} (< 1 KΩ). Also note, the reduction in I_{WRITE} is more prominent in AP→P switching, whereas the P→AP switching experiences only mild reduction in I_{WRITE} (Fig. 2.5 (e)). This is related to the source degeneration of the access transistor. For AP→P transition, the TS contributes to reducing I_{WRITE} by presenting a series resistance (R_{MET}) and simultaneously source degenerating the access transistor. As a result, the effect of R_{MET} on AP→P write is large and leads to ~30% slower switching than standard STT MRAM. Note, lower I_{WRITE} also translates to significantly reduced (~10%) power for AP→P switching. But, for P→AP transition, the TS only provides a series resistance (R_{MET}). The access transistor in this case is source degenerated by the MTJ, as in standard STT MRAMs [51],

[58]. Hence, the effect of R_{MET} is very low leading to only 3% write time increase with similar P→AP switching power. Note, for MRAM write, P→AP transition is the bottleneck (due to MTJ induced source degeneration) [93], [108] and hence, T_{WRITE} is determined by the P→AP transition time ($T_{P\rightarrow AP}$). Note, augmenting the TS on the same side as the MTJ will cause stronger source degeneration during P→AP switching and therefore will lead to much longer $T_{WRITE.}$ We avoid that by connecting the MTJ and TS to opposite terminals of the access transistor.

Interestingly, the connection of the TS and the MTJ to the opposite end of the transistor, leads to a mild mitigation of asymmetry in the write operation [79], [93]. Standard STT MRAMs typically exhibit a large difference in the switching time for P→AP and AP→P transitions. This is due to the bi-directional write current, which leads to the source degeneration of the access transistor for just one of the state transitions. As a result, the write time is determined by the switching time for the case when current flows from source line (SL) to BL (i.e. when the access transistor is source-degenerated) [93], [108]. Consequently, significant energy is wasted unnecessarily when current flows from BL to SL. In TSA MRAM, the access transistor gets source degenerated for both the directions of the current flow. When current flows from SL to BL, the MTJ resistance leads to the source-degeneration, as in the standard STT MRAMs. When the current flows from BL to SL, the metallic resistance of the CM results in source degeneration (albeit the effect is mild). This moderately reduces the excessive write current in the cell, leading to write power savings. Eventually, the TSA MRAM suffers from a mild increase (~3%) in write time, but consumes ~10% less power compared to STT MRAM.

2.4.3 Optimization of Performance Metrics with Biasing

So far, we have directed our attention towards ensuring the desired transitions in TSA MRAM. In this sub-section, we quantify the performance metrics. Let us start with the read operation. The transient interplay between the phase transitioning TS and the remainder of the memory cell leads to non-monotonous trends in performance metrics with respect to $V_{READ.}$ Fig. 2.6 (a-d) show comparative trends for some important read performance metrics. These metrics have been calculated by simulating the transient read operation of the STT

and TSA MRAM for different V_{READ}. Hence, the trends seen in these results carry signature of the transient correlation between different components of TSA MRAM.

The TSA MRAM shows up to ~ 15X boost in CTMR (Fig. 2.6 (a)) for V_{READ} chosen from within the ORO (marked in Fig. 2.4 (a)). The improvement in CTMR is prominent for lower V_{READ} (< 0.45 V) within the ORO because of two reasons. Firstly, the inherent TMR of the MTJ is larger for lower V_{READ}. Secondly, the TS with AP state MTJ can quickly go back to insulating state if the BL is pre-charged with lower V_{READ}. Hence, the CTMR is maximized for lower V_{READ} (within ORO). Similar explanation applies for RDM and the average read power ($P_{READ-AVG}$) (Fig. 2.6 (c, d)). Lower $I_{READ-AP}$ results in reduction of the read power. For lower V_{READ} (< 0.45 V) within the ORO, we get ~27% enhancement in RDM and ~40% reduction in $P_{READ-AVG}$. The SM, however shows slightly complex and non-monotonic trend with V_{READ}. Note, the SM is defined as (V_{BL-AP} - V_{BL-P})/2. Here, V_{BL-P} and

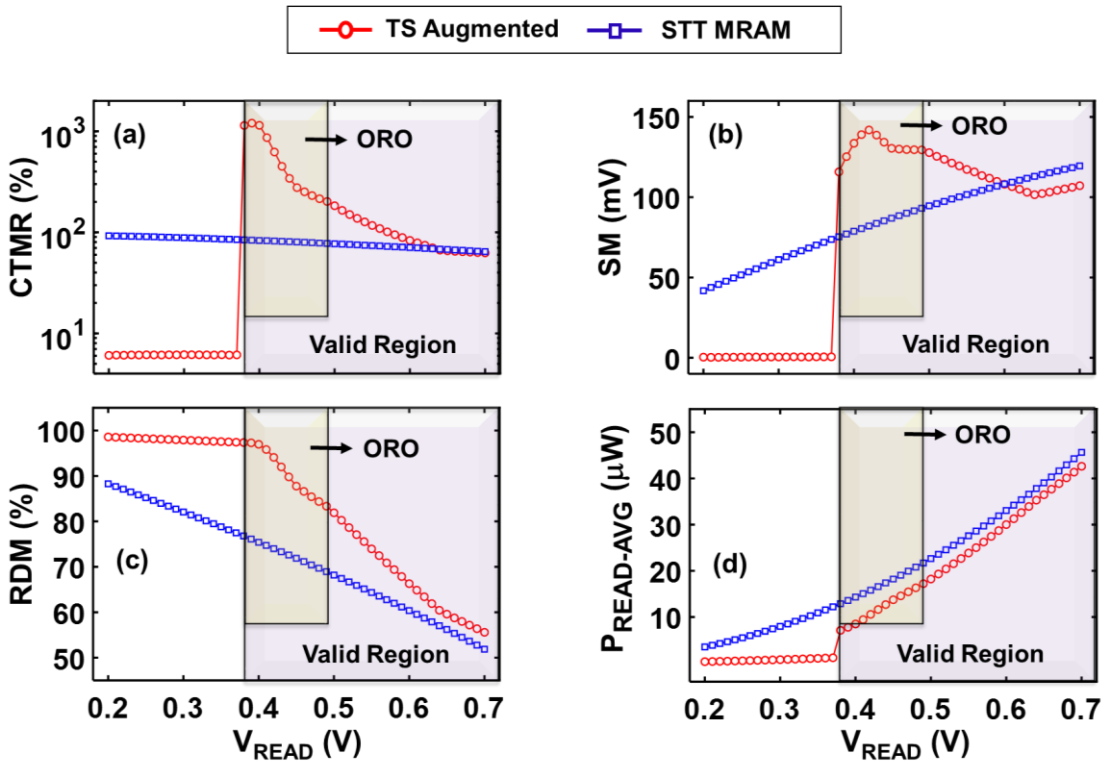


Fig. 2.6 Comparison of (a) cell tunneling magneto resistance (b) sense margin (c) read disturb margin and (d) average read power of STT and TSA MRAMs at different V_{READ}.

$V_{BL\text{-}AP}$ represent the values of V_{BL} at $t = T_{READ}$ for P and AP cases (respectively). As shown in Fig. 2.6 (b), the SM for the TSA MRAM increases with V_{READ} (within the ORO) up to $V_{READ} \approx 0.45$V. If a larger V_{READ} is chosen, the TS with AP MTJ, stays in metallic state longer, as the BL voltage takes more time to discharge below $V_{CELL\text{-}MIT\text{-}(AP)}$. Therefore, the initial discharge rates for both P and AP cases are high. By the time the TS undergoes MIT, the difference between $V_{BL\text{-}AP}$ and $V_{BL\text{-}P}$ gets slightly reduced and hence, the SM tends to decrease as V_{READ} increases beyond 0.45 V. Note, in all of these cases, the SM of the TSA MRAM is always much greater (~1.5X to 1.7X) than that of STT MRAM. Considering all these, it is optimal to choose V_{READ} for the TSA MRAM from within the lower portion (0.4-0.45V) of the ORO. Note, Fig. 2.6 (a-d) show performance improvements in TSA MRAM even beyond the ORO. This is a manifestation of the transient dynamics of the TS.

In addition to these trends, another important aspect needs to be considered to choose V_{READ} for TSA MRAM. Recall, the TSA MRAM initially (on assertion of WL) triggers IMT in the TS irrespective of the state of the MTJ. Then, based on the relative values of I_{READ}, the TS can either remain metallic or undergo MIT. This critical decision to trigger selective transition in TS is dependent on the difference of the initial I_{READ} with P and AP MTJ. We denote this quantity as $\Delta I_{READ\text{-}INIT}$. Compared to a STT MRAM at *iso*-V_{READ}, the TSA MRAM exhibits less $I_{READ\text{-}INIT}$ due to having an additional resistance (R_{MET}) in series (Fig.

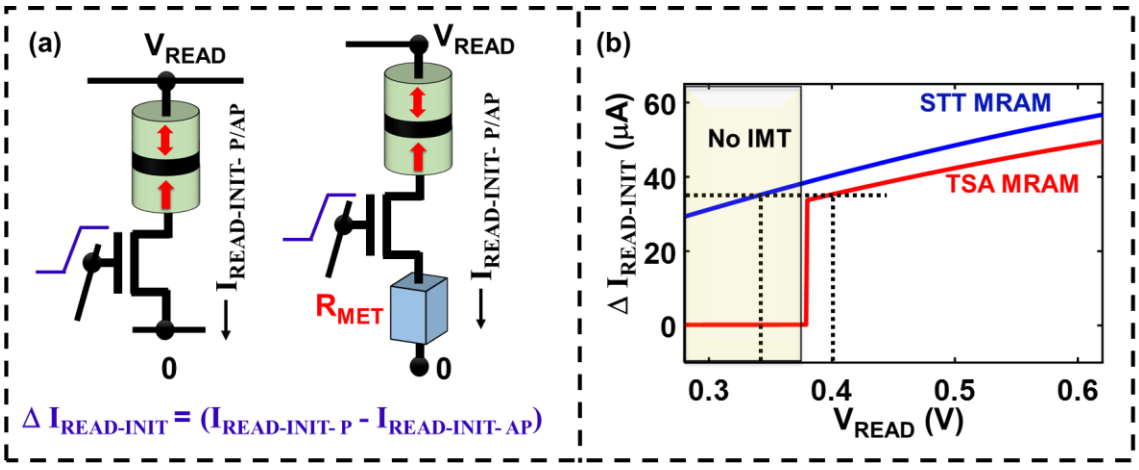


Fig. 2.7 (a) Illustration of $I_{READ\text{-}INIT}$ and (b) the concept of achieving *iso*- $\Delta I_{READ\text{-}INIT}$ between STT and TSA MRAMs.

2.7 (a, b)). To make sure that the robustness of the selective phase transition is not compromised due to the additional resistance, we choose a higher $V_{READ,}$ for TSA MRAM operation. To maintain same levels of $\Delta I_{READ\text{-}INIT}$ (Fig. 2.7 (b)), we use V_{READ} = 0.35 and 0.4 V for STT and TSA MRAM respectively (for subsequent analyses). *Note, the TSA MRAM permits use of higher V_{READ} without hurting the read stability, as it has significantly higher RDM compared to STT MRAM* (Fig. 2.6 (c)).

Fig. 2.8 (a, b) show the comparison for the write metrics. $|I_{WRITE}|$ for TSA MRAM is less than that of STT MRAM due to R_{MET}. That translates to lower average write power ($P_{WRITE\text{-}AVG}$) as shown in Fig. 2.8 (a). Actually, the power for AP→P transition in TSA MRAM is much less than that in STT MRAM. But, P→AP transition consumes almost same power for both cases. This difference is attributed to the source degeneration of the access transistor due to R_{MET} in the former case, as discussed before (in section 2.4.2). Recall, in the latter case, MTJ induced source degeneration determines I_{WRITE}, which reduces the effect of R_{MET}. On average, the TSA MRAM shows ~4-10% reduction in P_{WRITE} within the acceptable range of V_{WRITE}. Fig. 2.8 (b) shows that the TSA MRAM incurs slight increase (~3 to 7%) in T_{WRITE}, the reasons for which have been discussed in previous sub-section. In summary, it is important to choose a V_{READ} from within an appropriate range to ensure desired selective phase transitions. TSA MRAM can achieve significant boost in CTMR

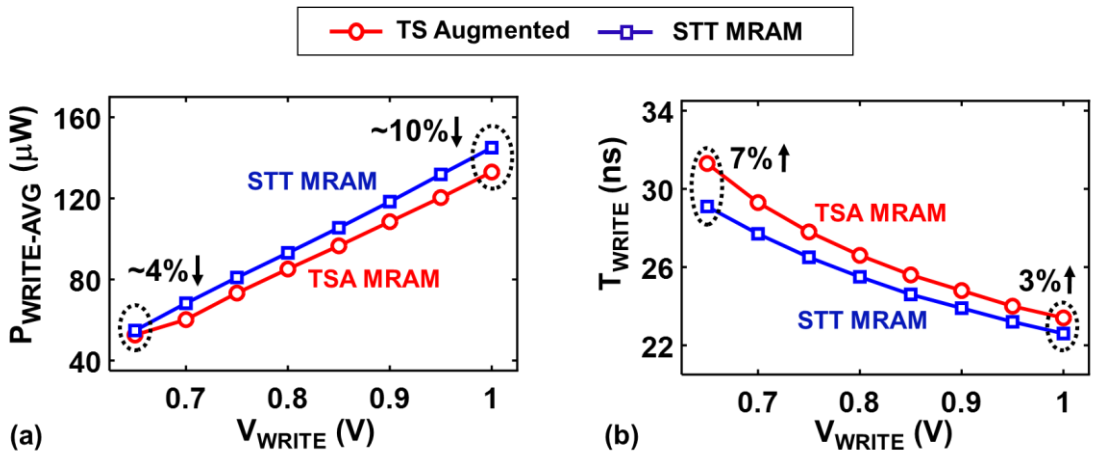


Fig. 2.8 (a) Average write power and (b) write time as functions of V_{WRITE} for STT and TSA MRAMs.

(and hence SM) and RDM without much degradation in write performance. The design technique discussed in this section provides insights on bias selection for a given set of parameters of the TS (Table 2.1). However, the resistance and transition thresholds of the TS can be chosen/tailored to alter the optimum biasing range, which we discuss next.

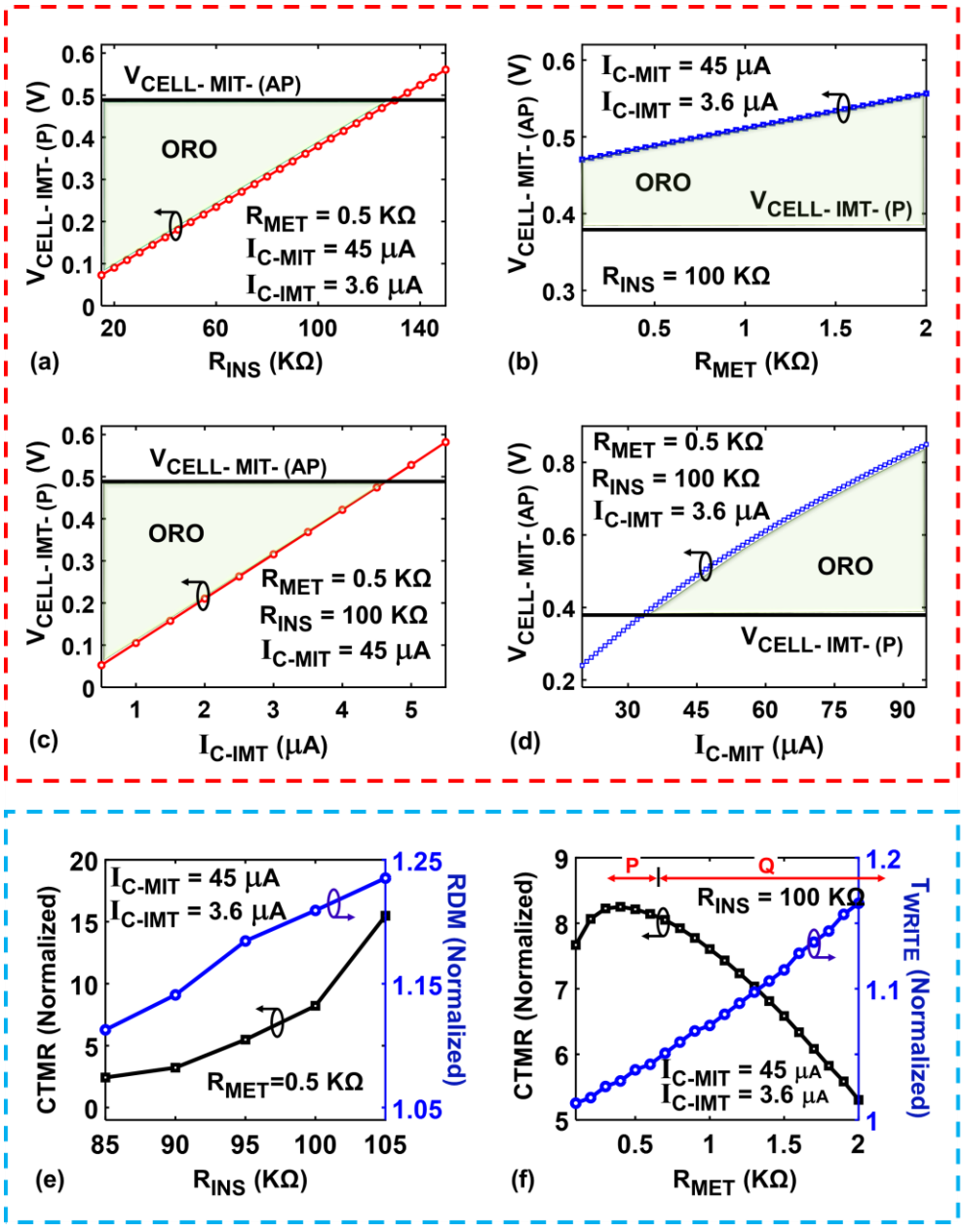


Fig. 2.9 The ORO for TSA MRAM can be tuned utilizing (a) R_{INS} (b) R_{MET} (c) $I_{C\text{-}IMT}$ and (d) $I_{C\text{-}MIT}$. (e) Change in R_{INS} has major impact on CTMR and RDM. (f) R_{MET} primarily shows impact on CTMR and T_{WRITE}.

2.5 Tuning Design Space with TS Parameters

We analyze the effect of four major TS properties ($R_{INS,}$ $R_{MET,}$ $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$) on TSA MRAM operation. While considering the impact of one of these parameters, we keep the others fixed at the nominal values (Table 2.1). That allows us to examine the individual influence of each of these parameters. In Fig. 2.9 (a-d), we plot the $V_{CELL\text{-}IMT\text{-}(P)}$ and $V_{CELL\text{-}MIT\text{-}(AP)}$ as functions of each of the four attributes of the TS. The ORO for TSA MRAM is defined by [$V_{CELL\text{-}MIT\text{-}(AP)}$ -$V_{CELL\text{-}IMT\text{-}(P)}$]. Note, parameters associated with the insulating state of TS (R_{INS} and $I_{C\text{-}IMT}$) affect the values of $V_{CELL\text{-}IMT\text{-}(P)}$ only. On the other hand, R_{MET} and $I_{C\text{-}MIT}$ only have influence on $V_{CELL\text{-}MIT\text{-}(AP).}$ $V_{CELL\text{-}IMT\text{-}(P)}$ increases with R_{INS} and $I_{C\text{-}IMT}$ (Fig. 2.9 (a, c)), as they lead to larger inherent critical voltage for IMT ($V_{C\text{-}IMT} = R_{INS} \times I_{C\text{-}IMT}$). As, $V_{CELL\text{-}MIT\text{-}(AP)}$ stays unchanged, the ORO is larger for lower R_{INS} and $I_{C\text{-}IMT.}$ On the contrary, increase in R_{MET} or $I_{C\text{-}MIT}$ leads to increase in $V_{CELL\text{-}MIT\text{-}(AP)}$ and therefore creates larger ORO (Fig. 2.9 (b, d)). This is because, increase in R_{MET} or $I_{C\text{-}MIT}$ leads to increase in $V_{C\text{-}MIT}$ (= $R_{MET} \times I_{C\text{-}MIT}$) which ultimately results in higher $V_{CELL\text{-}MIT\text{-}(AP).}$ Note, the resistances ($R_{INS,}$ R_{MET}) and transition threshold currents ($I_{C\text{-}IMT,}$ $I_{C\text{-}MIT}$) considered here, can themselves be tuned by changing material parameters (such as resistivity, critical current densities for IMT and MIT transitions) and/or geometry (length, area) of the TS [29], [109]. It is important to note that, the values of $R_{INS,}$ R_{MET} have impact on the read/write performance metrics as well. Fig. 2.9 (e, f) show several performance metrics associated with the TSA MRAM as functions of R_{INS} and R_{MET}. The metrics have been normalized with respect to the corresponding values for standard STT MRAM at V_{READ} =0.35V (*iso*-$\Delta I_{READ\text{-}INIT}$). R_{INS} primarily influences the CTMR (hence SM) and RDM during read operation. Larger R_{INS} leads to higher CTMR and RDM in TSA MRAM (Fig. 2.9 (e)). But we have also shown that larger R_{INS} provides smaller design window (ORO). Having a larger ORO is beneficial to handle the impact of variations. Hence, an optimum value of R_{INS} needs to be chosen to ensure sufficiently large ORO with adequate improvement in CTMR/SM and RDM, depending on the variability in different components.

R_{MET} has direct influence on CTMR and T_{WRITE}. Higher R_{MET} further reduces the average current during write and thereby leads to larger T_{WRITE}. Again, similar to the case of $R_{INS,}$ an optimum value of R_{MET} needs to be chosen to maximize ORO without significantly

increasing the write penalty. The CTMR shows non-linear trend (Fig. 2.9 (f)) with R_{MET} that requires a more involved explanation. Low R_{MET} (with fixed R_{INS}) leads to better CTMR (Fig. 2.9 (f)-zone Q), as the relative difference between LRS and HRS of the cell increases. However, if R_{MET} is too low (< 0.4 KΩ), we see an opposite trend in the curve for CTMR (Fig. 2.9 (f)-zone P). The CTRM gradually degrades as the R_{MET} is decreased below 0.4 KΩ. This trend can be explained considering the switching transient of the TS. For very low R_{MET}, $V_{C\text{-}MIT}$ becomes low as well. That allows the BL to discharge for longer time before the TS with AP MTJ can undergo MIT during read. Hence, the TS with the AP MTJ stays in metallic state for a longer time and meanwhile allows the V_{BL} to keep discharging. By the time TS incurs MIT and stops the discharge, ΔV_{BL} becomes less than what can be achieved for a nominal R_{MET}. This scenario again stresses the need to optimize R_{MET} considering its impact on ORO and performance metrics. To complete the discussion, we note that higher R_{INS} reduces $P_{READ\text{-}AVG}$ by reducing I_{READ} for AP. Similarly, higher R_{MET} lowers both $P_{READ\text{-}AVG}$ and $P_{WRITE\text{-}AVG}$ due to reduction in the respective currents. Moreover, RDM also increases slightly for high R_{MET} as the average I_{READ} for AP reduces.

Table 2.3 Specifications for Monte-Carlo Analysis

Parameter	Mean (μ)	Variation
Standard STT MRAM (3σ Monte Carlo)		
R_P and R_{AP}	4 KΩ, 9 KΩ	σ/μ = ±1.5%
V_{TH}	V_{TH0} (20nm HP)	$\sigma = \pm 40 / \sqrt{N_{FIN}}$ mV
TS Augmented STT MRAM (3σ Monte Carlo)		
R_P and R_{AP}	4 KΩ, 9 KΩ	σ/μ = ±1.5%
V_{TH}	V_{TH0} (20nm HP)	$\sigma = \pm 40 / \sqrt{N_{FIN}}$ mV
L_{TS}	45 nm	3σ = ± 1 nm
$V_{C\text{-}IMT}$, $V_{C\text{-}MIT}$	360 mV, 22.5 mV	σ/μ = ± 7 % , ± 3 %

2.6 Variation Analysis

TSA MRAM has an additional component (the TS) compared to STT MRAM which introduces more sources for variation. Here, we present Monte-Carlo simulation results for standard and TSA MRAMs to compare their relative variation tolerance. We perform 1000

and 500 Monte-Carlo simulations for read and write (respectively). In our analysis, we assume Gaussian distribution for the parameters with 3σ variation. We consider variation in MTJ resistances and the threshold voltage (V_{TH}) of the access transistor for the STT MRAM. For TSA MRAM, we consider additional variation in the length of TS (L_{TS}) and the transition thresholds. The mean (μ) and standard deviation (σ) for all the input distributions have been listed in Table 2.3. Note, distributions for the levels of the MTJ resistance, V_{TH} of the transistor and the switching thresholds of the TS have been taken from the references [110]–[112], respectively. We show results for both *iso*-V_{READ} and *iso*-$\Delta I_{READ\text{-}INIT}$ between STT and TSA MRAMs.

2.6.1 Effect of Variation on Read Performance

Even with additional sources of variation, the TSA MRAM offers larger separation between values of $V_{BL\text{-}P}$ and $V_{BL\text{-}AP}$ (Fig. 2.10 (a, b, c)). The markers in Fig. 2.10 (d, e, f) illustrate the values of $V_{BL\text{-}P}$ and $V_{BL\text{-}AP}$ for both STT and TSA MRAM. It is apparent that, the TSA MRAM achieves ~1.7X larger separation (with 2X lower T_{READ}) between $V_{BL\text{-}P}$ and $V_{BL\text{-}AP}$ compared to STT MRAM. The separation between max($V_{BL\text{-}P}$) and min($V_{BL\text{-}AP}$) is a vital determinant for the reference voltage (V_{REF}) for sensing. V_{REF} is usually chosen mid-way between $V_{BL\text{-}P}$ and $V_{BL\text{-}AP}$ [113]. The overall SM of MRAMs is defined by two parameters - SM_P and SM_{AP}. Here, SM_P is defined as (V_{REF} - $V_{BL\text{-}P}$) and SM_{AP} is defined as ($V_{BL\text{-}AP}$ - V_{REF}). Ideally, for symmetrically chosen V_{REF}, $SM = SM_P = SM_{AP}$. However, due to the effect of variation, distribution of $V_{BL\text{-}P}$ and $V_{BL\text{-}AP}$ yields variations in SM_P and SM_{AP}. Fig. 2.10 (g-j) show the distribution (extracted from Monte-Carlo results) of SM_P and SM_{AP}, for STT and TSA MRAMs. Note, the STT MRAM requires $T_{READ} \approx 9$ ns to generate ~100 mV of ΔV_{BL}. Hence, to extract practical values for SM_P and SM_{AP}, we use $T_{READ} \approx 9$ ns for STT MRAM and $T_{READ} \approx 3$ ns for TSA MRAM. It is clear from Fig. 2.10 (g - j), that the TSA MRAM exhibits higher and more robust SM compared to STT MRAM even with variations. The SM_{AP} of TSA MRAM (Fig. 2.10 (i, j)) shows bimodal distribution. The reason is that, the TS may undergo one or two complete IMT-MIT oscillations during the read operation. The nominal design is made to allow just one oscillation. But, due to variation, it is possible to get two oscillations within the allocated T_{READ}. For the values of T_{IMT} and T_{MIT} considered here (Table 2.1), we never get more than two complete

oscillations. Note, the values of transition times used here are based on projection from the measured data, reported in [86]. These results indicate that TSA MRAM will be less prone to read failure than STT MRAM. In addition, having larger SM_P and SM_{AP} eases the constraints on sense amplifier design. These benefits stem from the tremendous boost in

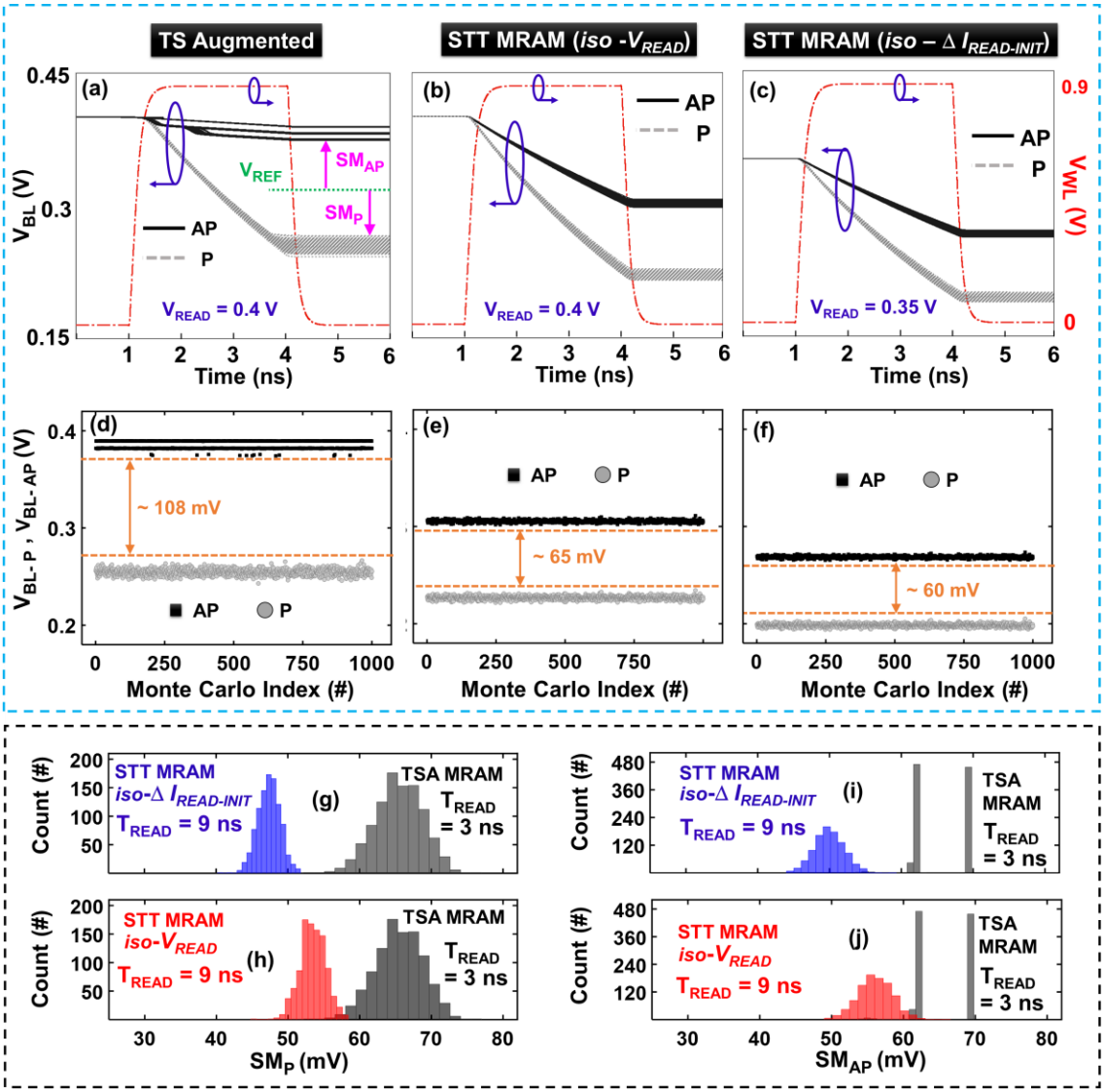


Fig. 2.10 Monte-Carlo simulation results for read operation. (a)–(c) Discharge of BL during read. (d)-(f) Extracted values of $V_{BL\text{-}P}$ and $V_{BL\text{-}AP}$. (g)-(j) Distribution of SM_P and SM_{AP} for both MRAMs. For (g)-(j), T_{READ} for STT MARM is 9 ns, whereas that for TSA MRAM is 3 ns. The STT MRAM requires additional time to achieve practical levels of SM_P and SM_{AP}.

CTMR in TSA MRAM. Recall, all of these advantages are accompanied by lower read time (3 ns) for TSA MRAM compared to STT MRAM (9 ns).

2.6.2 Effect of Variation on Write Performance

We complete our analysis by evaluating the effect of variations on write operation. If $T_{P\rightarrow AP}$ becomes larger than the allocated $T_{WRITE,}$ a write failure occurs. Due to variations, $T_{P\rightarrow AP}$ can become much more than the nominal value. Hence, T_{WRITE} must include enough slack time to accommodate the slower transitioning cases. In Fig. 2.11 (a), we examine this scenario for STT and TSA MRAMs. The worst case for the TSA MRAM is only 5% slower the worst case for the STT MRAM (Fig. 2.11 (a)). That implies, if T_{WRITE} for the standard STT MRAM needs to be extended by ΔT_{WRITE} to tackle the effect of variation, the TSA MRAM will demand an extension of $1.05\times\Delta T_{WRITE.}$ This can be seen more clearly from the scatter plot in Fig. 2.11 (b). Fig. 2.11 (c) shows the distribution of T_{WRITE} corresponding to

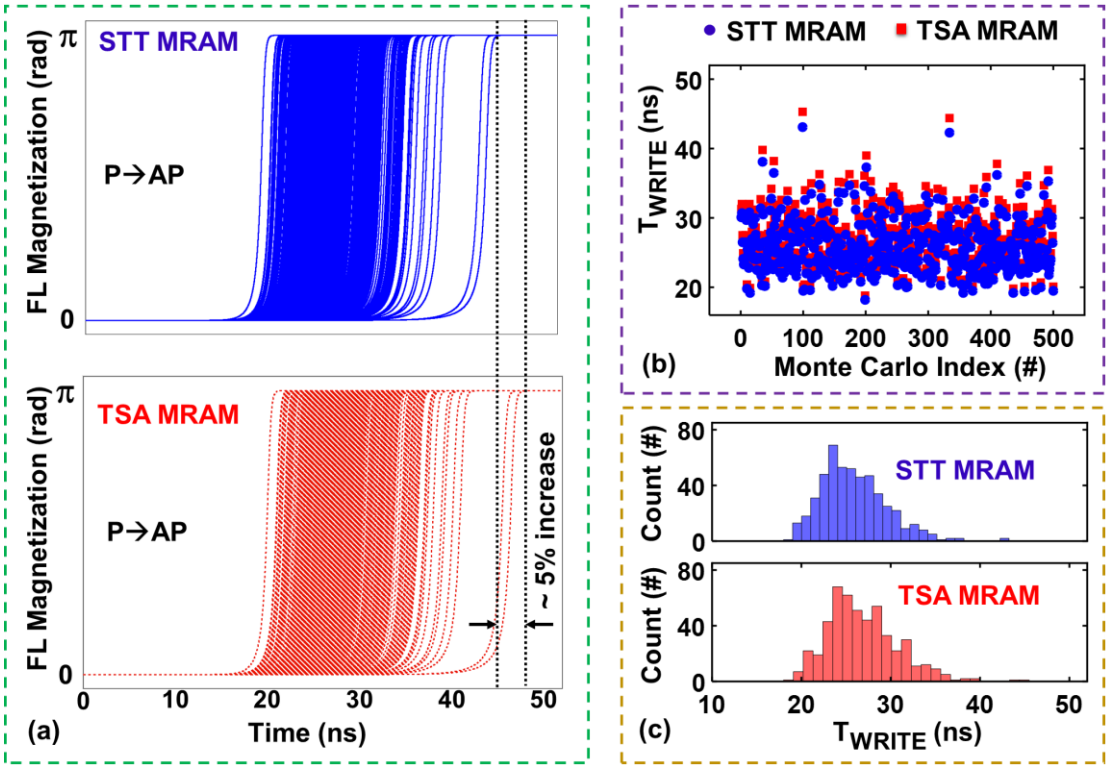


Fig. 2.11 Monte-Carlo simulation waveforms for write operation. (a) P → AP switching of the FL. (b) Values of T_{WRITE} for different combinations incurred during the simulations. (c) Distributions for T_{WRITE}.

both devices showing that the peak value and relative spread of the distribution is similar for both STT MRAM and TSA MRAM. All these results highlight the fact that, TSA MRAM does not lead to significant write penalty, even with additional variations.

2.7 Effect of Transition Time

For all of the analyses reported so far, we have considered constant transition times for IMT and MIT (T_{IMT}, T_{MIT}) as reported in Table 2.1. We have estimated the transition time based on an experimental work reported in [86]. This work reported ~793 ps transition time for VO_2 from experimental measurement with a sample of 100 nm length and 300 nm width. This paper [86] clearly shows a trend of regular reduction of transition time with scaling. It has also been envisioned that, by use of point contacts, the TS can be switched much faster as the filament formation becomes localized [114]. There exist other reports of similar or even smaller transition time for different threshold switches. Transition times for Ag/ HfO_2/Pt and Co/HfO_2 have been predicted to be < 1 ns and < 0.5 ns respectively, based on atomistic simulation [115]. The actual measurements for transition time for these devices are often limited by parasitic capacitance of the measurement instruments, as also mentioned in [86], [115]. The transition time can play an important role in determining the transient performance of the proposed technique. It is important to have T_{IMT}, T_{MIT} << T_{READ} and T_{WRITE}. Fig. 2.12 (a, b) show the effect of transition time on read/write performance of TSA MRAM. It is necessary to have T_{IMT} < ~1.75 ns, to obtain higher ΔV_{BL} from TSA

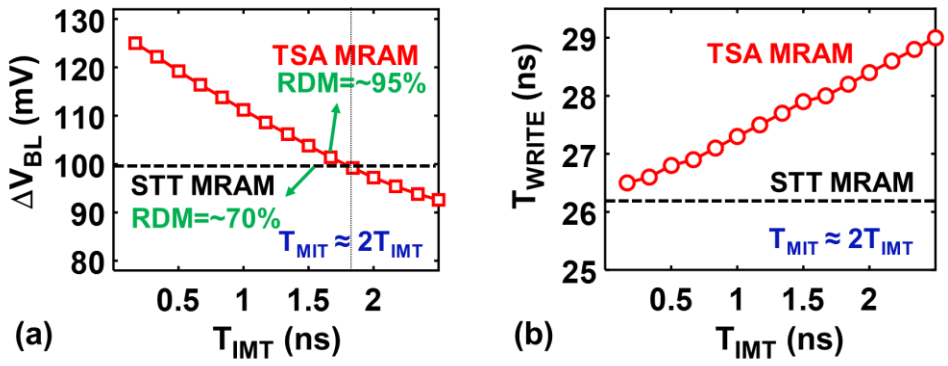


Fig. 2.12 Effect of transition time on (a) read and (b) write performance of TSA MRAM. T_{MIT} has been assumed to be ~double of the corresponding T_{IMT}.

MRAM during read (Fig. 2.12 (a)). Note, even though the benefit in SM reduces for high transition time, the improvement in RDM prevails in TSA MRAM. Penalty in T_{WRITE} reduces with T_{IMT} (Fig. 2.12 (b)).

2.8 Layout Aware Array Design

In this section, we present the layout implications of the proposed technique and discuss the design of memory array. Fig. 2.13 (a, b) shows the single-finger and two-finger layouts of an STT MRAM cell [93], [94], [106]. It is important to note that the layout area of the

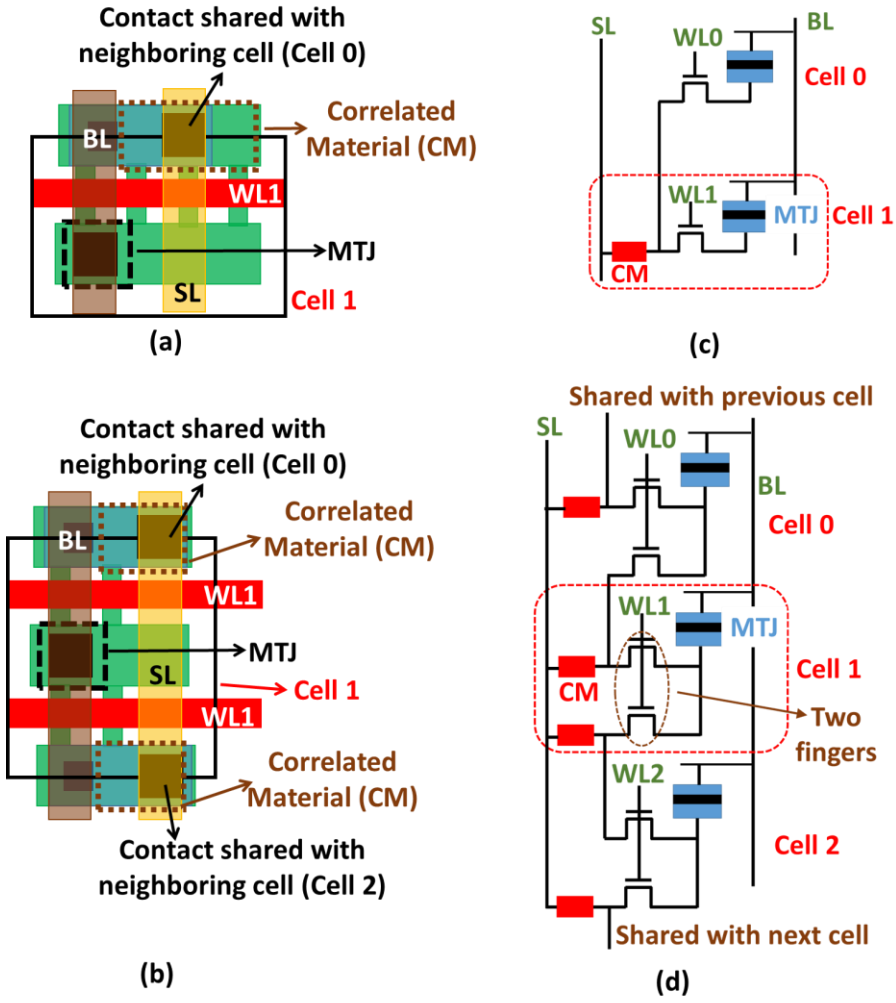


Fig. 2.13 Layout of memory cell with (a) single-finger and (b) two-finger access transistor showing sharing of the contact and the CM. Corresponding schematics are shown in (c) and (d).

cell is minimized by contact sharing. To maintain the contact sharing in a TSA MRAM, it is imperative that the TS is shared amongst neighboring cells in the same column, as shown in Fig. 2.13 (c, d). This sharing has no major effect on the read and write operations since the access transistors of the unaccessed cells are OFF. The only impact of the sharing of the TS is the added capacitance at the shared node. Note that the analysis performed in the previous sections take into account the sharing of the TS and the capacitance of the unaccessed cells. The TS can be fabricated in an upper front-end layer, as has also been proposed in [67], [116], [117]. The dimensions of the TS are such that it easily fits in the cell footprint. Hence, the proposed technique does not incur any area penalty.

2.9 Discussion on Endurance and Thermal Stability

In addition to the design considerations presented so far, we must also consider endurance and thermal stability of the TS. As discussed in chapter 1, the reason for phase transition in these materials can be attributed to diverse physical mechanisms. The endurance of the phase transition is expected to vary for different TS materials. To evaluate and possibly enhance the intrinsic endurance limit for TS materials has been a very important research topic for several years and the research thrust is still ongoing. Ag-filament based TS devices have shown endurance of over 100 million cycles [21] with a selectivity of 10^8 [21]. Rapid thermal processing has proved to be an effective way to enhance endurance of such devices [118], [119]. Reliable operation for over billion (10^9) cycles has been reported for VO_2 [22] and doped chalcogenide [73]. For TaO_x, and Cu-doped HfO_2, an endurance of over 10^{10} cycles have been demonstrated in [120] and [67], respectively. Another threshold switch, named as *field-assisted superlinear threshold selector* (FAST) was demonstrated to have endurance > 10^{11} cycles [121]. Most of these works report having the device functional even after such extensive cycling. Relentless effort is being directed to improve the endurance further. In addition, it is crucial to choose a TS material with sufficiently high thermal stability. Concurrent MRAMs can operate at up to 150^oC [122]. Several TS materials have been reported to be thermally stable even beyond 400^oC [123], [124]. In fact, the thermal stability of some TS materials can be tuned by appropriate doing [125].

2.10 Summary

We proposed and analyzed the augmentation of STT MRAM with electrically driven selective phase transition of TS to enhance the read operation. We provided a comprehensive discussion on necessary design considerations for TS augmented (TSA) MRAMs. We deduced constraints for read and write biasing that yields improved read operation of TSA MRAMs. We explained the dependence of read/write performance metrics on read/write biases and the properties (resistance and critical currents for transitions) of the TS. With proper device-circuit optimization, TSA MRAM showed up to 70% larger sense margin (SM), ~27% higher data stability with ~40% less power for read operation compared to STT MRAM (in nominal condition). We evaluated the impact of variation on TSA MRAM through Monte-Carlo simulations. We reported that, even with variation-induced spread in distribution of bit line voltages, TSA MRAM provided ~1.7X larger voltage differential between P and AP states of the MTJ. For the write operation, the TSA MRAM consumed ~10% less average power and demanded only ~5% more write time extension than the STT MRAM to achieve the same level of variation tolerance. Moreover, the TS can be fabricated in a backend layer within the MRAM cell layout and therefore no area penalty is expected in our design. All of these aspects clearly indicate that the TSA MRAM can be a promising alternative to the conventional STT MRAMs.

3. PHASE TRANSITION MATERIAL AUGMENTED MRAM WITH SEPARATE READ-WRITE PATHS

3.1 Introduction

As discussed in previous chapter, spin-based memories are currently attracting immense interest due to having non-volatility, high endurance and long retention [51], [122]. STT MRAM is the most common version of spin-based memory. However, several challenges and design conflicts still exist in STT MRAM design. Due to having shared read and write paths, it becomes extremely challenging to optimize both of these operations simultaneously in an STT MRAM cell. Several novel design techniques are being actively explored to enhance the read/write operations and to alleviate the design conflicts [79], [126]–[129]. Amongst such techniques, separation of read-write paths with a multi-port memory device has shown an immense promise for independent optimization of the read and write operations [97], [129]. It is possible to augment a PTM in series with the read path of this type of device and further boost the read performance using the technique discussed in the previous chapter. However, separation of the read-write paths brings in another interesting design option. In this chapter, we propose a novel technique to boost the cell tunneling magneto resistance (CTMR) and read stability of multi-port MRAMs by connecting a phase transition material (PTM) in parallel with a magnetic tunnel junction (MTJ) in the read path. Similar to the TSA MRAM technique discussed in chapter 2, this idea also utilizes selective transitions in phase transition materials (PTM). However, in this case, the PTM is augmented in parallel with a magnetic tunnel junction (MTJ) in the read path of a multi-port MRAM. This technique capitalizes the decoupled read and write paths to improve the read performance with absolutely no impact on write operation (unlike the TSA MRAM technique).

3.2 Cell Structure and Simulation Framework

Several propositions for multi-port MRAMs have been reported in literature. Fig. 3.1 (a, b) show two examples of previously proposed topologies of MRAM with separate read/write paths. Both of these designs use magnetic tunnel junction (MTJ) based read. However, the

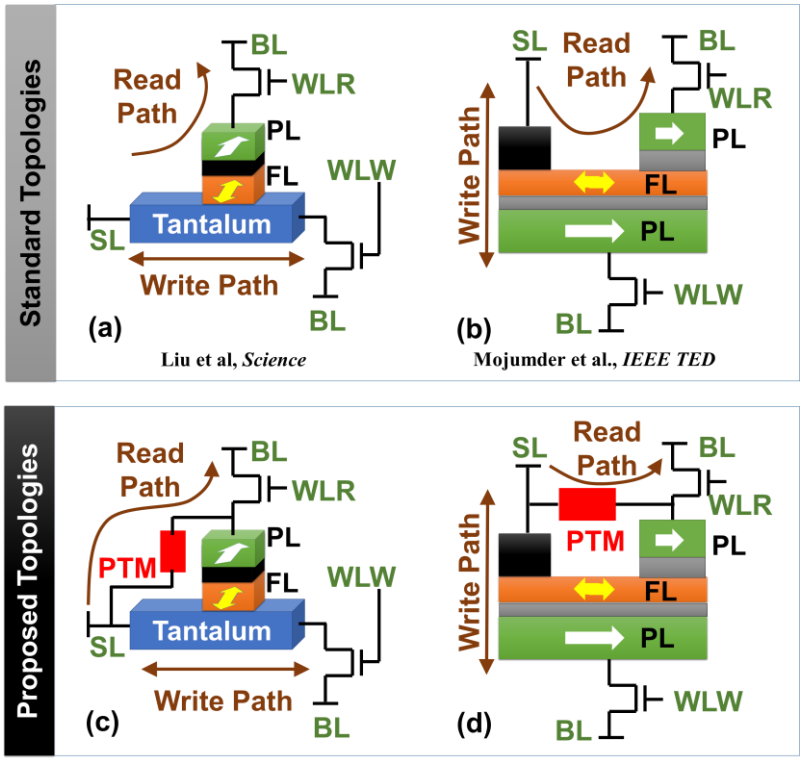


Fig. 3.1 (a) Multi-port MRAM with GSHE based write operation. (b) Multi-port MRAM with magnetic anisotropy based write operation. (c – d) Modified version of designs shown in (a) and (b) which show incorporation of PTM in the read path only.

techniques used for write operation are different. The first design (Fig. 3.1 (a)) uses Giant Spin Hall effect (GSHE) [97] and the second design (Fig. 3.1 (b)) utilizes magnetic anisotropy [129] based write operation. Our proposed technique can be implemented in any of these topologies and for that matter, any cell with separate read-write paths that uses MTJ based read. Fig. 3.1 (c, d) illustrate the modified versions of the designs showed in Fig. 3.1 (a, b). Clearly, the only modification required is the incorporation of PTM in parallel with the MTJ, without altering the write mechanisms.

Fig. 3.2 (a) shows an equivalent circuit for the read port of the MRAMs shown in Fig. 3.1 (c, d). For subsequent discussions, this common read equivalent circuit will be used. The crucial part of the proposed design is the PTM that creates a shunt resistive path along with the resistance of the MTJ. The purpose of augmenting the PTM is to trigger selective

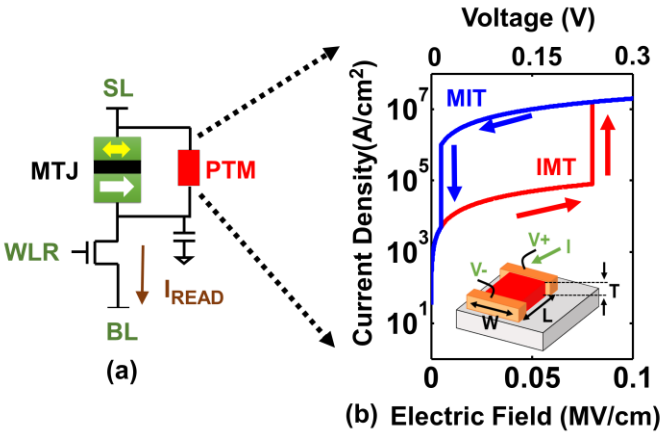


Fig. 3.2 (a) Read equivalent circuit for the proposed multi-port MRAM topology (b) current-voltage (*I-V*) characteristics obtained from the compact model using the experimentally extracted material parameters.

insulator-metal and metal-insulator transitions (IMT and MIT) depending on the stored data in the MTJ. To conceptually illustrate and validate the idea, we employ a simulation-based approach. We use the circuit compatible compact model for PTM (described in chapter 2), physics based model for MTJ [xx] and predictive technology model for the transistor [xx] to simulate the read operation of the proposed MRAM topology. We use experimentally measured current-voltage (*I-V*) characteristics from epitaxial VO_2 (a PTM) film on TiO_2 substrate to calibrate the model for PTM. Fig. 3.2 (b) shows the modeled *I-V* characteristics. The model-fit material parameters and specifications of the simulation framework are listed in Table 3.1.

Table 3.1 Specification of the Simulation Framework and Material Parameters

Simulation Parameters	
Area of MTJ in read path	1257 nm^2
PTM (VO_2) Dimensions [L x W x T]	30nm x 90nm x 35nm
MTJ Oxide Thickness (T_{OX-MTJ})	1.1 nm
Access Transistor Tech., Number of Fins (N_{FIN})	20 nm FinFET, 4
Parameters Extracted from Measured *I-V Characteristics*	
Resistivity of metallic state (ρ_{MET})	$5x10^{-3}$ Ω-cm
Resistivity of insulating state (ρ_{INS})	1 Ω-cm
Critical current density for MIT (J_{C-MIT})	$1x10^6$ A/cm^2
Critical current density for IMT (J_{C-IMT})	$4x10^4$ A/cm^2

Although the concept has certain commonalties to the TSA MRAM technique described in chapter 2, the principle of operation and the implications are somewhat different. We discuss the principle of operation for this new configuration in the next section.

3.3 Principle of Operation

The target of the proposed deign is to operate the PTM in its insulating (metallic) state when the associated MTJ is in parallel (antiparallel) state. This essentially leads to a larger ratio between low and high resistive states of the overall memory cell, as discussed later. Fig. 3.3 conceptually illustrates the proposed steps for read operation in our design. In standard scenario, the read word line (WLR) and bit line (BL) are kept at zero voltage in stand-by mode (before the read begins). So, the initial voltage across the MRAM cell is

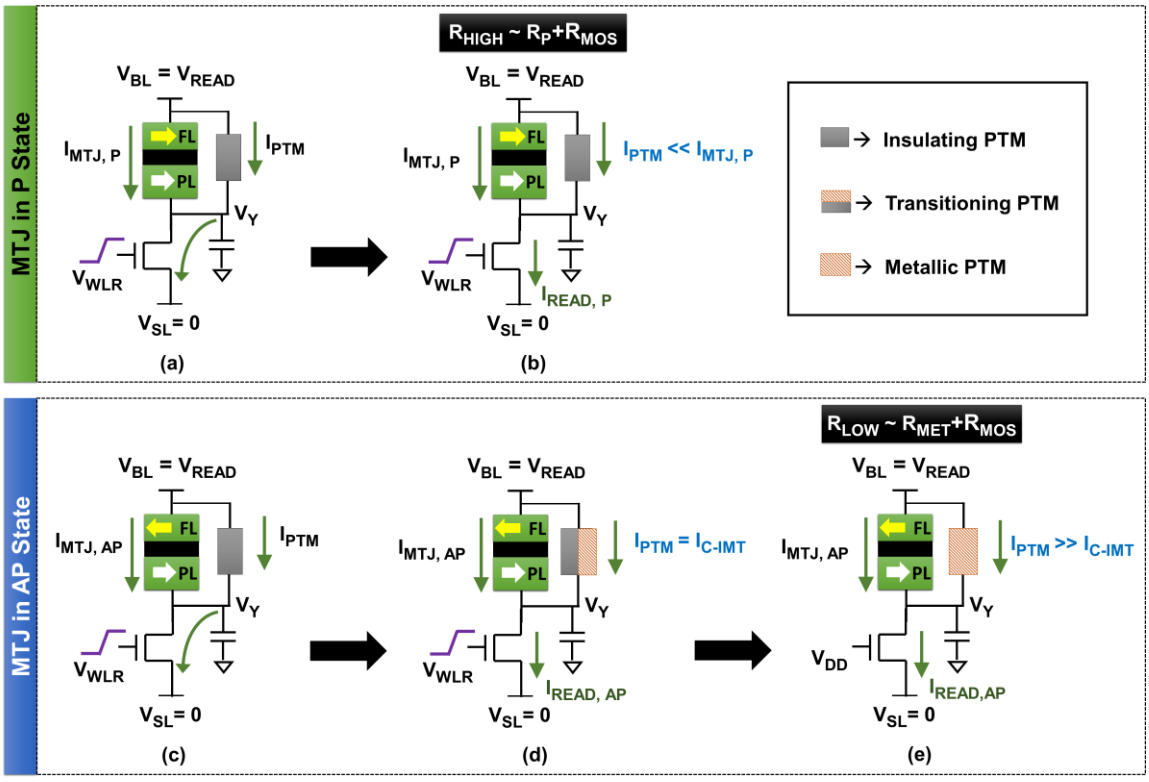


Fig. 3.3 Principle of the read operation for the proposed MRAM utilizing resistance switching of the PTM. Transient steps of read operation for an MTJ with (a-b) parallel magnetization (c-e) antiparallel magnetization.

zero, which keeps the PTM in the insulating phase (irrespective of the state of the MTJ). During read operation, read voltage (V_{READ}) is applied across the cell and the word-line voltage is asserted. That increases the voltage across the MTJ and PTM (V_{MTJ} and V_{PTM}, respectively). With PTM in the insulating phase, V_{PTM} is essentially controlled and determined by the MTJ resistance R_{MTJ} (since $R_{MTJ} << R_{INS}$). When the MTJ is in its low resistance parallel (P) state ($R_{MTJ} = R_P$), V_{PTM} must be less than the critical voltage for IMT ($V_{C\text{-}IMT}$) so that PTM remains in the insulating phase (Fig. 3.3 (a, b)). In this scenario, the equivalent resistance of the parallel network of the MTJ and PTM remains almost equal to that of the standalone MTJ (R_P). In different words, the cell current ($I_{READ,\ P}$) remains unaltered. When the MTJ is in its high resistance AP state ($R_{MTJ} = R_{AP}$), V_{PTM} becomes larger than the former case. If this voltage is designed to exceed the triggering point for IMT ($V_{C\text{-}IMT}$) in the PTM, an insulator-metal transition takes place (Fig. 3.3 (c-d)). Note, the metallic state resistance of the PTM is much smaller than even the MTJ in its high resistance (AP) state (*i.e.* $R_{MET} << R_{AP}$). As a result, the equivalent resistance of the parallel combination of the MTJ and the PTM decreases. Consequently, the total cell resistance also decreases significantly, leading to an increase in the read current ($I_{READ,\ AP}$). With proper design, this level of read current can be high enough to keep the PTM stable in metallic state (Fig. 3.3 (e)) throughout the read operation. Since $R_{MET} << R_{AP}$, the overall resistance of the cell (for the proposed design) for AP state of the MTJ is ~ (R_{MET}+R_{MOS}) and that for the P state is ~ (R_P+R_{MOS}). Here R_{MOS} is the resistance of the access transistor. Since R_{MET} can be much lower than R_P (for PTMs such as VO_2 [30], NbO_2 [83] etc.), we obtain $I_{READ,\ AP} >> I_{READ,\ P}$ in our proposed design. That leads to a boost in the distinguishability of stored data.

In addition to the envisioned benefit in terms of distinguishability, the proposed design also promises a significant improvement in stability of the stored data. The PTM provides a path for current flow in parallel with the MTJ. For an MTJ with AP magnetization, the PTM operates in metallic state and creates a low resistive path for the current flow. Therefore, a dominant proportion of the read current is bypassed through the PTM while reading an MTJ with AP magnetization. Reduction in read current flowing through the MTJ in AP state leads to increase in read disturb margin. Note, for the biasing scenario and

MTJ connection pattern considered here, only AP to P switching is possible. The likelihood of accidental data flipping during read operation is measured and represented in terms of the read disturb margin (RDM) which is defined as 1-($I_{MTJ,\ AP}$ / $I_{C,\ AP\rightarrow P}$). Here, $I_{C,\ AP\rightarrow P}$ denotes the critical current for AP to P transition in the MTJ for a given time. $I_{CMTJ,\ AP}$ is the current flowing through the MTJ in AP state during read operation. So, reduction in the read current for the AP case will suffice to reduce chances of accidental disturb during read.

3.4 Design Methodology

The proposed design can be realized by properly co-designing the MTJ, PTM and the access transistor in the read path of a multi-port MRAM. To establish an appropriate design methodology for the proposed technique, we first analyze the DC response. Fig. 3.4 shows the cell read current (I_{READ}) versus read voltage (V_{READ}) plots for standard and proposed designs. Note, the standard design represents the read portion of the existing multi-port MRAM topologies. The dotted lines in Fig. 3.4 represent cases for standard design and the solid lines represent the proposed design. Following the dotted lines in Fig. 3.4 (a), an increase in cell read current with read voltage can be observed, as expected. The MTJ with P magnetization produces larger read current due to having lower resistance. On the

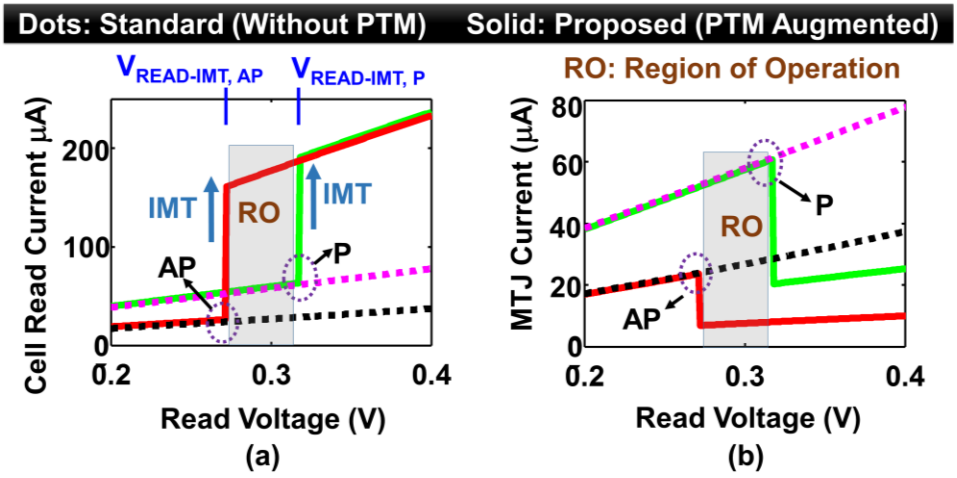


Fig. 3.4 (a) Read current versus read voltage for the standard and proposed designs of multi-port MRAMs. The valid region of operation has been highlighted. (b) Current flow through the MTJ (I_{MTJ}) in the read path. Significant reduction in I_{MTJ} is observed for an MTJ with AP magnetization in the proposed design.

contrary, the solid lines (representing proposed design) in Fig. 3.4 (a) show abrupt increase in current beyond particular read voltages. These abrupt changes are signatures of IMT in the PTM. Note, for MTJs with P and AP magnetization, different levels of read voltage are required to trigger IMT. These critical points have been marked as $V_{READ\text{-}IMT,\,AP}$ and $V_{READ\text{-}IMT,\,P}$ in Fig. 3.4 (a). For low V_{READ}, the PTM operates in the insulating state. In this scenario, V_{PTM} (= V_{MTJ}) is determined by the resistive divider action of R_{MTJ} and R_{MOS} (since, R_{MTJ} << R_{INS}). For P magnetization in the MTJ, V_{MTJ} (= V_{PTM}) becomes lower than that for the AP case. Hence for P magnetization, larger V_{READ} is required to achieve V_{PTM} = $V_{C\text{-}IMT}$. Clearly, within the range of V_{READ} bounded by the two critical values ($V_{READ\text{-}IMT,\,AP}$ and $V_{READ\text{-}IMT,\,P}$), the PTM will remain in insulating state with an MTJ with P magnetization and transition to metallic state in case of AP magnetization. This range of voltage will be referred to as the region of operation (RO = $V_{READ\text{-}IMT,\,AP}$ - $V_{READ\text{-}IMT,\,P}$) for the subsequent discussion.

Any V_{READ} within the RO results in a large increase in I_{READ} in our proposed design, when MTJ is in the AP state (Fig. 3.4 (a)). However, the cell current for the P state remains almost same as the standard case. This leads to larger distinguishability for a current based sense operation. Interestingly, increase in I_{READ} does not lead to higher chances of read disturb in our design (unlike the standard case). The reason is that, for AP case, prime portion of the read current is diverted through the PTM branch (because, R_{MET} << R_{AP}).

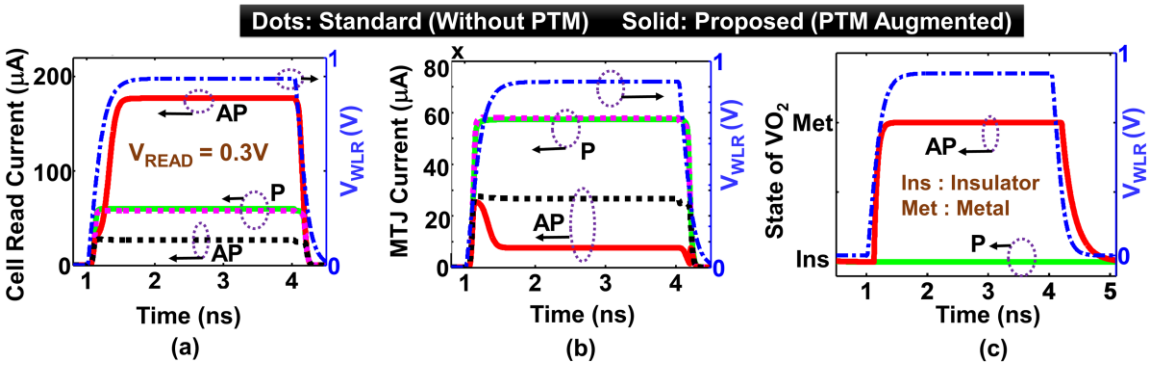


Fig. 3.5 Simulated transient response for the standard and proposed multi-port MRAMs. (a) Total read current through the cell when the WLR is asserted. (b) Current flowing through the MTJ. (c) Evolution of the resistive state of the PTM in the proposed design.

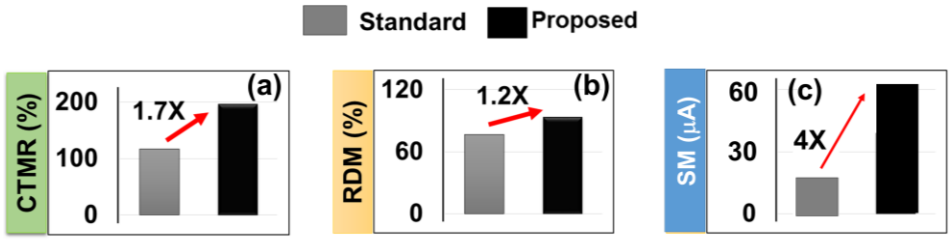


Fig. 3.6 Comparison of the (a) CTMR and (b) RDM (c) SM for the proposed and standard multi-port MRAM designs.

That in fact leads to a much lower current flow through the MTJ in AP state (Fig. 3.4 (b)) and provides better stability of data stored in the MTJ against accidental AP→P switching during read.

3.5 Transient Response

Based on the discussion in the previous section, it is important to choose a V_{READ} from a valid range (RO). To evaluate the feasibility of the proposed idea we simulate the memory cell and obtain the transient response. Fig. 3.5 (a) illustrates the transient response of standard and proposed multi-port MRAM cells. When the read word line (WLR) is asserted, read current starts flowing through. For V_{READ} = 0.3 V (chosen from within the RO shows in Fig. 3.4 (a)), the proposed design shows significantly higher current ratio between low and high resistance states compared with standard design. Note, for our proposed design, overall low resistance state occurs for an MTJ in AP state (unlike standard case). Fig. 3.5 (b) shows the transient current through the MTJ. For standard design, this current is the same as the cell current. In the proposed design, a shunt path with lower resistance exists with the MTJ and the I_{MTJ} for the AP case significantly reduces. The reduction in I_{MTJ} is manifested after the IMT transition occurs in the PTM. Fig. 3.5 (c) shows the evolution of the resistive state of the PTM for the proposed design illustrating that IMT takes place only for the AP state of the MTJ. Fig. 3.6 presents a comparison of the cell Tunneling Magneto Resistance (CTMR) and the RDM for standard and propose designs. Our technique achieves up to 70% boost in CTMR (Fig. 3.6 (a)), 20% increase in the RDM (Fig. 3.6 (b)) and ~4X increase in sense margin (SM) (Fig. 3.6 (c)) compared to a standard topology.

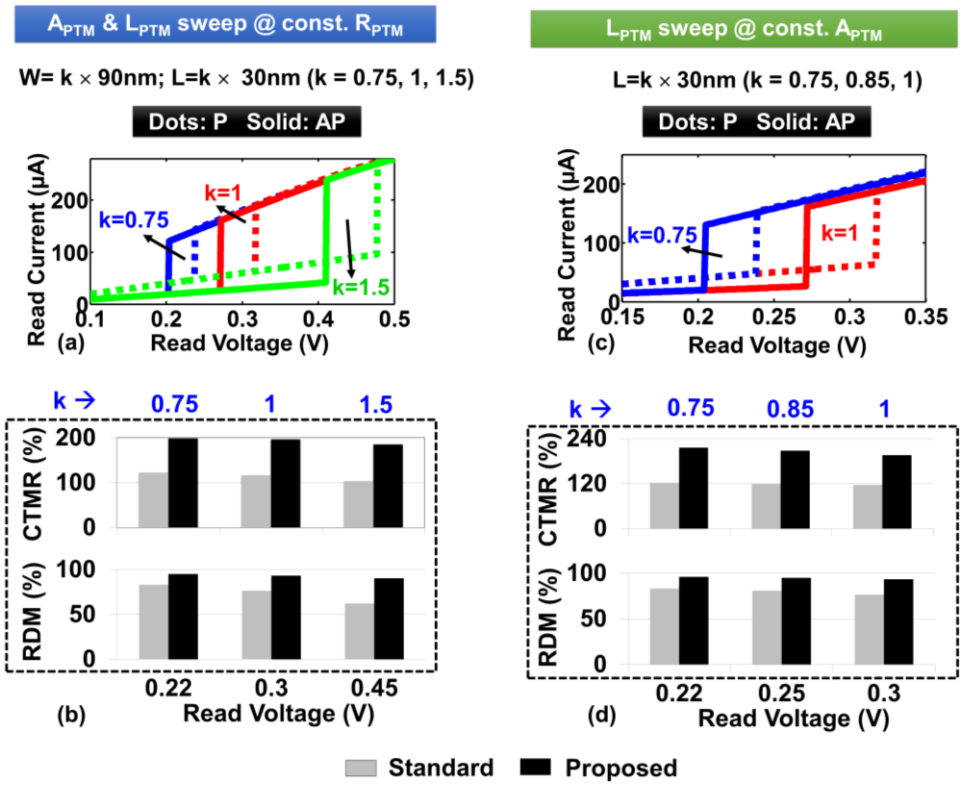


Fig. 3.7 (a) Option A: Tuning the valid region of operation by changing the critical currents of transitions. (b) Performance evaluation for the proposed design for different ROs, set using option A. (c) Option B: Tuning the valid region of operation by changing the resistance of metallic and insulating states. (d) Performance evaluation for the proposed design for different ROs, set using option B.

3.6 Tuning the Region of Operation

As mentioned earlier, the proposed cell needs to be operated within a pre-designed RO for read enhancement. The RO of the proposed design (and therefore the V_{READ}) can be tuned by tailoring the attributes of the PTM. The physical dimensions (area, length) of the PTM is a useful knob for tuning the RO of our design. Two possible approaches for tuning the RO have been demonstrated in Fig. 3.7. The first approach (option A) is to change the area and length of the PTM proportionally (Fig. 3.7 (a)). This leads to change in the critical currents of transition ($I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$), without altering the resistances in metallic and insulating states. We analyzed the proposed design by shifting the RO using option A and selected V_{READ} from within the corresponding RO. The analysis shows ~50-80 %

improvement in CTMR and ~20-40 % improvement in RDM (over standard design) for all of these selected V_{READ} values (Fig. 3.7 (b)). The second approach (option B) is to alter the length of the PTM (without changing the area). This approach effectively changes the resistance of the metallic and insulating states of the PTM (Fig. 3.7 (c)). We also used option B to selectively tune the RO and select appropriate V_{READ} values therefrom. For all of those chosen $V_{READ,}$ the proposed design showed ~70-90 % improvement in CTMR and ~15-30% improvement in RDM over the standard design (Fig. 3.7 (d)).

3.7 Effect of Design Parameters

Read path in multi-port MRAMs may be optimized by increasing the number of fins (N_{FIN}) of the access FinFET or MgO thickness in the MTJ ($T_{OX,MTJ}$) [129]. Fig. 3.8 shows the comparison of CTMR and RDM for different N_{FIN} and $T_{OX,MTJ}$. Compared to the baseline,

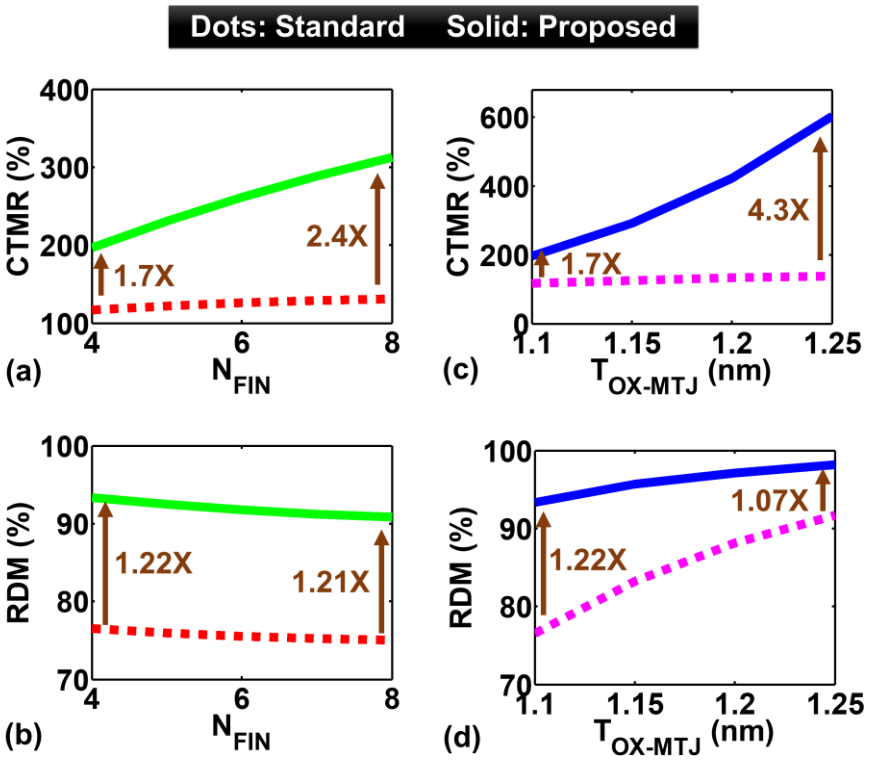


Fig. 3.8 CTMR and RDM for (a, b) different fin number of the read access transistor (N_{FIN}) with $T_{OX\text{-}MTJ}$ = 1.1 nm and (c, d) for different MgO thickness in the MTJ ($T_{OX\text{-}MTJ}$) with four fins in the access transistor.

the effect of increasing N_{FIN} in boosting CTMR is more pronounced in the proposed cell (Fig. 3.8 (a)). In the standard design, MTJ resistance is more influential than the transistor resistance during read operation (by design). In the proposed design, the overall resistance of the cell becomes much smaller (than standard design) for an MTJ in AP state. Therefore, the resistance of the access transistor renders more influence in determining the read current. As a result, for larger N_{FIN} (therefore lower resistance of the transistor), the proposed design obtains even more improvement in CTMR. On a different note, for larger values of $T_{OX\text{-}MTJ}$ the proposed design shows significantly more improvement over the standard design (Fig. 3.8 (c)). Higher value of $T_{OX\text{-}MTJ}$ leads to increase in both R_{AP} and R_P in the standard design. Therefore, no significant change is observed in the relative difference of read current (and hence CTMR) for standard design. However, the CTMR of the proposed design is controlled by the resistance difference between R_P and $R_{MET.}$ The latter remains insensitive to $T_{OX\text{-}MTJ,}$ while the former changes. So, the relative difference between high and low memory states becomes more evident with larger $T_{OX\text{-}MTJ}$ in proposed design. N_{FIN} and $T_{OX\text{-}MTJ}$ have negligible effects on the RDM of the proposed design (Fig. 3.8 (b, d)). The proposed technique achieves boost in RDM and CTMR across the entire range of N_{FIN} and $T_{OX,MTJ}$ as shown in Fig. 3.8.

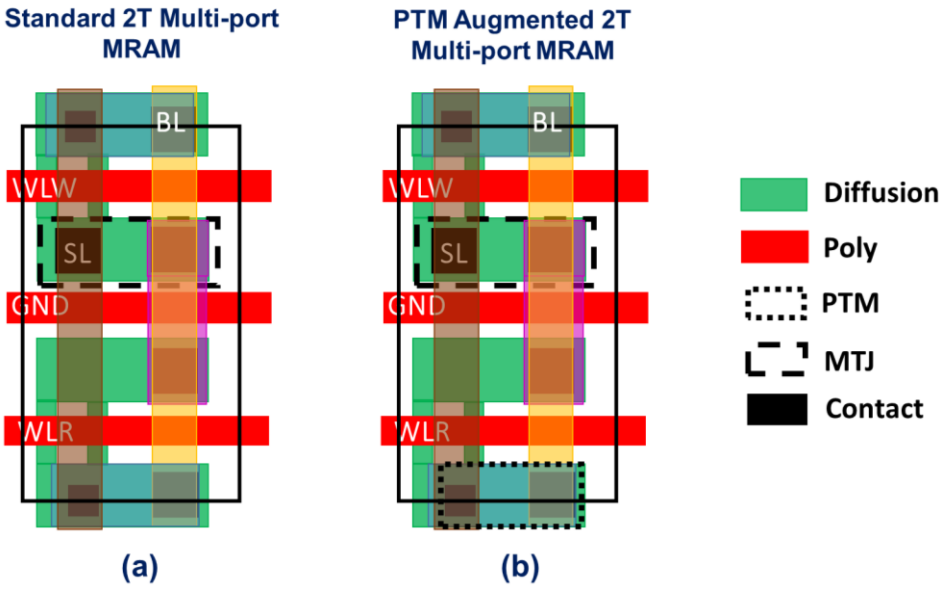


Fig. 3.9 Layout of (a) standard multi-port MRAM and (b) PTM augmented proposed multi-port MRAM.

3.8 Area Implications

As discussed above, the proposed design offers major improvements in performance metrics. However, it is important to evaluate the impact of introducing the additional component (PTM) on the cell area and overall integration density of the array. Fig. 3.9 shows the layouts for standard and proposed 2T multi-port MRAMs. The only difference between the layouts shown in Fig. 3.9 (a) and Fig. 3.9 (b) is the incorporation of the PTM in the latter. Clearly, both of these layouts have the same unit cell area. The PTM is back-end of the line (BEOL) compatible [67], [116] and can be placed in a different layer within the footprint of the regular layout. For both of the designs (standard and proposed), the access transistor is the bottleneck for area. Therefore, incorporation of the PTM does not lead to any additional increase in cell area.

3.9 Summary

We proposed a technique based on connecting PTM in parallel with the MTJ in the read path of multi-port MRAMs. Utilizing insulator-metal transitions in PTM, the proposed cell achieved 1.7X to 4.3X improvement in cell TMR (CTMR) along with 7% to 22% higher read disturb margin compared to a standard cell. Due to the separation of read-write paths in multi-port MRAMs, the PTM has no effect on the write operation. The proposed idea is not limited to any specific material and its benefits may be further enhanced by exploring suitable PTMs [29], [109] or by tuning the physical properties (*e.g.* resistivities, critical currents and thermal stability) of a given PTM by applying strain [75] or using doping [130]. To ensure compatibility with the cutting-edge MRAM technology, it is necessary to choose a PTM with high endurance and thermal stability.

4. ANALYSIS OF PHASE TRANSITION MATERIAL BASED SELECTORS FOR CROSS-POINT ARRAY

4.1 Introduction

In the previous two chapters, we proposed and explored unique applications of PTMs in the design of read optimized MRAMs. We explored the possibility of using selective transitions in PTMs to enhance the performance of spin based memory devices. This chapter focuses on a different avenue of application for PTM, targeted towards a different kind of memory array architecture applicable for generic non-volatile memory technologies. As discussed before, non-volatile memory design for on-chip applications has gained an immense attention in the recent past with a growing demand for battery-powered mobile systems operating under a tight power budget [131]–[133]. A considerable research effort is directed towards the exploration of various non-volatile memory technologies such as spin-transfer torque magnetic RAMs (STT MRAMs) [51], phase change RAMs (PCRAMs) [35] and resistive RAMs (ReRAMs) [31]. However, up until now, no single memory technology has exhibited all the desired attributes due to some limitation or the other. While the design solutions for each memory technology target the respective issues, a common goal for each involves enhancing the integration density. This enables the implementation of the memory in a smaller area, leading to lower bit-line and word-line parasitics and hence, lower power and improved performance. Alternatively, caches with larger data capacity may be designed in the same area, which lowers the miss rate and may offer higher throughput [134]. Therefore, techniques to reduce the layout footprint of the non-volatile memories assume critical importance. Amongst such approaches, cross-point architectures have shown an immense potential [109], [135]–[137].

A cross-point architecture achieves the reduction in the cell footprint by averting the use of the access transistor. The memory cell is sandwiched between two orthogonally running metal lines known as bit-lines (BL) and word-lines (WL). In order to access a sub-set of the array selectively, proper biasing of BL/WL is required to ensure that the unaccessed cells do not hamper the read/write operations and that the data in the unaccessed cells remain stable. Such design concerns stem from the sneak current paths due to cross-point

connections between the cells in the array, which, besides reducing the robustness, increase the power consumption [109], [136], [138]. This issue is typically addressed either by employing a memory device with highly non-linear current-voltage (*I-V*) characteristics [139] or by designing the memory cell with a two terminal non-linear selector in series with a memory element [109], [136], [140]. In typical non-volatile memory technologies, the non-linearity in the *I-V* characteristics is not sufficient, especially for large arrays, which necessitates the use of the selector devices.

The choice of the selector material is critical for robust energy efficient operation of the cross-point arrays. A selector must exhibit a highly non-linear electrical behavior [136]. This enables the reduction of the sneak current paths in the unaccessed cells while obtaining sufficient current in the accessed cells to meet the target performance. To achieve this, the bit-line/word-line biases are chosen so that (a) the accessed cells have higher voltage compared to the unaccessed cells and (b) the selector in the unaccessed cell exhibits a considerably large resistance compared to that in the accessed cells by virtue of the non-linear *I-V* characteristics. As may be expected, the choice of the selector is tightly coupled with the read/write voltages, which, in turn, are strongly dependent on the memory technology. In other words, the selector must be co-designed with the memory element taking into account the architecture needs. To that effect, several candidates for selectors are being explored [67], [141]–[143].

To commence with a more familiar entity, Si p-n junction diodes have high ON-state current density (25 MA/cm^2) and large ON-OFF ratio (~10^8) [144]. But, they can only support memories with unipolar write operations. Ovonic threshold switching devices are also promising candidates as selectors [142]. The overhead of these devices include high switching threshold and large delay during transition. Insulator-metal transitioning materials (*e.g.* VO_2) are garnering attention as bidirectional selectors [22] due to very high non-linearity. However, while some known materials (such as NbO_2 [145]) exhibit insufficient ON-OFF ratio (*i.e.* ratio between the resistance of their metallic and insulating state), the others may have issues like thermal stability. A recent addition to the family of selector devices is the threshold vacuum switch [141]. These type of devices have

endurance of over 10^8 cycles [141]. But, their large-scale fabrication is quite challenging as they demand ultra-narrow vacuum gaps. Recently, a novel device named field assisted super linear threshold selector (FAST) has been reported [146]. While the ON-OFF ratio of this device is promising, whether or not it exhibits sufficient hysteresis needs to be explored. Keeping in mind, all these pros and cons of diverse selectors, we emphasize on the need for systematic analysis of selector device characteristics and their array implications. In this chapter, we analyze the feasibility of using phase transition materials as selectors in a cross-point architecture. The abruptness of these transitions and orders of magnitude difference in the resistivities of the metallic and insulating phases make the PTMs highly suitable for selector applications. However, non-linearity is a necessary but not sufficient condition for proper operation of a cross-point array. The analysis presented in this chapter explores various aspects of cross point memory design involving PTM based selectors.

In this work, we perform a feasibility analysis of insulator-metal transitioning oxides (subsequently referred to as functional oxides) for applications as selectors in a cross-point architecture. Such materials (examples: vanadium di oxide (VO_2), copper doped hafnium oxide (Cu doped HfO_2), niobium di-oxide (NbO_2)) exhibit electro-thermally driven and abrupt insulator-to-metal and metal-to-insulator transitions (IMT and MIT respectively). The abruptness of these transitions and orders of magnitude difference in the resistivities of the metallic and insulating phases make them highly suitable for selector applications.

4.2 Basic Description of a Cross-Point Array

This section covers the basics of cross-point architectures and the role of PTM selectors to enable energy efficient and robust array operation. We also define the design parameters and metrics that are used in the rest of this chapter. Fig. 4.1 shows the array organization of a cross-point memory. The cell (memory element in series with the selector) has two terminals connected to a bit-line (BL) and word-line (WL). BLs and WLs are shared amongst cells belonging to the same column and row, respectively (Fig. 4.1 (a)). The memory bits that belong to the same word may be implemented in separate blocks (Fig. 4.1 (b)) [147], [148] or in the same block (Fig. 4.1 (c)) [149]. These two architectures will

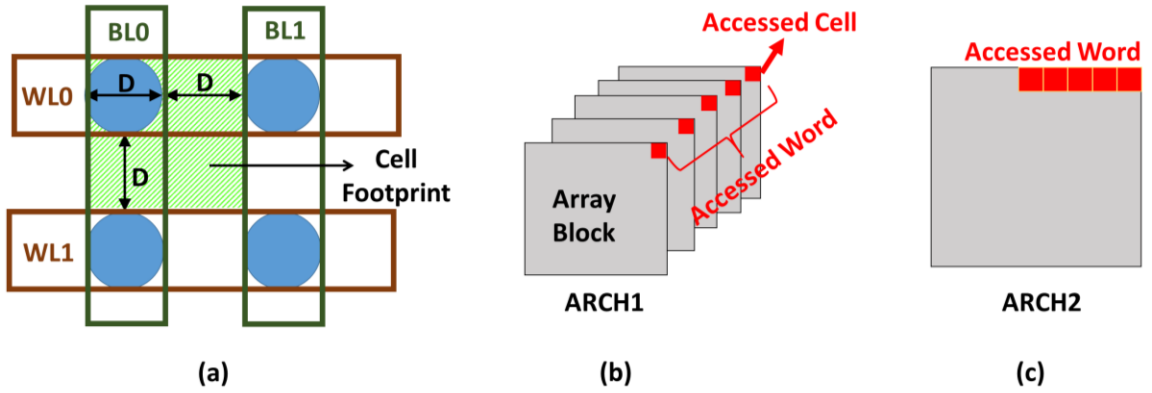


Fig. 4.1 (a) Layout (top view) of a 2×2 cross-point array. Cross-point architectures with bits of the accessed word in (b) separate blocks and (c) in the same block.

be referred to as ARCH1 and ARCH2, respectively. ARCH1 allows a single cycle write operation. However, the number of blocks is constrained to be greater than or equal to the number of bits in a word. This may not be optimal from the perspective of integration density.

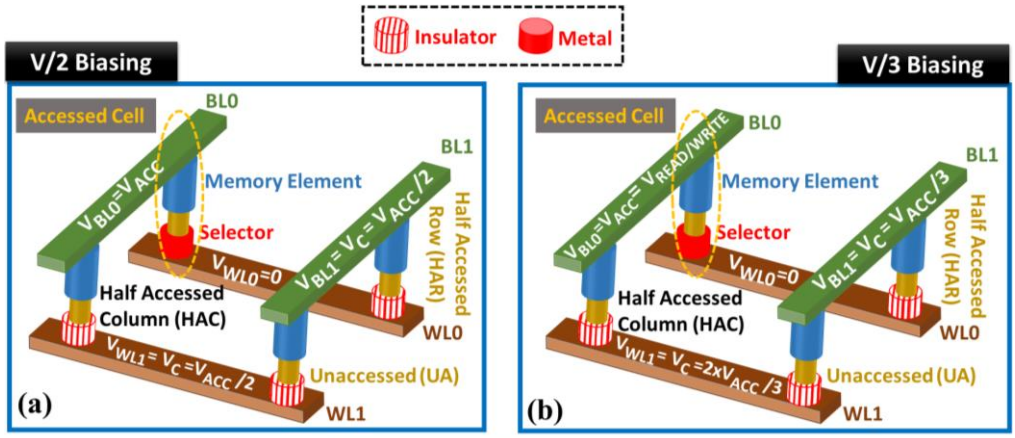
To elaborate on this point, let us consider a fixed memory size. Increasing the number of blocks tends to lower the size of the write drivers for each block, because of the decrease in the block size and the consequent reduction in the word-line and bit-line capacitances. However, at the same time, the number of peripheral circuits increase as separate peripheral circuits may be required for each block. The optimal number of blocks depends on the relative contributions of each factor discussed above on the overall area of the macro, as well as on the power-performance targets. Typically, for standard architectures, a hybrid of ARCH1 and ARCH2 may be used [150]. However, in cross-point architectures, an additional feature is that, ARCH1 offers single cycle write operation while ARCH2 requires two cycles for write. Moreover, the voltage drop across the WL and BL is typically larger in ARCH2 because multiple cells in the block sink the current at the same time. Hence, the architectural optimizations may prefer ARCH1 when performance is the key target. On the other hand, ARCH2 or hybrid architectures may be preferred for optimal number of blocks, leading to a balance between power, performance and area. The choice

between the two architectures is determined by the system-level requirements. In this work, we focus on ARCH1 to convey the key points, unless stated otherwise.

In either of these cases, the heart of the block organization is the cross-point nature of the connections between the cells, which offers significant area advantage over standard architectures. However, these connections lead to unwanted sneak current in the unaccessed cells, which needs to be minimized for low power robust array operation. To achieve this, it is critical to choose the voltage biasing of the bit-lines and word-lines properly in conjunction with appropriate selector design. We discuss that in the next section.

4.3 Biasing Schemes for Cross-Point Array

The two most common biasing schemes used in cross-point arrays, known as the V/2 and V/3 schemes, are shown in Fig. 4.2 (a, b). The bit-lines (BL) of the accessed cells (ACC) are biased at the read or write voltage (V_{READ} or V_{WRITE}) and their word-lines (WL) are



Cell Type	Voltage across Cell	
	$V/2$ Biasing	$V/3$ Biasing
Accessed	V_{ACC}	V_{ACC}
UA	0	$V_{ACC}/3$
HAR	$V_{ACC}/2$	$V_{ACC}/3$
HAC	$V_{ACC}/2$	$V_{ACC}/3$

Fig. 4.2 (a) A portion (2×2) of cross-point array illustrating (a) V/2 and (b) V/3 biasing schemes. The voltage levels across four types of cells in the array have been tabulated.

driven to ground. Note that for memory technologies requiring bi-directional write, bi-polar write voltage across the cell is required, which may be achieved by applying V_{WRITE} on WL and zero voltage on BL. In the V/2 scheme [137] (Fig. 4.2 (b)), the cells that belong to the same column as the accessed cells (also known as half-accessed column or HAC cells) have WL biased at $^1/_2 V_{READ\ /\ WRITE}$. Similarly, for the cells belonging to the same row as the accessed cells (half-accessed row or HAR cells), BL is biased at $^1/_2 V_{READ\ /\ WRITE}$. Thus, the half-accessed cells have half the voltage across them compared to the accessed cells. Cells that do not share the rows or columns with the accessed cell (marked as unaccessed cells or UA in Fig. 4.2 (a, b)) have zero voltage across them, because of which, no sneak current flows in UA cells. However, the current in the half-accessed cells need to be minimized, which is achieved through proper co-optimization of the selector, memory element and read/write bias (discussed later). As a result, the V/2 biasing introduces design constraints that may be difficult to meet for some selectors. Moreover, V/2 scheme may require a large write drivers, which leads to several layout challenges. In order to relax the design constraints and mitigate the layout issues, V/3 biasing is a promising alternative [149]. In this scheme (Fig. 4.2 (b)), WL of the HAC cells and BL of the HAR cells are biased at $^2/_3 V_{READ\ /\ WRITE}$ and $^1/_3 V_{READ\ /\ WRITE}$, respectively. Lower voltage across the half-accessed cells makes it easier to ensure the selector operation at the desired bias point to reduce the sneak current through the HAC/HAR cells. However, the UA cells now have a non-zero voltage across them (=V/3), that increases the overall leakage current. The choice between the V/2 and V/3 schemes strongly depends on the selector characteristics that

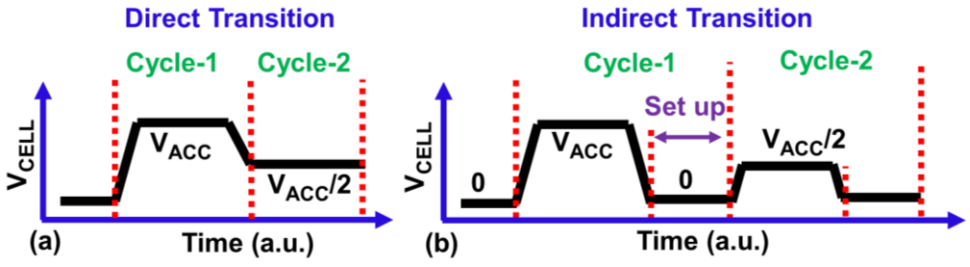


Fig. 4.3 Bit-line voltage of a cell (Cell A) transitioning from the accessed (ACC) mode to the half accessed row (HAR) mode for V/2 biasing showing - (a) direct transitioning scheme and (b) indirect transitioning scheme with a setup period in between the two consecutive access cycles.

determine the feasible operation space. The former scheme is preferable to minimize sneak current paths. On the other hand, the latter technique expands the design space offering more options for read/write voltages to optimize the performance and robustness (presented later).

Another important aspect of a cross-point architecture is the transition strategy between consecutive read/write operations. We discuss two possibilities as follow:

(i) The read/write voltages in cycle 1 are kept constant for the entire cycle and changed at the beginning of cycle 2. In this chapter, this will be subsequently referred to as the direct transition (Fig. 4.3 (a))

(j) A setup period is used in between the two read/write accesses. Operations such as decoding, sense amplification and other setup functions are performed before biasing WL and BL of the array [151]. This will be referred to as the indirect transition (Fig. 4.3 (b)).

Note, during the setup operation, all the WLs and BLs are biased at zero voltage to save power. While the former technique averts the additional delay penalty due to the setup

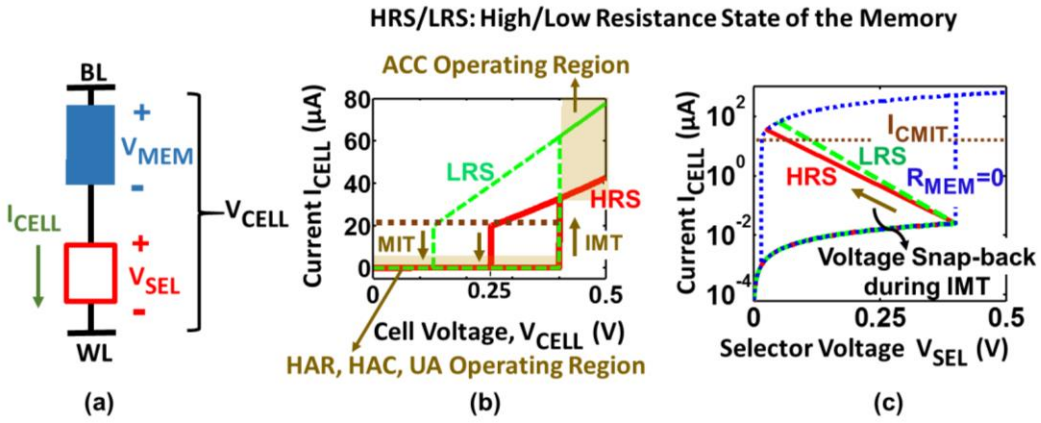


Fig. 4.4 (a) Cell schematic showing voltage drop across the memory element (V_{MEM}), selector (V_{SEL}) and the cell ($V_{CELL} = V_{MEM} + V_{SEL}$) with current-voltage characteristics of (b) a cell showing operating regions of accessed (ACC), half-accessed (HAR, HAC) and unaccessed (UA) cells and (c) selector (in series with the memory element) showing voltage snap-back due to IMT.

operation, it introduces additional design constraints for the selector (described later). On the other hand, the latter scheme can be useful to relax the selector requirements at the cost of performance.

4.4 Design Constraints in a Cross-Point Array

The minimization of the sneak current requires that the selector devices in half-accessed or unaccessed cells with cell voltage ~ $^1/_n V_{READ/WRITE}$) operate in the insulating phase. Here, n=2 for the V/2 scheme and n=3 for the V/3 scheme (Fig. 4.2 (a, b)). Further, to minimize the impact of the selector resistance on the power-performance of the memory array, selector devices belonging to the accessed cells (cell voltage ~ $V_{READ/WRITE}$) must operate in the metallic phase. As $V_{WRITE} > V_{READ}$, the aforementioned requirements can be translated to the following design constraints:

$$\frac{1}{n}|V_{WRITE}| < V_{C-IMT} < V_{READ} \tag{4.1-a}$$

$$\frac{1}{n}|V_{WRITE}| < \rho_{INS} J_{C-IMT} L < V_{READ} \tag{4.1-b}$$

$$J_{C-MIT} < I_{M0}/A \tag{4.2-a}$$

$$J_{C-MIT} < \frac{V_{READ}}{\rho_{MET} L + RA_{M0} + RA_{EFF,W}} \tag{4.2-b}$$

Here, L is the length of the selector device, A is the cross sectional area of the memory element and the selector (assumed to be equal for both to maximize the integration density), I_{M0} is the cell current when the memory is in high resistance state, RA_{M0} is the resistance-area product of the memory in its high resistance state and $RA_{EFF,W}$ is the effective resistance-area associated with BL and WL (discussed in detail later). $|V_{WRITE}|$ in (4.1) corresponds to larger of the two voltages required for 'Write 0' and 'Write 1' operations. Equation (4.1) assumes that the selector resistance in the insulating state is the dominant component of the cell resistance. This is typically a requirement to ensure that the bit-line leakage (which is a function of the parallel resistances of the HAC cells) does not sully the read current. Thus, the selector resistance in the insulating state must be much greater than number of HAC cells in a column times the memory resistance in its high resistance state.

Hence, in a cell with selector in the insulating state, almost all the voltage drop occurs across the selector, due to which the voltage drop across the memory element and the interconnect have been neglected in equation (4.1). Thus, for the unaccessed and half-accessed cells (with cell voltage (V_{CELL}) ~ selector voltage (V_{SEL}) ~ $^1/_n V_{READ/WRITE} < V_{C\text{-}IMT}$), the selector remains in the insulating phase (Fig. 4.4 (a, b)). In the accessed cells, the selector initially operates in the insulating phase. With $V_{CELL} \sim V_{SEL} \sim V_{READ/WRITE} > V_{C\text{-}IMT}$), the selector makes a transition from the insulator to the metallic phase as the BL/WL voltages are applied. As the selector undergoes IMT, it exhibits a voltage snap-back (Fig. 4.4 (c)) due to an abrupt change in its resistance. It is important to note that in order to capture the voltage snap-back, the resistances of all the components (selector, memory and BL/WL interconnect) are considered in (4.2) since they may all be comparable. The snap-back is larger if the resistance of the memory element (R_{MEM}) is higher. Equation (4.2) must be satisfied so that the selector of the accessed cell continues to operate in the metallic phase after voltage snap-back. If this condition is met for the read operation of the high resistance state of the memory, it is easy to deduce that the constraint is also satisfied for the read operation of the low resistance state of the memory and the write operation. It may be noted from Fig. 4.4 (c) that, anti-clockwise hysteresis ($V_{CIMT} > V_{CMIT}$) is necessary in the *I*-*V* characteristics of the PTM to satisfy (4.2).

Another design constraint stems for the direct transitioning scheme between consecutive read/write operations (see Fig. 4.3). To understand this, let us consider a cell (cell A –Fig. 4.3) accessed in the first cycle following which, another cell is accessed in the second cycle. Thus, cell A transitions from the accessed mode to either the HAR, HAC or UA modes (see Fig. 4.2), depending on which cell is accessed in the second cycle. Now, for direct transitioning scheme, it is essential that the selector of cell-A transitions from metallic state to the insulating state as the cell voltage reduces from $V_{READ\,/\,WRITE}$ to $^1/_n V_{READ\,/\,WRITE}$. We can represent this constraint with the following equation.

$$J_{C-MIT} > \frac{^1/_n |V_{WRITE}|}{\rho_{MET} L + R A_{M1}} \qquad (4.2\text{-c})$$

Equation (4.2-c) essentially suggests that the cell A with voltage = $^1/_n V_{WRITE}$ and the initial

selector phase being metallic, must have current density less than $J_{C\text{-}MIT}$ to be able to transition into the insulating state. Here, RA_{M1} is the resistance-area product of the memory in its low resistance state. It is easy to deduce that if (4.2-c) is satisfied (i.e. for low resistance state of the memory during write), the design constraint will automatically be met for the case when the memory is in the high resistance state as well as for the read operation. Note, V_{WRITE} in general could be different for 'Write 1' and 'Write 0' operations. In (4.2-c), it corresponds to the larger of the two in magnitude. Moreover, the voltage drop across WL/BL interconnects is not considered in (4.2-c) to account for the worst case scenario. Note, in the V/2 scheme, this constraint does not exist if cell A operates in the UA mode in the second cycle, since its cell voltage is reduced to zero (Fig. 4.2 (b)). Nevertheless, the worst case corresponds to the case when cell A transitions to the HAC or HAR modes. In this case, this constraint becomes important to consider. For V/3 scheme, this requirement must be met for all cases (i.e. cell A transitioning to UA, HAR or HAC modes). It is also noteworthy that if the indirect transitioning scheme (Fig. 4.3 (b)) is adopted, equation (4.2-c) is not required since the selector of cell-A transitions into the insulating phase during the setup period when the voltages of all WLs and BLs are reduced to zero. Thus, the indirect transitioning scheme yields less design constraints.

It may be reiterated that the selector parameters (ρ_{INS}, ρ_{MET}, $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$), in general, could be functions of L, A and voltage across the selector (V_{SEL}), as discussed in chapter 1. Similarly, $RA_{M0/1}$, typically is a function of the voltage across the memory element [131]. Equations (4.1) and (4.2) are generally valid in such cases as well, for which the selector and memory parameters needs to be considered as functions of A, L and voltage and their solution requires rigorous numerical simulations. The simplest case is when these parameters are constants i.e. independent of the geometry and voltage. Equations (4.1) and (4.2) form the basis for the selection criteria for suitable PTMs as well as for the co-optimization of L and BL/WL voltages for proper functionality of the cross-point array. In the rest of this chapter, we will use these equations to deduce important conclusions regarding the design space of cross-point memories. It may also be mentioned that another important metric of a selector is the maximum current that it can support. In general, if this current is less than the minimum current required to meet the performance requirements of

Table 4.1 List of Design Parameters and Metrics

	Parameters	Definitions
Material	ρ_{MET} ρ_{INS}	Resistivities in metallic and insulating phases of the PTM
	$J_{C\text{-}MIT}$ $J_{C\text{-}IMT}$	Critical current density of PTM for MIT and IMT
	J_{CM0} J_{CM1} J_{CM}	Critical current density for switching the state of the memory element to '0' or '1'. J_{CM} refers to the value corresponding to the worst case write (higher write voltage).
	RA_{M0} RA_{M1} RA_{M}	Resistance-area product of the memory element for logic '0' and '1'. RA_M refers to the value corresponding to the worst case write (higher write voltage).
	$R_{S,W}$	Sheet resistance of BL/WL metal
Device	D ($A=\pi D^2/4$)	Cross-sectional diameter of MTJ and selector
	L	Length of selector along the current direction
	$RA_{EFF,W}$	'Effective' resistance-area product of the BL/WL = $2R_{S,W}(N_C+N_R)A$
Circuit	V_{READ}	Read Voltage
	V_{WRITE}	Write Voltage
	$I_{M0,WRITE}$ $I_{M1,WRITE}$	Cell current during write when memory element is in logic '0' and '1' states
	$I_{M0,READ}$ $I_{M1,READ}$	Cell current during read when memory element is in logic '0' and '1' states
Array	N_C, N_R	Number of columns and rows in the block
	N_W	Number of bits in a word

Metrics	Definitions
WM	Write Margin = $MIN[(I_{M0,WRITE}/J_{CM1}A)-1, (I_{M1,WRITE}/J_{CM0}A)-1]$
T_W	Write Time
RDM	Read Disturb Margin = $1 - I_{M0/1,READ}/J_{CM0/1}A$ (Use 0 or 1 depending on the current direction)
SM	Sense Margin = $I_{M1,READ} - I_{M0,READ}$
$P_{AC,READ}$	Read Power in the Accessed Cells
$P_{AC,WRITE}$	Write Power in the Accessed Cells
$P_{HA,READ}$	Total Leakage Power in HAC and HAR cells during Read
$P_{HA,WRITE}$	Total Leakage Power in HAC and HAR cells during Write
BLL	Bit-line Leakage = Total leakage current in HAC cells (normalized to $I_{M0,READ}$)
TM	Threshold Margin = $V_{READ}/V_{CIMT} - 1 = 1 - V_{WRITE}/2V_{CIMT}$
HM	Hold Margin = $I_{READ0}/I_{CMIT} - 1 = I_{READ0}/(J_{CMIT}*A) - 1$

'0' refers to the high resistance state of the memory element
'1' refers to the low resistance state of the memory element

the memory, the selector cannot be employed for memory design. Therefore, this is one of the first checks that must be performed to prune out the unsuitable selector candidates. Once a selector meets this criteria, there are other conditions that it needs to satisfy, which are related to equations (4.1-4.2) presented above and discussed subsequently.

4.5 Design Parameters and Simulation Framework

Before we present our analysis, let us define the relevant design parameters and metrics that will be used subsequently. Here, we also describe the simulation framework used for the analysis. Table 4.1 lists the materials, device, circuit and array parameters. The selector material parameters (ρ_{INS}, ρ_{MET}, $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$) form a basis set for the PTMs in subsequent sections. We also consider the maximum current density that can be supported by the selector (J_{LIMIT}) considering thermal and reliability issues. The memory element parameters are defined with subscript '0' representing the high resistance state and '1' representing the low resistance state. We consider the same diameter D (and cross-sectional

area *A*) for the memory element and selector in order to minimize the cell footprint. The spacing between two neighboring cells is considered to be equal to *D* (Fig. 4.1 (a)). This information is used to obtain the effective resistance-area of the WL and BL interconnects ($RA_{EFF,W}$) in the simulation framework. For ARCH1 (Fig. 4.1 (b)), a closed form expression for the worst-case $RA_{EFF,W}$ accounting for both the WL and BL resistance can be approximated as,

$$RA_{EFF,W} \approx 2R_{S,W}(N_C + N_R)A \tag{4.3}$$

Here, $R_{S,W}$ is the sheet resistance of the WL/BL metal and N_C and N_R are the number of columns and rows in the block. Note that (4.3) has *A* (area of the memory element and selector) as one of the factors to be consistent with (4.2-b), which relates the currents normalized to *A*. Also, note that based on Fig. 4.1 (a), the length of the wire per cell is *2D* and its width is *D*. The definition of the *effective* resistance-area product will be used in the rest of this paper. For ARCH2, $RA_{EFF,W}$ needs to be obtained using numerical simulations to capture the distributed wire resistance and the dependence of WL voltage drop on the current of multiple accessed cells in the array block. Typically, $RA_{EFF,W}$ is larger for ARCH2 than ARCH1 since multiple cells sink current in ARCH2.

The array metrics considered in the analysis are listed in Table 4.1. Write margin (WM) is used as a measure of write performance as well as a design margin to account for variations. Similarly, read disturb margin (RDM) represents the read stability and sense margin (SM) measures the read distinguishability. Note that we use current based sensing in our analysis;

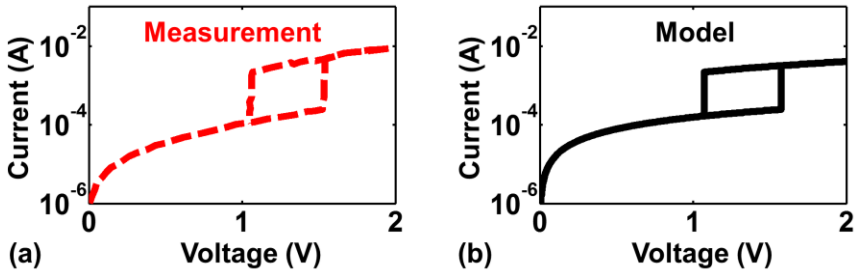


Fig. 4.5 Calibration of the compact model for PTM with the experimental data on VO_2. These films were fabricated using pulsed DC reactive sputtering.

therefore, sense margin is defined in terms of the current difference between the memory and the reference cell. We also analyze bit-line leakage defined as the total leakage current in the HAC cells (Fig. 4.2 (a, b)) normalized with respect to the read current. Large bit-line leakage can sully the current distinguishability between two states, making it challenging to read the data. Additionally, we define three metrics to keep suitable design margins for satisfying equations (4.1) through (4.2). Threshold margin (TM) is the measure of the difference between V_{READ} and $V_{C\text{-}IMT}$ or between $V_{C\text{-}IMT}$ and $^{1}/_{n}V_{WRITE}$ and corresponds to (4.1). Similarly, hold margin (HM) is a measure of the difference between I_{M0}/A and $J_{C\text{-}MIT}$ and is used to account for variations while meeting the constraint set by (4.2-a) and (4.2-b). Direct transition margin (DTM) is defined as the relative difference between $J_{C\text{-}MIT}$ and the initial current through HAC/HAR/UA cells (given by the right-hand side of (4.2-c)) and represents the margin for ensuring that cells undergo MIT when they transition from accessed to HAC/HAR/UA modes.

To carry out the analysis, we use a SPICE based model for the PTM. The details of the modeling approach were discussed in chapter 2. The model is calibrated to the data from our experiments on VO_2 [22] (shown in Fig. 4.5) and for several IMT based selectors [67], [143], [145], [146]. For the memory element, we use physics-based magnetic tunnel

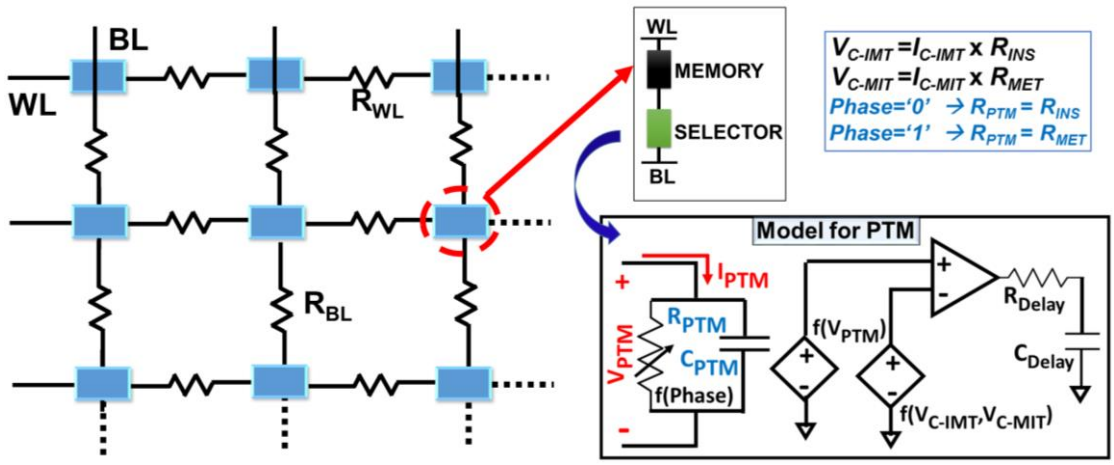


Fig. 4.6 Simulation framework based on SPICE model for the PTM. An MTJ has been used as the memory element. Distributed resistance and capacitance of the bit-line (BL) and word-line (WL) are considered.

junction (MTJ) models from [101]. We also consider the distributed resistance and capacitance of WL and BL interconnects in our analysis [149], [152]. These models are coupled in a self-consistent fashion to numerically obtain the solutions. We perform worst case analysis from the perspective of the WL/BL wire resistances. Thus, for write-ability, we consider the cell that experiences maximum IR drop on WL and BL. For read stability, the cell with the minimum IR drop is considered. For sense margin, we consider the difference in the read current between a cell storing '1' (low resistance state) with maximum IR drop and a cell storing '0' (high resistance state) with minimum IR drop on WL and BL. For the design constraints given by equations (4.2), the IR drop ($RA_{EFF,W}$) is considered only for (4.2) to account for the worst case scenario (as explained before). The complete simulation framework is illustrated in Fig. 4.6.

We pursue two approaches to carry out the selector analysis. First, we employ equation-based analysis to understand the selector requirements and define the feasible operating regions. The resultant equations offer insights into various aspects of the selector design. We complement the equation-based analysis with the numerical simulations using the framework described above and discuss the design space, achievable power-performance-robustness metrics and other design aspects. We first carry out a general analysis to define the selector material and device requirements for cross-point array design. This is followed by feasibility analyses of two selector materials – single crystal VO_2 [143] and copper-doped HfO_2 [67] for applications in spin-based cross-point arrays. Finally, we perform material space analysis and quantify the array metrics. We focus on single crystal VO_2 and copper-doped HfO_2 to convey the key points associated with the feasibility analysis of selectors. This analysis can be extended for other functional oxides, as required. We choose spin-based memories for our analysis because (a) it is one of the most promising technologies for non-volatile storage [131] and (b) it requires bi-directional write current that makes the discussion more general. Other memory technologies can be analyzed in a similar fashion.

4.6 Selector Design and Material Requirements

For proper operation of a cross-point array, it is critical that the design constraints presented in section 4.4 are satisfied. This requires proper selection of the PTM as well as judicious co-design of the memory element, selector device and the array architecture. In this section, we present the design methodology for the selector device and define figures of merit for the PTMs to determine their feasibility for application as selectors.

4.6.1 Co-design of Selector Length and Read/Write Voltages

The criteria for the selection of V_{READ} and V_{WRITE} is typically determined by the power, performance and stability targets of a memory macro. In cross-point architectures, the design constraints presented in section 4.4 lead to additional considerations. Consequently, upper and lower bounds on V_{READ} and $|V_{WRITE}|$ are obtained, which guide the selection of WL/BL biases as well as other design parameters. Since the write voltages may be bi-polar, we consider the absolute values in this analysis. Once the magnitudes of the write voltages are determined, appropriate signs/polarity can be used depending on the direction of the write current. The analysis presented below is general and is valid for memories with unipolar or bi-polar write voltages.

It is clear from (4.1) that the read voltage must be greater than $V_{C\text{-}IMT}$ and the write voltage must be less than $n \times V_{C\text{-}IMT}$. Also, V_{READ} should be large enough that (4.2) is satisfied. On the other hand, $|V_{WRITE}|$ should be small enough so that the constraint given by (4.2-c) is met for the direct transitioning scheme. Moreover, the maximum write voltage is also determined by the current carrying capability of the selector. In addition, write margin (WM) and read disturb margin (RDM) targets set the minimum and maximum limits for the write voltage and read voltage, respectively. Combining these observations and considering the margins defined in section 4.4 and Table 4.1, the following equations are obtained.

$$|V_{WRITE}|_{MIN} = (1 + WM) J_{CM} \left(\rho_{MET} L + RA_M + RA_{EFF,W}\right) \tag{4.4}$$

$$|V_{WRITE}|_{MAX1} = n(1 - TM)\, \rho_{INS} J_{C-IMT} L \tag{4.5-a}$$

$$|V_{WRITE}|_{MAX2} = n(1 - DTM)\ J_{C-MIT}(\rho_{MET}L + RA_{M1}) \quad (4.5\text{-b})$$

$$|V_{WRITE}|_{MAX3} = J_{LIMIT}(\rho_{MET}L + RA_{M1}) \quad (4.5\text{-c})$$

$$|V_{WRITE}|_{MAX} = MIN\ (|V_{WRITE}|_{MAX1}, |V_{WRITE}|_{MAX2}, |V_{WRITE}|_{MAX3}) \quad (4.5)$$

$$V_{READ,MIN1} = (1 + TM)\rho_{INS}J_{C-IMT}L \quad (4.6\text{-a})$$

$$V_{READ,MIN2} = (1 + HM)\ J_{C-MIT}\left(\rho_{MET}L + RA_{M0} + RA_{EFF,W}\right) \quad (4.6\text{-b})$$

$$V_{READ,MIN} = MAX\ (V_{READ,MIN1}, V_{READ,MIN2}) \quad (4.6\text{-c})$$

$$V_{READ,MAX} = (1 - RDM)\ J_{CM}(\rho_{MET}L + RA_{M}) \quad (4.7)$$

Here, the subscripts 'MIN' and 'MAX' refer the minimum and maximum values and J_{CM} is the critical current density for the memory element required for switching the state. Note that J_{CM} in (4.4) is the worst case critical current density corresponding to either 0→1 or 1→0, whichever yields a higher write voltage. Similarly, the resistance-area product of the memory RA_M corresponds to the worst case write. Same argument can be applied for (4.7). The reason is, typically the read current direction is chosen so that it is harder to flip the state of the memory element, which may correspond to the worst case write. On the other hand, RA_{M1} in (4.5-b,c) and RA_{M0} in (4.6-b) is the memory resistance-area product for the low and high resistance states, respectively to consider the worst case. It is also noteworthy that the worst cases of $V_{READ,MAX}$ (or RDM), $|V_{WRITE}|_{MAX2}$ (direct transitioning) and $|V_{WRITE}|_{MAX3}$ (constrained by the maximum selector current) correspond to the cell, which is closest to the WL/BL voltage source. Hence, (4.5-b), (4.5-c) and (4.7) do not contain the resistance-area product of the wire ($RA_{EFF,W}$). It is also important to mention that if indirect transitioning scheme is followed (Fig. 4.3 (b)), $|V_{WRITE}|_{MAX2}$ can be considered to be infinitely large (i.e. the constraint given be (4.2-c) does not exist, as discussed before).

Considering the minimum and maximum read/write voltages given by equations (4.4) - (4.7), we now discuss the respective design spaces. To simplify the analysis and to show the relevant trends, we assume J_{LIMIT} to be sufficiently large so that $|V_{WRITE}|_{MAX3}$ in (4.5-c) is larger than the other two maximum write voltages given by (4.5-a) and (4.5-b). The

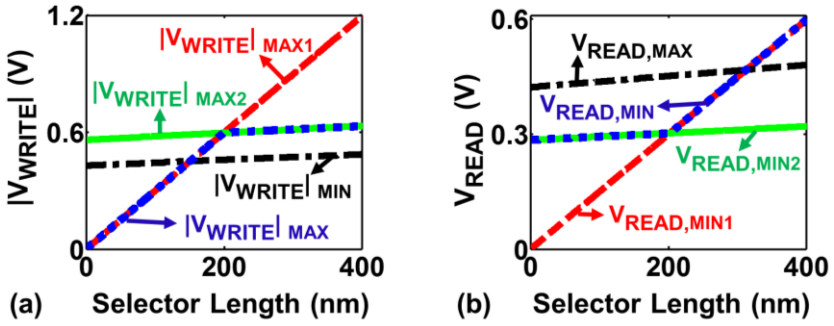


Fig. 4.7 Bounds on (a) magnitude of write voltage ($|V_{WRITE}|$) and (b) read voltage (V_{READ}) as a function of selector length (L) showing different components given by equations (4.4), (4.5), (4.6) and (4.7). The feasible region is where the maximum values are greater than the minimum values.

discussion on the feasible range of selector length does not change, as long as J_{LIMIT} is sufficiently larger than J_{CM}, as can be deduced from (4.4) and (4.5-c). If a material does not meet this condition (which should be the first check, as explained before), then it is unsuitable for selector application. However, if this condition is met, the following analysis on the bounds on selector length holds, irrespective of the magnitude of J_{LIMIT}.

Let us begin by considering the dependence of the write voltage on selector length shown in Fig. 4.7 (a). It can be observed that the requirement $|V_{WRITE}|_{MAX} >= |V_{WRITE}|_{MIN}$ is satisfied for a certain range of selector length (L). To elaborate on this point, let us consider the points of intersection of the plots corresponding to $|V_{WRITE}|_{MIN}$, $|V_{WRITE}|_{MAX1}$ and $|V_{WRITE}|_{MAX2}$. Equating (4.4) and (4.5-a), we obtain the intersection point which defines the feasible range of L (for which $|V_{WRITE}|_{MAX1} >= |V_{WRITE}|_{MIN}$).

$$L \geq L_{MINW1} = \frac{(1+WM)\, J_{CM}\left(RA_M + RA_{EFF,W}\right)}{n(1-TM)\rho_{INS}J_{C-IMT} - (1+WM)\,\rho_{MET}J_{CM}} \tag{4.8-a}$$

Similarly, considering (4.4) and (4.5-b), $|V_{WRITE}|_{MAX2} > |V_{WRITE}|_{MIN}$ corresponds to,

$$L \geq L_{MINW2} = -\frac{n(1-DTM)J_{C-MIT}RA_{M1} - (1+WM)\, J_{CM}\left(RA_M + RA_{EFF,W}\right)}{[n(1-DTM)J_{C-MIT} - (1+WM)J_{CM}]\rho_{MET}} \tag{4.8-b}$$

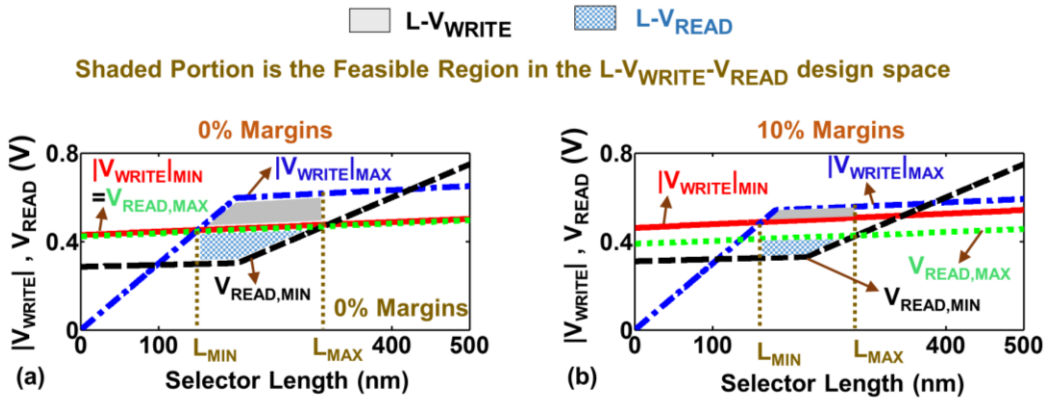


Fig. 4.8 Minimum and maximum read and write voltages as functions of selector length showing the feasible region where $|V_{WRITE}|_{,MAX} > |V_{WRITE}|_{,MIN}$ and $V_{READ,MAX} > V_{READ,MIN}$. The plots are shown for (a) 0% margins (WM, RDM, TM and HM) and (b) 10% margins. The results are for parameters corresponding to SC VO_2 (Table 4.2) except that larger J_{C-MIT} is used to illustrate the effect of $V_{READ,MIN1}$ and $V_{READ,MIN2}$ on $V_{READ,MIN}$, which can be observed from the change of the slope of the $V_{READ,MIN}$ line. V/2 scheme and direct transitioning method has been used.

Using (4.8-a) and (4.8-b), the minimum length above which a feasible range of write voltages (i.e. $|V_{WRITE}|_{MAX} >= |V_{WRITE}|_{MIN}$) is obtained and is given by

$$L_{MINW} = MAX(L_{MINW1}, L_{MINW2}) \tag{4.8}$$

It is important to note that the inequalities above are obtained by considering that the denominators of the fractions on the right-hand side are positive. If the denominators are negative, then no feasible region is obtained for $L>0$. This is elaborated in the next sub-section. An important point to mention is that for the indirect transitioning technique (Fig. 4.3 (b)), the non-existence of constraint given by (4.2-c) implies that (4.8-b) does not need to be considered. Therefore, the feasible range for L and V_{WRITE} expands, as shown later.

Similar to the write analysis, we obtain the conditions for $V_{READ,MAX} >= V_{READ,MIN}$. Considering Fig. 4.7 (b) and the points of intersection of (4.6-a) and (4.7), we obtain that $V_{READ,MAX} >= V_{READ,MIN1}$ corresponds to

$$L \leq L_{MAXR} = \frac{(1 - RDM)\, J_{CM}(RA_M)}{(1 + TM)\rho_{INS}J_{C-IMT} - (1 - RDM)\, \rho_{MET}J_{CM}} \tag{4.9-a}$$

Similarly, for $V_{READ,MAX}$ >= $V_{READ,MIN2}$ (equations (4.6-b) and (4.7)), the following condition is derived,

$$L \geq L_{MINR} = -\frac{(1-RDM)J_{CM}(RA_M) - (1+HM)J_{C-MIT}\left(RA_{M0} + RA_{EFF,W}\right)}{(1-RDM)J_{CM} - (1+HM)J_{C-MIT}} \quad \text{(4.9-b)}$$

Thus, for $V_{READ,MAX}$ >= $V_{READ,MIN}$,

$$L_{MINR} \leq L \leq L_{MAXR} \quad \text{(4.9)}$$

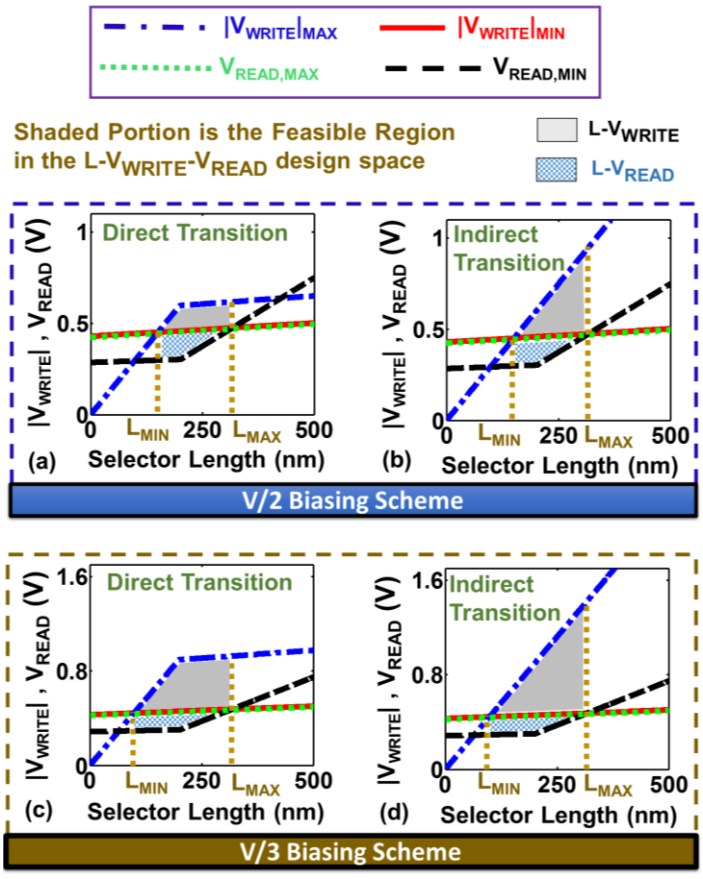


Fig. 4.9 Comparison of the feasible design space for different biasing schemes (V/2, V/3), and transition methods (direct, indirect) showing larger design space for V/3 scheme compared to V/2; and boost in design space using indirect transition method.

Similar to write, (4.9-a) and (4.9-b) consider the denominators to be positive. If the denominator becomes negative, then for (4.9-b), no feasible region ($V_{READ,MAX}$ >= $V_{READ,MIN2}$) is obtained for L>0. However, if the denominator for (4.9-a) is negative, $V_{READ,MAX}$ >= $V_{READ,MIN1}$ for all values of L>0. In other words, there is no upper bound on L. Combining the ranges for read and write, we obtain the minimum and maximum lengths (L_{MIN} and L_{MAX} respectively) as

$$L_{MIN} = MAX(L_{MINW}, L_{MINR}) \quad \text{(4.10-a)}$$

$$L_{MAX} = L_{MAXR} \quad \text{(4.10-b)}$$

The read and write voltages corresponding to L_{MIN} and L_{MAX} are obtained using (4.8)-(4.10) in (4.4)-(4.7). It is noteworthy that the parameters of the selector (ρ_{INS}, ρ_{MET}, $J_{C\text{-}IMT}$, $J_{C\text{-}MIT}$) and memory (J_{CM}, RA_M), in general, can be functions of L, A and voltage. In order to obtain L_{MIN}, L_{MAX} and the corresponding read/write voltages, the equations above need to be solved numerically. The solutions can be used to obtain the region of operation in the L-V_{READ}-V_{WRITE} design space, as illustrated in Fig. 4.8. It can be observed that the feasible design space shrinks as the design margins are increased, as expected. Fig. 4.9 shows the comparison of the V/2 and V/3 schemes and the direct transition and indirect transition techniques. Two important points to note are discussed as follows:

(a) The indirect transitioning scheme relaxes the constraint for the PTM and hence, permits a larger range of write voltages and selector length. This comes at the cost of reduced performance due to the need for an extra setup time.

(b) The conditions are less stringent for n=3 than for n=2. This implies that V/3 scheme expands the feasible L-V_{WRITE}-V_{READ} region, offering more design choices. However, this comes at the cost of leakage in the unaccessed (UA) cells.

To complete the discussion, let us analyze the impact of J_{LIMIT} on the design space (Fig. 4.10). It can be observed that for lower J_{LIMIT}, the allowed range of $|V_{WRITE}|$ reduces as expected. However, as explained before, the feasible range of selector length remains unaffected, as long as J_{LIMIT} is sufficiently larger than J_{CM}. The region of operation depends on the selector material parameters, memory attributes, array architecture and the design

margins. As discussed above, Equations (4.8) - (4.10) are valid for a certain range of parameters, which yield positive values of the denominators. These ranges provide useful information about the necessary conditions for the selector material properties, which is discussed next.

4.6.2 Selector Material Requirements and Figures of Merit

For the feasible range of L to exist, it is critical that the lines corresponding to $|V_{WRITE}|_{MAX}$ and $|V_{WRITE}|_{MIN}$ intersect each other. This condition is met if the denominators in (4.8) - (4.10) are positive. Before we discuss the implications for the selector material, let us elaborate on this considering constant (L, A, voltage independent) selector and memory parameters for providing an intuitive insight. It can be observed from (4.4) and (4.5-a) that the y-intercept of the $|V_{WRITE}|_{MAX1}$ and $|V_{WRITE}|_{MIN}$ lines are 0 and $(1 + WM)\, J_{CM}\left(RA_M + RA_{EFF,W}\right)$ respectively. Hence, for $|V_{WRITE}|_{MAX1} >= |V_{WRITE}|_{MIN}$, the necessary condition is that the slope of the $|V_{WRITE}|_{MAX1}$ line (4.5-a) is greater than that of the $|V_{WRITE}|_{MIN}$ line (4.4). This translates to the following equation.

$$n(1 - TM)\rho_{INS}J_{C-IMT} > (1 + WM)\, J_{CM}\rho_{MET} \tag{4.11}$$

It can be observed that (4.11) corresponds to the denominator of (4.8-a) being positive. Similar conditions can be obtained for the other equations. Although, the example above

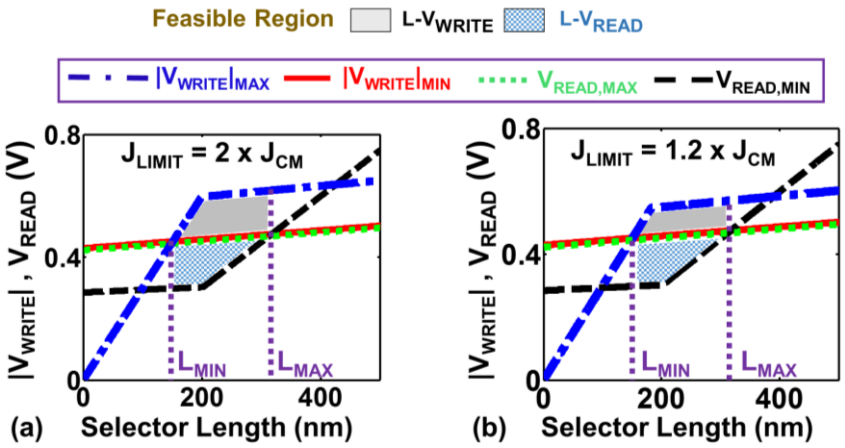


Fig. 4.10 Impact of J_{LIMIT} on the feasible design space. Lower J_{LIMIT} leads to reduction in the feasible ranges.

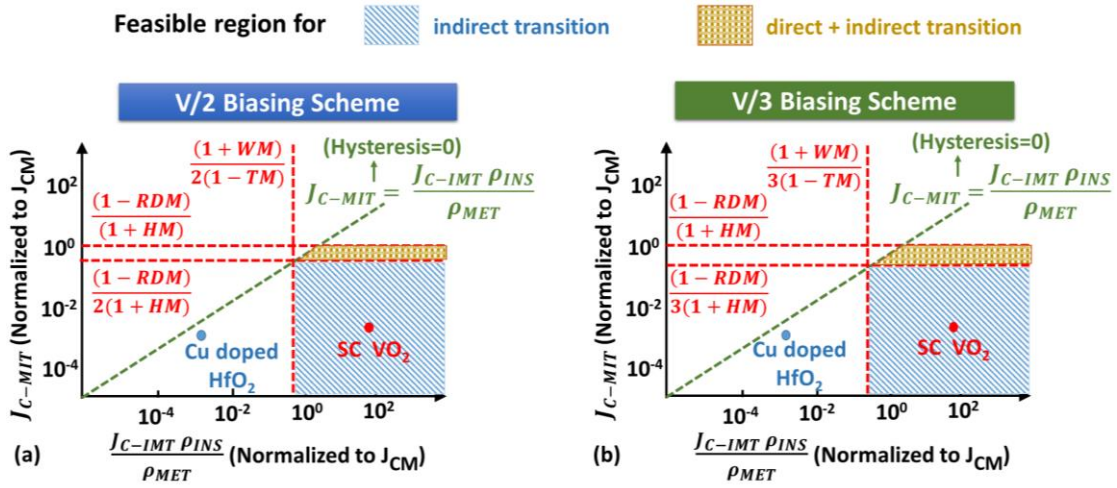


Fig. 4.11 Design space for the PTM showing feasible and infeasible regions for (a) V/2 and (b) V/3 biasing schemes. The region for indirect and direct transition techniques are also shown. The position of two PTMs: SC VO_2 and Cu doped HfO_2 are also illustrated, showing the former in the feasible region and the latter in the infeasible region.

is for constant selector and memory parameters, the conclusion about the positive denominators is equally applicable for *L*, *A*, voltage dependent parameters as well. Positive denominators yield to following conditions for the selector material.

$$\frac{\rho_{INS}\, J_{C-IMT}}{\rho_{MET}} > \frac{(1+WM)\, J_{CM}}{n(1-TM)} \tag{4.12-a}$$

$$\frac{(1+WM)\, J_{CM}}{n(1-DTM)} < J_{C-MIT} < \frac{(1-RDM)\, J_{CM}}{(1+HM)} \tag{4.12-b}$$

Equation (4.12-a) corresponds to (4.8-a) and (4.12-b) corresponds to (4.8-b) and (4.9-b). Note, as mentioned before, (4.9-a) does not lead to any constraints for negative denominator, but removes the upper bound for *L*. In other words, if $\frac{\rho_{INS} J_{C-IMT}}{\rho_{MET}} < \frac{(1-RDM)\, J_{CM}}{(1+TM)}$, L_{MAX} is infinity. Coming back to equations (4.12-a) and (4.12-b), it is interesting to observe that, since PTMs exhibit hysteresis i.e. $V_{CIMT} > V_{CMIT}$ or $\rho_{INS}\, J_{C\text{-}IMT} > \rho_{MET}\, J_{C\text{-}MIT}$, (4.12-a) is automatically satisfied if the lower bound on $J_{C\text{-}MIT}$ set by (4.12-b) is met (provided DTM ~ TM). Therefore, for the direct transitioning method, the necessary condition for the selector is given by (4.12-b). However, if the indirect transitioning method

is used, then (4.8-b) is not considered (as discussed before) and the conditions for the selector material are modified to

$$\frac{\rho_{INS}J_{C-IMT}}{\rho_{MET}} > \frac{(1+WM)\,J_{CM}}{n(1-TM)} \tag{4.13-a}$$

$$J_{C-MIT} < \frac{(1-RDM)\,J_{CM}}{(1+HM)} \tag{4.13-b}$$

Equations (4.12) and (4.13) yield important figures of merit for the PTM namely, $\frac{\rho_{INS}J_{C-IMT}}{\rho_{MET}}$ and $J_{C\text{-}MIT}$. Depending on the transitioning technique (direct or indirect) and the target margins, these figures or merit must be in the ranges given by (4.12) and (4.13), which directly depend on the critical current density of the memory. For a general case in which the selector parameters are dependent on *L*, *A* and the voltage across it, the figures of merit need to be evaluated self-consistently with other design parameters using numerical simulations. Fig. 4.11 illustrates the constraints graphically showing the material space for V/2 and V/3 schemes and for direct and indirect thresholding techniques, which are consistent with the previous discussions that (a) V/3 yields larger design space than V/2 and (b) indirect thresholding enhances the feasible range compared to the direct thresholding (Fig. 4.9).

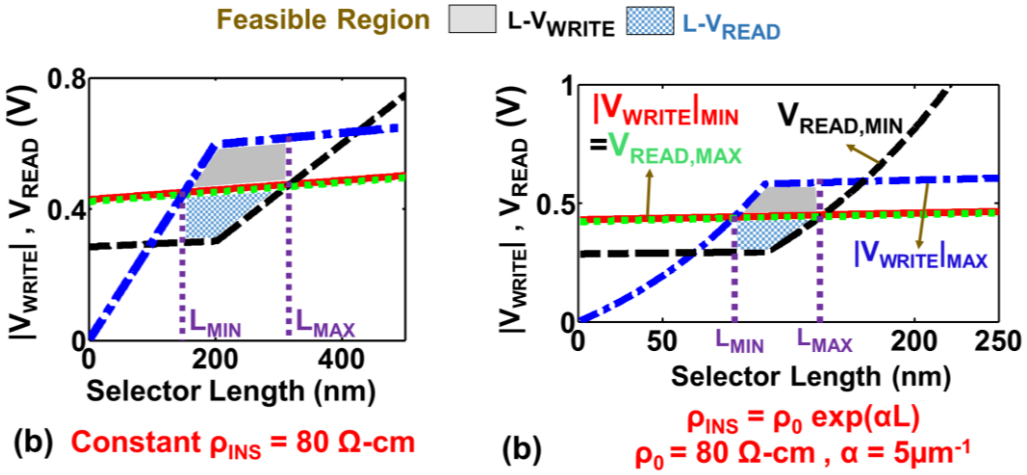


Fig. 4.12 Impact of non-linear insulating state resistivity of the selector on the feasible design space showing similar qualitative trends as with constant resistivity.

4.6.3 Non-linearity in Selector Parameters

In continuation with our discussion on the dependence of selector parameters on L, A and voltage, here we illustrate an example comparing the L-V_{WRITE}-V_{READ} design space for constant resistivities and critical current thresholds versus the case when the insulating state resistance of the selector shows an exponential dependence on L ($R_{INS}=R_0*L*\exp(\alpha L)$. It can be easily deduced that ρ_{INS} will be of the form $\rho_0*\exp(\alpha L)$ for the latter case. Fig. 4.12 shows the design space. The common attribute of both cases is that the maximum and minimum V_{WRITE} and V_{READ} plots intersect each other defining L_{MIN} and L_{MAX}. However, the range of feasible L for the non-linear resistivity is smaller due to exponential dependence on L. Thus, the general design constraints and inter-play between L, V_{READ} and V_{WRITE} exhibit similar qualitative behavior for both L-dependent and L-independent resistivity, illustrating the general applicability of the methodology developed in the previous sub-sections for obtaining the feasible design space.

4.6.4 Process Variations

The equations introduced in the previous sub-sections include various design margins to account for process variations. We showed in Fig. 4.8 that the feasible design space shrinks

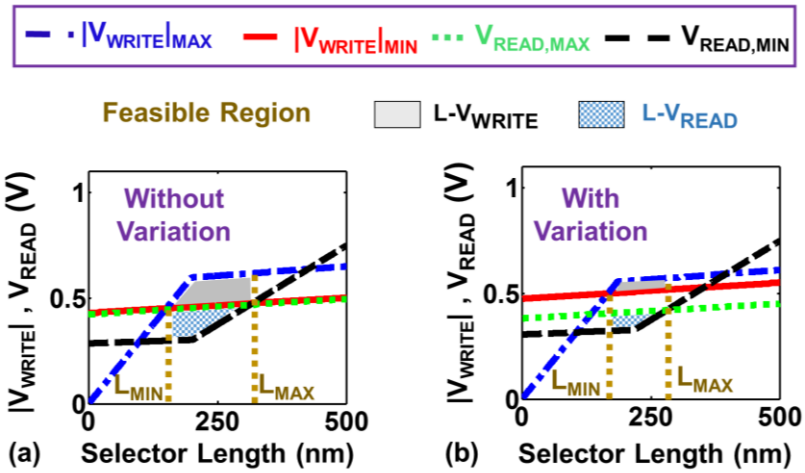


Fig. 4.13 Impact of worst-case process variations on the feasible design space showing reduced feasible range. The impact is similar to considering design margins (~10%) as in Fig. 4.8. Variations applied for the above results: ±5% for selector area, MTJ area, interconnect area and interconnect length each; ±1% for MTJ oxide thickness.

when the design margins are increased. In this sub-section, we perform a rigorous evaluation of the impact of process variations on the feasible design space. For this, we consider ±5% variation in the memory (MTJ) area, selector area, interconnect area and interconnect length. In addition, ±1% variation in the MTJ oxide thickness is considered. We evaluate the maximum and minimum read/write voltages considering the worst-case variations for each parameter. The results are shown in Fig. 4.13. As expected, worst case process variations shrink the feasible region of operation. Comparing Fig. 4.13 with Fig. 4.8, it can be observed the explicit inclusion of process variations give similar results compared to employing design margins to account for variations. Depending on the data available on parameter variations and the design targets, either of the two methodologies may be used to consider variations in the analysis. While the explicit inclusion of process variations offers the most accurate approach, the technique employing design margins enables establishing the relations between the figures of merit of the selector and various margins, as explained before. This can be used to provide quick and useful design insights into the selector down-selection and the optimal choice of L, V_{READ} and V_{WRITE} to meet the design targets.

4.6.5 Other Factors

The conditions and figures of merit presented in the previous sub-sections pertain to satisfying the design constraints for operation of the selector in a proper phase and for meeting the write performance (or WM) and read stability (or RDM) targets. The figures of merit define necessary but not sufficient conditions for the selector. There are other important design metrics, which can be affected by the selector material parameters and geometry. In particular, for a given WM and RDM, increase in ρ_{MET} necessitates the increase in read/write voltages which results in higher read/write power, higher leakage power in the half-accessed cells and increase in the bit-line leakage [153]. Higher ρ_{MET} also increases the cell resistance, which reduces the sense margin (SM).

Similarly, decrease in ρ_{INS} increases the leakage in half-accessed cells, including the bit-line leakage. Thus, in addition to meeting the conditions given by (4.12) and (4.13), the selector material must have sufficiently low ρ_{MET} and sufficiently high ρ_{INS} in order to

Table 4.2 Simulation Parameters for Case Studies and Material Space Analysis

Parameters	Values	
	SC VO_2	Cu-doped HfO_2
ρ_{MET}	5×10^{-4} Ω-cm	3.89×10^{1} Ω-cm
ρ_{INS}	80 Ω-cm	6.03×10^{5} Ω-cm
$J_{C\text{-}MIT}$	5.10×10^{3} A/cm^2	2.60×10^{3} A/cm^2
$J_{C\text{-}IMT}$	1.87×10^{2} A/cm^2	1.52×10^{-1} A/cm^2
MTJ Free Layer Parameters	Energy barrier = 51 k_BT Gilbert damping coefficient = 0.028 Saturation Magnetization = 80 kA/m	
D ($A=\pi D^2/4$)	45nm	
$N_C \times N_R$	128 x 128 per block	
N_W	64 (= number of blocks)	
Architecture	ARCH1	

obtain the best energy-delay-robustness trade-offs. In general, $\rho_{MET}L$ must be significantly less than the RA_M and may be comparable to the $RA_{EFF,W}$ to maintain a sufficiently large sense margin. Similarly, the bit-line leakage must be considerably less than the read current for robust read operation. In addition to the array metrics, L_{MIN} and L_{MAX} (i.e. the feasible range of the selector length) must be in a range suitable for the fabrication of the selector device. Moreover, the read/write voltages in the feasible range should also be compatible with other on-chip voltage supplies. All such design metrics and criteria drive the choice of a suitable PTM.

4.7 Case Studies

In the previous section, we discussed the selector material requirements and the L-V_{WRITE}-V_{READ} design space, establishing the figures of merit for functional oxides. In this section, we apply these concepts to two known PTMs considering MTJ as the memory element. As mentioned before, the case studies are focused on two PTMs to convey the relevant points and to avoid repetition. MTJs are chosen as the memory element for this analysis to consider the bi-polar write voltages and because spin-memories are one of the most promising non-volatile technologies [88], [131]. We consider ARCH1 (Fig. 4.1 (b)) as the

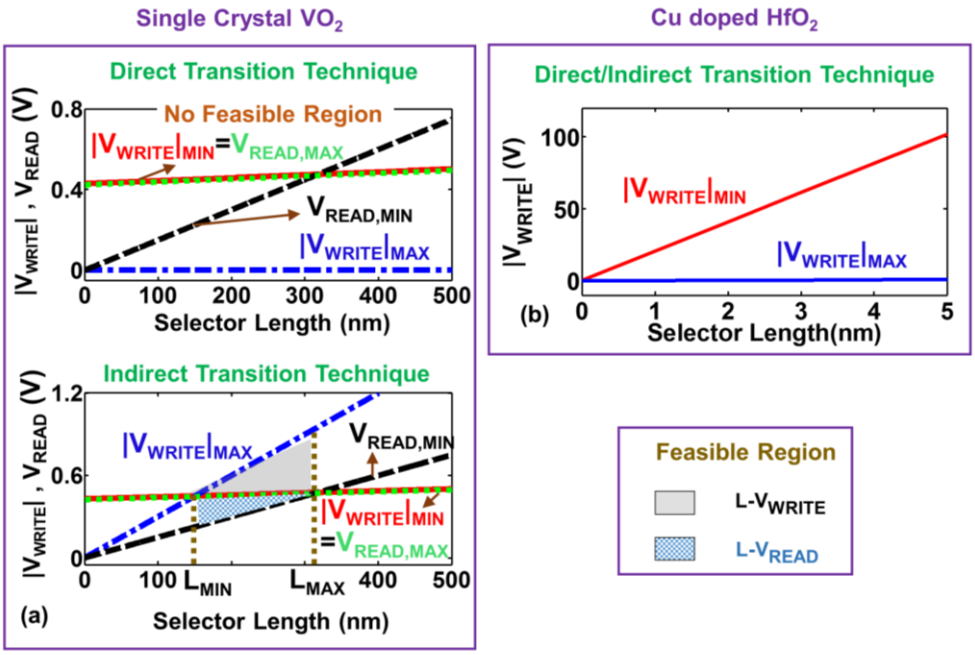


Fig. 4.14 Minimum and maximum read and write voltages for V/2 biasing scheme as a function of selector length for (a) SC VO_2 and (b) Cu-doped HfO_2. SC VO_2 shows a feasible region of operation for indirect transition scheme while for direct transition, $|V_{WRITE}|_{MAX}$ is always less than $|V_{WRITE}|_{MIN}$. Cu-doped HfO_2 shows $|V_{WRITE}|_{MAX} < |V_{WRITE}|_{MIN}$, irrespective of the transition scheme.

array architecture. The values of the simulation parameters are summarized in Table 4.2. The parameters for the PTMs are extracted from the experimental data in [143] and [67]. Since, the information on the L and A dependence of the PTM resistivities and critical current densities was not available; we consider constant parameters to illustrate the trends. We consider copper (Cu) interconnect for all of our analysis.

4.7.1 Single Crystal (SC) VO_2

To design the SC VO_2 selector for spin-based cross-point architecture, we first obtain the figures of merit from the material parameters. Fig. 4.11 shows that, SC VO_2 lies in the feasible region for indirect thresholding technique. Using our simulation framework, we obtain the L-V_{WRITE}-V_{READ} design space, which is shown in Fig. 4.14 (a). To reiterate the non-suitability of SC-VO_2 for direct thresholding, we show that there is no feasible write voltage (Fig. 4.14 (a)) to satisfy the design constraints discussed above. This is mainly due

to low $J_{C\text{-}MIT}$ of SC-VO_2 (see Table 4.2). However, by employing indirect thresholding, feasible L-V_{WRITE}-V_{READ} design space is obtained (Fig. 4.14 (a)). It can be observed that the selector length must be in the range of 150 nm to 318 nm if no margins are considered and in the range of 177nm to 260 nm for 20% design margins (not shown in the figure). In Fig. 4.15, we show different design metrics as a function of selector length in the feasible region. Different points in these plots have been obtained by sweeping V_{READ} and V_{WRITE} between their respective minimum and maximum values along with selector length. The plots show the range of values that can be achieved with SC VO_2. Metric values outside this range are not achievable with SC VO_2 selector and a better selector material (with higher ρ_{INS} or lower ρ_{MET}) may be required, which expands the feasible L-V_{WRITE}-V_{READ} design space. This analysis shows the capabilities and limitations of SC-VO_2.

Let us first consider the read operation. The conflict between sense margin (SM) and read disturb margin (RDM) is clear. As expected, while optimizing SM implies operating at a high V_{READ}, boosting RDM requires low V_{READ}. However, an interesting observation is that at L=L_{MIN}, the range of feasible read voltage is maximized, which enhances the design flexibility and enables read optimization aiming a balance between SM and RDM. Similarly, if the read power needs to be minimized for a given SM and RDM target, Fig. 4.14 provides the design space to achieve that. As an example, if the design specifications require SM > 20µA and RDM > 20%, then one can operate in the read voltages between 0.25 V to 0.35 V at L = 100 nm. In this range, one can choose to operate at 0.25 V to minimize the read power. Based on the trends observed in Fig. 4.15, an optimal design point can be chosen as per the power-performance targets. Alternatively, Fig. 4.15 can provide insights into the achievable metrics for SC VO_2 for a given set of V_{READ} and L.

Similar analysis can be performed for the write operation. To balance between the conflicting requirements for write power and write performance, L=L_{MAX} offers the largest range of $|V_{WRITE}|$. As for the read analysis, these plots can be used to either deduce the achievable write metrics for a given L and V_{WRITE} or to choose the optimal V_{WRITE} and L to meet the design specifications.

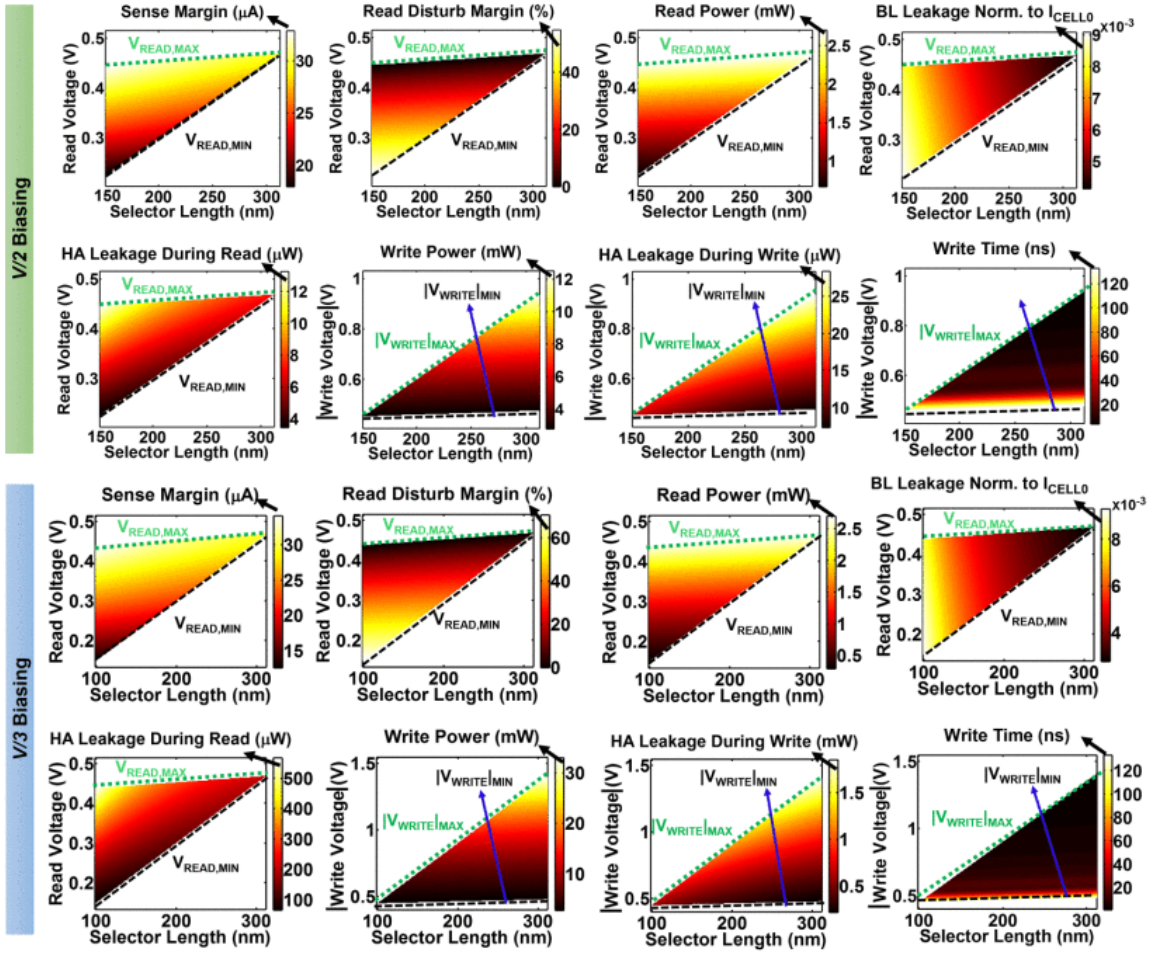


Fig. 4.15 Array metrics: sense margin; read disturb margin; total read power; bit-line (BL) leakage; total leakage power of the half-accessed/unaccessed (HA+UA) cells during read; total write power; total leakage power of the half-accessed cells during write; write time as a function of the selector length with single crystal VO_2 selector and read/write voltages. The analysis is performed considering 0% margins for V/2 scheme and V/3 scheme employing indirect transition.

BL leakage is very small relative to the read current (I_{CELL0}) by virtue of high ρ_{INS} of SC VO_2. The total leakage in the Half-Accessed/Unaccessed cells (HA/UA leakage) during read is minimized for lowest V_{READ}, which also corresponds to lowest L. HA/UA leakage during write is minimized for lowest V_{WRITE} and largest L (that yield maximum insulating state resistance). Comparing the V/2 and V/3 schemes in Fig. 4.15, it can be easily deduced that, V/2 scheme offers much lower HA+UA leakage, as the UA leakage is zero. On the other hand, V/3 scheme expands the design space for write offering higher write

performance. This is because the design constraints for the write voltage of half accessed cells (equation 4.1 (b)) is relaxed for n=3, which enables write operation at higher voltages. Two design approaches may be pursued to optimize the array design:

(a) Without considering any design margin initially, the maximum feasible design space is obtained. The point of operation is then chosen from the mid-portion of feasible region, considering sufficient margins for L, V_{READ} and V_{WRITE}.

(b) Appropriate margins (*WM, RDM, TM, DTM and HM*) are considered initially to obtain a smaller region of operation.

If the design priority is to optimize the read operation, L_{MIN} can be chosen as the design point, which offers the maximum flexibility to find a balance between *SM* and *RDM*, as discussed before. If write optimization is the priority, operation at L_{MAX} offers the lowest write time as well as maximum range for power-speed trade-offs. Note that although L_{MIN} and L_{MAX} lie at the edge of the operating range, the initial margins enable proper functionality (albeit with some loss in performance), even if process variations cause L to fall outside the region of operation.

4.7.2 Copper (Cu)-doped HfO_2

Repeating the same procedure for Cu-doped HfO_2, we obtain the figures of merit. It can be observed in Fig. 4.11 that due to large ρ_{MET}, Cu-doped HfO_2 (as fabricated in [67]) does not lie in the feasible region for spin-based memories. This is also confirmed from the V_{READ}/V_{WRITE} versus L plot (Fig. 4.14 (b)), which shows that $|V_{WRITE}|_{MIN}$ is always greater than $|V_{WRITE}|_{MAX,}$ for both the direct and indirect transitioning schemes. Higher values of $|V_{WRITE}|_{MIN}$ are due to a high the metallic phase resistance of the selector (~1.2 MΩ for L=5nm). It may be mentioned that if the analysis is repeated for a different memory technology with a lower J_{CM}, Cu-doped HfO_2 may fall in the feasible region. Alternatively, tailoring the material properties to reduce ρ_{MET} and in turn, to sufficiently increase the figure of merit can make Cu-doped HfO_2 suitable to be used as a selector device for spin-based cross-point memories.

4.8 Material Space Analysis

In the previous section, we used the concepts presented in this paper to perform feasibility analysis of two specific functional oxides. In order to present a more detailed discussion on the material design space, we analyze the dependence of array metrics on the material parameters of functional oxides in this section. We use the same simulation parameters as in the previous section (Table 4.2) and adopt the second design approach discussed in the previous section. We focus on the indirect transitioning method in this section to provide the trends for a larger design space. Given the four basis parameters (ρ_{INS}, ρ_{MET}, $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$), first the figures of merit are obtained to determine whether equations (4.13) are satisfied. If the design constraints are met, L-V_{READ}-V_{WRITE} region is obtained considering 30% WM, TM and HM. In this analysis, we focus on optimizing the read operation. Hence, based on the discussion in the previous section, a design point is chosen with (a) $L=L_{MIN}$, (b) V_{WRITE} corresponding to the value at L_{MIN} (at which $|V_{WRITE}|_{MAX}=|V_{WRITE}|_{MIN}$) and (c) V_{READ} equal to the maximum values (to maximize the sense margin). Note, this analysis is at *iso*-write-time (=50 ns corresponding to 30% WM at $|V_{WRITE}|=|V_{WRITE}|_{MIN}$) and *iso*-RDM (=30%). The resistivities of the functional oxide in the metallic and insulating phases are swept to obtain the dependence of the array metrics on the selector material properties. We perform the sweeps for two values of $J_{C\text{-}IMT}$ to illustrate the trends. $J_{C\text{-}MIT}$ is chosen to be a value less than $0.538\times J_{CM}$ so that (4.13-b) is satisfied for 30% margins. Thus, the analysis in this section is valid for any material with $J_{C\text{-}MIT} < 2.8\times10^{6}$ A/cm^2.

Fig. 4.16 shows the ρ_{MET} - ρ_{INS} space. It is important to note the there is an infeasible region in this space, which corresponds to high ρ_{MET} and low ρ_{INS} and therefore low value of the figure of merit in (4.13-a). In the feasible region, increasing ρ_{INS} implies increasing the slope of $|V_{WRITE}|_{MAX}$ (equation (4.5)) and $V_{READ,MIN}$ (equation (4.6-c)) lines, which reduces L_{MIN} and L_{MAX} and the corresponding values of V_{READ} and $|V_{WRITE}|$. This leads to lower read/write power. Decrease in L_{MIN} and consequent reduction in the selector resistance enhances SM. The trends with respect to ρ_{MET} can also be observed in Fig. 4.16. Selector with lower ρ_{MET} (lower resistance) leads to lower read/write voltage and hence, reduction in read/write power. In addition, leakage in the half-accessed cells is reduced and SM is boosted. Note that for low values of ρ_{INS} and high values of $\rho_{MET,}$ the read/write voltages

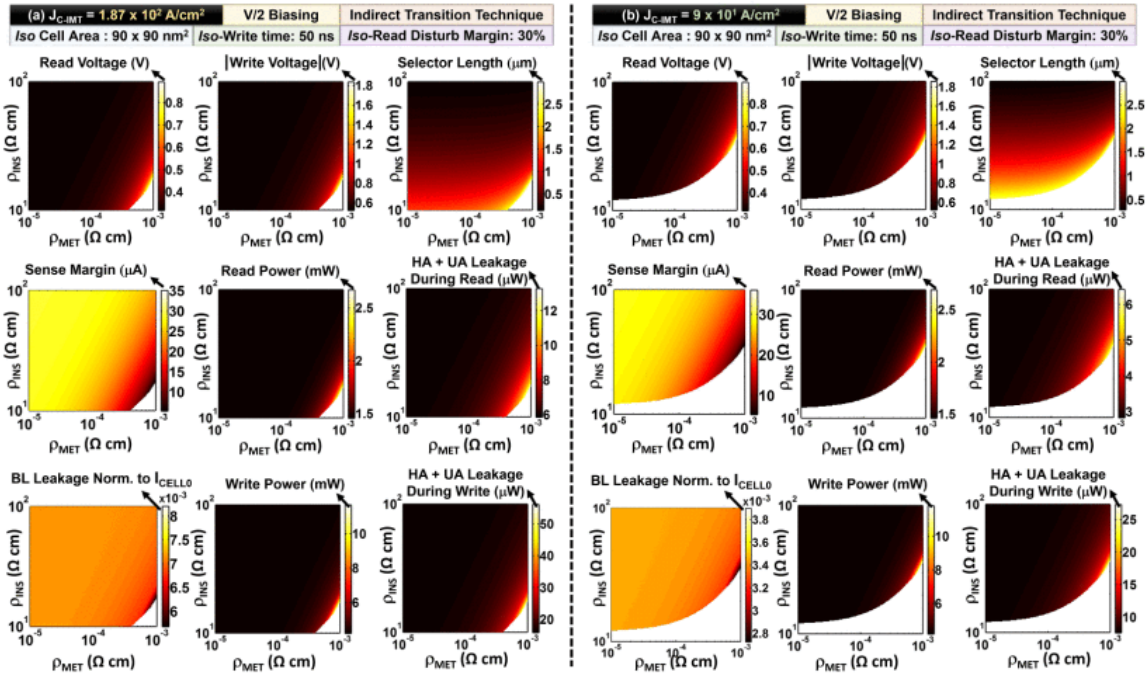


Fig. 4.16 Material space analysis for the PTM based selectors showing the dependence of read voltage, write voltage, selector length, sense margin, total read power, total leakage in the half-accessed/unaccessed (HA+UA) cells during read, bit-line leakage (normalized to read current), total write power and total leakage in the half-accessed/unaccessed (HA+UA) cells during write on the resistivity of the functional oxide in the metallic and insulating states (ρ_{MET} and ρ_{INS}) for (a) $J_{C\text{-}IMT}$ = 1.87x10^2 A/cm^2 and (b) $J_{C\text{-}IMT}$ = 9x10^1 A/cm^2 . The analysis is performed at *iso*-write time and iso-area for V/2 scheme and indirect transition.

and selector lengths increase to very large values. However, for high ρ_{INS} and low ρ_{MET}, near/sub-1 V operation and sub-500 nm selector lengths can be achieved. An important trend in Fig. 4.16 is that reduction in $J_{C\text{-}IMT}$ increases the infeasible region (Fig. 4.16 (b)), which is consistent with the figure of merit in (4.13-a). The array metric values in the common feasible regions are similar for the two values of $J_{C\text{-}IMT}$. The plots in Fig. 4.16 can be used to place various PTMs in the materials space and evaluate their array-level implications. Such plots can also be instrumental in guiding the material exploration of PTMs to meet power-performance-robustness targets for a cross-point memory.

4.9 Summary

In this chapter, we analyzed the design of cross-point arrays employing PTMs as selectors. We presented the design constraints that need to be satisfied for proper operation of the array and discussed their key role in two design aspects: (a) defining the design space for the selector material and (b) co-optimization of the selector length with read and write voltages. We established figures of merit for the selector material (*viz.* $\frac{\rho_{INS} J_{CIMT}}{\rho_{MET}}$ and $J_{C\text{-}MIT}$) and provided simple tests to determine whether a functional oxide is suitable to be used as a selector in a cross-point array. We also defined the feasible range for the selector length and the corresponding read/write voltages, which set the limit on the array metrics that can be achieved with a particular functional oxide. We compared the feasible regions for V/2 and V/3 schemes and showed a larger operating region for the latter at the cost of increase in the leakage. We also performed a comparative analysis of the direct and indirect transitioning scheme and discussed the impact of an additional constraint in the former technique on the feasible design space. We showed that single crystal VO_2 is suitable as a selector for spin-based cross-point memories, if indirect transitioning scheme is employed. For the direct transitioning, SC-VO_2 becomes infeasible due to low $J_{C\text{-}MIT}$. In contrast, Cu-doped HfO_2 showed no feasible regions for either of the transitioning schemes for the memories considered and therefore, requires further improvement, especially with regard to the reduction in its metallic state resistivity. We also performed a material space analysis for the PTMs, establishing the power, performance and robustness metrics as a function of the selector parameters. Our analysis suggests that the best array power-performance-robustness is achieved for high insulating state resistivity and low metallic state resistivity. With a better understanding of these materials in the future, other aspects of cross-point memory design and selector material selection can be added to the analysis presented in this chapter.

5. COMPUTATIONALLY EFFICIENT COMPACT MODEL FOR LEAKAGE ANALYSIS IN CROSS-POINT ARRAY

5.1 Introduction

Humungous growth in digital data from a multitude of sources necessitates reliable and robust memory storage. Through decades of innovation and evolution, several types of memory technologies and architectures have been engineered. With an advent of systems demanding tight power budget such as mobile/wearable electronics, energy scavenging systems and implantable devices, significant interest has been drawn towards non-volatile memory technologies, which allow complete shut-down of power supply in stand-by mode [131], [135], [154], [155]. In addition to *zero* stand-by leakage, such memories offer a promise of high integration density. However, standard memory architectures [156] cannot harness the full density benefits offered by non-volatile memory devices due to a much larger footprint of the access transistor and the contact pitches required in a three-terminal cell design [106], [117]. As discussed in the previous chapter, cross-point array architecture (Fig. 5.1 (a)) [146], [157], [158] is a cutting-edge technique to pack memory cells in a smaller area. In chapter 5, we discussed the structure of a cross-point array with V/2 and V/3 biasing schemes (Fig. 5.1 (b)). Recalling our discussion, selectors with extremely non-linear *I-V* characteristics are used (instead of access transistors) in cross-point array. We discussed the design methodology and constraints associated with PTM based selectors in such arrays. However, one aspect of the cross-point array requires special attention. This special topic is the assessment of array leakage, which is the focus of this chapter.

Due to presence of sneak paths (Fig. 5.1 (a)), the conventional biasing schemes of cross-point array generate leakage current through the half-accessed row (HAR), half-accessed column (HAC) and even through un-accessed (UA) cells (in case of *V/3* biasing). These leakage components contribute to power drainage and reduce robustness of current sensing during read operation [109]. Hence, accurate modeling and prediction of the array leakage is extremely important. However, the conventional process [159], [160] to calculate array leakage requires extensive computational effort as the entire array needs to be simulated

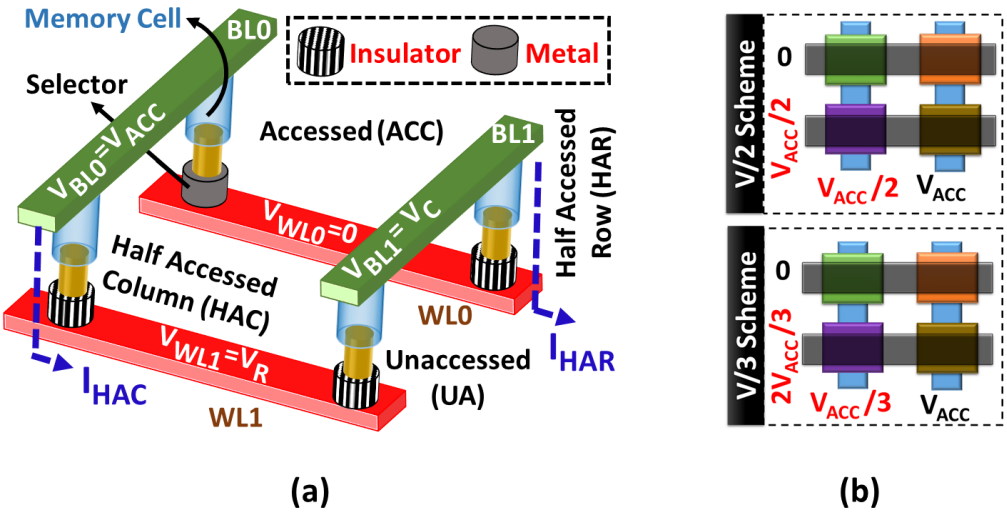


Fig. 5.1 (a) Typical cross-point memory array structures. Scenario of two types of biasing schemes – (b) V/2 and (c) V/3 used for biasing a cross-point array. V_{ACC} represents read/write voltage.

for sufficiently accurate estimation. Such extensive simulation is mandated by the degradation of supply voltage across the array due to resistive interconnect drop (discussed in detail later). In this chapter, we present a compact model that performs accurate computation of array leakage without simulating the entire array. The model is valid for designs that use threshold-switches (*e.g.* PTM) [21] as selector elements. We implement different sizes of cross-point array in SPICE simulator and run rigorous simulation to obtain leakage current and power. We then crosscheck the obtained results with those calculated from our compact model and prove the validity of our approach. We also evaluate the accuracy of the model for different selector resistance, interconnect resistance and access voltages.

5.2 Modeling Methodology

To discuss the methodology for our proposed model, we first explore and identify the design variables associated with the cross-point array. During regular operation, a block of memory cells is selected for read/write. This block of accessed cells in a cross-point array concurrently yields HAR, HAC and UA cells (Fig. 5.2 (a)). Distributed interconnect

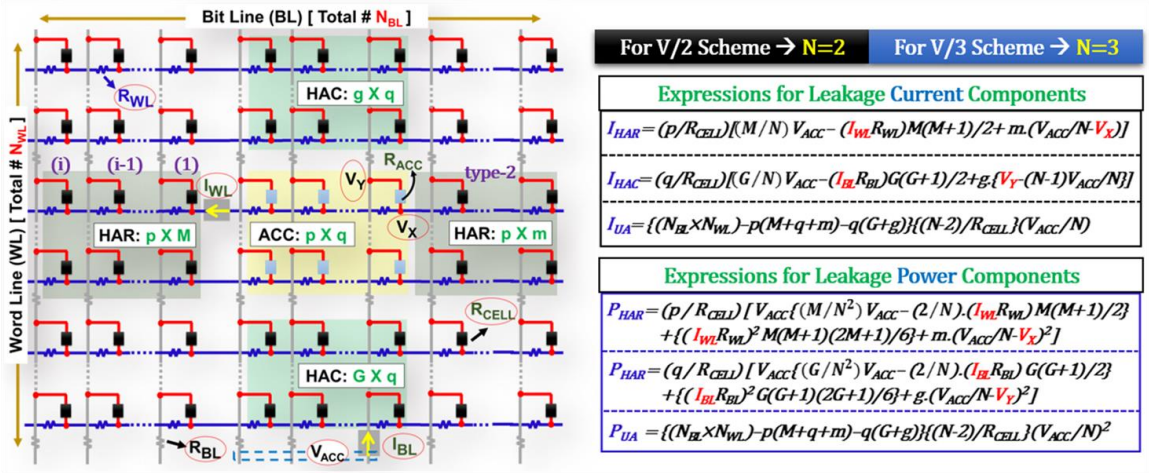


Fig. 5.2 (a) Detailed illustration of different variables used for modeling the leakage in a cross-point array. (b) The governing closed-form equations of the compact model.

resistances throughout the BLs and WLs produce gradients in supply voltage across the array due to the read/write current and therefore, each cell in the array produces different amount of leakage. Hence, for accurate estimation, traditionally the entire array is implemented and leakage through each cell is monitored. For larger size of array, this demands extensive computation. On the contrary, in our approach, we only need to simulate the accessed block, which is typically a tiny fraction of the entire array. We express the block of accessed cells as an equivalent circuit (Fig. 5.3) with distributed per cell interconnect resistances (R_{BL} and R_{WL}). We assume the resistances of the HAR and HAC cells to be significantly high compared to R_{BL} and R_{WL} (due to having selectors in OFF state). Therefore, the effect of HAR and HAC cells are coupled to the accessed block through lumped resistances R_{HAC} and R_{HAR} (Fig. 5.3), whose values are functions of the location of the accessed block.

We simulate this simplified equivalent circuit in SPICE (instead of implementing and simulating entire array) to obtain four parameters (I_{BL}, I_{WL}, V_X and V_Y - in Fig. 5.3). We use I_{BL}, I_{WL}, V_X, V_Y, R_{BL} and R_{WL} to formulate progressions of node voltages across the array and attain their mathematical equivalent to capture effect of voltage gradient. Based on these

Table 5.1 Sample of the Derivation Process

$P_{HAR\,(1)} = (V_{ACC}/N - I_{WL} \times R_{WL})^2 / R_{CELL}$ ..... (1)	$I_{HAR\,(1)} = (V_{ACC}/N - I_{WL} \times R_{WL}) / R_{CELL}$ ..... (1)
$P_{HAR\,(2)} = (V_{ACC}/N - 2 \times I_{WL} \times R_{WL})^2 / R_{CELL}$ ..... (2)	$I_{HAR\,(2)} = (V_{ACC}/N - 2 \times I_{WL} \times R_{WL}) / R_{CELL}$ ..... (2)
…….....	…….....
$P_{HAR\,(I)} = (V_{ACC}/N - I \times I_{WL} \times R_{WL})^2 / R_{CELL}$ ..... (I)	$I_{HAR\,(i)} = (V_{ACC}/N - i \times I_{WL} \times R_{WL}) / R_{CELL}$ ..... (i)
$P_{HAR\text{-}TYPE\text{-}2} = (V_{ACC}/N - V_X)^2 / R_{CELL}$	$I_{HAR\text{-}TYPE\text{-}2} = (V_{ACC}/N - V_X) / R_{CELL}$

$$P_{HAR\,(TOTAL)} = P \times [\{\sum_{i=1}^{M} P_{HAR\,(I)}\} + M \times P_{HAR\text{-}TYPE\text{-}2}]$$

$$= P \times [\{\sum_{i=1}^{M} (V_{ACC}/N - I \times I_{WL} \times R_{WL})^2 / R_{CELL}\} + M \times (V_{ACC}/N - V_X)^2 / R_{CELL}]$$

$$= (P / R_{CELL}) \times [\{\sum_{i=1}^{M} (V_{ACC}^2/N^2 - 2 \times I \times I_{WL} \times R_{WL} + I^2 \times I_{WL}^2 \times R_{WL}^2)\} + M \times (V_{ACC}/N - V_X)^2]$$

$$= (P/R_{CELL})\,[V_{ACC}\{(M/N)^2 V_{ACC} - (2/N).\,(I_{WL}R_{WL})M(M+1)/2\} + \{(I_{WL}R_{WL})^2 M(M+1)(2M+1)/6\} + M.\,(V_{ACC}/N - V_X)^2]$$

$$I_{HAR\,(TOTAL)} = P \times [\{\sum_{i=1}^{M} I_{HAR\,(I)}\} + M \times I_{HAR\text{-}TYPE\text{-}2}]$$

$$= P \times [\{\sum_{i=1}^{M} (V_{ACC}/N - I \times I_{WL} \times R_{WL}) / R_{CELL}\} + M \times (V_{ACC}/N - V_X) / R_{CELL}]$$

$$= (P/R_{CELL})\,[(M/N)\,V_{ACC} - (I_{WL}R_{WL})M(M+1)/2 + M.\,(V_{ACC}/N - V_X)]$$

parameters along with several other array, cell and material level constants (Fig. 5.2 (a)), we deduce closed form expressions (Fig. 5.2 (b)) for the leakage current and power (P_{HAR}, $P_{HAC,}$ P_{UA}, I_{HAR} and I_{HAC}) considering a general (V/N) biasing scheme. Here, N= 2 and 3 represent V/2 and V/3 biasing schemes respectively. The detailed steps for the deduction of these expressions (Fig. 5.2 (b)) have been shown in Table 5.1.

To avoid repetition, we only show the steps to calculate I_{HAR} and P_{HAR}. To deduce I_{HAC} and $P_{HAC,}$ similar steps can be carried out. The end expressions for all of these components have been shown in Fig. 5.2 (b). This approach leads to substantial reduction in computation complexity. As mentioned earlier, our compact model for leakage is suited for arrays with threshold switch type selectors [21]. Our model is general with respect to materials as long as the threshold switching behavior is involved. To justify the utility of the proposed approach, we implement a simulation framework based on both conventional and proposed techniques of computation. We discuss that in the next section.

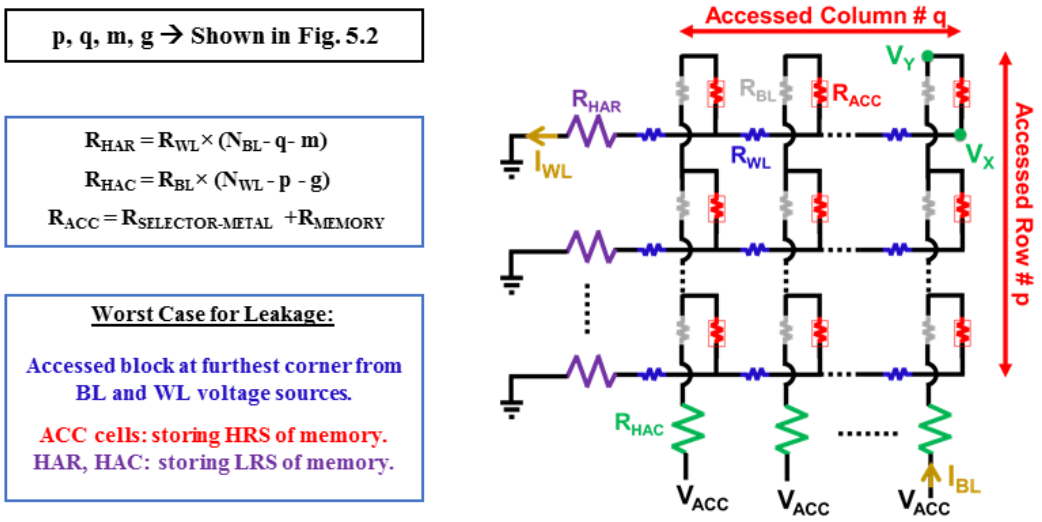


Fig. 5.3 Equivalent circuit for the p×q accessed block in the array (shown in Fig. 5.2). The resistances of the HAR and HAC cells are expressed using two equivalent resistances (R_{HAR} and R_{HAC}).

5.3 Description of Simulation Framework

To validate the results obtained from our model, we implement full cross-point array frameworks of different sizes (16×16, 32×32, 64×64, 128×128 and 256×256) in SPICE. We choose magnetic tunnel junction (MTJ) as memory element and use a compact model from [101] to obtain its properties. In addition, we use the SPICE model for threshold switching PTM based selectors (discussed before) [109]. This model considers constant resistances of the selector in metallic and insulating states and captures the state transition as a function of electrical stimuli. The selector model coupled with MTJ model forms the basis for a memory cell in the cross-point array. Several of such cells are coupled to form larger cub-circuit blocks and eventually the entire array. The parameters used in the proposed compact model and for the subsequent simulations are shown in Table-5.2.

5.4 Analysis and Verification

To keep consistency in all our analyses, we consider a 1×8 accessed block (except in Fig. 5.8) at the furthest corner of the array from the BL/WL drivers. For the analysis, we focus

on *V/2* biasing (although our model is applicable for *V/3* biasing scheme as well). We calculate total leakage power and current through the HA cells for different sizes of array (Fig. 5.4) (Note, in a *V/2* scheme, no leakage occurs in UA cells). The results attained from the compact model are in excellent agreement with values obtained through rigorous simulations. Next, we fix the size of the array to 256×256 and examine the effectiveness of the model in capturing impact of major design variables.

Table 5.2 Default Simulation Parameters and Specifications

Memory Element	Magnetic Tunnel Junction (MTJ). $T_{OX\text{-}MTJ}$ = 1.1 nm, D_{MTJ} =45 nm, H_{SAT}= 80 KA/m
Selector Type	Insulator ↔ Metal Transitioning Threshold Switch Single Crystal VO_2 : $\rho_{MET} \approx 5x10^{-6}$ Ω m, $\rho_{INS} \approx 0.8$ Ω m
Interconnect	Copper (Cu)

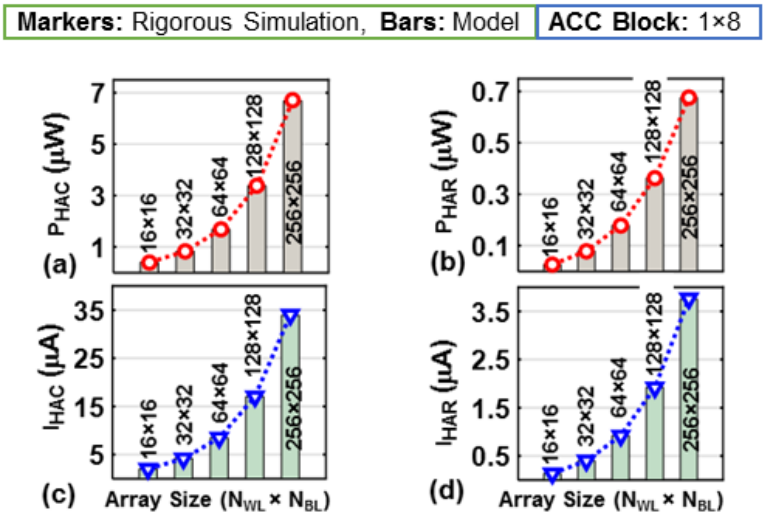


Fig. 5.4 The leakage power (a, b) and current (c, d) for HAR and HAC in different sizes of array. The values obtained from the compact model matches accurately with those obtained through rigorous simulation of complete array (V/2 biasing scheme).

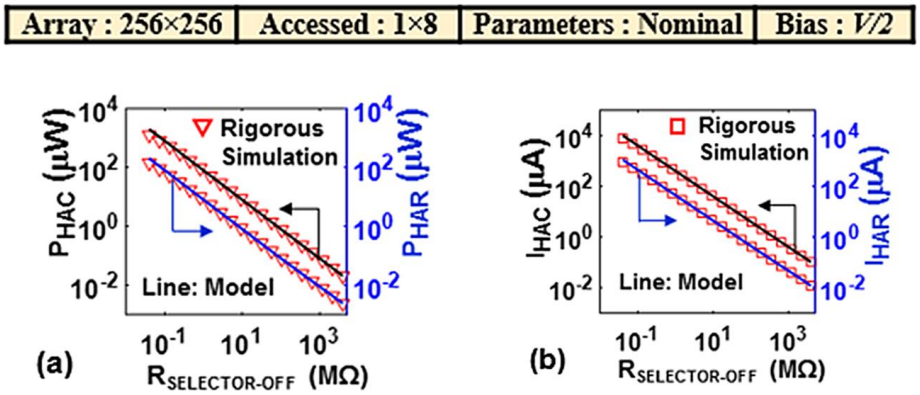


Fig. 5.5 The compact model precisely captures the effect of $R_{SELECTOR\text{-}OFF}$ on (a) leakage power and (b) leakage current of half accessed (HA) cells.

5.4.1 Impact of OFF State Resistance of Selector

Higher OFF state resistance of the selector ($R_{SELECTOR\text{-}OFF}$) reduces leakage power and current significantly (Fig. 5.5). To obtain $I_{HAR} < 1$ μA, $R_{SELECTOR\text{-}OFF}$ needs to be over 50 MΩ. The model provides accurate (~99%) estimation of leakage if $R_{SELECTOR\text{-}OFF} > 1$ MΩ. For very low $R_{SELECTOR\text{-}OFF}$ (< 0.2 MΩ), we observe up to 10% mismatch in estimation**.** The reason for that is, lower $R_{SELECTOR\text{-}OFF}$ allows a portion of I_{WL} to flow through the HAR cells. So, the assumption of considering lumped R_{WL}(see Fig. 5.3) becomes less accurate. Note,

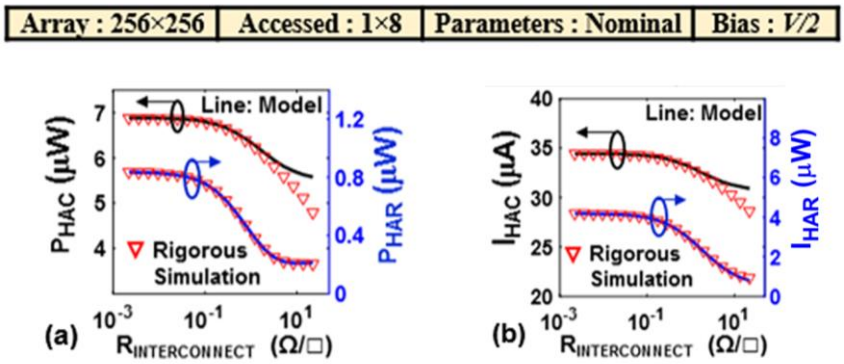


Fig. 5.6 The distributed interconnect resistance model considered to formulate the closed-form equations (in Fig. 5.2) yields accurate results up to $R_{INTERCONNECT} \approx 5$ Ω/□.

a useful selector device is expected to have large OFF state resistance. Therefore, the model has excellent precision for practical range of values for $R_{SELECTOR\text{-}OFF}$.

5.4.2 Impact of Interconnect Resistance

Similar analysis with sheet resistance of interconnect (Fig. 5.6) shows that, our model can provide accurate results with up to 5 Ω/□ sheet resistance. The interconnect resistance reduces the accuracy of approximation in our model only if it becomes comparable to the metallic state resistance (LRS) of the *selector*. In such scenario, using lumped resistance technique to calculate R_{HAC} and R_{HAR} becomes less accurate.

5.4.3 Impact of Access Voltage

The array leakage current and power increases with access voltage (Fig. 5.7). The leakage current through HAR is significantly low compared to that through HAC cells. This is due to using 1×8 accessed block, which yields more HAC than HAR cells. For access voltage of 0.4 V (considered for read), leakage current through HAR cells is ~4 μA as opposed to that through HAC cells being ~40 μA. Most importantly, the compact model provides a close match to the rigorous array level simulations for different levels of access voltages (Fig. 5.7).

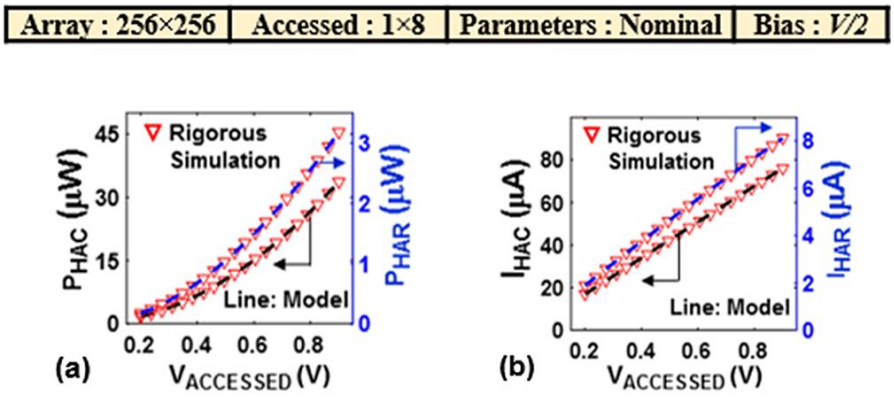


Fig. 5.7 Leakage (a) power and (b) current of the HA cells increases with access voltage ($V_{ACCESSED}$). For all values of $V_{ACCESSED}$, the compact model provides accurate results.

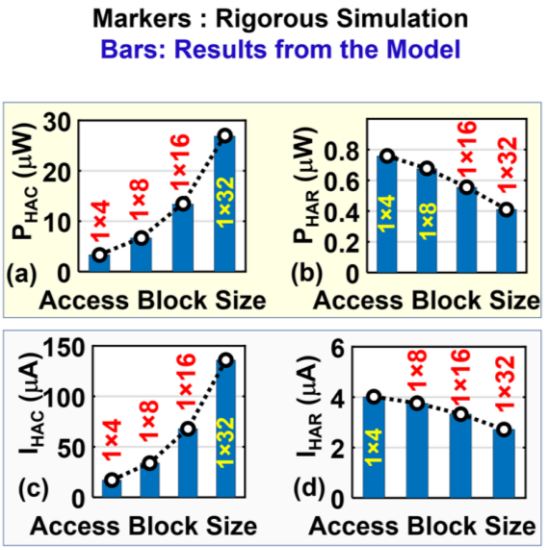


Fig. 5.8 Leakage (a, b) power and (c, d) current of the HA cells is a function of the size of the accessed block. If the number of rows in an accessed block increases with fixed number of column, P_{HAC} and I_{HAC} increase, whereas P_{HAR} and I_{HAR} decrease.

5.4.4 Effect of Size of the Accessed Block

Finally, we examine the generality of the model by cross-checking the leakage for different sizes of accessed block. We consider 1×4, 1×8, 1×16 and 1×32 accessed blocks. As shown in Fig. 5.8, leakage power and current through HAC cells increases for larger accessed blocks because of the increased number of columns. Concurrently, leakage through HAR cells reduce mainly because the number of HAR cells reduces with increased sizes of accessed block. Moreover, the increased number of columns sink in more current from the BL and add them to yield larger current in the accessed WL. As a result, a larger voltage gradient occurs throughout the WL, which leads to decreased effective voltage across the HAR cells. That also contributes to reducing the leakage in HAR cells. Assuring to note, the model captures the trends well and provides accurate results for different sizes of accessed blocks.

5.5 Summary

We presented a computationally efficient approach to model the total array leakage of cross-point array averting the need for rigorous and intensive simulation of entire array. We provided closed form mathematical expressions for leakage and explained the derivation methodologies. We analyzed and verified the validity of the model by crosschecking with results from conventional rigorous array simulations. The model showed excellent matching (~99% accuracy) with rigorous simulations for different array sizes (16×16 through 256×256). We tested the model for various ranges of selector OFF resistance (0.1 MΩ to 1 GΩ), interconnect resistance (1 mΩ/□ to 10 Ω/□) and access voltage (0.2 V to 1 V). The test results from the model show accurate response in comparison with those obtained from intensive array simulations.

6. HYBRID PHASE TRANSITION FET (HYPER-FET): DEVICE-CIRCUIT CO-DESIGN

6.1 Introduction

In the previous chapters, we explored the possible applications of PTMs to enhance spin based memory devices and analyzed their implications as selectors in cross-point memory array. This chapter focuses on a completely different domain of application for phase transition materials (PTM). The unique electronic properties of the PTMs can be utilized to overcome the fundamental Boltzmann limit [30], [161], which pertains to conventional CMOS transistors. With a growing demand for portable, wearable and implantable electronic systems, a strong emphasis is being placed on the design of ultra-low power devices and circuits. To that effect, considerable effort has been rendered to achieve 'steep switching' in transistors to go below the 60mV/decade limit (Boltzmann limit) for the sub-threshold swing associated with standard MOSFETs (at room temperature). Hybrid-phase-transition FET (Hyper-FET) is one of the most promising and recent inclusions to the family of steep switching devices. Prototypical demonstration of Hyper-FET was first presented in [30] and the first monolithic integration of PTM on top of the source contact was reported in [22]. Subsequently, several other versions of this device have been fabricated [21], [23], [24]. In literature, this device is also mentioned as 'Phase-FET', to highlight the major role of the PTM in its principle of operation.

Hyper-FET achieves steep switching by utilizing the abrupt insulator-metal transitions in a PTM, integrated in series with the source of a host transistor [28], [30]. This device also achieves a boost in the ratio of ON and OFF currents (I_{ON} and I_{OFF}), compared with standard/baseline transistor. Along with these desired features, Hyper-FET exhibits hysteresis in its transfer and output characteristics. Hysteresis and abrupt switching lead to unconventional characteristics and therefore, Hyper-FETs are far from being drop-in replacement for FinFETs/MOSFETs. The unique features of Hyper-FETs necessitate rigorous evaluation of the device design coupled with the analysis of the circuit implications. In addition, the influence of different parameters of the PTM needs to be examined in correlation with circuit level performance; to establish the targets for material

down-selection. This chapter presents a detailed analysis of Hyper-FETs from the perspective of device design and optimization. We also explore the material space for optimal operation and provide details on Hyper-FET based circuit design.

6.2 Principle of Hyper-FET Operation

The basic concept of Hyper-FET operation is to enhance the switching characteristics of a transistor by utilizing the orders of magnitude difference in ρ_{INS} and ρ_{MET} and the abrupt IMT and MIT of the PTM. The circuit schematics and device structure of the Hyper-FET is shown in Fig. 6.1 (a, b). The PTM is connected to the source of a conventional FET and the operation of the hybrid device is governed by the characteristics of the transistor as well as the PTM. Fig. 6.1 (c) shows typical transfer characteristics for Hyper-FET. In the OFF state of the device, the small current ($I_D < I_{C\text{-}IMT}$) flowing through the series combination of the FET and the PTM ensures that the material remains in insulating state. Hyper-FET with an insulating PTM connected to the source terminal is essentially a transistor source degenerated by a very high resistance. Hence, insulating PTM leads to reduction in the gate-to-source voltage ($V_{GS'}$) as well as the drain-to-source voltage ($V_{DS'}$) of the host FET (Fig. 6.1 (a)), thereby significantly reducing the OFF current (I_{OFF}). As the applied gate-to-source voltage (V_{GS}) is increased, current through the transistor and the PTM increases. When the current becomes equal to $I_{C\text{-}IMT}$, the PTM abruptly switches to the metallic state at $V_{GS} = V_{GS\text{-}IMT}$ (Fig. 6.1 (c)). The abrupt reduction in resistance of the PTM during IMT

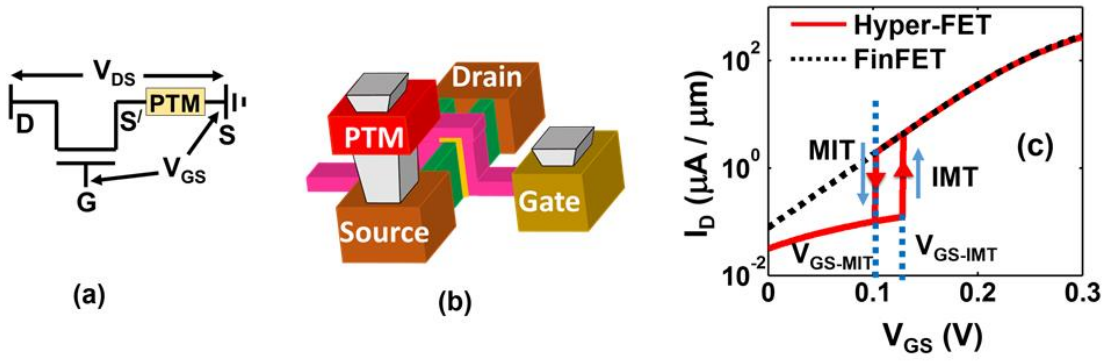


Fig. 6.1 (a) Schematic and (b) 3D structure of Hyper-FET. (c) Typical transfer characteristics Hyper-FET (compared with the standard 14 nm FinFET).

leads to a sharp increase in the current, as the transistor gets source-degenerated only with a small metallic resistance. As a result, the Hyper-FET abruptly turns ON with a steep sub-threshold slope. Due to the small metallic state resistance of the PTM, the ON current of Hyper-FET in only negligibly reduced in comparison to the conventional FET. Hence, with proper design (discussed later), PTM of the Hyper-FET operates in metallic state when the FET is ON ($V_{GS} = V_{DD}$, $V_{DS} = V_{DD}$) and in the insulating phase during the OFF state. This leads to an increase in the ratio of ON current (I_{ON}) and OFF current (I_{OFF}). Another important point to note is that, due to the hysteretic behavior of PTM, the transfer characteristics of Hyper-FETs also exhibit hysteresis (Fig. 6.1 (c)). As V_{GS} is reduced from V_{DD} (supply voltage) to zero, the current reduces and as it goes below $I_{C\text{-}MIT}$, the PTM undergoes MIT and turns insulating at $V_{GS} = V_{GS\text{-}MIT} < V_{GS\text{-}IMT}$. We discuss the transfer and output characteristics of this device in detail in the next few sections. We utilize a simulation-based approach to develop insights on device and circuit level characteristics. We begin by describing the simulation framework used for this work and then move on to the subsequent discussions.

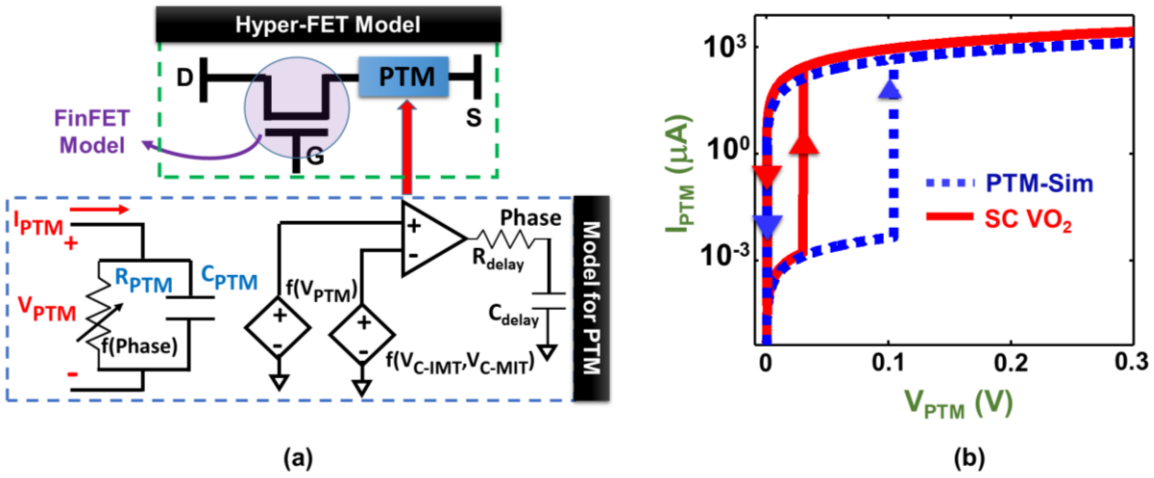


Fig. 6.2 (a) Behavioral representation of different components of the modeling framework for Hyper-FET. (b) Current-voltage (*I-V*) characteristics of the model material (PTM-Sim) used for simulations. The *I-V* characteristics of single crystal VO_2 has also been shown for comparison.

6.3 Modeling and Simulation Framework for Hyper-FET

To explain the device operation and circuit implications of Hyper-FETs, we perform simulation-based analyses employing 14 nm FinFET [162] as the baseline technology. A circuit compatible SPICE model for PTM has been used for the simulations performed in this work (Fig. 6.2 (a)) [28], [79]. The model represents the phenomenological behavior of the PTM using a voltage-dependent resistor (R_{PTM}) in parallel with a capacitor (C_{PTM}). The model monitors the current through the PTM during circuit operation and triggers phase transition depending on the parameterized critical values of switching threshold currents. The voltage across the PTM (V_{PTM}) is compared to the critical levels ($V_{C\text{-}IMT}$ and $V_{C\text{-}MIT}$) to decide on the *phase* (and thereby R_{PTM}). Hence, the resistance switching behavior of the PTM is self-consistently invoked in correlation with the biasing scenario. We use a separate *R-C* network to model the delay associated with the phase transition. We couple PTM and FinFET models [103] in SPICE to perform the device and circuit analysis. The nominal cross-sectional area of the PTM (A_{PTM}) is determined by the design rules for contact formation [162] to ensure the feasibility of monolithic integration. A list of nominal values of the relevant simulation parameters and important assumptions is provided in Table 6.1.

Table 6.1 Nominal Simulation Parameters

Device Level Specifications	
Technology, Fin Pitch	14nm FinFET, 42nm
Number of Fins	2
Phase transition material	PTM-Sim
Dimensions (L_{PTM} , A_{PTM})	20nm, 42x21nm^2 (fin pitch x 3λ)
λ = ½ of the minimum feature size	
Material Parameters for PTM-Sim	
Resistivity of metallic state (ρ_{MET})	1x10^{-3} Ω-cm
Resistivity of insulating state (ρ_{INS})	100 Ω-cm
Critical current density for MIT ($J_{C\text{-}MIT}$)	8x10^3 A/cm^2
Critical current density for IMT ($J_{C\text{-}IMT}$)	5.2x10^2 A/cm^2

An important point to note is that the family of PTMs is quite rich with materials (e.g. VO_2, V_2O_3, V_2O_4, TiO, Ti_2O_3, Cu-doped HfO_2, doped chalcogenide etc. [30], [67], [69], [71]–[73]. These materials exhibit a wide range of resistivity, hysteresis and thermal stability. New PTMs are still being explored and novel approaches (such as using strain) have been reported to tailor their properties [75], [125], [130]. We perform our subsequent analyses considering a model material (termed as *PTM-Sim*) with resistivity ratio and critical currents suitable for Hyper-FET operation (Fig. 6.2 (b)). Note that the critical currents associated with IMT/MIT and the resistivity ratio are of the same order of magnitude compared to single crystal VO_2 [143]. The choice of the nominal parameters for *PTM-Sim* (shown in Table 6.1) enables us to achieve sufficient I_{ON}/I_{OFF} and hysteresis in Hyper-FETs to reveal the important effects in device-circuit operation. At a later stage of our discussion, we will explore ranges of material parameters to make the analysis more general.

6.4 Constraints for Material Selection and Design

As discussed in section 6.2, the Hyper-FET operation leverages high insulating state resistivity (ρ_{INS}) and low metallic state resistivity (ρ_{MET}) of the PTM to achieve higher I_{ON}-I_{OFF} ratio. However, the gain in I_{ON}/I_{OFF} as well as the functionality of the Hyper-FET strongly depends on the relative resistance of the transistor and PTM as well as the current thresholds for IMT and MIT. In this section, we discuss the constraints on the properties of the PTM to achieve proper Hyper-FET operation.

Higher ρ_{INS} reduces the OFF current and lower ρ_{MET} reduces the penalty in the ON current. Generally, the resistance of the PTM in the insulating state must be comparable to that of the host FET in the OFF state. Otherwise, the reduction in the OFF current will be insignificant since the voltage at *S'* (Fig. 6.1(a)) will be ~ equal to that at *S*, leading to only a mild source degeneration of the FET. Moreover, the resistance of the PTM in the metallic state must be much less than the ON state resistance of the transistor so that the ON current of the Hyper-FET is comparable to that of the host FET. Therefore, PTMs with the resistivity ratio ρ_{INS}/ρ_{MET} larger than the inherent I_{ON}-I_{OFF} ratio of the standard FET can provide gain in the I_{ON}-I_{OFF} ratio of the Hyper-FET. Fig. 6.3 (a, b) presents the achievable

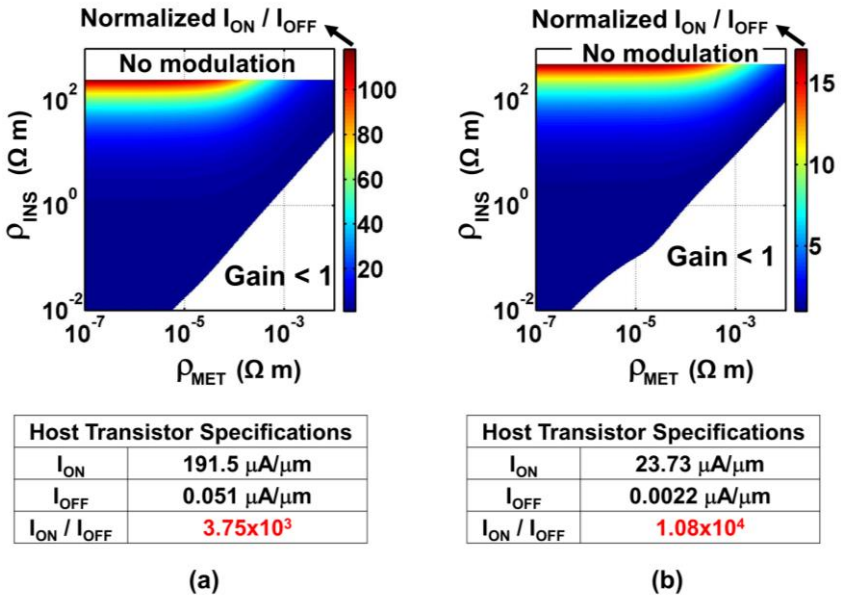


Fig. 6.3 Mapping of $I_{ON} - I_{OFF}$ ratio of Hyper-FET with a host transistor having (a) low and (b) high I_{ON}/I_{OFF}. The values of the I_{ON}/I_{OFF} of the Hyper-FETs have been normalized to that of their corresponding host transistors.

I_{ON} / I_{OFF} in a Hyper-FET, showing larger gains for lower ρ_{MET} and higher ρ_{INS} (up to a certain limit discussed later). If ρ_{INS}/ρ_{MET} is not sufficiently high, I_{ON}/I_{OFF} of the Hyper-FET may be degraded with respect to the host transistor. The region representing the combinations of ρ_{INS} and ρ_{MET} corresponding to gain > 1, shrinks as the inherent I_{ON}/I_{OFF} of the host transistor increases (Fig. 6.3 (b)). Hence, as a primary comment, materials with high ρ_{INS} and lower ρ_{MET} are preferable for Hyper-FET operation. But, ρ_{INS} cannot be arbitrarily large. Moreover, choosing PTMs with high ρ_{INS}/ρ_{MET} is not a sufficient condition for optimum Hyper-FET design. The explanations for both these comments are related to the constraints associated with critical currents for IMT and MIT, as discussed next.

In addition to achieving high ρ_{INS}/ρ_{MET}, it is crucial to ensure that the PTM undergoes phase transitions within the voltage window of operation ($0 < V_{GS} < V_{DD}$ and $0 < V_{DS} < V_{DD}$). Otherwise, PTM will always be in insulating state throughout the entire operating voltage range and thereby disturb normal transistor operation. This necessitates an analysis to find the allowable critical currents of switching ($I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$) for a particular design

specification. We perform this analysis considering a FinFET with a constant series resistor at the source terminal, representing the insulating/metallic PTM (Fig. 6.4 (a) / (b) respectively). Let us first consider the series resistance to be equal to that of a PTM in insulating state. For this transistor configuration, I_D at V_{GS} = 0 and I_D at V_{GS} = V_{DD} essentially represent the lower and upper bounds for $I_{C\text{-}IMT}$ within the respective voltage ranges (Fig. 6.4 (c)). To make sure that PTM undergoes IMT within this current limit, we can either choose a material with appropriate $J_{C\text{-}IMT}$ or properly design the cross-sectional area of a given PTM. In this section, we focus on the former approach. Similar analysis for the constraints to ensure MIT is shown in Fig. 6.4 (b). Here, a transistor has been considered with a low resistance connected to the source representing the metallic state of PTM. In this case, I_D at V_{GS} = 0 and I_D at V_{GS} = V_{DD} set the limit for allowable $I_{C\text{-}MIT}$. Outside this limit, PTM fails to undergo MIT and the Hyper-FET is unable to harness the benefit of higher I_{ON}-I_{OFF} ratio.

The ranges of $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$, which ensure proper phase transition in the PTM during the device operation depends on ρ_{INS}, ρ_{MET} and the intrinsic resistance of the base transistor. We first consider the impact of the resistivity of the PTM (ρ_{INS} and ρ_{MET}). Fig. 6.4 (d) shows the limit of $I_{C\text{-}MIT}$ assuming two different values of metallic state resistivity and it is clear that higher metallic state resistivity reduces the range of $I_{C\text{-}MIT}$. Fig. 6.4 (c) shows $I_{C\text{-}IMT}$ ranges for two different values of insulating state resistivity. It can be observed that the range to achieve IMT is much smaller than that for MIT (in Fig. 6.4 (c, d)). Moreover, an increase in ρ_{INS} reduces the modulation of the current with V_{GS}, thereby shrinking the range of $I_{C\text{-}IMT}$ for proper device operation. Our analysis shows that for ρ_{INS} > 20000 Ω.cm, the range of $I_{C\text{-}IMT}$ becomes so small that it may not be suitable for a practical design. This is because, for very high insulating phase resistance (R_{INS}) of the PTM, the resistance of the Hyper-FET is dominated by the PTM even during the OFF state. As a result, the change in the resistance of the FET with V_{GS} is not reflected during the Hyper-FET operation. Hence, materials with ρ_{INS} much greater than the OFF state resistance of the FET are not suitable for Hyper-FET design due to insufficient modulation of current with V_{GS}. The range for such values of ρ_{INS} has been marked to have no modulation in Fig. 6.3. On the other hand, if ρ_{INS} is too less, no gain in I_{ON}-I_{OFF} ratio is achieved (see Fig. 6.3), as discussed before.

While ρ_{INS} and ρ_{MET} are vital aspects in determining the constraints for $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$, the base transistor also plays an important role for the same. The trends shown in Figs. 6.4 (c), (d) correspond to a host transistor with I_{OFF} = 51 nA/μm, whereas those in Figs. 6.4 (e), (f) are for a transistor with lower I_{OFF} (2.2 nA/μm). Since the transistor with lower I_{OFF} has higher inherent resistance, it exhibits relatively less sensitivity towards the PTM resistance. Therefore, the reduction in the allowable ranges of critical currents with increase of ρ_{INS}

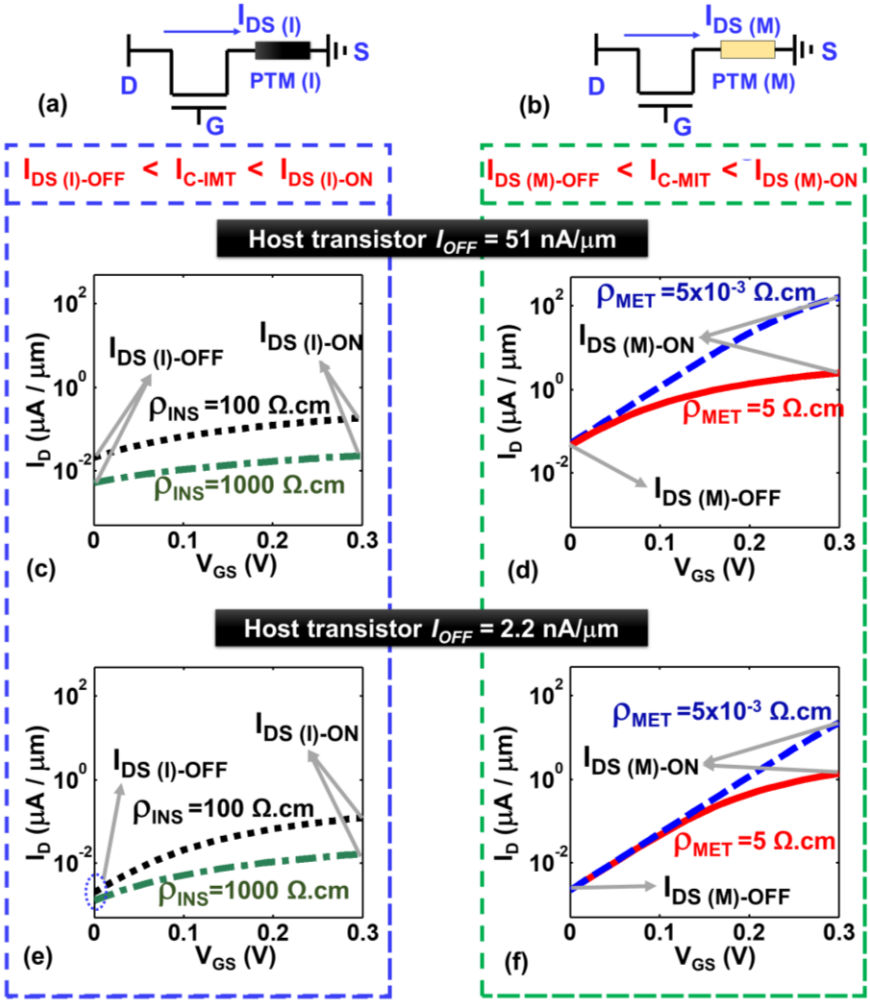


Fig. 6.4 Constraints on critical current level for (c) IMT and (d) MIT phase switching corresponding to a host transistor with I_{OFF} = 0.051 μA/μm. (e - f) Same metrics for a host transistor with lower inherent I_{OFF} (higher OFF resistance). The limits have been obtained considering a constant resistor attached to the source of a standard MOSFET, with resistance equal to (a) insulating and (b) metallic state of PTM.

and ρ_{MET} is lower for a host transistor with inherently lower I_{OFF} (Figs. 6.4 (e) and (f)). Moreover, it can be observed in Fig. 6.4 that the host transistor with lower I_{OFF} necessitates the PTM to have reduced $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT.}$ Essentially, if the host transistor innately has low I_{OFF}, the Hyper-FET will require a PTM with low critical currents for IMT/MIT.

The arguments presented so far can be utilized to explore another interesting possibility. In Fig. 6.1 (c), we presented the transfer characteristics of a Hyper-FET showing the reduction in I_{OFF} with a mild I_{ON} penalty. However, if the OFF state current for the Hyper-FET is matched to the standard FET employing threshold voltage tuning [163], the former will exhibit higher ON current as depicted in Figs. 6.5 (a), (b). In other words, Hyper-FETs can be tailored to provide gain in I_{ON} (therefore higher drive strength) at *iso*-I_{OFF} compared to a standard transistor. It is important to note, that the ranges for $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$ will have to be re-evaluated for *iso*-I_{OFF} condition. The shift of the allowable ranges for $I_{C\text{-}IMT}$ (R1 and R2) and $I_{C\text{-}MIT}$ (R3 and R4) has been illustrated in Figs. 6.5 (c), (d). Observing that R2 < R1 and R4 < R3, we deduce that the design constraints are more stringent at *iso*-I_{OFF}. We perform all our subsequent analysis considering the *iso*-I_{OFF} condition.

6.5 Device Characteristics of Hyper-FET

To begin our discussion in this part, we take a look at the device characteristics from a different perspective. We analyze both the transfer and output characteristics and draw a correlation between them. We first analyze the output characteristics of Hyper-FET (Fig. 6.6 (a)). The PTM operates in insulating state at $V_{DS} = 0$ ($I_D = 0$). With an increase in V_{DS}, drain current (I_D) tends to increase. However, with the PTM being in insulating state, I_D is negligible compared to the standard FET. As V_{DS} is further increased, the PTM transitions into the metallic state as the current reaches $I_{C\text{-}IMT}$. The corresponding V_{DS} ($V_{DS\text{-}IMT}$ in Fig. 6.6 (a)) marks the end of the voltage range for which Hyper-FET does not produce considerable drain current. Now, considering the reverse sweep, reducing V_{DS} reduces I_D and eventually as current drops below $I_{C\text{-}MIT}$, PTM turns insulating again at $V_{DS} = V_{DS\text{-}MIT.}$ Note that $V_{DS\text{-}MIT} \sim 1$ μV and therefore is not visible in Fig. 6.6 (a). We show $V_{DS\text{-}MIT}$ for an illustrative high value of $I_{C\text{-}MIT}$ in Fig. 6.8 (a). In summary, because of having PTM in the insulating state, Hyper-FETs do not turn on in response to low drain bias and may also get

turned "OFF" at non-zero drain bias (especially for high $V_{DS\text{-}MIT}$). So, there exists a range of V_{DS} for which, even with a sufficient V_{GS} bias, the Hyper-FET does not turn "ON". This zone in V_{DS} will be subsequently referred as '*dead zone*'. These '*dead zones*' in output characteristics, especially those defined by MIT are crucial aspects for the design of CMOS circuits. The transfer characteristics at *iso*-I_{OFF} for different V_{DS} are shown in Fig. 6.6 (b). At $V_{DS} = V_{DD}$, the impact of IMT and MIT on the characteristics are similar to that discussed in section 6.2. However, at $V_{DS} = 50$ mV, the PTM never undergoes IMT and the transistor remains in the cut-off mode even at $V_{GS} = V_{DD}$. It is a direct consequence of the *'dead zone'* in the output characteristics. $V_{DS} = 50$ mV actually falls below $V_{DS\text{-}IMT}$ (~100 mV). This adds an apparent concern about device operation. However, our analysis shows that, this aspect does not disrupt operation of digital logic circuits (discussed later).

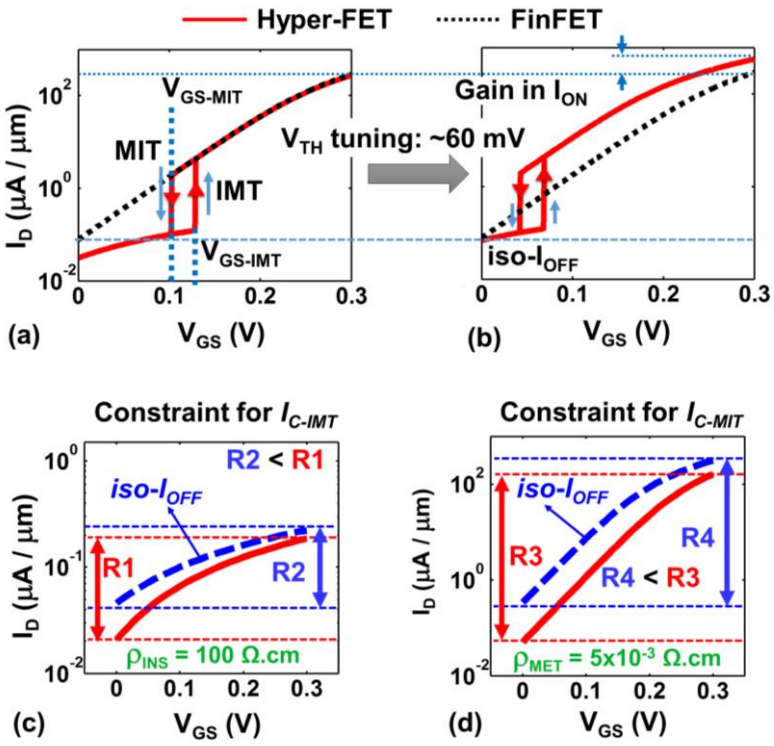


Fig. 6.5 (a) Transfer characteristics of Hyper-FET (b) At matched I_{OFF} condition (possibly through threshold voltage tuning) Hyper-FET exhibits higher I_{ON} compared to FinFETs. (c) R1 and R2 represent the valid ranges for $I_{C\text{-}IMT}$ for regular and *iso*-I_{OFF} versions of Hyper-FET. (d) R3 and R4 show the ranges for $I_{C\text{-}MIT}$ for similar conditions as in (c).

An interesting feature of Hyper-FET operation is its hysteretic behavior arising from the inherent hysteresis in the PTM characteristics. As we discussed before, in the transfer characteristics, $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ (Fig. 6.1 (c)) correspond to thresholds for IMT and MIT. Comparing the transfer and output characteristics, we define the hysteresis in the transfer characteristics as $HYST_{VGS} = (V_{GS\text{-}IMT} - V_{GS\text{-}MIT})$ and that in output characteristics as $HYST_{VDS} = (V_{DS\text{-}IMT} - V_{DS\text{-}MIT})$. Hysteresis in the device characteristics demands additional attention in functioning circuit design. Hence, we now correlate these two types of hysteresis, which will help understand their circuit level impact in part II. Fig. 6.6 (b) shows that both $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ slightly increase (by ~20mV) for lower V_{DS}. Hence, the hysteresis window ($=V_{GS\text{-}IMT} - V_{GS\text{-}MIT}$) also moves towards higher V_{GS}. This trend can be attributed to the reduction in I_D with decreasing V_{DS}. Thus, triggering IMT necessitates

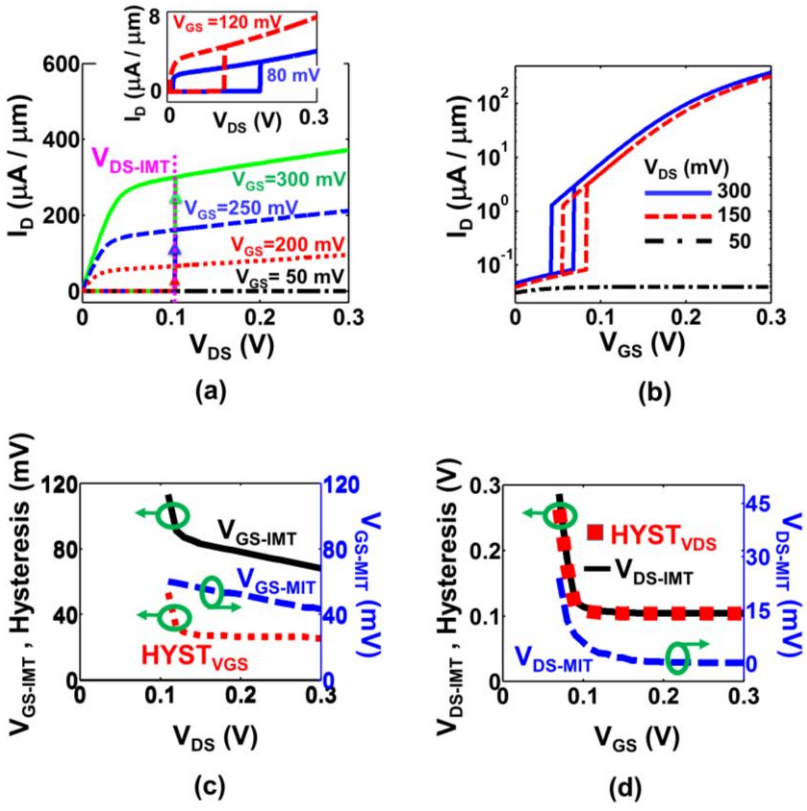


Fig. 6.6 (a) Output characteristics of Hyper-FET for different V_{GS}. (b) Transfer characteristics of Hyper-FET at different V_{DS} (c) Drain bias affects the hysteresis in the transfer characteristics when V_{DS} approaches $V_{DS\text{-}IMT}$ (d) Gate bias affects hysteresis in the output characteristics when V_{GS} approaches $V_{GS\text{-}IMT}$.

higher V_{GS}, thereby increasing $V_{GS\text{-}IMT.}$ Similarly, reduction in I_D favors MIT, yielding higher $V_{GS\text{-}MIT.}$ The trends for $V_{GS\text{-}IMT,}$ $V_{GS\text{-}MIT}$ and $HYST_{VGS}$ corresponding to the applied V_{DS} is illustrated in Fig. 6.6 (c). We observe almost constant hysteresis for V_{DS} > 150 mV. However, as V_{DS} approaches $V_{DS\text{-}IMT,}$ IMT becomes significantly more difficult. Hence, $V_{GS\text{-}IMT}$ increases much more than $V_{GS\text{-}MIT}$ and the corresponding hysteresis increases. The trends for $HYST_{VDS}$ with respect to V_{GS} (Fig. 6.6 (d)) show similar behavior. For V_{GS} much larger than $V_{GS\text{-}IMT}$, $HYST_{VDS}$ is almost insensitive to V_{GS}. But, as V_{GS} approaches $V_{GS\text{-}IMT}$, the hysteresis increases. This insight on the interdependence of $V_{GS\text{-}IMT}$ and $V_{DS\text{-}IMT}$ is vital for determining operating voltage for digital and analog circuits.

6.6 Effect of Material Properties on Device Operation

Tailoring the hysteresis can be a very important aspect of device/circuit design. Hence, a proper material with the right combination of $\rho_{INS,}$ $\rho_{MET,}$ $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$ is required to yield the desired Hyper-FET characteristics. In this section, we explore the effects of these material parameters on the transfer and output characteristics of the Hyper-FET. The target is to analyze the trends of device level behavior considering change in one variable at a time. That will allow us to identify desirable ranges of material parameters.

6.6.1 Analysis on Transfer Characteristics

Fig. 6.7 shows the transfer characteristics of Hyper-FETs for various PTM parameters. The hysteresis in transfer characteristics of Hyper-FET can be controlled by $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$ of the PTM as $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ increase with $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$ respectively. Hence, higher $J_{C\text{-}MIT}$ and lower $J_{C\text{-}IMT}$ produces the least hysteresis in the transfer characteristics. The device design must ensure that Hyper-FETs do not exhibit negative hysteresis (*i.e.* it must be ensured that $V_{GS\text{-}IMT} >= V_{GS\text{-}MIT}$). The reason for imposing this condition is that negative hysteresis physically does not allow the PTM to stabilize in either the insulating or metallic states. As a result, the PTM shows (undesired) oscillatory behavior [81], [105]. Other than that, the hysteresis does not play any key role from the perspective of the device operation, as long as the PTM undergoes IMT and MIT at appropriate voltages. However, from the point of view of circuit operation, the hysteresis as well as the absolute values of $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ must be regulated, as discussed later. It is clear from Figs. 6.7 (a), (b) that

proper material selection (with suitable range of critical current densities) is important to design the device with an appropriate $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$. In addition, the geometry of the PTM can be optimized to achieve IMT and MIT at proper points (discussed later).

The resistivity of the two states of the PTM used in Hyper-FET determine the gain in I_{ON} at *iso*-I_{OFF}. In continuation to the previous discussion, lower ρ_{MET} increases the ON current (Fig. 6.7 (c)) and thereby improves the device performance. Since $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ are mainly governed by R_{INS} of PTM and the transistor resistance (respectively), ρ_{MET} does not significantly affect the hysteresis. On the other hand, an increase in ρ_{INS} (within a certain

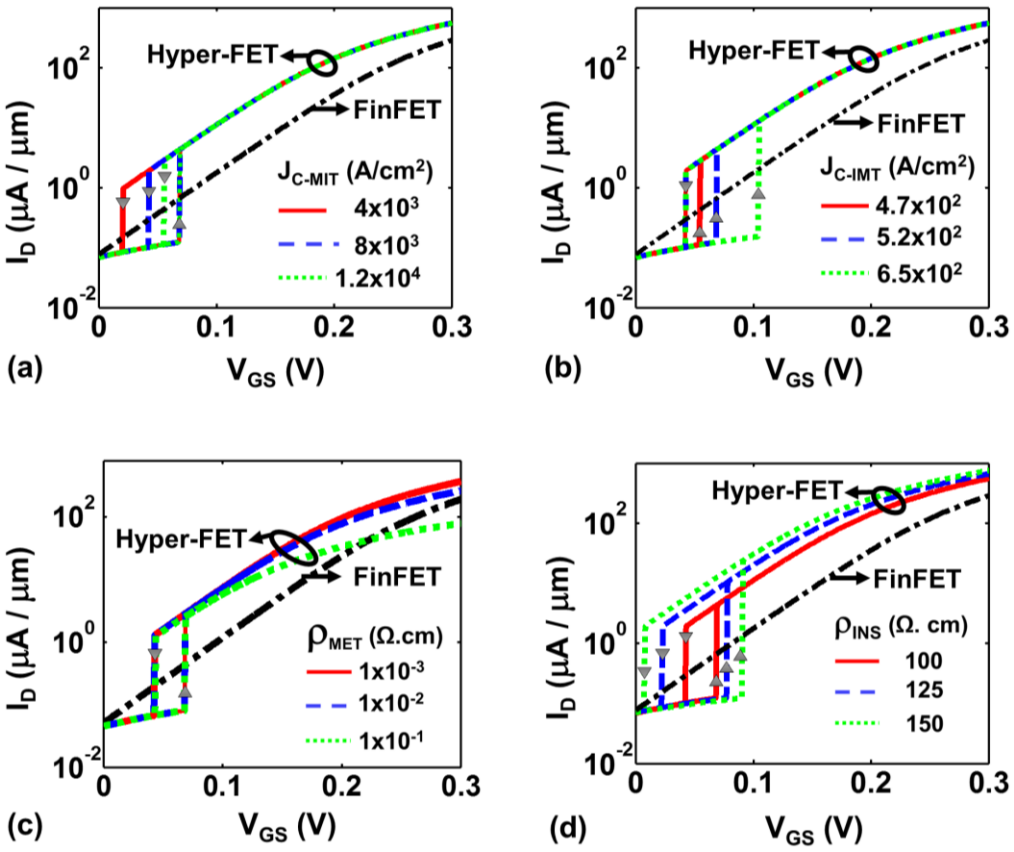


Fig. 6.7 Influence of different material properties on the transfer characteristics of Hyper-FET. (a) $J_{C\text{-}MIT}$ and (b) $J_{C\text{-}IMT}$ sets the hysteresis. (c) High metallic state resistivity reduces ON current and (d) high insulating state resistivity reduces OFF current. At matched I_{OFF} condition, that translates to gain in I_{ON} along with increase in hysteresis. V_{DS} = 0.3 V for all of these cases.

range – as discussed before) not only yields higher I_{ON} at *iso*-I_{OFF} but also increases the hysteresis (Fig. 6.7 (d)).

6.6.2 Analysis on Output Characteristics

Fig. 6.8 (a - d) show the output characteristics of Hyper-FETs for different values of material parameters. $V_{DS\text{-}IMT}$ and $V_{DS\text{-}MIT}$ increase with $J_{C\text{-}IMT}$ and $J_{C\text{-}MIT}$, respectively (Figs. 6.8 (a), (b)). It can also be observed in Fig. 6.8 (a), that with sufficiently low $J_{C\text{-}MIT}$ (< $6x10^5$ A/cm^2), the *dead zone* associated with the reverse sweep (decreasing V_{DS}) is practically eliminated ($V_{DS\text{-}MIT}$ ~1 μV). Figs. 6.8 (c), (d) show the impact of the resistivity

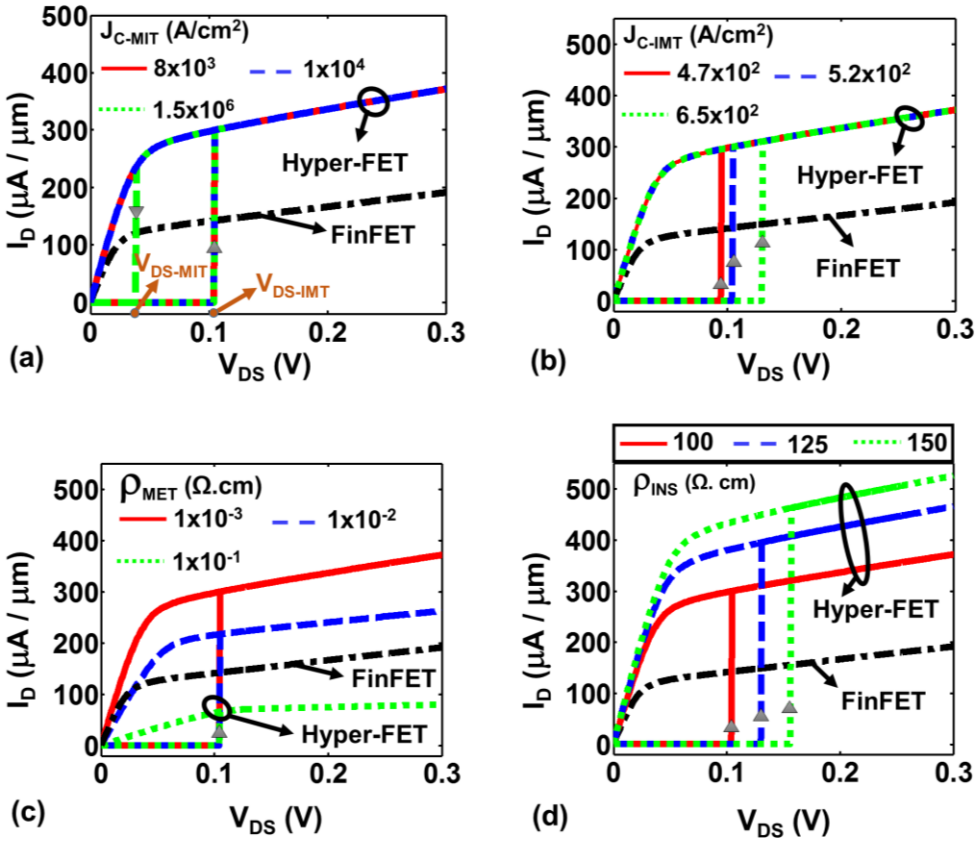


Fig. 6.8 Influence of different material properties on the output characteristics of Hyper-FET. (a) $J_{C\text{-}MIT}$, if too high, may enforce drain current shut off even before V_{DS} becomes close to 0 and thereby limits rail to rail swing in logic devices. (b) Higher $J_{C\text{-}IMT}$ necessitates higher V_{DS} to turn ON the device. (c) High metallic state resistivity reduces ON current and (d) high insulating state resistivity increases gain in I_{ON} along with increase in minimum V_{DS} to turn ON the device. V_{GS} = 0.3V for all of these cases.

of the PTM on the output characteristics of the Hyper-FET. The relative reduction of the ON current with increasing ρ_{MET} is evident in Fig. 6.8 (c). On the other hand, as ρ_{INS} increases, I_{ON}-I_{OFF} ratio is boosted. As a result, larger improvement in I_{ON} (with respect to the standard FinFETs) is observed at *iso*-I_{OFF}. In addition to tailoring the properties of the PTM to achieve the target device characteristics, PTM geometry (length, L_{PTM} and cross-sectional area, A_{PTM}) serves as another important design knob, which we discuss next.

6.7 Effect of PTM Geometry on Device Operation

The length and area of the PTM can be useful knobs for tuning the hysteresis and even ON-OFF ratio of Hyper-FET. The size of the PTM can be a major determinant of its resistance and the critical thresholds for transitions. We will explore this possibility with a constant set of material parameters. To maintain clarity of argument and discussion, we consider linear dependence of critical currents with the area (as mentioned in chapter 1). We also consider that the resistance of the PTM is proportional and inversely proportional to its length and area (respectively).

6.7.1 Tailoring Hysteresis

Figs. 9 (a) and (b) show the influence of length of PTM (L_{PTM}) on $V_{GS\text{-}IMT}$, $V_{GS\text{-}MIT,}$ $V_{DS\text{-}IMT}$ and $V_{DS\text{-}MIT.}$ The PTM presents higher resistance for larger L_{PTM} and thereby reduces the current. As a result, larger voltage is required to trigger IMT; hence, $V_{GS\text{-}IMT}$ *and* $V_{DS\text{-}IMT}$ increase with L_{PTM}. On the other hand, at the vicinity of MIT, PTM is in metallic state and has very low resistance (compared to its baseline transistor). Hence, similar change in L_{PTM} does not modulate $V_{GS\text{-}MIT}$ and $V_{DS\text{-}MIT}$ significantly. It is obvious that an increase in $V_{GS\text{-}IMT}$ (and $V_{DS\text{-}IMT}$) with almost constant $V_{GS\text{-}MIT}$ ($V_{DS\text{-}MIT}$) will increase hysteresis in transfer (and output) characteristics (Fig. 6.9 (a, b)).

Figs. 6.9 (c) and (d) show impact of changing area of the PTM (A_{PTM}) on the switching thresholds ($V_{GS\text{-}IMT}$, $V_{GS\text{-}MIT,}$ $V_{DS\text{-}IMT}$ and $V_{DS\text{-}MIT}$). Unlike L_{PTM}, change in A_{PTM} has a two-fold impact. Increase in A_{PTM} increases $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$ with concurrent reduction in resistance of the PTM. The effect of increase in $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$ and decrease in resistance of PTM have opposite effects on switching thresholds in the transfer and output

characteristics. The effect of PTM resistance is partially suppressed by the transistor resistance. As a result, increase in $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$ with A_{PTM} becomes relatively more influential. Hence, $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ increase simultaneously by increasing A_{PTM}, yielding almost constant hysteresis (Fig. 6.9 (c)). On the other hand, even with larger A_{PTM}, $V_{DS\text{-}IMT}$ stays almost constant (Fig. 6.9 (d)). The reason is that high insulating state resistance of PTM (R_{INS}) sets high voltage at the *source* terminal and leaves very small share of V_{DS} across the transistor. Hence, V_{DS} cannot effectively modulate the transistor resistance and the $V_{DS\text{-}IMT}$ essentially gets pinned at a value ≈ $V_{C\text{-}IMT}$. On the contrary, since the metallic state resistance of the PTM (R_{MET}) is much smaller than that of the FET (R_{FET}), $V_{DS\text{-}MIT}$ increases considerably with A_{PTM} (due to increase in $I_{C\text{-}MIT}$). Increase in $V_{DS\text{-}MIT}$ with fixed $V_{DS\text{-}IMT}$ reduces hysteresis for larger area. But, our analysis shows that, $V_{DS\text{-}MIT}$ never exceeds $V_{DS\text{-}IMT}$ (*i.e.* hysteresis never becomes negative) for practically acceptable A_{PTM}.

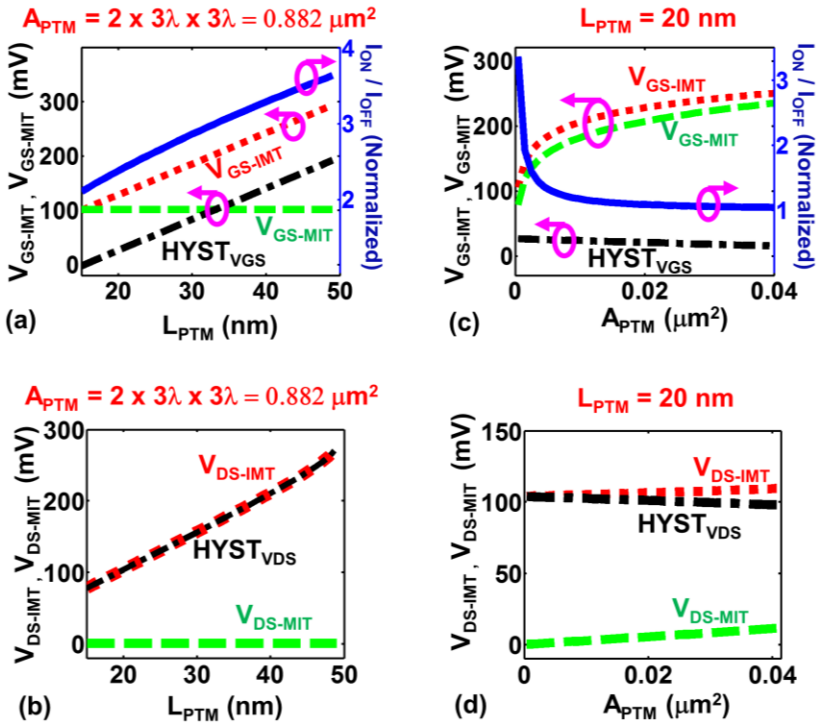


Fig. 6.9 Effect of the geometry of CM on device metrics. (a) $V_{GS\text{-}IMT}$ changes significantly with L_{PTM} , whereas $V_{GS\text{-}MIT}$ is almost desensitized to L_{PTM} . Higher L_{PTM} also yields high I_{ON} - I_{OFF} ratio. (b) Both $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ changes significantly with A_{PTM}. Higher A_{PTM} reduces I_{ON} - I_{OFF} ratio. (c) $V_{DS\text{-}IMT}$ and corresponding $HYST_{VDS}$ increases with L_{PTM}. (d) $V_{DS\text{-}IMT}$ remains fixed while $V_{DS\text{-}MIT}$ increases with A_{PTM}, reducing $HYST_{VDS}$.

Such changes in hysteresis are accompanied by a concurrent change in $I_{ON}/I_{OFF,}$ which we discuss next.

6.7.2 Modulating I_{ON}/I_{OFF}

I_{ON}/I_{OFF} increases with L_{PTM} (Fig. 6.9 (a)). Due to increase in L_{PTM}, I_{OFF} reduces significantly whereas I_{ON} does not reduce as much (since $R_{MET} < R_{FET}$). This yields higher I_{ON} - I_{OFF} ratio. On the contrary, increase in A_{PTM} leads to reduction in I_{ON}/I_{OFF} (Fig. 6.9 (c)). Larger A_{PTM} reduces R_{INS}, resulting in an upsurge in I_{OFF}. However, reduction in R_{MET} contributes to only slight increase in I_{ON}. Note, a large increase in L_{PTM} or reduction in A_{PTM} can yield prohibitively large R_{INS}. This reduces the modulation of current with increasing V_{GS} (as discussed before), thereby, precluding IMT and hampering the device operation. Considering the nominal values of parameters reported in Table 6.1, we report $L_{PTM\text{-}(maximum)}$ = 4 μm and $A_{PTM\text{-}(minimum)}$ =10 nm^2. Clearly, both L_{PTM} and A_{PTM} are instrumental in modifying the device characteristics of Hyper-FET. Tuning L_{PTM} accompanied by alteration in A_{PTM} (and *vice versa*) forms a fine-tuning knob in designing Hyper-FETs. Nevertheless, A_{PTM} may be limited by the layouts and it necessitates co-optimization of area-performance- power of logic gates.

6.8 Hyper-FET Inverter: DC Response

So far, we have discussed the device characteristics of Hyper-FET and explained its operating principle. We showed that, hysteresis and abrupt switching in the current-voltage (*I-V*) characteristics of the PTM are manifested in the transfer and output characteristics of Hyper-FET. The hysteresis and I_{ON}/I_{OFF} can be tailored by tuning the geometry of the PTM and/or selecting PTMs with suitable resistivity and current thresholds for IMT and MIT. The impact of hysteresis continues all the way from material to circuit level and hence gives rise to unconventional circuit responses. In some cases, the unique attributes of Hyper-FETs and their interactions with circuits may lead to functional failure of the logic. To avert such scenarios, we analyze the device-circuit interactions in Hyper-FET based logic and establish design methodologies to achieve functioning circuits. We start our circuit level discussion with a comprehensive analysis of the inverter. We discuss the

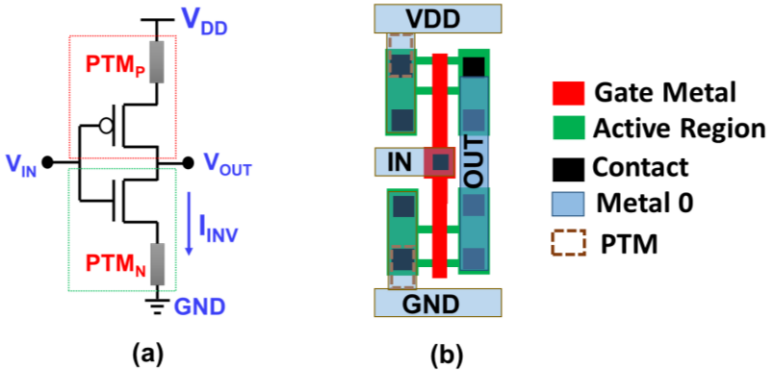


Fig. 6.10 (a) Circuit diagram and (b) layout of Hyper-FET based inverter.

inverter operation in detail to provide insights into some unique circuit level phenomenon that the Hyper-FETs exhibit.

6.8.1 Voltage Transfer Characteristics

A Hyper-FET inverter comprises of complementary n channel and p channel Hyper-FETs with PTMs connected to the supply rails (Fig. 6.10 (a) and (b)). Fig. 6.11 shows the voltage transfer characteristics (VTC) and the DC current of a functioning Hyper-FET based inverter along with the corresponding transfer and output characteristics of the n- and p-Hyper-FETs. For the DC analysis, it is important to note that the current through the pull-up and pull-down Hyper-FETs are equal (defined as I_{INV}). Therefore, if the corresponding phase transition materials (PTM_N and PTM_P - Fig. 6.10 (a)) are designed to have the same dimensions, they have the same critical currents for IMT and MIT and therefore, operate in the same phase. Moreover, they undergo IMT and MIT at the same input/output bias. When the inverter input (V_{IN}) is 0, PTM_N and PTM_P operate in insulating state. This is due to the inverter current being less than $I_{C\text{-}IMT,}$ as the pull-down Hyper-FET is in the OFF state. It is important to note that although the V_{GS} of the p-Hyper-FET is $-V_{DD}$, PTM_P operates in the insulating state. Therefore, its V_{DS} must be less than $V_{DS\text{-}IMT}$ (Fig. 6.11 (b)). It is also noteworthy that the pull-up resistance is dominated by the insulating state resistance of PTM_P. Hence, the output voltage (V_{OUT}) is determined by the relative resistance of PTM_P in the insulating phase and that of the pull-down Hyper-FET in the OFF state. Since both may be comparable, we obtain $V_{OUT} < V_{DD}$ in the VTC (Fig. 6.11 (c)) for

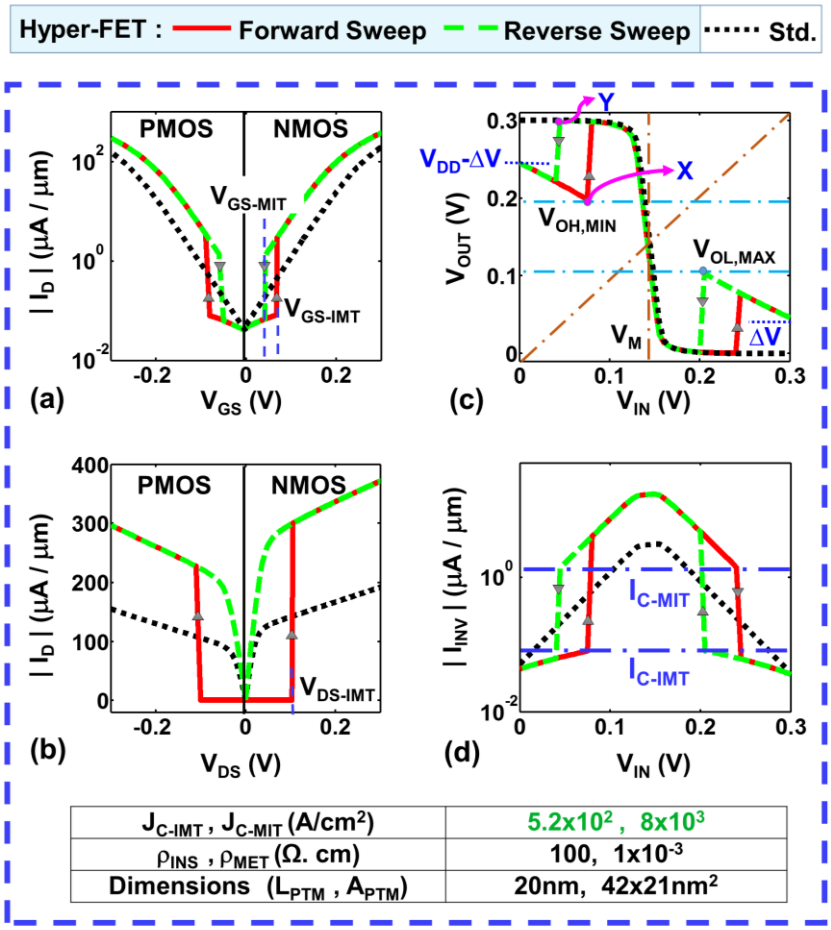


Fig. 6.11 (a) Transfer and (b) output characteristics of complementary n and p Hyper-FETs yielding phase switching at low (< V_{DD}/2) bias voltage. (c) Voltage transfer characteristics (VTC) of the functioning Hyper-FET inverter. (d) Current through the inverter.

V_{IN} = 0 V. Similarly, for V_{IN} =V_{DD}, a non-zero DC output is observed. During the low to high input transition, the inverter current increases as n-Hyper-FET turns ON, and the output voltage decreases mildly as the relative resistance of the pull-down network decreases. When the inverter current increases beyond I_{C-IMT} (Fig. 6.11 (d)), PTM_N and PTM_P transition into the metallic state, thereby exhibiting characteristics similar to the standard inverter.

In the transition region of the VTC, PTM_N and PTM_P must operate in the metallic state in order to achieve a gain (V_{OUT} /V_{IN}) greater than 1 in magnitude (to ensure regenerative

action [164]). As the input exceeds the logic threshold voltage (V_M) of the inverter, the current starts reducing. PTM_N and PTM_P continue to operate in the metallic state as long as the current remains larger than $I_{C\text{-}MIT}$. As V_{IN} increases beyond a certain point and the current becomes less the $I_{C\text{-}MIT}$ (Fig. 6.11 (d)), PTM_N and PTM_P transition back into the insulating state, which leads to a rise in the output voltage, as shown in Fig. 6.11 (c). In a similar manner, decrease in the output voltage from V_{DD} to 0 first triggers IMT in the PTMs. As a result, gain in the transition region is observed in the VTC. Once V_{IN} reduces below a certain point, MIT is triggered, causing the output voltage to drop. Hysteresis in observed in the non-transition region of the VTC (as predicted before). Note, the VTC of the Hyper-FET inverters is quite unconventional and needs further discussion. Subsequently, in this sub-section, we present several aspects of the DC behavior of the Hyper-FET inverter and its relationship with PTM properties and device design.

6.8.2 PTM Selection: DC Perspective

In section 6.6, we presented requirements for the material parameters to yield optimum device characteristics. Here, we re-evaluate those requirements and show how they become even more constrained when circuit functionality is taken into account. Redirecting to the VTC of Hyper-FET inverter (Fig. 6.11 (c)), we note two vital points:

(a) PTM_N and PTM_P must undergo IMT in the non-transition region to achieve |gain| ($|V_{OUT} / V_{IN}|$) > 1 in the VTC, thus enabling the regenerative action.

(b) When the PTMs operate in the insulating state and V_{IN} is less than the logic threshold voltage of the inverter (V_M), the lowest output voltage (marked as $V_{OH,MIN}$ in Fig. 6.11 (c)) must be greater than V_M. Similarly, when $V_{IN} > V_M$, the highest output voltage ($V_{OL,MAX}$) must be less than V_M.

These two conditions can be met by properly designing the Hyper-FETs either via appropriate material design or by tuning the PTM dimensions.

We start with discussion for the first design requirement. To illustrate its significance, we show the VTC of a non-functioning Hyper-FET based inverter and the corresponding device characteristics in Figs. 6.12 (a) - (d). Comparing the functional (Fig. 6.11) and the

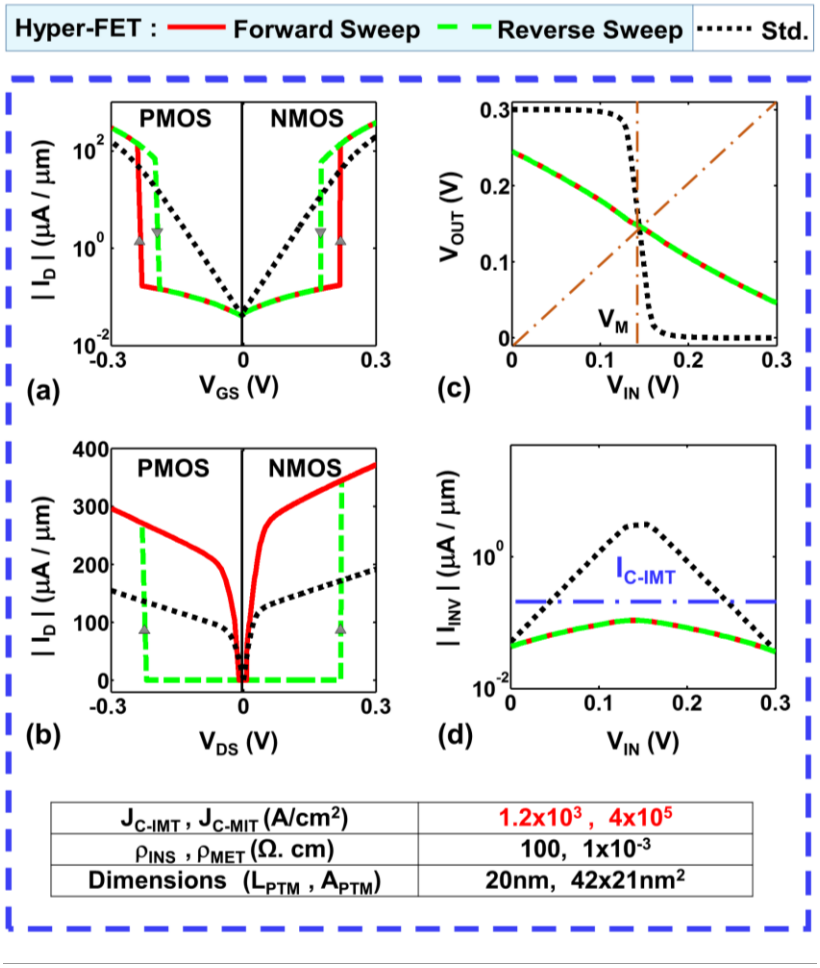


Fig. 6.12 (a) Transfer and (b) output characteristics of complementary n and p Hyper-FETs yielding phase switching at higher (> V_{DD}/2) bias voltage. (c) VTC of the Hyper-FET inverter illustrating |gain| < 1 in the transition region. (d) Current through the non-functioning inverter.

non-functional inverters (Fig. 6.12), it can be observed that $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ are higher in the latter case. High values of $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ make it more difficult to trigger IMT during the forward sweep but easier to trigger MIT during the reverse sweep. If the Hyper-FET exhibits $V_{GS\text{-}IMT} > V_{DD}$ /2 (typical V_M) at $V_{DS} = V_{DD}$ /2, PTMs never undergoes IMT ($I_{INV} < I_{C\text{-}IMT}$, Fig. 6.12 (d)) and no gain is observed in the VTC, as shown in Fig. 6.12 (c). Based on our discussion in sections 6.6 and 6.7, it can be restated that the modulation of hysteresis (in transfer and output characteristics of n and p-Hyper-FETs) can be achieved through sizing or proper material down-selection. Thereby, to achieve functional logic

gates with proper DC gain, appropriate circuit-driven device design is required to ensure that $V_{GS\text{-}IMT}$ is sufficiently less than $V_{DD}/2$ at $V_{DS} = V_{DD}/2$.

We can render this voltage based discussion to a current based one and thereby use it to deduce the ranges for I_{CIMT} and I_{CMIT}. $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ correspond to $I_{INV} = I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$ respectively. As mentioned earlier, IMT in PTM needs to occur within the non-transition voltage zones of the VTC ($V_{IN} < V_{DD}/2$ and $V_{IN} > V_{DD}/2$ for rising and falling V_{IN} respectively). Hence, $I_{C\text{-}IMT}$ must be achievable within $V_{GS} < V_{DD}/2$ (at $V_{DS} = V_{DD}/2$). Recalling our discussion in section 6.5, it was sufficient to achieve $I_{C\text{-}IMT}$ within $V_{GS} < V_{DD}$ (at $V_{DS} = V_{DD}$) for a stand-alone Hyper-FET. With a similar analysis as in Fig. 6.4, but with a different bias target, we obtain a feasible range of $I_{C\text{-}IMT}$ (Fig. 6.13 (a)) for a Hyper-FET based inverter. To prevent the oscillatory behavior ($V_{GS\text{-}IMT} > V_{GS\text{-}MIT}$), $I_{C\text{-}MIT}$ must be reduced accordingly. Clearly, the feasible range for $I_{C\text{-}MIT}$ also reduces compared to standalone Hyper-FET (Fig. 6.13 (b)).

Let us now discuss the second design requirement related to $V_{OH,MIN}$ and $V_{OL,MAX}$. This design aspect mainly depends on the insulating state resistivity of the PTM. With increasing ρ_{INS}, $V_{OH,MIN}$ reduces and $V_{OL,MAX}$ increases. If the insulating state resistance of PTM_P and PTM_N is much higher than the OFF-state resistance of their host FETs, then through voltage division, the V_{OUT} of the inverter becomes $\approx V_{DD}/2$ ($\approx V_M$ for equal strength

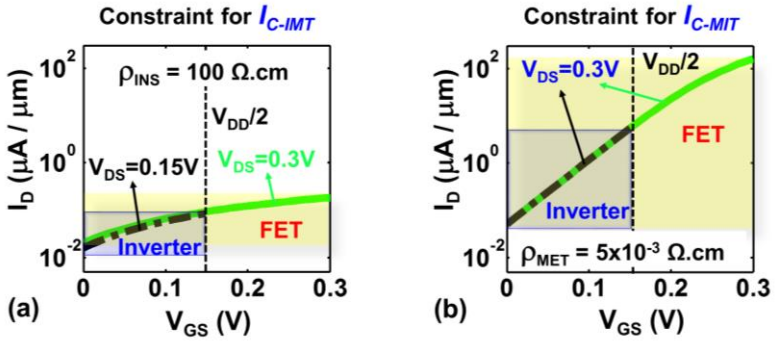


Fig. 6.13 (a) Feasible ranges of critical current level for (a) IMT and (b) MIT phase switching. The feasible ranges for $I_{C\text{-}IMT}$ and $I_{C\text{-}MIT}$ becomes stringent for a Hyper-FET inverter as compared to those for the Hyper-FET.

of n and p-Hyper-FET). Therefore, for symmetrically designed n- and p- Hyper-FETs with PTMs having identical dimensions, $V_{OH,MIN}$ and $V_{OL,MAX}$ saturate at $V_{DD}/2$ as ρ_{INS} increases. Our analysis shows that as long as the device level constraints for ρ_{INS} (discussed in section 6.6) are met, $V_{OH,MIN} > V_{DD}/2$ and $V_{OL,MAX} < V_{DD}/2$ can be easily obtained. However if the n and p base transistors are designed to have unequal strengths (*i.e.* for $V_M \neq V_{DD}/2$) or PTM_N and PTM_P do not have identical dimensions, this circuit requirement may have to be considered while optimizing the devices. In such a scenario, this constraint may introduce an upper bound on ρ_{INS}, above which $V_{OH,MIN}$ may become less than V_M or $V_{OL,MAX}$ may exceed V_M. This calls for selecting PTMs with optimum ρ_{INS}.

Another prominent aspect of the inverter characteristics is the hysteresis in VTC, which demands a special attention and necessitates tuning appropriate design knobs. In that regard, we next examine the effect of different material parameters (within feasible range) on the

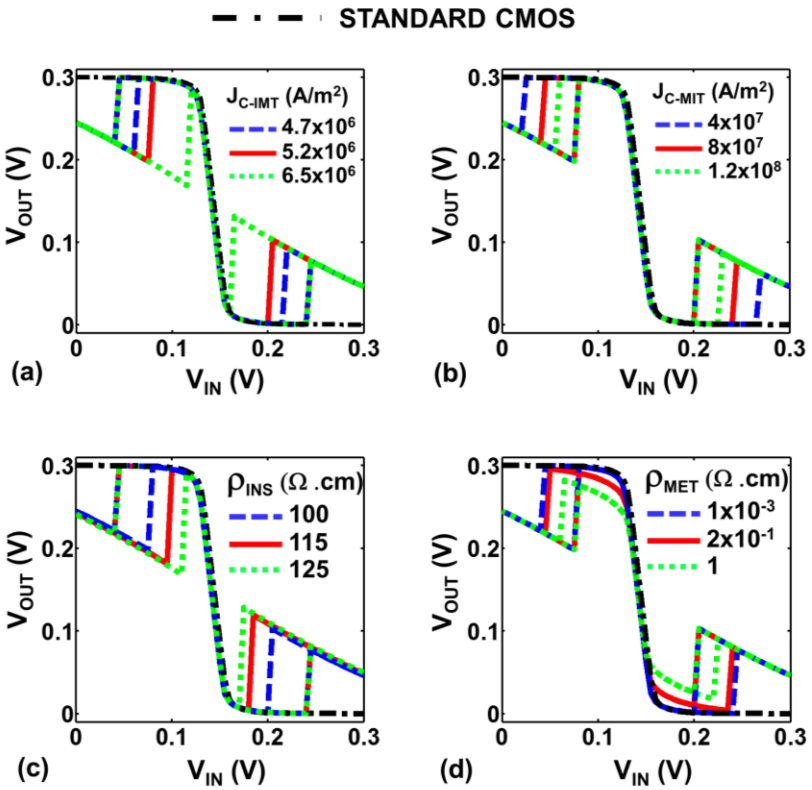


Fig. 6.14 Effect of (a) $J_{C\text{-}IMT}$ (b) $J_{C\text{-}MIT}$ (c) ρ_{INS} and (d) ρ_{MET} on the VTC of Hyper-FET based inverter.

VTC and the inverter gain $|V_{OUT}/V_{IN}|$. As shown in Fig. 6.14 (a) - (c), hysteresis window widens with increasing $J_{C\text{-}IMT}$, $J_{C\text{-}MIT}$ and ρ_{INS}. However, the gain in the inverter VTC remains similar as the standard CMOS inverter, as long as the constraints discussed above are met. On the other hand, higher ρ_{MET} lowers hysteresis in VTC (Fig. 6.14 (d)). However, if the value of ρ_{MET} is too high (> 1 Ω.cm), it adversely affects the inverter operation by reducing the gain. Very high ρ_{MET} may also lead to incomplete voltage swing in transient operation (discussed later). To complete the discussion on the DC behavior, we show the correlation between the device and circuit level hysteresis in the following subsection.

6.8.3 Correspondence between Hysteresis in Device and Circuit Characteristics

A Hyper-FET based inverter exhibits hysteresis in its VTC because the n and p- Hyper-FETs are themselves hysteretic. We illustrate the hysteresis window for a standalone Hyper-FET and a Hyper-FET inverter in Figs. 6.15 (a) and (b) respectively. It is clear that, increase in device level hysteresis linearly increases hysteresis in VTC (Fig. 6.15 (c)). Interestingly, the hysteresis in the VTC is always higher than that seen in the transfer characteristics. It occurs because, during inverter operation, the Hyper-FET concurrently experiences changes in V_{GS} and V_{DS}. Taking an example, the n-Hyper-FET experiences rising V_{GS} and falling V_{DS} for low to high input transition in an inverter. Evoking our discussion in section 6.5, lower V_{DS} leads to higher $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$, as IMT becomes more difficult and MIT becomes easier (due to reduction in I_D). Now, during logic transition in inverter, (for n-Hyper-FET) IMT occurs at $V_{DS} = V_{OUT} < V_{DD}$ (point X in Fig.

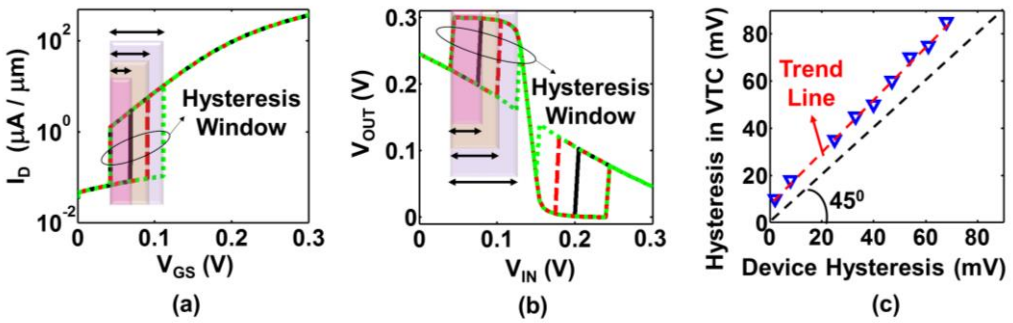


Fig. 6.15 (a) Different levels of hysteresis window in transfer characteristics of Hyper-FET. (b) Corresponding hysteresis in VTC. (c) Trend line shows that hysteresis in VTC is linearly dependent on that in transfer characteristics but is always larger in magnitude.

6.11 (c)), whereas MIT occurs at $V_{DS} = V_{OUT} \approx V_{DD}$ (point Y in Fig. 6.11 (c)). As a result, $V_{GS\text{-}IMT}$ increases but $V_{GS\text{-}MIT}$ remains the same with respect to the values from the device transfer characteristics (which are obtained at V_{DS}=V_{DD}). Thus, the hysteresis increases in the VTC. In addition, the VTC of the Hyper-FET inverter raises '*apparent*' concerns of incurring incomplete voltage swing and reduced noise margins. We address these concerns next.

6.8.4 Apparent and Achievable Voltage Swing

Referring back to the discussion about VTC from a different viewpoint, here we investigate the achievable voltage swing in the inverter output. Fig. 6.11 (c) shows that *DC output* of Hyper-FET based inverter may span between V_{DD} - ΔV and ΔV (unlike, V_{DD} and 0 for its ideal CMOS counterpart). Here, ΔV is the deviation in the output voltage from the ideal values as marked in Fig. 6.11 (c). It provides an apparent notion of possible incomplete voltage swing in Hyper-FET based inverters. It also raises a concern regarding static power consumption in Hyper-FET based inverter. However, interesting point to note is that the

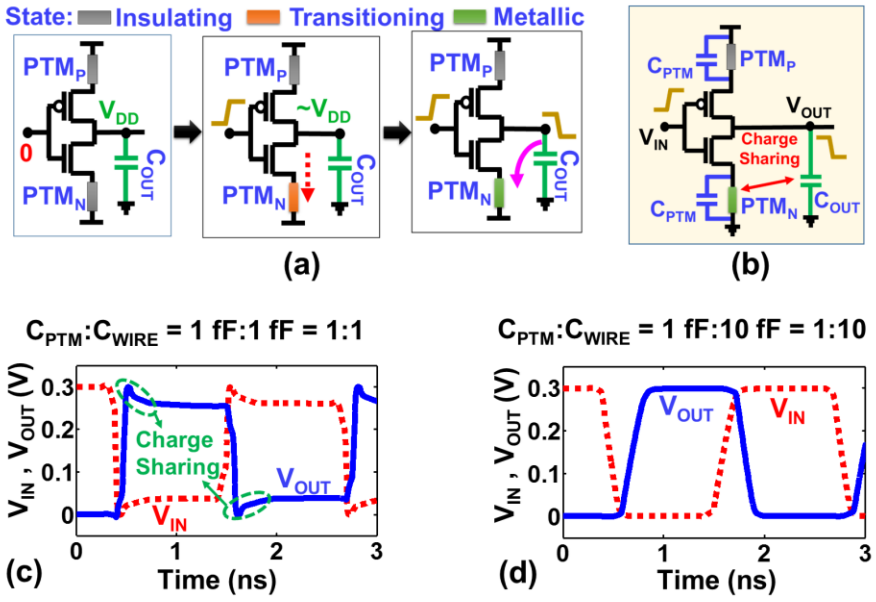


Fig. 6.16 (a) Steps of transient operation of a Hyper-FET based inverter. (b) Representation of charge sharing in Hyper-FET inverter. (c) Transient waveforms for Hyper-FET inverter chain illustrating charge sharing between C_{PTM} and C_{OUT}. (d) Charge sharing is not pronounced for C_{WIRE} dominated circuit (*i.e.* for $C_{PTM} < C_{OUT}$).

transient analysis (discussed in the next section) shows full voltage swing (Fig. 6.16). To explain the reason, we emphasize on the fact that the DC responses correspond to an indefinite (infinite) time. Given a sufficiently long time in static condition, the output of Hyper-FET inverter will discharge from full V_{DD} to a lower value, V_{DD} - ΔV; or will charge from 0 to ΔV. However, the charging/discharging occurs through a path containing phase transition material in insulating state (very high resistance). Hence, this process is extremely slow and during the dynamic circuit operation, this degradation in the voltage levels may not be significant (detail discussion in next section). In addition, since both PTM_N and PTM_P operate in a very high resistance insulating state as the output voltage charges/discharges to ΔV or V_{DD}-ΔV, respectively, the static current is very small. In summary, full swing can be achieved in a Hyper-FET based logic circuit during its transient operation (shown in the next section). The apparent reduction in the voltage swing in the DC characteristics merely indicates the change in the output voltage if the inverter remains static for a very long time (~R_{INS}×C_{OUT}, where R_{INS} is the insulating state resistance of the PTM and C_{OUT} is the output capacitance of the inverter). It is important to mention that the voltage swing in a Hyper-FET is dependent on additional parameters and to ensure full voltage swing, the device-circuit interactions during inverter transients need to be analyzed and the devices need to be properly designed (will be discussed in section 6.9).

Interestingly, we see that the PTM appears to settle in its insulating state both for high and low logic level at the output. This implies that, the inverter will be connected to the supply rails (V_{DD} and *Gnd*) through a very high resistance. Consequently, the output will tend to be *floating* during a long-term static operation of the inverter. It raises concern regarding *noise* induced output degradation. In addition, the unique non-transition regions of the VTC suggest a possible reduction in the noise margins. However, due to the unconventional characteristics, classical DC approaches of evaluating noise margin may not be valid for Hyper-FET based inverter and may yield misleading results. We analyze the noise response of Hyper-FET inverter in section 6.10 by performing transient analysis and describe an important counter-effect that mitigates this concern.

To summarize the concepts discussed throughout this section as a whole, Hyper-FET, being a hysteretic device, demands additional considerations for inverter design. In addition, we need to devote special consideration towards the transition thresholds of the PTM to achieve proper gain in the VTC. The specific $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ points do not affect the device characteristics and performance metrics (like I_{ON} / I_{OFF}). However, circuit functionality imposes additional constraints on these metrics. We realize that the specific values of $V_{GS\text{-}IMT}$ and $V_{GS\text{-}MIT}$ are as much important as the magnitude of hysteresis (= $V_{GS\text{-}IMT}$ - $V_{GS\text{-}MIT}$) itself. VTC of the Hyper-FET inverter is instrumental in verifying the gain of the logic gate. However, voltage swing and noise margin cannot be determined from the VTC and need proper transient analysis, as discussed next.

6.9 Hyper-FET Inverter: Transient Operation

In this section, we describe the dynamic operation of Hyper-FET inverter. We discuss the possibility and the process of charge sharing which may have interesting implications on noise response. We provide additional selection criteria for PTM to obtain better transient performance. We also present energy-delay benchmarking for Hyper-FET based ring oscillator (RO).

6.9.1 Analysis of Transient Waveforms

The transient waveforms for Hyper-FET based inverter are shown in Fig. 6.16. Initially, both PTM_N and PTM_P operate in the insulating phase (Fig. 6.16 (a)). For low-to-high input transition (increasing V_{IN}), the n-Hyper-FET experiences forward (increasing) sweep in $V_{GS.}$ As its V_{GS} surpasses $V_{GS\text{-}IMT}$, PTM_N turns metallic and starts discharging the output. (Note that PTM_P remains in the insulating phase during this time). As V_{OUT} reduces, so does the V_{DS} of the n-Hyper-FET. When V_{OUT} reduces beyond $V_{DS\text{-}MIT}$ (Fig. 6.17 (a)), PTM_N turns insulating and restricts further discharge of V_{OUT}. In other words, the output settles at a value equal to $V_{DS\text{-}MIT}$ of the n-Hyper-FET. With a similar argument with regard to the p-Hyper-FET, it is apparent that the output settles at a value = V_{DD} -$V_{DS\text{-}MIT}$ during high-to-low input transition. Thus, by designing the Hyper-FETs with $V_{DS\text{-}MIT}$ less than a few mV (by choosing appropriate PTM or proper optimization of its area), full voltage swing is achieved. This validates our previous claim about voltage swing in section 6.8. However,

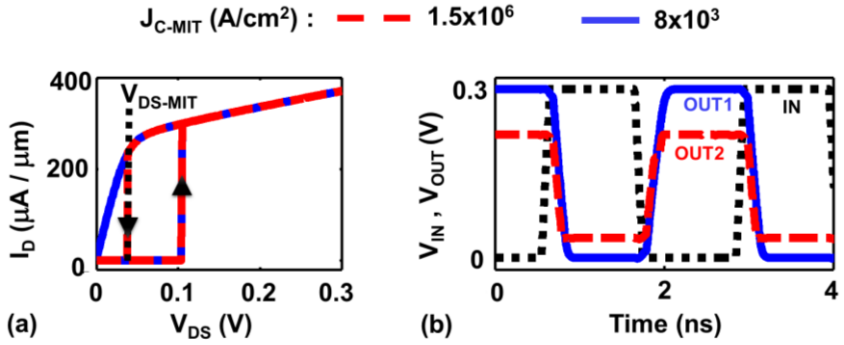


Fig. 6.17 (a) Output characteristics of two versions of Hyper-FET (with different PTMs), illustrating MIT driven *'dead zone'* in one. (b) The *'dead zone'* in I_D-V_{DS} results in incomplete voltage swing at the output of the inverter.

there is a possibility of getting incomplete voltage swing if $V_{DS\text{-}MIT}$ of the Hyper-FETs in an inverter is not very close to 0. The relationship between the device characteristics (specifically $V_{DS,MIT}$) and the output voltage swing is illustrated in Fig. 6.17, pointing out the critical need for a circuit-driven device design for Hyper-FET. Note, $V_{DS} < V_{DS\text{-}IMT}$ yields a *dead zone* in output characteristics for increasing V_{DS} (as discussed in section 6.5). But, according to the basic principle of inverter operation, both n and p- Hyper-FETs experience only decreasing V_{DS} during dynamic operation. Hence, *dead zone* occurring below $V_{DS\text{-}IMT}$ does not affect the inverter operation.

Another important aspect to consider during the transient analysis is the inherent capacitance of the PTM ($C_{PTM,N}$ and $C_{PTM,P,}$ Fig. 6.16 (b)). After the output voltage switches, PTM_N and PTM_P operate in the insulating phase. As a result, charge sharing may occur between the output capacitance (C_{OUT}) and PTM capacitance (C_{PTM}). This effect becomes critical if C_{PTM} is comparable to the wire and other load capacitances present at the output and eventually deteriorate the waveforms. Since the PTM stays in the insulating state during the static mode, an undesired voltage level may build up across PTM due to charge sharing (Fig. 6.16 (c)). However, if $C_{PTM} < C_{OUT}$, charge sharing is mitigated (Fig. 6.16 (d)). Charge sharing does not disrupt logic functionality. However, given a need, it is possible to eliminate it by choosing appropriate PTM yielding $C_{PTM} < C_{OUT}$. An additional

assurance comes from the experiment, which shows C_{PTM} can be tuned with PTM geometry [165].

6.9.2 Ring Oscillator (RO): Energy-Delay Analysis

With the understanding of the transient behavior, we benchmark Hyper-FET based circuits and evaluate the energy-delay characteristics through ring oscillator (RO) simulations (Fig. 6.18). As evident from the previous discussion, the delay of a Hyper-FET-based circuit is a function of the inherent switching time associated with IMT, the drive strength of the Hyper-FET and the capacitance of the PTM. Note, in our analysis, the IMT switching time has been considered in addition to C_{PTM}. While the latter represents the delay in building up the voltage across PTM, the former models the finite delay to undergo IMT once the voltage exceeds $V_{C\text{-}IMT}$). In general, the benefits of Hyper-FET depend on the inter-play between these effects and are a function of V_{DD}. For V_{DD} < 0.5V, Hyper-FET based RO achieves up to 70% lower delay at *iso*-energy (Figs. 6.18 (b) and (c)). This is a direct consequence of the higher I_{ON} of Hyper-FET at iso-I_{OFF}. At high V_{DD}, the performance of Hyper-FETs is limited by the transition time associated with IMT and MIT (assumed to be ~50 ps based on projection from experiments [86]). Hence, standard inverters exhibit higher speed at V_{DD} > 0.5V (Fig. 6.18 (c)). As V_{DD} is scaled, the transistor speed reduces below the IMT and MIT switching rate. As a result, the circuit performance is determined by the drive strength of the Hyper-FET, which is superior to the standard FETs at *iso*-I_{OFF}

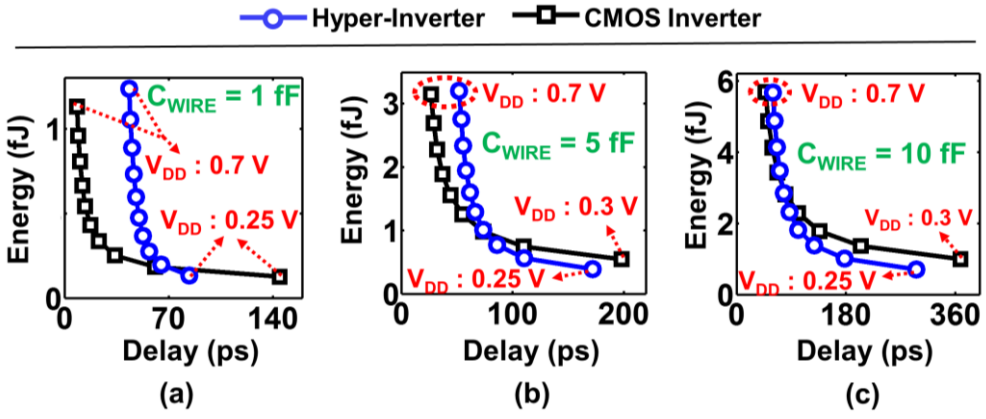


Fig. 6.18 (a) Energy-delay metrics for Hyper-FET based and standard ring oscillators (RO) for (a) low (b) moderate and (c) high C_{WIRE}.

(see Fig. 6.11 (a)). It is clear that, to obtain performance benefits, PTMs used in Hyper-FETs must have lower transition time than the target circuit speed at low voltages. The performance of Hyper-FET based RO is also influenced by relative values of C_{PTM} and the output capacitance (C_{OUT}) of the inverter. We capture the effect of various C_{OUT} by using different wire capacitance (C_{WIRE}). Hyper-FET based RO does not exhibit benefit over standard CMOS RO if C_{WIRE} is comparable to C_{PTM} (Fig. 6.18 (a)). In such a scenario, charging and discharging of C_{PTM} and charge sharing (discussed before) acts as a bottleneck to the RO performance by introducing additional delay. Nevertheless, for higher C_{WIRE} or lower C_{PTM} this concern is mitigated. Thus, with proper selection of the materials and PTM geometry, an appropriately designed Hyper-FETs (as discussed in this work) can exhibit 25%-68% less energy at *iso*-delay for low voltage operation (Figs. 6.18 (b), (c)).

We also analyze the trends for energy and delay of Hyper-FET based RO within feasible ranges of material parameters (Fig. 6.19). Increasing ρ_{INS} has two opposing effects on delay.

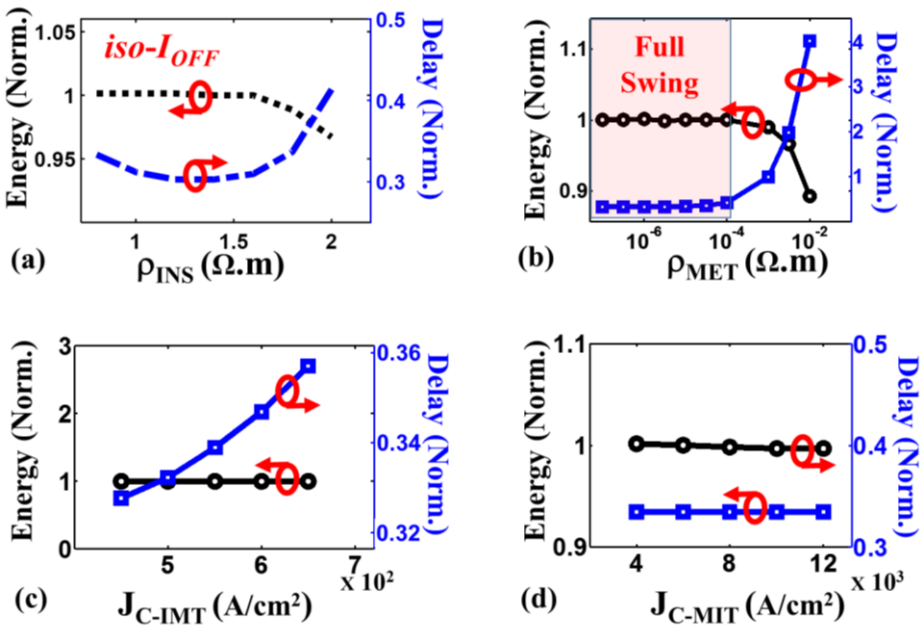


Fig. 6.19 Trends for energy and delay of Hyper-FET based RO with respect to (a) ρ_{INS} (b) ρ_{MET} (c) $J_{C\text{-}IMT}$ (d) $J_{C\text{-}MIT}$. V_{DD} = 0.25 V for all of these cases. The values have been normalized with respect to the corresponding energy and delay of a FinFET based CMOS inverter operating with V_{DD} = 0.25 V. Here, C_{WIRE} = 10fF.

Higher I_{ON} at *iso*-I_{OFF} tends to reduce the delay. However, large ρ_{INS} (hence, R_{INS}) leads to increase in the potential at the *source* terminal of the host FET. This tends to increase the delay associated with charging/discharging C_{PTM} to V_{DD} or 0 after the PTM undergoes IMT (see Fig. 6.16 (a)). Because of these two opposing factors, the delay shows a non-monotonic trend with respect to ρ_{INS} (with the minimum delay for ρ_{INS} ~1.5 Ω.m). On the other hand, energy reduces with increasing ρ_{INS} (Fig. 6.19 (a)). In contrast to ρ_{INS}, ρ_{MET} does not affect the energy or delay of the RO, as long as ρ_{MET} is sufficiently low (< ~10^{-4} Ω.m). This is because the transistor resistance dominates over R_{MET}. However, ρ_{MET} >10^{-4} Ω.m reduces I_{ON} of the inherent transistors and thereby leads to large delay (Fig. 6.19 (b)). In addition, such high ρ_{MET} leads to large value of $V_{DS\text{-}MIT}$ and therefore causes incomplete voltage swing. As a result, the energy decreases for high ρ_{MET} (Fig. 6.19 (b)). $J_{C\text{-}IMT}$ do not affect the energy of the RO (Fig. 6.19 (c)). However, the delay increases with $J_{C\text{-}IMT,}$ since the PTM becomes more prone to be in insulating state (Fig. 6.19 (c)). On the contrary, $J_{C\text{-}MIT}$ does not modulate delay or energy much. (Fig. 6.19 (d)). But, for $J_{C\text{-}MIT}$ > 1.5x10^6 A/cm^2, $V_{DS\text{-}MIT}$ becomes considerably high and the incomplete swing starts occurring at the inverter output. For such scenario, energy reduces with $J_{C\text{-}MIT}$ (Not included in the plot).

6.9.3 PTM Selection: Transient Perspective

The previous discussions highlight the additional material constraints on the PTM for a fixed geometry. To achieve full voltage swing and therefore sufficiently low $V_{DS\text{-}MIT}$, PTM with low $J_{C\text{-}MIT}$ (< 6x10^5 A/cm^2) and/or low ρ_{MET} (< 10^{-4} Ωm) is required. $J_{C\text{-}IMT}$ should be as low as possible. To maximize the benefits in Hyper-FET inverter, optimum ρ_{INS} (~ 1.5 Ωm, in our case) should be chosen. In addition, PTMs with a low inherent capacitance (sufficiently smaller than the typical fan out / wire capacitance in a circuit) is preferable. It is also important to ensure low switching time for IMT and MIT, so that the transition processes do not become the bottleneck in transient operation.

6.10 Noise Response

Noise appears to be an obvious concern in Hyper-FET based logic circuits due to the high impedance output node. However, intermittent phase switching in PTMs mitigates the problem. To illustrate this, let us consider Fig. 6.20. The coupling between the input and

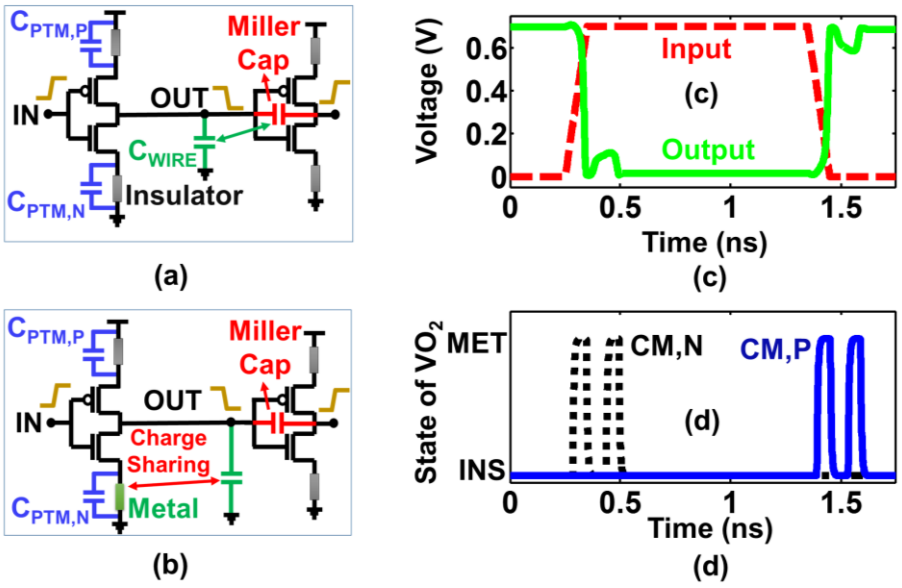


Fig. 6.20 (a) Charge injection at the output node of an inverter stage through miller capacitance effect arising from the next stage. (b) Increase in output voltage triggers IMT in PTM once it crosses critical voltage level. (c) Hyper-FET inverter waveforms showing full rail-to-rail swing with time limited glitches due to floating output node. (d) Short spanned oscillatory phase transition in PTMs eradicating noise contribution from output.

output nodes of an inverter through the gate to drain capacitance (C_{GD}) can feed charge into a node. It is more plausible in Hyper-FET based circuits since the supply buses cannot directly drive the output in static mode due to high insulating state resistivity of the PTM. Let us consider the case when OUT is at 0. Due to C_{GD}, the voltage at node OUT (Figs. 6.20 (a), (b)) rises. However, as the voltage of OUT changes, it starts sharing charge with the inherent capacitance of the PTM (Fig. 6.20 (b)). If the output noise increases beyond a certain value, the voltage across PTM increases beyond $V_{C\text{-}IMT}$, triggering the transitions of the PTM to the metallic state (Fig. 6.20 (d)). Thus, the connection to ground gets re-established for a certain amount of time and the output noise in cancelled out. Similar explanation can be used to describe the origin and removal of the voltage droop in Fig. 6.20 (c). Likewise, for other noise sources, the dynamic change in the resistance of the PTM in response to increasing noise signal reduces its effect at the high impedance node. Concisely, properly designed Hyper-FET inverter will provide reasonably stable noise response in addition to performance improvement (at low V_{DD}). We end our comprehensive

discussion on Hyper-FET inverter here and examine the possibility of implementing other logic gates up next.

6.11 Hyper-FET Based NAND and NOR Gates

In more complex CMOS logic, two or more transistors may need to be stacked in series. However, in stacked structures with two or more transistors, we only use one PTM and connect it to the transistor closest to the supply rail (V_{DD} or *Gnd*) (Fig. 6.21 (a)). This allows contact sharing between stacked transistors (Fig. 6.21 (b)) and avoids very large series resistance in the circuit. In a regular CMOS logic, transistors are appropriately sized to provide equal rise and fall time. For Hyper-FETs, an additional constraint is that the hysteresis in transfer characteristics can change due to transistor stacking. But, it is assuring

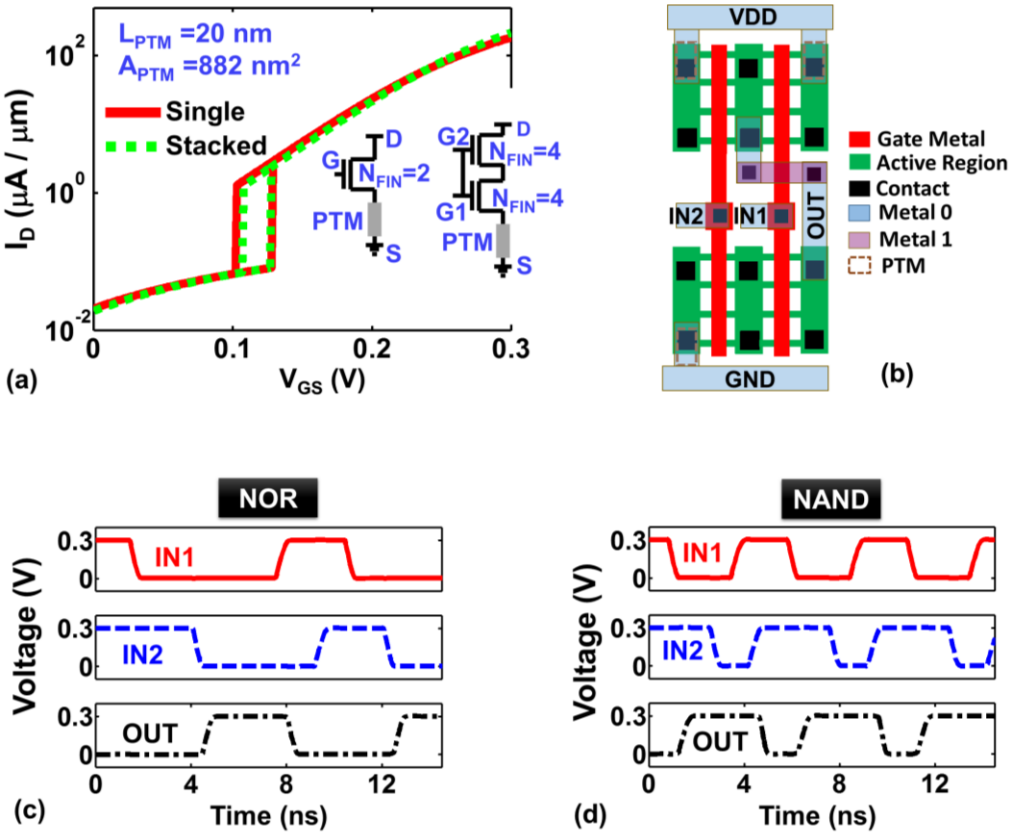


Fig. 6.21 (a) Through proper sizing of transistors, stacked Hyper-FET structure can present identical characteristics as a single device. (b) Layout of a Hyper-FET based NAND gate. Transient waveforms for (c) NOR and (d) NAND gates designed with Hyper-FET.

to note, Hyper-FETs can also be properly sized to redesign hysteresis as shown in Fig. 6.21 (a). That ensures the possibility of implementing complex logic functions using Hyper-FETs. Two such examples have been provided in Figs. 6.21 (c) and (d), which show the NOR and NAND waveforms obtained from properly sized Hyper-FET based complementary logic.

6.12 Direction for Material Exploration

In this chapter, we have discussed about several constraints and requirements for optimum device-circuit co-design with Hyper-FET. All of these factors need to be carefully considered while choosing a PTM or optimizing its size. To organize these diverse insights discussed so far, we compile them in Table 6.2.

Table 6.2 Summary of Material Requirements Dictated by Design Constraints

Purpose	Material requirement
Inverter with $V_{OUT}/\ V_{IN} > 1$	$V_{GS\text{-}IMT} < V_{DD}/2\ @V_{DS} = V_{DD}/2$ & $V_{GS\text{-}MIT} < V_{DD}/2\ @V_{DS} = V_{DD}$ $\Rightarrow J_{C\text{-}IMT} \times \rho_{INS} \times L_{PTM} < V_{DD}/2$ & $J_{C\text{-}MIT} \times \rho_{MET} \times L_{PTM} < V_{DD}/2$
$V_{OH,MIN} > V_{DD}/2$, $V_{OL,MAX} < V_{DD}/2$	R_{INS} < Transistor OFF resistance
Rail to rail swing	$V_{DS\text{-}MIT} < 1\text{mV} \Rightarrow J_{C\text{-}MIT} < 1.5\text{x}10^6\ \text{A/cm}^2$ For nominal values of geometry and other parameters.
Avoid charge sharing	$C_{PTM} << C_{LOAD}$
Reduce RO delay	PTM transition time << Intrinsic delay of the FET
General	High endurance and thermal stability

Considering the constraints on material parameters discussed in this chapter, we evaluate the characteristics of a few phase transition materials and provide the target direction for tailoring their properties (Table 6.3). For our assessment, we use the reported material parameters for Cu-doped HfO_2, single-crystal VO_2 and doped chalcogenide from [67], [143]

and [73] respectively. Table 6.2 and 6.3 will be instrumental for material exploration and to set targets to tailor the characteristics of the existing PTMs.

Table 6.3 Assessment of Feasibility of some Currently Available PTMs

Material	$J_{C\text{-}IMT}$	$J_{C\text{-}MIT}$	ρ_{INS}	ρ_{MET}
Cu-doped HfO_2	Not feasible	Not feasible	Need to be reduced	Need to be reduced
Single Crystal VO_2	Feasible	Feasible	Feasible, increase for better performance	Feasible, reduce for better performance
Doped Chalcogenide	Feasible	Feasible	Need to be reduced	Need to be reduced

6.13 Summary

We presented the device and circuit level analysis and co-design methodology for Hyper-FETs. We established the requirements of the phase transition materials for proper device/circuit operation and functionality. We discussed the constraints and feasible ranges for critical switching currents and the impact of resistivity ratio on I_{ON} / I_{OFF} of Hyper-FETs. We explored the ways to tune the hysteresis in the transfer and output characteristics of Hyper-FET. Our analysis showed that several design aspects need to be considered to exploit the targeted benefits from Hyper-FET. We reported that "*dead zone*" in the output characteristics of Hyper-FET can be eliminated if V_{DS-MIT} is maintained below 1 μV. In addition, we evaluated the dynamic performance of Hyper-FET based logic (inverter, NAND, NOR) with energy-delay benchmarking. Our analysis showed that several design aspects need to be considered to exploit the targeted benefits from Hyper-FET in functioning circuits. We showed that, *rail to rail* voltage swing is possible during dynamic operation of Hyper-FET based logic circuits. To achieve this $V_{DS\text{-}MIT}$ needs to be kept below 1 mV through proper material selection or geometry tuning. Issues like charge sharing can be avoided if the $C_{PTM} << C_{LOAD}$, which again calls for proper material choice. In addition, careful co-design of base transistor and PTM driven by the circuit requirements is essential to implement energy efficient circuits with superior performance and to avoid the

possibility of discrepancies like loss in the regenerative action of the logic gates. While, many of the reported PTMs may not fulfil *all* the requirements for optimal Hyper-FET design, further material exploration and optimization, as per the analysis presented in this paper can harness the full benefits of Hyper-FETs. Based on our comprehensive evaluation, an optimized Hyper-FET holds strong promise for providing superior performance at *iso*-energy than currently available transistors for low voltage operation, offering an exciting opportunity for future low power digital systems.

7. LOW POWER SENSE AMPLIFIER BASED ON PHASE TRANSITION MATERIAL

7.1 Introduction

Memories are one of the most important components of any high performance or low power processor, consuming a major portion of the chip area [166]. The overall performance, energy efficiency and yield of a system is heavily dependent on the memory speed, power, capacity and robustness [167]. As a result, an immense effort has been directed towards memory optimization and exploration of new techniques to improve the memory design [108], [167]. Several novel methods have been proposed at the device [167], circuit [108] and architecture levels [168] to improve, complement or even replace the conventional SRAMs. As a part of this effort, there has been an upsurge in the interest in non-volatile memory technologies, as discussed in chapters 2-4. While the bit-cell design of the emerging memory technologies poses several challenges due to self-conflicting design requirements, the design of low power robust peripheral circuits meeting the needs of the memory array is also critical. Amongst the peripheral circuits, the design of sense amplifiers for the new memory technologies has received widespread attention [169]. With the new memory technologies having different ranges of operating voltage, design requirements and sensing mechanisms, traditional sense amplifier designs prove to be sub-optimal. As an example, stability requirements of spin-transfer torque (STT) MRAMs necessitates the use of a low read voltage. This increases the challenges with respect to data sensing as low read voltage increases the design complexity of the sense amplifiers with regard to proper biasing and achieving sufficient voltage gain. Similarly, some memory technologies and architectures are more suitable for current sensing [92] rather than voltage sensing [93], [169]. As a result, novel sense amplifier architectures need to be explored to meet the demands of the emerging memory technologies.

Several research works have explored novel techniques to improve the performance, energy efficiency and robustness of the sensing operation [169]–[171]. While some approaches directly modify the design of the sense amplifier to counter the associated challenges [170], some others utilize the distinct features of the memory element to employ

novel sensing schemes, with an objective to relax the design requirements of the sense amplifiers [172]. In addition, several techniques are being explored for the generation of robust reference voltages and currents [169]. However, with each of the techniques having their own overheads, there is a need for novel methodologies for the design of low power robust sense amplifiers compatible with the new and emerging memory technologies. Most of the previous works have employed circuit techniques to improve the sense amplifier design [169], [172]. In this chapter, we present a novel approach of designing a sense amplifier based on PTM [173]. We exploit the distinct properties of PTM and Hyper-FET (discussed in chapter 6) [29] to design a low power sense amplifier. Before introducing our design, we provide a brief description of the existing sense amplifier topologies to streamline the subsequent discussions.

7.2 Conventional Sense Amplifier Topologies

Several topologies of sense amplifiers (SA) are being actively used and many are being proposed keeping in mind the unique requirements and limitations of different types of memory. In a broad perspective, sense amplifiers can be categorized into two major types- voltage mode and current mode SA. In conventional voltage sense amplifier, the bit line (BL) is pre-charged to a target voltage and then let discharge during sensing. The BL selectively discharges based on the state of memory stored in the cell. A voltage comparator is used to compare the sense node voltage with a reference and produce a digital output [169]. However, voltage sense amplifiers require high sense time for memories with low cell current (I_{CELL}) and/or high BL load. To improve the sensing speed in memory technologies with low sense current, charge-transfer based voltage sense amplifier is often used. But this topology is also vulnerable to BL offset [169].

Current mode sense amplifiers (CSA) are typically well known for high speed sensing. Cascode-Current-Load CSA (CCL-CSA), Global-Clamping-Local-Discharging CSA (GCLD-CSA) and current mirror based CSA (CM-CSA) are few common topologies in reported literature [169], [172], [174]. Differential input current mirror type SA is widely used for fast sensing. The basic component of this topology includes current mirrors to make copies of the cell current (I_{CELL}) and reference current (I_{REF}) to feed into a differential

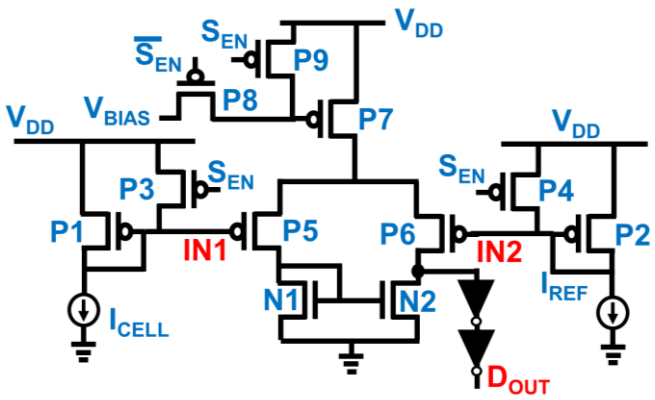


Fig. 7.1 conventional current based sense amplifier topology.

amplifier. The amplifier performs current-voltage conversion and comparison. Depending on the relative difference between the reference and the cell current input, sense node generates different voltage levels, which then is further processed by a buffer chain to produce a digital output. Fig. 7.1 shows a circuit diagram for such conventional CM-CSA [169]. Here P1 and P2 transistors convert I_{CELL} and I_{REF} (respectively) into voltages and feed into the inputs of the differential amplifier. This design requires proper biasing of transistors to ensure proper operating condition and can be susceptible to mismatches between the two legs of the amplifier.

The design that we introduce in this chapter, uses a unique principle of operation. It relies on the inherent ability of the PTM augmented transistor - Hyper-FET (discussed in chapter 6) to create abrupt threshold point to distinguish between levels of current/voltage in the memory cell. We describe that in more details in the next section.

7.3 Abrupt Threshold Point in Hyper-FET

The abrupt resistivity change in PTMs (Fig. 7.1 (a)) can be exploited to achieve steep (sub-*KT/q*) subthreshold switching in a transistor [22], [30], [175]. As discussed in chapter 6, such transistors (named- Hyper-FET) comprise of a PTM connected in series to the source of the transistor (inset of Fig. 7.2 (b)). The PTM electrically couples with the transistor to

invoke a negative differential resistance at the source terminal of the host transistor (S′). Fig. 7.2 (b) shows typical transfer characteristics (I_D - V_{GS}) of a p-type Hyper-FET (For details, refer to chapter 6). As V_{GS} is increased, the current through the transistor and PTM increases and once it becomes equal to $I_{C\text{-}IMT}$, the PTM undergoes transitions to the metallic state, which leads to an abrupt increase in the current, as illustrated in Fig, 7.2 (b). The gate-to-source voltage at which IMT occurs is denoted as $V_{GS\text{-}IMT}$. Similarly, when V_{GS} is reduced, the reduction in current triggers MIT at V_{GS} defined as $V_{GS\text{-}MIT}$. It may be noted that the inherent hysteretic behavior of the PTM translates to hysteresis in the I_D - V_{GS} plot. The abrupt change in current in response to increasing V_{GS} leads to interesting possibilities for low power circuit design. For $V_{GS} < V_{GS\text{-}IMT}$, the Hyper-FET remains in a high resistance state, while $V_{GS} > V_{GS\text{-}IMT}$ leads to the low resistance operation. In other words, due to its abrupt characteristics, Hyper-FET serves as a near-ideal component to distinguish between voltages lying in the range from 0 to $V_{GS\text{-}IMT}$ with that greater than $V_{GS\text{-}IMT}$. Therefore, $V_{GS\text{-}IMT}$ acts as a threshold and separator between low and high resistive states of the Hyper-FET (shown in Fig. 7.2 (c)). This has useful implications in the design of low power sense amplifiers. In the subsequent sections, we propose and describe the design of a sense amplifier based on the aforementioned properties of the PTM and Hyper-FET.

7.4 Phase Transition Material Based Sense Amplifier

Considering the challenges of the existing sense amplifier designs using scaled transistors, we propose a novel topology for a low power sense amplifier employing the PTM in conjunction with the CMOS circuits [173]. Fig. 7.3 shows the circuit diagrams for two versions of the proposed topology. The methodology that we propose can be utilized for both current-based (Fig. 7.3 (a)) and voltage-based sensing (Fig. 7.3 (b)). Note, the primary difference between the current-based design (Fig. 7.3 (a)) and the voltage-based design (Fig. 7.3 (b)) is that, the latter does not require current to voltage conversion. The current-based design pre-discharges its critical sensing node (X- in Fig. 7.3 (a)) before the sensing operation begins, whereas the voltage-based design does the opposite (pre-charge). To facilitate the pre-charge process, the core of the voltage-based design is implemented using a network of n-type transistors and an n-type Hyper-FET. Because of the similarity

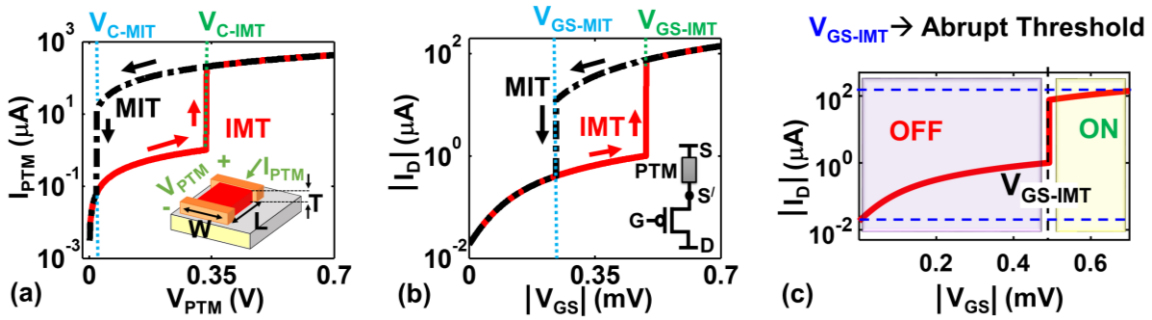


Fig. 7.2 (a) Current –voltage characteristics of a phase transition material-VO_2 illustrating IMT and MIT. Inset shows transport geometry and biasing scenario. (b) Transfer characteristics of a p-type Hyper-FET.

between the operation of the voltage and current based designs, we focus on discussing the current-based sensing (Fig. 7.3 (a)) only. The proposed circuit comprises three major sections as marked in Fig. 7.3 (a). The first section converts the current through a memory cell to a voltage level using a similar principle as in a conventional CSA design. A network of transistors is used to implement latching functionality and perform auxiliary functions. The core of the proposed amplifier contains a Hyper-FET (P2) coupled with regular transistors. The purpose of each of these components and the overall principle of operation have been described in detail in the next section.

7.4.1 Circuit Description and Principle of Operation

To achieve the proposed functionality from the sense amplifier described above, proper co-
A diode connected transistor P1 produces a voltage bias at node G (V_G) in response to the cell current flowing through it. For high resistive state (HRS) and low resistive state (LRS) of the memory, I_{CELL} is different and the corresponding values of V_G are $V_{G\text{-}LRS}$ and $V_{G\text{-}HRS}$. The node G is also the gate terminal of a p-type Hyper-FET (P2). The Hyper-FET transistor is designed (in terms of PTM geometry and transistor size) in such a way that, $(V_{DD} - V_{G\text{-}HRS}) < |V_{GS\text{-}IMT}| < (V_{DD} - V_{G\text{-}LRS})$. In other words, the Hyper-FET triggers IMT in the PTM for LRS of the memory cell, while restricting IMT for the HRS. Thus, the state of the memory cell is reflected in the phase of the PTM, which is then translated to a digital voltage by employing additional transistors in conjunction with the Hyper-FET. Transistor

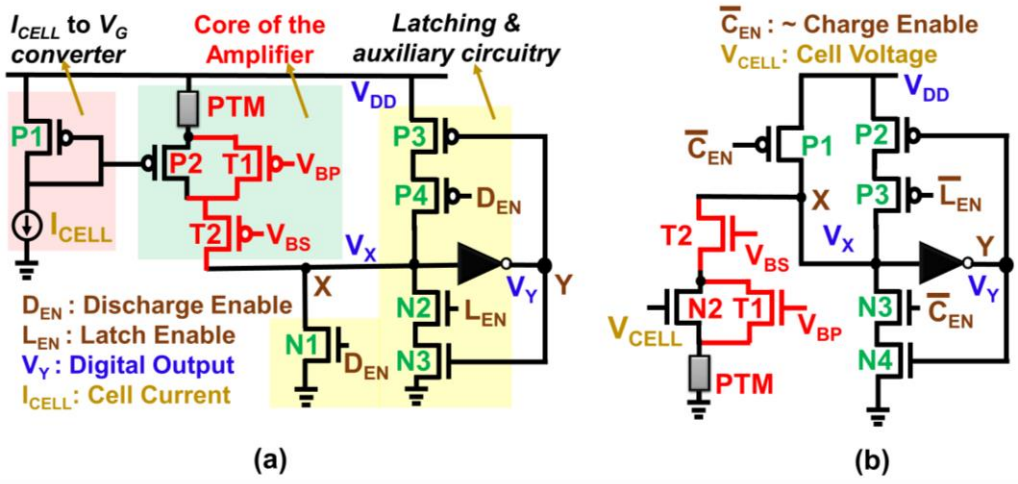


Fig. 7.3 Circuit diagrams of the proposed sense amplifier topologies illustrating (a) current based and (b) voltage based sensing.

N1 is used to pre-discharge node X before each sensing cycle. With V_X = 0, the drain-to-source voltage of the Hyper-FET ($|V_{DS}|$) is V_{DD}. In addition, the output of the inverter V_Y is pulled up to V_{DD}. Transistors N2, N3, P3 and P4 are used to latch the sensed data. During the sensing operation, the function of the inverter is to convert the node voltage generated at node X into full swing digital voltage. The D_{EN} signal, controls the pre-discharge of node X and L_{EN} controls the latching of the output. The purpose of the transistors T1 and T2 is to help in dynamic tuning of $V_{GS\text{-}IMT}$ and therefore the reference. We will discuss this feature in sub-section 7.4.3. Before that, we will omit these two transistors (T1, T2) from the circuit diagrams and the discussions to simplify the explanations and for ease of understanding.

The principle of operation of the proposed cell is illustrated in Fig. 7.4. While the memory cell is in the unaccessed mode and I_{CELL} =0, the gate voltage of P1 and the Hyper-FET is V_{DD} (*i.e.* V_{GS} = 0 V). Hence, the sense amplifier is in the inactive mode and the PTM remains in the insulating state (Fig. 7.4 (a)). Let us first consider the stages for sensing the low resistance state of the memory. As mentioned before, $I_{CELL} = I_{LRS}$ triggers IMT in PTM (Fig. 7.4 (b)) since $|V_{GS}| = (V_{G\text{-}LRS} - V_{DD}) > V_{GS\text{-}IMT}$. As the PTM transitions into the metallic state, the Hyper-FET starts injecting current into node X and charges it up. D_{EN} is de-asserted during this time so that N1 does not create conflict with the charging process. As the

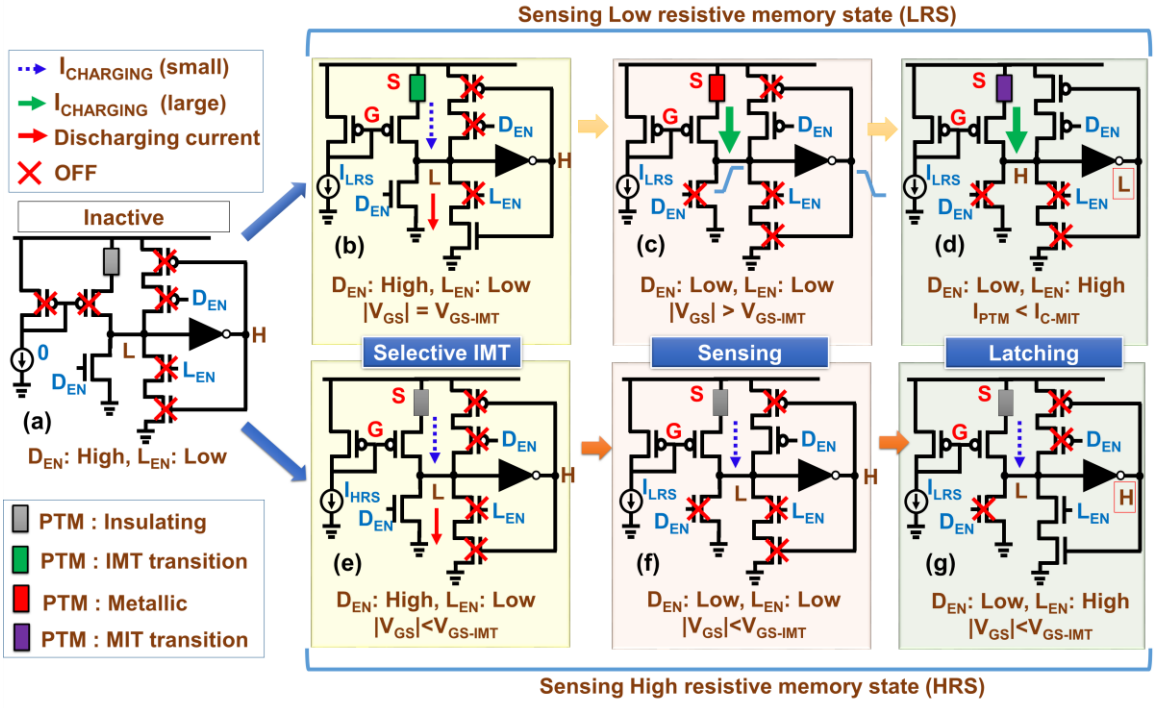


Fig. 7.4 (a) – (d) Steps of sensing low resistance state in the memory cell. (e) – (g) Steps for sensing high resistance state in the memory cell.

metallic state resistance of the PTM is low, (≈ 1.6 KΩ for our reported design), the charging occurs quickly. As V_X rises, V_Y keeps falling and that gradually turns ON the PMOS (P3). With D_{EN} set to 0 and P4 in the ON state, P3 and P4 help the Hyper-FET in charging up the node X, making the process even faster (Fig. 7.4 (c)). Note, as V_X rises, $|V_{DS}|$ across the Hyper-FET reduces and that eventually reduces the current. As the current (I_{VO2}) falls below $I_{C\text{-}MIT}$, the PTM starts undergoing MIT and P2 stops contributing to the charging of node X. However, P3 and P4, along with the inverter automatically latches the state at node X and Y (Fig. 7.4 (d)).

Let us now consider the case when $I_{CELL} = I_{HRS}$. As $(V_{DD}\text{-}V_{G\text{-}HRS}) < |V_{GS\text{-}IMT}|$ (by design), IMT is not triggered in the PTM (Fig. 7.4 (e)). So, the Hyper-FET can only supply very low current due to high insulating state resistance of the PTM (≈ 0.3 MΩ in our design) (Fig. 7.4 (e)). P2 still tries to pull up node X, but the time constant for charging is extremely high (Fig. 7.4 (f)). We use the L_{EN} signal to latch the output after a certain time during

sensing. Recall, since node X was pre-discharged to 0 before the sensing operation and V_Y was pulled-up to V_{DD}, N3 operates in the ON state. Hence, as L_{EN} is asserted, N2 and N3 pull down node X and latch the output (Fig. 7.4 (g)).

The time to assert $L_{EN,}$ essentially marks the end time for sensing and is determined by the LRS sensing. While sensing LRS, the PTM has to transition into metallic state to trigger the desired output change. Hence, the time taken for IMT is the major contributor to the total sense time. L_{EN} is asserted when the PTM completes transitioning into metallic state. So the sense time for our design can be formulated as: $T_{SENSE} = T_{SET\ UP\ :\ ICELL} + T_{IMT} + T_{MARGIN}$. Here, $T_{SET\ UP\ :\ ICELL}$ is the setup time for $I_{CELL,}$ After assertion of word line for sensing, the cell current (I_{CELL}) requires some time to reach its stable value. $T_{SET\ UP\ :\ ICELL}$ accounts for that time span. T_{IMT} is the IMT transition time (≈ 50 ps in our design [29], [86], [173]) and T_{MARGIN} is the safety time lag that we keep before asserting L_{EN}. This time lag is required to let the node X charge up and cross the logic threshold voltage level of the inverter to start changing the output. An important point to note, the sensing time is governed completely by the LRS sensing. Because, during HRS sensing, output does not change from its pre-set value (V_{DD}).

7.4.2 Design Methodology and Simulation Set-up

To achieve the proposed functionality from the sense amplifier described above, proper co-design between the devices and the circuit is required. Here, we present the methodology that we follow to design the proposed circuit. We also illustrate the functionality with the transient simulation results. For the analysis of the PTM, we use the compact model described in chapter 2 [161]. We extract the material parameters for VO_2 (a PTM) from epitaxial VO_2 films grown on Ti substrate using reactive oxide molecular beam epitaxy [30], [93]. The parameters are used to calibrate our model with the measured *I-V* data of VO_2 [30]. We use the 14 nm transistor technology node to simulate both the proposed and conventional sense amplifier topologies [162]. We also analyze a standard STT MRAM cell to obtain the levels of cell current with low and high resistance states of the memory [92]. We used a physics based compact model for the magnetic tunnel junction (MTJ) [101] with the same parameters as reported in Table 3.1. The simulated levels of cell current are

used as inputs for the conventional and proposed sense amplifiers. We use predictive technology model [103] to simulate the transistor characteristics. A list of relevant simulation parameters has been compiled in Table 7.1.

Table 7.1 List of Simulation Parameters and Specifications

Parameters	Values
ρ_{INS}	1 Ω.cm
ρ_{MET}	5×10^{-3} Ω.cm
$J_{C\text{-}IMT}$	8×10^{4}A/cm^2
$J_{C\text{-}MIT}$	1×10^{6} A/cm^2
L_{PTM} , A_{PTM}	42 nm, 60×21 nm^2
Technology, V_{DD}	14 nm FinFET, 0.7 V

We first analyze the transfer characteristics of the diode connected transistor P1 and find the values of V_G that will occur in response to I_{LRS} and I_{HRS} (Fig. 7.5 (a)). Then we choose a target $V_{GS\text{-}IMT}$, keeping ~equal margin from $V_{G\text{-}HRS}$ and $V_{G\text{-}LRS}$ (Fig. 7.5 (b)). To achieve the targeted $V_{GS\text{-}IMT}$, we generate a mapping of $V_{GS\text{-}IMT}$ in relation to the area and length of the PTM (in this case, VO_2) (Fig. 7.5 (c)). Using the mapping shown in Fig. 7.5 (c), we

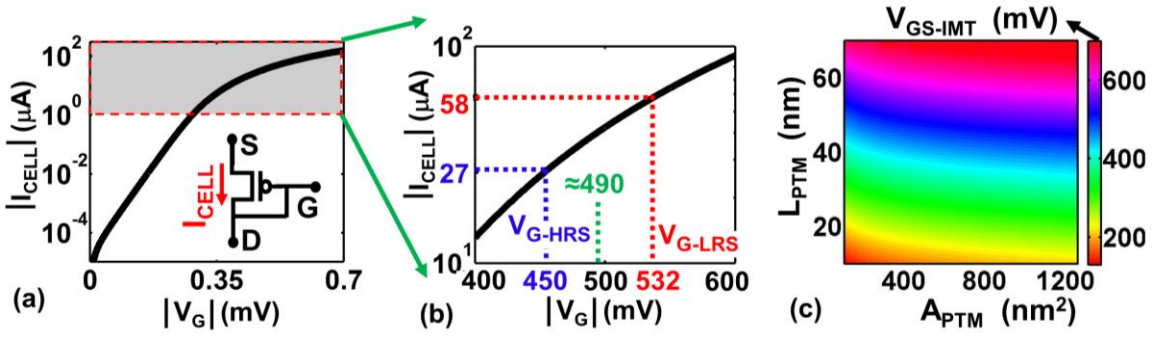


Fig. 7.5 (a) Transfer characteristics of the diode connected transistor P1 in Fig. 7.4. (b) Zoomed version of the super-threshold part of the transfer characteristics. This portion of the transfer characteristics is used to deduce the voltage values (V_G) generated by two levels of I_{CELL} (corresponding to LRS and HRS). The $V_{GS\text{-}IMT}$ must be designed to be between these two values of V_G. (c) Mapping of $V_{GS\text{-}IMT}$ with respect to geometry of PTM, showing possible options of length and area to achieve the desired $V_{GS\text{-}IMT}$.

choose the dimension of the PTM that yields desired $V_{GS\text{-}IMT}$ (≈ 490 mV). This is the process of 'design-time' reference tuning, which makes the sense amplifier compatible with the specific needs of a particular memory technology.

To validate the concept, we design and simulate the proposed sense amplifier topology. We perform transient simulations for memory cells storing LRS and HRS. Fig. 7.6 (a) – (d) show the simulated steps of sensing the LRS of the memory ($I_{CELL} = I_{LRS}$). Fig. 7.6 (b) illustrates the assertion of the control signals (L_{EN}, D_{EN}). Fig. 7.6 (c) demonstrates the change in output voltage level, occurring due to the switching of resistance states of the PTM (Fig. 7.6 (d)). Fig. 7.6 (e) – (h) show similar steps for sensing high resistance state of the memory ($I_{CELL} = I_{HRS}$). In this case, gate input to the Hyper-FET does not reach up to

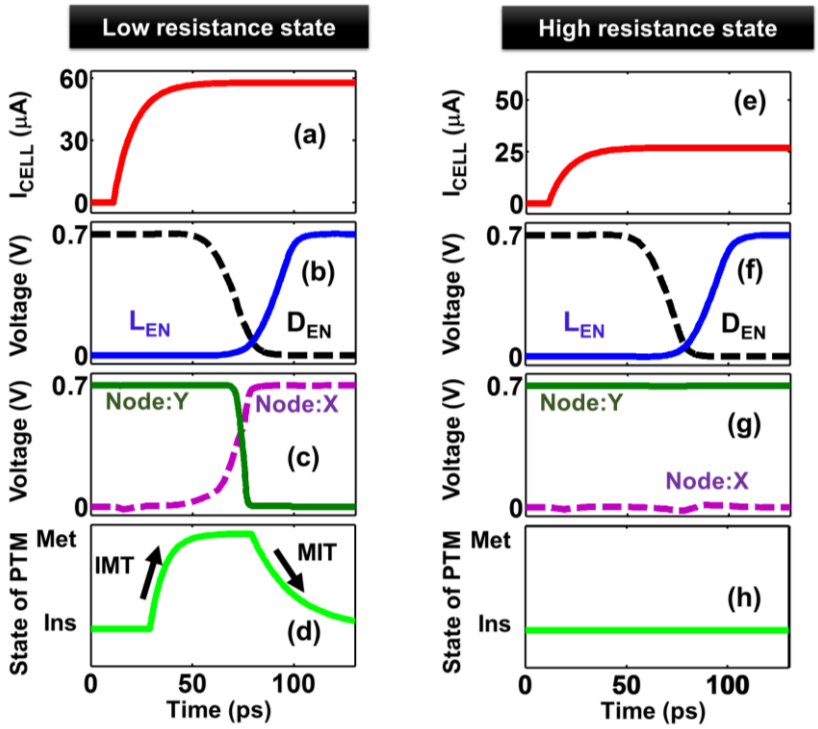


Fig. 7.6 (a) Transfer characteristics of the diode connected transistor P1 in Fig. 7.4. (b) Zoomed version of the super-threshold part of the transfer characteristics. This portion of the transfer characteristics is used to deduce the voltage values (V_G) generated by two levels of I_{CELL} (corresponding to LRS and HRS). The $V_{GS\text{-}IMT}$ must be designed to be between these two values of V_G. (c) Mapping of $V_{GS\text{-}IMT}$ with respect to geometry of PTM, showing possible options of length and area to achieve the desired $V_{GS\text{-}IMT}$.

$V_{GS\text{-}IMT}$ and hence the transistor passes very small amount of current. Therefore, node X cannot rise up to high value. From a different angle, during LRS sensing, the ON current of the Hyper-FET charges node X. For HRS, the OFF current charges node X. That creates a significant difference in charging time and practically V_X never considerably charges up in HRS sensing. On top of it, we enable the latching action that restricts gradual rise of V_X after the end of the sensing period (Figs. 7.6 (f), (d)). Fig. 7.6 (a) – (h) clearly demonstrate the intended functionality in the proposed design and thereby validates the concept in principle.

7.4.3 Dynamic Reference Tuning

An important point to note is that, our design does not require any external reference circuit or source. The $V_{GS\text{-}IMT}$, itself is the reference for differentiating between HRS and LRS. In the previous sub-section (7.4.2), we mentioned that $V_{GS\text{-}IMT}$ could be tuned and set by choosing appropriate dimensions (length, area) during the design phase. However, due to process variations, there could be considerable deviations in the intended values of the reference (*i.e.* $V_{GS\text{-}IMT}$). Therefore, to counter global variations, dynamic tuning of the reference is required. We propose an approach to change $V_{GS\text{-}IMT}$ dynamically according to the global process corner. Fig. 7.7 (a) highlights the important part of the proposed circuit with dynamic $V_{GS\text{-}IMT}$ tuning capability. Two additional PMOS transistors (T1 and T2) are used in conjunction with P2 to change $V_{GS\text{-}IMT}$ dynamically. We briefly mentioned about T1 and T2 in sub-section 7.4.1, but skipped describing their purpose detail. Here, we will explore their usage in detail. T1 and T2 are driven with different gate bias voltages (V_{BP} and V_{BS}), which could be independently set to different values. By changing V_{BP} and $V_{BS,}$ the resistance of T1 and T2 can be finely modulated. The purpose of using these transistors (T1 and T2) is to tailor the resistive voltage division between the PTM and its host transistor. T1, being in parallel with the host transistor of the Hyper-FET, can reduce the resistance of the combination if biased properly in the linear region of operation. When T1 is kept in saturation or cut-off mode, it cannot affect the overall resistance of the transistor combination. On the contrary, T2 is in series with the host P2 and can increase the resistance of the combination. In a Hyper-FET, $V_{GS\text{-}IMT}$ is determined by the relative resistance of the PTM and its host transistor. Hence, by manipulating the transistor's

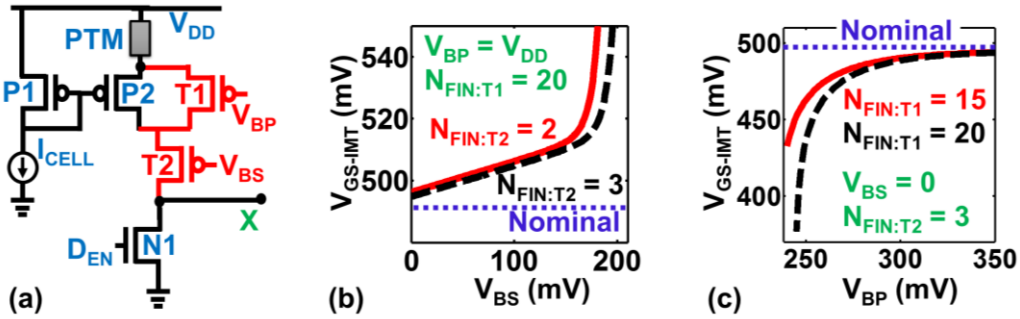


Fig. 7.7 (a) Additional transistors (T1 and T2) to provide dynamic tuning of $V_{GS\text{-}IMT}$ in the proposed topology. (b) Increasing $V_{GS\text{-}IMT}$ by tuning the gate bias of T2. (c) Reducing $V_{GS\text{-}IMT}$ by using proper biasing at the gate of T1.

resistance, we can tune $V_{GS\text{-}IMT}$. T1 is used to reduce $V_{GS\text{-}IMT}$ in case the global variations lead to reduction in the cell currents. Similarly, T2 is used to increase $V_{GS\text{-}IMT}$ from the nominal value (for the fast process corner). The responsiveness of $V_{GS\text{-}IMT}$ to the gate bias of these tuning transistors is evident in Fig. 7.7 (b) and (c). Note, the use of lesser number of fins is beneficial for T2, since that increases its resistance and makes it more influential over P2. However, T1 should have higher number of fins so that it can sufficiently contribute to reducing the overall resistance of the parallel combination.

7.4.4 High Performance and Low Power Designs

In continuation to the discussion so far, it is important to point out, P1 and P2 do not form a current mirror. Because a PTM is connected in series with, which operates in the insulating state for high resistance state of the cell. Only when the PTM transitions to the metallic phase, the cell current invokes current-flow through P2. This current (I_{PTM} in Fig. 7.8 (a)) is an important design parameter for the power and performance of the proposed circuit. Since I_{PTM} flows (to a considerable extent) only when the memory cell is in the low resistance state, it affects the power and speed of LRS sensing. Large I_{PTM} speeds up the charging at node X and thereby yields faster sensing. However, that also increases the power consumption of the circuit. The metallic state resistance of the PTM determines the magnitude of I_{PTM}. Note, same $V_{GS\text{-}IMT}$ can be achieved by choosing different combinations of dimensions of the PTM. Two such choices and results have been shown in Figs. 7.8 (b), (c). $V_{GS\text{-}IMT}$ is strongly affected by the length of PTM and hence by decreasing the length,

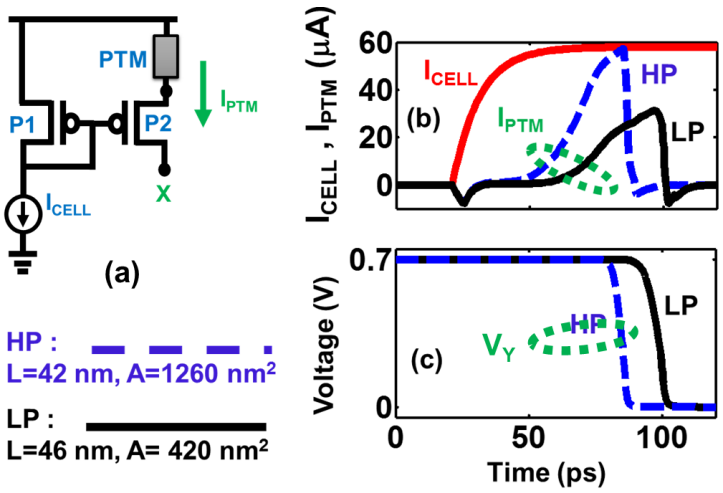


Fig. 7.8 (a) Representation of I_{CELL} *and* $I_{PTM.}$ (b) Different levels of I_{PTM} flowing in response of the same value of I_{CELL} = I_{LRS}. The difference occurs due to choosing different dimensions of PTM to achieve same $V_{GS\text{-}IMT}$. One choice of geometry leads to high performance (HP) through faster sensing. Another choice leads to low power (LP) with reduced speed. (c) Relative switching of output voltage (V_Y) in same scenario, showing faster transition in HP configuration.

we get a scope to increase the area significantly, maintaining the same $V_{GS\text{-}IMT}$ (shown in Fig. 7.5 (c)). But, resistance of the PTM reduces due to such increase in area (and reduction in length) and that eventually results in a larger current flow through the PTM. In other words, it is possible to maintain the same functionality and selectively choose high performance or low power, by carefully selecting the length-area combination of the PTM.

7.5 Effect of Variation

Mismatch between transistors is a serious cause for concern in conventional sense amplifier designs. Especially in scaled technologies, it is even more challenging to account for mismatches in sensing circuits. To minimize the effect of mismatch occurring due to random process variations, it is customary to use large transistor sizes. That renders adverse effect on the area and integration density of the chip. In our proposed topology, we use 6 fins for the transistors- P1 and P2 (Fig. 7.3 (a)). Here, P1 converts I_{CELL} into voltage and P2 creates the reference, $V_{GS\text{-}IMT.}$ Hence, to reduce the probability of failure due to variations, these two transistors need to be sized up. However, the other transistors, N2,

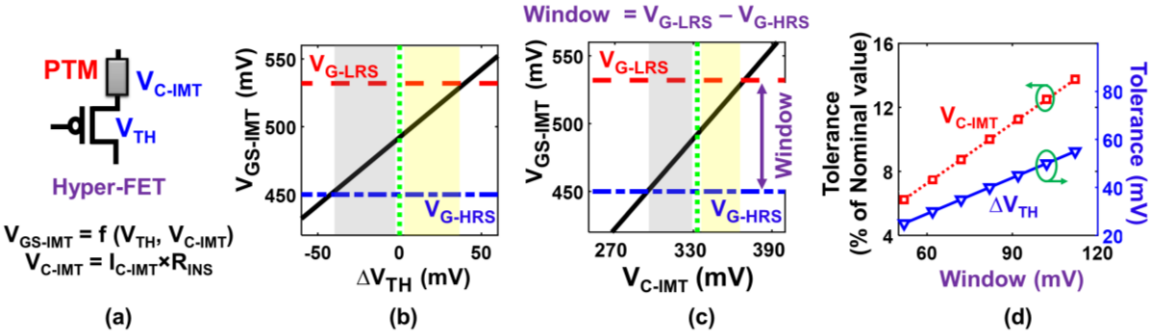


Fig. 7.9 (a) Major sources of variation in a Hyper-FET. $V_{GS\text{-}IMT}$ of the Hyper-FET changes with (a) the threshold voltage of the host transistor and (c) the inherent $V_{C\text{-}IMT}$ of the PTM. (d) Large memory window further improves variation tolerance in our design.

N3, P3, P4 and those in the inverter are not critically affected by variation. Since these transistors render feedback and perform operation in digital manner, they do not necessarily require large sizes. In our proposed circuit, the Hyper-FET (P2) is most susceptible to variations. Therefore, we perform a sensitivity analysis to identify the amount of variation that the Hyper-FET can tolerate without hurting the functionality.

Note, the host transistor and the PTM both contribute to the overall degree of variations in a Hyper-FET. The critical parameter to consider is $V_{GS\text{-}IMT,}$ which is affected by the threshold voltage (V_{TH}) of the transistor as well as the $V_{C\text{-}IMT}$ of the augmented PTM (Fig. 7.9 (a)). The variations in material parameters and geometry of the PTM are modeled together as variations in $V_{C\text{-}IMT}$. The sensitivity analysis of $V_{GS\text{-}IMT}$ shows that, ±40 mV V_{TH} variation in P2 or ±10% variation in $V_{C\text{-}IMT}$ can be tolerated (Figs. 7.9 (b), (c)). These results are for the sensing window = ($V_{G\text{-}LRS}$ - $V_{G\text{-}HRS}$) ≈82 mV, provided by spin memories used in our analysis. For larger sensing window, variation tolerance is further enhanced (Fig. 7.9 (c)). With ~100 mV of sensing window, the PTM segmented design can tolerate ~±50 mV variation in V_{TH} or over ±12% variation in $V_{C\text{-}IMT.}$ We also perform a worst-case variation analysis for our design to estimate the achievable improvements over conventional design. We discuss that in the next section.

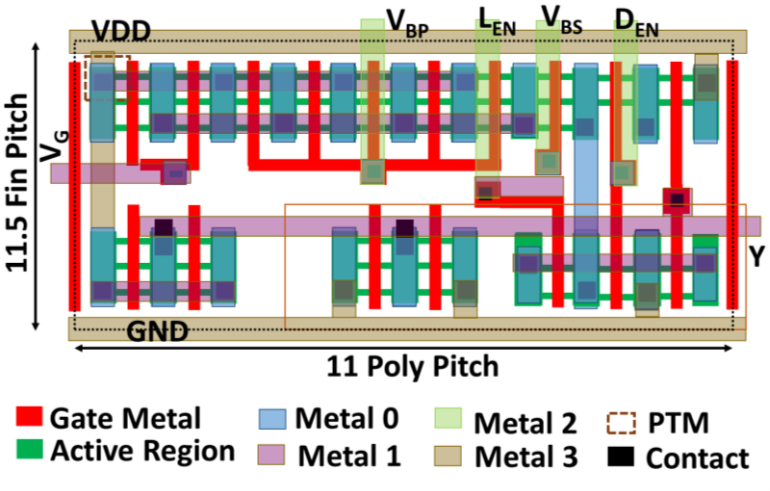


Fig. 7.10 Layout of the proposed sense amplifier topology.

7.6 Evaluation of Layout and Performance Metrics

As just mentioned in the previous section, the proposed circuit topology does not require larger sizes for all the transistors. That eventually gives significant area advantage over conventional sense amplifier. Moreover, or design uses a smaller number of transistors compared to most of the conventional designs. The layout of the proposed design is shown in Fig. 7.10. The layout has been drawn using λ based rules and in compliance with Intel's 14 nm FinFET technology parameters [162]. Our design achieves 42%-45% reduction in sensing power, 32% decrease in sensing time and 74% less area (considering layout in Fig. 7.10) in comparison to standard current based SA [169], [172]. The sensing delay of the proposed SA is dependent on the IMT time (assumed ≈50 ps based on projections from experiments [86]). Considering worst-case *simultaneous* variations in all parameters of PTM and V_{TH} of each transistor in our SA, 18% delay reduction is achieved compared to standard SA. Table 7.2 shows detailed results of the performance comparison and the relevant parameters of the variation analysis.

Table 7.2 Comparison of Performance Metrics

	Conventional		Proposed		Reduction	Parameters for Worst-Case Variation Analysis
Power (μW)	Nom	82.7	Nom	48.3	42 %	Variation in- V_{TH}: ± 25 mV/Fin $V_{C\text{-}IMT}$: ± 5% R_{METAL}: ± 5% (Simultaneous)
Delay (ps)	Nom	96.3	Nom	65.4	32 %	
	Var	98.5	Var	81.4	18 %	
Area	1.45 μm^2		0.37 μm^2		74 %	
Nom: Nominal, Var: With worst case variation						

7.7 Summary

We propose a novel sense amplifier topology, which exploits the orders of magnitude difference in the levels of resistivity of the two phases of the PTM and the abruptness in the phase transition to achieve low power robust data sensing. The proposed design uses the inherent switching threshold of the PTM as the reference for sensing. Therefore, it does not require any separate circuitry to generate reference current or voltage. We discuss the design methodology for the PTM based sense amplifier along with the options to choose high performance or low power designs. We present a design approach to tune the reference dynamically to counter the effect of global process variations. We perform power, performance and area analysis revealing that our proposed structure shows higher performance, lower power and lower area compared to conventional sense amplifier topology. Our design does not mandate large sizes of all the transistors to counter the effects of random variations. Only a few critical transistors need be sized up to ensure required level of variation tolerance. The proposed concept is also applicable and extendable to several different memory technologies and is not restricted to any specific PTM. The primary target applications are non-volatile memory technologies, which utilize the resistance difference between their two states to perform the read operation.

8. HARNESSING UNIPOLAR THRESHOLD SWITCHES FOR ENHANCED RECTIFICATION

8.1 Introduction

The unique properties of phase transition materials (PTM) can be utilized to realize innovative designs at device, circuit and array levels. So far, we have focused on capitalizing the high ON-OFF ratio, hysteresis and abrupt transitions in PTMs. Interestingly, some PTMs (e.g. Ag/HfO_2/Si [21], Ag/HfO_2/Pt [115], [176] etc.) exhibit an additional feature of unipolar conduction. This special feature, along with the standard properties of PTMs, can be harnessed for diode-like rectifying behavior, which when coupled with its hysteretic characteristics, offers unique advantages. This chapter evaluates the feasibility of this interesting application of unipolar PTMs. We use Ag/HfO_2/Pt threshold switch (TS) as unipolar PTM in our analysis. This TS is one of the most recent inclusions in the group of unipolar PTMs and provides high selectivity (~10^7) [21], [115]. We present some exceptional benefits of this hysteretic rectifier (Ag/HfO_2/Pt TS) and demonstrate (through simulations) its circuit level implications. We implement a *Cockcroft-Walton Multiplier* (CWM) [177]–[180] utilizing conventional diode and Ag/HfO_2/Pt TS. This circuit is used to convert an AC pulse to a DC output with higher amplitude. The performance of a CWM is strongly dependent on the efficiency of the rectifying component. We analyze the performance of Ag/HfO_2/Pt based CWM and compare it against the conventional diode based design to illustrate the benefits of the TS based hysteretic rectifier.

8.2 Fabrication and Simulation Set-Up

We first discuss the procedure to fabricate Ag/HfO_2/Pt devices based on the works reported in [21] and [115]. The Ag/HfO_2/Pt threshold switch consists of a 60 nm Pt bottom electrode, a 4 nm HfO_2, and a 150 nm Ag top electrode [115], [176]. Fig. 8.1 (a) shows the scanning electron microscope (SEM) image of a cross-point structure where each point of intersection creates an Ag/HfO_2/Pt device [176]. Fig. 8.1 (b) shows the false colored SEM image of a single Ag/HfO_2/Pt device [115], [176]. The transmission electron microscope

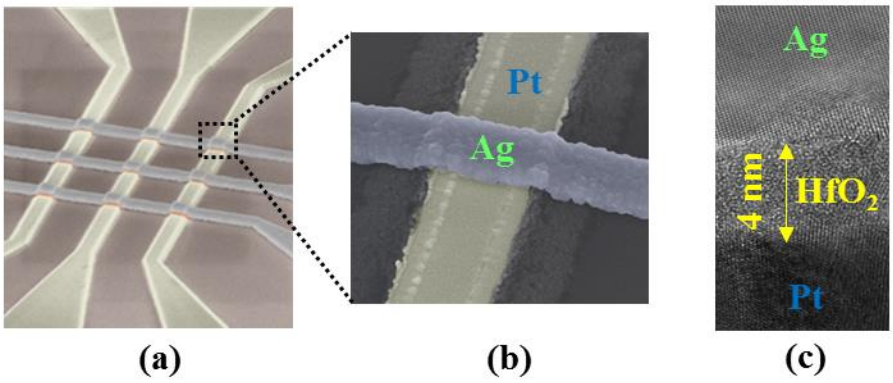


Fig. 8.1 (a) SEM image of group of Ag/HfO_2/Pt devices fabricated in a cross-point arrangement. (b) False colored SEM of a single Ag/HfO_2/Pt device. (c) TEM image showing cross section of the device.

(TEM) image in Fig. 8.1 (c) shows the cross section of the Ag/HfO2/Pt TS [115], [176]. Fabrication of the device starts with thermal growth of 90 nm SiO_2 on Si insulating substrate. Bottom electrode (Pt) is formed by electron beam lithography patterning and electron beam evaporation of 15 nm/60 nm Ti/Pt contacts. A 4 nm HfO2 film is then deposited using atomic layer deposition (ALD) at 120° C, forming a sub-stoichiometric, low density film with high interstitial site density. These interstitial sites have important implications in the device characteristics, as reported in [115].

The interstitial sites in HfO_2 allow the formation of Ag filaments (Fig. 8.2 (a)) when electric field is applied from the active Ag electrode towards the Pt electrode [115]. This will be subsequently referred to as positive polarity. If the voltage (with positive polarity) exceeds insulator-metal transition (IMT) threshold ($V_{C\text{-}IMT}$), the filament bridges the Ag and Pt electrodes. Thus, a low resistive path is created between the two terminals of the device, which is equivalent to its metallic state. When the applied voltage (with positive polarity) drops below metal-insulator transition (MIT) threshold ($V_{C\text{-}MIT}$), the filament is ruptured. In this condition, the device exhibits very high resistance (insulating state). For opposite (negative) polarity, no filament formation takes place (Fig. 8.2 (b)). This is because the inert Pt electrode does not form any filament towards the Ag electrode. Therefore, with negative polarity of applied electric field, the device remains in insulating state (until it

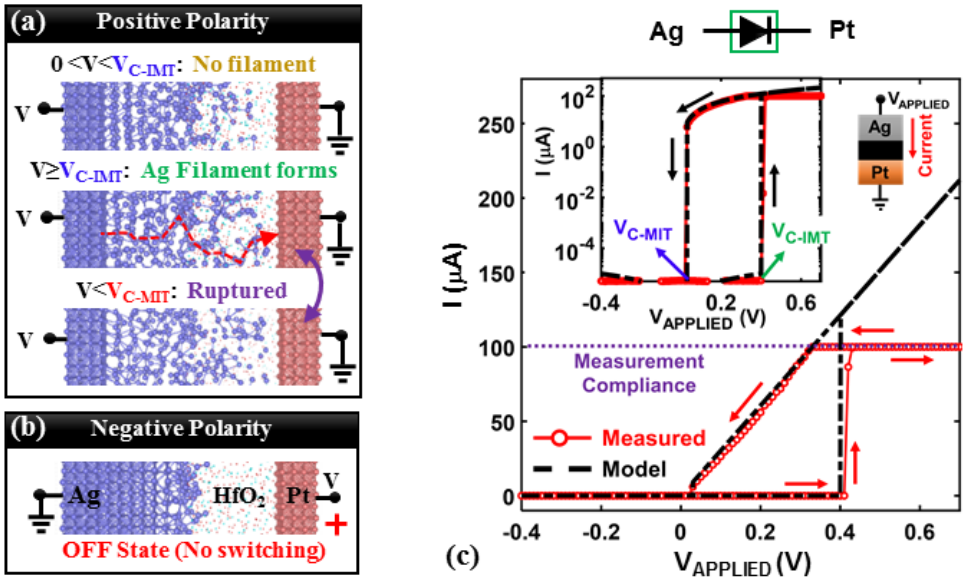


Fig. 8.2 (a) SEM image of group of Ag/HfO_2/Pt devices fabricated in a cross-point arrangement. (b) False colored SEM of a single Ag/HfO_2/Pt device. (c) TEM image showing cross section of the device.

breaks down). The unipolar behavior of Ag/HfO_2/Pt TS is clearly manifested in the measured current-voltage (*I-V*) characteristics shown in Fig. 8.2 (c) (data taken from [115]). Here, positive polarity of the applied voltage ($V_{APPLIED}$) denotes an electric field from Ag towards Pt. For positive $V_{APPLIED}$, the device exhibits metal-insulator phase transitions at certain thresholds. However, for negative $V_{APPLIED}$, all transitions are suppressed and the device allows very low current flow.

We use the measured *I-V* characteristics of Ag/HfO_2/Pt TS to extract material parameters and calibrate our compact model. The model is a variant of the SPICE based model described in chapter 2. The only exception in modeling approach is the incorporation of the unipolar response. The modified model not only considers the level of voltage across the TS device, but also assesses the polarity. The model output closely resembles the measured *I-V* characteristics (Fig. 8.2 (c)). Note, a current compliance of 100 μA was set during measurement [115]. Therefore, the measured characteristics flattens out beyond that level. The semilog plot of the *I-V* characteristics (Inset - Fig. 8.2 (c)) helps in identifying the thresholds for IMT and MIT transitions ($V_{C\text{-}IMT}$ and $V_{C\text{-}MIT}$).

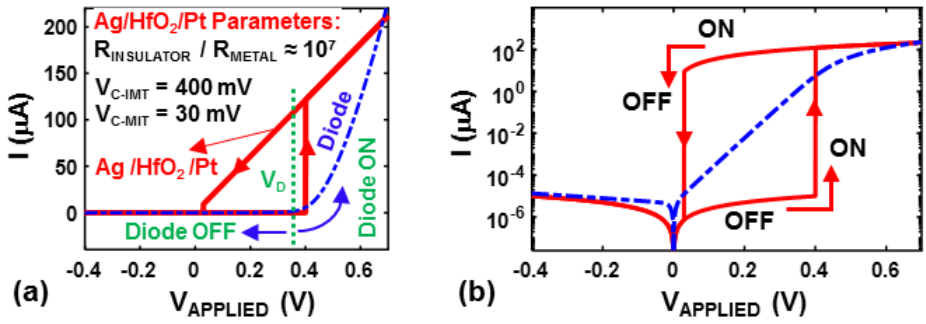


Fig. 8.3 *I-V* characteristics of a diode ((a) linear scale (b) semilog scale), designed to exhibit ~similar ON current and turn ON threshold ($V_D \approx V_{C\text{-}IMT}$) as those of the unipolar Ag/HfO_2/Pt. Unlike any diode, the turn ON and turn OFF thresholds for Ag/HfO_2/Pt is different due to its hysteretic characteristics.

8.3 Unipolar Ag/HfO_2/Pt TS versus Regular Diodes

The unipolar conduction in Ag/HfO_2/Pt is similar to a diode. However, there are several fundamental differences between the characteristics of this unipolar TS and that of any conventional diode (Schottky, p-n junction, transistor based etc. [181]–[184]). With positive polarity, a diode switches from ON→OFF and OFF→ON at around a specific voltage (V_D in Fig. 8.3 (a)). On the contrary, due to inherent hysteresis, Ag/HfO_2/Pt switches from ON→OFF at $V_{C\text{-}IMT}$ and OFF→ON at $V_{C\text{-}MIT}$ (Fig. 8.3 (b)). In addition, the abruptness of OFF↔ON switching makes the Ag/HfO_2/Pt distinct from diodes. We employ a transistor-based diode model [185] for the purpose of subsequent comparison. We use predictive technology model [103] at 14nm technology node [162] (LSTP version) to simulate the diode-connected transistor, which implements the diode functionality. We calibrate the diode and the Ag/HfO_2/Pt models to have similar ON-OFF ratio and turn-ON threshold ($V_D \approx V_{C\text{-}IMT}$) (Fig. 8.3). That ensures fair comparison between the conventional and proposed rectifier designs.

To illustrate the implication of hysteretic rectification (in Ag/HfO_2/Pt) as opposed to a non-hysteretic one (diode), we first analyze a simple diode/TD based circuit and analyze its step respone. (Fig. 8.4 (a)). This circuit charges a capacitor (C_{OUT}) through a rectifying element,

using an input voltage source (V_{IN}). The input (V_{IN}) steps up from zero to $V_{IN\text{-}P}$. For $V_{IN} > V_{C\text{-}IMT}$ ($\approx V_D$), the rectifying element (diode or Ag/HfO_2/Pt) turns ON and starts charging the output (V_{OUT}) (Fig. 8.4 (b)). As the output voltage charges, the effective voltage across the rectifying element (diode or Ag/HfO_2/Pt) gradually decreases. The diode turns OFF as soon as V_{OUT} exceeds V_{IN}-V_D. This is because, in this scenario, the voltage across the diode becomes less than V_D. On the other hand, the Ag/HfO_2/Pt still remains in low resistance state and keeps charging the output. As shown in Fig. 8.3, the Ag/HfO_2/Pt TS has distinct OFF→ON and ON→OFF transition thresholds due to its hysteretic nature. The ON→OFF transition level is very low (~30 mV) compared to the OFF→ON transition threshold ($V_{C\text{-}IMT} \approx$ 400 mV). As $V_{C\text{-}MIT} << V_D$, the output keeps on charging through the Ag/HfO_2/Pt rectifier and reaches at a much higher level ($V_{OUT} = V_{IN} - V_{C\text{-}MIT}$). Fig. 8.4 (b) clearly illustrates this difference between the conventional and Ag/HfO_2/Pt based rectifier. In addition to the voltage level, the IMT transition time (τ) of the TS is an important aspect to consider. The time to reach the final output is determined by the IMT time for Ag/HfO_2/Pt (Fig. 8.4 (b)), which can be in the order of ~1 ns [115]. We analyzed the performance of the TS based rectifier considering even slower transition times (2 ns and 3 ns). While the diode may switch faster than the TS, its inherent voltage drop ($V_{DROP} = V_D$) compels V_{OUT} to saturate at a lower voltage level than that allowed by Ag/HfO_2/Pt, which exhibits $V_{DROP} = V_{C\text{-}MIT}$ ($< V_D$). As long as the input is kept steady for a sufficiently long

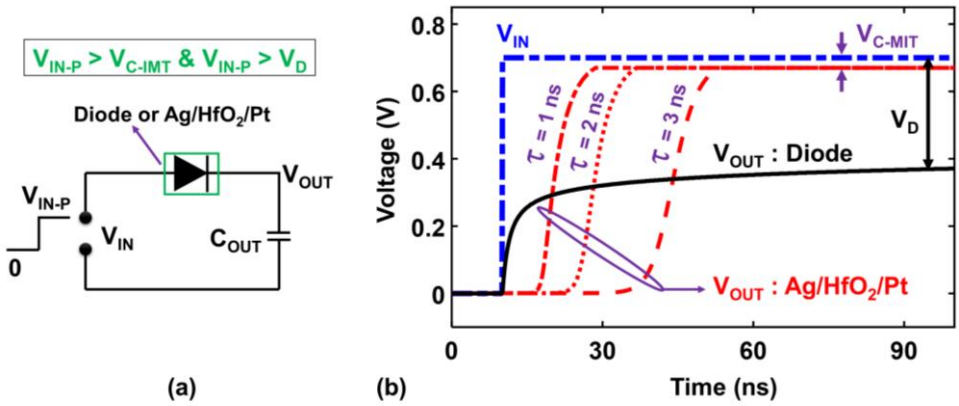


Fig. 8.4 (a) A simple circuit set-up to illustrate the advantage of a hysteretic rectifier. (b) Simulated step response of the circuit in (a), showing better performance with Ag/HfO_2/Pt compared with conventional diode.

time (> τ), Ag/HfO_2/Pt manages to charge the output up to a much higher level. With the understanding of this unique advantage that Ag/HfO_2/Pt based rectifier can provide, we now analyze its implications in a Cockcroft-Walton multiplier.

8.4 Cockcroft-Walton Multiplier (CWM) Design and Comparison

CWM is a standard and well-known circuit that can generate high levels of DC voltage from AC inputs (peak value: $V_{IN\text{-}PEAK}$). The basic version of conventional CWM [177], [186] comprises of diode-capacitor ladders as shown in Fig. 8.5. Each stage of this circuit comprises of two capacitors and two rectifying components (diodes). The final DC output depends on the number of stages used in the design. Ideally, the output for a CWM with N stages (at no load condition) should be $V_{OUT:\,N} = 2\times N\times V_{IN\text{-}PEAK}$. However, due to the voltage drops in the rectifiers, the output reaches up to a lower voltage level. The difference between the ideal and practical output levels depends on the number of stages used. At no-load condition, the N^{th} stage of CWM produces a DC output, $V_{OUT:\,N} = N\times (2\times V_{IN\text{-}PEAK} - V_{DROP})$. Recall, V_{DROP} is the loss in rectifying element (for diode: $V_{DROP} = V_D$ and for Ag/HfO_2/Pt: $V_{DROP} = V_{C\text{-}MIT}$). With a load, the output DC level reduces due to incomplete charging of the stage capacitors [186].

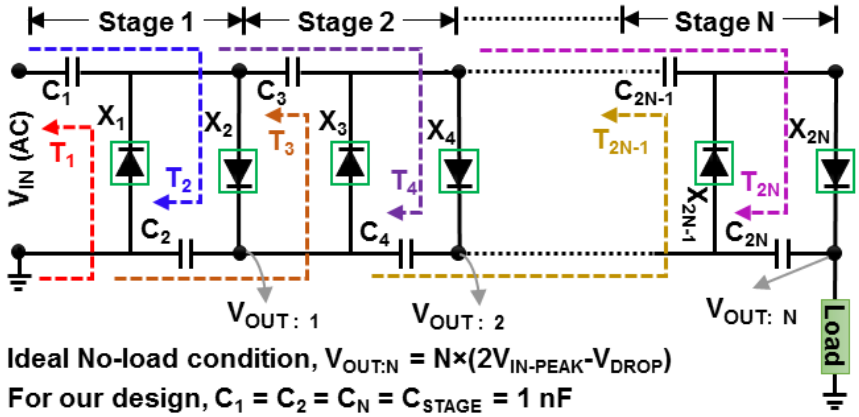


Fig. 8.5 An *N*-stage *Cockroft-Walton* multiplier (CWM) circuit. Here, X denotes regular diode or Ag/HfO_2/Pt. T_N represents N^{th} half-cycle of input.

We implement (in simulation) CWMs with different number of stages (up to 5) for our analysis. To represent conventional designs, we use transistor based diodes as the rectifying component. We implement corresponding versions of the CWM using our proposed Ag/HfO_2/Pt TS based hysteretic rectifier. Fig. 8.6 (a) shows that, the CWM designed with Ag/HfO_2/Pt produces ~40% higher DC output compared to CWM based on regular diode. The improvement becomes more pronounced with increased number of stages (Fig. 8.6 (a)). Note, selectivity and turn ON threshold for the two elements are kept same in the analysis, as discussed before**.** Therefore, the improvement observed here is a direct result of the advantage at the device level rendered by the hysteretic TS. This is a direct consequence of having $V_{DROP} = V_{C\text{-}MIT} (<V_D)$ in Ag/HfO_2/Pt. In practice, many more stages may be used in a CWM (depending on the target output DC level). Therefore, the margin of improvement is expected to be even higher.

The results shown in Fig. 8.6 (a) are obtained for a constant input frequency (1 MHz) and with 100 input cycles. We next analyze the performance with different levels of input frequency (f). Fig. 8.6 (b) shows that, Ag/HfO_2/Pt based CWM performs even better at

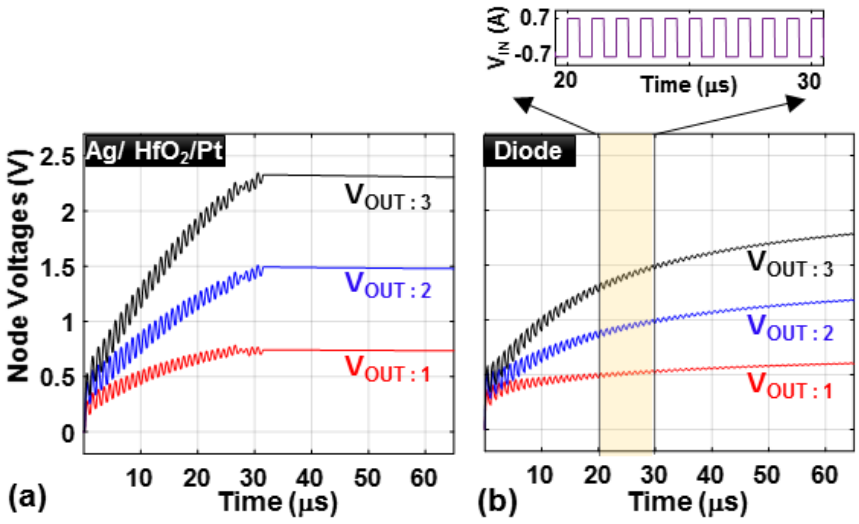


Fig. 8.6 Transient simulation of a 3 stage CWM based on (a) Ag/HfO_2/Pt and (b) regular diode. The former shows higher output (V_{OUT}) at every stage. [Inset: Input voltage used for both of the designs. $V_{IN\text{-}PEAK} > V_{C\text{-}IMT} (\approx V_D)$]

higher frequency. The reason is that, with each complete cycle of the input, the capacitors get charged up by a certain amount (ΔV), through the rectifiers. In the Ag/HfO_2/Pt based design, the extent of voltage drop in the rectifiers is negligible (compared with diode based design). In other words, the Ag/HfO_2/Pt based CWM accumulates higher level of charge per cycle in its stage capacitors. Higher frequency (more number of cycles) generates higher level of voltage at the output of Ag/HfO_2/Pt based CWM, within a certain time span. Therefore, given a constant time window, the Ag/HfO_2/Pt based design can charge up the stage capacitors to a much higher level. With 5 MHz of input frequency, the V_{OUT} (5^{th} stage) for Ag/HfO_2/Pt based design reaches at ~70 % higher output level compared to the diode based design. This trend is observed for, $f << 1/2\tau$. This range of frequency ensures that the TS can undergo IMT within each half-cycle of the oscillating input.

We also analyze the effect of transition thresholds of the TS ($V_{C\text{-}IMT}$ and $V_{C\text{-}MIT}$) on the device performance (Fig. 8.7 (a)). The Ag/HfO_2/Pt based CWM shows ~15%-50% larger V_{OUT} (Fig. 8.7 (a)) over the diode-based design across a range of turn ON voltages ($V_{C\text{-}IMT} \approx V_D$). The DC voltage level at the output reduces with increase in $V_{C\text{-}IMT}$ in Ag/HfO_2/Pt based design. High $V_{C\text{-}IMT}$ mandates a higher terminal voltage across the TS to turn in ON (invoke insulator-metal transition). In this scenario, the leading stages of the CWM (closest

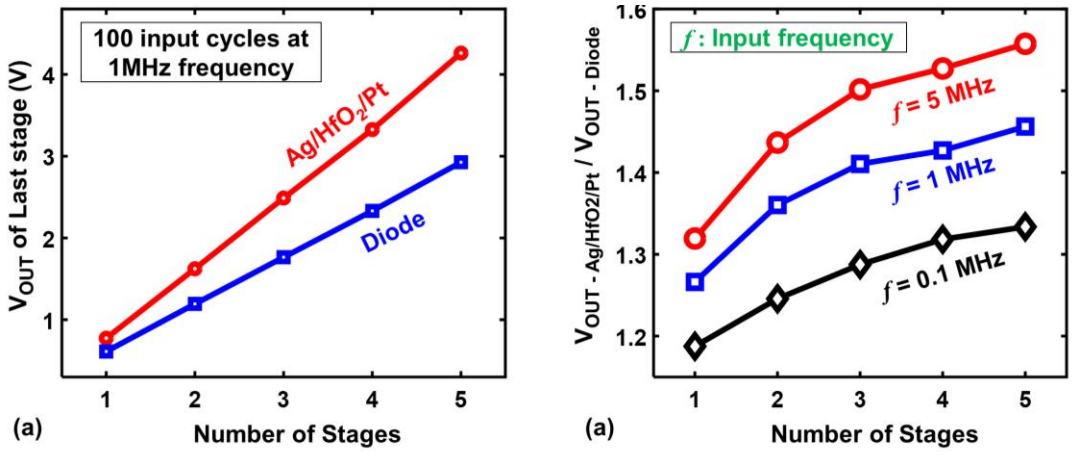


Fig. 8.7 (a) Achievable V_{OUT} in CWM with different # of stages, showing greater improvement for more stages. (b) High input frequency further boosts the improvement.

to input) need to generate high enough voltage levels at the intermediate output nodes ($V_{OUT:1}$, $V_{OUT:2}$ etc. in Fig. 8.5) to turn on the rectifiers of the subsequent stages. Before achieving sufficient voltage levels at these intermediate nodes, the capacitors at the latter stages receive very less charge through the insulating rectifiers. Lower $V_{C\text{-}IMT}$ ensures that all of the stages of the CWM can quickly accumulate sufficient voltage at output nodes and thereby manage to transfer charge efficiently from the input to the final output.

$V_{C\text{-}MIT}$ has even more vital influence on the performance of the CWM. Low $V_{C\text{-}MIT}$ (< 100 mV) is desirable to obtain best performance from Ag/HfO_2/Pt based design (Fig. 8.7 (b)). In our design, $V_{C\text{-}MIT}$ is equivalent to the diode drop in standard design. Recalling our discussion in section 8.3 and Fig. 8.4 (b), $V_{C\text{-}MIT}$ in our design plays the same role as the diode drop in standard rectifiers. As shown in Fig. 8.4 (b), an Ag/HfO_2/Pt device can only charge a load capacitor up to $V_{OUT} = V_{IN} - V_{C\text{-}MIT}$. Therefore, lower $V_{C\text{-}MIT}$ will ensure higher output levels at each stages of the CWM. Note, the results shown in Fig. 8.8 were obtained with $f << 1/2\tau$. It is also important to note that, lowering the V_D of a diode leads to penalty in its OFF current. But $V_{C\text{-}IMT}$ or $V_{C\text{-}MIT}$ can be reduced maintaining similar selectivity in TS [21], [115].

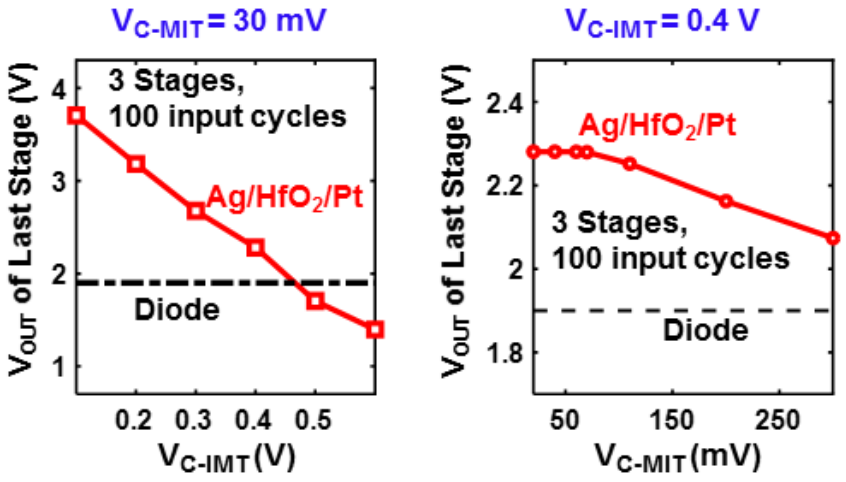


Fig. 8.8 Impact of (a) $V_{C\text{-}IMT}$ and (b) $V_{C\text{-}MIT}$ on the output voltage levels of Ag/HfO_2/Pt based CWM. Lower $V_{C\text{-}IMT}$ and $V_{C\text{-}MIT}$ lead to increase in V_{OUT}.

8.5 Summary

We introduced a new avenue of applications for unipolar threshold switching materials. The unipolarity and inherent hysteresis enable these materials to act as efficient rectifiers with unique benefits over conventional diodes. We utilized the unipolar, hysteretic and abrupt phase transitions of Ag/HfO_2/Pt to design a *Cockroft-Walton* multiplier. Ag/HfO_2/Pt based CWM achieved up to ~70% larger DC output compared to a diode-based design. While our analysis demonstrates the benefits of a hysteretic rectifier for a specific application, the utility of such devices is manifold. The concept of utilizing hysteresis in a rectifier can enable several unique benefits in rectifier-based circuits like envelope detectors, clipper-clampers and so on. This can also be utilized to design more efficient diode based circuits such as electro static discharge (ESD) protection circuits [187] for semiconductor ICs.

9. CONCLUSION

9.1 Summary

Phase transition materials (PTM), by dint of their unique characteristics, hold immense promise to be used for several emerging electronic applications. This dissertation explored and evaluated the suitability of PTMs as enablers to a number of device, circuit and array level innovations. The scope of this work spanned the applications of PTMs in designing steep switching transistor, optimized spintronic memory, cross-point array, peripheral circuits and analog converter. We used experimentally calibrated compact models to simulate and analyze the PTM based devices and circuits.

A major emphasis was given to the analysis of PTM augmented steep switching transistor, called Hyper-FET. The abrupt insulator-metal transitions and high level of selectivity of the PTMs are employed to realize sub-60 mV/decade swing in a Hyper-FET. We established the device-circuit co-design methodology for this novel device and identified its fundamental design constraints. Our analysis showed that, at low supply voltage (< 300 mV), Hyper-FET based inverters could exhibit up to ~70% less energy at *iso*-delay compared with FinFET based CMOS inverters. We presented the implications of different material parameters on device/circuit level characteristics. We described possible ways to tailor the inherent hysteresis of the device to ensure proper circuit level operations.

In addition to low-power logic design, PTMs can be used to improve non-volatile memory devices. We proposed a PTM augmented STT MRAM (named-TSA MRAM) to optimize the read operation with minimum effect on write performance. We proposed to connect a PTM in series with standard STT MRAM cell without increasing the cell area. We utilized selective phase transitions in PTM to boost the sense margin of the MRAM by 70% and (simultaneously) increase the read stability by over 25% (compared with standard STT MRAM). Monte-Carlo variation analysis showed that, the PTM augmented design could achieve ~1.7X larger bit line differential within a third of the time required by standard STT MRAM. Our design suffered only ~5% write time penalty with ~10% and ~40% less

power demand for write and read operations (respectively). We extended the concept of TSA MRAM operation to other variants of MRAMs that have separate read-write paths. These multi-port MRAMs provided a unique opportunity to implement parallel connection between MTJ and PTM, without affecting the write operation and integration density. This approach promised up to ~4.3X boost in Cell TMR, ~20% more data stability and 4X high sense margin compared to the conventional counterparts. Both of these PTM augmented designs mandate careful co-design between different components (the access transistor, memory element and the PTM) to ensure the intended operation. We analyzed and deduced valid ranges for the bias voltage to ensure proper operation in both of these designs.

In addition to their possible role in improving cell level performance, PTMs can play a major role in high-density array design for non-volatile memory. The threshold switching behavior and extreme non-linearity (in the *I-V* characteristics) make them ideal candidates for *selector* applications in a cross-point memory array. However, the design variables of the PTM, coupled with the complicated constraints of cross-point array, lead to a challenging and complex design space. We deduced the design constraints of a cross-point memory with PTM based selectors and established figures of merit to select feasible PTMs for this application. We reported detailed mechanism to co-optimize the biasing scheme, memory element, selector geometry and the material parameters of the PTM. We directed special attention to the estimation of leakage across the cross-point array, which is a vital determinant of the overall performance of the array. We developed a computationally efficient compact model for accurate estimation of sneak path leakage across the cross-point array. We developed a general framework for cross-point array and performed rigorous simulations for arrays with different sizes. Our compact model showed ~99% accurate matching with results from rigorous simulations for 16×16 through 256×256 cross-point array blocks. The model proved to be accurate for wide ranges of selector OFF state resistance (0.1 MΩ to 1 GΩ), interconnect resistance (1 mΩ/□ to 10 Ω/□) and access voltage (0.2 V to 1 V).

Besides their possible applications in the memory cell and array, PTMs can be employed to design improved peripheral circuits. We proposed a novel sense amplifier circuit

utilizing the threshold sensitive abrupt transitions of PTM. Our design achieved up to 45% reduction in sensing power, over 30% lower sense time and ~75% less area compared to a standard and mainstream current based sense amplifier in nominal condition. Our design offered a built-in reference and thereby averted the need to implement separate reference generator circuitry. This design also allowed both design time and dynamic tuning of the reference current/voltage to help counter global process variations. Due to its unique principle of operation, the proposed design could achieve a comparable level of variation tolerance by increasing the size of only two critical transistors, whereas the conventional design required sizing up all its transistors.

Finally, we explored applications of PTMs in the analog domain. We proposed an idea to achieve improved rectification by harnessing the unipolar and hysteretic phase transitions in Ag/HfO_2/Pt threshold switch (TS). Because of the hysteretic nature and very low metal-insulator transition threshold, the Ag/HfO_2/Pt TS led to very low (~30 mV) voltage drop during rectification. We implemented an AC to DC converter, known as *Cockcroft-Walton Multiplier* (CWM), to analyze the practical implications of the improved rectification in Ag/HfO_2/Pt. Compared to a conventional diode based CWM, the TS based design could produce ~70% larger DC voltage output (at 5^{th} stage). The improvements become more pronounced for larger number of stages, as the benefit provided by each rectifying device adds up. The Ag/HfO_2/Pt based CWM showed ~15% - 50% larger DC output than the diode-based design within a range (0.1 V – 0.4 V) of turn ON voltages. Lower metal-insulator transition threshold (< 100 mV) was required to obtain benefits over the standard design. Higher input frequency (*f*) was shown to be able to further enhance the performance of Ag/HfO_2/Pt rectifier, given that the phase transitions could take place within a half-cycle of the input pulse.

For all these applications, it is crucial to choose PTMs with high endurance, reliability and sufficient thermal stability. There have been demonstration of PTMs with endurance over billion cycles [67], [121]. Several PTMs have been shown to be thermally stable well over the operating temperature of electronic chips [121], [123], [124], [188]. PTMs with diverse ranges of resistance ratio and transition thresholds have been discovered [21], [22], [30],

[67], [73], [115], [116], [123], [146], [188]. The properties of the existing PTMs can be further tuned and tailored by using strain [75] and doping [125], [130]. Very fast transitions (sub-nanosecond) have been experimentally demonstrated in some PTMs [86], [189]. In many cases, the measurement of transition time is limited by the parasitics of the instruments [21], [86], [115]. Hence, in practice, much faster transitions are expected. A clear trend of further reduction in transition time with scaled dimensions was observed in [86]. It has been envisioned that, scaled dimension and use of point contact will significantly reduce the nucleation time and make the phase transitions even faster [86]. All of these aspects indicate that the PTMs can play an important role in enabling major innovations in next-generation electronics.

9.2 Outlook and Future Work

We have explored a wide range of possible applications for the exotic phase transition materials with a view to enabling unique features and advantages in digital/analog circuits and devices. There are several other fields of applications of these materials, which demand attention and some of which are already being explored. The following will be possible extensions of the research presented in this dissertation:

9.2.1 PTM Augmented Logic-in-Memory

Conventional Von Neumann architecture [190] requires frequent communication between logic and memory blocks. With ever-increasing complexity in digital applications, such communication has started to become a bottleneck for performance. Among many innovative ideas to mitigate this problem, implementing logic insider the memory (and *vice versa*) has garnered major attention. Recently, a logic-in-memory set up has been proposed in [191] for an array of STT MRAMs, where multiple word lines are turned ON simultaneously to create different levels of read current. A sense amplifier with variable reference is used to distinguish between the levels of current and accordingly provide digital output which mimics specific logic operations. With all of its promise, this technique suffers from low sense margin, especially with random process variations. A technique similar to that used for out TSA MRAM design (chapter 2) can be implemented with the design proposed in [191] to boost the difference between different levels of read

current and thereby improve the sense margin. In addition, it is possible to utilize our PTM based sense amplifier design (chapter 7) to provide the variable reference current required in this set up. Thereby, the peripheral overhead will be significantly reduced. But the feasibility and compatibility of these two ideas need to be assessed by extensive analysis.

9.2.2 PTM based Artificial Spiking Neuron

Brain inspired/neuromorphic computing has concurrently become a major topic of interest, due to its immense prospect in applications like image recognition and machine learning. A prime target in realizing a neuromorphic system is to develop artificial versions of the compute primitives (neuron and synapse) of the human brain. PTMs have the potential to exhibit oscillatory behavior if the material cannot become stable in metallic or insulating states. All of the applications covered in this dissertation mostly dealt with the stable mode of operation of the PTM, where they were stabilized in either metallic or insulating states. But, the PTMs can be forced to oscillate by augmenting them in series with other non-transitioning resistors and providing appropriate bias voltage [81], [82], [192], [193]. Such designs can be made to operate as spiking neurons to mimic the functionality of the neurons of human brain. Although a few prototypical demonstrations have been reported for such designs [82], [194], [195], there remains a strong need to perform comprehensive material to system level co-design to examine the implications and optimize this emerging design.

9.2.3 Hybrid Thermo-Electric Switching for Cryptography

PTMs exhibit metal-insulator and insulator-metal transitions when driven by electrical stimuli. But, they can also be triggered by thermal, optical and even magnetic stimuli. Particularly, the thermal effect on PTMs is of great influence in the device performance [196], [197]. The transition thresholds of some PTMs can be strongly influenced by the operating temperature [112], [197], [198]. For the designs proposed in this dissertation, it is important to ensure and provide sufficient design margins to account for temperature driven fluctuations in transitions thresholds. However, this may also provide another unique opportunity to introduce stochastic behavior in the system, by careful design. If designed properly, such hybrid thermos-electric transitions can be utilized for cryptography and hardware security.

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