

**SWITCH MODE RF POWER AMPLIFIER DESIGN, ANALYSIS AND  
IMPLEMENTATION**

by

**Feroz Ahmmed Bhuyan**

**A Thesis**

*Submitted to the Faculty of Purdue University*

*In Partial Fulfillment of the Requirements for the degree of*

**Master of Science in Engineering**



School of Electrical & Computer Engineering

Fort Wayne, Indiana

August 2019

**THE PURDUE UNIVERSITY GRADUATE SCHOOL  
STATEMENT OF COMMITTEE APPROVAL**

Dr. Abdullah Eroglu

Department of Electrical and Computer Engineering

Dr. Chao Chen

Department of Electrical and Computer Engineering

Dr. David Momoh

Department of Computer, Electrical and Information Technology

**Approved by:**

Dr. Chao Chen

Head of the Graduate Program

To my mentors and my family

## TABLE OF CONTENTS

LIST OF FIGURES .....	6
ABSTRACT.....	8
1. INTRODUCTION .....	9
1.1 The Basics of RF Power Amplifier.....	9
1.2 Definations of Efficiency .....	10
1.3 Gain Compression.....	11
1.4 AM-PM Conversion.....	11
1.5 Intermodulation Distortion.....	11
1.6 Adjacent Channel Power ratio .....	12
2. CLASSES OF POWER AMPLIFIERS.....	13
2.1 Working Principle.....	13
2.2 Types of Power Amplifier .....	14
2.2.1 Class A Amplifier .....	15
2.2.2 Class B Amplifier .....	16
2.2.3 Class AB Amplifier .....	17
2.2.4 Class C Amplifier .....	18
2.2.5 The Class-D Amplifier .....	19
2.2.6 Class-E Amplifier .....	20
3. AMPLIFIER DESIGN.....	22
3.1 The Basics of Design .....	22
3.2 Initial Design Decisions.....	23
3.2.1 Differential or Single-Ended Operation.....	23
3.2.2 Number of Stages.....	23
3.2.3 Gain & Efficiency Budget .....	24
3.3 Design of Individual Stages.....	24
3.3.1 Transistor Sizing and Load Impedance Selection.....	25
3.3.2 Source Impedance Selection.....	26
3.3.3 Design of Matching Networks.....	26
3.4 Combination of Stages.....	26

3.4.1 Design of Inter-stage Matching Networks.....	27
3.5 Harmonic filters .....	27
3.5.1 Type of filters.....	27
4.AMPLIFIER SIMULATION AND IMPLEMENTATION .....	30
4.1 Power Amplifier Design.....	30
4.2 DC Biasing.....	30
4.3 Amplifier Circuit Design .....	32
4.4 Amplifier Fine Tuning and Harmonics Reduction .....	34
4.5 Implementation .....	36
REFERENCES .....	43

## LIST OF FIGURES

Figure 1.1 Simple Power Amplifier .....	9
Figure 1.2 Principle of a two stage power amplifier.....	10
Figure 1.3 Output power as a function of input power .....	11
Figure 1.4 Third-order intermodulation products .....	12
Figure 2.1 Working principle of the PA .....	13
Figure 2.2 Various Classes of power amplifiers.....	14
Figure 2.3 Class A PA outputs.....	15
Figure 2.4 Class B RF PA output .....	17
Figure 2.5 Class AB $V_{DS}$ and $I_D$ .....	17
Figure 2.6 Class C Amplifier $V_{DS}$ and $I_D$ .....	18
Figure 2.7 Class D amplifier.....	20
Figure 2.8 Class-E amplifier .....	20
Figure 2.9 Drain and capacitor current and drain voltage of Class E PA.....	21
Figure 3.1 Flowchart for initial design concept.....	22
Figure 3.2 Design flow for initial design decisions .....	23
Figure 3.3 Design flow for individual stage design.....	24
Figure 3.4 Design flow for transistor sizing .....	25
Figure 3.5 Design flow for combination of individual stages .....	27
Figure 3.6 Frequency response of filters.....	28
Figure 3.7 Inductive model of low pass filter .....	29
Figure 3.8 Capacitive low pass filter .....	29
Figure 4.1 DC biasing of the MOSFET .....	30
Figure 4.2 DC Biasing. $V_{DS}$ VS $I_D$ curve.....	31
Figure 4.3 Amplifier circuit before fine tuning .....	32
Figure 4.4 Output of the amplifier before fine tuning .....	33
Figure 4.5 Voltage signals before fine tuning.....	33
Figure 4.6 Amplifier circuit after fine tuning .....	34
Figure 4.7 Output of the amplifier after fine tuning .....	35
Figure 4.8 Voltage signals after harmonics reduction .....	36

Figure 4.9 ESR VS Capacitance .....	37
Figure 4.10 Q VS Capacitance.....	37
Figure 4.11 Current rating VS capacitance.....	38
Figure 4.12 Impedance VS Frequency.....	38
Figure 4.13 Amplifier circuit design for PCB implementation .....	39
Figure 4.14 Copper top layer of PCB .....	39
Figure 4.15 Copper bottom layer of PCB .....	40
Figure 4.16 Component placement on the PCB.....	40
Figure 4.17 3D view of final PCB layout simulation .....	41
Figure 4.18 RF Power Amplifier-5MHz.....	42

## ABSTRACT

Author: Bhuyan, Feroz Ahmmed, .MSE

Institution: Purdue University

Degree Received: August 2019

Title: Switch Mode RF Power Amplifier Design, Analysis and Implementation

Committee Chair: Dr. Abdullah Eroglu

In the recent years, there has been an increased focus on RF power amplifiers for communications especially for wireless applications. The main reasons of focus include high integration of power amplifier and low cost of production. To be able to reach the goal some theory on RF power amplifiers is necessary. The different classes of operation are explained, then the principles of impedance matching is discussed. This includes the development of the simulated load-pull method and synthesis of impedance matching networks. Then the biasing of the power amplifier is discussed along with the stability issues. RF power amplifier designing, simulation and implementation at 5MHz is described in this thesis.

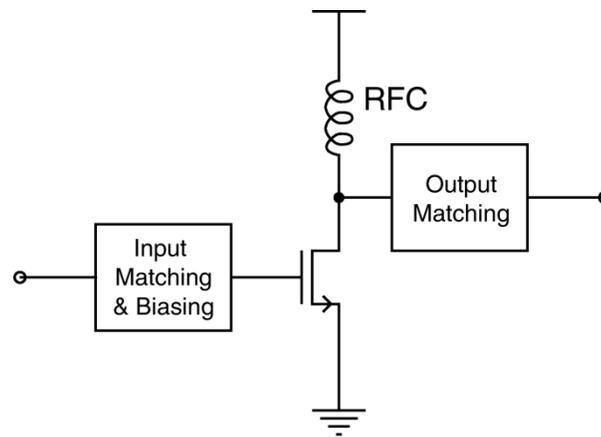
The issues of modeling a complete power amplifier are treated. This includes modeling of the circuit, the passive devices on-chip and off-chip as well as the package and PCB. To ease the design of power amplifier a design method is developed based on the theory and the experimental work.

At last the experimental work is described. The first part is a linearization system based on simulation. Then the RF power amplifier designed during the project are introduced. The power amplifier shows superior performance when at its operating frequency 5MHz. The output power of this power amplifier is 50.419dB. The power amplifier utilizes the design method develop as well as the models described. The accurate modeling combined with superior performance proves the future of integrated RF power amplifiers for wireless communication.

# 1. INTRODUCTION

## 1.1 The Basics of RF Power Amplifiers

A simple power amplifier is shown in Figure 1.1. The power amplifier consists of an input impedance matching network, an amplifying stage and an output impedance matching network[1]. Moreover, DC bias is applied at the input and output ports of the amplifying stage



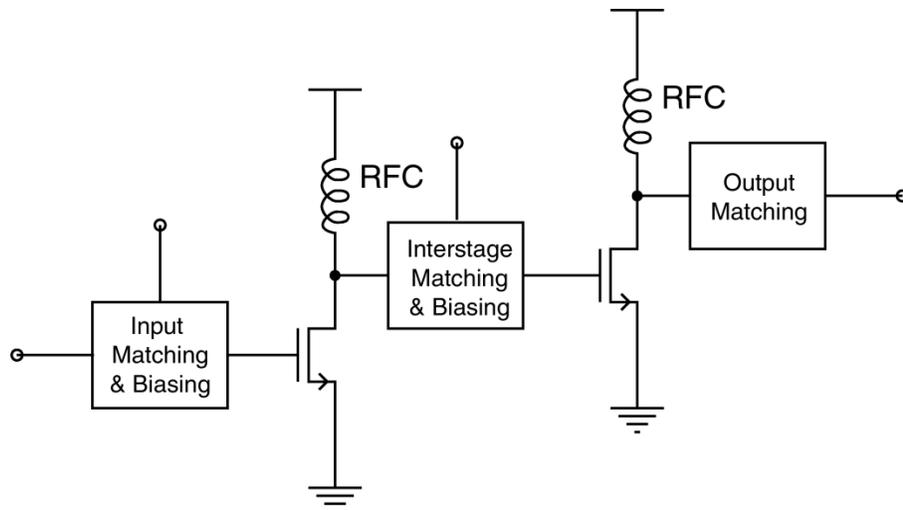
**Figure 1.1 Simple power amplifier.**

The power amplifiers can be described into narrowband and broadband power amplifiers. Narrowband power amplifiers are used in most communication systems, since they are usually more efficient than the broadband amplifiers.

The power amplifier has a number of characteristic properties that will now be explained. First of all the power gain of a power amplifier is defined as the output power divided by the input power:

$$G = \frac{P_{out}}{P_{in}}$$

In practice most power amplifiers can be multistage amplifiers to obtain desired power gain. The combination of several stages often introduces problems with stability of the power amplifier due to the increased gain from input to output [1]. The principle of a two stage power amplifier is shown in Figure 1.2



**Figure 1.2 Principle of a two-stage power amplifier.**

## 1.2 Definitions of Efficiency

The efficiency is one of the most important parts of the power amplifier, since a very large part of the total power dissipated in a RF circuit is inside the power amplifier. The efficiency is limited by the selected class of operation and the parasitic components. The efficiency can be expressed as either drain efficiency or power added efficiency. The drain efficiency is given by:

$$\eta_{drain} = \frac{P_{out}}{P_{DC}}$$

On the system level, the efficiency of the driver stages is also important, and then the power gain of the power amplifier must be included. The power gain of a power amplifier is also dependent

upon the class of operation, as well as the chosen technology. Different amplifier classes of operation have different relative power gains.

### 1.3 Gain Compression

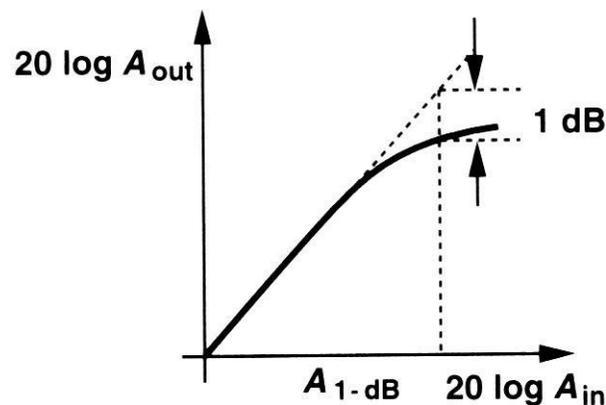
Gain compression describes the relationship when the input and output power levels is no longer linear. When the output power is 1dB less than expected by the linear relationship, it is called 1dB Gain Compression Point. The gain compression is also familiar as AM-AM conversion.

### 1.4 AM-PM Conversion

The phase shift of the power amplifier caused by the amplitude of the signal causes AM-PM conversion. This can be a effect of the non-linear drain- source capacitance of the transistor.

### 1.5 Intermodulation Distortion

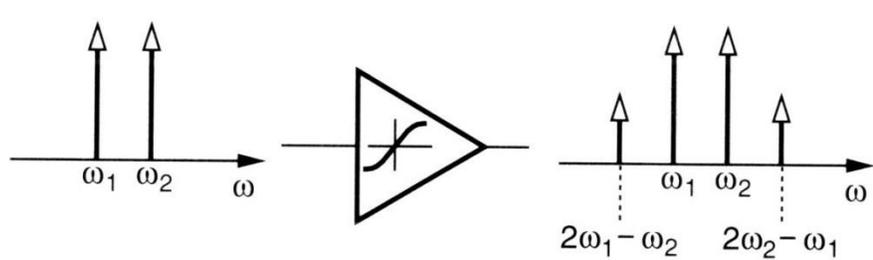
The harmonic distortion is caused by the nonlinear active components of the amplifier. The result is distortion components at integer multiples of the signal frequency.



**Figure 1.3 Output power as a function of input power.**

When multiple signals are present on the input, Inter-modulation distortion IMD is generated. The Nonlinearities of the amplifier is also a reason for the inter-modulation distortion. New

third-order signals are generated at e.g.  $2f_1 - f_2$  and  $2f_2 - f_1$ . The point at which the extrapolated power levels of the third-order products meet the wanted power is called the Third-order Intercept Point [2]. Although third-order distortions will probably be the most important a number of other orders may also be significant



**Figure 1.4 Third-order inter-modulation products.**

## 1.6 Adjacent Channel Power Ratio

The adjacent channel power ratio (ACPR) is one of the most important ways of characterizing the nonlinearity of a power amplifier in linear communication standards.

$$ACPR = \frac{P_{adj}}{P_{ch}}$$

## 2. CLASSES OF POWER AMPLIFIERS

### 2.1 Working Principle

Amplifiers hold an important functionality in radio frequency circuits. To ameliorate their performance, researchers are conducting experiments worldwide. The RF power amplifier amplifies a small input signal to large RF output power. Basic working process of RF amplifier is shown in Figure 2.1.

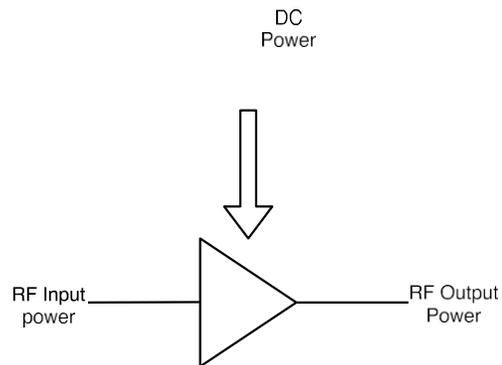


Figure 2.1: Working principle of the PA.

The efficiency of RF power is can be expressed by following equation:

$$\eta = \frac{P_{out}}{P_{DC}}$$

Unlike low noise amplifiers (LNA) where required DC power is small, in power amplifiers the requirement of DC power is really big as it is amplifying large signals. So, the performances of power amplifiers are considered as one of the important feature of amplifier design[3].

The inclusion of the power gain leads to the expression for power added efficiency:

$$\begin{aligned} \eta_{add} &= \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}} \left(1 - \frac{1}{G}\right) \\ &= \eta \frac{P_{out}}{P_{DC}} \end{aligned}$$

## 2.2 Types of Power Amplifiers

Power amplifiers can be classified into linear power amplifiers and non-linear power amplifiers. In linear power amplifiers, output signal is proportional to the input signal. Linear power amplifiers do not add huge harmonics in the output. It is a big benefit of using linear amplifiers. On the other hand, non-linear power amplifiers create a lot of harmonics in the output. It is because the non linear amplifiers operate at the cut-off region of the MOSFET and it causes to create harmonics. The non-linear power amplifiers always have higher efficiency with respect to linear power amplifiers. But the disadvantages are low quality output and the output signal is not proportional with input of the power amplifier.

Amplifiers are divided into two types. One type has common amplifiers, i.e. class A, B, AB and C amplifiers. These amplifiers are classified based on the current conduction angle at the output and the way their biasing is done. Other type of amplifiers basically switching mode amplifiers. These are class D,E,F,G amplifiers. These amplifiers are great for operating in specific frequency.

Figure2.2 shows the various types of radio frequency power amplifiers.

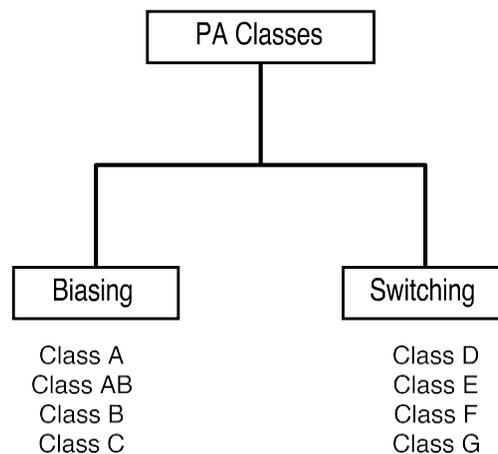


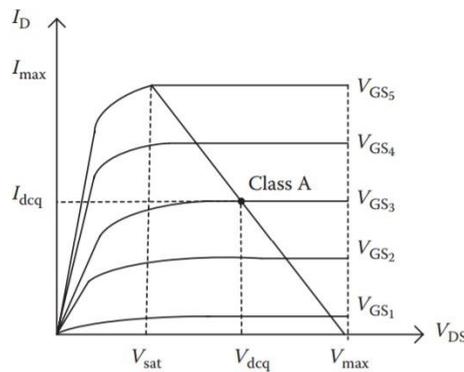
Figure 2.2: Various types of power amplifiers.

### 2.2.1 Class A Power Amplifier

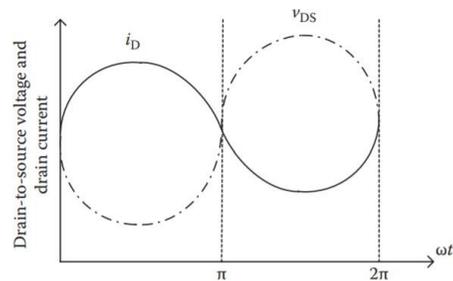
Class A power amplifiers operate in the linear region. The biasing of the amplifier is done between cut-off and saturation region. The conduction angle of this type of amplifier is  $360^\circ$ . The advantages of having 360 degree conduction angle is the output signal will contain full waveform.

In Figure 2.3, class A power amplifier load line and voltage vs current wave is displayed. When the drain voltage is  $0V$  to  $2V_{DC}$ , highest level of efficiency can be obtained in the class A PA. Class A power amplifier DC power equation:

$$P_{DC} = V_{DC} I_{DC} = \frac{V_{DC}^2}{R_L}$$



(a) Class A Power amplifier load line.



(b) Class A power amplifier  $V_{DS}$  and  $I_D$

Figure 2.3: Class A PA outputs.

The radio frequency power amplifier output is represented by following equation:

$$P_{out} = \frac{V_{DC}^2}{R_L}$$

In class A amplifier, the MOSFET conducts the full wave. But the efficiency of these type of amplifiers are lower than all classes of power amplifiers. These types of amplifiers are used for small scale signal amplification, such as low noise amplifiers. These amplifiers take small amount of DC power for amplification. They can be great fit for linear application, where linearity of output signal is more important than the efficiency of the amplifier.

### 2.2.2 Class B Amplifier

For these type of power amplifier, the transistor is biased in almost near to cut-off region. As a result, the transistor will get turned on at half cycle and it will be turned off for remaining half cycle. Finally, the conduction angle of class B amplifier is 180 degree.

The class B amplifier is biased in such a way that it amplifies only the positive part of the signal. In the remaining part of the time, the output from the amplifier is zero. Since the conduction angle of a class B amplifier is only 180°, a filter must be placed at the output in order to filter the harmonics out of the signal. Another way to retrieve the original signal is to couple two class B amplifiers in a push-pull configuration.

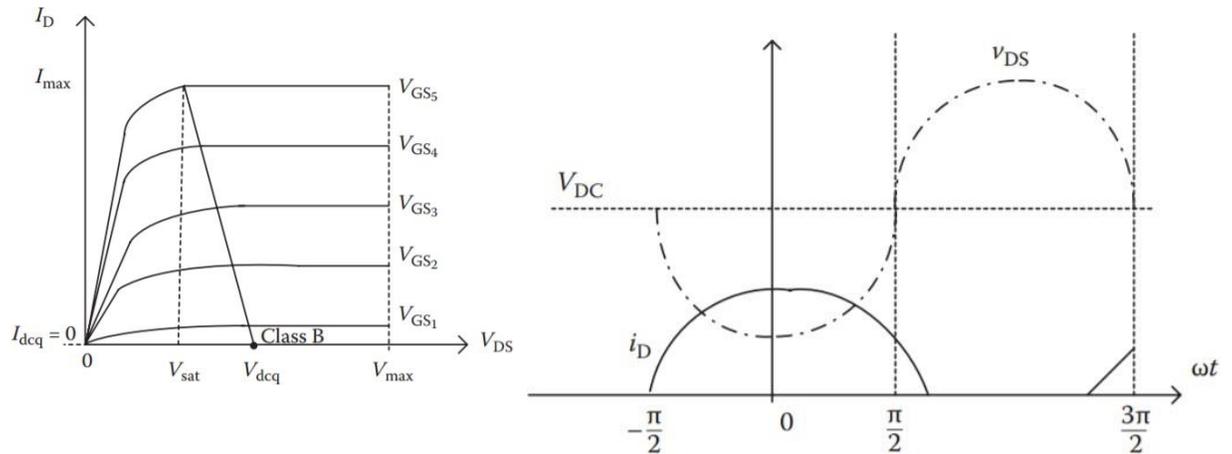
The class B amplifier is basically linear and has a maximum efficiency of 78.5% .

$$P_{DC} = V_{DC} I_{DC} = \frac{2}{\pi} I_m V_{DC}$$

The radio frequency output power is:

$$P_{DC} = \frac{1}{2} V_m I_m = \frac{1}{2} V_{DC} I_m$$

As class B amplifiers have small conduction angle, the efficiency of this type amplifier is higher than class A amplifier.



(a) Class B Power amplifier load line (b) Wave of Class B ( $V_{DS}$  and  $I_D$ )

Figure 2.4: Class B RF PA output.

### 2.2.3 Class AB Amplifier

Class AB amplifiers are biased in such a way that the conduction angle is between 180 degree and 360 degree. The maximal efficiency is therefore between 50% and 78.5% depending on the conduction angle. In practice most class B amplifiers will be designed slightly into the class AB region, due to the nonlinearities of the turn-on region in the transistor. This means that a vast majority of the power amplifiers for wireless communications operate in class AB

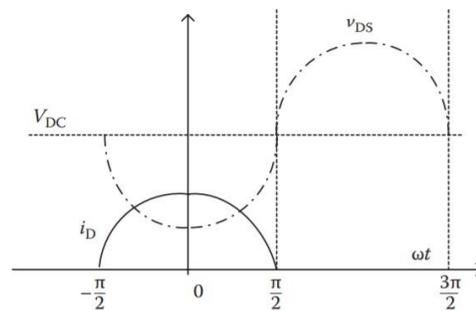


Figure 2.5: Class AB  $V_{DS}$  and  $I_D$

### 2.2.4 Class C Amplifier

In a class C amplifier the conduction angle is less than 180 degree. The efficiency depends upon the conduction angle and can ideally reach 100%. As the efficiency rises, the power gain decreases, and the power added efficiency, will eventually fall to 0. The Class C amplifier operates highly non-linearly.

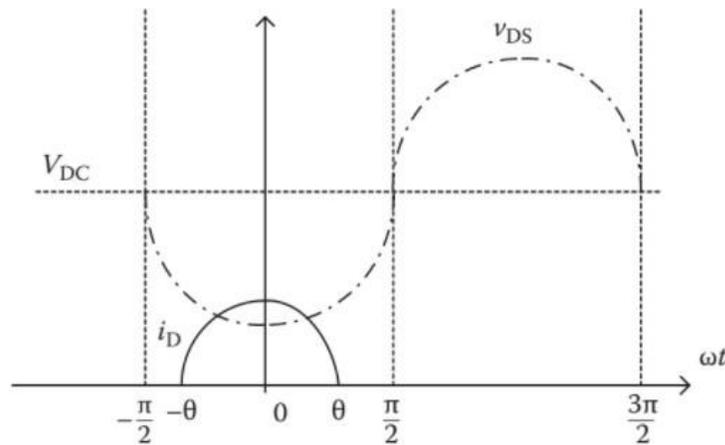


Figure 2.6: Class C Amplifier  $V_{DS}$  and  $I_D$ .

Efficiency for class C power amplifiers:

$$\eta = \frac{\theta - \sin \theta}{4[\sin(\theta/2) - (\theta/2)\cos(\theta/2)]}$$

$$P_{\text{out}} = \frac{I_p^2 \cdot R_L^2}{4\pi^2} \cdot (2\theta - \sin 2\theta)^2$$

$$P_{\text{DC}} = \frac{V_{\text{dd}} \cdot I_p}{\pi} \cdot (\sin \theta - \theta \cos \theta)$$

$$\eta_{\text{max}} = \frac{P_{\text{out}}}{P_{\text{DC}}} = \frac{2\theta - \sin 2\theta}{4(\sin \theta - \theta \cos \theta)}$$

### 2.2.5 The Class-D Amplifier

Class D amplifier modulates a signal, amplifies the signal. So, their efficiency is higher than other amplifiers. In portable audio device, this method can be applied. In cell phones and low power audio devices, where efficiency is a big concern class D amplifier can be a good fit. Furthermore, Class D, can also be used at larger systems [9].

Class D amplifier is not as simple as other amplifiers. Those amplifiers are popular because of their simple construction and easy building procedure. The application of Class D amplifiers are limited. In the recent times, Class D design has developed enough. There are lots of benefits for the use of these type amplifiers in audio amplifications. The problems are shrinking along with the research and developments.

Class D amplifiers have good efficiency, practically it can be over 95%. It is a remarkable achievement over the Class B amplifier, which can reach up to efficiency of 78.5%. For applications that handle high power, difference in efficiency is important because it makes a large savings in the amount of energy taken by the amplifier. Another advantage of this type amplifier is, for small amplifications, these amplifiers can be used at IC. For large amplifications, heat sinks are needed, but the dimension of the heat sink is shorter than on other amplifiers of equivalent power output.

The current through it is zero, when the transistor is off. The voltage across it is small and almost tends to zero, when it is on. The power consumption is very small in the described cases. As a result, the efficiency is increased and requires less amount of power. For these reasons, we also need smaller heat sink. For portable equipments, the size of the battery is very important and these conditions help to choose smaller battery sizes.

a bipolar power supply so that  $V_- = -V_+$ . The amplifier is built by two transistors (MOSFET) and driven by a comparator. There are two available inputs of the comparator. In one input, a triangle wave is given and in the other input audio signal is given.

$$v_C = -V_1 \text{ for } v_S > v_T \quad v_C = +V_1 \text{ for } v_S < v_T$$

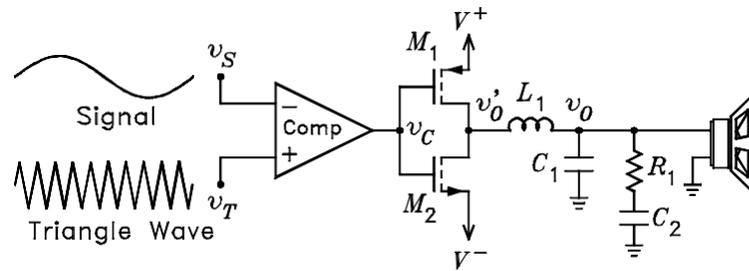


Figure 2.7: Class D amplifier

### 2.2.6 Class-E Amplifier

The class E amplifier is a tuned amplifier, which ideally can reach an efficiency of 100% [4]. The transistor works as a switch as is the case with class D amplifiers, but only one transistor is used. The basic idea is to delay the voltage curve so that the drain voltage does not rise till after the switching is done. This kind of operation causes the class E amplifier to be very nonlinear. Even for a non-ideal transistor the efficiency of a class E power amplifier can be quite high.

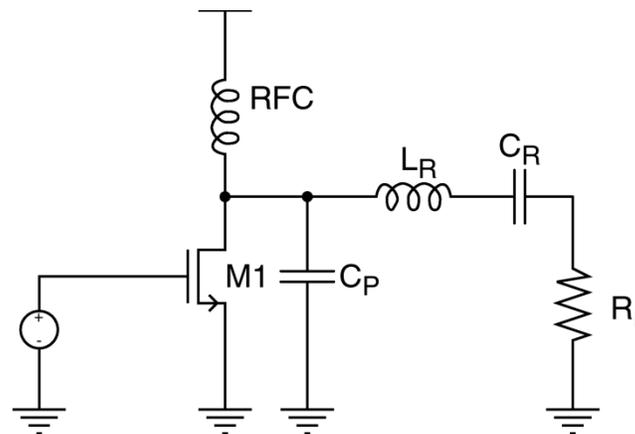


Figure 2.8: Class-E amplifier

The design of a class E power amplifier is characterized by the choice of conduction angle, supply voltage and peak current. The output power and peak voltage depends on the conduction angle. This means that they both rise with increasing conduction angle. For a reasonable output power the peak voltage is at least three times the supply voltage. This causes problems if the transistors used have relatively low breakdown voltage.

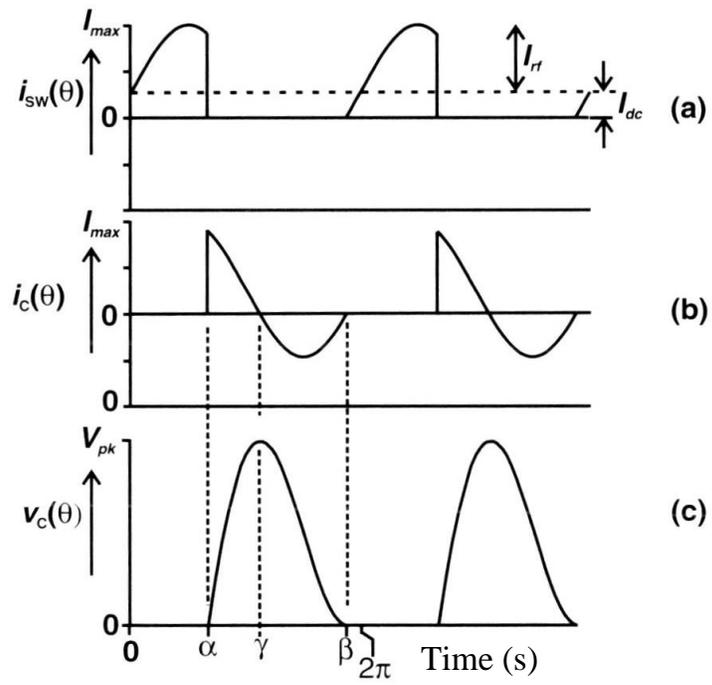


Figure 2.9 Drain and capacitor current and drain voltage of a class E PA

### 3. AMPLIFIER DESIGN PROCESS

#### 3.1 The Basics of Design

The design of power amplifiers has so far involved some amount of black magic performed by experienced RF designers. A large part of this work has focused on removing atleast some of the black magic in power amplifier design. During the design process a lot of choices will have to be made, if just one of the choices is wrong the whole project is in jeopardy. The following design method will try to formalize the decision process. A number of design methods have previously been published but have all focused on single stage power amplifiers [2].

The design process starts at the output stage of the power amplifier, since this stage will influence the rest of the power amplifier. The design will therefore start at the output load and work backwards through the power amplifier. The overall design flow is illustrated in Figure3.1.As can be seen from the figure the design flow is divided into three major parts. In Initial Design Decisions about differential or single-ended operation and the number of amplifying stages are made. In Stage Design the individual stages of the power amplifier are designed.

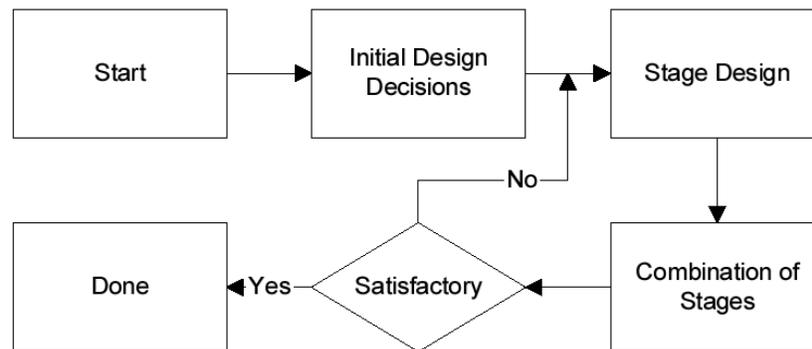


Figure 3.1: Flow chart for initial design concept

In Combination of Stages the designed stages are combined. After the combination of the individual stages the complete power amplifier is evaluated. If the result is not satisfactory the individual stages are redesigned.

## 3.2 Initial Design Decisions

Before the actual design of the power amplifier starts a number of initial decisions will have to be made. This includes the choice of the single-ended or differential operation, the number of stages and a budget for gain and efficiency. The design flow for the initial design decisions is shown in Figure.



Figure 3.2 : Design flow for initial design decisions.

### 3.2.1 Differential or Single-ended Operation

As discussed in Chapter 2 there are a number of benefits and drawbacks of differential operation of the power amplifier. The choice between single-ended and differential operation will always be a trade-off between a number of different factors. It is also possible to switch between differential and single-ended operation somewhere in the power amplifier chain.

### 3.2.2 Number of Stages

The next decision to make is to decide on the number of stages in the power amplifier. The number of stages is restricted by a number of requirements. The total gain necessary along with the maximum gain of a single stage sets the absolute minimum number of stages. The isolation obtainable in each stage and the total isolation needed also sets a lower limit. Power control is another example that may increase the minimum number of stages, but additional stages increase the cost and complexity of the power amplifier and it is therefore desirable to keep the number of stages low. Another upper limit is set by the total efficiency of the power amplifiers, since each extra stage will lower the total efficiency of the power amplifier.

### 3.2.3 Gain & Efficiency Budget

To be able to design the individual stages in the following steps, it is necessary to have information about the behavior of the individual stages. A budget is therefore made for key parameters like gain and efficiency of the stages.

### 3.3 Design of Individual Stages

After the initial design decisions have been made, the actual design of each stages in the power amplifier starts. The first stage to be designed is the output stage, since most of the characteristics of the power amplifier will be derived from this stage. The necessary output power from the preceding stage is also determined by the output stages. This means that it is most rational to work backwards through the chain and start with the output stage and stop with the input stage. In some application show ever it will be more convenient to start with the output stage then design the input stage and at last design the remaining stages.

The design flow for the design of the individual power amplifier stages is shown in Figure3.3. First of all the class of operation is selected, then the transistor is designed and at last the load and source impedance matching network are designed.

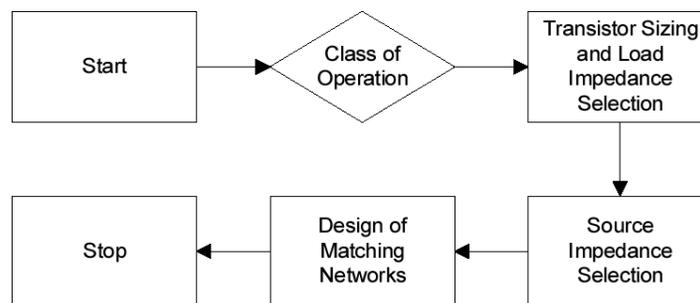


Figure 3.3: Design flow for individual stage design.

The choice of class of operation is the first decision to make in the design of the stage. The mode of operation influences almost all parameters of the power amplifier including linearity, gain and efficiency. The class of operation of each stage is a trade-off between a number of factors. The

factors include linearity, power gain, and efficiency. The individual stages of the power amplifier do not necessarily all operate in the same class.

### 3.3.1 Transistor Sizing and Load Impedance Selection

An initial guess of the transistor size originates from the I-V characteristic of the transistor. After an initial value is selected the more accurate RF behavior is found using load-pull simulations. The design flow for transistor sizing and load impedance selection is illustrated in Figure.

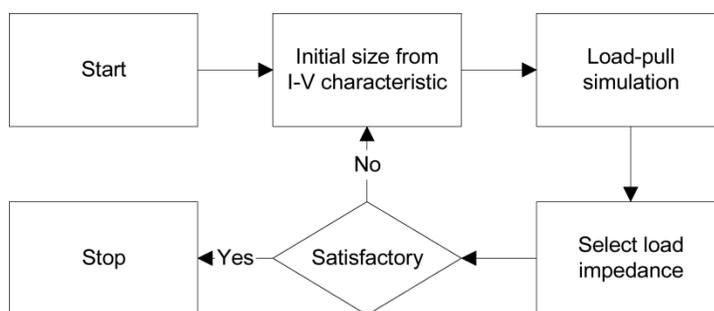


Figure 3.4 : Design flow for transistor sizing and load impedance selection.

The load-pull simulations are the simulation equivalent of the load-pull measurements. The load-pull simulation determines not only the transistor size but also the load impedance. In practice the load-pull simulation sweeps a range of impedance points and draws e.g. power, efficiency and linearity contours. This is done with either ideal load impedance or a matching network with the desired topology. If the matching network is chosen it will have to be synthesized at each impedance point, but the results resembles the actual performance more closely. The load impedance is then chosen as a trade-off between e.g. output power, efficiency and linearity. The load-pull simulations are described in more detail in Chapter 3. The impedances at harmonic frequencies are part of the definition of the mode of operation and is therefore defined by the selection of the class of operation.

### 3.3.2 Source Impedance Selection

The source impedance can be found using the small-signal impedance matching methods. Using one of the small-signal methods with the load impedance found in the previous step, single source impedance will be given. It is also possible to use a source-pull simulation in the same way as the load-pull simulation.

### 3.3.3 Design of Matching Networks

If the matching network topology was already chosen for the load-pull simulation it will only have to be synthesized. In the synthesis it is necessary to take all the important parasitics into account, this can be omitted in the initial load-pull simulations. Based on the choice of impedance at fundamental and harmonic frequencies the output matching network is designed [11].

When selecting the matching network topology the biasing of the stages is often an important part. Selecting the right topology will give DC blocking and biasing at the same time as the impedance matching. Depending on the mode of operation the optimal drive conditions for the output stage may differ. In the design of the input matching network biasing will also have to be incorporated, either as an integrated part of the matching network or explicitly, the latter will then have to be considered as a parasitic in the input matching network.

## 3.4 Combination of Stages

The final part of the power amplifier design is to combine the individual stages and the input matching networks will have to be merged with the output matching networks of the preceding stage. Then the stability of the complete power amplifier will have to be examined. This is done using transient simulations and small-signal stability analysis. The small-signal analysis uses all ports, DC or RF, as RF ports and the stability is then analyzed.

The design flow for the combination of the individual power amplifier stages is shown in Figure

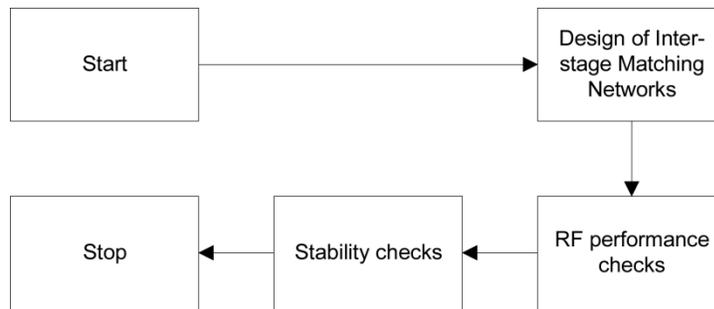


Figure 3.5: Design flow for combination of individual stages.

### 3.4.1 Design of Inter-stage Matching Networks

The design of the inter-stage matching networks will be based on the output matching network of the preceding stage and the input matching network of the following stage. It is often possible to reduce the number of passive components compared to the total number of components used in the two initial networks [10]. In integrated power amplifiers the passive components often dominate the die size as well as the losses in the power amplifier. It is therefore often desirable to minimize the number of passive components. The design of the inter-stage matching networks is an iterative process where the performance is verified continuously by a large-signal simulator

## 3.5 Harmonic filters

### 3.5.1 Types of filters

**Low pass filter (LPF):** Low pass filter allows passing low frequency signals though it but blocks high frequency signals. The transition happens at cut-off frequency.

**High pass filter (HPF):** This type of filter allows passing high frequency signals though it but blocks low frequency signals. The transition happens at cut-off frequency.

Band pass filter (BPF): This kind of filter allows passing specific band of frequency and rejects other frequencies. Band pass filters have two cut-off frequencies. One is lower cut-off frequency and other is higher cut-off frequency. Any frequency below lower cut-off frequency is blocked and any frequency above higher cutoff frequency is also blocked.

Band stop filter (BSF): Band stop filter performs exactly opposite of band pass filters. It blocks specific band of frequencies and allows rest of the bands.

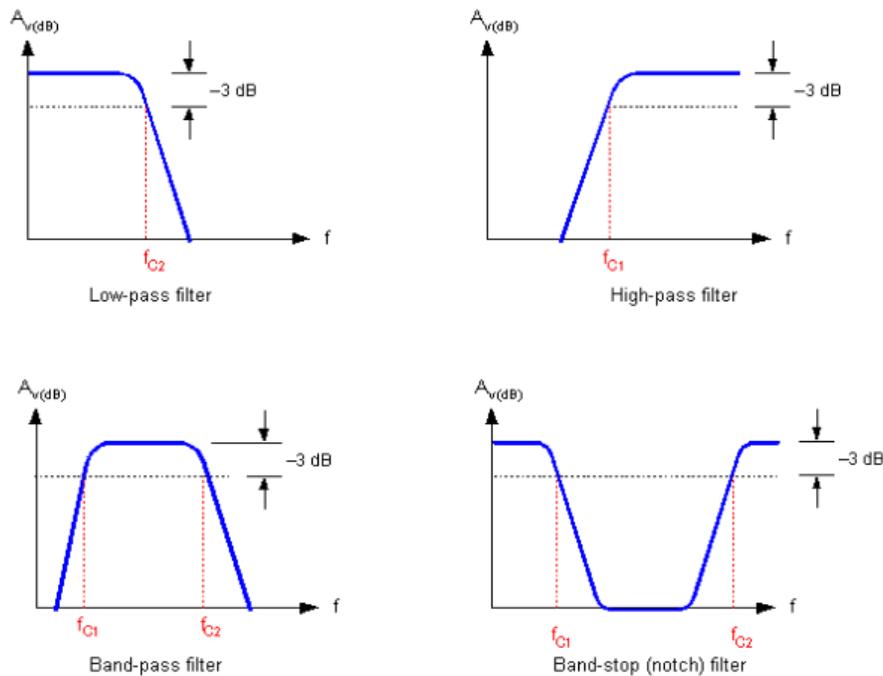


Figure 3.6: Frequency response of filters

Cut-off frequency of the filter is the frequency where gain of the filter is 3dB less than the maximum gain [12]. In the above figures, lower cut-off frequencies are defined by  $f_{c1}$  and higher cut-off frequencies by  $f_{c2}$ .

As we are developing 5MHz RF amplifier, main challenge will be reduction of higher order harmonics. Low pass Filter (LPF) can be a good solution for removing harmonics. So, we will discuss about low pass filter in details

First order low pass filter models: This type of low pass filter can be two types. Inductive and capacitive.

Inductive model of low pass filter:

When the frequency of the signal is low, the signal can pass through the filter. But, when the frequency increases, the impedance of the inductor also increases. As a result, the signal cannot pass through the filter [12].

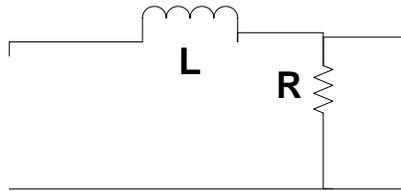


Figure 3.7: Inductive model of low pass filter

Capacitive model of a low pass filter:

When the frequency increases, the signal cannot pass through the filter, because the capacitor will pass all the signals and there will not enough voltage across load.

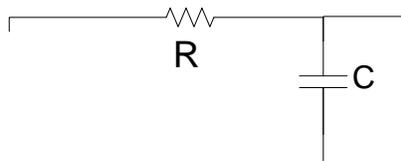


Figure 3.8: Capacitive low pass filter

## 4. AMPLIFIER SIMULATION AND IMPLEMENTATION

### 4.1 Power Amplifier Design

To start designing, it is necessary to determine the operating point of the MOSFET. It is necessary to simulate the complete power amplifier to verify the output power and efficiency. After simulation, the amplifier design needs to be converted to PCB layout design. Component selection is also important part of the implementation. After completing final design, pcb can be designed using PCB prototyping machine.

### 4.2 DC Biasing

At first, we do the DC biasing of the MOSFET and determine the operating point.

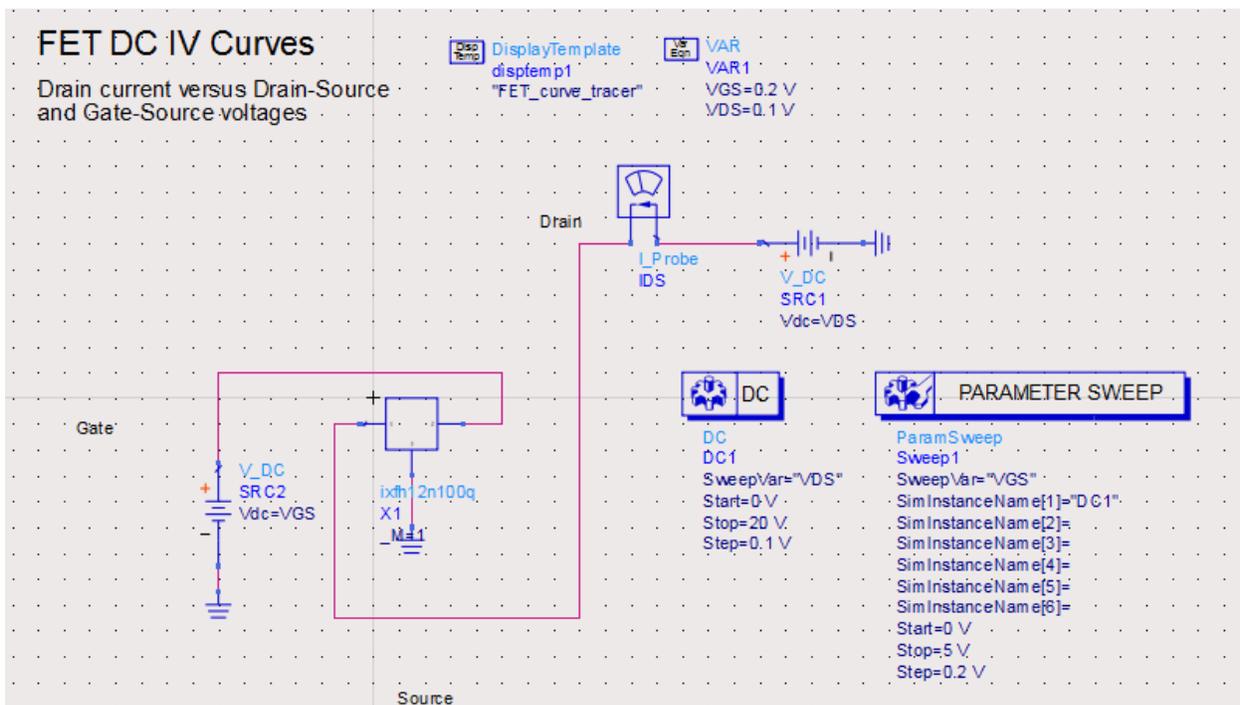


Figure 4.1: DC biasing of the MOSFET (IXFH12N100P)

We need to check the output and determine the operating point.

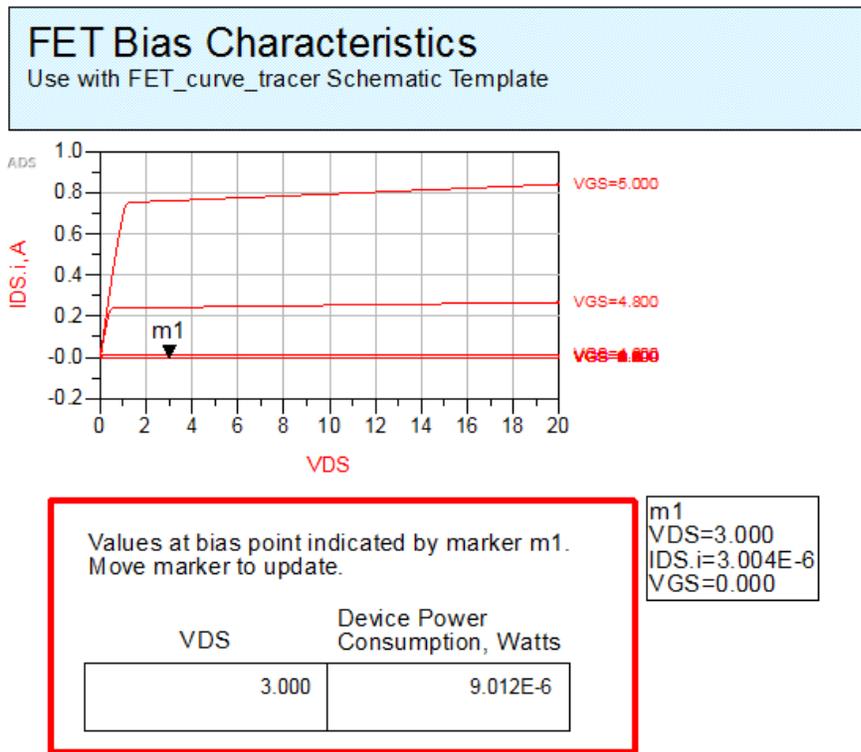


Figure 4.2: DC Biasing.  $V_{DS}$  vs  $I_{DS}$  curve

### 4.3 Amplifier Circuit Design

The design process described in the chapter 3 is followed and we have designed an amplifier circuit that can amplify 5MHz RF signal.

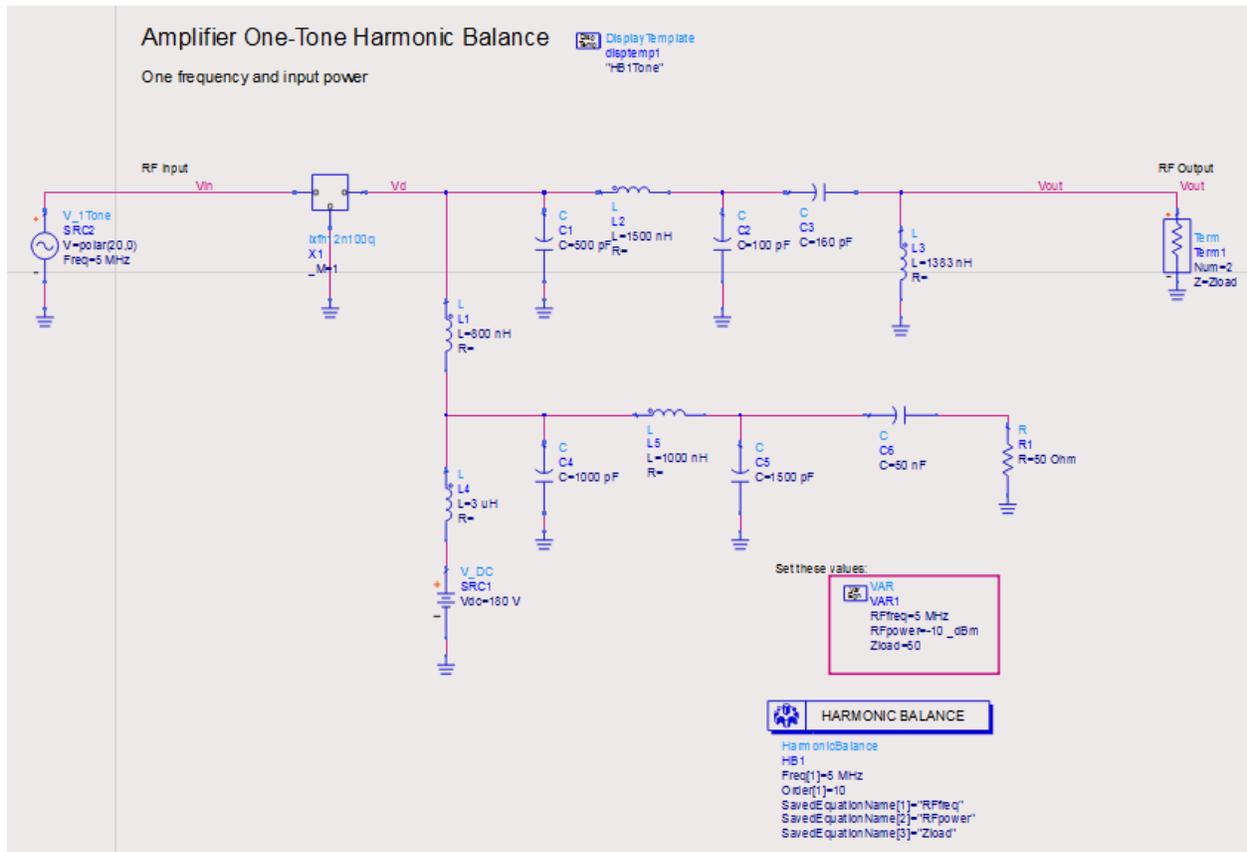


Figure 4.3: Amplifier circuit before fine tuning and removing harmonics

We have obtained following output from the circuit we designed above.

**Harmonic Balance One-Tone Test**  
Use with HB1 Tone Schematic Template

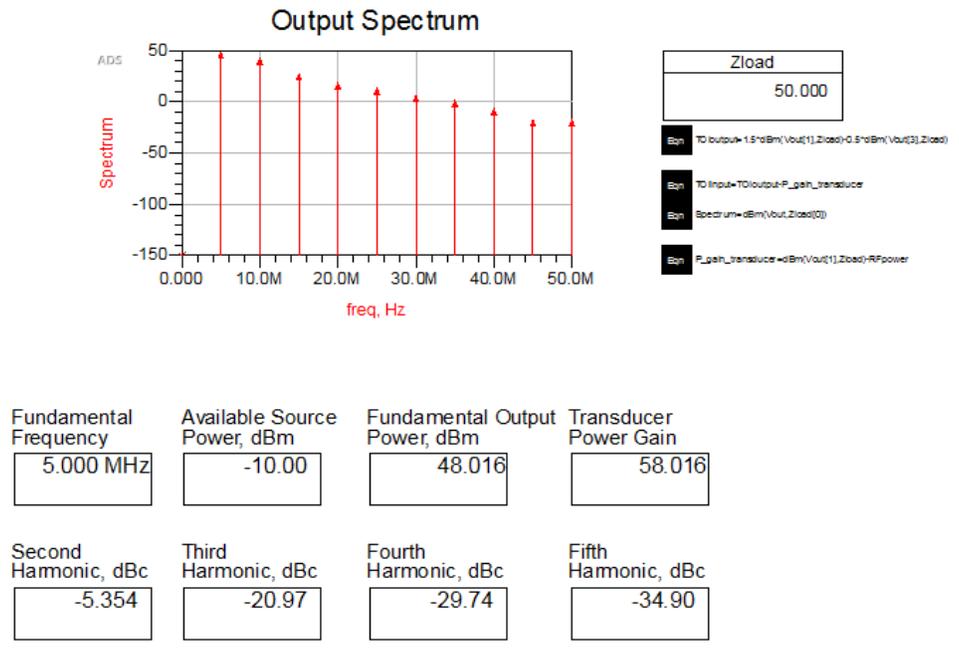


Figure 4.4: Output of the amplifier circuit before doing fine tuning

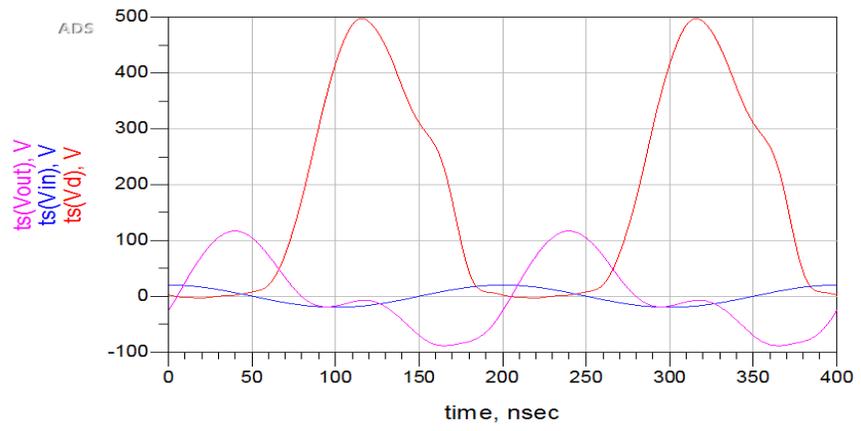


Figure 4.5: Voltage signals before fine tuning

If we look at the above figures, it is obvious that the amplifier will amplify RF input signals at 5MHz. But the amplifier has some limitations. There are lots of harmonics at other frequencies. The voltage wave shape has distortion, and it has to be solved.

### 4.4 Amplifier Fine Tuning and Harmonics Reduction

To solve the harmonics problem, several methods can be applied. One of the methods is applying filters at the output. We have searched several filtering methods and chose Chebyshev filter for steep cut off beyond the desired frequency.

Final circuit design after adding Chebyshev filter is shown below:

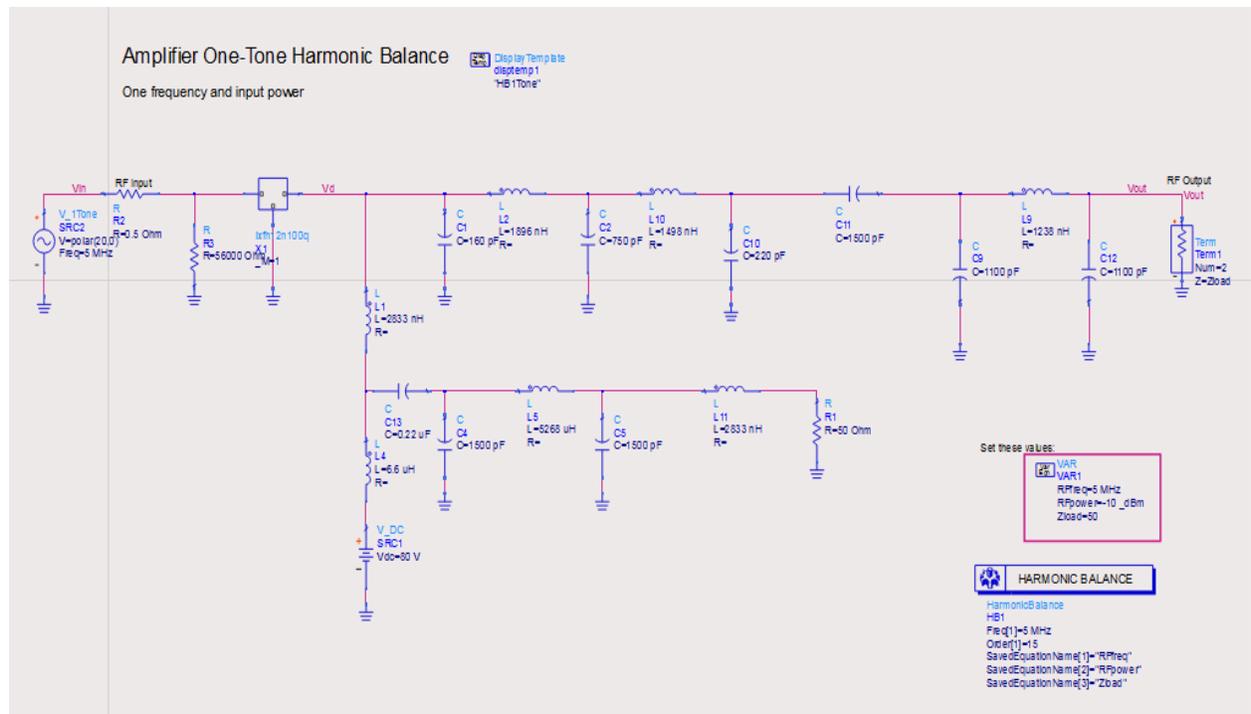
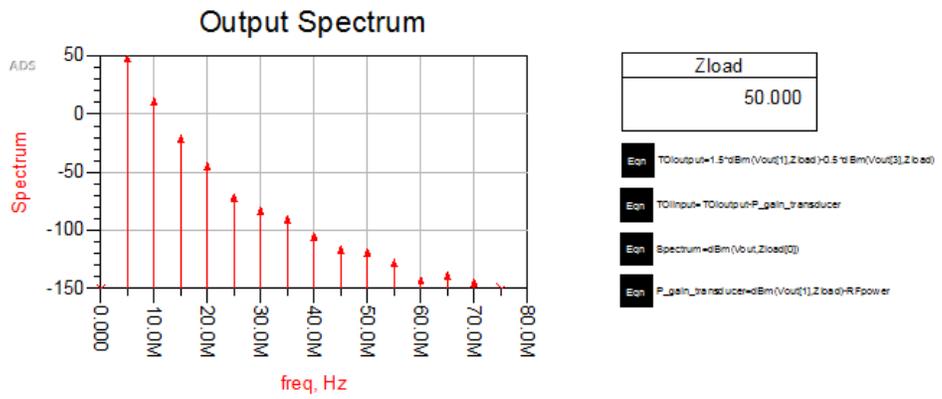


Figure 4.6: Amplifier circuit after fine tuning and applying harmonics filter

After analyzing the circuit in the Advanced Design System (ADS) simulation software, we have obtained following output:

## Harmonic Balance One-Tone Test

Use with HB1Tone Schematic Template



Fundamental Frequency	Available Source Power, dBm	Fundamental Output Power, dBm	Transducer Power Gain
5.000 MHz	-10.00	50.419	60.419
Second Harmonic, dBc	Third Harmonic, dBc	Fourth Harmonic, dBc	Fifth Harmonic, dBc
-37.23	-69.21	-92.66	-119.3

Figure 4.7: Output of the amplifier after fine tuning and reduction of harmonics

From the above output, it is clear that the harmonics are reduced significantly. From second harmonic to fifth harmonic, all are reduced and below -37dB. While the fundamental output power is still 50.419dB. At this point, the amplifier is amplifying at our desired 5MHz frequency and the harmonics are below considerable level.

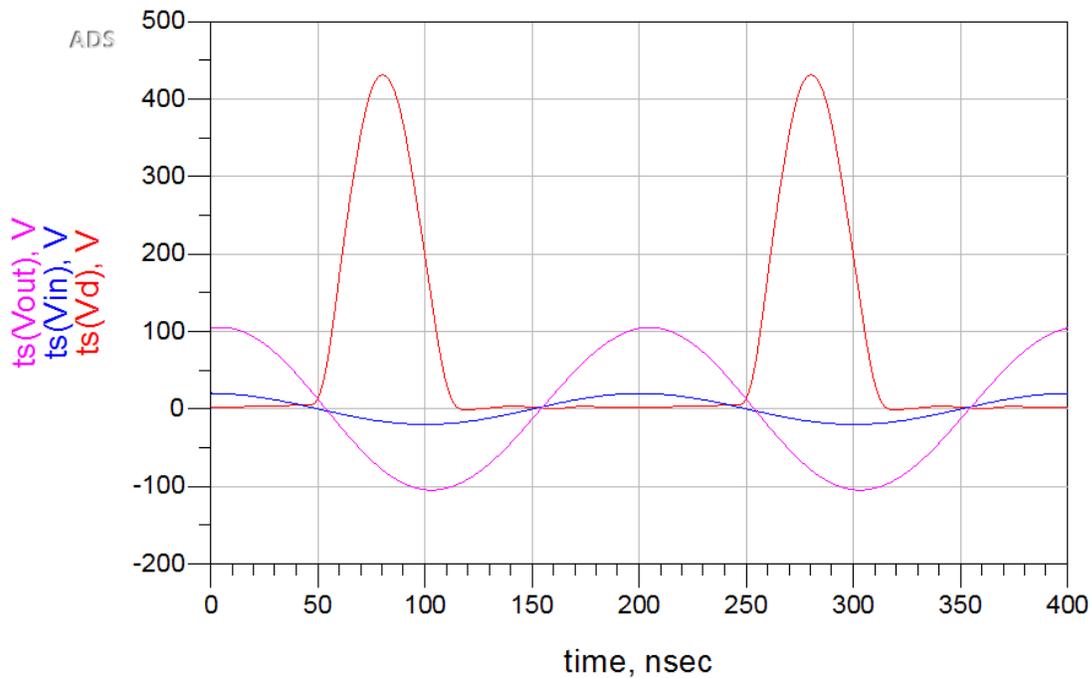


Figure 4.8: Voltage signals after harmonics reduction

After applying filter, the distortion in wave shape is no longer present.

#### 4.5 Implementation

To build the RF power amplifier, the first stage is component selection. We have selected and managed custom components for the design.

As the supply DC voltage is 80V, the components must sustain at high voltages. Conventional low voltage components are not eligible for this type of application. For choosing capacitors, main focus was high Q, high RF current and voltage, high RF power, Low ESR/ESL, ultra stable performance. The PPI 2225C series capacitors met the requirements.

## ESR vs Capacitance

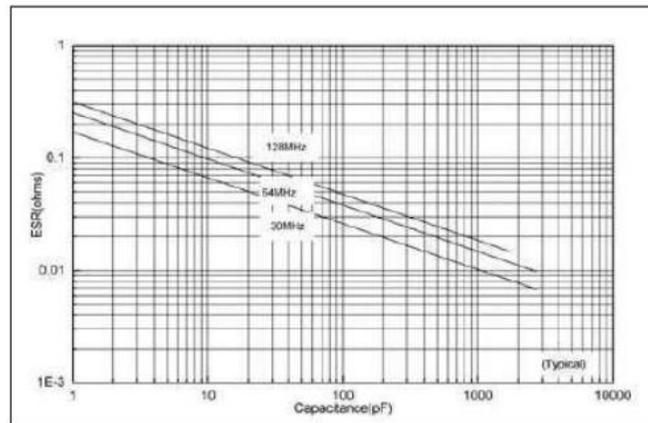


Figure 4.9: ESR vs Capacitance

## Q vs Capacitance

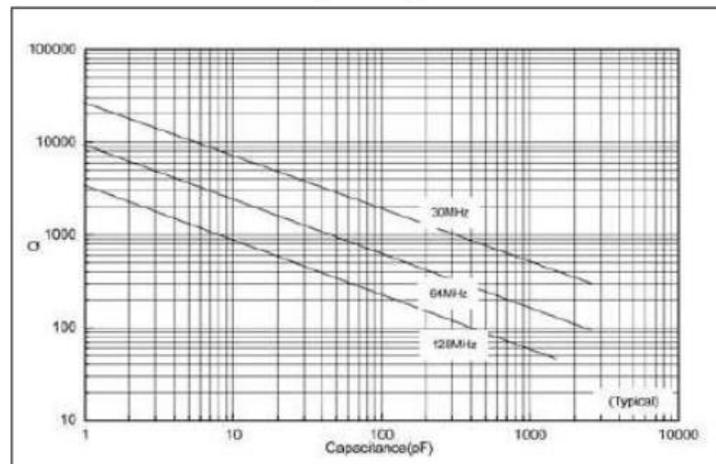


Figure 4.10: Q vs capacitance

### Current Rating vs Capacitance

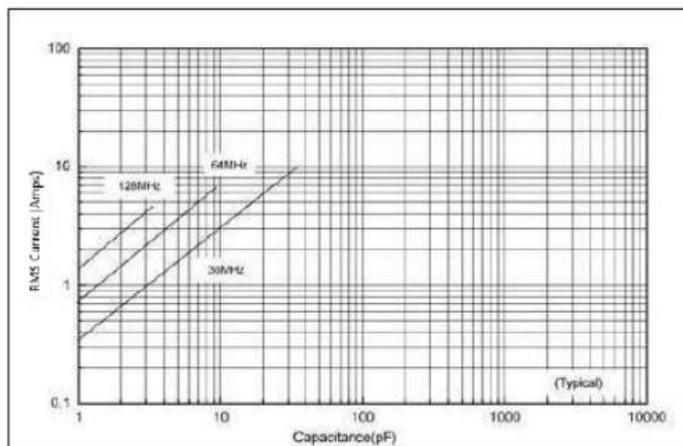


Figure 4.11: current rating vs capacitance

For the 50 Ohm resistors RFP-250-50RM are chosen due to their performance at desired frequency 5 MHz. At 5 MHz the components have nearly 50 Ohm value. The following curve is manufacturer provided performance curve.

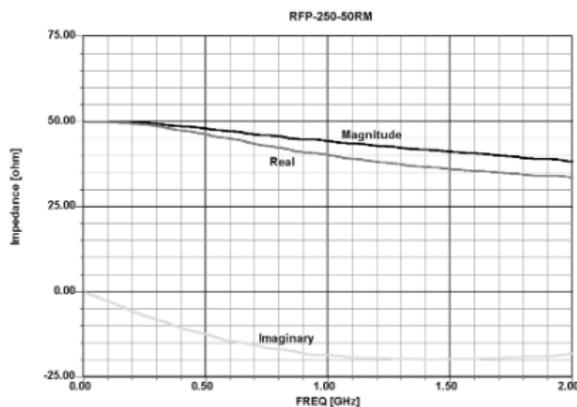


Figure 4.12: Impedance vs Frequency

The chosen MOSFET is IXFH12N100P. The MOSFET can sustain up to 1000V. It's TO-247 package. It has option to add heat sink for heat dissipation. Source-Drain current can be as high as 12A.

For inductors, it is really difficult to get exactly same size inductor. For this proto type custom made inductors are used. Mainly, two types of toroidal inductor cores are used and different numbers of turns are used to build the inductors with required inductance. Two types of toroidal cores are used (T106-6 and T130-6).

Next challenge is to design PCB with minimizing RF Desense. Electromagnetic interference can reduce the performance of the amplifier. Parasitic value can significantly affect the efficiency of the amplifier at desired frequency. In the PCB design process, BNC connectors are chosen for input and output signals.

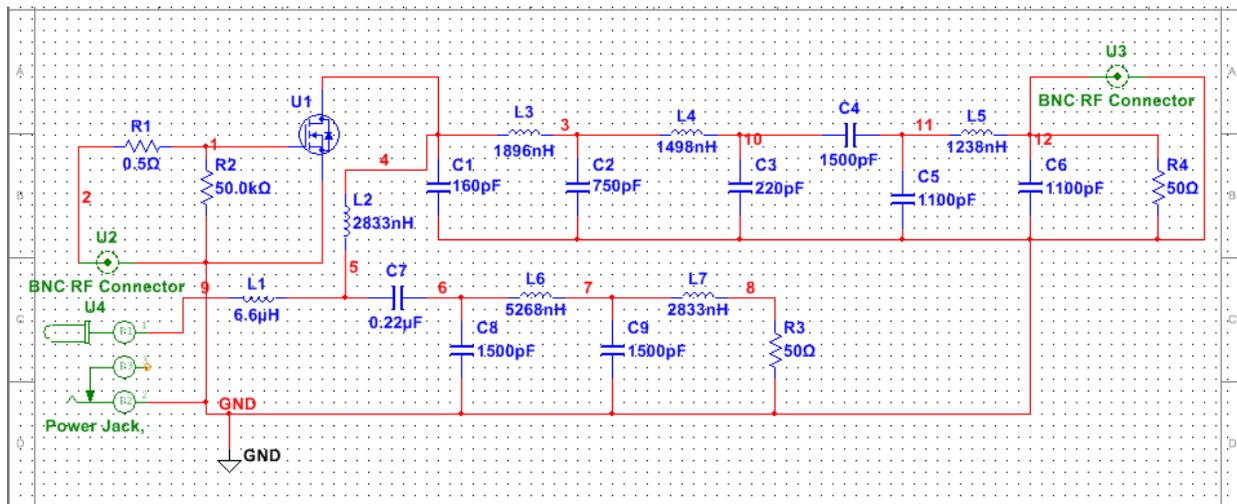


Figure 4.13: Amplifier circuit design for PCB implementation

We have followed some strategy to avoid potential EMI sources. First, concept is to extend the ground. The PCB layout has bigger ground plane. The following figure is PCB top layer. The green color is connected to the ground.

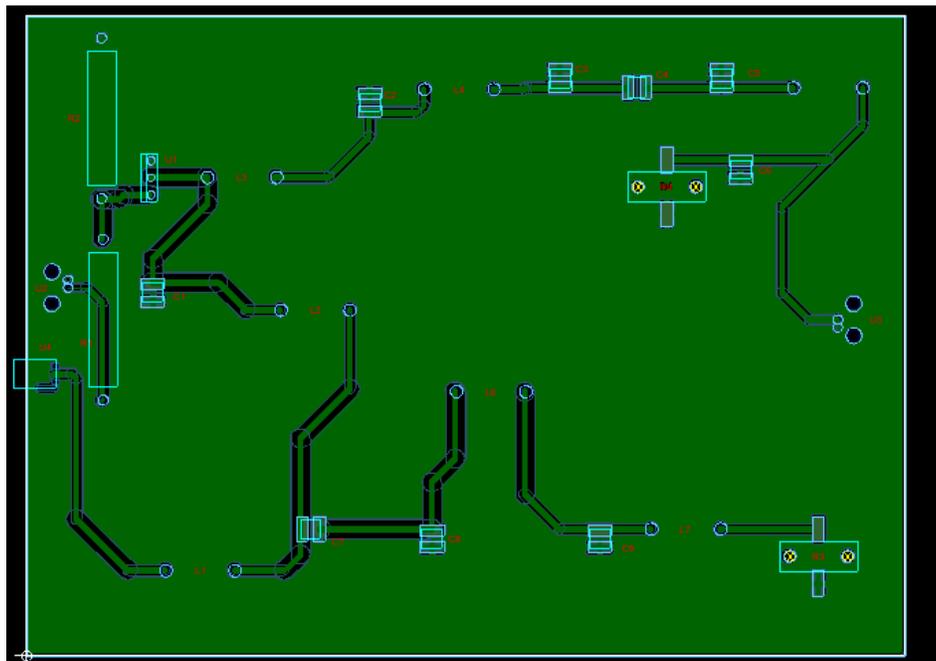


Figure 4.14: Copper top layer of PCB.

In the above figure, the whole areas except the traces are connected to the ground. This type of design will help to minimize the electromagnetic interference significantly.

The following figure is the view of PCB bottom part. The whole area is connected to the ground except the punch and holes.

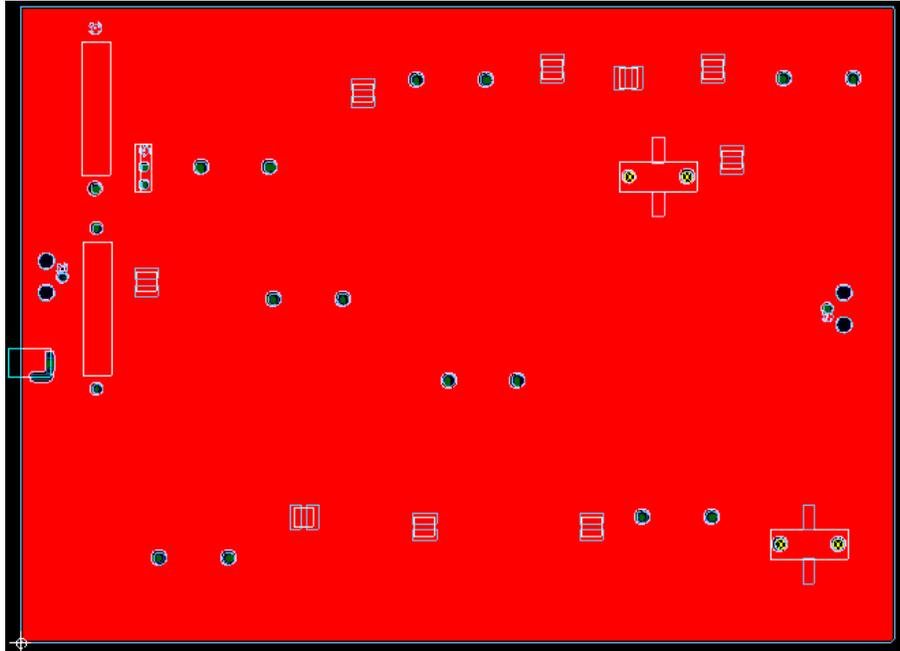


Figure 4.15: Copper bottom layer of PCB.

The components are placed in the following way. The left side BNC connector will receive

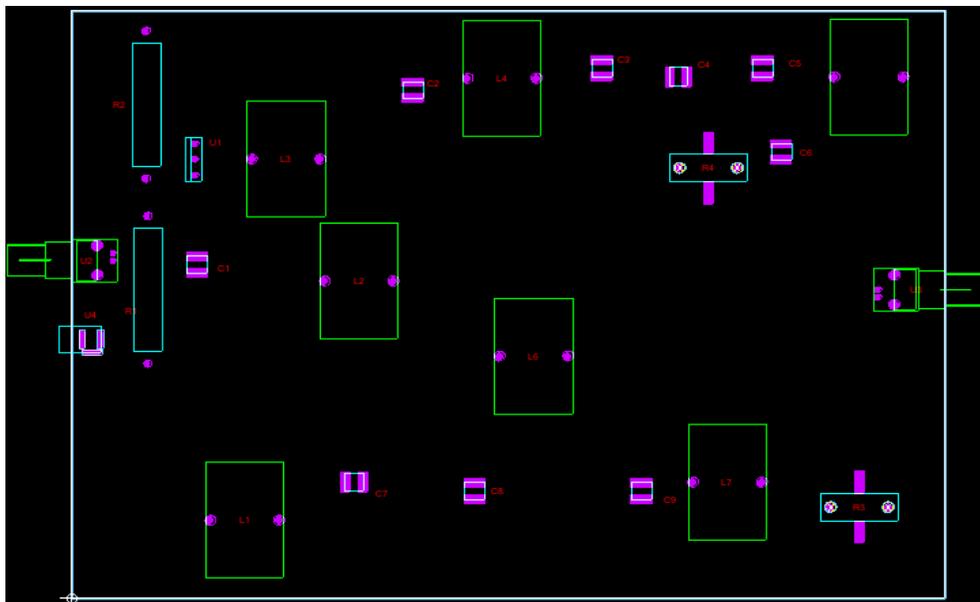


Figure 4.16: Component placement on the PCB.

RF signal from the source and the right side BNC connector will give amplifier output of the signal. The transistor is placed near the input signal as the signal contains low power and it will need to travel less distance before it gets amplified.

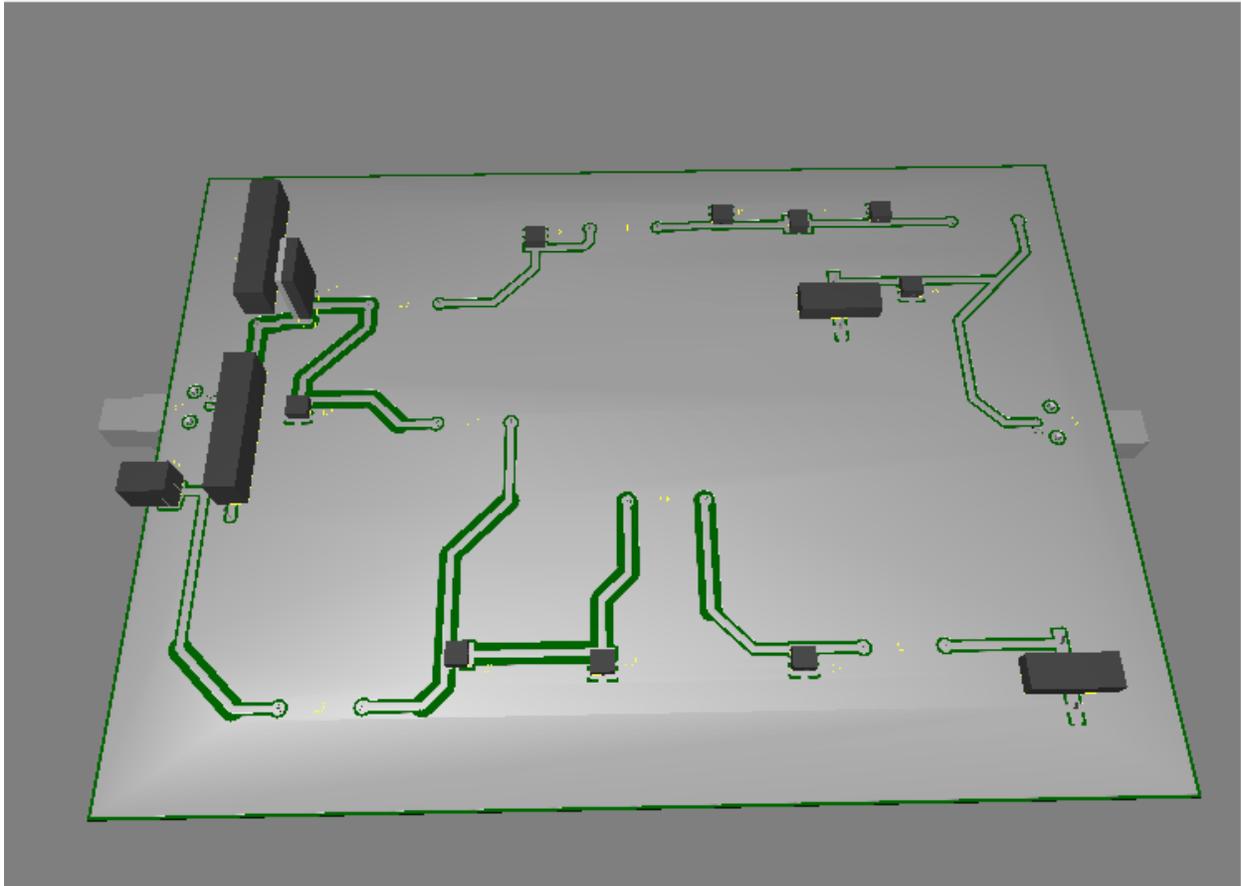


Figure 4.17: 3D view of the final PCB layout simulation

The above figure is the final PCB layout design 3D view. Based on the above design, gerber files were generated for pcb machine. As the voltage rating is higher, 1.6mm thickness PCB was used. The pcb is double sided, copper claded and non perforated with 1OZ copper layer on the both surfaces. The board material is FR4. (Model: MG chemicals 555 copper claded board).

Finally we built the circuit based on the design and final circuit is shown below:

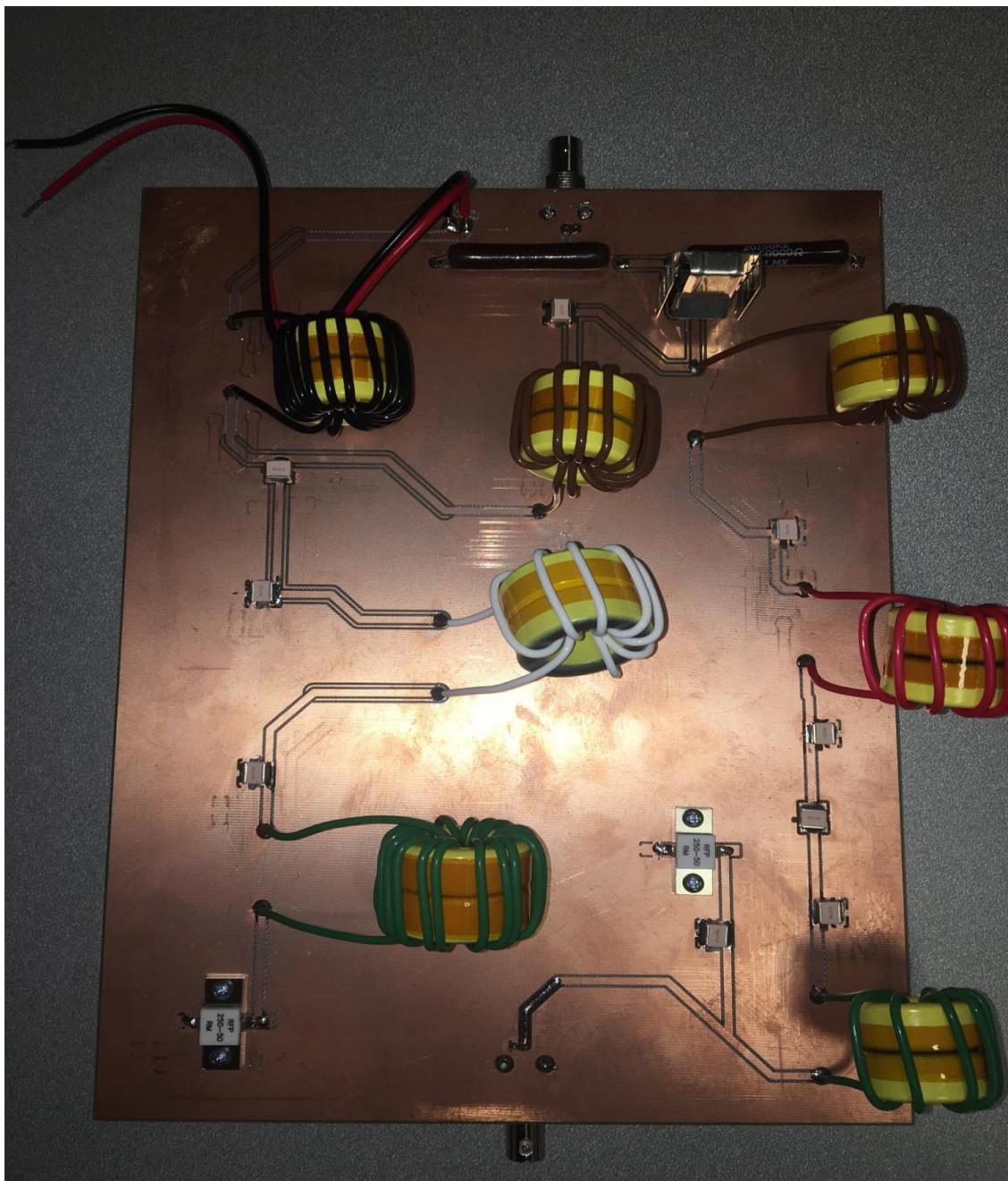


Figure 4.18: RF Power Amplifier-5MHz

## REFERENCES

- [1] Design Of A High Efficiency Power amplifier By Using Doherty Configuration. Retrieved from <https://pdfs.semanticscholar.org/4c71/e619b849a89946a583075a4ec02e81185eb5.pdf>
- [2] RF Power Amplifier Efficiency Enhancement, Retrieved from Delft University of Technology.
- [3] C.Fallesen,G.Hanington,andP.M.Asbeck,"Improvedlinearityofadynamic supply voltage power amplifier using digital predistortion," in *1999IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, (San Diego, USA), September1999.
- [4]C.Fallesen and P.Asbeck,"A highly integrated1WCMOS power amplifier for GSM 1800," in *2000IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, (San Diego, USA), September2000.
- [5] C. Fallesen and P.Asbeck,"A highly integrated 1WCMOS power amplifier for GSM-1800 with 45% PAE," in *18th NorChip Conference*, (Turku, Finland), November2000.
- [6] C. Fallesen and P. Asbeck, "A 1 W 0.35 um CMOS power amplifier for GSM- 1800 with 45% PAE," in *2001 IEEE International Solid-State Circuits Conference*, (San Francisco, USA), February2001.
- [7] C.FallesenandP.Asbeck,"A1WCMOSpoweramplifierforGSM-1800with 55% PAE," in *2001 IEEE International Microwave Symposium*, May2001.
- [8] M. Ranjan, K. H. Koo, G. Hanington, C. Fallesen, and P. Asbeck, "Microwave power amplifiers with digitally-controlled power supply voltage for high efficiency and high linearity," in *2000 IEEE MTT-S International Microwave Symposium*, (Boston, USA), June2000.

- [9] P.Asbeck and C. Fallesen,"A RF power amplifier in a digital CMOS process," in *18th NorChip Conference*, (Turku, Finland), November2000.
- [10] Abdullah Eroglu, "Introduction to RF power amplifier Design and Simulation" from <https://www.amazon.com/Introduction-Power-Amplifier-Design-Simulation/dp/1482231646>
- [11] C. Yoo and Q. Huang, "A common-gate switched, 0.9W class-E power amplifier with 41% PAE in 0.2 um CMOS," in *2000 Symposium on VLSI Circuits*, pp. 56--57,2000.
- [12] K.-C. Tsai and P. R. Gray, "A 1.9 GHz 1-W CMOS class-E power amplifier for wireless communications," *IEEE Journal of Solid-State Circuits*, July1999.