ELECTRICAL CHARACTERIZATION OF EMERGING ELECTRONIC DEVICES IN LOW AND HIGH POWER APPLICATIONS

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To my supportive Parents,
my life partner and lovely wife,
and to my kids

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SYMBOLS

m	mass
v	velocity
f	frequency
k	Boltzmann constant
q	elementary charge
T	temperature
Q	total charge
A	area
V_{DD}	supply voltage
V_{GS}	gate to source voltage
V_{DS}	drain to source voltage
V_S	source voltage
V_D	drain voltage
V_G	gate voltage
V_T, V_{th}	threshold voltage
t	time
C_L	load capacitance
C_{ox}	oxide capacitance
C_D	depletion capacitance
C_S	surface capacitance
C_{GB}	gate to top barrier capacitance
C_{SB}	source to top barrier capacitance
C_{DB}	drain to top barrier capacitance
ϵ_{ox}	oxide permitivity

I_{ON}	on current
I_{OFF}	off current
I_{DS}	drain to source current
I_D	drain current
I_S	source current
μ	mobility
W	channel width
W_{ch}	channel width
t_{ch}	channel thickness
t_{ox}	Oxide thickness
L, L_{ch}	channel length
W, W_{ch}	channel width
P	power
P_{ON}	power dissipated at ON-state
P_{OFF}	power dissipated at OFF-state
N_T	number of transistors per unit area
N	number of carriers
N_D	doping concentration
V_T	threshold voltage
E_G	Bandgap
D_{it}	Interface trap density
I_{cp}	charge pumping current
$I_{cp,RIASE}$	charge pumping current due to rising edge of a pulse
$I_{cp,FALL}$	charge pumping current due to falling edge of a pulse
t_{RISE}	voltage pulse rise time
t_{FALL}	voltage pulse fall time
Q_{it}	Interface trap charge quantity
C_{it}	Interface trap capacitance
E_F	fermi level

E_T	trap energy level
E_C	conduction band energy level
E_V	valence band energy level
g_m	transconductance
R_{SD}	S/D series resistance
R_S	source series resistance
R_D	drain series resistance
R_C	contact resistance
R_{sh}	sheet resistance
Φ_S	surface potential
τ_c	capture time constant
τ_e	emission time constant
S_{ID}	power spectral density of drain current I_D
P_r	remnant polarization
$D_{it}(E)$	Donor-like interface trap states
$D_{it}(E)$	acceptor-like interface trap states

ABBREVIATIONS

FET	field-effect transistor
MOS	metal-oxide-semiconductor
MIM	metal-insulator-metal
MOSCAP	metal-oxide-semiconductor capacitor
MOSFET	metal-oxide-semiconductor field-effect transistor
HEMT	high electron mobility transistor
MOS-HEMT	metal-oxide-semiconductor High Electron Mobility transistor
CMOS	complementary metal-oxide-semiconductor
IoT	Internet of things
RF	radio frequency
GND	ground
SOI	silicon on insulator
UTB	ultra thin body
2D	2-dimensional
3D	3-dimensional
SCE	short channel effects
CNL	charge neutral level
EOT	equivalent oxide thickness
GAA	gate all around
GOOI	β-Ga_2O_3 on-insulator FET
TFET	tunneling field-effect transistor
FinFET	Fin field-effect transistors
NC-FET	negative-capacitance FET
FeFET	Ferroelectric FET

MEMS	microelectromechanical system
I-V	current-voltage
SS	subthreshold slope
C-V	capacitance-voltage
G-V	conductance-voltage
TMA	Trimethyl Aluminum
S/D	source and drain
n+	highly n-doped
p+	highly p-doped
ALD	atomic layer deposition
RTA	rapid thermal annealing
AFM	atomic force microscopy
RMS	root mean square
RBS	Rutherford back scattering
HRXRD	High-resolution X-ray diffraction
DIBL	drain induced barrier lowering
TEM	transmission electron microscope
LFN	low frequency noise
RTN	random telegraph noise
PSD	power spectral density
BTI	bias temperature instability
HCI	hot carrier injection
HZO	hafnium zirconium oxide
FE	Ferroelectric Dielectric
DE	Linear Dielectric
WGFMU	waveform generator/fast measurements unit
RSU	remote-sense and switch unit

ABSTRACT

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Si-based technologies and semiconductor industries are reaching an inevitable scaling and power dissipation constrains. On top to that, fast growing demands for applications such as Internet of things (IoT) is calling for low power and low cost devices, while other applications as for RF, 5G, and Electrical Automotive applications is calling for extremely power efficient, high quality, and high speed devices. Researchers over the recent years have been exploring an alternative channels in order to help Moors law survive. Areas of research involve: competitive materials, such as high-mobility III-V semiconductors, 2-dimensional (2D) materials, and Germanium (Ge), in addition to a novel device structures, as metal-oxide-semiconductor (MOS) high-electron-mobility transistors (HEMT) (or MOS-HEMT), fin field-effect transistors (FinFETs), negative capacitance field-effect transistors (NC-FETs), and ferroelectric field-effect transistors (FeFETs). However, as important as realizing these alternatives, it is equally important to accurately characterize electrical performances, reliability, and variability of these state-of-the-art ultra-scaled devices. In this thesis, an interface passivation by a lattice matched atomic layer deposition (ALD) epitaxial magnesium calcium oxide (MgCaO) on wide-bandgap gallium nitride (GaN) has been applied for the first time and expensively studied via various characterization methods (including AC conductance methods, pulsed current-voltage, and single pulse charge pumping). Also, β-Ga_2O_3 with a monoclinic crystal structure that offers several surface oriented channels has been demonstrated as potential β-Ga_2O_3 FET. Among those surfaces, commercially available (-201) and (010), in which have been studied

and compared from the interface quality point of view through another set of electrical characterization methods (such as frequency dependent, photo-assisted capacitance-voltage (C-V), and ultraviolet light-Based currentvoltage measurements). This thesis also provides guidance for future high speed, high power devices development.

On the other hand, low frequency noise studies in 2-D MoS_2 NC-FETs was reported for the first time. Low frequency noise of the devices is systematically studied depending on various interfacial oxides, different thicknesses of interfacial oxide, and ferroelectric hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O$ or HZO). Interestingly enough, the low frequency noise is found to decrease with thicker ferroelectric HZO in the sub-threshold regime of the MoS_2 NC-FETs, in stark contrast to the conventional high-k transistors. This result can be interpreted as electrostatic improvement induced by the negative capacitance effect. And to gain further insights about ferroelectric dielectric, time response of polarization reversal in Germanium nanowire (NW) Fe-FETs with HZO as ferroelectric insulator have been analyzed by fast dual gate voltage sweep, where it is found that the time response of polarization reversal leads to a voltage hysteresis and maximum drain current time-dependency in Ge NW Fe-FETs. Also, the ferroelectric switching speed is found to be related with the maximum electric field applied during the fast gate voltage sweep, suggesting the internal ferroelectric switching speed can be even faster depending on the devices electrical bias conditions and promises a high speed performance in our ferroelectric HZO. In addition, reliability issues related to ferroelectric HZO when accompanied by another layer of conventional high-k oxide, including switching mechanism and endurance performance, were primarily studied and revealed a significant degradation in the polarization retention, which is an essential part in the longevity of access memory devices made of ferroelectric HZO.

1. INTRODUCTION

This chapter gives an introductory summary to motivation behind what is known as beyond-CMOS devices research. Focused on characterization and reliability of these modern semiconductors devices as an experimental measure to their performance, the thesis is outlined thereafter.

1.1 Beyond Moore's Law: It Is All About Power

For decades, Moore's law has been the driving force towards smaller transistors and higher integration capabilities of transistors in a single electronic chip. 1.5 - 2 years was the time period that Moore predicted for every technology node to double the density of transistors per unit area. The semiconducting silicon chip revolutionized the electronic industry and gave birth to the digital life of the 21^{st} century through complementary metal oxide semiconductors (CMOS) technology. After more than 50 years now, and despite the noticeable slowdown in chip scaling amid an increase in the fabrication costs and variable consumers' demands, the research for high speed and low power devices have been consistently the focus for process engineers and researchers, because with higher operating speed and larger integration density, the power dissipation is becoming one of the main challenges resulting from that aggressive scaling, and overcoming this challenge requires seeking alternatives in both: materials of the transistor's channel and the fundamental structure.

The power dissipation is described as follows:

$$P = P_{ON} + P_{OFF} \tag{1.1}$$

$$P_{ON} = NfCV_{DD}^2 \tag{1.2}$$

$$P_{OFF} = NI_{subthreshold}V_{DD} \tag{1.3}$$

Table 1.1.
Electrical properties some semiconductor material

Property	**Si**	**Ge**	**GaAs**	**GaN**	**InAs**
$E_g(eV)$	1.12	0.66	1.42	3.39	0.36
μ_n $(cm^2/V.s)$	1,500	1,900	8,500	1,200	40,000
μ_p $(cm^2/V.s)$	450	3,900	400	200	500
$n_i(cm^{-3})$	1x10^{10}	2x10^{13}	2.1x10^{6}	1x10^{10}	1x10^{15}

Where P_{ON} is the power dissipated at on-state of the device and P_{OFF} is the power dissipated when the device is off. f is the operating frequency, C is the gate capacitance, V_{DD} is the voltage supply, and N is the number of transistors. From eq. 1.2, P_{ON} is proportional to V_{DD}, hence, lowering the supply voltage could potentially lower the power dissipation, however, this would also lower the driving current in the channel of the transistor, which will lower the performance. in order to compensate the reduction in the drive current, a higher mobility channel material, when used, would increase the injection velocity, according to eq. 1.4 below, and that is due to the higher mobility μ of the carrier along the channel, therefore, a higher mobility channel is advantageous in this case when the total charge Q_s is kept the same and even with low electric field ξ

$$I_D = Q_s v_{injection} = Q_s \xi \mu \tag{1.4}$$

Table 1.1 shows some essential electrical properties of Si, Ge, and other III-V semiconductors. Except for GaN, which has a different applications other than CMOS logic applications, all the other material have electron mobilities higher than Si, which is why these (and other III-V semiconductors) were recently studied and developed intensively to replace silicon.

Referring to eq. 1.1 and eq. 1.3, another way to lower the power dissipation is to lower the dissipation due to the leakage current (or subthreshold current $I_{subthreshold}$)

at off-state, and this could be achieved by lowering the subthreshold slope SS of the transistor's transfer curve I-V. This particular topic has attracted lots of attention lately. Lowering SS enabled by various techniques such as the use of advanced 3-dimensional structure around the channel for better electrostatic control of the gate, ultra-thin-body devices (UTB) on insulators, or steep-slope transistors, where the later has a superiority over both of the formers, and that is because steep-slope transistors by definition are transistors with SS less than the thermonic limit of $\sim$ 60 mV/dec.

1.2 High Mobility Channel Materials and Compound Semiconductors

III-V materials is believed to be the best solution to today's devices hurdles, however, those high mobility semiconductors candidates, such as: GaAs, InSb, InGaAs, etc ..., others like, Germanium or 2-dimensional semiconductors, such as: Transitional Metal Dichalcogenide or TMD (MoS_2, BP, BN), or Nanowires have proven lack of cost effectiveness and reliability in general. The imperfection of the channel to insulator interface was suggested to be one of the main issues that need to be addressed in today's under-research electronics in order for these candidates to strive. The advantages of Silicon over all of the other semiconductors are: the native oxide SiO_2 that is formed naturally over the silicon channel, which enables a very low trap density (D_{it}) in the interface between the oxide and the Si channel, the reasonable values of hole and electron mobilities, and the suitable bandgap (E_G) of about 1.1 eV. In order to get a better material to replace silicon, these three advantages have to be considered. First a material that has higher hole mobility and higher electron mobility must be chosen. Many research groups have reported on the use of GaAs or InGaAs as the potential channel materials for transistors utilized in logic circuits, thanks to the high electron mobility of these material and the relatively suitable bandgap. However, the lack of homogenous oxide for these material results in higher than the silicon D_{it} in the oxide/semiconductor which in return would result in what

it is called fermi level (E_F) pinning. Fermi level pinning is the case where the (E_F) is pinned within the bandgap of the semiconductor at the interface, and it becomes difficult to move with the application of external electric field (E_F) to allow for higher carrier transport, thus higher current. The main reason for this phenomena is the high U-shaped (D_{it}) of the III-V semiconductors which does not allow (E_F) to move far from the charge neutral level (CNL). Refer Fig. 1.1 to find CNL for some selected

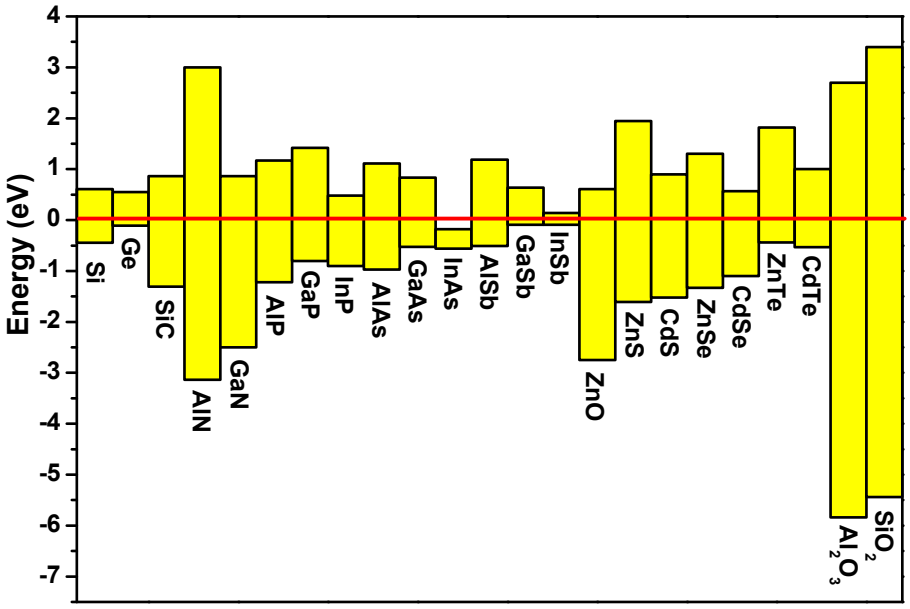

Fig. 1.1. Charge neutral level alignments for selected semiconductor materials

III-V semicondutres. The closer the CNL to the band edge (conduction/valence) the easier for the respected carrier (electrons/holes) to accumulate near the interface and contribute to the transport. Using a down scaled III-V semiconductors also requires scaling the effective oxide thickness of the gate stack between channel and gate electrode. Our group have worked extensively in growing oxides with high dielectric constant (known as High-k materials) as an alternative to SiO_2 for MOSFETs with

III-V channel using Atomic Layer Deposition (ALD). Growing thin film insulator atomic layer by atomic layer on the channel surface proved to improve the quality of the oxide/semiconductors interface and lower D_{it}.

A proper characterization techniques are then required to study the interface quality and its effect on both on-state and off-state performances, some of these techniques, such as, Conductance method, UV-Assisted Capacitance-Voltage measurements (UV-CV), and Low Frequency Noise (LFN) are discussed in details and implemented in this thesis.

1.2.1 Germanium (Ge) and 2-D van der waals Materials

Germanium

Ge was used in the very early stages of the revolution of electronics, the very first transistor in fact was made of Ge and two gold contacts, see Fig. 1.2

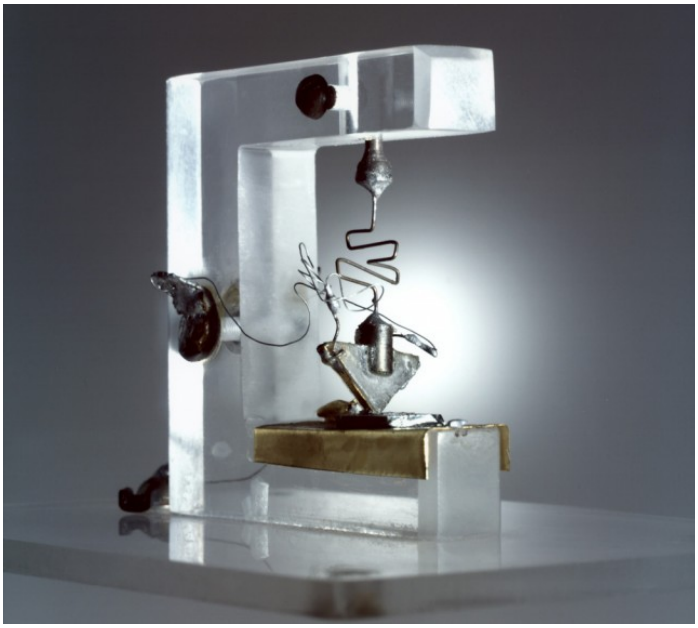

Fig. 1.2. The first Transistor made of Ge [1]

Implementation of two material systems, namely, III-V and Ge, has been studied very widely in CMOS applications in the recent years, and that is for its high electron mobility and for its high electron mobility, respectively, Thus, Ge is considered a very suitable semiconductor for p-type MOSFETs (p-MOSFET). It has a hole mobility over 3900 cm^2/V.s which is the highest amongst all the material in Table 1.1. However, fabricating CMOS circuits with two different material systems is cost effective from mass production point of view, complexity of manufacturing, and performance reliability. Our group have developed the first experimental Ge CMOS circuit where both n-MOSFET and p-MOSFET devices are made of Ge only [2]. Ge and Si are both located at the same column in the periodic table, namely, group IV, which makes them similar in term of physical and chemical properties. Ge however, has a smaller effective mass (m_t) for electrons and holes, which what have given it the advantage over Si for higher carrier mobilities, and ultimately higher current. Furthermore, Ge was incorporated with Si in what was known as SiGe strain techniques in order to increase the doping concentration in the source and drain areas in p-type Si channel. SiGe process was first introduced back in 2004 (90 nm node, see Fig. 1.3), that is more than 14 years ago, and it has been produced ever since by several manufacturers, such as AMD and TSMC. This along with a well-controlled oxide deposition as a gate

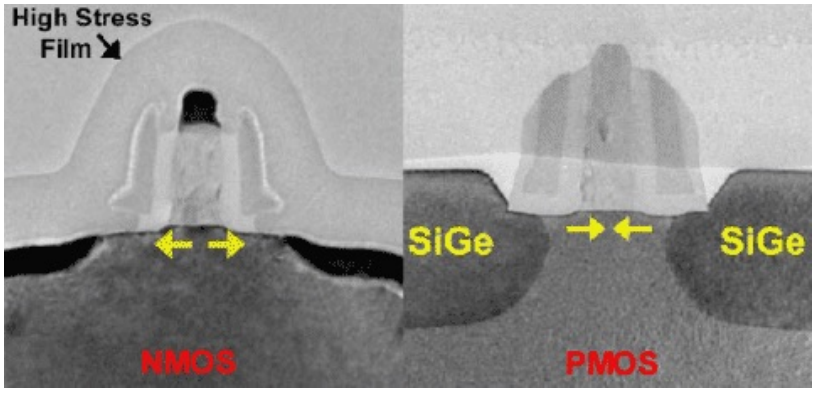

Fig. 1.3. Strain introduction in CMOS for mobility enhancement [3]

insulator for high interface quality, and multi-gate structures, have opened the door

for switching the channels and was enough motivation for the use of Ge as a channel material. Ge also has a processing compatibility that is adaptable to the standard Si-CMOS technology but was quite challenging that could be easily overcome with the advanced fabrication technologies. But nothing is completely perfect, Ge also suffers some drawbacks when it comes Fermi level pinning and D_{it} reported, which is at least one order of magnitude higher than that of Si/SiO_2. Also, the large Schottky barrier that is relatively high for electrons between the Ge and the metal contacts increases the resistivity of those contacts in Ge n-MOSFETs. Short channel effect is still a major issue for all downscaled device, and Ge is not an exception. Many of these issues were addressed in recent work done by Heng Wu et. al. [2, 4, 5]. In the following sections we will see how this Ge devices was included in the next generation devices such as FinFET, Gate All Around FET (GAA-FET), Negative Capacitance FET (NC-FET), and Ferroelectric FET (Fe-FET) for better gate electrostatic control, and for potential non-volatile memories. But before that, another material system is of great interest in terms of high performance, low power, and flexible ultra-scaled electronics, 2-dimensional (2D) material that is.

2-Dimensional Ultra-Thin Semiconductors

One of the major issues with ultra-scaled devices is the short channel effect (SCE), which occur in MOSFETs when the channel length is comparable to the depletion-layer widths around the source/drain (S/D) junctions. SCE results in many other degradation in device performance including hot carrier degradation, drain-induced barrier lowering (DIBL), and velocity saturation. Solutions to overcome these consequences include increasing the channel area controlled by the gate, minimizing the depletion width by shallow doping near S/D, and introducing ultra thin body (UTB) silicon-on-insulator (SOI) structure. In SOI the depletion width is physically limited by the thickness of the semiconductor, which allow better electrostatic gate control. Two-dimensional (2D) materials have a similar effect as SOI technology. 2D have at-

tracted extensive research interests due to their electrical properties. A single layer of carbon atoms off graphite was the first 2D material in its current known form known as graphene, ever since, the research on 2D materials had an exponential expansion to the present day. In this thesis, I will study a very promising material, which is molybdenum disulfide (MoS_2). MoS_2 is part of the Transition metal dichalcogenide (TMD) monolayers family (atomically thin semiconductors that is usually represented as MX_2, where M is a transition metal atom (Mo, W, etc.) and X is a chalcogen atom (S, Se, or Te)). In MoS_2, as in all TMDs a layer of molybdenum (M) atoms is sandwiched between two layers of sulfur (S), as seen in a representative MOSFET in Fig. 1.4 with monolayer MoS_2 as a device channel.

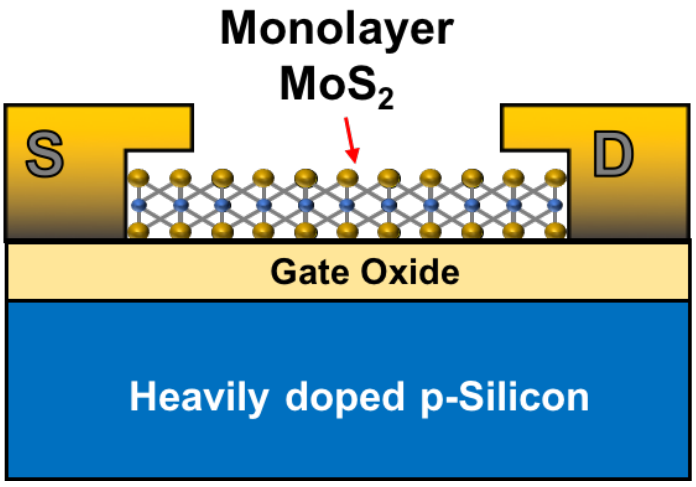

Fig. 1.4. Schematic of back gated MOSFET with MoS_2 as a channel

Currently, these TMD materials are expected to be employed in low power low cost transistors (optical emitters and detectors) or flexible electronics as the 2D materials are flexible in its nature. Our research groups have done an incredible progress in developing MoS_2 [6,7]. MoS_2 has an indirect bandgap semiconductor similar to silicon, with a bandgap of 1.3 eV, however, the bandgap changes from 1.3 eV up to 1.8 eV as the number of layers or its thickness decreases. Thus, it is important to accurately characterize this material when utilized for electronic devices.

1.2.2 Gallium Nitride (GaN) and Gallium Oxide (Ga_2O_3)

When it comes to high temperature, high power, and high frequency applications, GaN along with other nitride compound semiconductors such as InN, AlN, AlGaN, and InAlN have attracted researchers' attention to replace the long dominated Si-based power and RF devices. Its wide band gap (ranging from 3.4 eV to 6.2 eV for $Al_xGa_{1-x}N$), high breakdown field ($\sim 10^6$ V/cm), high electron saturation velocity ($\sim 10^7$ cm/s), high sheet carrier concentration (10^{13} cm^{-2}), and high electron mobility ($\sim$1200 cm^2/V.s) are superior properties that GaN enjoys compared to other semiconductors. However, achieving a gate dielectric with low interfacial defect (interfacial trap, D_{it}) density, high permittivity and low leakage current still remains challenging [8] on GaN. Also, unlike Si/SiO_2, the interface between GaN and its native oxide Ga_2O_3 has a very high trap density. ALD has been proven to be the most efficient fabrication process to grow a lattice-matched insulator. Using ALD to grown a defect-free interface was previously achieved on other systems by growing a lattice matched epitaxial film as in lanthanum oxide (cubic La_2O_3) on GaAs (111) [9] which produces the best transistors ever made on GaAs, as well as the first CMOS circuits made using both p-GaAs and n-GaAs channels. Other ALD films have also been grown on GaN-based HEMT and MOSHEMT devices [10, 11]. The key feature to have an epitaxial insulators is to have a very low lattice mismatch. In the case of Sc_2O_3 [10] grown film on AlGaN/GaN HEMT has a large lattice mismatch (between Sc_2O_3 and the GaN substrate ($\sim$9%)), epitaxial growth could not be achieved, other various dielectrics, such as HfO^2 [12], Al_2O_3 [13], SiO_2 [14], etc, have also been employed as dielectrics on GaN in various studies, However, GaN devices with a low defect interface and high quality dielectric have not been achieved with any material.

Also, and for the past 5 years, β-Ga_2O_3 has attracted more and more interests due to its ultra-wide bandgap (4.8 eV) compared with GaN (3.4 eV), potential cost-effective large size substrate, and moderate electron mobility, which makes it a promising candidate as the next generation power electronic materials

1.3 Emerging Transistors Structures

In addition to the effort being made to increase channel mobility, and to reduce power dissipation by limiting the leakage current (current that tunnel through gate oxide to the gate electrode), an innovative device structures are also a major research topic that were introduced (and eventually applied by Intel in 14 nm node's FinFET) few years back. Engineering device structure to reduce the subthreshold swing (SS) in the transistors transfer characteristics, or to effectively gain better gate control over the channel are one of the ideas that could spare Moore's law extra more years to survive. Fig.1.5 summarizes the emerging electronic devices accoridng to the new International Technology Roadmap for Semiconductors - ITRS 2.0. Chen et al. [15] in his 2014 has reported the challenges in CMOS scaling that motivated research on a wide range of emerging devices, to extend the life of CMOS or to explore beyond-CMOS applications. In this report, I have studied some of these emerging devices such as: FinFET, nanowire (NW) FET, NC-FET, and FeFET and will continue study them before finalizing my thesis.

1.3.1 Ferroelectric Insulators

Steep-slope transistors and Ferroelectric switches both share a ferroelectric gate insulator integrated in their FET structure. The ferroelectricity as a main feature that have recently enabled below 60 mV/dec characteristic in these devices depends on the polarization mechanism occur within the ferroelectric gate insulator.

What polarization mechanisms occur in ferroelectric insulators?

There are four types of polarization: electronic, ionic(atomic), orientation, and spacecharge (interfacial).

- **Electronic polarization** occurs when the center of an electron cloud around anucleus is displaced under an applied electric field.

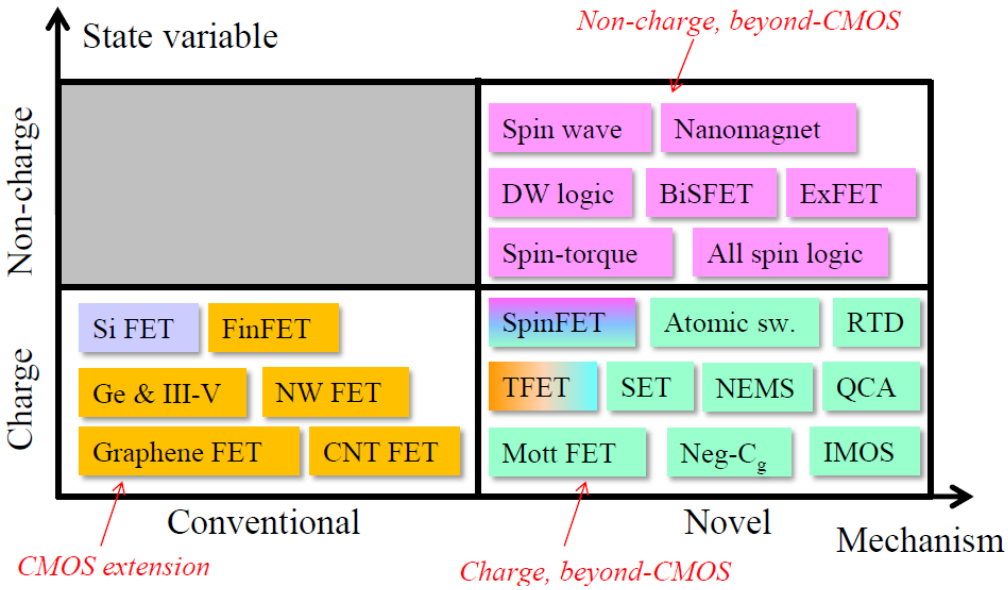

Fig. 1.5. A classification of emerging devices based on the state variables and the switching mechanisms. [15]

- **Ionic polarization** occurs in ionic materials under an applied field that acts to displace ions in a direction opposite to the applied field and cations in the direction of the filed.

- **Orientation polarization** can occur in materials that possess permanent electric dipole moments. Unlike the previous types, orientation polarization is highly temperature dependent because these permanent dipoles tend to become aligned with the applied electric field, but thermal effects act as a counter alignment.

- **Space charge polarization** this polarization results from the accumulation of charge at the electrode or at the interface in multiphase dielectrics. Such polarization occurs when one of the phases has a much higher resistivity than the other, normally, in ferrites and semiconductors.

When insulators are under electrical operation, polarization subjected to an electric field is a function of time, the time that which the permanent or induced dipoles within the insulator can reverse their alignment. This time is called the relaxation time τ_r, ($1/\tau_r$ is called the relaxation frequency). The relaxation times are different for different types of polarization mechanisms, thus, the polarization response is different for different filed frequencies.

What is Ferroelectricity?

Ferroelectricity in a material is defined as the spontaneous alignment to electric dipoles by their internal mutual interaction when no electric field is applied. The ferroelectric materials is said to possess permanent dipoles when the local field increases in proportion to the polarization amplitude. A change in the spontaneous polarization will result in a change in the surface charge. This can cause a to current flow even when no external voltage is applied to the capacitor gate electrode in capacitors with ferroelectric insulator. The ferroelectric insulators have a very high dielectric constants at a relatively low applied field frequencies.

1.3.2 Steep-Slope Transistors

As it could be seen from Fig.1.5, there are many devices concepts that could be implemented in order to boost the device performance and have SS below the Boltzman's thermionic limit of SS for MOSFET as in eq. 1.8 (which what was meant earlier in this chapter by 60 mv/dec at room temperature), from these concepts are the tunneling FET (TFET) [16,17] and negative-capacitance FET (NC-FET) [18,19]. The SS of a MOSFET is expressed as:

$$SS = ln(10) \times m \times \frac{kT}{q} \tag{1.5}$$

$$m = 1 + \frac{C_{it} + C_S}{C_{ox}} \tag{1.6}$$

$$SS = 2.3\left(\frac{kT}{q}\right)\left(1+\frac{C_{it}+C_S}{C_{ox}}\right) \tag{1.7}$$

where k is Boltzmann constant, T is temperature, q is elementary charge, C_{it} is interface trap capacitance and C_S is the surface capacitance. C_S approximately equals the depletion capacitance (C_D). Ideally, transistors have no interface traps, hence, C_{it}=0, and $C_S \ll C_{ox}$, eq. 1.7 at room temperature becomes (in mV/dec):

$$SS = 2.3\frac{kT}{q} \sim 60 \tag{1.8}$$

Negative Capacitance Field Effect Transistor (NC-FET)

Work now in progress in the device research community to effectively operate transistors below this limit. NC-FETs are one of recent novel concepts that was first introduced here at Purdue by Salahuddin and Datta [18]. although that NC-FET is fundamentally an integration of a ferroelectric oxide in the gate stack of a MOSFET in order to a get a net negative capacitance [20]. The negative capacitance here is a conceptional based on eq. 1.7 when the second term become a negative number and result in a SS being less than the limit in eq. 1.8. Planar MOSFETs, FinFETs and even gate-all-around, can incorporate a ferroelectric properties. Electrically, the ferroelectric oxide layer acts as a voltage amplifier due to the polarized dipoles within. Fig.1.6 shows the schematic of a NC-FETs device and an equivalent elemental capacitances.

1.3.3 Ferroelectric Transistors (Fe-FET)

NC-FETs stems from a what is called the ferroelectric FET (FeFET). NC-FETs and FeFETs benefit from the ferroelectric properties in insulators such as hafnium oxide (HfO_2). FeFETs however, are slightly different in their applications. NC-FETs are designed for low power logic while FeFETs are for non-volatile memories. Ferroelectric devices show improved sub-threshold slopes. NC-FETs are preferred to

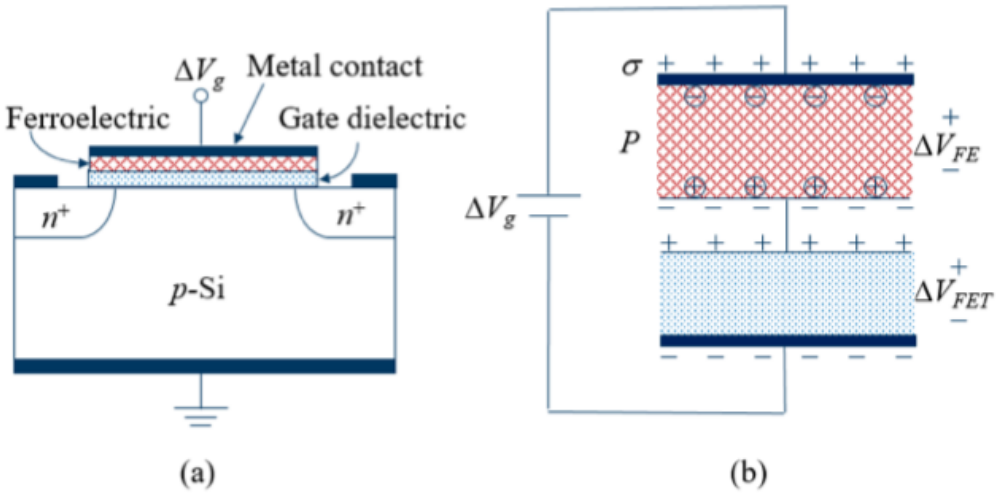

Fig. 1.6. Schematics of NC-FETs, (a) Device structure, and (b) illustration of the gate stack with Ferroelectric material. [20]

have zero hysteresis in their transfer curve, FeFETs exploit the hysteric nature of the ferroelectric dielectric for the non-voltile application.

Ring oscillator that can operate at frequencies similar to regular dielectrics has already been reported at 14 nm technology by Z. Krivokapic [21], but NC-FETs still faces some challenges. The ferroelectrics are thick by nature (50 to 80 angstroms), hence, scaling down while keeping the ferroelectric properties is a genuine concern, in addition to the reliability challenges, and some distinctive device design constraints due to parasitics.

1.4 Electrical Characterization Methods for Modern Devices

The development of the above-mentioned systems and material involves an advancement in the devices technologies and a consequent advancement in the testing methods and performance measures. The following methods are have established a good electrical characterization techniques that are reliable enough to perfectly gauge the main material physical properties and the relative device electrical performances.

1.4.1 AC Conductance

The AC conductance method is widely used in characterizing oxide/semiconductor interface, and it is recognized as one of the most sensitive in extracting interface traps due to its sensitivity to the changes in the conductance energy map caused by defects. MOSCAPs are the typical structures used in characterization [22,23]. The equivalent circuit of a MOSCAP under the test is illustrated in Fig. 1.7.

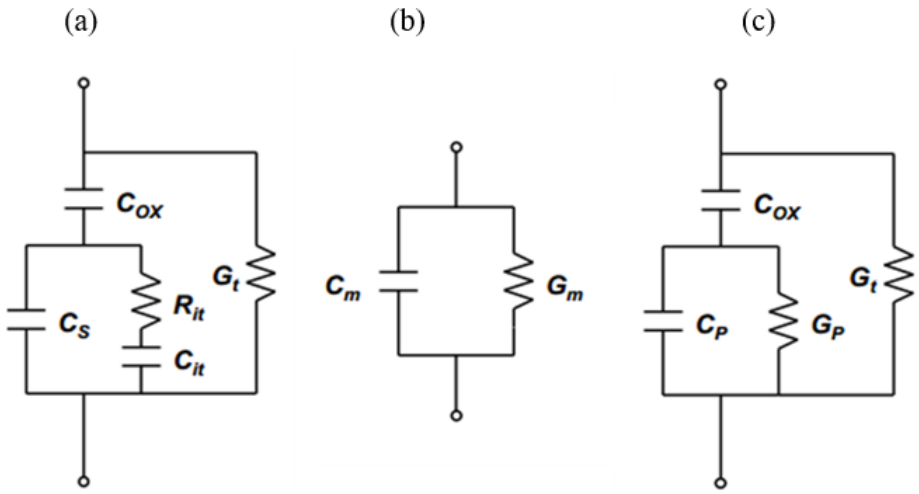

Fig. 1.7. Equivalent circuits of measurements; (a) an equivalent circuit model of the MOS capacitor, (b) the measured circuit, (c) a simplified circuit of (a) [24]

The extracted (D_{it}) can be expressed by the following equation:

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \tag{1.9}$$

Where $\frac{G_p}{\omega}$ is

$$\frac{G_p}{\omega} = \frac{\omega(G_m - G_t)C_{ox}^2}{G_m^2 + \omega^2(C_{ox} - C_m)^2} \tag{1.10}$$

And C_{ox}, C_m, G_m and G_t are oxide capacitance, measured capacitance, measured conductance, and measured oxide tunnel conductance, respectively. Then the trap energy level is determined according to the following:

$$\Delta E = E_C - E_T = kT \times ln\left(\frac{\sigma V_T N}{2\pi f}\right) \tag{1.11}$$

And k, T, σ, V_T, N, and f are Boltzmann constant, temperature, trap capture cross section, thermal velocity, conduction band density, and conductance peak corresponding frequency, respectively.

1.4.2 Pulsed Current-Voltage (Pulsed I-V)

Pulsed current-voltage (pulsed I_d-Vgs or Pulsed I-V) has been considered as one of direct and effective methods for detecting MOSFET's oxide/semiconductor interface defects, as well as the current collapse characterization in high-electron-mobility transistors (HEMTs) [25,26]. Pulsed I-V is also well-knonw for the ability to avoid or eliminate any self-heating effect that gives insight into the degradation of a transistor characteristics due to negative differential resistant (NDR). This measurements usually targets the fast interface traps but depending on the pulse's width and frequency, other traps could be probed as well. Pulsed I_d-Vgs measurements is based on a constant drain bias synchronized with a pulsed gate biases. The pulsed gate sweeps is done into two splits: 1) up-sweep with low V_{gs} pulse base, and 2) down-sweep with high V_{gs} pulse base. Fig. 1.8 shows a schematic of the pulsed I-V measurements signal.

During the up-sweep sequence, V_{gs} is pulsed to the normal sweeping values as in DC measurements up until the maximum gate voltage with low V_{gs} base (below threshold voltage (V_T)) in between pulses. That means pulses are having the same width, same delay between each consecutive pulses with stepped up pulse heights. The drain current is measured simultaneously at each pulse (when V_{gs} is the pulse height). The same procedure is done with down-sweep sequence but in the opposite direction. The hysteresis in V_T Between the up-sweep transfer characteristic, where

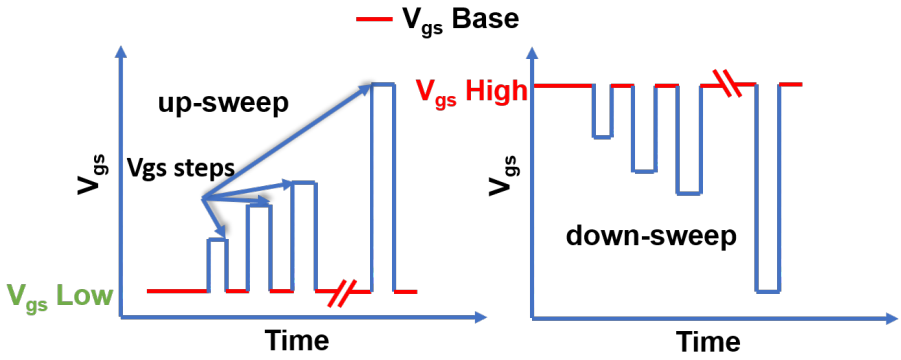

Fig. 1.8. Illustration of the pulsed I-V signal applied on gate

V_T extracted here corresponds to the empty-traps state and down-sweep transfer characteristic, where V_T corresponds to filled-traps state Therefore, is attributed to the traps with the detrapping time constant larger than the pulse width. Then, using eq. 1.12

$$Q_{it} = \frac{1}{q} C_{ox} \Delta V_T \tag{1.12}$$

1.4.3 Conventional and Single Pulse Charge Pumping methods

The conventional charge pumping (CP) method is one of the techniques that is widely used for characterizing the interface states (or interface traps) of MOSFETs, making it suitable for measurements on small geometry devices instead of large-area MOS capacitors. The CP process in MOSFETs first discussed by Brugler and Jespers [27], and utilized for the interface analysis by Groeseneken et al. [28]. The CP method allows the interface state density (N_{it}) to be evaluated by measuring average current caused by frequent gate pulses. CP does not only estimate N_{it} quantitatively but also enables a spacial analysis of there energy distribution investigate their energy and spatial distributions [24, 29, 30]). It begin with an application of train of pulses as a gate voltage with sufficient amplitude for the surface under the gate to be driven into inversion and accumulation. A DC current (I_{cp}) is generated by these pulses then

measured and averaged. I_{cp} is measured at the substrate, with the source/drain tied together, or at the source and drain separately. Fig. 1.9 shows a schematic of the CP process and explained herein.

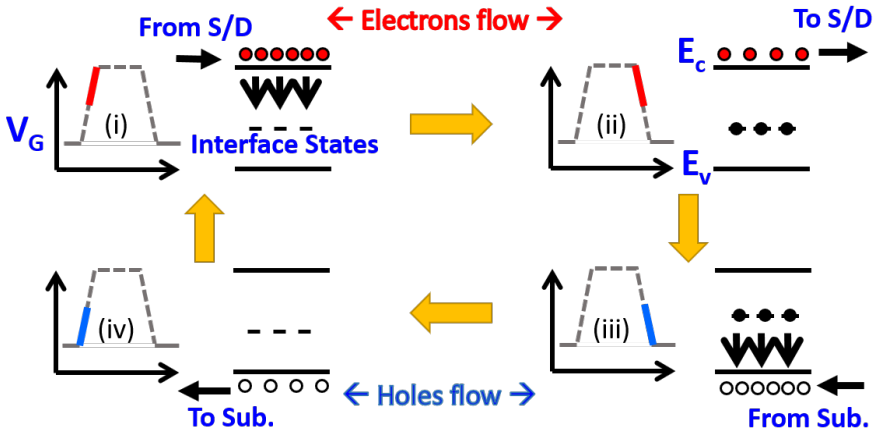

Fig. 1.9. Schematic band diagram of n-MOSFET device showing the CP process during the conventional CP measurements

During a single pulse on the gate with voltage varies between the accumulation and the inversion, four processes take place: (i) electrons flow-in, where the electrons are captured to the interface states. Number of electrons captures here depends on the time constant of the traps and pulse transient specification. (ii) electrons flow-out, and some of the captured electrons by the interface states cannot escape. hence, the number of electrons flow out to S/D is decreased. (iii) holes flow-in, where a recombination of captured electrons with free holes occur. (iv) holes flow-out, where the number of holes that flow out to the substrate is decreased and again the difference is related to total N_{it} (All four processes are depicted in Fig. 1.9). The averaged difference between the flow-in electrons and the flow-out ones gives rise to a total I_{cp} current which is proportional to interface trap density in $eV^{-1}\cdot cm^{-2}$ ($D_{it}(E)$):

$$I_{cp} = qfD_{it}\Delta E \tag{1.13}$$

Where q, f, and ΔE are the elemental electron charge, pulse signal frequncey, and the energy difference between the specific trap and conduction band edge (E_C), respectively.

The current averaging, however, overlook some of the fundamental events of electrons capture to defects, and recombination with holes, in the CP sequence. The gate is swept and the net charge pumping current is measured in DC, but the time for one dc point takes 10150 ms, and a typical CP measurement can have tens of points. Thus, the CP speed is slow (on the order of seconds) in order to measure these recovery times of stress induced interface states (on the order of μs) [31]. Therefore, measuring the CP current in real time is suggested and performed to measure the recovery time of stress-induced interface states [32], enabling a direct access to these fundamental processes, and availing a modified method of CP called single pulse charge pumping (SPCP). SPCP technique detects the net charges pumped into devices by monitoring the transient current of a single pulse applied on a transistor through off-state to on-state. More details on the use of this method is discussed in chapter 3.

1.4.4 Low-Frequency Noise (LFN)

Low-Frequency Noise (LFN) measurements is one of most effective characterization methods to study low dimensional and integrable solid state devices. But before explaining the importance of LFN an introductory summary to "Noise" in the semiconductor is important.

Noise in electronic semiconductors devices, MOSFETs, arises from the fluctuation in voltage or current in certain physical areas. To be more specific it arises from the fluctuation in the charge carriers that are responsible for the current transport throughout the channel and channel/oxide interface. The inherent noise in electronic devices are undesirable that it effects the performance and the overall circuit capabilities. Signal-to-noise ratio, for example, limits the lowest communicable signals without being distorted. Although that the nature of these fluctuated carriers are in-

herently found in semiconductors devices, noise can function as a investigative probe to determine an important device parameters [33,34]. Noise is usually defined according to the origin of the fluctuated charge carriers, the power spectral density (PSD) related to the operational region of the device, and frequency. In general, noise in semiconductors device are categorized into different types as in fig. 1.10

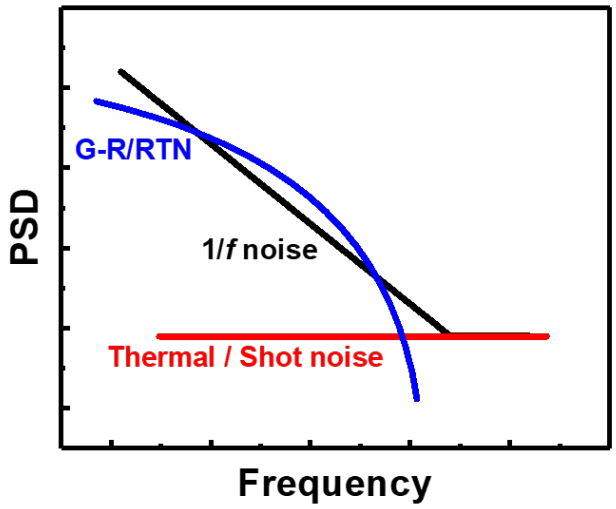

Fig. 1.10. Schematic representation of different types of noise power spectral density vs frequency in MOSFETs

- **Thermal noise**: due to the random thermal transport of electrons in the material.
- **Shot noise**: stems from from the random statistical fluctuation of the current charge carries over a potential barrier. Thermal noise and shot noise is more pronounced in high operating frequencies, Ghz to THz regions.
- **Generation-recombination (*G-R*) noise**: due to the fluctuation in number of free carriers in relation to random transitions of charges between one energy

level to another, for example, the transition between the conduction band carriers to a localized level in the forbidden bandgap. G-R noise is a function of both temperature and biasing conditions.

- **Low-frequency noise ($1/f$ or flicker noise)**: Low frequency noise is characterized by its current or voltage PSD. It is called $1/f$ noise because the PSD is inversely proportional to the measured frequency. generally, the PSD of $1/f$ noise is based on the fluctuation in drain current of the transistor. If the measured power spectral density $S(f)$ has a slope, which is inversely proportional to frequency with a constant f^{γ}, where γ is approximately 1, then the measured noise is considered as $1/f$ noise (as shown in Fig. 1.10). In MOSFETs where the surface of the channel is the where the carrier transport occur, a large noise at low frequencies also produced, this makes the study of $1/f$ noise very important, especially, with the miniaturizing of devices, and the integration of crystalline oxides. Low-frequency noise will discussed in more details later chapter in 4.

- **Random telegraph noise (RTN)**: In devices with a relatively small area, as well as low interfacial traps only few energy levels are are available for transport, or fluctuations as we discussed in terms of noise, these levels are within few k_BT form the Fermi level, RTN noise hence produced due to the trapping detrapping mechanism, in a very similar fashion as G-R noise. In fact, RTN noise is a special case of G-R noise which is displayed as discrete switching events in the time domain. The PSD for the RTN noise and the G-R noise are both of the Lorentzian type [35]. The capture time and emission time, as well as the magnitude of the voltage or drain current fluctuations determine the characteristics of the RTN noise. When an electron is captured by a trap, the current switches to the lower value and remains at the same state as long as the electron remains trapped, When the trapped electron is released, the current jumps to the high value and remains at the same state as long as another electron is captured by the trap as illustrated in Fig.

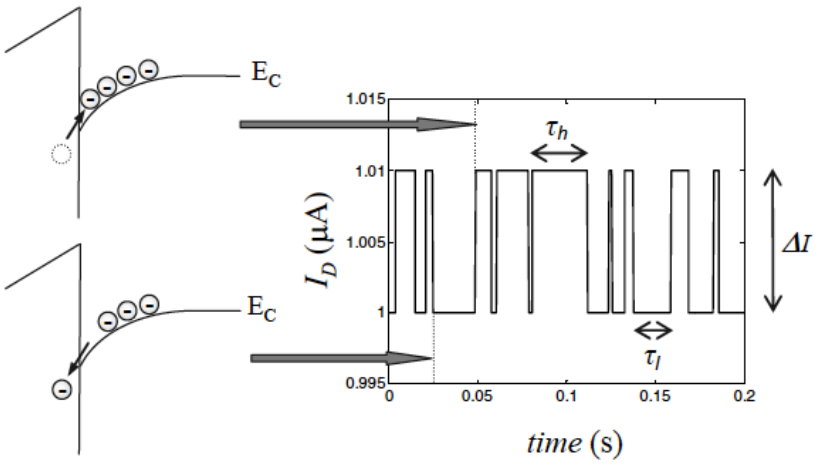

Fig. 1.11. Schematic representation of RTN noise along side a representation of the trapping de-trapping process. The drain current fluctuate between two distinct current levels when a channel electron moves in and out of a trap in the gate oxide [35].

1.5 Thesis Overview

In this thesis, major power dissipation issues in MOSFETs has been introduced with some of state-of-the-art solutions. The gate insulator/channel interface has been a central part of these challenges in solid-state devices, for both, low power applications (CMOS, Memories, IoTs, ... etc), and high power applications (power electronics, RF applications, ... etc). The thesis main discussion is the proper proper choice of a characterization method and/or reliability studies for both streams, as well as providing insights into some of the potential channel materials and device concepts (or structures) before employing them into the post silicon generation of solid-state devices.

Chapter 2 discusses systematically the ALD passivation influence on the interfacial properties of our new incorporated epitaxial oxide MgCaO, as well as a comparison with the amorphous A_2lO_3 on wide-bandgap semiconductors channels made of GaN and Ga_2O_3, explaining the significance of the low surface traps density (defects) on the

performance of these potential devices. Measurements methods such as C-V, G-V, and photo-assisted C-V were conducted on capacitors structures and showed compelling improvements in interface trap density in GaN with a lattice matched oxide MgCaO, and Al_3O_3 ALD grown on commercially available (-201) oriented surface as high quality surface for future β-Ga_2O_3 high power and high frequency devices.

These systems were studied again but rather as transistor devices in chapter 3. HEMT and MOS-HEMTs devices with InAlN and AlGaN, as part of the gate stack on a GaN channels, are discussed using pulsed I-V and a modified charge pumping method which is the single pulse charge pumping (SPCP). The SPCP study is one of the main contributions of this thesis owing to the simplicity and ingenuity of this measurements in characterizing interface traps not only for GaN transistors which has a 2-dimentional electron gas (2DEG) on insulating substrate, but also for GaN other state-of-the-art devices that do not exhibit body contacts such as ultra-thin-body (UTB) devices with floating body channels. Also, a novel method is proposed for the simultaneous extraction of energy distribution of donor- and acceptor-like interface trap states based on the difference in the gate voltage-dependent ideality factors due to the photonic response of the carriers excited with ultraviolet light within the β-Ga_2O_3 channel surface.

Chapter 4 discusses advanced electrical characterization techniques for Ge NW and 2D MoS_2 negative capacitance FETs (NC-FETS) or Ferroelectric FETs (FeFET) with hafnium zirconium oxide (HZO) incorporated in gate dielectric of these devices. Low-frequency noise measurements reveals am interesting fact proves the negative capacitance existence. It was also found that when HZO is integrated in NC-FETs not only improve on and off-state current, but also suppresses noise and provide better gate electrostatic control.

Chapter 5 studies the time response characteristics of these Ge NW FeFETs with HZO as gate dielectric and the significance of polarization reversal process in device speed and current performance. This chapter also discusses some of the reliability issues related with the ferroelectric HZO in terms of switching mechanism and en-

durance. The studies take into the account the integration of ferroelectric HZO with other linear dielectric material and gives impressions about the negative effects on HZO reliability.

Chapter 6 gives a summary and future work suggested for this thesis.

2. INTERFACE CHARACTERISTICS OF EMERGING WIDE-BANDGAP SEMICONDUCTORS

2.1 Introduction

Lacking a naturally grown native oxide on substrates surfaces of both surface-channel and buried-channel MOSFETs is one of the main drawbacks the III/V semiconductor materials is suffering. Commercializing these high mobility channel is limited by the progress made in perfecting the oxide/semiconductor interface in these systems. This is mostly due to the ionic dangling bonds (*traps*) found on the substrate surface, the substrate surface roughness, or the oxide charges (*space charges*) within the gate oxide itself. Many fabrication processes where developed to minimize the density of those traps (D_{it}), because the higher the D_{it} the more scattering process occur with charge carriers responsible for the current transport. As a result to these extra scattering, devices will dissipate higher power, have lower current performance, and incur higher levels of noise. The reasons behind the formation of the above mentioned traps in a lattice mismatched oxides will not be discussed, since this is out of the scope of this chapter, but we will discuss the importance of accurately characterizing the oxide/semiconductor interface in order to design an appropriate gate insulator for III/V semiconductor devices, specifically, for devices with Gallium Nitride (GaN) and the new emerging wide-bandgap "semiconductor" Gallium oxide (Ga_2O_3) as a conducting channels.

2.2 Epitaxial Lattice Matched MgCaO Insulator on GaN

We have demonstrated for the first time that an epitaxial $Mg_xCa_{1-x}O$ film can be deposited on GaN (0001) by ALD with low interfacial defect density, as demonstrated by excellent transistor properties [36].

Magnesium oxide (MgO) and Calcium oxide (CaO), have been studied as a potential gate dielectric for GaN devices due to their relatively high dielectric constants (MgO ∼9.8, CaO ∼11.8) and large band gaps (both 7 ∼ 8 eV), which make them a suitable gate oxides for GaN. Moreover, the mixture of both oxides, namely, Magnesium Calcium oxide (MgCaO), have a lattice constant follows Vegard's Law [37] which states that a linear relation exists between the crystal lattice constant of an alloy and the concentrations of the constituent elements at constant temperature. And similarly, the bandgap E_g of the mixture could be written as a linear relationship between the band gap and composition as:

$$E_{g,A_xB_{1-X}} = xE_{g,A} + (1-x)E_{g,B} \tag{2.1}$$

Fig. 2.1 depicts the band alignments for GaN and other semiconductors with various dielectrics. A large band offset can clearly seen for both band edges (conduction band, E_c, and Valence band, E_v) for MgCaO with 1:3 Mg to Ca composition.

Interestingly enough, the lattice size of MgCaO fall between those of MgO and CaO and close to GaN lattice size (a mismatch of -6.5% for MgO and +6.5% for CaO). Hence, a precise control of the composition of $Mg_xCa_{1-x}O$ would result in a high quality lattice matched oxide with GaN. Therefore, this epitaxial oxide/GaN stack is expected to provide a better interface with lower defect density for electronic devices. Three different composition ratios were developed and examined, Mg:Ca=1:1, Mg:Ca=1:2 and Mg:Ca=1:3. The compositions of the resulting films were determined by Rutherford back scattering (RBS) [36] to be $Mg_{0.72}Ca_{0.28}O$, $Mg_{0.51}Ca_{0.49}O$, and $Mg_{0.25}Ca_{0.75}O$, respectively. The lattice mismatch was found to be 2.2% for $Mg_{0.25}Ca_{0.75}O$ by High-resolution X-ray diffraction (HRXRD). Fig. 2.2 shows a TEM image of the interface between MgCaO film and GaN surface.

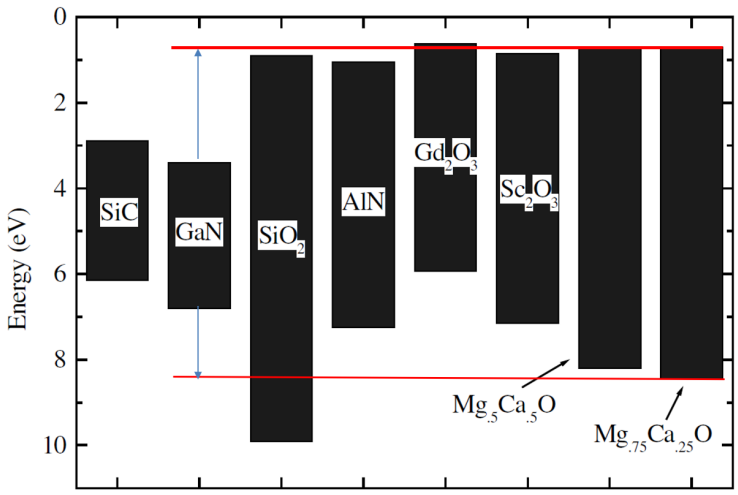

Fig. 2.1. Band alignments for SiC, GaN with various dielectrics [38].

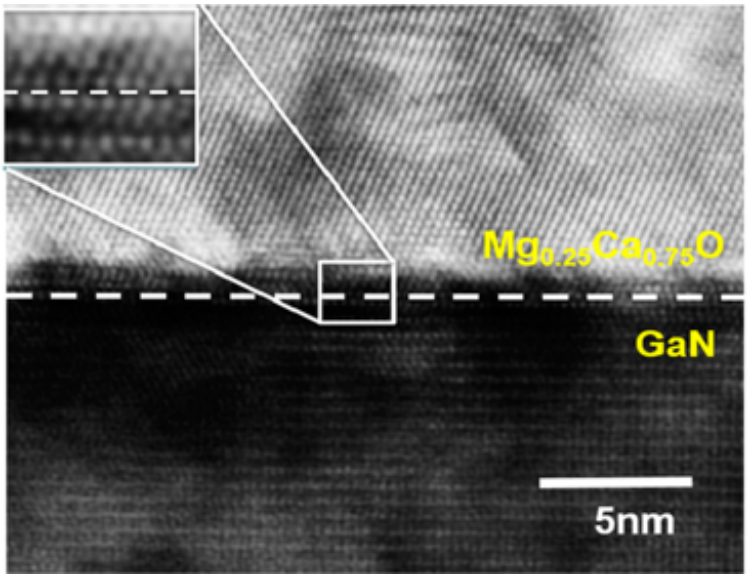

Fig. 2.2. Cross-sectional TEM of $Mg_{0.25}Ca_{0.75}O$ film grown on GaN(0001) surface. [36]

2.3 MgCaO/GaN Interface Electrical Characterization

In order to examine the quality of the MgCaO/GaN interface for each of the three compositions mentioned above, a Metal-Oxide-Semiconductor capacitors (MOSCAPs) were fabricated by depositing 15 nm of $Mg_xCa_{1-x}O$ with 5 nm Al_2O_3 as a capping layer on 5 μm epi-layers GaN grown on sapphire substrate with resistivity of 0.02 Ω·cm. Then a circular capacitor pattern was defined by photo lithography followed by 300 nm of aluminum deposition as a gate electrode followed by lift-off process. Fig. 2.3 shows (a) The top view and, (b) Side view of the 5 nm Al_2O_3/15 nm $Mg_xCa_{1-x}O$/GaN MOSCAPs.

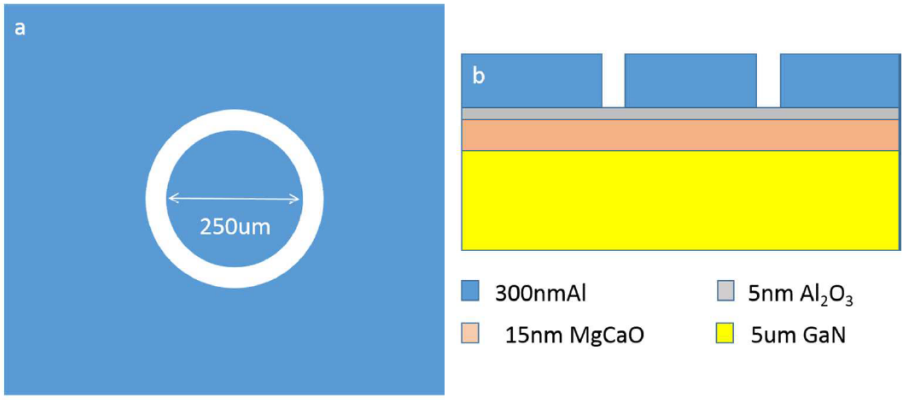

Fig. 2.3. (a) The top view, and (b) Side view of the 5 nm Al_2O_3/15 nm $Mg_xCa_{1-x}O$/GaN MOSCAPs. [36]

2.3.1 Interface Traps via C-V and AC Conductance Methods

A high precision HP4284 LCR meter was then used for the capacitance-voltage (C-V) and conductance-voltage (G-V) measurements in room temperature (RT) first and high temperatures (HT) (HT measurements is essentially due to the fact that the large bandgap of GaN does not allow RT measurements to effectively probe defects near the middle of the bandgap. Therefore, MOSCAPs were also measured

at 150 ^{o}C). Using C-V measurements of these MOSCAPs the D_{it} level could be extracted from conductance peaks of different frequencies and gate voltages using the AC conductance method. The AC conductance is used herein.

For conductance method, we need to determine the dielectric constant k for MgCaO. To calculate the dielectric constant the maximum gate capacitance value at low frequency is measured, which is the accumulation capacitance at 1 kHz. This capacitance is approximately the MgCaO oxide capacitance (C_{ox}):

$$C_{ox} = \frac{k\epsilon_o A}{t_{ox}} \tag{2.2}$$

Where A is the capacitor area, $\epsilon_o = 8.85 \times 10^{-12} F.m^1$, and t_{ox} is the oxide thickness. We found that $k \approx$10.8 which is close to the permitivities of MgO and CaO.

2.3.2 Frequency and Temperature Dependent C-V

A multi-frequency C-V measurements were conducted for 5 nm Al_2O_3/15 nm $Mg_xCa_{1-x}O$/GaN MOSCAPs at RT and HT. D_{it} is believed to be relatively low from the very small frequency dispersion observed in 1 kHz to 1 MHz (<6% frequency dispersion is observed in deep depletion region for all three $Mg_xCa_{1-x}O$ samples, and about 20% dispersion is seen in the same region for Al_2O_3/GaN sample) in Fig. 2.4, this demonstrate that the epitaxial MgCaO, regardless of which composition, has less interface traps as compared to the well controlled Al_2O_3, and it is an indication of a good interface between GaN and the MgCaO gate stack. C-V measurements for the four samples is summarized in Fig. 2.4. As mentioned above, and due to the low interfacial trap density, a numerical value for D_{it} could not be extracted from the room temperature CV measurements. During the CV measurement, the Fermi level is moved deeper in the band gap at a higher temperature; thus, defect information can be obtained over a wider range of energies within the band gap [39]. Fig. 2.5 represents the conductance peaks vs. frequency for each of the three compositions and 20 nm Al_2O_3 for comparison. From eq.1.9 and Fig. 2.5, D_{it} is extracted for each of MgCaO compositions in this study and plotted in 2.4 (I).

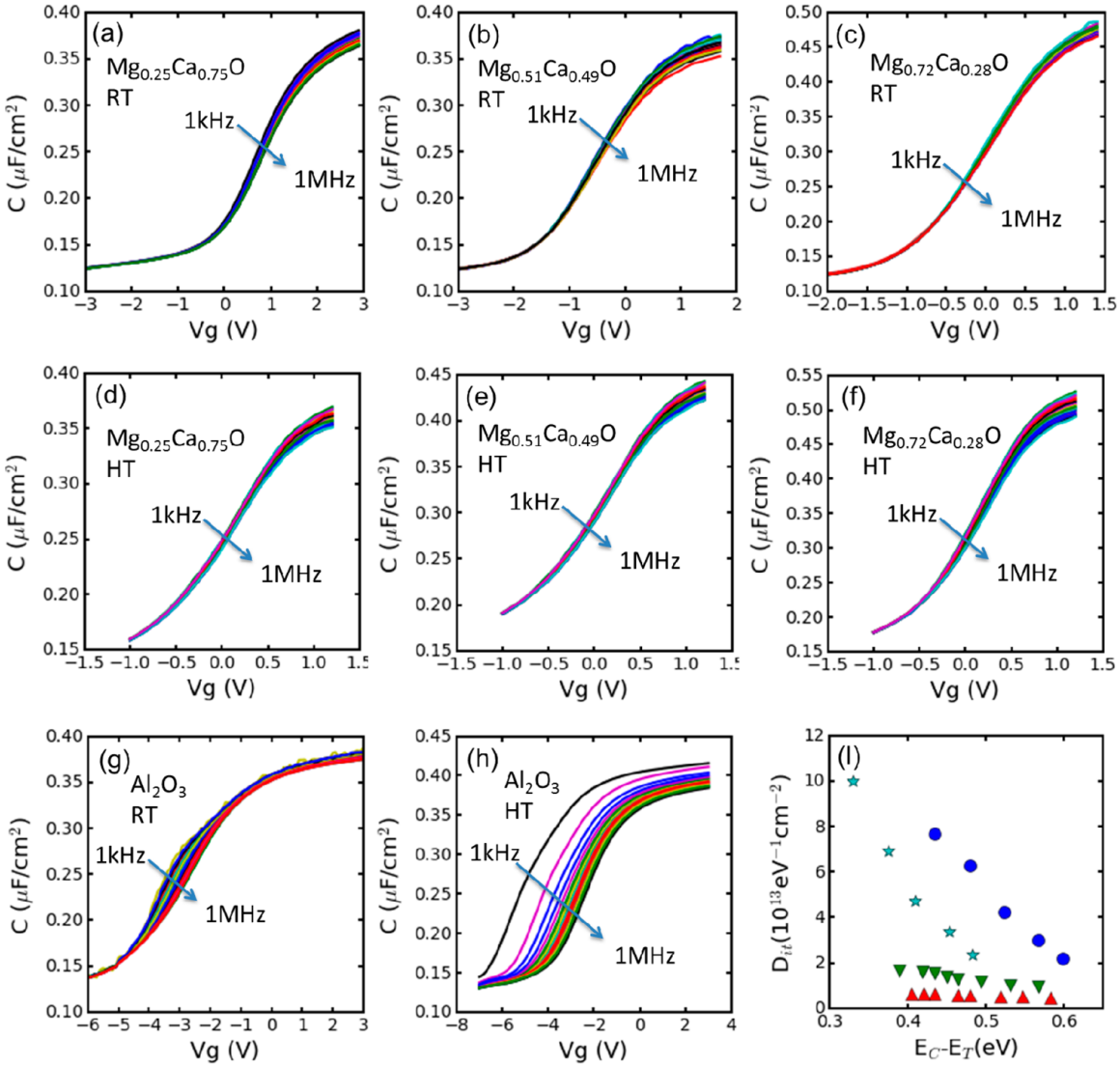

Fig. 2.4. C-V measurements for $Mg_xCa_{1-x}O$ /GaN and Al_2O_3/GaN samples.
(a) to (c) at RT (20^{o}C); (d) to (f) at 150^{o}C, (g) 20^{o}C 20 nm Al_2O_3/GaN for and (h) at 150^{O}C; (i) D_{it} summary of four samples determined by the conductance method: ($\star$) 20 nm Al_2O_3/ GaN, ($\bigcirc$) 5 nm Al_2O_3/15 nm $Mg_{0.72}Ca_{0.28}O$/GaN, ($\bigtriangledown$) 5 nm Al_2O_3/ 15 nm $Mg_{0.51}Ca_{0.49}O$/GaN, and ($\bigtriangleup$) 5 nm Al_2O_3/ 15 nm $Mg_{0.25}Ca_{0.75}O$/GaN. [36]

The differences between the three epitaxial MgCaO samples is clear in terms of D_{it} levels, but, the lattice mismatch of the $Mg_{0.25}Ca_{0.75}O$ is slightly larger than that

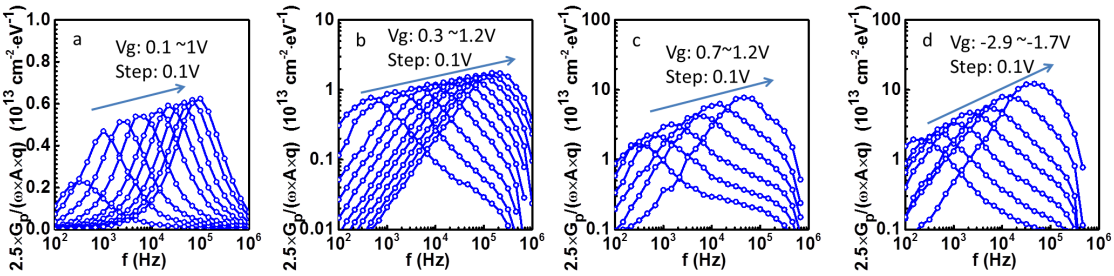

Fig. 2.5. G_p/ω vs. frequency at 150 ^{o}C. (a) 5 nm Al_2O_3/ 15 nm $Mg_{0.25}Ca_{0.75}O$/GaN (b) 5 nm Al_2O_3/ 15 nm $Mg_{0.51}Ca_{0.49}O$/GaN (c) 5 nm Al_2O_3/15 nm $Mg_{0.72}Ca_{0.28}O$/GaN (d) 20 nm Al_2O_3/GaN. [36]

of the other two $Mg_xCa_{1-x}O$ samples, this sample however, has the lowest D_{it} value among the others, with a lowest measured D_{it} level of $\approx 5 \times 10^{12}$ eV$^{-1}\cdot$ cm^{-2}.

From the AC conductance measurements, we can summarize that an epitaxial $Mg_xCa_{1-x}O$ films have been successfully grown on GaN (0001) surfaces using ALD. We can also confirm the high quality interface of this gate dielectric with GaN channel devices. The study showed that the traps density is affected not only by the lattice mismatch but also by the composition choice of the film. $Mg_{0.25}Ca_{0.75}O$ film is found to have the lowest interface D_{it} and hence, best interface quality with fewest traps. Thus, and in the area of high-power and high-frequency applications, this epitaxial $Mg_xCa_{1-x}O$ film can provide higher performance devices that other non-epitaxial counterparts. The ultimate goal of developing this material is to be included in a gate stack of GaN MOS-HEMT devices with high quality oxide/semiconductor interface [40], which is discussed next.

2.4 β-Ga_2O_3: A Promising Wide-Bandgap Semiconductor

Nowadays, β-Ga_2O_3 has been considered as the next generation power electronic semiconductor material. Some of the reasons why are is that: it has a wide bandgap of 4.8 eV, higher than other well-known systems like GaN with direct Bandgap of 3.4

eV, and Silicon Carbide (SiC) with indirect bandgap of 3.2 eV. Its Potential low cost substrate. It has Baliga's [41] figure of merit as high as 3444.

Generally, the oxide/Semiconductor interface trap density could be determined by utilizing many electrical characterization methods, such as Terman method, Hi/Low frequency (f) method and AC conductance method [42, 43]. However, some basic limitations exist when applying those methods to β-Ga_2O_3 with the above mentioned 4.8 eV bandgap. For instance, wrong estimation of the doping concentration and oxide capacitance in addition to the negligence of deep energy level traps lead to underestimation of D_{it} by comparing the ideal C-V curve with high f C-V curve. Hi/Low f method leads to significantly underestimated D_{it} also since it takes an extremely long time to generate holes in n-Ga_2O_3 so that low f criteria is not satisfied. AC conductance method can only detect shallow energy level (0.2-0.6 eV) D_{it} due to the limited f to detect the traps deeply inside the bandgap. Furthermore, the Ga_2O_3 trap capture cross-section σ is still undetermined yet, which makes the trap energy level in the bandgap less accurate. In this experiment, the photo-assisted C-V has a light source of deep UV light with wavelength of 300 nm takes advantage of the illumination to generate electron-hole pairs in the wide bandgap materials, ensuring that all the traps in the bandgap can respond during the measurement [44, 45]. By comparing the dark high f C-V curve with the post-UV C-V curve, an overall average D_{it} can be obtained from the voltage shift of the two capacitance curves.

In the following sections; we first introduce the significance of sample preparation for β-Ga_2O_3 to provide a guidance for future device development. Then, a comparative study of the interface properties of standard commercial surfaces Al_2O_3/β-(-201)Ga_2O_3 and Al_2O_3/β-(010)Ga_2O_3 is given and compared through frequency dependent and photo-assisted C-V measurements where both surfaces have been undergone the same treatments (piranha and PDA).

2.4.1 β-Ga_2O_3 Surface Treatment and Preparation

The device fabrication process starts with Acetone, Methanol and IPA cleaning of the as received 2 inch Sn-doped samples for 30 mins to remove oils and organic residues and any other surface contamination. Before loading into ALD chamber, an important step involves a pretreatment with piranha solution (98% H_2SO_4:30% H_2O_2=3:1) was used to further extract organic residues and smooth the surface. The piranha pretreatment is found to be useful in smoothing the sample surface and removing organic contamination, such as carbon [46]. Then 15 nm of Al_2O_3 was deposited with ASM F-120 ALD reactor using TMA and H_2O as precursors at 250 ^oC. Optimized post deposition annealing (PDA) is applied to further improve the interface quality. The effect and improvement sought by piranha pretreatment and PDA is discussed in details next in section **??**. Finally, serial MOS capacitors (MOSCAPs) were fabricated with Ti/Au (30/70 nm) via lift-off process. Fabrication process and schematic illustration of the fabricated capacitors are summarized in Fig. 2.6. After piranha pretreatment, the surface root mean square (RMS) roughness is measured using Atomic Force microscopy (AFM) and found reduced from 0.26 nm without treatment to 0.17 nm after treatment as shown in Fig. 2.7

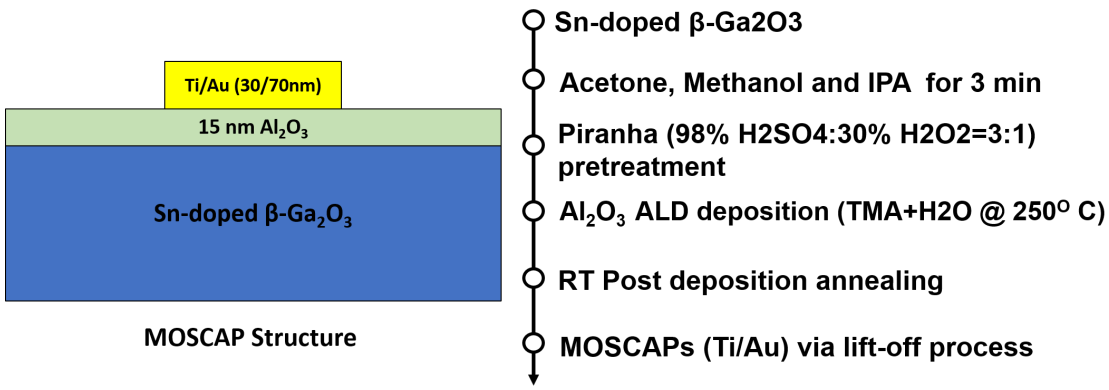

Fig. 2.6. Schematic of fabricated 15 nm Al_2O_3/ bulk β-Ga_2O_3 MOSCAP (left), and flow of fabrication process (right)

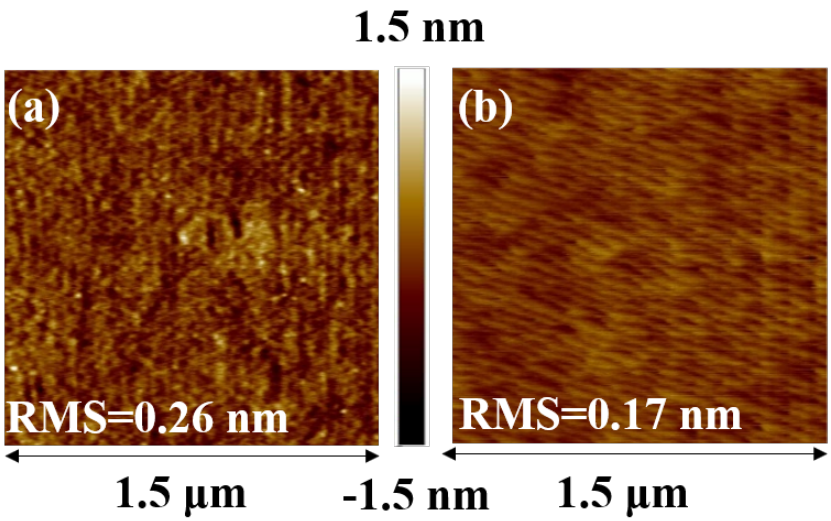

Fig. 2.7. (a) and (b) are atomic force microscopy images of β-Ga_2O_3 without and wit piranha treatment, respectively [47].

2.4.2 Comparative Interface Study of β-Ga_2O_3 Surfaces

β-Ga_2O_3 has a monoclinic crystal structure so that it has several surface oriented conducting channels as potential β-Ga_2O_3 MOSFETs. Among those surfaces, (-201) and (010) surfaces have attracted most of the attentions in the area of high power and optical electronics. High breakdown voltage of 750 V [48] and breakdown field of 3.8 MV/cm have already been achieved on the (010) oriented [49] in such an immature β-Ga_2O_3 MOSFET research. On the other hand, the oxide/ β-(-201)Ga_2O_3 reveals that the interface trap density can be as low as 10^{11}-10^{12} $cm^{-2}eV^{-1}$ as reported by Zeng in [50]. Unlike GaN HEMT and MOSHEMT with buried channels, β-Ga_2O_3 can only form surface channel depletion-mode MOSFET so far. Therefore, the insulator/ β-Ga_2O_3 interface property plays a determining role in terms of achieving high performance MOSFET. Overall, high-k dielectric constant, high conduction band offset, and high oxide/β-Ga_2O_3 interface quality are major concerns in terms of obtaining high performance on-state and off-state behaviors. Commercial standard

(-201) and (010) oriented β-Ga_2O_3 substrates are used as the representative samples for the insulator/β-Ga_2O_3 interface study.

2.4.3 C-V Measurements on Al_2O_3/β-Ga_2O_3 MOSCAP

Going through a similar measurments as in section **??**, a high precision HP4284 LCR meter was used again for the capacitance measurements. The fabricated MOSCAPs were shown in Fig. 2.8(c), and the doping concentration (N_d) of the β-(-201)Ga_2O_3 is found to be 2.7 $\times 10^{18}$ cm^{-3}, and 5.8 $\times 10^{18}$ cm^{-3} for β-(010)Ga_2O_3.

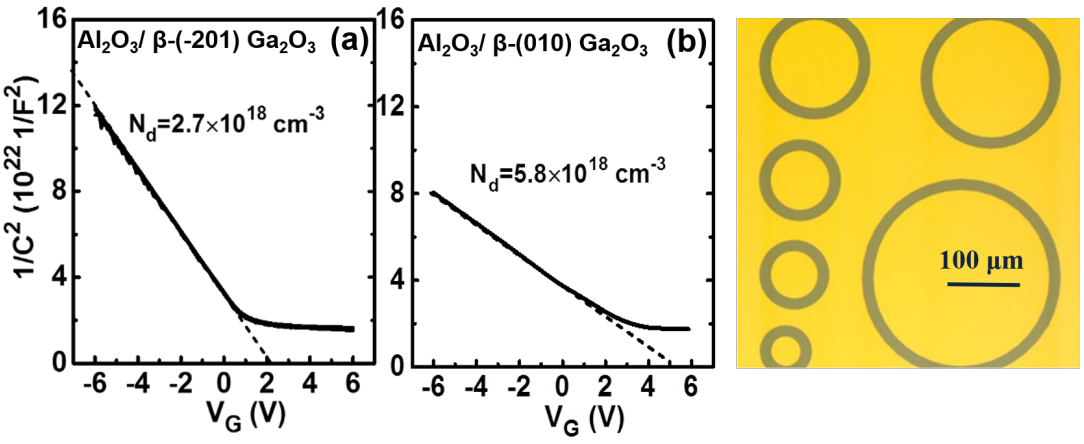

Fig. 2.8. characteristic as a function of V_G for (a) Al_2O_3/β-(-201)Ga_2O_3 and (b) Al_2O_3/β-(010)Ga_2O_3, and (c) is the top microscopic view of Al_2O_3/ β-Ga_2O_3 MOS serial capacitors.

Fig.2.9 shows the f-dependent C-V comparisons between two samples. The accumulation capacitance difference is due to different optimized annealing conditions. The significant frequency dispersion reduction of Al_2O_3/β-(-201)Ga_2O_3 reveals a higher quality interface and lower border traps compared with Al_2O_3/β-(010)Ga_2O_3 interface. Fig.2.10 further confirms the higher quality Al_2O_3/β-(-201)Ga_2O_3 interface through the bi-directional hysteresis C-V measurements. The hysteresis measurements start from depletion to accumulation and then sweeping back to depletion.

The existence of the interface and bulk traps leads to a shift of the flat-band voltage or voltage hysteresis (ΔV) due to the trapping and de-trapping at the bi-directional sweeps. The trapped electrons or detectable interface trap quantity (Q_{it}) can be estimated by this equation:

$$Q_{it} = C_{ox} \times \frac{\Delta V}{q} \tag{2.3}$$

Where C_{ox} is the oxide capacitance (C_{ox}=0.42μF/cm^2 for β-(-201)Ga_2O_3 and 0.4μF/cm^2 for β-(010)Ga_2O_3), and ΔV is the voltage hysteresis

A low hysteresis of 0.1 V is achieved for the Al_2O_3/β-(-201)Ga_2O_3 MOSCAP, which translates to an interface trap numbers of $\approx 3\times10^{11}$ cm^{-2}, and 3.7×10^{12} cm^{-2} for the other one with ΔV=1.5 V as seen in Fig.2.10.

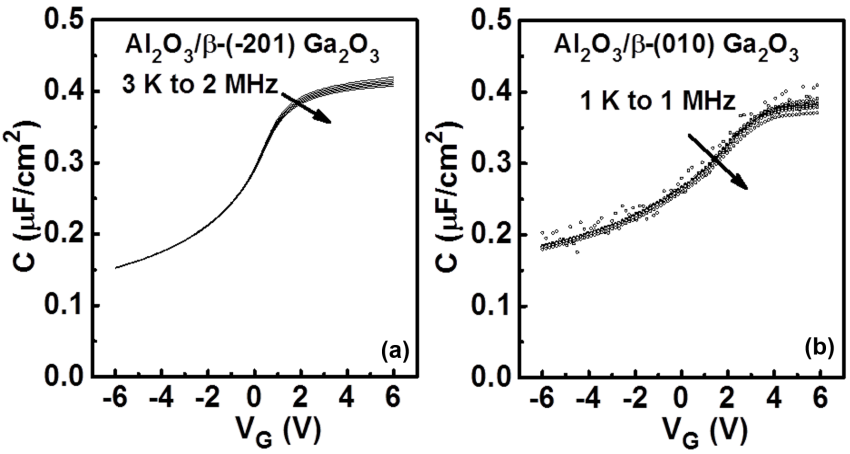

Fig. 2.9. f-dependent C-V measurements of (a) Al_2O_3/β-(-201)Ga_2O_3 and (b) Al_2O_3/β-(010)Ga_2O_3.

2.4.4 Photo-Assisted C-V on Al_2O_3/β-Ga_2O_3 MOSCAP

Due to the wide bandgap of β-Ga_2O_3, photo-assisted C-V measurements is performed to extract the average D_{it}. The measurements begins with V_G biased at

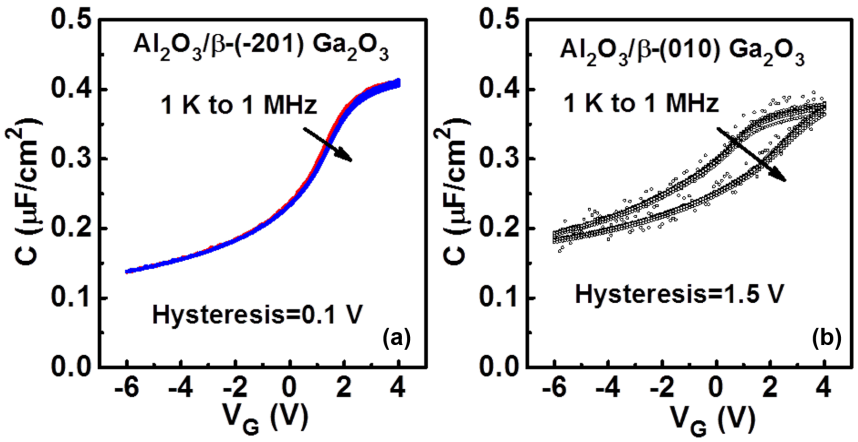

Fig. 2.10. Bi-directional C-V measurement of Al_2O_3/β-(-201)Ga_2O_3 with hysteresis of 0.1 V (Left), and Al_2O_3/β-(010)Ga_2O_3 with hysteresis of 1.5 V (Right).

accumulation ans applying short stress of 10 s to insure all traps are filled with electrons, then sweeping gate voltage down from depletion to accumulation at high freq. of 1 MHz and under dark conditions and considered as "ideal" C-V curve. Then, V_G is kept at deep depletion while UV light is being illuminated on the sample for 10 minutes, this time is optimized and chosen to generated as much electron-hole pairs as possible, and also forcing generated holes to move up to the Al_2O_3/β-Ga_2O_3 interface. After that the UV light is turned off and then C-V is swept again from depletion to accumulation in dark, thus, this second curve is measured and compared with the "ideal" curve. During the second curve the generated holes will recombine with the trapped electrons, thus, the interface has donors-like traps compared with the interface without UV illumination in the post UV exposure sweep. Therefore, a left shift of the C-V curves is seen and flatband voltage (V_{FB}) shift is translated into average D_{it} by equation **??**.

Fig.2.11 are the photo-assisted C-V measurement results of (-201) and (010) samples.

The average D_{it} of Al_2O_3/β-(-201)Ga_2O_3 and Al_2O_3/β-(010)Ga_2O_3 interfaces are 2.3×10^{11} $cm^{-2}eV^{-1}$ and 6.7×10^{11} $cm^{-2}eV^{-1}$, respectively.

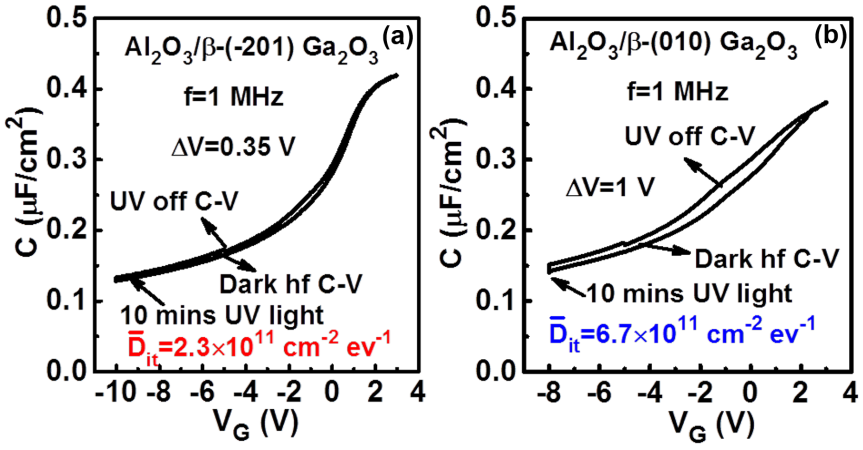

Fig. 2.11. Photo-assisted C-V measurements of (a) Al_2O_3/β-(-201)Ga_2O_3 and (b) Al_2O_3/β-(010)Ga_2O_3.

2.5 Summary

In summary, We have investigated the piranha pretreatment and PDA effects on Al_2O_3/β-Ga_2O_3 interface through frequency and temperature-dependent and photo-assisted C-V measurements. Low C-V hysteresis of 0.1 V, reduced high-temperature frequency dispersion and reduced V_{FB} shifts are benefited from the improved interface quality. Piranha pretreatment and PDA process are demonstrated to effectively improve the Al_2O_3/β-Ga_2O_3 interface, making MOS structure possible for future power electronics. we can also conclude that (-201) oriented β-Ga_2O_3 can provide a much higher quality interface with less frequency dispersion, much lower hysteresis and average D_{it}. A deep investigation of the (-201) shows that this surface is similar to (0001) hexagonal surface of wurtzite crystal or (111) surface of cubic crystal. Similar to GaAs (111)A surface with unpinned Fermi level compared with (010)

surface. We suggest that this (-201) β-Ga_2O_3 has less dangling bonds so that the Al_2O_3/β-(-201)Ga_2O_3 interface is of a higher quality compared with (010) surfaces.

3. DIRECT INTERFACE STUDIES ON WIDE-BANDGAP SEMICONDUCTORS TRANSISTORS

Metal-Oxide-Semiconductor Capacitors (MOSCAP) are the first and the simplest structure to study the interface characteristics between channel and gate insulator in emerging compound semiconductors devices, and this is widely acceptable and proven sufficient in the majority of recent technologies. However, the ultimate goal of developing such materials from electronic devices point of view is implementing them into transistors with unprecedented oxide/semiconductor interface quality, and with the need of aggressive device miniaturizing, utterly new material systems along with new fabrication and processing methods, and the substantial difference in physical interpretation between measurements on capacitors and measurements on transistors, characterization of interface properties directly on transistors could be a wiser choice for researchers. We have briefly introduced some of these characterization methods in chapter 1, and have been characterizing GaN and $Ga2O_3$ channels utilizing MOSCAP structures. In this chapter, a novel characterization methods are used, reported, or proposed to directly characterize interface properties on transistors.

3.1 GaN MOS-HEMT With MgCaO As Gate Dielectric

Recently, GaN-based high-electron-mobility-transistor (HEMT) has demonstrated its promise in high frequency [51], high power [52], and low noise [53] electronic devices and it has been eventually used in 5G telecommunication networks, the most advanced RF technology. The lattice matched InAlN/GaN HEMT structure provides a higher 2D electron density than AlGaN/GaN due to a larger bandgap offset and minimized short-channel-effects due to its thinner barrier. However, because of its several-nm-thick barrier, those devices usually suffer from high gate leakage and

interface trap issues, the device off-state performance is degraded and thereby the off-state breakdown voltage is decreased. Therefore, finding a good method to reduce the gate leakage and interface trap density is of great importance to improve the device off-state performance. In this study, we use atomic layer epitaxial MgCaO as gate dielectric successfully to fabricate sub-100 nm InAlN/GaN MOSHEMTs with significantly improved maximum drain current, current on/off ratio and low subthreshold swing.

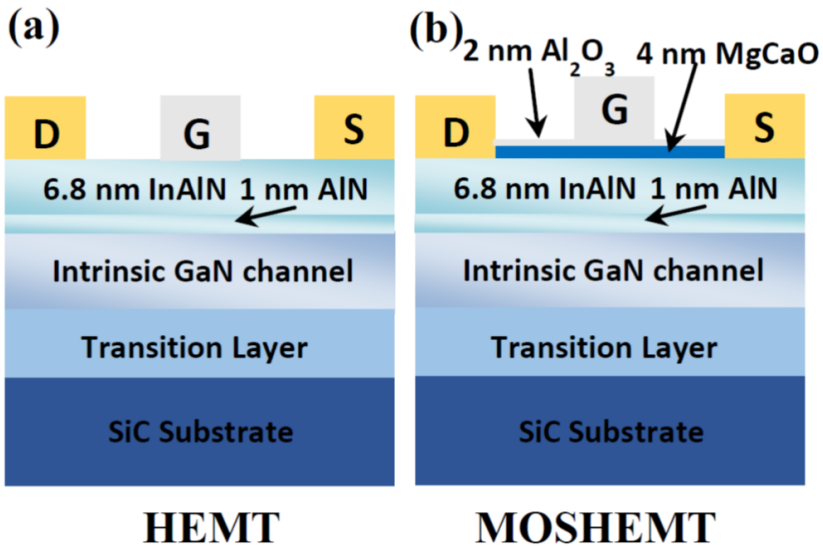

Fig. 3.1. Schematic of (a) GaN HEMT (left), (b) MOSHEMT (right)

Fig. 3.1 shows the device structures of the InAlN/GaN HEMT and MOSHEMT, respectively. Device fabrication was started with the mesa isolation by Cl_2/BCl_3 etching. The ohmic contacts were formed by depositing Ti/Al/Au (15/60/50 nm) followed by 775 ^oC rapid thermal annealing in N_2 with optimized R_c of 0.3 Ω·mm. Two splits of experiments are performed. 1) Device set A was treated by O_2/Ar plasma with 12/120 sccm at the power of 100 W for 5 minutes. These devices are used as reference to show the affect of surface passivation [54]. 2) Device set B was first deposited with 4 nm of atomic-layer epitaxial (ALE) $Mg_{0.25}Ca_{0.75}O$ (or MgCaO for simplicity), followed by 2 nm Al_2O_3 as a capping layer to avoid MgCaO absorbing

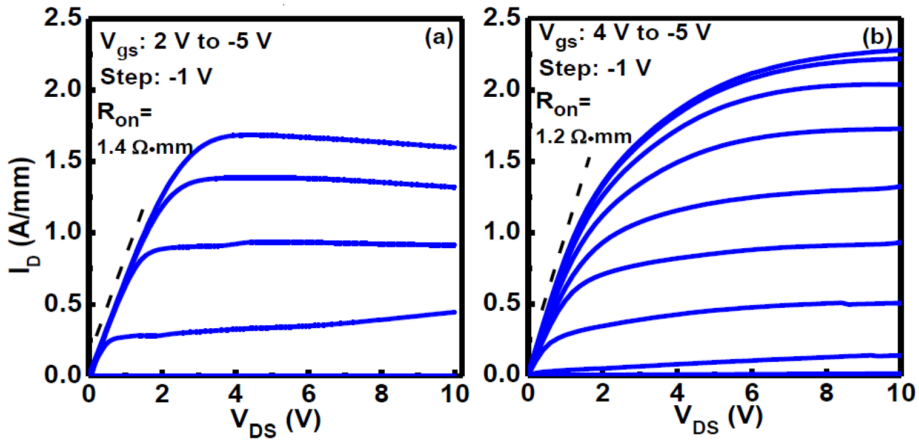

Fig. 3.2. (a) Output characteristics of GaN HEMT with an $I_{ds,max}$=1.7 A/mm, on-resistance R_{on}= 1.4 Ω·m, V_T= -1.75 V, and $g_{m,max}$= 600 mS/mm at V_{ds}= 4 V. (b) Output characteristics of a GaN MOSHEMT with ALE MgCaO as gate dielectric. This device demonstrates an $I_{ds,max}$ of 2.3 A/mm and R_{on}= 1.2 Ω·m

water in the following processes. Single crystalline MgCaO offers the right band offset and the best interface on InAlN/GaN system [36]. This is the central point of this work. Finally, the gate was formed by Ni deposition followed with a lift-off process. The devices that have L_G=85 nm and Lsd=1 μm are used as the representative in this brief introduction to GaN MOS-HEMT. All the lithography processes were carried out using a Vistec VB6 electron beam lithography system.

Fig 3.2 (a) and (b) show the DC output characteristics (I_d-V_d) of the InAlN/GaN HEMT and the InAlN/GaN MOSHEMT with ALE MgCaO as gate dielectric. Thanks to the 6 nm thick gate oxide, a high gate bias of 4 V is applied and the $I_{ds,max}$ has reached 2.3 A/mm with an on-resistance (R_{on}) of 1.2 mm. The $I_{ds,max}$ is significantly improved, compared to 1.7 A/mm for HEMT, due to the capability of further positive bias the gate voltage and dielectric passivation of source and drain regions of the InAlN surface. Despite the thicker gate to channel spacing (14 nm) compared to HEMT, MOSHEMT still exhibits a high transconductance of 465 mS/mm at V_{ds}=5 V shown in Fig. 3.3 (a). Fig. 3.3 (b) depicts the log-scale I_d-V_g curves of the

MOSHEMT and HEMT; respectively. The MOSHEMT demonstrates one of the highest on/off ratio that have been reported so far of 10^{12}.

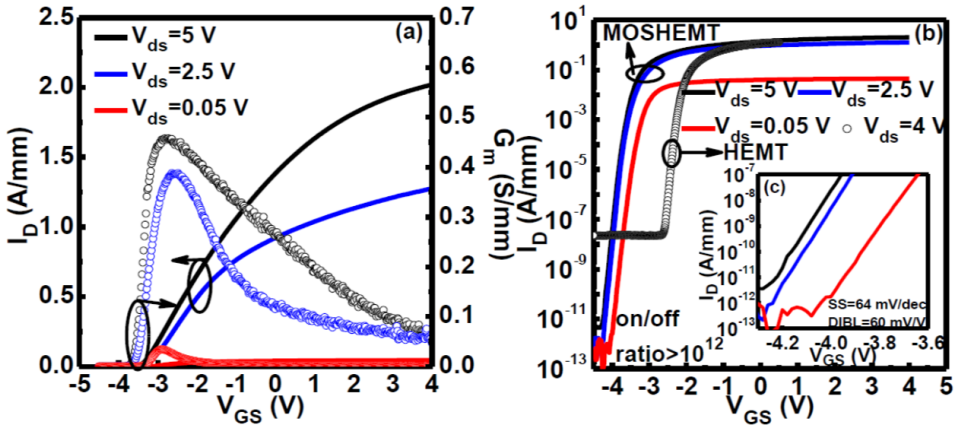

Fig. 3.3. (a) I_d-V_g transfer characteristics of MOSHEMT (b) Log-scale view of the I_d-V_g for both HEMT and MOSHEMT. A high on/off ratio higher that 10^{12} and 10^8 are obtained for MOSHEMT and HEMT, respectively. (c) as the inset in shows the zoom-in view of I_d-V_g (for MOSHEMT) in the subthreshold region. SS of 64 mV/dec is observed with a small DIBL=60 mV/V

The higher on/off ratio of the MOSHEMT (compared to HEMT of 10^8) is from the much lower gate leakage current exhibited by the MOSHEMT. Thanks to the stable process, more than 80% of measured devices on the same chip show an on/off ratio of 10^{10} ~10^{12} with L_G from 250 to 80 nm. Fig. 3.3(c) describes the zoom-in image of the I_d-V_g of the MOSHEMT in the subthreshold region. The SS of the V_{ds}= 0.05 V, V_{ds}= 2.5 V, V_{ds}=5 V are quite similar with small value of 64 mV/dec. This low SS indicates the good interface quality between the ALE MgCaO and InAlN barrier. It suggests that the lattice matched epitaxial MgCaO on the InAlN barrier has a direct impact on a good on-state and off-state device performances. In conclusion, high performance sub-100 nm gate length InAlN/GaN MOSHEMTs are demonstrated using lattice matched ALE MgCaO as gate dielectric. The representative MOSHEMT has an $I_{ds,max}$ of 2.3 A/mm, R_{on} of 1.2 mm, SS of 64 mV/dec, and a high on/off ratio of 10^{12}. ALD MgCaO shows the promise for GaN MOS technology.

3.1.1 Interface Trap Density using Pulsed IV

For this measurements, and referring to chapter 1, the pulse width and period are 500 μs and 100 ms, respectively. The pulsed I_d-Vgs measurements was conducted on a device with L_{ch}= 140 nm. The quiescent bias points are set as (V_{GSQ},V_{DSQ})= (5,0) and (5, 8) for gate and drain pulse, respectively, and shown in Fig. 3.4.

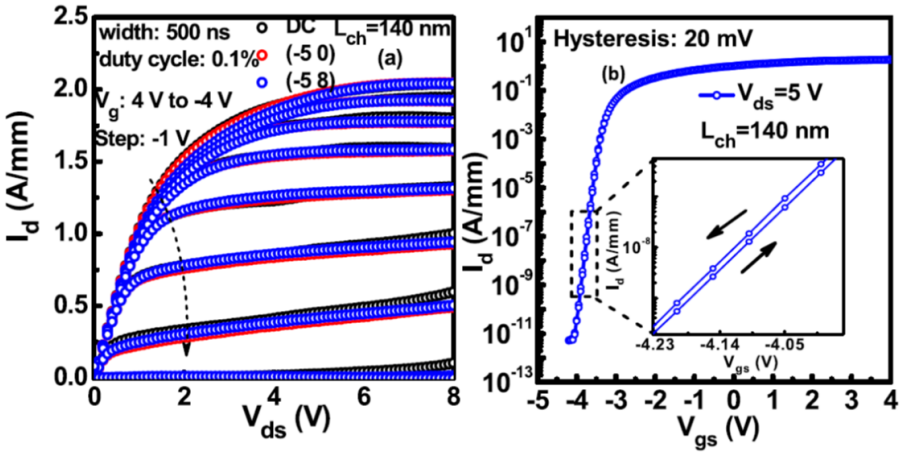

Fig. 3.4. (a) Pulsed I-V measurements with 500 ns pulse width and 0.1% duty cycle and (b) I_d-V_{gs} hysteresis of a MOSHEMT with L_{ch} = 140 nm [40]

Effective suppression of the current collapse by MgCaO is demonstrated with little difference between the DC, and gate and drain pulsed drain currents. Fig. 3.4(b) is the I_d-V_{gs} hysteresis measurement of the same device. A negligible hysteresis of 20 mV is observed when V_g is swept from V_g= 4.5 to 4 V and then sweeping back, which further confirms an ultra-high quality interface between MgCaO and InAlN barrier. From a hysteresis like this a Q_{it} levels in the range $10^{11} \sim 10^{12}$ are estimated using the above equation for this MgCaO/InAlN/GaN MOS-HEMT.

3.1.2 Interface Trap Density using SPCP

In this part of the thesis, we reported on the single pulse charge pumping (SPCP) measurements as a method to extract the interface trap density (N_{it}) in the AlGaN/GaN metal-oxide-semiconductor high-electron mobility transistors (MOS-HEMT) with epitaxy gate dielectric $Mg_{0.25}Ca_{0.75}O$ (MgCaO). The electron capture and emission processes are monitored in time domain and studied during the rise and the fall edges of a single gate voltage pulse. The signature charge pumping current peaks are observed enabling a direct extraction of N_{it} as low as 2×10^{11} cm^{-2} with gate voltage sweeping from off-state to on-state. SPCP realizes a direct N_{it} measurement on transistors and confirms the high quality of interface between the single crystalline epitaxy MgCaO and GaN interface. SPCP is verified as a fast and reliable interface characterization method on III-V HEMTs (MOS-HEMT) devices, or other devices that do not exhibit body contacts as the conventional Si transistors needed for the conventional charge pumping measurements.

Based on our previous discussion that an epitaxy single crystalline MgCaO insulator, which is lattice matched to GaN, would achieve a very high quality interface and subsequently low interface trap density (D_{it} with a dimension of $cm^{-2}\cdot eV^{-1}$ or N_{it} with a dimension of cm^{-2}) on top of GaN heterostructures [36,40,55]. However, these low D_{it} were generally measured using C-V and conductance methods and mostly on bulk GaN MOS capacitors and not directly on the transistors, and because the conventional methods including Terman method, AC conductance, charge pumping (CP) methods [22, 28, 43] require an adequate body contact. However, the state-of-the-art GaN transistors has a 2-dimentional electron gas (2DEG) on insulating substrate, similar to Si ultra-thin-body (UTB) devices with floating body channels. Also, the subthreshold method using the subthreshold swing is just an estimation of average D_{it} in the sub-threshold region. Thus, an interface trap density extraction method with high accuracy and direct measurements on GaN HEMTs is highly demanded and this methodology can also extended to other emerging device research such as gate-all-

around nanowire transistors and ultra-thin-body transistors based on 2D materials, where the channels are floated [56].

Single pulse charge pumping method provides a real time monitoring of the capture and emission process of electrons with the interface traps, enabling us to investigate the interaction between electrons and interface defects and consequently obtain an accurate extraction of the interface trap density [31]. In the SPCP measurements, the signature characteristic in the charge pumping current peaks is used for a direct extraction of N_{it}. In this work, for the first time, we apply the SPCP approach to quantitatively study the N_{it} on MgCaO/AlGaN/GaN MOS-HEMTs on SiC substrate. N_{it} is determined to be as low as 2×10^{11} cm^{-2} with gate voltage sweeping from off-state to on-state and a significant N_{it} reduction comparing to GaN MOS-HEMT with Al_2O_3 as gate dielectrics. This conclusion is consistent to our previous discussion using MOS capacitors by conductance method and UV-assisted C-V measurements.

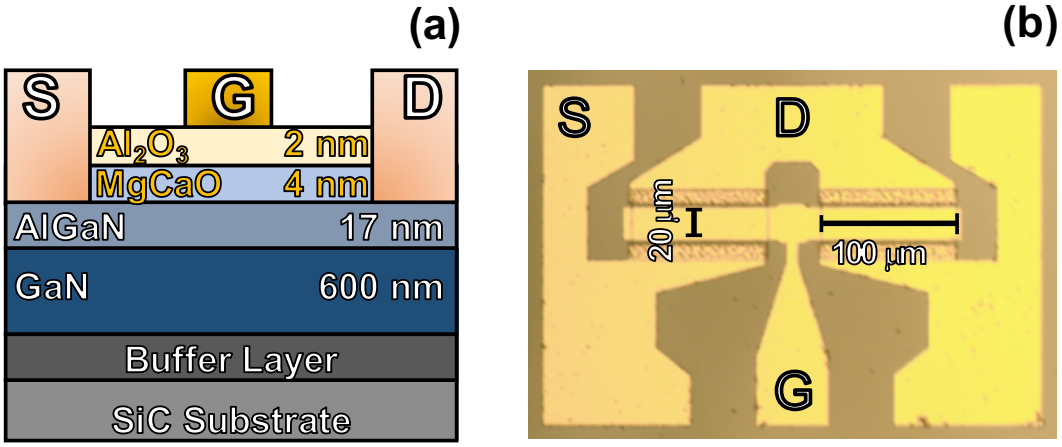

Fig. 3.5. (a) Schematic of the AlGaN/GaN MOS-HEMT. (b) Microscope image of a fabricated device.

Fig. 3.5(a) shows a cross-sectional schematic view of an AlGaN/GaN MOS-HEMT and Fig. 3.5(b) shows a microscopic image of two fabricated devices with 20 μm channel length and 100 μm width each. The detailed fabrication process of the experimental devices is described in section 3.1. An important fact is that epitaxy Mg-

CaO, grown by ALD, is lattice-matched on GaN material system and offers unprecedented high-quality interface for the device. Keysight B1500A Semiconductor Device Analyzer, Keysight B1530A waveform generator/fast measurements unit (WGFMU) along with remote-sense and switch unit (RSU), and high precision Agilent E4980A LCR meter were used for DC, SPCP, and C-V measurements, respectively, and all measurements are done at room temperature in a N_2 environment. Fast I-V measurements were carried out using the shortest cabling possible to minimize parasitic effects taking into consideration a 50 Ω impedance that matches the pulse generator source to avoid any desirable signal reflection. The floating system's time delay was found to be less than 5 ns, less than the B1530A's minimum effective current sampling interval of 10 ns.

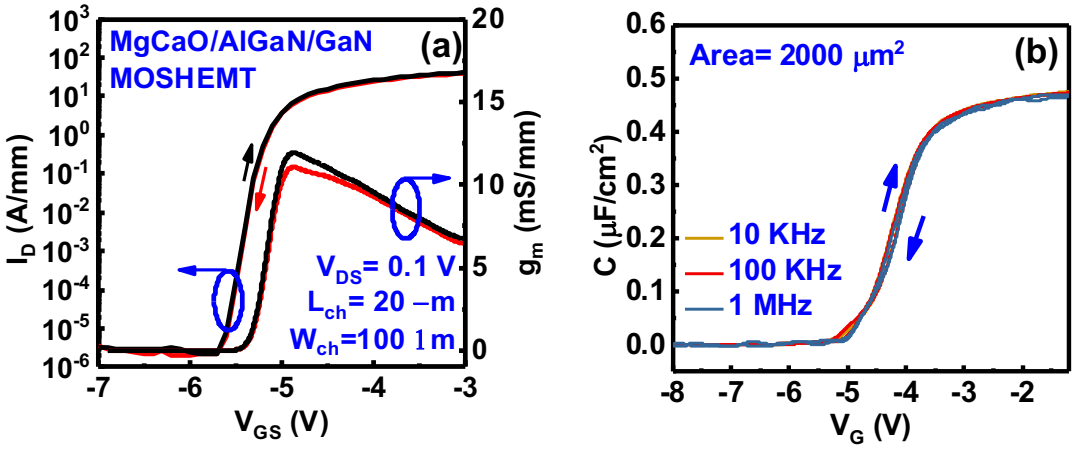

Fig. 3.6. (a) I_D-V_{GS} characteristics and transconductance (g_m) of a representative AlGaN/GaN MOS-HEMT. (b) C-V characteristics of the same device at different frequencies.

Fig. 3.6(a) shows the I-V characteristics with drain to source voltage (V_{DS}) of 100 mV. A threshold voltage (V_{th}) of -5 V is extracted by linear extrapolation method at low V_{DS}. Fig. 3.6(b) shows the C-V measurements of the same device with source and drain connected as one terminal and gate being the other terminal. The near hysteresis-free transfer characteristic and C-V curves in different frequencies achieved

in our MgCaO GaN MOS-HEMT suggest a high-quality interface. The I-V transfer characteristic indicates a high drain current and high on-off ratio, which turned out to be important factors in detecting the charged pumping current considering that the substrate current is not included in this method. The threshold voltage difference in I-V and C-V are due to the stress induced V_{th} shift.

The test circuit of SPCP measurement is depicted in Fig. 3.7(a). SPCP measurements begin by an application of a sufficiently high gate voltage pulse (V_G) to switch the channel from depletion to accumulation. During the rising edge of the pulse, electrons from source to drain are pumped into the conduction band of the channel and also captured by interface states during capture process, while the emission of electrons back to source takes place during the falling edge as described in the bandgap process illustration in Fig. 3.7(b), where E_c is the conduction band, E_v is the valence band, and S/D stands for source/Drain contacts. The process in which SPCP measurements takes place within the band structure is explained previously in chapter 1. In regards to this GaN MOS-HEMT however, the electrons filled traps in the interface states are considered slow traps because they are located deeply in the bandgap and require long time in off-state to emit electrons and get detrapped (conceivably in seconds) while the slowest measurements time in this study is 1 ms. As a result, during the falling edge, only the accumulation electrons in the conduction band is fast enough to respond and go back to the source. The difference between the rise current and fall current is the charge pumping current of Q_{it}, originated from the charge trapping process, where the Q_{it} is qN_{it} and q is the elementary charge. The accumulation electron charge is defined as Q_{acc} and the total charge of trapped electrons is defined as Q_{it}. Note that the charge pumping current response is a superposition of traps responses from dielectric/AlGaN interface, AlGaN/GaN interface and also bulk traps in dielectrics/AlGaN/GaN. Therefore, the Nit measured in this work is an effective 2-dimensional trap density considering all these trap origins.

The integration of the charge pumping current during rise time ($I_{cp,RISE}$) is the total charge including Q_{acc} and Q_{it}, as shown in eq. 3.1. The integration of the charge

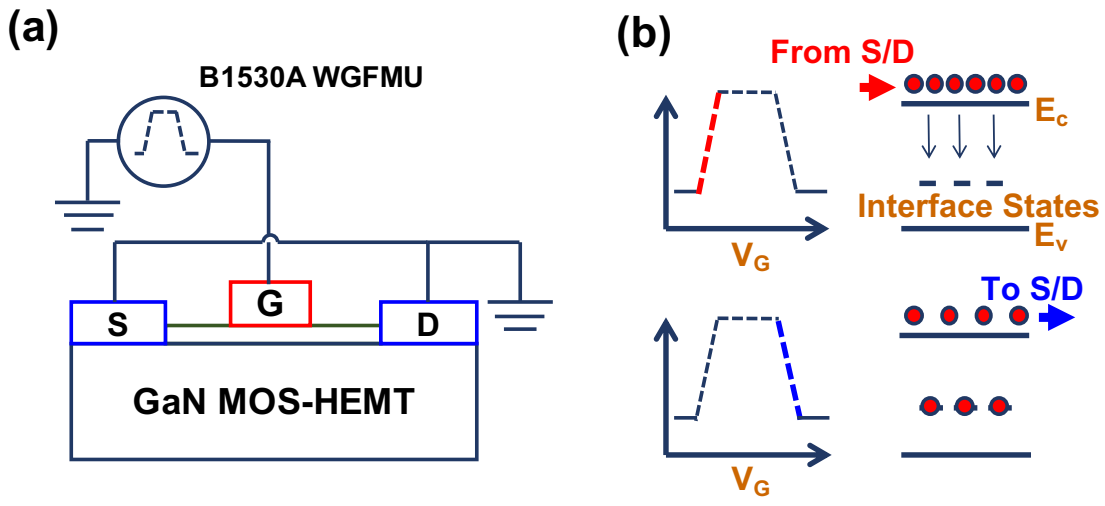

Fig. 3.7. (a) Schematic diagram of SPCP experimental setup. (b) Sequence of capture and emission process within the band structure of the device channel for the SPCP measurements.

pumping current during fall time ($I_{cp,FALL}$) is the total charge of Q_{acc} only, as shown in eq.3.2.

$$Q_{acc} + Q_{it} = \int I_{cp,RISE} dt \tag{3.1}$$

$$Q_{acc} = \int I_{cp,FALL} dt \tag{3.2}$$

The rise time (t_{RISE}) and fall time (t_{FALL}) of the pulse as well as pulse width interval (t_{INT}) are varied, and the response of charge pumping current, I_{cp}, is then monitored. Sharp current peaks during capture process and broad tails during emission were observed. These two signature behaviors in I_{cp} are attributed to the interface traps [31, 32, 56–60], which is utilized in SPCP to estimate the Nit of AlGaN/GaN MOS-HEMT.

Fig. 3.8 shows the transient electron current due to the depicted gate voltage pulse for $t_{RISE} = t_{FALL} = 100$ μs. V_{ON} is gate pulse voltage that accumulates electrons and turns on the transistor while V_{BASE} is the off-state voltage of this device. D_{it} levels in the range of $10^{11} \sim 10^{12}$ cm^{-2}·eV^{-1} was found previously in this chapter

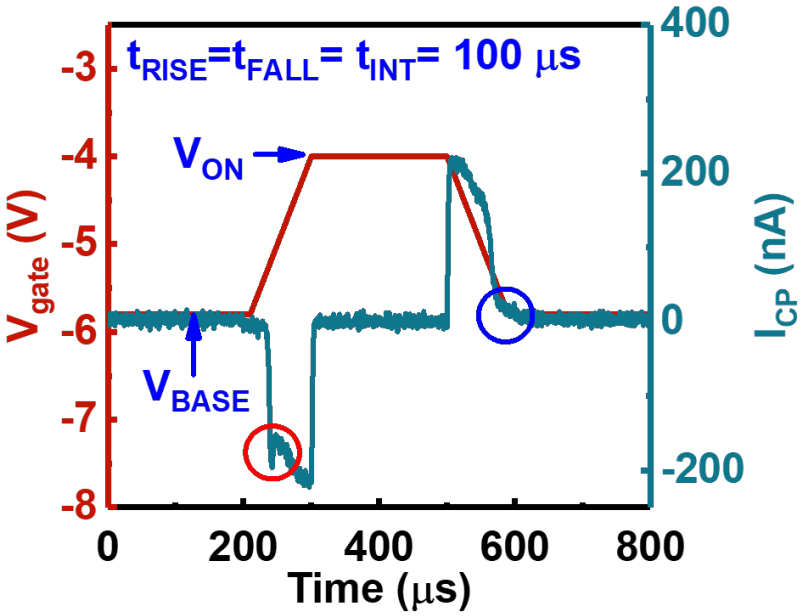

Fig. 3.8. An illustration of the applied gate pulse with the resulting charge pumping current I_{cp} as a function of time. Electron capture and emission behaviors are observed in red and blue circles, respectivley

using the well-established conductance method on MgCaO/GaN MOS capacitors. To the uniqueness of this SPCP method, similar level of Nit is achieved in this work with major difference that it was directly measured on MOS-HEMTs devices and significantly faster measurement turnaround time. The electron capture and emission processes to and from interface states are examined with various characteristic ramping times (t_R) of the gate pulse where $t_R = t_{RISE} = t_{FALL}$, and various t_R from 1 μs to 1 ms showed similar charge pumping features. In this measurements t_{INT} is always chosen as $2t_R$ to ensure a full recovery of charged traps between both edges. Fig. 3.9(a) shows the microscopic response of I_{cp} for when V_{BASE} is being changed as off-state volatge for each pulse with a maximum pulse height of -1 V, while Fig. 3.9(b) shows the response of I_{cp} with multiple pulse heights, or V_{ON} and fixed V_{BASE}. Sweeping gate voltage from depletion to accumulation effectively changes the surface

potential at the interface, thus, different trap energy levels (E_t) are accessed in this way. The only difference between the two measurements techniques is whether the pulse base is low enough to detrap all available surface or bulk traps before deciding that the resulting current is actually an accurate representative of the total effective traps density. From Fig. 3.9(a) no N_{it} peaks when V_G is swept near or above V_{th}, except when sweeping from -6 V, thus, in order to see the traps charging current peaks, V_{BASE} must be less than V_{th} at around -6 V. From this V_{BASE}, we can step up the pulse peak and monitor the charge pumping current response, which is utilized to estimate trap density Q_{it}.

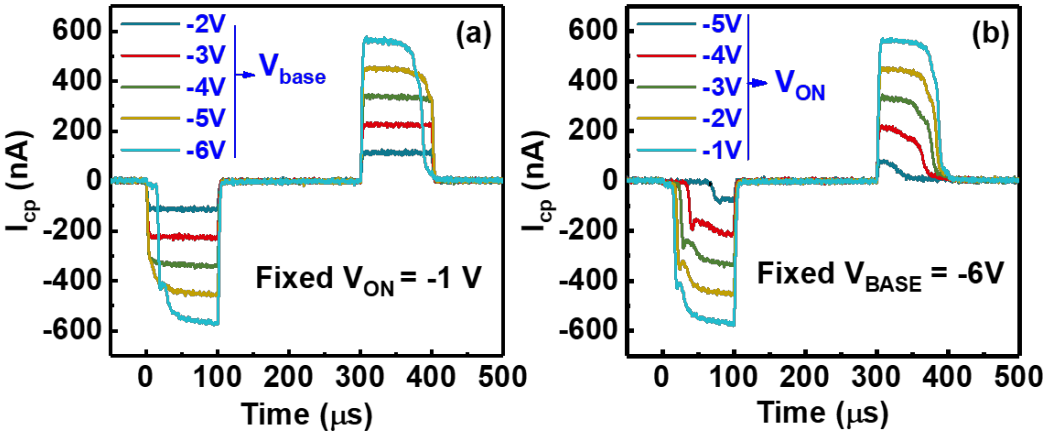

Fig. 3.9. Measured I_{cp} vs time for (a) multiple V_{BASE} levels with pulse maximum V_{ON} held at -1 V and (b) multiple gate voltages V_{ON} with V_{BASE} being fixed. Both rise and fall edges are shown as measured directly by SPCP.

Q_{it} can be calculated according to equations (3.1) and (3.2) and by subtracting the impact of Q_{acc}. Eq. (3.3) is then used to calculate Q_{it}. In details, Q_{it} is extracted by the curves of the two charge pumping currents as follows; the rise edge current is flipped vertically, fall edge current is flipped horizontally, and then both are superimposed in order to determine charge difference as the interface charge Q_{it} from the

extra peaked area under the superimposed curves. This is illustrated in Fig. 3.10(a) for different V_{ON} where The current peaks of interest in Fig. 3.9(b) are highlighted.

$$Q_{it} = \int (I_{cp,RISE} - I_{cp,FALL})dt \tag{3.3}$$

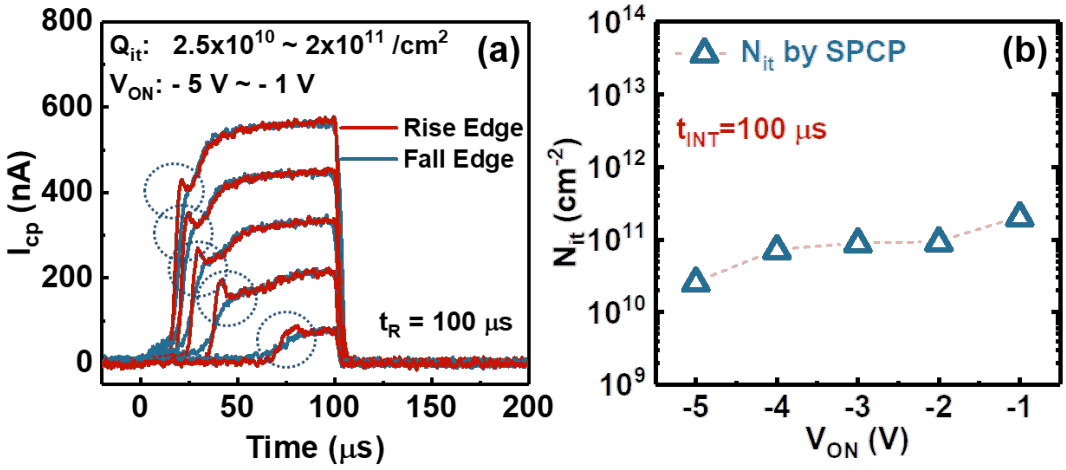

Fig. 3.10. (a) Measured I_{cp} as a function of time at different V_{ON}. V_{BASE} is fixed at -6 V. The current differences are compared for the purpose of Q_{it} estimation in (b).

A repeated measurement on the same device measured above was conducted but within two days from each other, and compared in Fig. 3.11. The charge pumping current responses almost overlap for the two subsequent measurements, as shown in Fig. 3.11(a). And the extracted Nit value from these two measurements are very similar, as shown in Fig. 3.11(b). Therefore, the single pulse charge pumping measurements are repeatable and reliable method for interface traps estimation.

The key advantage of this SPCP method is the real-time monitoring of the capture and emission process of carriers by traps. DC and small signal measurements usually takes longer characteristic time (millisecond if not seconds), which maybe long enough time for traps to emit their electrons before taking part in any traps measurements, therefore, SPCP is very sensitive to detecting and distinguishing both capture and

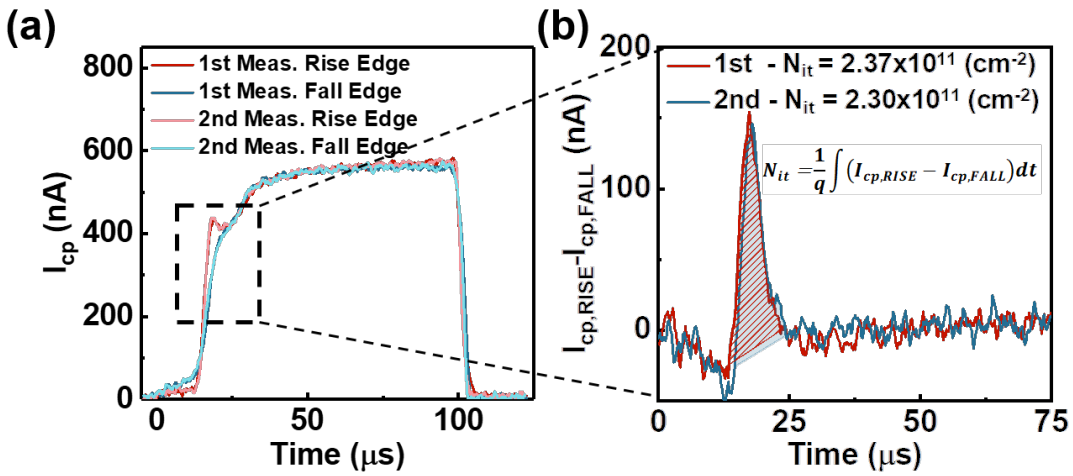

Fig. 3.11. Comparison of two subsequent measurements by single pulse charge pumping. (a) I_{cp} versus time. (b) Nit extracted for each run.

emission processes. The Variation of rise time would be directly linked to charging interface states and finding interface traps density in the process [32]. The shorter the rise time t_{RISE} (faster ramping) the higher I_{cp} current and peak position (peak voltage value within the pulse range with respect to time) [32,58] as understood from the following equation:

$$I_{cp} = \frac{\partial Q}{\partial t} = C\frac{\partial (V_G)}{\partial t} \tag{3.4}$$

Where C is the capacitance. The fast response of free electrons, especially the ones near the conduction band, is reflected as higher interface traps are detected for shorter t_{RISE}. This is seen in the next experimental measurements. Rise (and fall) time was changed from 1 μs to 1 ms. For 6 devices measured, Fig. 3.12 shows that the Nit levels are still within the range of $10^{11} \sim 10^{12}$ but with slight increase towards shorter rise times, as expected.

In this type of MOS-HEMT, however, it is worth mentioning that there are two interfaces where band bending is taking place, one is the dielectric/AlGaN interface, the other is the AlGaN/GaN interface. While all studies in this chapter confirm that this novel gate dielectric of MgCaO helped improve the quality of the dielectric/AlGaN

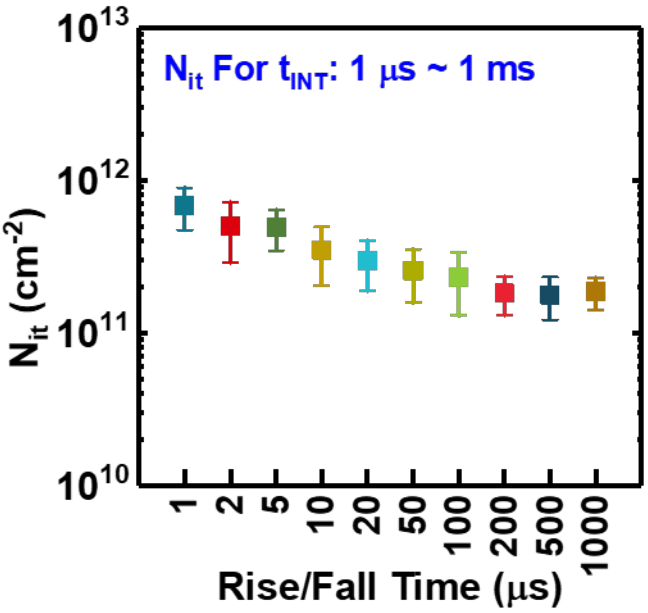

Fig. 3.12. Nit extracted from charge pumping current of 4-6 devices with various rise times.

interface, a justified question may arise which is which of the two interfaces is being studied here in this SPCP measurements, and whether MgCaO could affect the AlGaN/GaN interface?

Although that the gate voltage used for measurements corresponds to the formation of the 2DEG, one may think that the carriers activity is taking place only at the 2DEG interface, while in fact, the active traps in the MOS-HEMT structure used in this work are originated from the four different regions, namely:

- AlGaN/GaN interface
- Dielectric/AlGaN interface
- Bulk trap in AlGaN and GaN
- Bulk trap in dielectric

In, the single pulse charge pumping method proposed in this work, the charge pumping current signal and trap response is affected by both bulk traps and interface traps. Therefore, the interface trap density measured in this work is an effective normalized 2D trap density, considering both bulk trap and interface trap and that is the reason why Nit in cm^{-2} is extracted and not D_{it} in $cm^{-2}{\cdot}eV^{-1}$.

To understand which origin is dominating, we have two experimental evidences. The experimental results indicate that the dielectric/AlGaN interface will have a significant contribution to the single pulse charge pumping current response.

The first experiment is the conductance method measurements on both GaN MOS-HEMT with Al_2O_3 as gate dielectrics and MgCaO as gate dielectrics. Analogous to the early discussion in this chapter (section 2.3.1 specifically), a repeated AC conductance shown in Fig. 3.13 and its inset show the G_p/ω versus frequency, where a significant difference is pronounced in conductance peaks between the two. The extracted D_{it} levels are also very different on GaN MOS-HEMT with Al_2O_3 as gate dielectrics versus MgCaO as gate dielectrics. This data suggests the dielectric/AlGaN interface can play an important and extended role in terms of traps density and traps response through all four regions mentioned above.

The second experiment is a single pulse charge pumping measurement on both GaN MOS-HEMT with Al_2O_3 as gate dielectrics and MgCaO as gate dielectrics, as shown in Fig. 3.14. The signature charge pumping current peaks is significantly higher in Al_2O_3 than that in MgCaO which directly mean higher traps are being charged in Al_2O_3 MOS-HEMT as opposed to MgCaO. To quantify these results, extracted 2D trap density (Nit with a dimension of cm^{-2}) of GaN MOS-HEMT with Al_2O_3 as gate dielectrics is compared with those extracted for MgCaO and are found to be significantly higher, as in Fig. 3.15. Thus, the dielectric/AlGaN interface must have a direct and important contribution to the single pulse charge pumping current response and the overall traps estimation suggesting a high quality MgCaO/AlGaN interface.

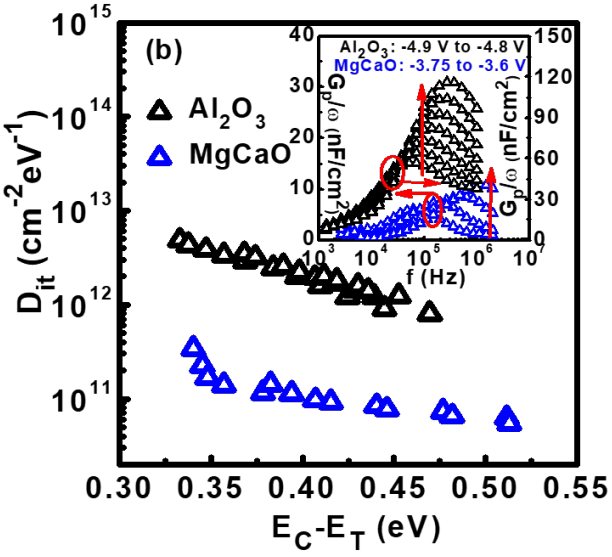

Fig. 3.13. D_{it} distribution extracted from conductance method on GaN MOS-HEMT with Al_2O_3 as gate dielectric and MgCaO as gate dielectric.

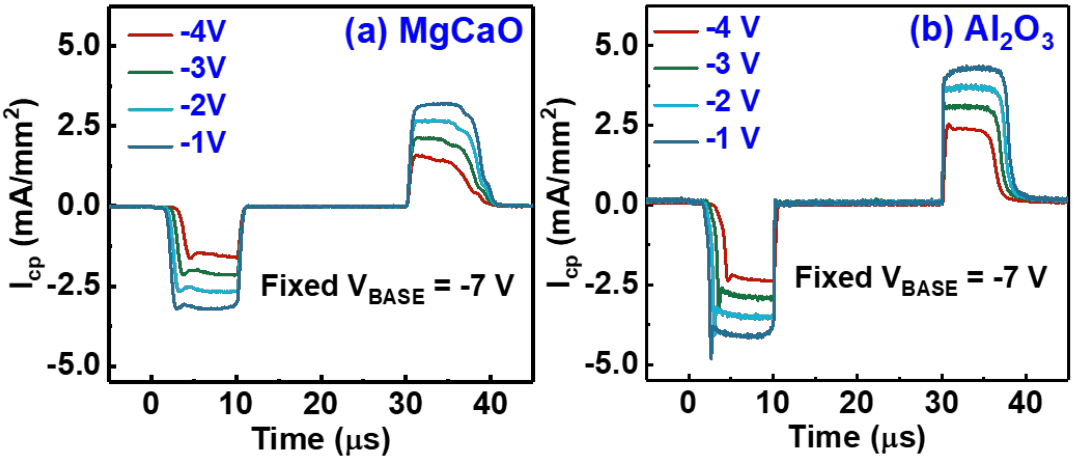

Fig. 3.14. Measured I_{cp} vs time for multiple gate voltages V_{ON} for (a) MgCaO as gate dielectric and (b) Al_2O_3 as gate dielectric.

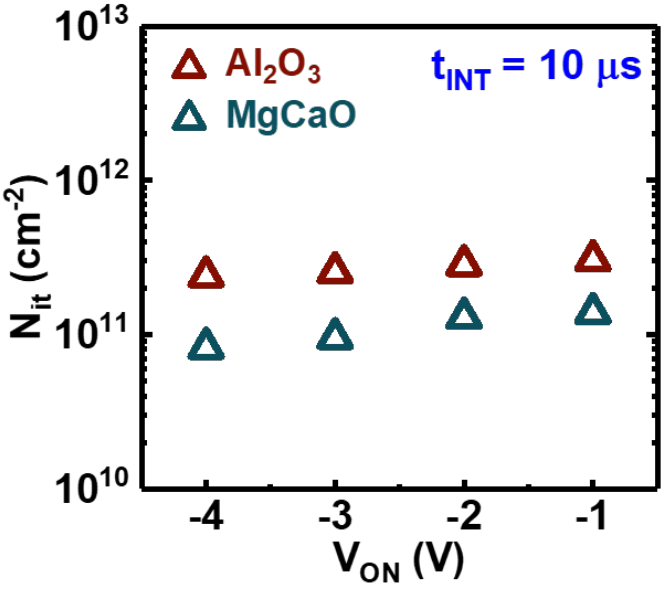

Fig. 3.15. Comparison of Nit versus V_{ON} using SPCP method on GaN MOS-HEMT with MgCaO as gate dielectrics and Al_2O_3 as gate dielectrics.

Considering the above experimental evidence and the fact that AlGaN/GaN interface usually has a low interface trap density, we believe that although the single pulse charge pumping measurement captures the traps response mutually from both interfaces, the dielectric/AlGaN interface can contribute significantly.

In summary, we reported on the use of the single pulse charge pumping measurements as a reliable method to directly monitor the capture and emission processes of the channel electrons and its interaction with interface traps. As an accurate and fast technique to estimate Nit of the novel AlGaN/GaN MOS-HEMT, SPCP shows how electrons are captured by the interface states during the rising edge of the gate pulse and how it gets emitted in a slower way during the falling edge of the same pulse. Nit extracted via SPCP technique is significantly low down to 2×10^{11} cm^{-2}, suggesting a high-quality interface of epitaxy MgCaO on GaN devices. SPCP is suggested as a

promising technique for direct N_{it} estimation for state-of-the-art devices with floating body channels.

3.1.3 Ultraviolet Light-Based I-V Method for Interface Traps Extraction in β-Ga_2O_3 FETs

As done with GaN MOS-HEMTs and characterized with SPCP method, this section introduces a novel technique is proposed for the simultaneous extraction of energy distribution of donor- and acceptor-like interface trap states ($D_{it\_D}(E)$ and D_{it_A} (E)) over a wide range of bandgap energy using a deep UV light with sub-bandgap.

The interface quality between the gate insulator and the active channel material becomes a critical issue in the characterization of β-Ga_2O_3 FETs for both better speed and high power applications [47, 50]. characterization of $D_{it}(E)$ over the forbidden bandgap from valence band maximum (E_V) to conduction band minimum (E_C) become very important for device research. The interface traps, which arises from the fabrication between the gate oxide and the channel surface, could lead to short- or long-term device degradation and prevent high performance and reliability of the devices. Several exquisite techniques have been developed to characterize and analyze D_{it} in the MOS system, such as high/low frequency method, Terman method, photo-assisted I-V method, AC conductance method, and deep level optical and transient spectroscopy, and Terman method [24, 42, 43, 61–63] . In addition, in Ref. [61], acceptor-like density-of-states (DOS) using the current-voltage (I-V)-based optical charge pumping technique in n-channel amorphous indium-gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) has been analyzed. However, there is a limited energy range for the DOS close to the E_C and there is the absence of a general technique for the extraction of DOS close to the E_V. Also, the simultaneous extraction of both $D_{it\_D}(E)$ and $D_{it\_A}(E)$ over a wide range of bandgap energy based on only experimental photonic I-V data in β-Ga_2O_3 FETs has never been reported.

In this work, we proposed a I-V-based sub-bandgap optoelectronic characterization technique for the simultaneous extraction of both $D_{it\_D}(E)$ and $D_{it\_A}(E)$ using the deep UV light with a sub-bandgap photon energy (E_{ph}=3.6 eV and λ=390 nm). By employing the measured I_{DS}-V_{GS} curves under both dark and photonic states and the measured generation-recombination current (I_{G-R}), a consistent mapping of the surface potential (ψ_S) for $D_{it\_D}(E)$ and $D_{it\_A}(E)$ over the bandgap energy (E_C<E<E_V) was applied in two distinguishable subthreshold regions (V_{ON}<V_{GS}<V_{FB} and V_{FB}<V_{GS}<V_T).

Fig. 3.16(a) shows a measurement setup and an equivalent circuit model for the photonic I-V characterization of the β-Ga_2O_3 FETs with bottom-gate structure. A schematic illustration of the energy band diagram for the extraction of $D_{it\_D}(E)$ and $D_{it\_A}(E)$ under a photonic state in shown in Fig. 3.16(b) and (c). The UV optical source illuminates the β-Ga_2O_3 channel of the fabricated device vertically. The UV light (λ=390 nm, E_{ph}=3.6 eV < E_{g_Ga2O3}=4.8 eV, and P_{opt}=2.8 mW) is employed to pump the trapped electrons in the channel surface region from E_C-E_{ph} to E_C. The drain current (I_{D_sub}) in the subthreshold region (V_{ON}<V_{GS}<V_T) in the β-Ga_2O_3 FETs can be described as

$$I_{\mathrm{D\_sub}} = \mu_{\mathrm{eff}} C_{\mathrm{OX}} \left(\frac{W}{L}\right) (\eta(V_{\mathrm{GS}}) - 1)\, {V_{\mathrm{th}}}^2 \times \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{T}}}{\eta(V_{\mathrm{GS}}) V_{\mathrm{th}}}\right) \tag{3.5}$$

with $\eta(V_{GS})$ as the ideality factor related to $D_{it}(E)$ controlled by V_{GS}, μ_{eff} as the effective mobility, C_{OX} as the oxide capacitance, W as the channel width, L as the channel length, V_{th} as the thermal voltage. Also, the $\eta(V_{GS})$ can be expressed as

$$\eta(V_{\mathrm{GS}}) = \left(\frac{(V_{\mathrm{GS}} + \Delta V_{\mathrm{GS}})}{V_{\mathrm{th}}}\right) \Big/ \ln\left(\frac{I_{\mathrm{D\_sub}}(V_{\mathrm{GS}} + \Delta V_{\mathrm{GS}})}{I_{\mathrm{D\_sub}}(V_{\mathrm{GS}})}\right) \tag{3.6}$$

with ΔV_{GS} as step of V_{GS} [64]. For the $\eta(V_{GS})$ under dark and photonic states, each component is also described as

$$\eta_{\mathrm{dark}}(V_{\mathrm{GS}}) = 1 + \left(C_{\mathrm{dep}}(V_{\mathrm{GS}}) + C_{\mathrm{it}}(V_{\mathrm{GS}})\right)/C_{\mathrm{OX}} \tag{3.7}$$

$$\eta_{\mathrm{UV}}(V_{\mathrm{GS}}) = 1 + \left(C_{\mathrm{dep}}(V_{\mathrm{GS}}) + C_{\mathrm{it}}(V_{\mathrm{GS}}) + C_{\mathrm{it\_UV}}(V_{\mathrm{GS}})\right)/C_{\mathrm{OX}} \tag{3.8}$$

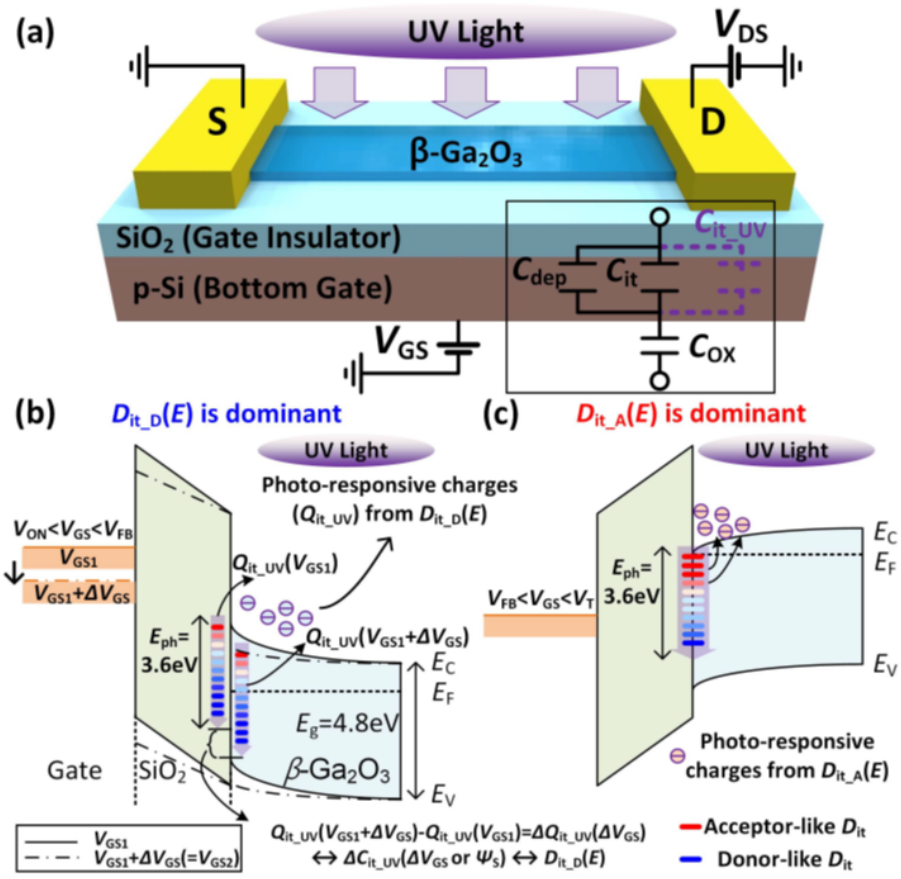

Fig. 3.16. (a) Schematic view of the measurement setup under a photonic state with the sub-bandgap UV light including the equivalent circuit model as the inset. (b) and (c) Energy band diagrams for the concept of simultaneous extractions of both $D_{it\_D}(E)$ and $D_{it\_A}(E)$.

with $C_{it}(V_{GS})$ as the interface traps-induced capacitance under dark state, $C_{it\_UV}(V_{GS})$ as the photo-responsive capacitance for the photo-excited charges, and $C_{dep}(V_{GS})$ as the depletion capacitance. In eq. (3.8), the $\eta_{UV}(V_{GS})$ includes photo-responsive charges generated from $D_{it\_D}(E)$ and $D_{it\_A}(E)$ by sub-bandgap photon as shown in Fig. 3.16. The $\Delta\eta(V_{GS})$ as the difference between $\eta_{dark}(V_{GS})$ and $\eta_{UV}(V_{GS})$ can be expressed as

$$\Delta\eta(V_{\mathrm{GS}}) = \eta_{\mathrm{UV}}(V_{\mathrm{GS}}) - \eta_{\mathrm{dark}}(V_{\mathrm{GS}}) = C_{\mathrm{it\_UV}}(V_{\mathrm{GS}})/C_{\mathrm{OX}} \tag{3.9}$$

We can determine the $\Delta C_{it\_UV}(V_{GS})$ through eqs. (3.10) $\sim$ (3.12)

$$C_{\mathrm{it\_UV}}(V_{\mathrm{GS}}) = C_{\mathrm{OX}}\Delta\eta(V_{\mathrm{GS}}) \tag{3.10}$$

$$d\Delta\eta(V_{\mathrm{GS}})/dV_{\mathrm{GS}} = \left((dC_{\mathrm{it\_UV}}(V_{\mathrm{GS}})/d\psi_{\mathrm{S}}) \cdot (d\psi_{\mathrm{S}}/dV_{\mathrm{GS}})\right)/C_{\mathrm{OX}} \tag{3.11}$$

$$\Delta C_{\mathrm{it\_UV}}(V_{\mathrm{GS}}) = C_{\mathrm{OX}} \int_{\psi_{\mathrm{S}}(V_{\mathrm{GS}})}^{\psi_{\mathrm{S}}(V_{\mathrm{GS}}+\Delta V_{\mathrm{GS}})} \left(\frac{d\Delta\eta(V_{\mathrm{GS}})}{dV_{\mathrm{GS}}} \Big/ \frac{d\psi_{\mathrm{S}}}{dV_{\mathrm{GS}}} \right) d\psi_{\mathrm{S}} \tag{3.12}$$

In the extraction of $D_{it\_D}(E)$ and $D_{it\_A}(E)$ as illustrated in Fig. 3.16(b) and (c), eq. (3.12) can be converted to $\Delta C_{it\_D}(V_{GS})$ and $\Delta C_{it\_A}(V_{GS})$ over two different regions ($V_{ON}<V_{GS}<V_{FB}$ and $V_{FB}<V_{GS}<V_T$) with ΔV_{GS} as follow respectively:

$$\Delta C_{\mathrm{it\_D}}(V_{\mathrm{GS}}) = C_{\mathrm{OX}} \int_{\psi_{\mathrm{S}}(V_{ON})}^{\psi_{\mathrm{S}}(V_{\mathrm{FB}})} \left(\frac{d\Delta\eta_{\mathrm{D}}(V_{\mathrm{GS}})}{dV_{\mathrm{GS}}} \Big/ \frac{d\psi_{\mathrm{S}}}{dV_{\mathrm{GS}}} \right) d\psi_{\mathrm{S}} \tag{3.13}$$

$$\Delta C_{\mathrm{it\_A}}(V_{\mathrm{GS}}) = C_{\mathrm{OX}} \int_{\psi_{\mathrm{S}}(V_{\mathrm{FB}})}^{\psi_{\mathrm{S}}(V_{\mathrm{T}})} \left(\frac{d\Delta\eta_{\mathrm{A}}(V_{\mathrm{GS}})}{dV_{\mathrm{GS}}} \Big/ \frac{d\psi_{\mathrm{S}}}{dV_{\mathrm{GS}}} \right) d\psi_{\mathrm{S}} \tag{3.14}$$

For the mapping of the V_{GS} to the specific trap energy level for both $D_{it\_D}(E)$ and $D_{it\_A}(E)$ $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ over the bandgap, the measured $I_{D\_sub}(V_{GS})$ was also divided into two operation regions ($V_{ON}<V_{GS}<V_{FB}$ and $V_{FB}<V_{GS}<V_T$). Then, the $\psi_S(V_{GS})$ corresponding to V_{GS} was calculated as Ref. [61].

Finally, $D_{it\_D}(E)$ and $D_{it\_A}(E)$ can be extracted through

$$D_{\mathrm{it\_D}}(E) = \Delta C_{\mathrm{it\_D}}(V_{\mathrm{GS}})/q^2 \tag{3.15}$$

And similarly for $D_{it\_A}(E)$.

In order to extract $D_{it\_D}(E)$ and $D_{it\_A}(E)$ by the photonic I-V technique, we measured the I_{DS}-V_{GS} and I_{G-R} characteristics (Keysight B1500 Semiconductor Parameter Analyzer and a Cascade Summit probe station) of β-Ga_2O_3 FETs with bottom-gate structure. The representative β-Ga_2O_3 FET has the channel length of L=1 μm and the channel width of W=1 μm.

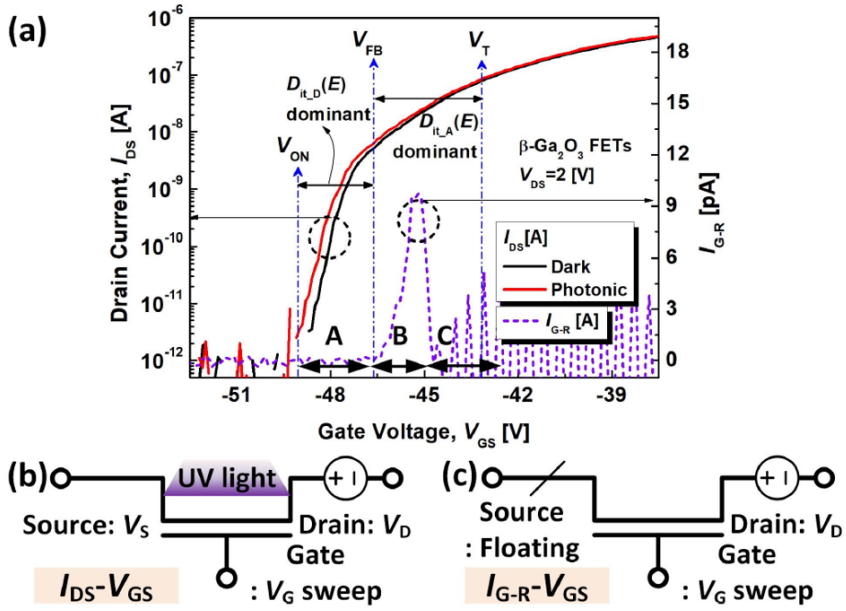

Fig. 3.17. (a) Measured I_{DS}-V_{GS} characteristics under dark (black line) and photonic (red line) states. The I_{G-R} (dash line) was measured with the source terminal floating. Measurement setup for (b) I_{DS}-V_{GS} with UV light and (c) I_{G-R}.

Fig. 3.17 shows the measured I_{DS}-V_{GS} characteristics under both dark and photonic states and I_{G-R}-V_{GS} curve. It is well known that the electrons arising from $D_{it}(E)$ according to the ΔV_{GS} correspond to those from a specific ψ_S or energy level over the bandgap. To fully pump out carriers from $D_{it\_D}(E)$ and $D_{it\_A}(E)$, which is located in the range from E_C to E_V, the UV light with E_{ph}=3.6 eV is employed. Also, the measured I_{G-R} as a function of V_G at V_D=2 V is shown in Fig. 3.17(a). Initially, the I_{G-R} is negligible because the energy difference between the Fermi en-

ergy E_F and E_C near the channel interface is so large compared with the thermal energy when the V_G is less than V_{FB}. Also, the amount of thermally generated charges which can contribute to the I_{G-R} is insufficient because the source terminal is floated (A region in Fig. 3.17(a)). As V_G increases, the I_{G-R} at the drain side increases by the thermal generation since E_F get closer to E_C in the channel region near the interface (B region in Fig. 3.17(a)). On the other hand, the I_{G-R} decreases when the V_G is too larger than flatband voltage V_{FB} because the increase of both the electron concentration and empty trap states makes the recombination process dominant (C region in Fig. 3.17(a)). The measurement setup for I_{DS}-V_{GS} curves under a photonic state with UV light and I_{G-R}-V_{GS} characteristic is shown in the Fig. 3.17(b) and (c), respectively. Accordingly, a dominant component between $D_{it\_D}(E)$ and $D_{it\_A}(E)$ can be determined based on the V_{FB} in the measured I_{G-R} curve [22]. In depletion region (V_{ON}<V_{GS}<V_{FB}), the photo-responsive charges generated from the $D_{it\_D}(E)$ mainly affect I_{DS}, while the photo-responsive charges excited from the $D_{it\_A}(E)$ contribute to I_{DS} in accumulation region (V_{FB}<V_{GS}<V_T).

Fig. 3.18 shows $D_{it\_D}(E)$ and $D_{it\_A}(E)$ obtained from the proposed photonic I-V technique. V_{GS}-dependent experimental $\eta_{dark}(V_{GS})$ and $\eta_{UV}(V_{GS})$ in two distinguishable regions (V_{ON}<V_{GS}<V_{FB} and V_{FB}<V_{GS}<V_T) are shown in the inset of Fig. 3.18(a) and (b), respectively. Through the proposed technique, we obtained D_{it_D}(E) and $D_{it\_A}(E)$ over the subgap energy range with the range of 0.5×10^{11} $eV^{-1}cm^{-2}$ to 5.5×10^{11} $eV^{-1}cm^{-2}$ and of 2.1×10^{11} $eV^{-1}cm^{-2}$ to 1.1×10^{12} $eV^{-1}cm^{-2}$, respectively. The extracted values obtained in this work are comparable to those of other reports [47, 50].

It worth noting that this proposed technique allows the simultaneous characterization of $D_{it\_D}(E)$ and $D_{it\_A}(E)$ with a wide range of bandgap energy by applying the calculated ψ_S separately in two distinguishable subthreshold regions, instead of the single ψ_S over full subthreshold range. We also note that the C-V-based extraction method, which demands large-sized devices, has a limit on a parasitic component to be corrected for accurate extraction of the $D_{it}(E)$ in the only β-Ga_2O_3 channel re-

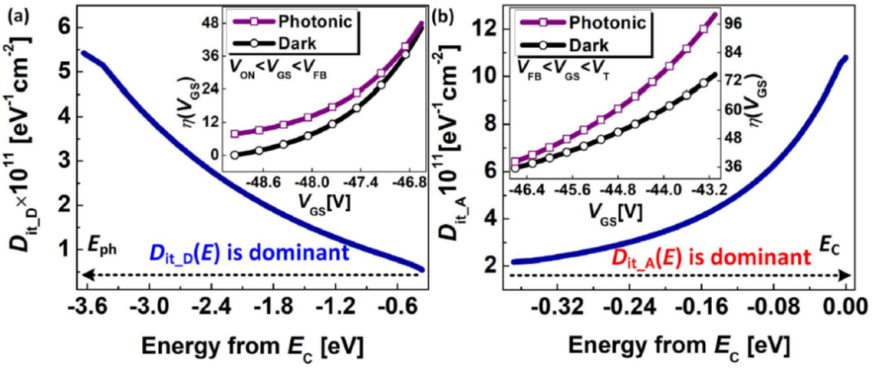

Fig. 3.18. Energy distribution of extracted D_{it} [(a): $D_{it\_D}(E)$ and (b): $D_{it\_A}(E)$] via photo-responsive I-V characteristics with sub-bandgap UV light. The inset shows the extracted $\eta(V_{GS})$

gion excluding the contribution from the gate-to-source and gate-to-drain overlapped regions.

A drawback to this technique, however, that it is limited when applied to top-gate devices when the incident light cannot pass through the gate metal. In this regard, two possible methods can be used to improve the applicability of this technique: 1) irradiation of the tilted light on the top of the device, and 2) irradiation of the backlight at the bottom of the device with a transparent substrate.

in conclusion,a sub-bandgap UV light-based photonic IV technique based on a differential subthreshold ideality factor in the dark and photonic states was proposed for the extraction of $D_{it}(E)$ over a wide range of bandgap energy in β-Ga_2O_3 FETs. We found that the extracted $D_{it}(E)$ is fully separated into $D_{it\_D}(E)$ and $D_{it\_A}(E)$ based on the photo-responsive carriers generated by the sub-bandgap UV light and the I_{G-R} configuration for generation and recombination processes. This proposed method has the advantage of simplicity compared to other techniques such as the temperature-dependent characterization, complicated numerical calculations, charge-pumping method, or $1/f$ noise characterization method owing to the extraction of $D_{it\_D}(E)$ and $D_{it\_A}(E)$ with a consistent mapping of the ψ_S for the sub-bandgap

energy from the same subthreshold current data. We expect that the proposed technique will become an effective tool for the solid characterization in β-Ga_2O_3 FETs and other nano-devices with small dimensions.

4. NOISE MEASUREMENTS IN NEGATIVE CAPACITANCE FIELD-EFFECT TRANSISTOR

As introduced in section 1.4 of chapter 1 that the low-frequency noise (LFN) measurements is an important investigative tool that helps understand the characteristics of the state-of-the-art miniaturized devices where most of other classical characterization methods are not applicable in ultra-scaled devices. For example, studying the channel/insulator interface using conductance method as done in the previous chapter, requires a large gate oxide area, and effective inversion layer thickness in order to get a reliable data about the device's interface quality and general properties. Charge pumping method will also fail due to very small gate area and charge pumping current is proportional to gate area. This where LFN plays an important role to quantitatively analyze the performance, reliability, and variability of ultra downscaled devices [34, 65–71].

4.1 LFN Measurements on MoS_2 NC-FETs

It is beyond any doubt that low noise devices are required for digital and analog applications. A systemic study on the noise performance of a transistor is therefore important too. Noise has been extensively studies in conventional MOSFET with regular (positive) oxides. However, The integration of negative capacitance using ferroelectric insulator in gate stack has triggered intensive research interest recently as one of the emerging solutions to achieve subthreshold swing (SS) below the Boltzmann limit of 60 (mV/dec) at room temperature for a MOSFET [7, 18, 72–78]. Meanwhile, 2-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs), have the potential for ultra-scaled transistor technology beyond the 10 nm technology node because of their atomically thin layered structures and low dielectric constant,

which offers strong electrostatic control [77, 78]. Recently, MoS_2 negative capacitance field-effect transistors (NC-FETs) have been demonstrated with sub-thermionic SS and non-hysteretic transfer characteristics, suggesting the potential for 2D NC-FETs for future ultra-scaled and low power digital applications [7, 77]. The 2D semiconductor and its interface to ferroelectric gate stack in MoS_2 NC-FETs may present unique interface and ferroelectric properties. low-frequency noise characterizations can be utilized to quantitatively analyze the performance and reliability of these devices. However, there have not yet been any studies on the low-frequency noise on 2D NC-FETs.

We have reported on low-frequency noise studies on MoS_2 NC-FETs. low-frequency noise is systematically studied for various interfacial oxides, and with different thicknesses of interfacial oxide on top of the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO). The low-frequency noise is found to decrease with thicker ferroelectric HZO in the subthreshold regime of a MoS_2 NC-FET, because thicker HZO leads to stronger negative capacitance effect and thus larger series of gate capacitance and better electrostatic control of the channel. The existence of negative capacitance in ferroelectric HZO facilitates a new approach to suppress the noise of the semiconductor devices.

Fig.4.1 shows a schematic view of a MoS_2 NC-FET. The NC-FET devices presented in this study consist of a few-layer MoS_2 flake as the channel, and a gate stack composed of an amorphous interfacial oxide (Al_2O_3, ZrO_2, or HfO_2) and polycrystalline HZO employed as a ferroelectric oxide on a heavily doped silicon substrate as the gate electrode and nickel source/drain (S/D) contacts. Fig.4.2 shows a top-view of a Scanning Electron Microscopy (SEM) image of two MoS_2 NC-FETs fabricated on the same MoS_2 flake with different channel lengths.

Table 4.1 summarizes the different gate stacks of the samples studied in this work. MoS_2 NC-FETs were fabricated as follows: HZO film was deposited by atomic layer deposition (ALD) at 250 ^{o}C on a heavily p-doped (p++) silicon substrate that was cleaned by standard solvent cleaning, BOE dip, and deionized water rinse. TDMAHf, TDMAZr, and H2O were used as Hf precursor, Zr precursor, and oxygen precursor,

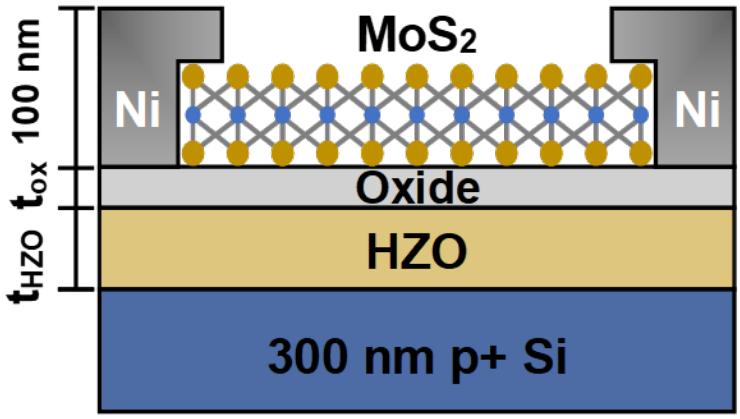

Fig. 4.1. Schematic diagram of a MoS_2 NC-FET. The device includes the p++ Si as gate electrode, HZO as the ferroelectric layer, Al_2O_3, HfO_2, or ZrO_2 as the oxide layer and 100 nm Ni as source/drain contacts.

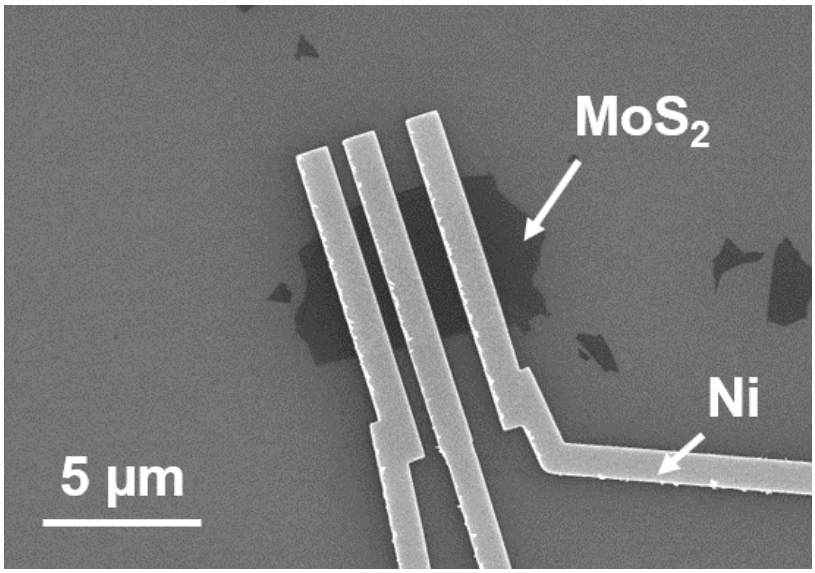

Fig. 4.2. Top-view SEM image of two MoS_2 NC-FETs, capturing the MoS_2 flake and Ni electrodes. .

respectively. Another Al_2O_3, ZrO_2, or HfO_2 layer was subsequently in-situ deposited by ALD at the same temperature. Then, rapid thermal annealing (RTA) in nitrogen

Table 4.1.
Description of samples and device dimensions

SAMPLE	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Channel $4 \sim 10$**nm**	MoS_2	MoS_2	MoS_2	MoS_2	MoS_2	MoS_2	MoS_2
$\mathbf{Al_2O_3}$ **(nm)**	-	-	0.5	1	2	2	2
$\mathbf{HfO_2}$ **(nm)**	1	-	-	-	-	-	-
$\mathbf{ZrO_2}$ **(nm)**	-	1	-	-	-	-	-
HZO (nm)	20	20	20	20	20	15	35

ambient for 1 minute at 500 ^{o}C was performed. MoS_2 flakes were transferred afterward to the substrate by mechanical exfoliation.

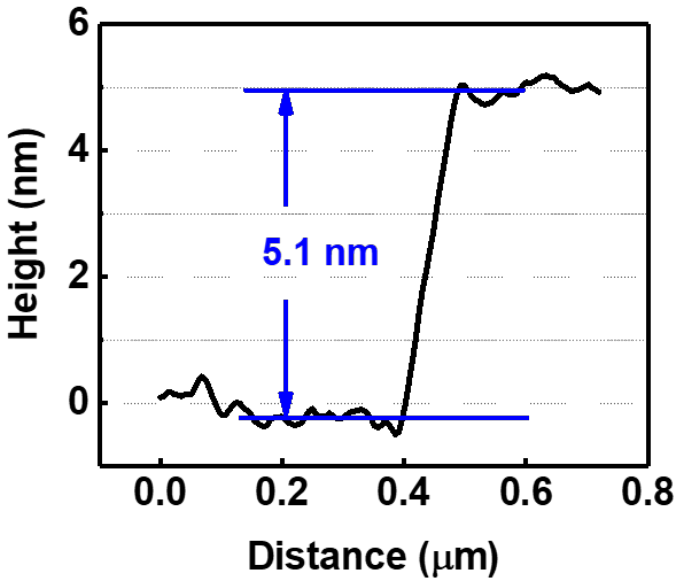

Fig. 4.3. Typical MoS_2 flake thickness measured by AFM for a MoS_2 NC-FET.

Fig.4.3 shows the Atomic Force Microscopy (AFM) measurement of a typical exfoliated flake with thickness controlled between 4 nm and 10 nm. Electrodes of 100 nm

nickel were fabricated by an electron-beam lithography, electron-beam evaporation, and lift-off process. All electrical and noise measurements were performed in air at room temperature using a Keysight B1500/B1530A system, see Fig.4.4.

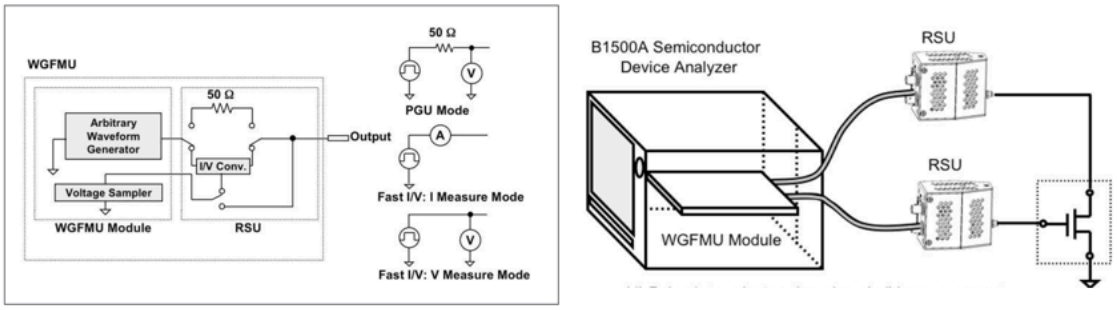

Fig. 4.4. Simplified circuit diagram of the WGFMU showing its operation modes (left) and Measurements setup (right)

To confirm the ferroelectricity of the film, A metal-insulator-Si (M-I-S) capacitor was fabricated and measured. Fig.4.5 and Fig.4.6 show the 100 nm Ni/3 nm Al_2O_3/20 nm HZO/n++ Si structure of the capacitor and the C-V measurements of , respectively. As seen from Fig.4.6 the capacitance peaks for forward gate voltage sweep is measured at different voltage at the reveres gate voltage sweeps. Furthermore, the polarization vs. voltage (P-V) is directly measured on this ferroelectric capacitor at different frequencies using Radiant Precision LC II test system at a 10 V voltage sweep range.

The polarization measurement is fundamentally done by applying a stimulus signal on the capacitor's gate and integrating the measured current passing through the capacitor to compute the charge. Clean hysteresis loops can be observed for 10 V voltage sweep in Fig.4.7 at frequencies ranges from 50 Hz to 1 KHz. The P-V characteristics as a function of the voltage sweep range with fixed frequency at 100 Hz are shown in Fig.4.7. Both remnant polarizations and coercive field increase with larger voltage sweep range, indicating the polycrystalline nature of the ferroelectric

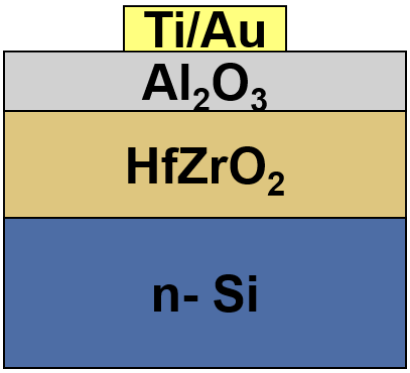

Fig. 4.5. M-I-Si capacitor structure schematic of the capacitor used in C-V and P-V measurements.

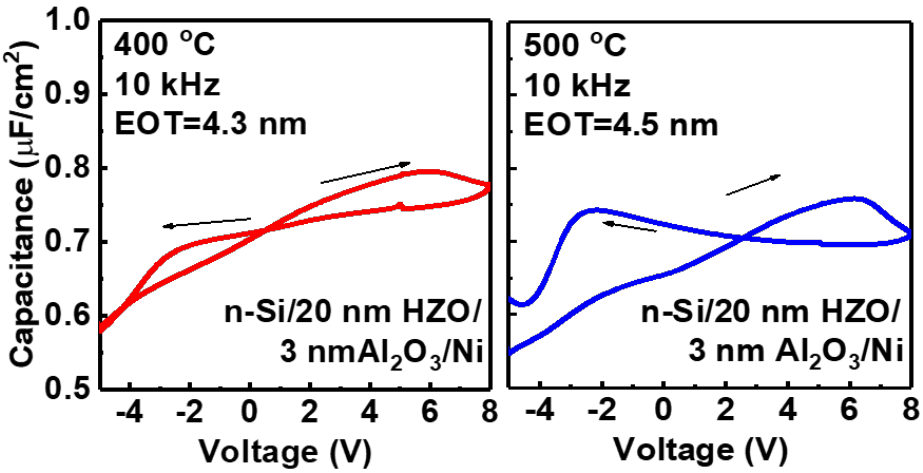

Fig. 4.6. C-V measurements of the M-I-M capacitor with different capacitance peak for forward and reveres V_G sweeps.

HZO. Different grains can provide different remnant polarizations and coercive fields due to the different domain sizes and crystal orientations.

I_D-V_{DS} characteristics of a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO at room temperature, low V_{GS}, and low V_{DS} conditions are plotted in Fig.4.8, where I_D is the drain current and V_{DS} is the drain-source voltage. This device has a channel length

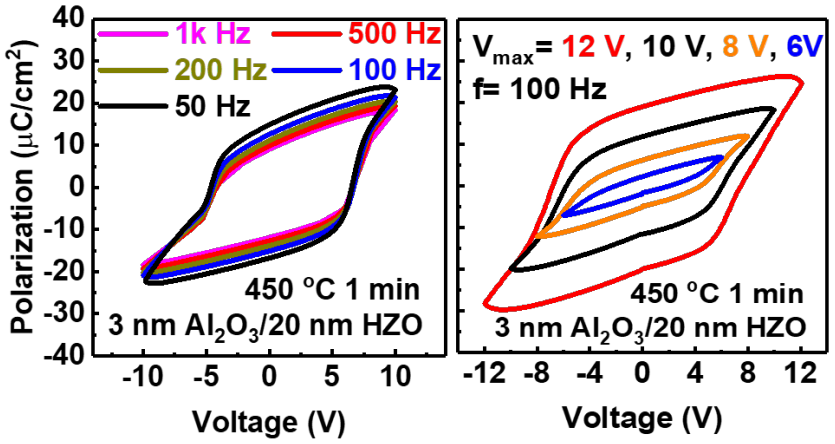

Fig. 4.7. (LEFT) Hysteresis loops of P-V for 20 nm HZO/3 nm Al_2O_3 annealed at 450 ^{o}C, measured from 50 Hz to 1 kHz. (RIGHT) Hysteresis loops of P-V for 20 nm HZO/3 nm Al_2O_3 annealed at 450 ^{o}C at voltage sweep ranges from 6V to 12 V.

(L_ch) of 2 μm and channel thickness (T_ch) of 10 nm. The I_D-V_{GS} characteristics of the same device at room temperature was measured and shown in 4.9, measured at V_{DS} voltages of 0.1 V, 0.5 V, and 0.9 V.

The I_D-V_{GS} characteristics are measured using bi-directional sweeps (sweeping the gate voltage from low to high then from high to low voltages, with sweep time of 1 minute for each V_{DS} bias). No significant hysteresis can be observed on this device (less than 5 mV measured at 0.1 nA/μm). The device also displays good switching behavior ($I_{ON}/I_{OFF} > 10^6$), and a linear relationship between I_D and V_{DS}, which indicates a minimal effect on measured I_D noise from S/D Schottky barriers. The MoS_2 NC-FET was confirmed to have SS less than 60mv/dec, Fig.4.10 shows SS vs. I_D at the off-state of the device. The MoS_2 NC-FET exhibits SS for forward sweep and for reverse sweep of 55.1 mV/dec and 45.0 mV/dec, respectively, which are below the 60 mV/dec limit in both sweeps. To examine drain current fluctuation, I_D vs. time characteristics are measured at constant V_{GS} and V_{DS} biases after a few seconds hold time (V_{DS}=0.1V unless otherwise specified, and chosen to ensure linear

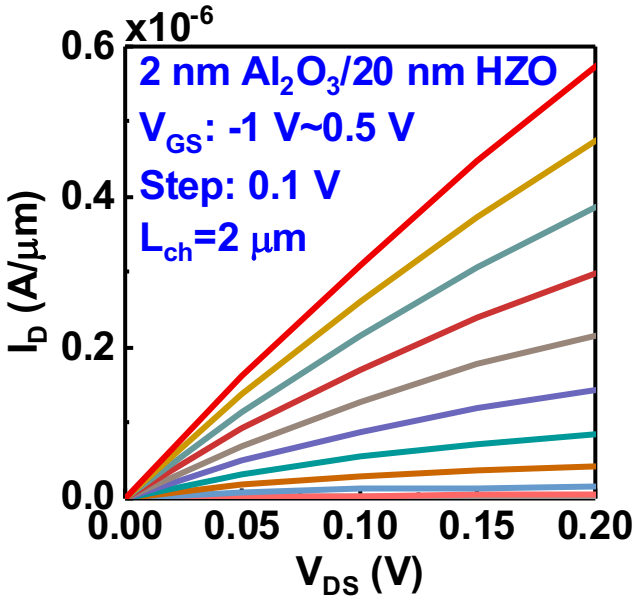

Fig. 4.8. I_D-V_{DS} characteristics of a MoS_2 NC-FET measured at room temperature, W_{ch}=5.7 μm. The transistor exhibits good switching behavior (I_{on}/I_{off}¿$10^6$6), with linear relationship between I_D and V_{DS} which also confirms minimal effect of the S/D Schottky barriers

operation mode). Fig.4.11 shows measured I_D vs. time during low-frequency noise measurement. No obvious drain current (or V_T) drifting can be observed, suggesting bias temperature instability (BTI) is not a concern during the noise measurement (less than 100 seconds of a stress) and all charge trapping is screened during the initial hold time. The power spectral density (S_{ID}) is calculated based on the the measured I_D vs. time characteristic.

Fig.4.12 shows the normalized power spectral density (S_{ID}/I_D^2) vs. frequency of a MoS_2 NC-FET with L_ch= 2 μm, 5.7 μm channel width (W_ch), and 2 nm Al_2O_3/20 nm HZO as gate dielectric, measured for different gate voltages. Each sweep shows a clear $1/f$ characteristic. S_{ID}/ID2 as a function of I_D at single frequency f=10 Hz of the same device is depicted in Fig.4.13. In this figure, S_{ID}/ID2 vs. I_D deviates from a linear curve and is proportional to (g_m/I_D)2. This suggests carrier number

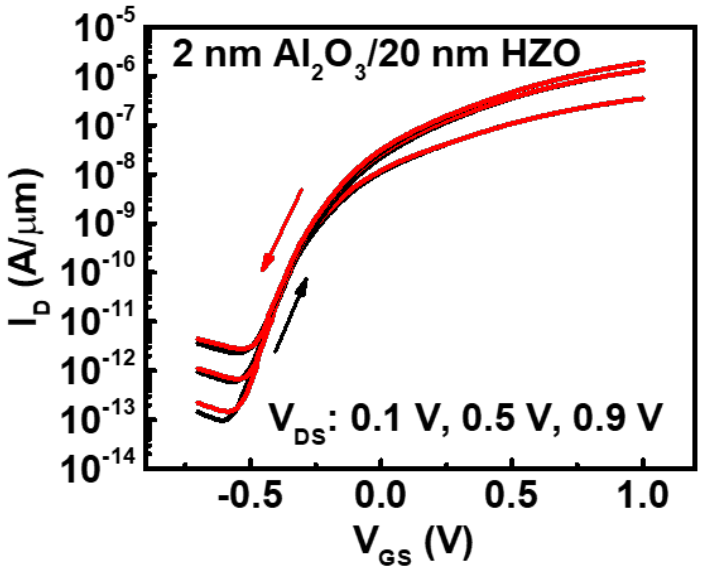

Fig. 4.9. I_D-V_{GS} characteristics of a MoS_2 NC-FET measured at room temperature. This device has a L_{ch} of 1 μm, W_{ch} of 5.7 μm, channel thickness of 10 nm, and 2 nm Al_2O_3 and 20 nm HZO as gate dielectric.

fluctuation (CNF) contributing to the low-frequency noise rather than carrier mobility fluctuation. S_{ID}/I_D^2 as a function of V_{DS} at f=10 Hz is shown in Fig.4.14 for MoS_2 NC-FETs with 2 nm Al_2O_3 and HZO thickness varying from 15 nm to 35 nm as the gate dielectrics. Here, although the noise from the Schottky contacts reduces with increased V_{DS}, the dependence of power spectral density above V_{DS}=0.1 V is weak, which also confirms that the noise measured comes from the channel instead of Schottky contact resistance [79]. Therefore, CNF inside the MoS_2 channel is verified as the main noise source for MoS_2 NC-FETs in this work. From the well established model for carrier number fluctuation, the drain current noise varies approximately as in eq. 4.1 for the above threshold region and eq. 4.2 for the subthreshold region [80],

$$\frac{WL * S_{IiD}}{I_D^2} = \frac{q^2 kT\lambda N_t}{f^\gamma C_{insulator}(V_{GS}-V_T)^2} \propto \frac{q^2 g_m^2 kT\lambda N_t}{f^\gamma} \tag{4.1}$$

$$\frac{WL * S_{IiD}}{I_D^2} = \frac{q^2 \lambda N_t}{kT f^\gamma (C_{insulator}+C_{it}+C_d)^2} \tag{4.2}$$

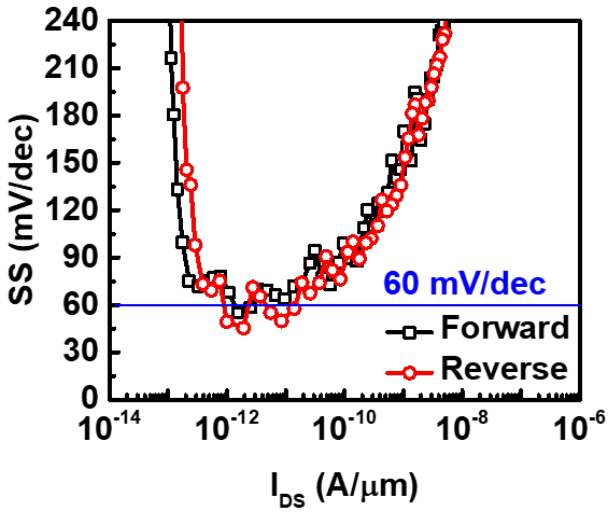

Fig. 4.10. SS vs. I_D characteristics of the same device as in Fig.4.9. SS less than 60 mV/dec is obtained at room temperature for both forward and reverse gate voltage sweep directions.

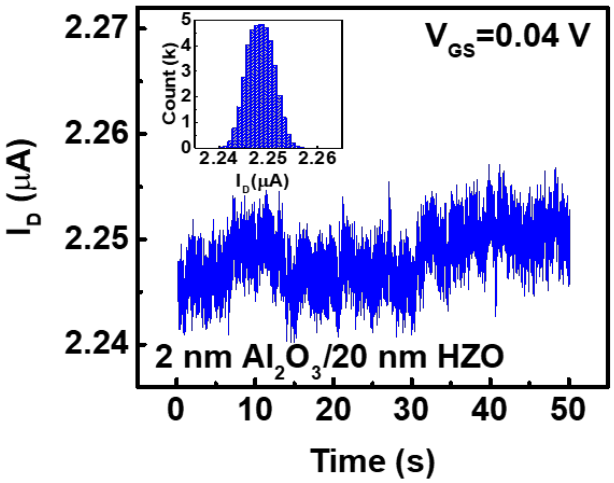

Fig. 4.11. SS vs. I_D characteristics of the same device as in Fig.4.9. A typical I_D fluctuation vs. time measured at V_{GS}=0.04 V for a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO as gate dielectric. .

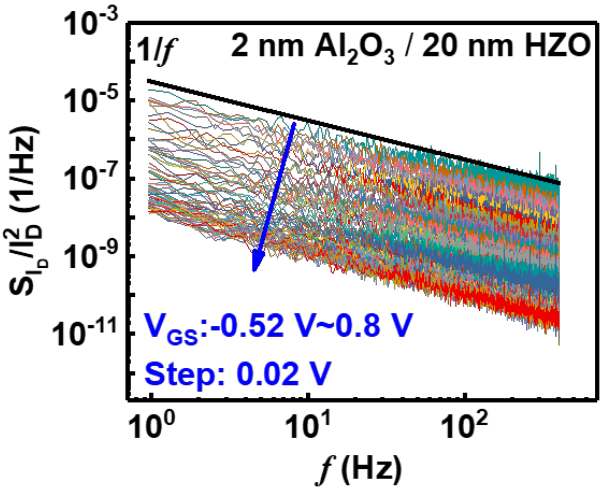

Fig. 4.12. Normalized I_D noise at f=10 Hz for a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO as gate dielectric. The non-linear behavior at low drain current and the proportional scaling with $(g_m/I_D)^2$ indicates charge number fluctuation to be the source of the low-frequency noise measured in this work.

where N_t is the trap density in the gate dielectric, λ is the tunneling attenuation length (constant in this work), γ is the frequency exponent (1 in this work as seen in Fig.4.12), C_d is the depletion capacitance and C_{it} is the interface trap capacitance. From eq. 4.1, the normalized power spectral density by drain current and area ($W_{ch}L_{ch}{}^*S_{ID}/I_D^2$) vs. I_D is not dependent on oxide thickness in the on-state, hence, our major discussion in this work focuses on the subthreshold regime. In this regime, C_d is the same at a given I_D with the same doping concentration. Therefore, a larger gate capacitance ($C_{insulator}$) results in less normalized noise, $W_{ch}L_{ch}{}^*S_{ID}/I_D^2$ when the same number of traps N_t are present and hence same C_{it} in eq. 4.2. For conventional MOSFETs, $W_{ch}L_{ch}{}^*S_{ID}/I_D^2$ increases with thicker gate oxide since $C_{insulator}$ is decreased as described in eq. 4.2.

Furthermore, depending on the measured normalized PSD for different gate oxides to compare the effect of the the different ferroelectric insulators matchings, Fig.4.15 shows $W_{ch}L_{ch}{}^*S_{ID}/I_D^2$ vs. I_D at 10 Hz frequency for MoS_2 NC-FETs with different 1

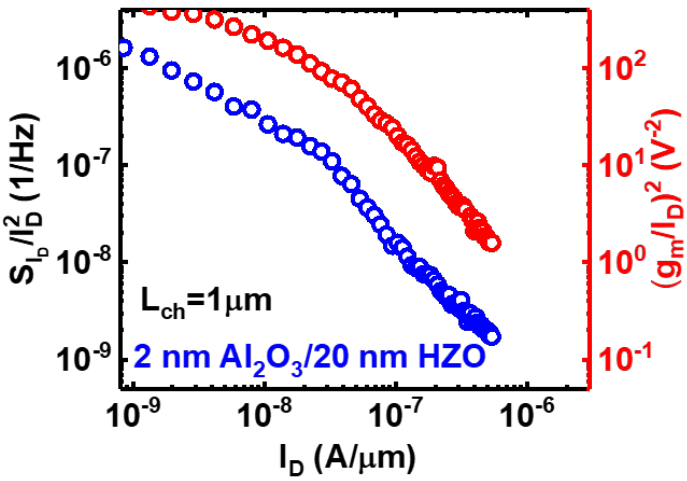

Fig. 4.13. Normalized I_D noise at f=10 Hz for a MoS_2 NC-FET with 2 nm Al_2O_3/20 nm HZO as gate dielectric. The non-linear behavior at low drain current and the proportional scaling with $(g_m/I_D)^2$ indicates charge number fluctuation to be the source of the low-frequency noise measured in this work.

nm interfacial oxide layers on 20 nm HZO as the gate dielectric. $W_{ch}L_{ch}{}^*S_{ID}/I_D^2$ is different with different interfacial oxide, showing that oxide traps within the Al_2O_3/HZO gate stack are the lowest amongst the three measured combinations. Then Al_2O_3/HZO was chosen for further noise study. In Fig.4.16 the $W_{ch}L_{ch}{}^*S_{ID}/I_D^2$ vs. I_D at 10 Hz for MoS_2 NC-FETs but with three Al_2O_3 thicknesses, namely, 0.5 nm, 1nm, and 2 nm with 20 nm HZO as the gate dielectric are compared. Referring to eq. 4.2, $W_{ch}L_{ch}{}^*S_{ID}/I_D^2$ should be smaller for thinner Al_2O_3 since the total gate capacitance is larger. The data matches the theoretical prediction from this equation well. We ascribe the part of the larger noise at high current level in the 0.5 nm Al_2O_3 sample to the significant amount of oxide traps inside HZO, which may affect the channel noise directly with only 0.5 nm of Al_2O_3 in between. Therefore, a suitable oxide layer design between HZO and the channel is required for high performance MoS_2 NC-FETs with low noise.

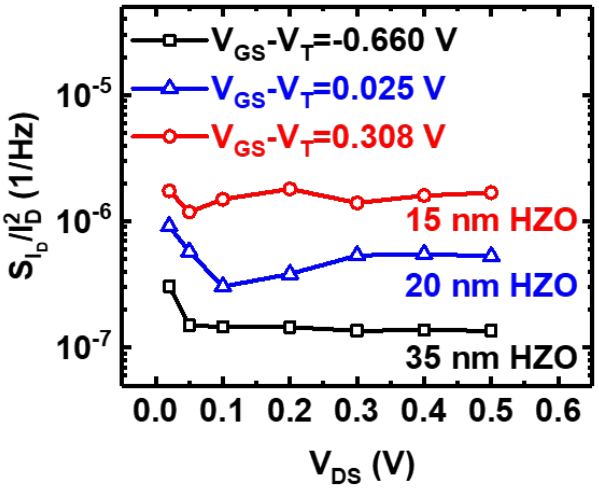

Fig. 4.14. Normalized I_D noise vs. V_{DS} at f=10 Hz for MoS_2 NC-FETs with 2 nm Al_2O_3 and HZO from 15 nm to 35 nm as gate dielectric. The weak dependence of S_{ID} above V_{DS}= 0.1 V suggests the noise mostly comes from the channel instead of Schottky contacts..

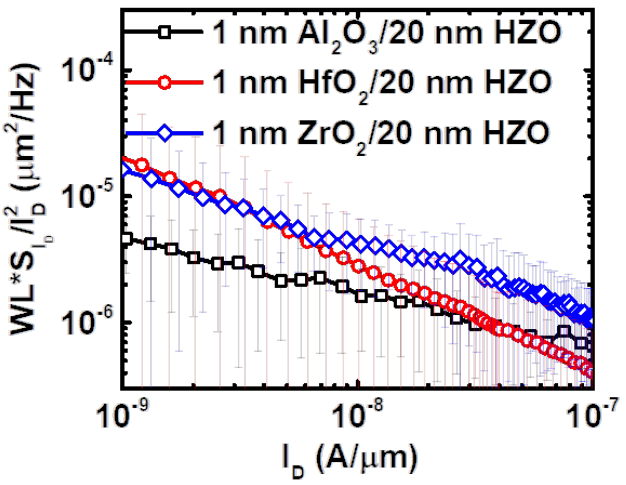

Fig. 4.15. Normalized I_D noise vs. I_D at f=10 Hz for MoS_2 NC-FETs with 1 nm different interfacial oxides and 20 nm HZO as gate dielectric.

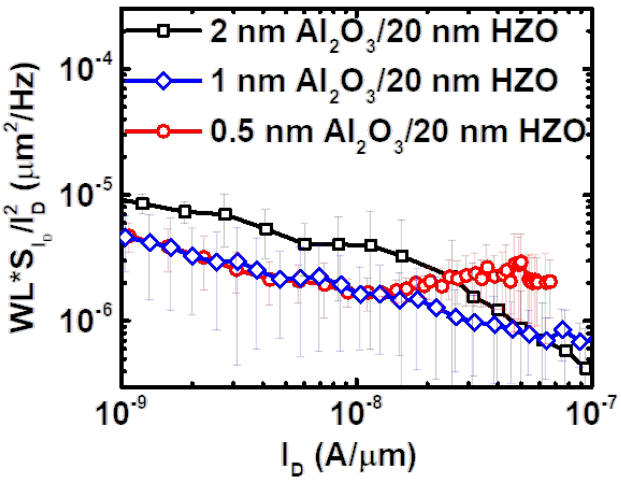

Fig. 4.16. Normalized I_D noise vs. I_D at f=10 Hz for MoS_2 NC-FETs with 0.5, 1, and 2 nm Al_2O_3 and 20 nm HZO as gate dielectric.

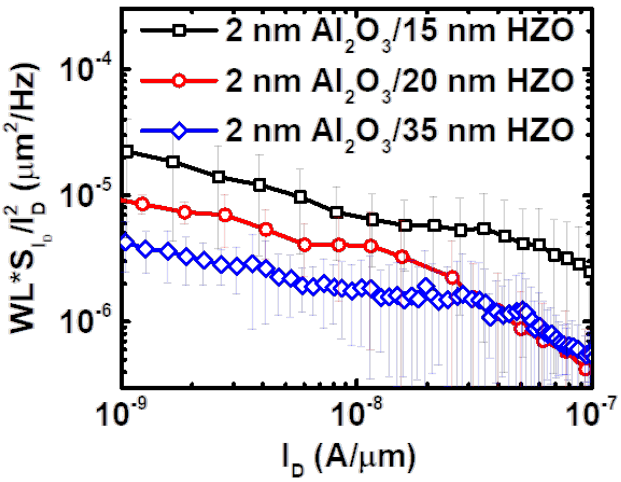

Fig. 4.17. Normalized I_D noise vs. I_D at f=10 Hz for MoS_2 NC-FETs with 2 nm Al_2O_3 and 15 nm, 20 nm, and 35 nm HZO as gate dielectric.

4.1.1 Experimental Evidence of Negative Capacitance

To investigate the effect of the thickness of the ferroelectric HZO, The normalized noise $W_{ch}L_{ch}{}^{*}S_{ID}/I_D^2$ vs. I_D at f=10 Hz are plotted in Fig.4.17 for MoS_2 NC-FETs with 2 nm Al_2O_3 interfacial layer and different HZO thicknesses as gate dielectrics. The HZO thicknesses are 15 nm, 20 nm, and 35 nm. From this figure, the normalized power spectral density $W_{ch}L_{ch}{}^{*}S_{ID}/I_D^2$ is lower with thicker ferroelectric HZO in the subthreshold regime in significant contrast to the conventional high-k MOSFETs [18, 19]. Based on eq. 4.2, this suggests that a larger gate capacitance occurs for a thicker HZO instead. This key result verifies that the NC effect not only provides steep subthreshold slope and enhances on-state and off-state performances, but also can suppress $1/f$ noise in devices. Since the devices in Fig.4.17 have the same 2 nm Al_2O_3 as interfacial oxide layer, therefore, the capacitance of the HZO layer must be negative to achieve a larger total gate capacitance for thicker oxide gate stacks. Hence, the existence of negative capacitance in the ferroelectric HZO can be employed to physically explain the noise measurement results. Note that the data in figures 4.15, 4.16, and 4.17 are based on at least 3 to 5 similar fabricated devices measured and averaged.

4.1.2 Anomalous RTN Signal Observed in MoS_2 NC-FETs

Aside from the measured $1/f$ noise, an unlooked-for RTN noise was detected in few NC-FET devices. Fig.4.18 shows the I_D fluctuation due to RTN for a MoS_2 NC-FET with L_ch=1 μm, W_ch =3 μm, and 1 nm ZrO_2 and 20 nm HZO as gate dielectric at V_{GS}=0.92 V (strong inversion) where I_D is fluctuating by 20% from the nominal saturation value. Fig.4.19 (Top) shows the histogram of measured drain current, the histogram clearly shows a two-level transition in the gaussian distributed I_D, while Fig.4.19 (Bottom) displays I_D RTN amplitude variation dependence on V_{GS}. At low V_{GS}, it is difficult to observe RTN signals due to the longer emission time constant than the measurement time. RTN is typically attributed to single-

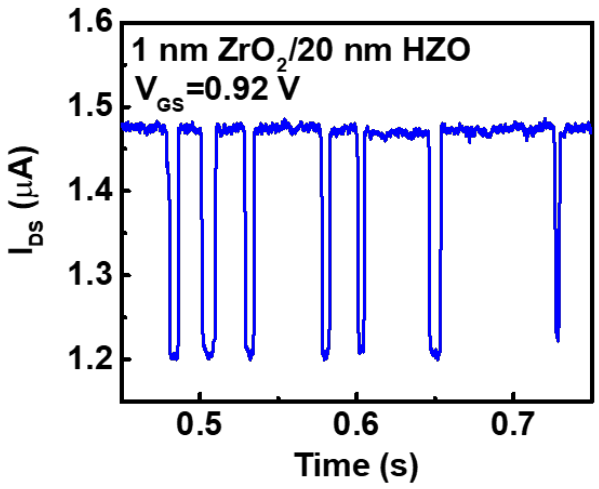

Fig. 4.18. I_D fluctuation due to RTN for a MoS_2 NC-FET with 1 nm ZrO_2 and 20 nm HZO as gate dielectric. Clear two-level transition can be observed.

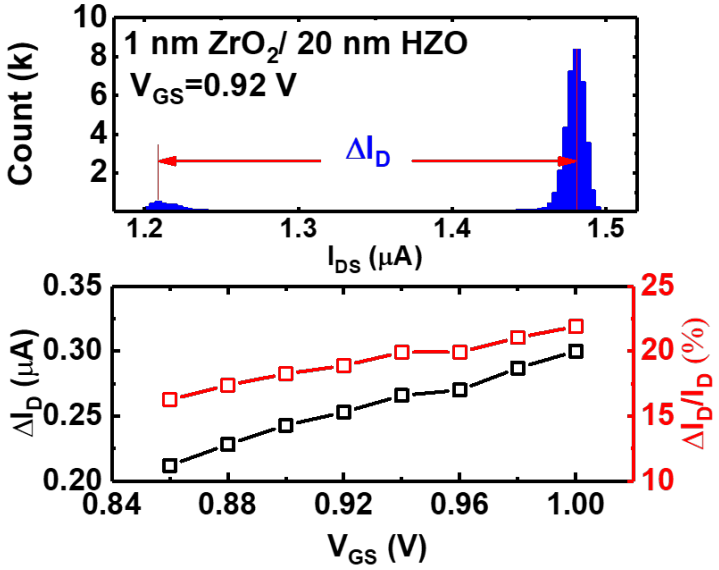

Fig. 4.19. (Top) Histogram of the RTN signals in Fig.4.18. (Bottom) ΔI_D and $\Delta I_D/I_D$ relation with different V_{GS} of the RTN signals observed in the same device.

electron trapping/de-trapping event and observed for the first time for 2D NC-FETs. To see the PSD of this event, Fig.4.20 illustrates the normalized I_D noise in frequency domain; a well-defined Lorentz spectrum can be observed with $1/f^2$ characteristic.

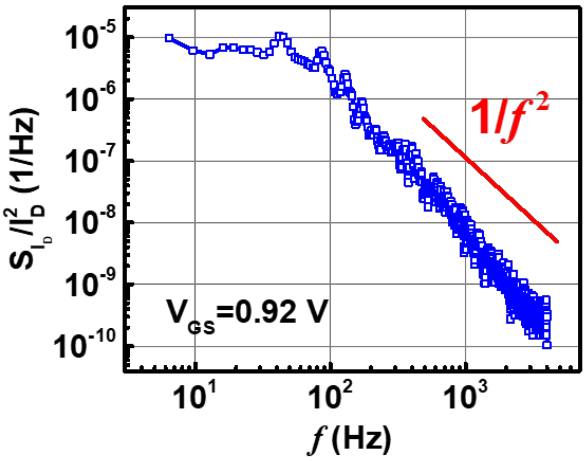

Fig. 4.20. Normalized I_D noise vs. frequency for the device in 4.18, showing a Lorentz spectrum and $1/f^2$ characteristic that confirms the RTN signal.

The results confirm that RTN signals can be occasionally obtained from long channel MoS_2 NC-FETs, although the physical origin of this RTN phenomenon is still unknown, but this could give an impression of an affect related to polarized carriers that have not yet confirmed, and it would be under investigation lately in this thesis.

Conclusion

We reported on low-frequency noise studies on MoS_2 NC-FETs for the first time. Devices with various interfacial oxides, different thicknesses of interfacial oxide, and ferroelectric HZO are systematically studied. The low-frequency noise is found to decrease with thicker ferroelectric HZO in the subthreshold regime of the MoS_2 NC-

FETs, in contrast to the conventional high-k transistors, and interpreted as electrostatic improvement induced by the negative capacitance effect. It concludes that negative capacitance can not only improve the device performance in the on- and off-states, but also suppress the noise of the devices.

4.2 LFN Measurements on Ge NC-FinFET and Ge NW Fe-FET

As mentioned in chapter 1, Ge is one of the most superior candidates for future semiconductors devices to replace Si in CMOS technology, many research groups have reported a high performance Ge devices with various fabrication processes and device structures [62, 81–83]. However, an advanced gate stack with minimal channel/insulator interface imperfections are still in demand of progressive fabrication enhancements to lower the power dissipation resulting from poor interface quality. In parallel to interface quality, there are works that have reported Ge FETs with sub-60 mV/dec characteristics [84,85]. Integrating Ultrascaled Ge FinFETs with ferroelectric insulator however, have only been reported recently by Chung et al. [86]. FE HZO film was grown on the Ge p-type and n-type FinFETs and by integrating HZO in Ge MOSFETs a voltage hysteresis in the transfer curve of the transistor may occur due to the hysteretic nature of the FE oxide. A negative capacitance FET with near zero voltage hysteresis could be created, and Ge pFinFET with relatively large hysteresis as Ferroelectric field-effect transistor (Fe-FET) is realized too. A minimum of 7 mV/dec SS and Bi-directional sub-60mV/dec SS down to 43 and 41 mV/dec for both n- and pFinFET was observed.

The fabrication process begins with solvent and acid cleaning of a 400 nm thick Si subtract and 100 nm Ge (100) on top as a Germanium-On-Insulator substrate (GeOI), p-type and n-type ion implantation, and channel recess and fin definition. Then e-beam lithography is conducted for device patterning followed by 1 nm ALD Al_2O_3 as the control layer for post oxidation process that occurs during RTA at 500 ^oC in O_2 atmosphere for 30 seconds. A nanometer-thin GeO_x is formed below Al_2O_3,

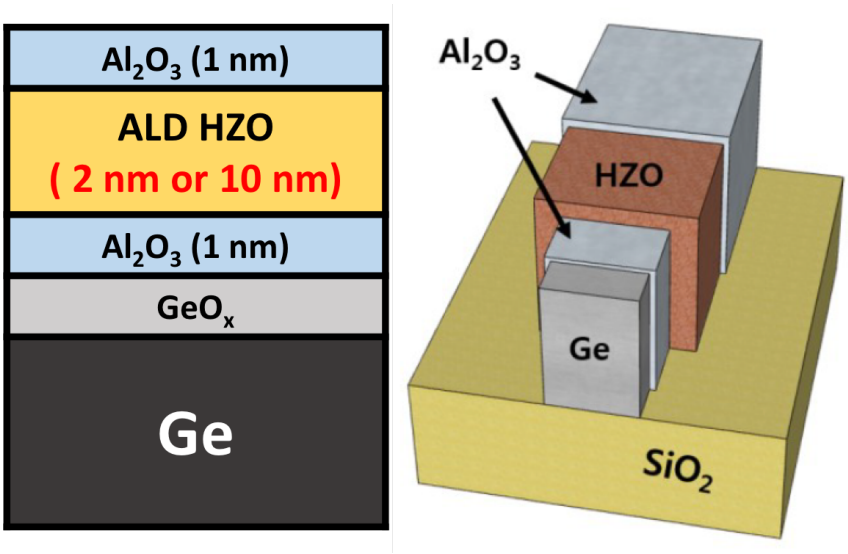

Fig. 4.21. Schematic structure of the Ge FinFET with 1nm $Al_2O_3/Hf_0.5Zr_0.5O_2$/1nm Al_2O_3 as gate insulator after ref. [86].

this layer was reported to have a significant positive impact on the quality of the Ge MOS interface [62]. HZO film was deposited with ALD at 250 ^oC by alternating Hf and Zr precursors. Another in situ Al_2O_3 capping layer was deposited, and the gate stack was RTA annealed at 500 ^oC in N_2 for 60 seconds. The last step is essential to activates the ferroelectricity of HZO film which was confirmed by the hysteresis loops in a P-V (or P-E) measurements as shown in Fig.4.22. Then Ni/n-Ge and Ni/p-Ge Source/Drain contacts was defined and Ohmic annealed (250 ^oC for 30s in N_2) followed by gate metalization. The schematic structure of the Ge NC FinFET is described in Fig.4.21.

The polarization versus voltage (P-V) was measured directly utilizing a ferroelectric analyzer as shown in Fig.4.22. The clearly seen hysteresis with voltage sweep range of $\pm$4V confirms the FE property of the 500 ^oC annealed HZO film. Coercive field (E_c) of 1.8 MV/cm and remnant polarization (Pr) of 22 $\mu C/cm^2$ are read from the same figure.

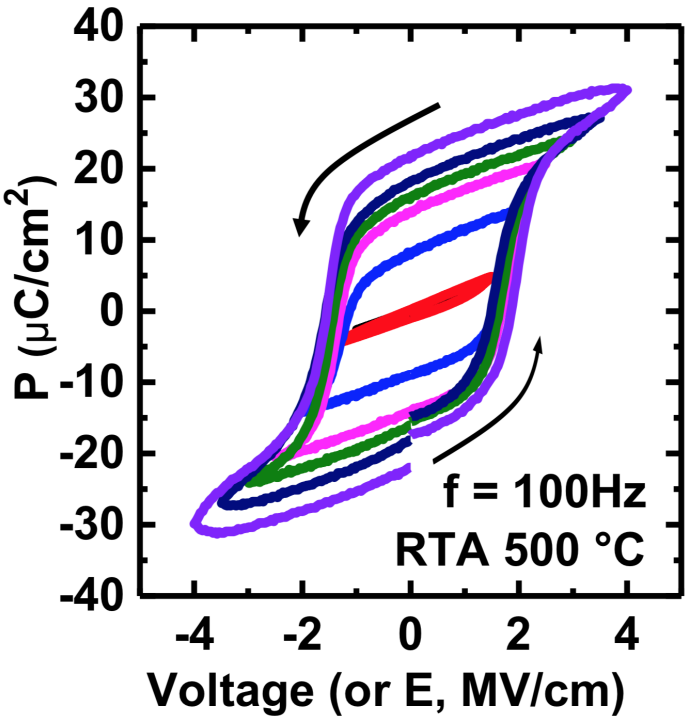

Fig. 4.22. Measured P-V (or P-E) of 10 nm HZO film for different voltage sweep ranges. after ref. [86].

Realizing a hysteresis-free I-V characteristics requires a carefully measured combination of positive and negative capacitance in order to compensate the energy barrier in the W-like energy (U) profile of the FE film in Fig.4.23 [87, 88].

Chung et al. (2017) [86] reported a hysteresis-free Ge NC-FET for CMOS, and a Ge FeFET for potential non-volatile memories applications. Fig.4.24 shows the I_D-V_{GS} characteristics of both NC-FinFETs (n-, and, p-type). Fig.4.25 show the Ge FeFET with with large hysteresis of about ∼4.3 V. ΔV_T is the voltage hysteresis value from forward to reverse. If traps in the channel/oxide interface dominate then ΔV_T is clockwise for NMOS and counter clockwise for PMOS, if the ferroelectric polarization effect dominates, ΔV_T will be in the opposite direction.

Due to the scaled nature of this device however, low-frequency noise measurements is again the proper choice to characterize and optimize the device performance due

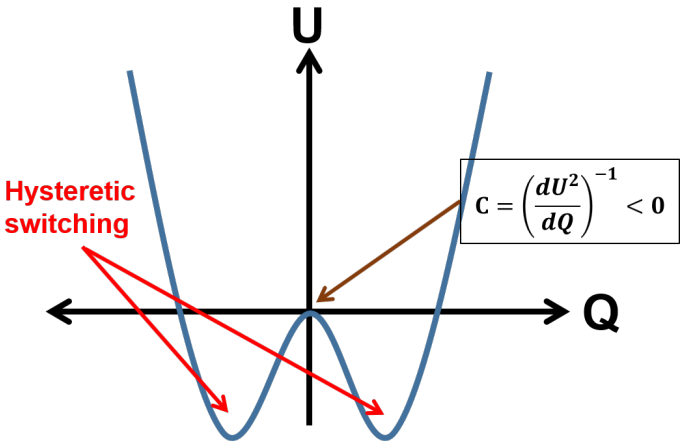

Fig. 4.23. Energy (U) vs. charge (Q) profile of FE film shows the origin of voltage hysteresis in a NC-FET. Compensation of the energy barrier is needed for hysteresis-free device [88].

to the fact that it can be done regardless of the small gate capacitance or the floated-body channel, not to mention that low-frequency noise could drastically affect the performance of scaled non-volatile memories and CMOS circuits that these Ge devices are intended for. Several groups have reported a low-frequency noise studies in long-channel Ge MOSFETs [89, 90]. Recently, W. Wu et al. have reported the first observation of RTN in Ge nanowire (NW) nMOSFETs [82], and the low-frequency noise study in Ge NW nMOSFETs with sub-100-nm channel length [91]. However, LFN analysis in negative capacitance and ferroelectric FETs with Ge as transistor channel is not yet reported. In this section the low-frequency noise is studied in Ge NC-FinFET and Ge NW Fe-FET for the first time.

In a similar analysis to low-frequency noise measurements in MoS_2 NC FinFETs, LFN and associated Hooge parameters was studied in Ge NC FinFETs and Ge pFe-FETs with two different gate stacks. The noise measurements set up and methods are identical to that described in MoS_2 LFN measurements in section 4.1 above using Keysight B1500/B1530A system at room temperature.

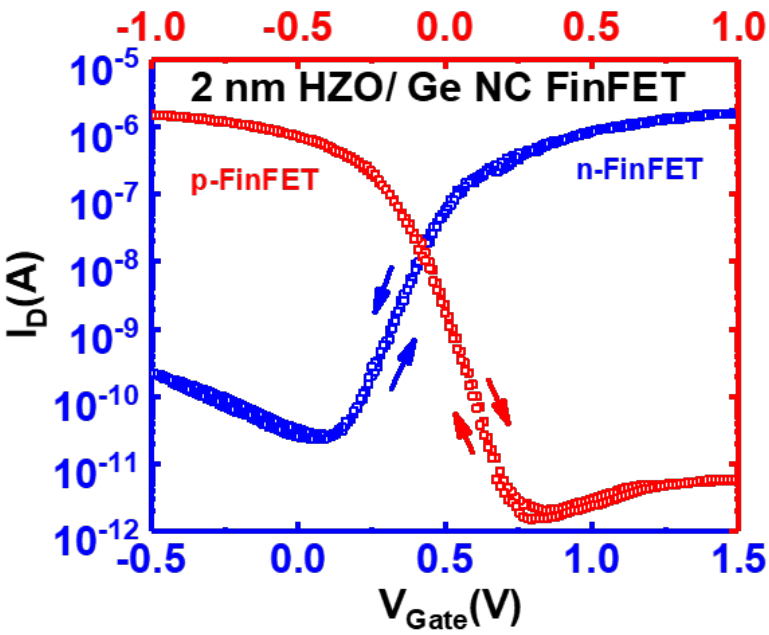

Fig. 4.24. $I_D - V_{GS}$ Characteristics of 2 nm HZO Ge NC pFinFET and nFinFET with a negligible gate voltage hysteresis, refer to 2017 IEDM reference [86] for SS<60 mV/dec.

The power spectra density of drain current fluctuation (S_{ID}) is calculated from the measured I_D after the application of a gate voltage for different timings. Fig.4.26 show the current vs. time characteristics of Ge NW Fe-FET with L_{ch}=60 nm, W_{ch}= 42 nm, and channel thickness T_{ch}= 26 nm, and Fig.4.27 shows S_{ID} of the same device over a range of gate voltages. It was found that LFN in both Ge NC-FET and Fe-FET follow the typical $1/f$ noise characteristics at gate voltages where no RTN is observed, and follow the Lorentzian spectrum $1/f^2$ when RTN signal is observed, similar to results in ref. [91]. The $1/f$ noise in Ge NC-FET and Fe-FET could originate from the carrier number fluctuation (CNF) near the channel/oxide interface or from the carrier mobility fluctuation (CMF) within the channel itself.

To examine the noise source in the three samples under test, namely, n-channel and p-channel Ge NC FinFET, and p-channel Ge NW Fe-FET, a normalized PSD

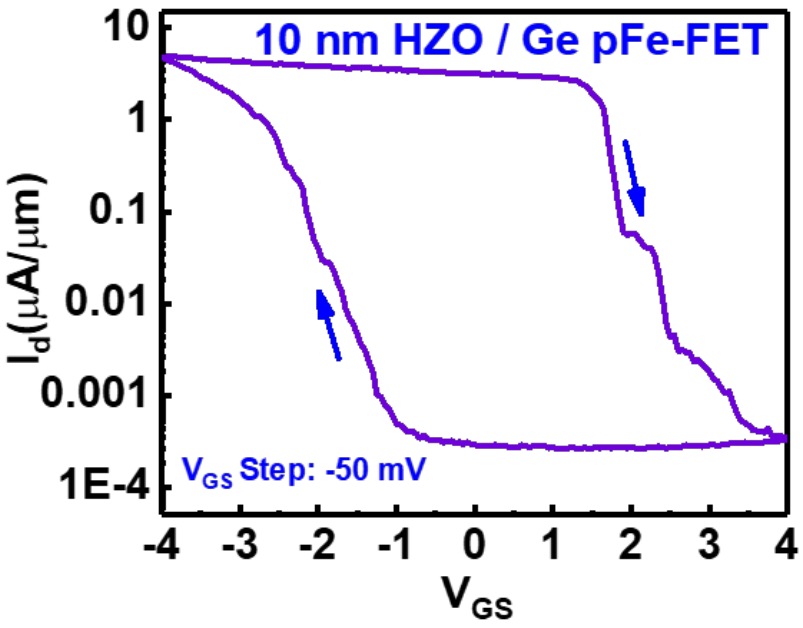

Fig. 4.25. $I_D - V_{GS}$ characteristics of 10 nm HZO Ge pFe-FET with $\sim$ 4.25 V hysteresis.

S_{ID}/I_D^2 should be plotted as a function of I_D at single frequency (10 Hz is chosen for all results). In general, CMF states that S_{ID}/I_D^2 will be linearly proportional to $1/I_D$, while CNF states a $1/I_D^2$ proportionality. Fig.4.28 shows S_{ID}/I_D^2 vs I_D in Ge NC nFinFETs. In this figure S_{ID}/I_D^2 is linearly proportional to the $1/I_D$. This indicates that CMF is the main source of the $1/f$ noise in n-channel Ge NC FinFET. This conclusion agrees well with the the conclusion deduced before in [91] with similar noise levels. The difference between the tow results is that the channel length scaliing in this work complies with Hooge's model in eq.4.3. And according to Hooge [92] and Ghibaudo [93], we can use the eq.4.3 to correlate it with noise results to find Hooge's parameter value:

$$\frac{S_{ID}}{I_D^2} = \frac{q\alpha_H \mu_{eff} V_{ds}}{f L_{ch} I_D} \tag{4.3}$$

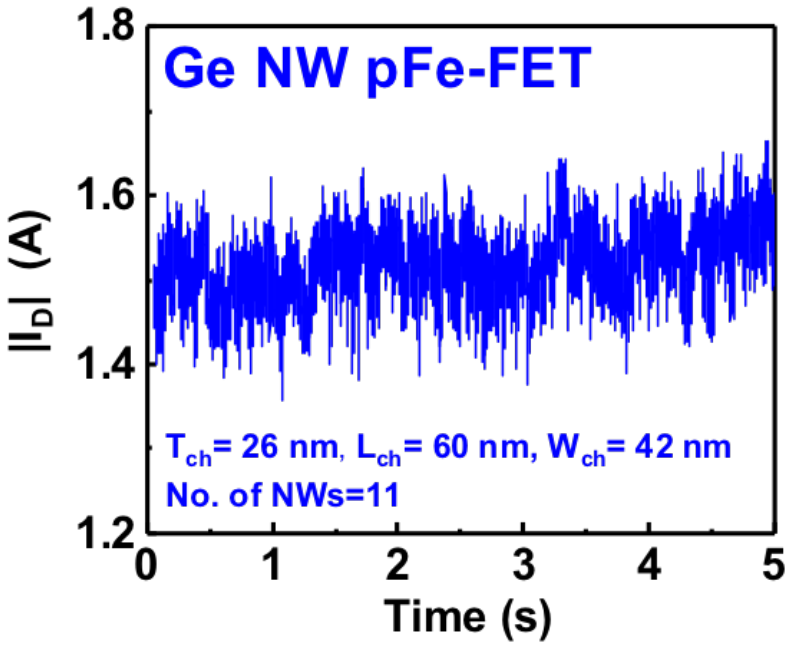

Fig. 4.26. I_D vs. time characteristics of 10 nm HZO Ge pFe-FET that has the $I_D - V_{GS}$ in Fig.4.25.

Where q is the electron charge, α_H is Hooge's parameter, μ_{eff} is the carriers' effective mobility. Using the value of 200 cm^2/V.s for μ_{eff}, and 50 mV V_{ds} (true throughout the measurements in this section), and f of 10 Hz, $\alpha_H \approx 2.6 \times 10^{-3}$, similar to the value calculated in [91]. RTN signals was also observed but not included in this section.

Ge is known to have higher hole mobility, thus, carrier mobility fluctuation in a p-channel Ge devices may not be the dominated source of noise. Fig.4.29 depicts a normalized PSD by channel length and width ($W_{ch}L_{ch} * S_{ID}/I_D^2$) vs I_D in p-channel Ge negative capacitance FETs with two different HZO thicknesses. S_{ID}/I_D^2 in both devices deviates from linear dependence and is proportional to I_D^2, hence, the $1/f$ noise in p-channel devices in this study origins from carrier number fluctuation. As we have reported before that a thicker ferroelectric insulator would enhance the noise

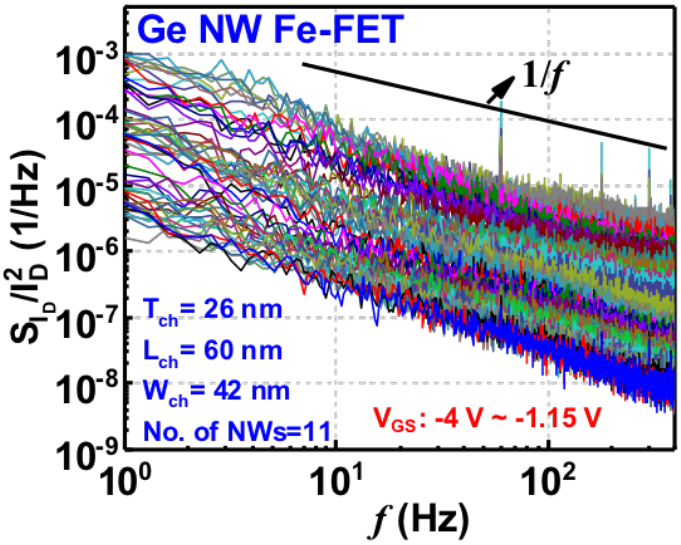

Fig. 4.27. Normalized S_{ID}/I_D^2 vs. frequency characteristics of 10 nm HZO Ge pFe-FET. A clear $1/f$ dependence is found.

performance and result in lower CNF noise in NC-FETs [94]. Ge NC-FinFET with 10 nm HZO film has lower noise level than devices with 2 nm HZO, in agreement with the noise study in section 4.1.

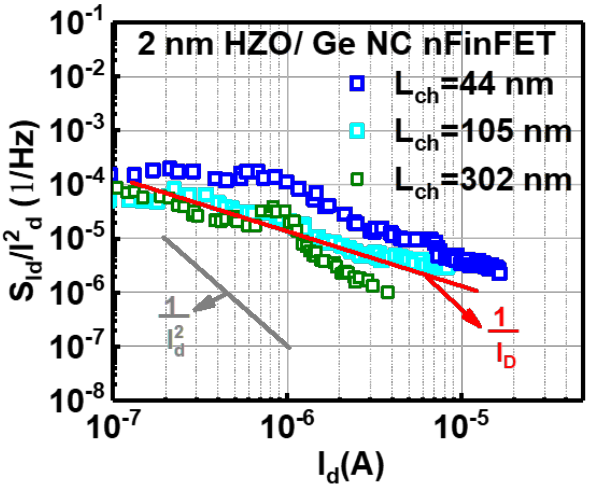

Fig. 4.28. Normalized S_{ID}/I_D^2 vs. I_D characteristics of Ge nFin-FET with 2 nm HZO in the gate dielectric. A linear dependence with $1/I_D$ which indicates carrier mobility fluctuation is the source of $1/f$.

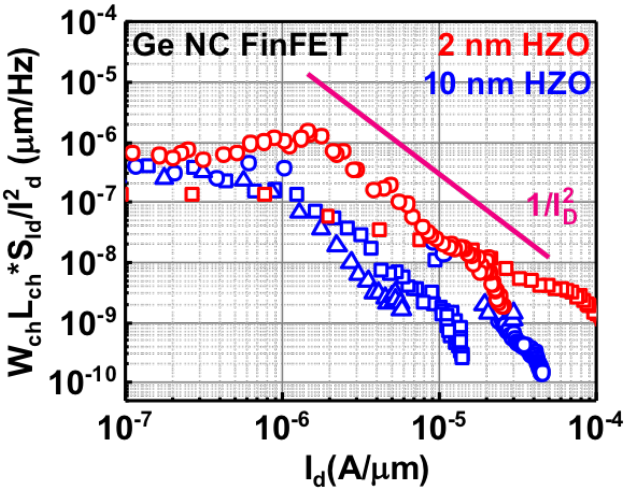

Fig. 4.29. Normalized S_{ID}/I_D^2 vs. I_D characteristics of two p-channel samples, Ge NW Fe-FET and Ge NC FinFET sharing the same 10 nm HZO in there gate dielectrics. The $1/f$ noise deviates from linear dependence and is proportional to I_D^2, indicating a carrier number fluctuation as the noise source.

By choosing the 10 nm HZO, noise levels of two different devices, Ge Ferroelectric FET and Ge negative capacitance FET, is compared in Fig.4.30. Fig.4.30 shows $W_{ch}L_{ch} * S_{ID}/I_D^2$ vs I_D in p-channel Ge Fe-FETs and Ge NC-FinFETs. Noise in both devices deviates from linear dependence as in Fig.4.29 and is proportional to $1/I_D^2$. The $1/f$ noise source in these devices, including Ge NW Fe-FET, is confirmed as CNF. Also, noise level in Ge NW Fe-FETs is higher than noise in NC-FinFETs. This could be due to the additional current fluctuation that occurred by the internal reversal (or un-reversal) mechanism of the ferroelectric polarization switching.

This has led me to study the time response of polarization switching in Ge HZO NW Fe-FETs. The following chapter (Chapter 5) explains in details the transient response of the polarization switching to an external electrical field.

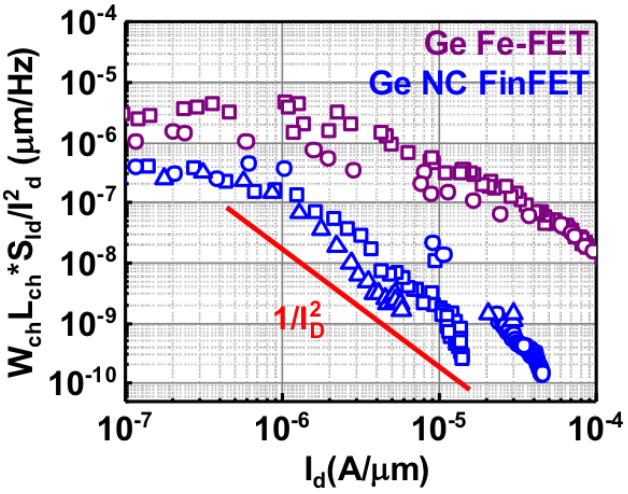

Fig. 4.30. Normalized S_{ID}/I_D^2 vs. I_D characteristics of two p-channel samples, Ge NW Fe-FET and Ge NC FinFET with 10 nm HZO in there gate dielectrics.

5. RELIABILITY ISSUES WITH FERROELECTRIC HAFNIUM ZIRCONIUM OXIDE (HZO)

5.1 Introduction

A mix of Hafnium Hf_x and Zirconium (Zr_{1-x}) Oxide ($Hf_xZr_{1-x}O_2$) fabricated in thin films proved to have a variety of of ferroelectric phase stability, which opened door to the possibility to adapt the potential of the material properties for wide range of applications [72, 95, 96].

Negative-capacitance field-effect transistors (NC-FETs), ferroelectric field-effect transistors (Fe-FETs), ferroelctric memories and other variety of other application-oriented devices realized by this ferroelectric films as gate insulators, have been extensively studied recently as a potential replacement to metal-oxide-semiconductors field-effect-transistors (MOSFETs) in digital logic and for non-volatile memory applications. Steep-slope NC-FETs have attracted a lot of attention to break the physical limit of Boltzmann of subthreshold swing (SS) in MOSFETs, where hysteresis-free sub-60 mV/dec NC-FETs at room temperature have been demonstrated very recently by static DC measurements [7, 86, 97].

In the previous chapter, we discussed the existence of the negative capacitance in NC-FET devices and the positive impact of the matched FE insulator and linear dielectric oxide on the electrostatic control of the channel. In the aforementioned study, LFN measurements was used, where NC-FETs was under a long electric filed stress for more than 50 seconds for instance in order to measure the noise created by this field. In this chapter, however, another major concern in NC-FETs and FeFETs is the operating speed, which might be limited by the slow polarization reversal in ferroelectric films due to heavy atom re-positioning [72, 98]. A Fe-FET is a proper structure to study the ferroelectric switching speed due to the very pronounced

counterclockwise hysteresis loop in its transfer curve, and it is used as a detector to measure the switch speed of the ferroelectric gate.

5.2 Ferroelectric HZO Polarization Switching Speed

In this work, we reported on the studies of time response of polarization reversal using a Germanium nanowire (NW) Ferroelectric FET (Fe-FET) with hafnium zirconium oxide (HZO) as ferroelectric insulator by fast dual gate voltage (V_{GS}) sweep down to 10 μs for single sweep direction (forward or reverse) of +5 V to -5 V range with 0.2 V step. That is 200 ns per voltage step, which enables us to closely simulate the actual operation of the Fe-FET, as in a single transistor memory. The Ge Fe-FETs exhibit clear time-dependent ferroelectric hysteresis loop detected at shortest possible sweep time of 25 μs. The time response of polarization reversal leads to a voltage hysteresis and maximum drain current ($I_{D,Max}$) time-dependency in Ge NW Fe-FETs. Also, the ferroelectric switching speed is found to be related with the maximum electric field applied during the fast gate voltage sweep, suggesting the internal ferroelectric switching speed can be even faster depending on the device's electrical bias conditions.

Fig. 5.1 shows a 3D schematic of a Ge NW Fe-FET and Fig. 5.2 is the false-color SEM image of the device. The Ge Fe-FET under-test has 260 nm channel length (L_{ch}), 42 nm NW width (W_{NW}), 26 nm NW thickness (T_{ch}), and 11 nanowires in parallel. 1 nm Al_2O_3/10 nm HZO/1 nm Al_2O_3/GeO_x is used as the gate stack. The fabrication process is the same as in Ref [86] except NWs were released after fin structure pattering and before gate oxide deposition.

Fig. 5.3 shows the polarization vs. electric field (P-E) on a TiN/HZO/TiN capacitor. It shows a clear ferroelectric hysteresis loop and confirms the ferroelectric property of the film used in this work.

Fig. 5.4 depicts the $I_D - V_{GS}$ characteristics of a representative Ge NW Fe-FET biased at V_{DS} =-50 mV and measured using source measure unit (SMU), which is a

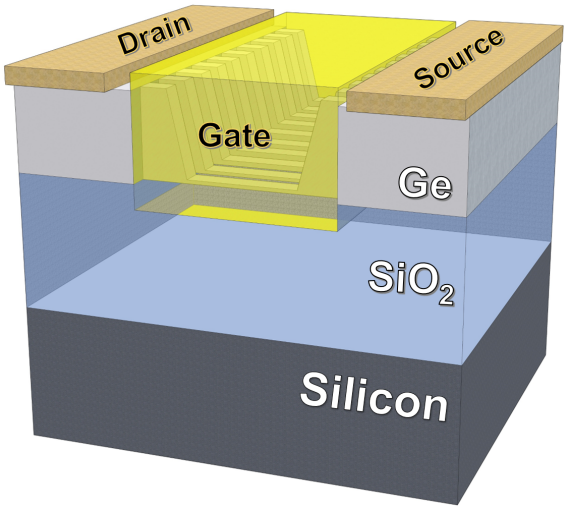

Fig. 5.1. 3D representation of the device structure of Ge NW Fe-FET.

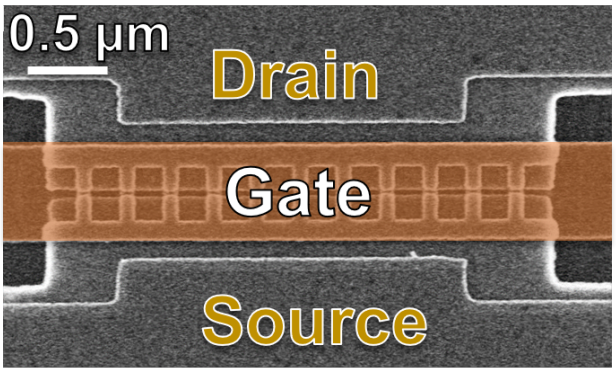

Fig. 5.2. False-color SEM image of a Ge NW Fe-FET

quasi-static slow DC measurement (typically takes more than 30 seconds to measure). The forward sweep begins at +4 V gate voltage with 200 mV step, down to -4 V and switches from OFF-state to ON-state at -0.8 V. At the reverse back sweep, the ON current starts high at 23 μA/μm and held constant until it switches OFF at +1 V with voltage hysteresis of ΔV= -4.2 V, where:

$$\Delta V = V_{GS,forward} - V_{GS,reverse} \tag{5.1}$$

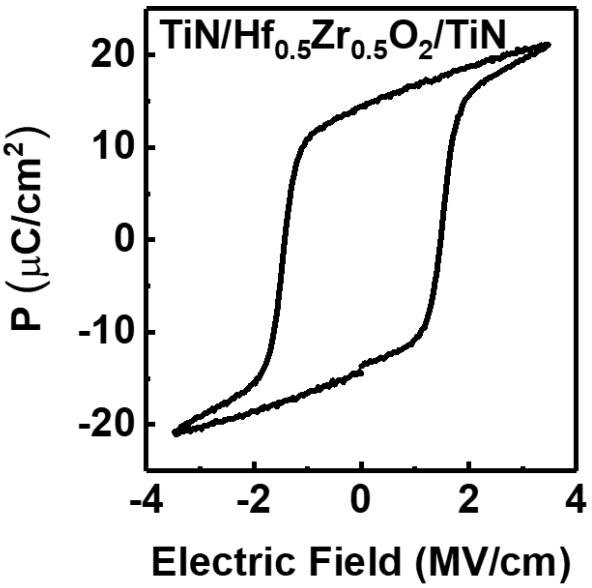

Fig. 5.3. P-E Measurement of 23 nm HZO film annealed at 500 ^{o}C with clear ferroelectric property.

This device was then systematically measured using a Keysight B1530A WGFMU with remote sensing unit to serves as an very sensitive amplifier. The time chart of the gate voltage sequence set-up of this measurements is illustrated in Fig. 5.5. The fast gate voltage sweeping measurements started with minimum measurements speed of 100 ns per sweep for different gate voltage ranges, and V_{DS} is kept at constant -50 mV. No switching was detected. Then the sweeping speed is incrementally increased until 25 μs per one sweep direction.

Figs. 5.6, 5.7, and 5.8 shows the $I_D - V_{GS}$ characteristics at different sweep speeds for $\pm$5 V, $\pm$5 V, and $\pm$5 V gate voltage sweep ranges, respectively. The relatively high off-state current is due to the short integration time in the high-speed measurement, which is not the real off-state current but will not affect the on-state measurement and the conclusion in this work.

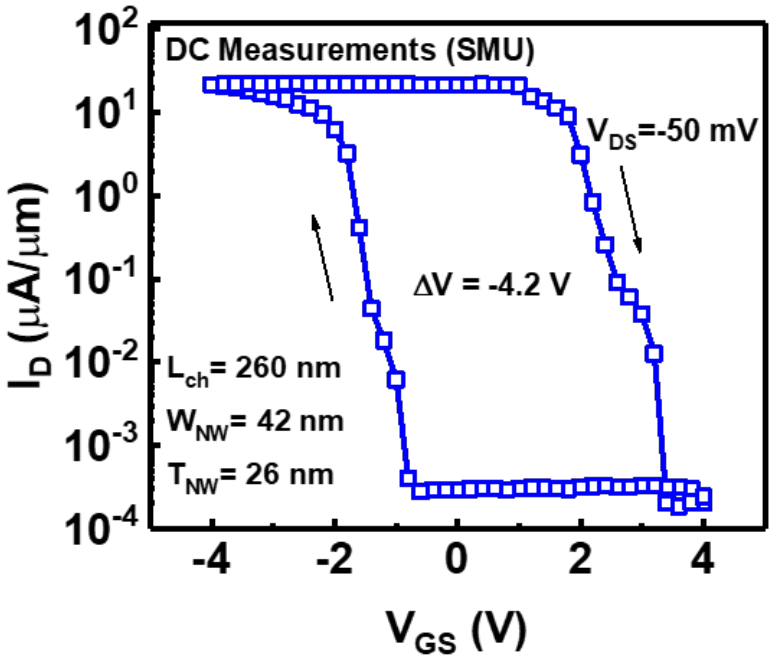

Fig. 5.4. DC transfer characteristics of a Ge nanowire Fe-FET, measured using standard SMU.

From Fig. 5.6, it is found that the ferroelectric I-V hysteresis loop in the Ge NW Fe-FET has larger hysteresis and and lower $I_{D,Max}$ with faster gate voltage sweep, as summarized in Fig. 5.9. The increase of hysteresis and reduction of $I_{D,Max}$ occurred because the polarization reversal in the Fe-FETs is slower than the gate voltage sweeping. As a result, the Fe-FET turns on slower at higher voltages, and the HZO cannot be fully polarized within a short amount of time to reach maximum drain current. Similarly, the measurements with ±4 V and ±3 V (Figs. 5.7 and 5.8) as maximum gate voltage shows that the ferroelectric switching speed is related with the maximum voltage applied during the fast gate voltage sweep.

Fig. 5.10 depicts the maximum drain current measured for each voltage range at different sweep speed. It shows that the ferroelectric switching speed is related to the maximum voltage applied during the fast gate voltage sweep. The Ge Fe-FET shows

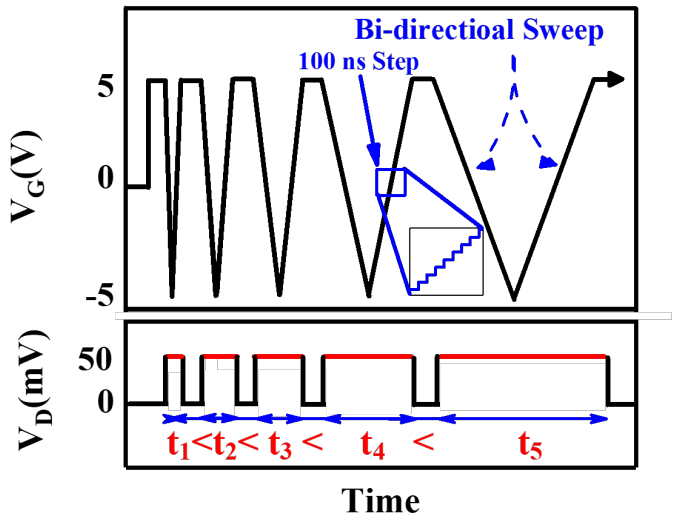

Fig. 5.5. Time chart of the applied voltage sweep with different sweep time for ±5V range.

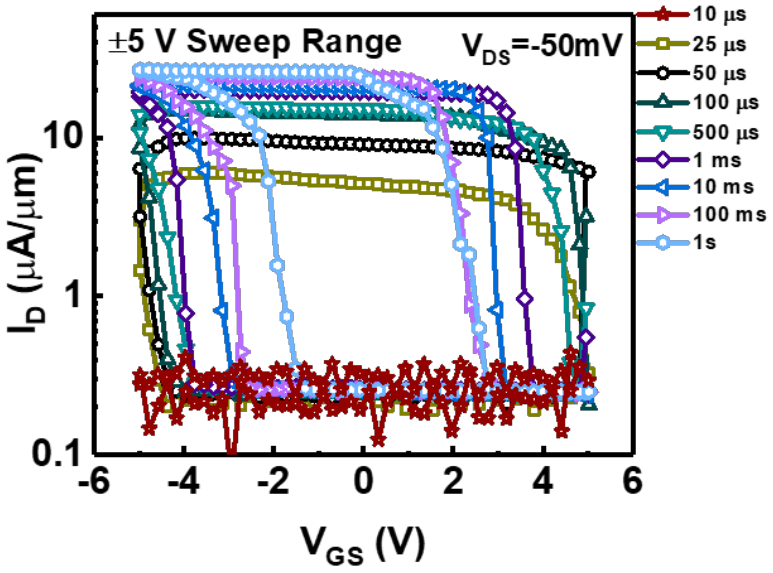

Fig. 5.6. Transfer characteristics of the same Ge nanowire Fe-FET as in Fig. 5.4, measured using fast voltage sweep at ±5 V range.

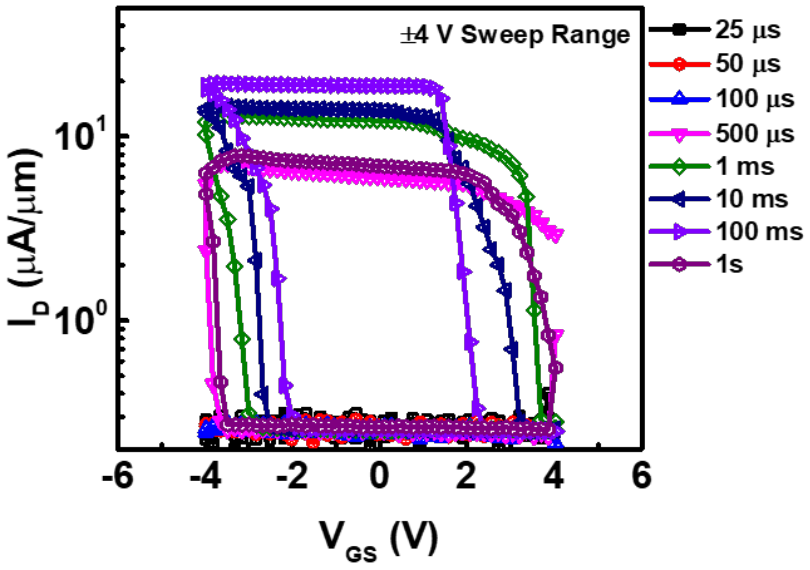

Fig. 5.7. Transfer characteristics of the Ge nanowire Fe-FET measured using fast voltage sweep at ±4 V range

clear ferroelectric hysteresis loop as fast as 25 μs per sweep for the ±5 V voltage range, while for ±3 V voltage range a hysteresis loop could only be obtained at 10 ms of sweeping time. The slow response in low voltage sweep range is partly related to the RC delay in gate voltages (however, the time constant (RC delay) in our set-up (without the device being connected) was obtained using function generator and oscilloscope and it less than 10 ns, which is faster than the minimum of step delay allowed by the system) and The internal ferroelectric reversal can be faster than all measurements in this work.

In this respect, a shorter time response measurement were very recently reported by our group (Wonil et al accpeted at VLSI 2018 [99]) on the same device with L_{ch}=100 nm, W_{NW}=32 nm, and T_{NW}= 26 nm.

Picosecond pulses were sought to be analyzed and measured using the setup shown in Fig.5.11, where AVTECH pulse generator (PG) was used and triggered by the Agilent 81110 PG with a period of 2 μs. Then, a Lecroy oscilloscope with sampling

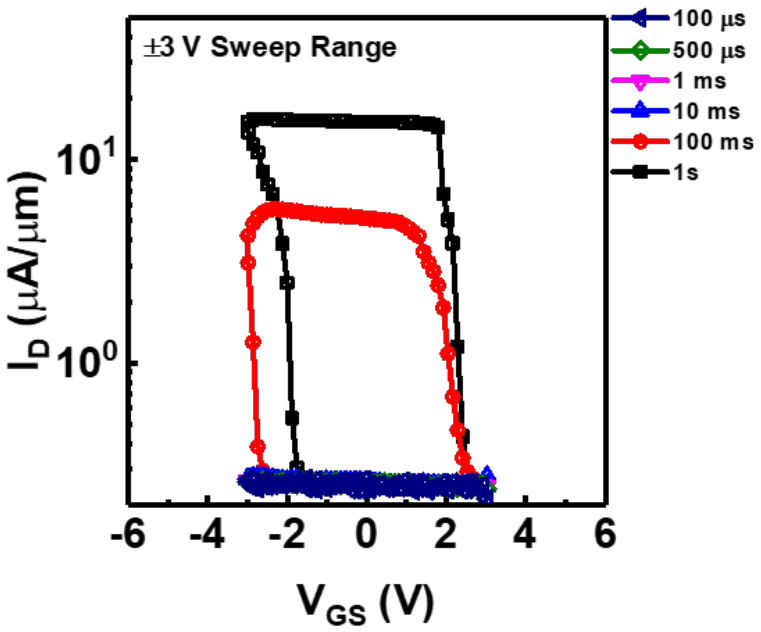

Fig. 5.8. Transfer characteristics of the Ge nanowire Fe-FET measured using fast voltage sweep at ±3 V range

capabilities of 80 GS/s was used as a real time monitoring equipment for the sub-nanosecond pulses. Multiple gate voltages (V_G) (-1 ∼ -10V) were applied on the gate in the form of various pulses and pulse widths while the change in polarization current (I_D) was closely and accurately monitored using the above mentioned oscilloscope and through a current amplifier. V_G and drain voltage (V_D) were held at 0 V and -50 mV, respectively, in between pulses. The results in Fig. 5.12 shows that it takes much shorter time to switch the polarization when the V_G pulse approaches -4 V.

As pulse width was decreased to sub-μs regime, transient current fluctuation was observed when the polarization switching occurred as seen in Figs. 5.12 (a) and (b). Therefore, the current was read after stabilization to ensure it was the current caused by changed polarization state only. At higher V_G (-5 ∼ -10 V), sub-10ns switching was also observed directly by experiment and it switched fastest at V_G = - 10 V as shown in Fig. 5.13. Off-state current was plotted at t = 1 ns to show clear I_D

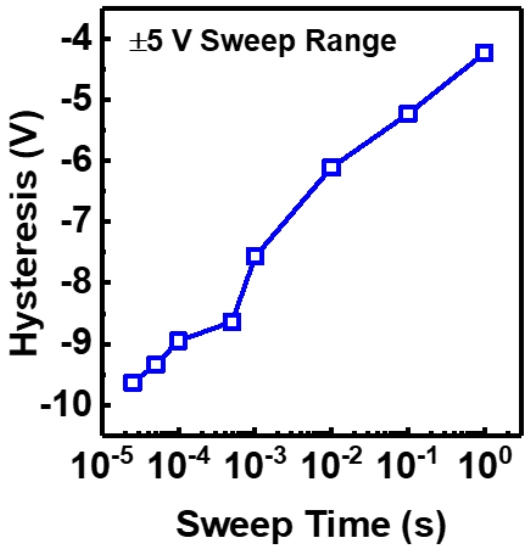

Fig. 5.9. Hysteresis versus sweep time extracted for ±5 V gate voltage range. Hysteresis increases with faster sweep time.

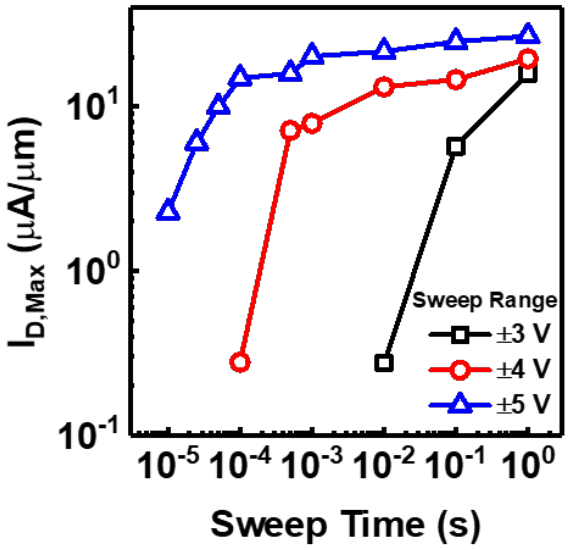

Fig. 5.10. Maximum drain current versus sweep time for different ranges of gate voltage sweep.

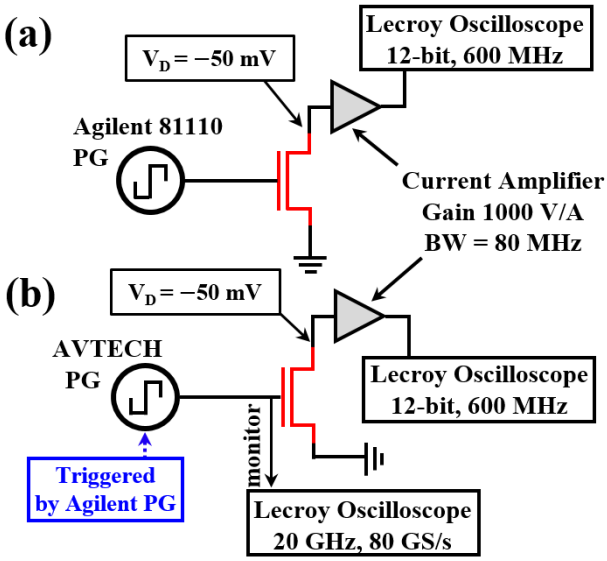

Fig. 5.11. Ultrafast pulse generation and measurement set-up for (a) pulse widths > 3.6 ns and (b) picosecond pulses. [99]

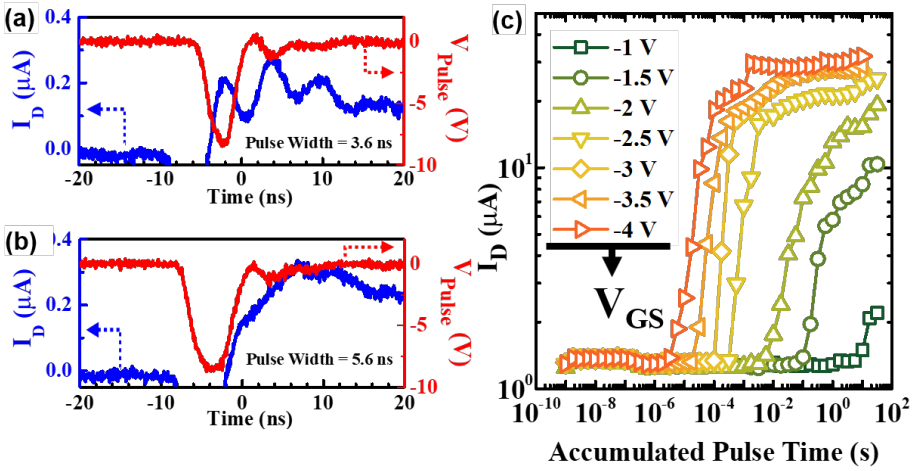

Fig. 5.12. Polarization current (I_D) over (a), (b) single and (c) accumulated pulse time with different V_G pulses. Keysight B1530A was used for (c). [99]

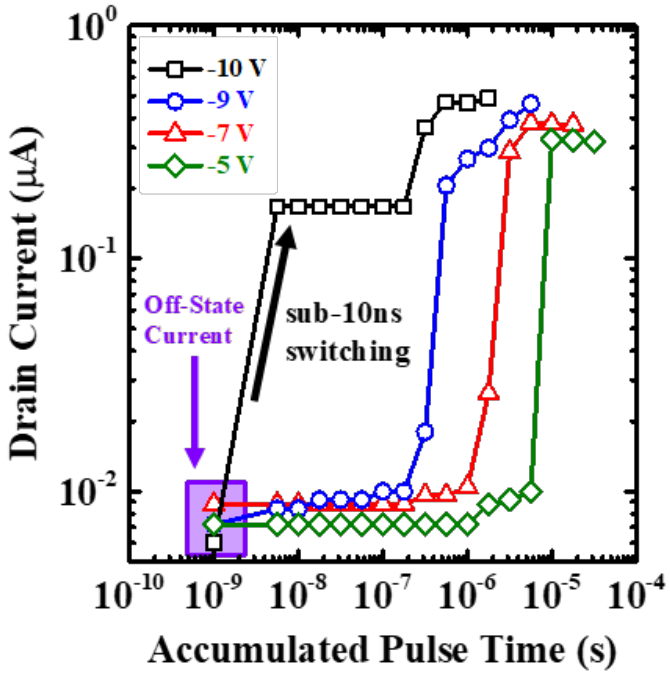

Fig. 5.13. V_G was pushed down to -10 V to probe the polarization switching limit which showed minimized time under 10 ns. Off-state current was plotted at 1 ns for reference. [99]

transition from off to on-state. The fastest switching by a single pulse observed in our Ge FeFETs with 10 nm HZO was 3.6 ns. Considering the RC delay present in the measurement set-up and the large probing pads, the intrinsic time response of polarization is expected to be even faster than 3.6 ns.

Conclusion

In summary, the time response of polarization reversal in Ge NW Fe-FETs are characterized by fast gate bias dual sweeps. The Ge NW Fe-FETs exhibit clear time-dependent ferroelectric hysteresis loop starting from 25 μs. The time response of polarization reversal leads to time-dependent hysteresis and maximum drain cur-

rent in Ge NW Fe-FETs. The ferroelectric switching speed is found to be related with the maximum voltage applied during the fast gate voltage sweep. The internal ferroelectric switching speed could be faster and depends on the applied electrical field.

5.3 Ferroelectric HZO Polarization Switching Mechanism

Ever since the ferroelectricity HZO was introduced in 2010 [72, 100], there has been a tremendous interest in this material. The scalability and compatibility with CMOS technology served a s solution for the new ferroelectric (FE) based devices. Most recent and promising devices that utilize ferroelectric insulator, and especially, HZO in the gate stack are Negative capacitance field-effect transistors (NC-FETs) as well as ferroelectric field-effect transistors, although device are not limited to these only. Previously we have discussed an example of the former in chapter 4 in term of noise reliability, and a representative device of the latter in this chapter but in terms of switching speed. From these devices and similar application we see the importance of combining a linear dielectric (DE) insulator in a bilayer gate stack in the gate structure of such devices. A linear DE layer is set to improve the interfacial characteristics (or isolate potential interfacial issues) between the semiconductor channel and ferroelectric insulator, this fits very well in the scope of this thesis. Also, having a linear dielectric would provide sufficient capacitance matching if the quasi-static negative capacitance (QSNC) concept is applied for the development of NC-FETs [18, 101]. It is worth noting that over the last years there has been a significant and fundamental misconception in understanding the difference between an FE/DE stack capacitor and a FE capacitor that is in series with DE capacitor. Therefore, an investigative study to help understanding the impact of the DE layer on the ferroelectric properties related to ferroelectric switching mechanism in Fe-FETs and NC-FETs is important. As investigated by M. Si et. al. [102] This section we will establish a discussion about an important attribute of the ferroelectric HZO related to the polarization switching

mechanism. The study was conducted by our group (Ref. [102]) using C-V and polarizationvoltage (P-V) measurements on four types of FE/DE capacitor structures: (a) TiN/Al_2O_3/TiN (type A), (b) TiN/HZO/TiN (type B), (c) TiN/Al_2O_3/HZO/TiN (type C), and (d) TiN/Al_2O_3/TiN/HZO/TiN (type D), as depicted in Fig.5.14.

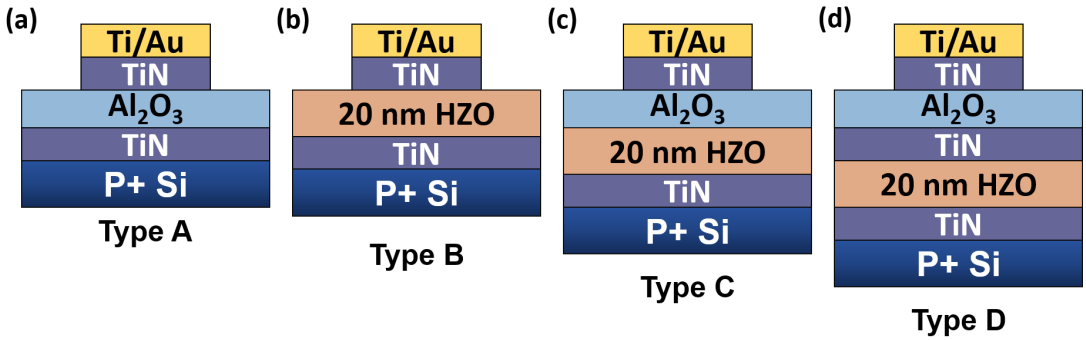

Fig. 5.14. Capacitor structures used to study switching mechanism in Si's study [102]. (a) Al_2O_3 only (type A), (b) HZO only (type B), (c) Al_2O_3 and HZO stack without internal metal (type C), and (d) Al_2O_3 and HZO stack with TiN layer as the internal metal (type D).

The C-V of capacitors of type (A) showed (not listed here) a typical dielectric C-V with extracted dielectric constant of 8, which is the typical value of Al_2O_3. The measured C-V and P-V of a type B capacitor with 20 nm HZO (also not shown here) have showed the two signature peaks and the CV hysteresis loop indicating a ferroelectricity characteristics. The focus of this section is, in fact, type C capacitors, with Al_2O_3 thicknesses of 0, 4, 6, 8, 10, and 20 nm. The interest in this structure will perpetuate on to the next section when we study ferroelectric polarization endurance.

Fig. 5.15 shows C-V measurements for type C capacitors measured at 10 kHz. From the first glimpse it is apparent that as the Al_2O_3 layer gets thicker a significant decrease in the capacitance occur (Fig. 5.15(a)), as well as gradual disappearance of the two signature ferroelectricity peaks up until the 20 nm HZO/20 nm Al_2O_3 stack, implying a reduction of ferroelectricity in the thick DE layer and FE layer stack. This effect is more pronounced in Fig. 5.15(b), where the PV measurements shows a

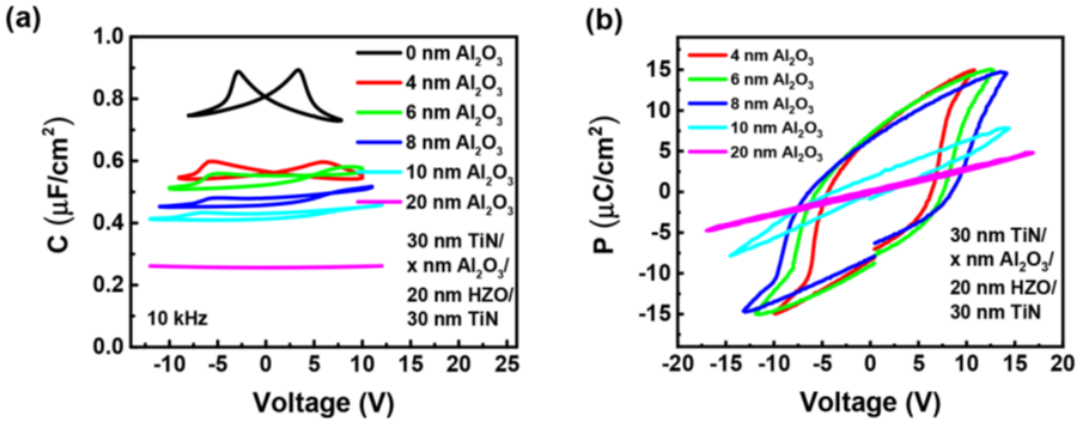

Fig. 5.15. (a) CV measurements and (b) PV measurements on type C capacitors with different Al_2O_3 thicknesses and 20 nm HZO. (c) PV measurements on a type C capacitor with 6 nm Al_2O_3 and 20 nm HZO at different voltage sweep ranges [102].

considerable decrease of remanent polarization (P_r) during the P-V hysteresis loops. P_r is gradually decreases for 4 nm Al_2O_3 through thicker layers, until it disappears in 20 nm Al_2O_3. In this study, this phenomena is attributed to the leakage current and the interfacial charges. Referring that to the difference between the maximum charge in DE (typical $Al_2O_3 \approx 7\mu C/cm^2$) and the remanent polarization in FE (in the range of 10-30 $\mu C/cm^2$) with a sufficient charge balance still exists. The impact of leakage current in FE/DE bilayer was also reported, and the interfacial charging is accepted to be important in the ferroelectric switching process by a thermodynamic free energy model [103–105]. The study goes further into a simulation of these findings, readers referral to this paper is recommended when a positive external voltage (V_{TOT}) is applied and explains why the leakage current is believed to be the source of charge compensation. Form this figure, and if there is no leakage current, charges in DE layer (Q_{DE}) must be the same as the charge in FE (Q_{FE}), which is not the case as discussed. But with leakage current, there is a critical electrical field (E_{effect}) assumed to be constant independent of DE thickness and charge carried by the leakage current

will be trapped at the FE/ DE interface as Q_{it}. In the equilibrium condition, there is no charge exchange with zero current. Thus, the electric field in the DE layer will be pinned at the E_{effect}, and;

$$Q_{DE} = \epsilon_{DE} E_{effect} \tag{5.2}$$

And the charge balance is then described in the following equation;

$$Q_{FE} = Q_{DE} + Q_{it} \tag{5.3}$$

Thus, it is important that there exist a sufficient interface charges in order to see high Q_{FE} and the polarization switching process must be leakage-assist-switching.

To summarize, even though its practically important to have a gate stack of FE/DE whenever a thin FE insulator is utilized, the thickness of the dielectric layer is found to have crucial impact on the ferroelectric polarization switching of HZO. The remanent polarization is found to decrease with a relatively thick dielectric layers, and leakage current is proposed to be the cause of a full polarization switching in the ferroelectric layer in thin dielectric layer.

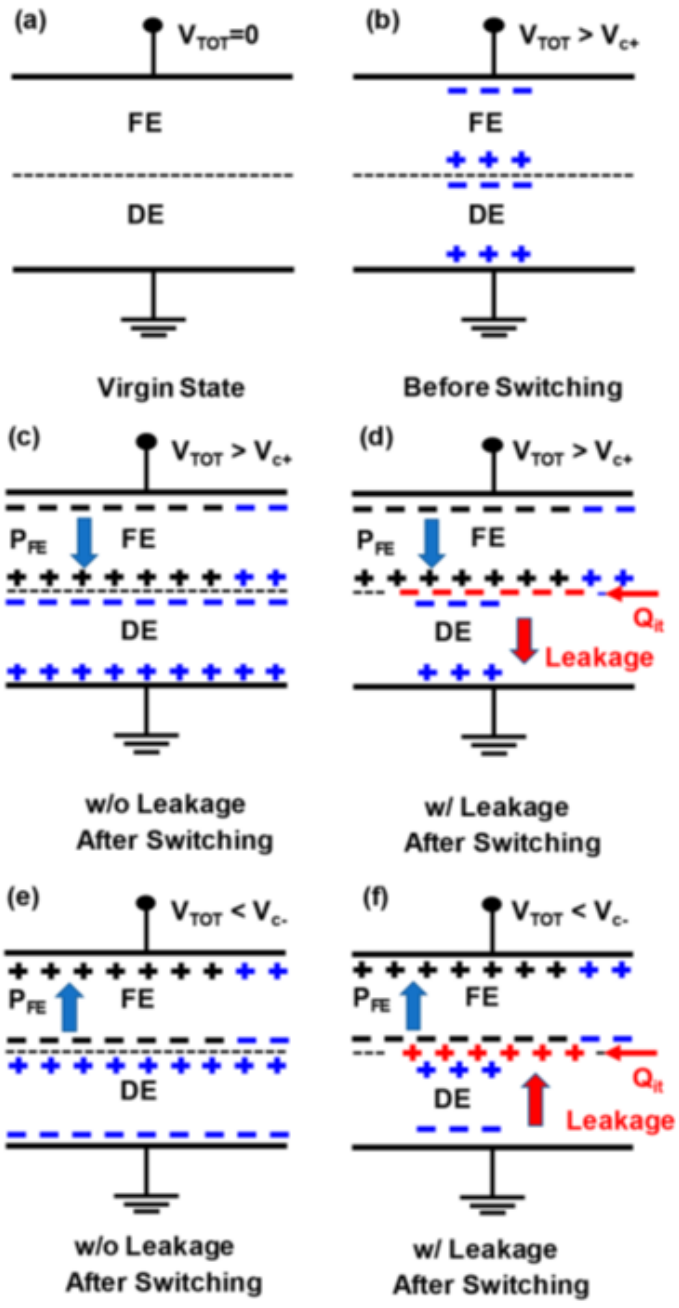

Fig. 5.16. Illustration of charge distribution in FE/DE stack explaining the leakage-assist-switching process is steps from (a) through (f). Refer to Ref. [102].

5.4 Ferroelectric HZO Polarization Switching Endurance

HfO_2-based ferroelectrics are set to solve two of the most critical issues refrain the commercialization of ferroelectric memories: down scaling (to provide CMOS integration), and providing better retention (compared to other ferroelectric memories). They though show some reliability concerns that are directly related to the memory window, such as polarization wake-up and fatigue. The origin of the degradation in the HZO endurance during the electric-field cycling is usually referred to the build-up/accumulation of traps large number of defects such as oxygen vacancies in the HZO films, which could drift to domain walls or ferroelectric/electrode interfaces resulting in polarization switching pinning or "Wall Pinning Mechanism", and the other scenario that explains the loss in polarization is called "seed inhibition mechanism" in which the switching ability of the domians seeds is restrained in the embryonic state of these seeds prior to the creation of any macroscopic domains. There is a third explanation called: "local imprint", this mechanism limits the switching locally at the ferroelectric/electrode interface. This mechanism is related to the electrostatic effect of charges trapped there, more details about both mechanism are explained in Ref. [106]. On that account, studying HZO endurance is important for the development of any memory devices since it is mainly a program/erase process.

5.4.1 Endurance Measurements

Endurance of a memory device in general is characterized by the ability of preserving stability of two or more distinct memory states (e.g. 0 state or 1 state in binary devices). This stability is required to have a retention period measured by number of program/erase cycles. In case of the ferroelectric HZO, a high filed bipolar stress cycling has a direct impact on the remnant polarization, where two phenomena are usually observed: 1) wake-up, and 2) Fatigue. During Wake-up effect, the remnant polarization memory window, associated with the voltage difference between positive and negative remnant polarization, gets wider with field cycling. Fatigue (or

aging) on the other hand, is the loss of the remnant polarization due to field cycling after number of cycles, and the memory window in this case gets narrower due to aging [106].

Measuring a sample's endurance (fatigue and wake-up), involve measuring the remanent polarization through a method called PUND measurements. PUND is a standard pulse measurement of five consecutive pulses described in Fig. 5.17. First pulse presets the sample to an initial polarization state, or initialization pulse. Second pulse is a switching pulse that switches the sample to the opposite polarization state and measures the switched polarization. The measurement here contains both Remanent and Non-Remanent polarization. The third pulse is a duplicate of the second but does not switch the sample and measures only Non-Remanent polarization components. The fourth and the fifth do the same as the second and the third but rather for negative polarization. Fatigue progression is characterized as a function of the log of the total number of stress cycles, in which each subsequent stress/measure cycle is by default of a longer time than the previous, hence, more cycles of stress signals are applied.

5.4.2 Experiments and Electrical Measurements

Considering the mechanism of the polarization switching discussed earlier, and reports on the reliability of the ferroelectric polarization switching by many researchers [108–113], the following study explores the polarization endurance of the FE HZO when integrated with linear dielectric oxide. Although that there have been several reports on HZO endurance, very limited to null studies the endurance of an integrated several-nanometers-thick DE with the FE HZO [96], utilized for for NC-FETs and FeFETs devices. This could be a deal breaker for the use of FE insulators in high speed memories or NC-FETs longevity. We anticipate that the incorporation of DE will improve the breakdown limits due to external electric field but may degrade the remanent polarization with increased number of polarization retention

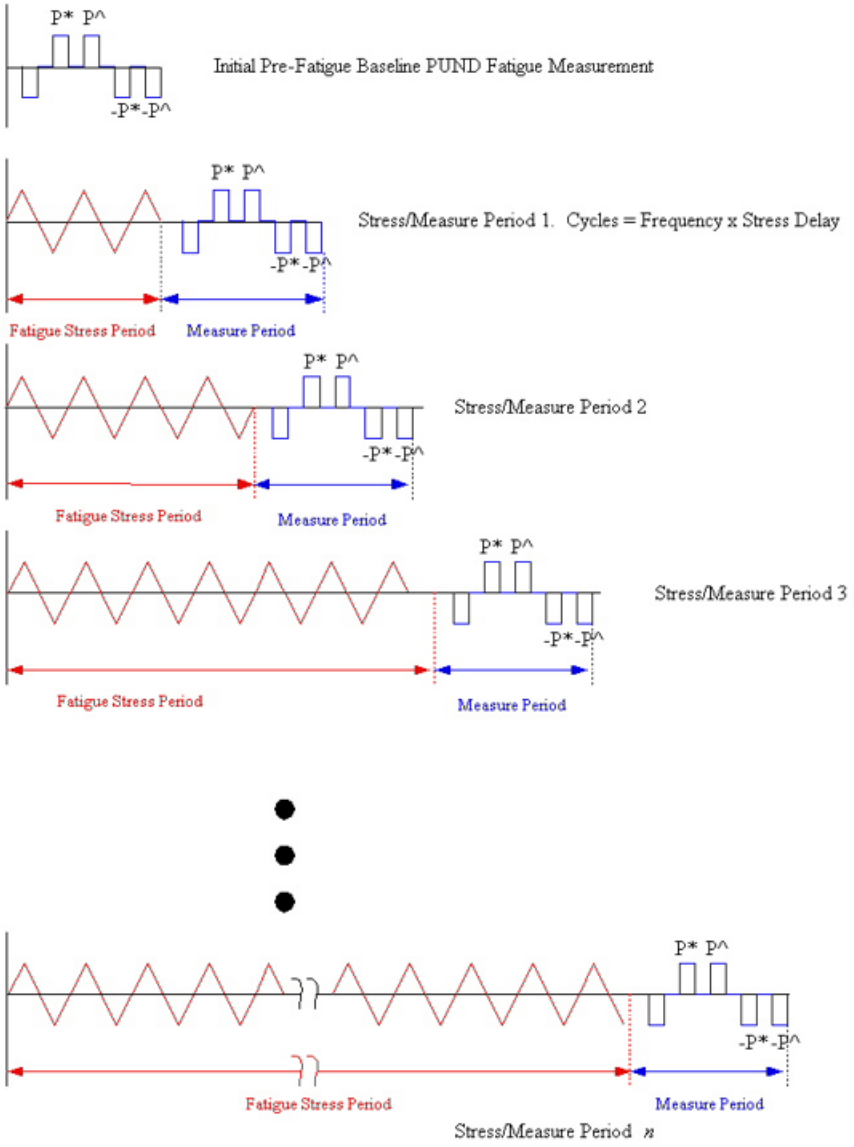

Fig. 5.17. The algorithm of endurance measurements using Radiant RT66C ferroelectric tester, Fig. taken from Ref. [107]

cycles. The physics behind such anticipation is not yet thoroughly investigated, however, it is believed that the tarpped charges induced electric field would oppose the fields created by the ferroelectric dipoles [96], which become more pronounced when more charges are being "pumped" (or leaked).

In this section of the thesis we study the endurance of HZO (serves as FE layers) on metal-insulator-metal (MIM) capacitors with various Al_2O_3 (serves as DE layers) thicknesses in order to see the effect of the Al_2O_3 on the retention properties of the FE HZO polarization. The MIM used here is the same as type C capacitor mentioned in section 5.3, depicted again in Fig. 5.18. Fabrication starts with 30 nm TiN deposited by ALD at 250 ^oC, followed by deposition of 20 nm $H_{1-x}Z_xO_2$ by ALD at 200 ^oC with $x = 0.5$, and x nm ALD deposition of Al_2O_3 (x= 4 nm and 6 nm). After that samples were thermally annealed at 500 ^oC in N_2 environment for 1 min by RTA, all on a heavily p-doped Si substrate.

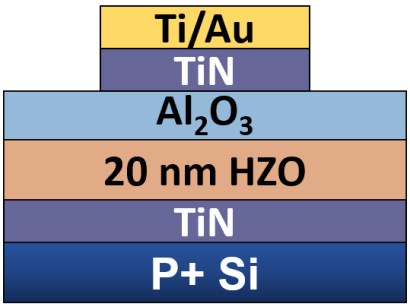

Fig. 5.18. Capacitor structure consisting of metal layers - DE layer - FE layer - metal and substrate

The electrical measurements begins with the P-V measurements of hysteresis loops, using Radiant RT66C ferroelectric tester, on three different capacitors: 20 nm HZO only, 20 nm with 4 nm Al_2O_3, and 20 nm HZO with 6 nm Al_2O_3, and hysteresis loops are depicted in Fig. 5.19. Consistently with Ref. [102], the remnant polarization is lower with thinker DE layer, while the coercive filed points are larger, meaning higher electrical field is required for thicker DE layer.

Next, endurance measurements is conducted as explained using PUND method with square cycling signal (Different from Fig. 5.17 which shows triangular signal). The capacitor area is 7850 μm^2. Multiple frequencies are tested to see the effect of the cycling signal's frequency on the endurance, and to be able to measure polarization

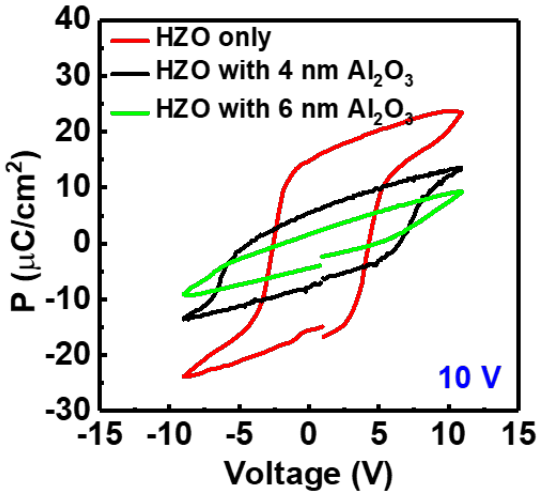

Fig. 5.19. P-V measurements for three MIMs with HZO layer only, 4 nm Al_2O_3, and 6 nm Al_2O_3. Note the reduction in maximum polarization with thicker Al_2O_3 layer.

retention in early cumulative cycles. Before describing our findings from this type of measurements, it should be mentioned that although many mechanisms and interpretations could be summarized from measurements results, as studied systematically and extensively before [106, 108, 114–117], the scope of this report is only to show the effect of an added dielectric layer to the ferroelectricity of HZO. Fatigue frequency dependence in Ref. [118] shows that the slower the switching, the higher the fatigue rate, this is true for our HZO only sample. Fig. 5.20(a) shows the endurance of 20 nm HZO capacitor with no Al_2O_3 layer. At f= 1 KHz (f is the frequency of the cycling signal) we can see that HZO is shows a small peak in remnant polarization (P_r) which is consistent with wake-up effect reported. This effect is decreased in higher f, as in 10 KHz, and 100 KHz, but with subsequent increase in fatigue resistance. Thus, at typical operating frequency ($\sim$ 1 MHz), it can take more than 10^8 cycles for HZO-based memories before a significant reduction in P_r is observed. Fig. 5.20(b) shows the P-V hysteresis loops for the same device: fresh and after fatigue. We can clearly see the loss of P_r after the device is stressed.

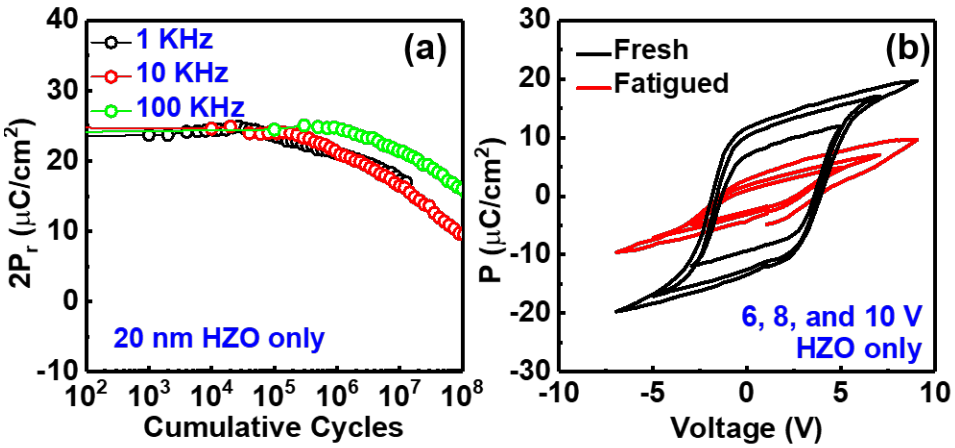

Fig. 5.20. (a) Fatigue behaviors of 20 nm HZO MIM against cumulative number of cycles. (b) P-V measurements of the same sample before and after the endurance measurements for multiple voltages

Nonetheless, when a dielectric layer of Al_2O_3 is integrated, and taking into the account the reduction in the measured P_r (as seen in Fig. 5.19), it was found, in the contrary, that the higher the cycling frequency f the faster the loss in P_r for both thicknesses as seen in Fig. 5.21, even though P_r is measured at similar levels at the beginning of fatigue cycling (for each individual thickness). Therefore, the endurance is believed to become worse with thicker Al_2O_3 layer. The pulse voltage and cycling voltage are equal and chosen to provide an equal effective field (E_{eff}= 4 MV/cm) for all three samples with different thickness of Al_2O_3.

Fig. 5.22 shows a comparison of the three samples at f= 10 KHz. With the significant change in P_r levels for thicker Al_2O_3, the retention seems to be lost faster too in thicker Al_2O_3 to almost disappear after 10^5 cycles.

In conclusion, even though the retention is believed to be better in HZO-based devices compared to other ferroelectric material, it has shown that the ferroelectricity is degraded when the FE HZO layer is integrated with Al_2O_3 dielectric in the gate stack, thus, more careful studies and improvements have to be made.

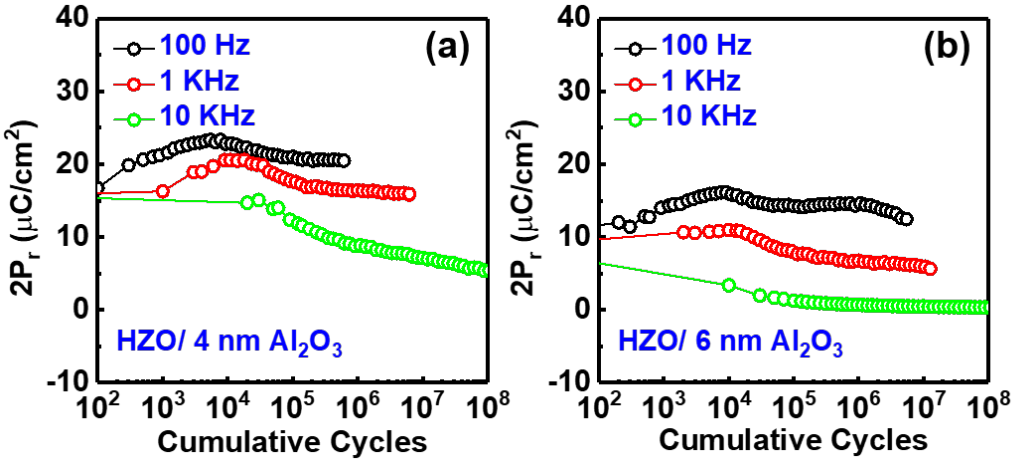

Fig. 5.21. Fatigue behaviors of 20 nm HZO MIM with (a) 4 nm of Al_2O_3 and (b) 6 nm of Al_2O_3 at various cycling frequencies.

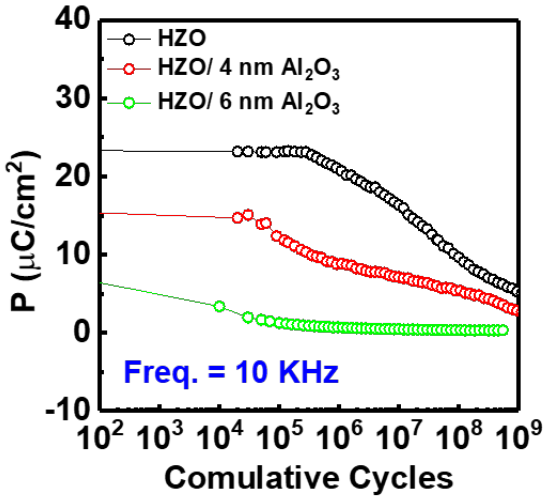

Fig. 5.22. Fatigue behaviors of 20 nm HZO MIM with different Al_2O_3 thicknesses at f= 10 KHz

6. SUMMARY AND FUTURE WORK

In summary, an epitaxial MgCaO film was developed, characterized and compared with amorphous gate oxides in chapter 2. We found that this single crystalline gate oxides has a huge impact on the improvement of oxide/GaN interface quality. D_{it} was systematically measured and extracted for various $Mg_xCa_{1-x}O$ compositions via C-V measurements and conductance method in room and elevated temperatures. The study shows that $Mg_xCa_{1-x}O$ with x=0.25 has the best interface quality and lowest D_{it} levels. A comprehensive study of the interface properties on MOSHEMT and HEMT devices with various gate stacks was carried out in order to determine the correlation between different insulators combination and how interface quality influences high performance GaN devices for RF and high power devices. Table 6 lists the combination of the devices of interest and fabricated by our group. Where 1,2,3, and 5 form the table are studied and the rest are still potential candidate for future work. A novel ultra-wide bandgap semiconductor β-Ga_2O_3 MOSCAPs were fabricated. An optimized fabrication process for ALD Al_2O_3/β-Ga_2O_3 interface is achieved through piranha pretreatment and post deposition annealing. We have investigated (-201) and (010) surface oriented Al_2O_3/β-Ga_2O_3 interfaces via f-dependent, dual sweep, and photo-assisted C-V measurements. A very low hysteresis of 0.1 V for span of frequencies from 1 kHz to 1 MHz is obtained and an average D_{it} of $\approx 2\times10^{11}$ $cm^{-2}\cdot eV^{-1}$ is extracted. In close agreement with low frequency dispersion, this low defect property enables β-(-201)-Ga_2O_3 to be a promising substrate for β-Ga_2O_3 MOSFET, which was later used for Ga_2O_3-on-insulator FETs (GOOI) and occurred in high performance D/E-mode β-Ga_2O_3 with record I_{DMAX} of 600/450 mA/mm and negligible transfer characteristic hysteresis, high I_D on/off ratio of 10^{10}, and breakdown voltage of 185 V and an average E of 2 MV/cm. A novel UV-IV method has been suggested and employed to study the interface quality of both types of interface traps,

Table 6.1.
HEMT and MOSHEMT GaN Devices

Gate Stack		Device Type	Gate Oxide
InAlN/GaN on SiC	1	MOSHEMT	Al_2O_3
	2	MOSHEMT	MgCaO
	3	HEMT	—
AlGaN/GaN on SiC	4	MOSHEMT	Al_2O_3
	5	MOSHEMT	MgCaO
	6	HEMT	—
AlGaN/GaN on Si	7	MOSHEMT	Al_2O_3
	8	MOSHEMT	MgCaO
	9	HEMT	—

namely, donor-like and acceptor-like. Therefore, both GaN and β-Ga_2O_3 are systimatically studied. A suggestion of considering these two channel material for future development incorporating ferroelctric insulators in negative capacitance transistors in order to take advantage of the high mobility material property with NCFET and MOSHEMT structure. The SPCP study in chapter 3 is one of the main contributions of this thesis owing to the simplicity and ingenuity of this measurements in characterizing interface traps not only for GaN transistors which has a 2-dimentional electron gas (2DEG) on insulating substrate, but also for other state-of-the-art devices that do not exhibit body contacts such as ultra-thin-body (UTB) devices with floating body channels. Also, a novel method is proposed for the simultaneous extraction of energy distribution of donor- and acceptor-like interface trap states based on the difference in the gate voltage-dependent ideality factors due to the photonic response of the carriers excited with ultraviolet light within the β-Ga_2O_3 channel surface. SPCP is set to be tested as of the writing of this thesis on our β-Ga_2O_3 GOOI devices, which have less complicated structure compared to GaN MOS-HEMT, thus, a direct interface

characterization considering the minimal bulks and border traps in the crystalline β-Ga_2O_3 and ALD Al_2O_3 gate insulator.

A report on low frequency noise studies on MoS_2 NC-FETs for the first time is included in chapter 4, as well as Ge NC-FETs. Devices with various interfacial oxides, different thicknesses of interfacial oxide, and ferroelectric HZO are systematically studied. The low-frequency noise in MoS_2 and p-type Ge NC-FETs show $1/f$ characteristics with carrier number fluctuation as source to this noise. in n-type Ge NC-FETs however, the carrier mobility fluctuation was found to be the source of $1/f$ noise. The low frequency noise is found to decrease with thicker ferroelectric HZO in the subthreshold regime of the MoS_2 NC-FETs, in contrast to the conventional high-k transistors, and interpreted as electrostatic improvement induced by the negative capacitance effect. It concludes that negative capacitance can not only improve the device performance in the on- and off-states, but also suppress the noise of the devices. In chapter 5 the time response of polarization reversal in Ge NW Fe-FETs are characterized by fast gate bias dual sweeps. The Ge NW Fe-FETs exhibit clear time-dependent ferroelectric hysteresis loop starting from 25 μs. The time response of polarization reversal leads to time-dependent hysteresis and maximum drain current in Ge NW Fe-FETs. The ferroelectric switching speed is found to be related with the maximum voltage applied during the fast gate voltage sweep. The internal ferroelectric switching speed could be faster and depends on the applied electrical field. This chapter also discusses some of the reliability issues related with the ferroelectric HZO in terms of switching mechanism and endurance. The studies take into the account the integration of ferroelectric HZO with other linear dielectric material and gives impressions about the negative effects on HZO reliability.

Further improvement of FE/DE gate stack is required in near future before implementing FE HZO in a harsh high power environment or ultra-fast circuits. A characterization and reliability tests including: Bias temperature instability (BTI), Time-dependent gate oxide breakdown (TDDB), and Hot carrier injection (HCI) are also suggested to be performed to have a complete picture.

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