LOW FREQUENCY NOISE SOURCES AND MECHANISMS IN TWO DIMENSIONAL TRANSISTORS

by

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To my Parents and my Son, Junbeom Kwon

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ABSTRACT

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Beyond graphene, two-dimensional (2D) atomic layered materials have drawn considerable attention as promising semiconductors for future ultrathin layered nano-electronic device applications, transparent/flexible devices and chemical sensors. But, they exhibit high levels of low-frequency noise due to interfacial scattering (small thickness) and interlayer coupling (large thickness). The sources and mechanisms of low frequency noise should be comprehensive and controlled to fulfill practical applications of two-dimensional transistors. This work seeks to understand the fundamental noise mechanisms of 2D transistors to find ways to reduce the noise level. It also verifies how noise can provide a spectroscopy for analysis of device quality.

Most noise analysis tend to apply classical MOSFET models to the noise and electrical transport of 2D transistors, which put together all possible independent noise sources in 2D transistors, ignoring the contact effects. So this could lead to wrong estimation of the noise analysis in 2D transistors. This work demonstrates how the noise components can come from the channel and contact/access regions, all independently adding to the total noise. Each noise source can contribute and may dominate the total noise behavior under the specific gate voltage bias. Herein, the measured noise amplitude in our MoS_2 and $MoSe_2$ FETs shows a direct crossover from channel- to contact-dominated noise as the gate voltage is increased. The results can be interpreted in terms of a Hooge relationship associated with the channel noise, a transition region, and a saturated high-gate voltage regime whose characteristics are determined by a voltage-independent conductance and noise source associated with the metallurgical contact and the interlayer resistance. The approach for separating channel contributions from those contact/access region allows clear evaluation of the channel noise mechanism and also can be used to explain the qualitative differences in the transition regions between contact- and channel-dominated regimes for various devices.

1. INTRODUCTION

1.1 The Rising of the 2-Dimensional (2D) Materials – Graphene and TMDCs

The importance of graphene discovery is not only to prove the existence of stable 2D crystal, but also exhibit a family of materials with very high crystal quality. The most outstanding electronic quality in graphene is that the charge carriers can travel a distance between thousands of atoms without scattering. With these unique advantages, the mobility of graphene can approach 15,000 cm^2/Vs in ambient condition, and even exceed 100,000 cm^2/Vs at low-temperature. [1]–[5] On the other hand, the transfer properties of graphene are also remarkable in showing distinct ambipolar behavior, and the charge carriers of graphene can be continuously tuned between electrons and holes by applying external electric field. [2], [3], [6], [7] With these advantages, the advent of graphene with single atomic layer in the vertical direction is easily exfoliated due to interlayer van der Waals (vdW) interactions, and continues to surprise people in this field by providing new intuition into low dimensional devices. One aspect of graphene that severely limits its potential electronic application is the lack of bandgap, so low-power switching or digital transistors can't be realized. [6], [7]

Alternatively, TMDC is another material family with layer to layer structure. TMDC family materials are composed of strong MX_2 interlayer covalent bonds ($M \equiv$ Mo, W and $X \equiv$ S, Se). [8]–[10] Unlike the graphene, TMDCs have shown great potential in device applications due to their comparable bandgaps, thermal stability, carrier mobility, and compatibility to silicon CMOS process.[11] Among many TMDCs, Molybdenum disulfide (MoS_2), one of the most extensively investigated materials for the application of thin-film transistors, has been considered as a promising candidate for field-effect transistors with relatively high on/off ratio and reasonable electron mobility. [11]–[16] With recent findings on direct bandgap to indirect bandgap, optoelectronic devices with MoS_2 have attracted the new interest in the optical society. [17], [18]

1.2 Novel 2D Semiconducting Material – $MoSe_2$

With the scaling approach of the traditional MOSFET towards a dead end, 2-Dimensional transition metal dichalcogenides (2D-TMDCs), including MoS_2, WS_2, and WSe_2, are being widely explored as channel materials in Field-Effect Transistors (FETs). Recently, as an analog of MoS_2, $MoSe_2$ is considered as another promising new material to study in various applications. While MoS_2 has been the most extensively investigated TMDC for the diverse device applications, $MoSe_2$ exhibits significantly different properties from MoS_2. Tongay et al. showed the existence of degenerate direct and indirect bandgap and decoupling of bulk and the limit of 2D in few layer $MoSe_2$ with temperature.[19] $MoSe_2$ is also proposed as a material of choice for solar cell applications and optoelectronics applications due to the adjustable interlayer coupling that enables the tuning of bandgap in the solar spectrum.[20]–[24] Compare to MoS_2, fast optical response and high and tunable excitonic binding energy have been shown in $MoSe_2$.[25], [26] In terms of the oxide interface in the channel, it is also scientifically interesting to know how the interface of Se-oxide affects the $1/f$ noise and compare it with the counterpart of S-oxide in a MoS_2 transistor. While Mo-Se bonding is more stable, MoS_2 appears to be more vulnerable to defect formation due to sulfur (*S*) vacancies.[25]

1.3 Motivation

Spontaneous fluctuations (noise) underlie the most amazing and common phenomena in both the physical and biological fields. The observed random time record of noise can carry a large amount of information about a system and its interaction with the surrounding environment. Noise can limit the speed of information transfer and data manipulation; however, noise also can contain a treasure-chest of information about a particular system. As shown in Fig. 1.1, today's noise research covers the most important fields including the integrated sensors, bio-implant system, bio/silicon interfaces, SRAM yield, Transistor reliability, Ultra-low power circuits and portable electronics. Moreover, low frequency noise is very sensitive to traps and defects in the device and is strongly related to physical processes such as the trapping and release phenomena. Thus, low-frequency noise can be an important diagnostic tool to estimate the quality and reliability of gate oxide dielectrics.

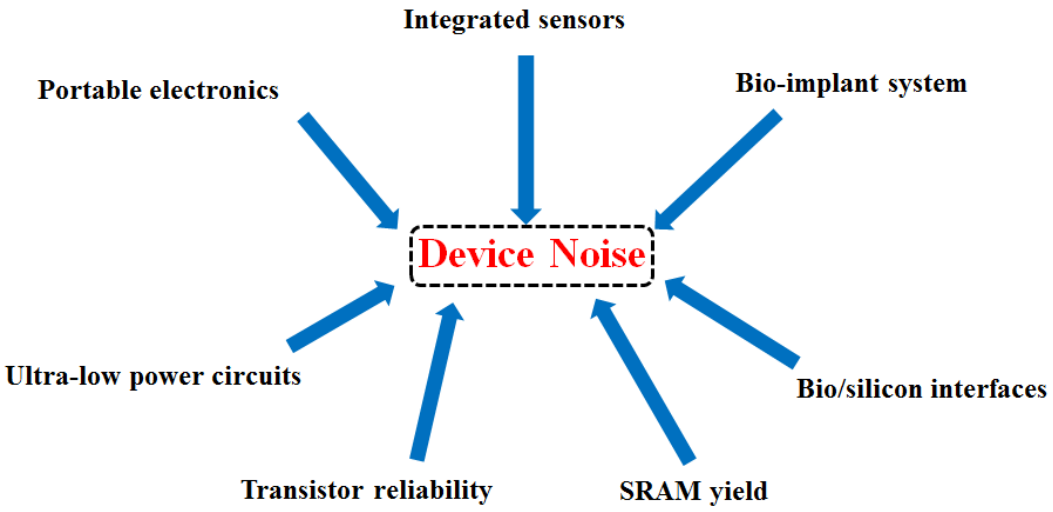


Fig. 1.1 The importance of low frequency noise in many different fields.

1.4 Outline of the Dissertation

This report will be focusing on novel 2D materials such as MoS_2 and $MoSe_2$, and the correlation of electronic transport and 1/*f* noise behaviors in terms of the dependences of channel lengths, channel thicknesses and different contact metals. The main results achieved in this thesis are listed as follows:

Low-frequency noise (LFN) is introduced in **Chapter 2** together with the theory of noise in semiconductor devices, and the setup of 1/*f* noise measurement.

Chapter 3 reports correlating electronic transport and 1/*f* noise in $MoSe_2$ FETs. Here we report the 1/*f* noise properties in $MoSe_2$ FETs with varying channel thickness (3 to 40 atomic layers). Contributions of channel vs. access/contact regions were extracted from current-voltage (transport) and 1/*f* noise measurements. The measured noise amplitude shows a direct crossover from channel- to contact-dominated noise as the gate voltage is increased. The results can be interpreted in terms of a Hooge relationship associated with the channel noise, a transition region, and a saturated high-gate voltage regime whose characteristics are determined by a voltage-independent conductance and noise source associated with the metallurgical contact and the interlayer resistance. Both the channel Hooge coefficient and the channel/access noise amplitude decrease with increasing channel thickness over the range of 3 to 15 atomic layers, with the

former remaining approximately constant and the latter increasing over the range of 20 to 40 atomic layers.

Chapter 4 reports transitions between channel and contact regimes of low-frequency noise in many-layer MoS_2 field effect transistors. Prior low-frequency noise studies have generally shown that devices with single/few layer channels exhibit larger levels of noise than those with multi-layer channels. Within these studies, the noise has been attributed to either mobility fluctuation, number fluctuation or correlated mobility/noise fluctuation behavior. The lack of clear analysis of the contributions of the contacts/access regions to the measured noise and resistance in many studies makes it difficult to draw specific conclusions regarding the dominant noise mechanism in the channel, or even to identify the onset of contact-dominated behavior in the measured noise or resistance. Here, we have studied voltage-dependent $1/f$ noise and resistance in MoS_2 FETs with ~ 142 atomic layer-thickness channel and three different channel lengths. The gate-voltage dependence of the noise amplitudes can be understood in terms of a channel contribution, which follows a mobility fluctuation model with comparable Hooge parameter for the three devices, and a contact/access region contribution which is independent of gate voltage. The approach for separating channel contributions from those of contact/access region allows clear evaluation of the channel noise mechanism, and also can be used to explain the qualitative differences in the transition regions between contact- and channel-dominated regimes for various devices.

In Chapter 5, we will talk about a systematic study on the current model and Hooge's constants in multilayer MoS_2 and $MoSe_2$ field-effect transistors. In particular, we focus on a theoretical framework to explain our experimental findings of the general trend in the hooge parameter vs. layer thickness (initially decreasing, and then saturating or gradually increasing) and its dependence on charge screening and interlayer coupling for various contact metals (Sc, Mo, Ni and Cr/Au) and channel materials (MoS_2 and $MoSe_2$). Furthermore, our $1/f$ noise results allow us to unravel new fundamental information about carrier transport and $1/f$ noise in two-dimensional layered systems that will likely play a very important role in the fulfillment of future electronics applications that have not been evaluated in the past.

Chapter 6 will summarize the results achieved in this thesis.

2. 1/*F* NOISE THEORY AND EXPERIMENTAL SET-UP

2.1 Low-Frequency Noise

Generally, noise has two sources in electronic nano-devices: one is intrinsic, and the other is extrinsic. Extrinsic noise comes from interference from other outside signals, radio interference and so on. This noise can be controlled through proper circuit design, grounded point and the degree of brightness. Therefore, it is not usually a concern in semiconductor devices. However, intrinsic noise is generated within the device itself, so more prominent attention should be taken into control it. Besides, low frequency noise has a terrific impact on devices and circuits. Noise is not only a problem that should be avoided as much as possible, useful information such as interface quality, material condition, defect and reliability can be captured by the noise analysis. Therefore, understanding noise is helpful to the device engineers to decrease its influence on circuits and systems, defection in materials. Low frequency noise refers to random signal fluctuations below 100 kHz, which forces a practical limit on the high performance electronic devices. Subsequently, I will discuss different types of noise and how to measure 1/*f* noise.

2.2 Noise Sources in Semiconductors

The intrinsic noise in a semiconductor device is generated by several different mechanisms. Because of the difference of these mechanisms, the frequency response of noise becomes very complicated. The most common types of intrinsic noise seen in devices are discussed in the following sections.

2.2.1 Thermal Noise

Thermal noise (also known as Johnson or white noise) is caused by random thermal movement of charge carriers (electrons or holes) in semiconductors. Thermal noise always occurs for all semiconductors in the absence of an applied electric filed. The power spectral density (PSD) of this noise is called as white noise because it is constant in the frequency range. The voltage noise PSD of thermal noise (S_V)due to the Brownian motion of charge carriers is given by [27]

$$S_V(f) = 4kTR \tag{2.1}$$

where *k* is the Boltzmann constant, *T* is the absolute temperature and *R* is the device resistance. And in terms of current noise PSD (S_I) of thermal noise can be expressed as

$$S_I(f) = \frac{4kT}{R} \tag{2.2}$$

Thermal noise can be seen in every devices and materials. Moreover, the thermal noise level is relatively small, and its presence is everywhere in all electronic components, so this is not a problem with the minimum level of noise.

2.2.2 Shot Noise

Because electrical charge consists of discrete carriers, shot noise can be generated when the random movements of charge carriers cross a barrier. The time-domain mean squared deviation from the mean dc value is known as shot noise. And the expression for shot noise PSD takes the following form [28]

$$S_I(f) = 2qI \tag{2.3}$$

where *I* is the dc current and *q* is the electron charge of 1.6 x 10^{-19} C. Shot noise is most commonly observed in diodes as electrons and holes cross p-n junction, but is indistinguishable from the thermal noise as far as the spectral form is worried.

2.2.3 Generation-Recombination (G-R) Noise

In a MOSFET, electron-hole pairs (ehp) are consistently and randomly generated due to thermal or optical excitation of the semiconductor lattice. In addition, the generated ehp's tend to recombine after some time, no longer contributing to charge movement. This random generation and recombination (G-R) of ehps leads to a small current fluctuation, given by [29]

$$\frac{S_I(f)}{I^2} = \tau/[1 + (2\pi f)^2\,\tau^2] \tag{2.4}$$

where τ is the average lifetime of generation-recombination events. Note the $1/f^2$ dependence on frequency. G-R events can also cause fluctuations in local mobility or diffusion as new donor or acceptor sites are being vacated, which will add to the total current fluctuation. The power spectral density plot of G-R noise is a Lorentzian spectrum which is constant at low frequencies but drops down as $1/f^2$ above the characteristic frequency defined by 1/τ. G-R noise is only important when Fermi-Level lies on a few *k*T energy to the single trap.

2.2.4 1/*f* flicker Noise

When PSD of the noise is inversely proportional to the frequency, this kind of noise is called as the flicker noise (1/*f* noise) or pink noise. The current noise PSD (S_I) for flicker noise can be expressed as

$$S_I(f) = \frac{\alpha I^{\beta}}{f^{\gamma}} \tag{2.5}$$

where I is the device current, α, $\beta \fallingdotseq 2$ and $\gamma \fallingdotseq 1$ are constants. In general, for 1/*f* noise, the frequency exponent of γ is between 0.8 and 1.2. 1/*f* noise in the device has been observed in the low frequency part of the spectrum (10^{-5} to 10^{7}) in most conducting materials and a wide variety of semiconductor devices.[30], [31] And there are basically two physical noise mechanisms for fluctuations in current: Mobility fluctuation and Carrier number fluctuation. 1/*f* noise is the most common type of noise in the electronic devices due to possible noise sources. It is also the largest source of noise in active semiconductor devices, tends to overwhelm other noise types, and it is directly associated with the quality of device.

2.3 1/*f* Noise models for FET structures

Here, the origin of low-frequency noise is discussed. Two different models of low-frequency noise are summarized and included: Hooge mobility fluctuation model and Carrier number fluctuation model. In this thesis, we will use Hooge model as the basic model to investigate the details of low-frequency noise mechanism in 2D layered systems.

2.3.1 Hooge Mobility Fluctuation Model

In 1969, Hooge proposed that the 1/*f* noise model for homogeneous bulk systems and the model was attributed to carrier mobility fluctuations.[32]–[34] Moreover, the model was an empirical relationship between the amplitude of 1/*f* noise and the total number of carriers. It is simply expressed by:

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{\alpha_H}{fN} \tag{2.6}$$

and

$$N = \frac{C_{OX}(V_{gs}-V_{th})W_{ch}L_{ch}}{q} \tag{2.7}$$

for the linear region where S_R is the resistance noise PSD, α_H is the dimensionless parameter

called as the Hooge's constant, N is the total number of carriers, C_{OX} is the gate oxide capacitance per area, V_{gs} is the gate voltage, V_{th} is the threshold voltage, W_{ch} and L_{ch} are the width and length of the channel. At first, Hooge's constant (α_H) has been known to be a universal constant with a value of 2 x 10^{-3} for all materials, but later it is known to be wrong. For instance, if the same material has many defects, α_H would be high, and if it has few defects and a crystalline form, α_H would be low. For Si, the values of α_H have been colorfully observed from 5 x 10^{-6} to 2 x 10^{-3}.[34]

Then, the model has been extensively applied to MOSFET structures, and the mobility is affected by scattering due to both impurities and lattice, hence, the observed mobility, μ, can be written by:

$$\frac{1}{\mu} = \frac{1}{\mu_{imp}} + \frac{1}{\mu_{latt}} \tag{2.8}$$

where μ_{imp} is the mobility due to the impurity scattering, and μ_{latt} is the mobility due to the lattice scattering. In 1978, Hooge and Vandamme [35] found experimentally that the Hooge mobility fluctuation model is generally affected from the mobility fluctuations by the scattering due to trapped charge carrier at the oxide-semiconductor interface in a MOSFET. Moreover, the Hooge mobility fluctuation model can be well explained by the current fluctuations from the mobility scattering of lattice vibrations.

2.3.2 Carrier Number Fluctuation Model

In 1957, McWhorter proposed a model in which low-frequency 1/f noise was attributed to carrier number fluctuation in the channel.[36] In this model, McWhorter considered that 1/f noise is caused by carrier number fluctuation due to trapping and de-trapping of charge carriers at the surface and interface of semiconductor-oxide. In other words, the low frequency noise is associated with the surface effect.[36] Each trapping/de-trapping event produces a G-R spectrum of Lorentzian with a time constant of τ, and the observed phenomenon would look like a random telegraph signal (RTS) in the single trap.[37]–[39] The current noise PSD is derived as:

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_{low}+\tau_{high})\left[\left(\frac{1}{\tau_{low}}+\frac{1}{\tau_{high}}\right)^2+(2\pi f)^2\right]} \tag{2.9}$$

where ΔI is the amplitude of current fluctuation, and τ_{low} and τ_{high} are two time constants of low and high states, respectively. Moreover, if the traps are spatially distributed, the

superposition of all the Lorentzian distributions related to each trap gives 1/*f* spectrum as shown in Fig. 2.1. In McWhorter model, a time constant of single tunneling is related to each trap, and the time constant (τ) is defined as:

$$\tau = \tau_0 e^{\gamma x} \tag{2.10}$$

where τ_0 is a time constant of trap from the interface, γ is the attenuation coefficient in the oxide (for Si-SiO_2, γ = 10^8 cm^{-1}), and x is the distance from the interface.[40] Since the states more than a few value of kT above/below the Fermi level are filled/empty, the traps that contribute to 1/*f* noise are around the Fermi level.

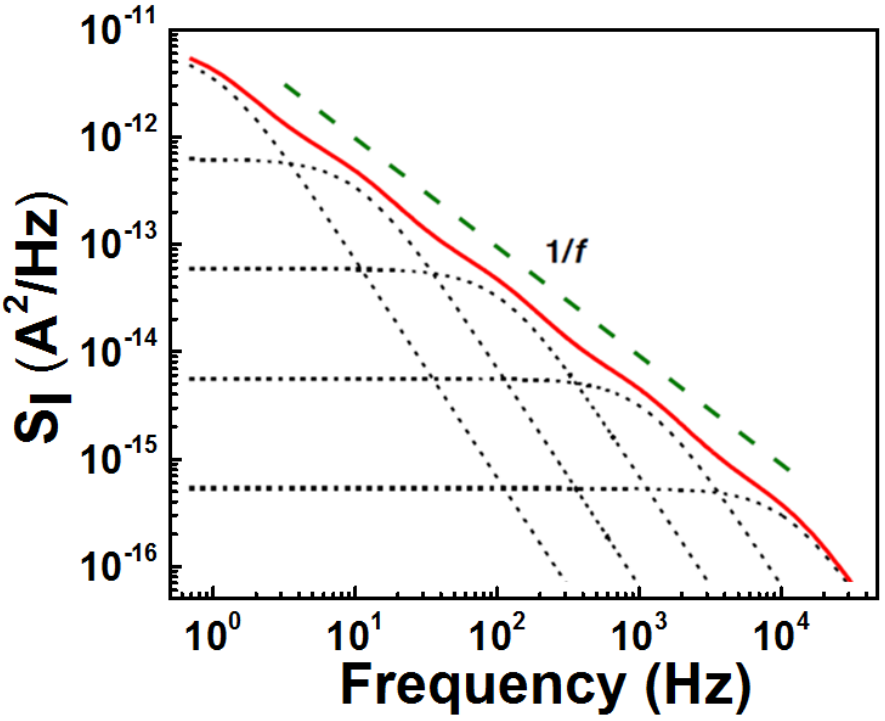


Fig. 2.1 Superposition of five Lorentzians providing a total spectrum that roughly represents the 1/*f* dependency over several decades of frequency.

2.4 1/*f* Noise Measurement

In order to measure 1/*f* noise in transistors, a constant gate and drain bias is applied while a spectrum analyzer is used to record the frequency domain of the resulting current. The configuration of test setup is shown in Fig. 2.2. A low pass filter is placed across the gate voltage

source to filter noise from the applied voltage. A Stanford Research SR 570 preamplifier is used to convert the drain current into a voltage with appropriate range for the Agilent 35670A spectrum analyzer. The preamplifier also applies the drain voltage bias to the device.

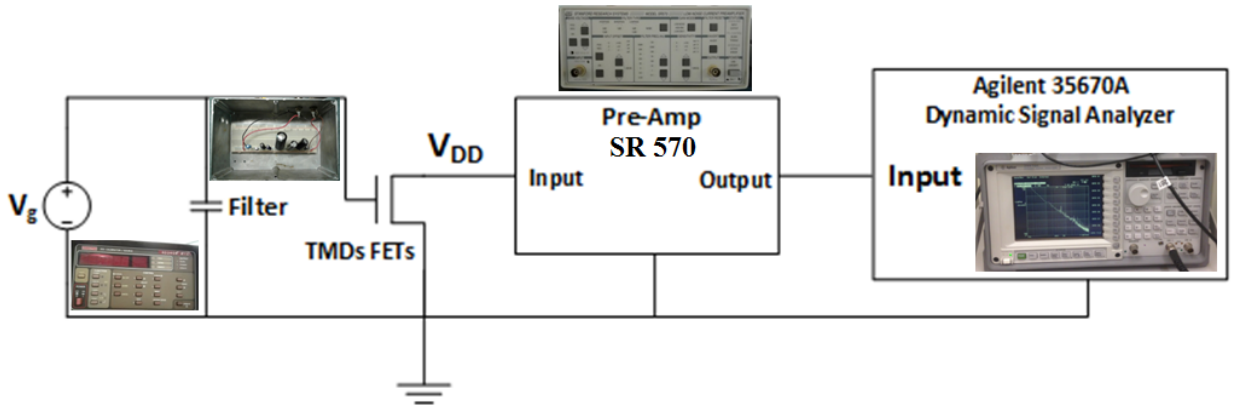


Fig. 2.2 The configuration of noise measurement.

The device is connected between ground and the preamplifier input, with the gate terminal driven by a DC voltage source, most often in this work a Keithley 263 voltage calibrator was used. The spectrum analyzer records and averages together up to 50 measurements to obtain a final frequency spectrum of the device noise. The entire setup is carefully grounded and enclosed to reduce extrinsic noise influences. The Agilent spectrum analyzer was configured for FFT analysis and to measure the power spectral density of the input signal. The low-noise current preamplifier is used to convert the drain current into a voltage readable by the spectrum analyzer. The preamplifier's input bias voltage was enabled, usually to V_{DS} of 50 mV, to supply the drain voltage to the device. Other preamplifier internal filters and offsets were disabled, and the sensitivity set to the lowest possible value without overloading the output or dropping the bandwidth below the desired frequency range. Because the measured signal is a voltage output from the preamp, the spectrum analyzer will display the voltage power spectral density in V^2/Hz. For analysis, the current spectral density, S_I, in A^2/Hz, is needed, so the voltage value must be multiplied by the square of the preamp sensitivity.[41] At each bias point, multiple measurements were taken and averaged together automatically by the spectrum analyzer. Above mentioned, usually 50 measurements were averaged together, but in some devices where current drift was high, 25 or 30 measurements were taken to quicken the measurement time. With a lowest frequency of 1 Hz, each measurement takes at least one or two seconds, so with averaging,

getting a single data point can leave the device under bias for a full minute, allowing time for significant current drift. In order to solve this difficulty, an oscilloscope was usually used to watch the output from the preamplifier and check the average voltage, which was compared with a previously measured I-V characteristics.

For the consideration of bandwidth, the bandwidth limits of SR 570 preamplifier depend closely on the sensitivity setting, and most noise measurements in this thesis were taken over a frequency range from 1 to 1600 Hz, then, the noise results were analyzed with the data picked at 100 Hz. And to keep gain up to 1600 HZ, the sensitivity was kept above 100 nA/V with the low-noise operating mode all the time.

For the control of extrinsic noise, a large capacitor device was placed in parallel with the gate voltage to reduce noise from the power supply. The ground connections of each device, as well as ground terminals at each microprobe, were all tied to ground system in the lab. The device during the measurement was also put in a shielded and dark probe station hood to minimize extrinsic noise sources. Lastly, the preamplifier can be a large source of noise in the set-up, so it was always operated from battery power to reduce introduction of extra 60 Hz noise stems from the AC power.

3. CORRELATING ELECTRONIC TRANSPORT AND 1/*F* NOISE IN $MOSE_2$ FIELD-EFFECT TRANSISTORS

3.1 Introduction

Two-dimensional atomic crystals, especially transition metal dichalcogenides (TMDCs) such as MX_2 (M ≡ Mo, W and X ≡ S, Se) have shown fascinating electronic and optical properties, are of interest for future nanoelectronic, optoelectronic, and nanophotonic devices.[11], [18], [42], [43] Multi-layer TMDC materials show layer stacking via van der Waal interaction between layers. Characteristics such as an indirect to direct bandgap crossover [12], [44], formation of strongly correlated many-body bound states in monolayers [45]–[47] and tunability in band gap between 1.0 eV and 2.0 eV make 2D-TMDCs attractive for fundamental as well as applied research. [48]–[52] A number of TMDCs have been used as channel materials in FETs, yielding devices with low off-current, ON/OFF ratio above 10^6, high field effect mobility, and near 60 mV/decade subthreshold swings. [16], [53]–[56] There are also recent demonstrations of fully integrated circuits and logic building blocks (such as an inverter, NAND gate, static RAM and five-stage ring oscillator) from 2D FET devices. [14], [15], [57]–[60]

Contacts play a very important role in the charge injection process into the channel of a back-gated SB-FET, particularly for the metal source/drain contacts typically employed to TMDCs. [48], [61]. In a study on MoS_2 FETs comparing contact metals with various work functions, Das *et al.* [62] showed a significant change in extrinsic mobility over the range of work functions, with the highest performance observed for the lowest work function material (scandium). There has been detailed transport measurements focused on microscopic analysis of channel materials as well as channel-metal contact effects (both room and low temperature). [63], [64] Low-frequency (1/*f*) noise, a ubiquitous phenomenon in every electronic device, has not been well understood and correlated to transport features in these 2D FET devices.

Low-frequency (1/*f*) noise, a fundamental technique in characterizing semiconducting materials and devices [34], [65], [66], has also become valuable in characterizing nanoscale materials and devices, shedding light on the microscopic origin of transport fluctuations, and providing a means to evaluate electronic states at the channel/dielectric interface. Low-frequency device noise can also have significant implications on circuits and systems (such as circuits for RF communications). The noise properties are dependent on the interaction of carriers with the

channel/dielectric interface states as well as the contact and access-region properties. Therefore, it is essential to characterize the 1/*f* noise of devices consisting of low dimensional materials such as nanowires, carbon nanotubes, graphene, and TMDCs. [67]–[73] Furthermore, 2D van der Waal channel materials (graphene, TMDCs) are expected to show unique noise characteristics due to the existence of interlayer resistances between the individual ultra-thin channel layers and the presence of grain-boundaries as transport barriers in case of large scale 2D channels (typically grown using chemical vapor deposition techniques). Indeed, in recent studies some of these features have been demonstrated in noise characteristics: for example, the contrasting nature of 1/*f* noise in single layer graphene (SLG) and bilayer graphene (BLG) has been studied by Min *et al.* and interpreted in terms of their unique band structure. [74] There are several reports of noise in transistors with TMDC channels. The impact of strong localization with a five order of magnitude higher 1/*f* noise along the grain boundaries of CVD MoS_2 compared to the inter-grain noise has been shown recently by Hsieh *et al.* [75] In prior studies on noise in various TMDC transistors, the gate-voltage and/or current dependences have been interpreted in terms of various noise mechanisms, including McWhorter (number fluctuation) model, Hooge (mobility fluctuation) model, or a transition from Hooge to McWhorter models. [72], [76]–[78] Some prior studies in TMDC FETs with relatively thin channel layers have shown behavior consistent with a McWhorter model, either within a channel-dominated regime above threshold [79] or over a bias range spanning sub-threshold and above threshold (e.g. weak versus strong "inversion"), but without explicitly considering contact effects. [78] However, other studies have observed behavior that is consistent with a Hooge mechanism over a significant gate voltage range (above threshold voltage). [72], [80] Combined number fluctuation/correlated mobility fluctuation models have also been discussed. [76], [77] Na et al.[76] studied unpassivated and passivated MoS2 devices (~18 layers) and analyzed the results with a mixture of Hooge and McWhorter models but observed Hooge behavior in "bulk" (~62 Layer) devices. Other studies also showed the interpretation with the unified model of carrier number fluctuation and correlated mobility fluctuations in single-layer chemical-vapor deposited [81] and thick-layer (75 Layers) TMDC FETs. [82] A transition from Hooge regime to McWhorter regime with increasing I_d in these studies generally ignores the contact effects, which could be responsible to the observed transition in noise behavior. In general, these studies indicate that noise behavior is different in strong versus weak "inversion" regimes and that increased layer thicknesses yield lower noise

than single/few layer devices. However, it is difficult to draw specific conclusions regarding what device parameter or material choice yields a specific dominant noise mechanism. For example, Hooge behavior is observed for thin layers (monolayer and bilayer) in some cases but for bulk layers in other studies. [83] Some studies have considered contact and channel effects [79], [84], but consideration of noise properties versus layer thickness has been limited and a comprehensive model for layer-thickness dependence is not available. A more thorough understanding of 1/*f* noise behavior, including consideration of channel thickness and contributions of contacts, should enable better device structures, which will be important for sensors, [85] digital and analog electronics, [86] as well as linear circuits for radio frequency communications. [87]

The current study focuses on multilayer $MoSe_2$ FET devices with channels of various atomically controlled thicknesses. Analogous to MoS_2, $MoSe_2$ shows tunable energy gap and crossover from indirect to direct bandgap in the monolayer limit. [19], [88], [89] However, in our observation, $MoSe_2$ FETs have shown higher ambient stability for prolonged duration with minimal hysteresis during forward and reverse bias conditions. Several other unique characteristics of $MoSe_2$ over MoS_2 are (1) degenerate indirect and direct bandgap with decoupling of bulk and 2D limit, [19] (2) angle resolved photoemission spectroscopy (ARPES) shows the dispersion of the valence bands decreases along $k_{\parallel}$ and $k_{\perp}$ directions, indicating increased 2D character (or increased interlayer distance). [90] (3) $MoSe_2$ shows much weaker bound exciton peak compared to MoS_2, therefore, having a faster photoresponse time (~ three orders of magnitude faster; 25 ms compared to < 30 s for MoS_2) than MoS_2, indicating potential application in efficient phototransistors. [25] (4) the atomic defects (Mo-Se defects) in $MoSe_2$ are reported to be less significant than the Mo-S defects in MoS_2. [91] These properties, along with observed transistor characteristics, make $MoSe_2$, a promising material for nanoelectronic and optoelectronic device applications. While the transport properties of $MoSe_2$ FETs have been reported, 1/*f* noise characterization has not been considered in detail, e.g. to include consideration of the channel and contact noise in terms of the channel thickness. [84], [92]

Herein, we present an experimental study of the current-voltage relationships and gate-bias dependent *1/f* noise in $MoSe_2$ transistors with channel thicknesses varying from 3 to 40 atomic layers. For a given layer thickness, the gate-bias dependences of both the conductance and noise at low drain fields (linear regime) can be understood in terms of noise contributions and

conductance from the channel and contact/access regions. The model developed in the current work can fit voltage dependence without the need to assume a voltage-variable noise mechanism within the channel. Our study shows that the voltage dependence can be fit by a model considering a transition from channel-dominated noise to contact-dominated noise, and that a single noise mechanism is satisfactory to explain the channel contribution to noise. Comparison of properties of devices with varying layer thicknesses allows both qualitative and quantitative comparison of the intrinsic channel properties (mobility and Hooge parameter) and the contributions from the contact and interlayer coupling resistances. As the layer thickness increases over the range of 3-15 monolayers the mobility increases, and noise amplitude decreases, consistent with decreasing interactions between carriers and interface states. For thickness of 20 layers and beyond, increasing layer thickness leads to decreased extrinsic mobility and increased noise amplitude, associated with increased series resistance involved with interlayer coupling resistance.

3.2 Experimental Details

$MoSe_2$ layers of various atomic thicknesses were exfoliated on Si/SiO_2 (90 nm) substrates using mechanical exfoliation method and their locations were identified using predefined alignment markers on the Si/SiO_2 substrates. Precisely, $MoSe_2$ layers with 3L, 5L, 8L, 10L, 15L, 20L, and 40L were selected for FET device fabrication. L stands for a single molecular layer of $MoSe_2$ solid. High quality bulk $MoSe_2$ crystals (from *2D Semiconductor, Inc.*) were used to obtain the above flakes with mechanical exfoliation. The thicknesses of the flakes were determined by atomic force microscopy and the quality of the flakes was evaluated using Raman spectroscopy (with laser excitation wavelength of 532nm). 50 nm thick nickel was used as source/ drain (S/D) contact electrodes in the transistor structure. The channel length of each of the devices was kept 2μm and the channel widths, determined by the flake dimension, were kept approximately between 2μm and 4μm. A semiconductor parameter analyzer, electrical probe station, and arrangements for $1/f$ noise measurements were used for the transport and noise characteristics study of all the above FETs. More details of the device fabrication and measurement set up were provided in 3.5.1.

3.3 Results and Discussion

Fig. 3.1 (a) shows the schematic view of the nickel S/D and back-gated $MoSe_2$ FET structure studied in this study. Fig. 3.1 (b) shows the AFM image and step profile of a representative $MoSe_2$ flake that forms the channel of a FET with thickness around 9.7nm, corresponding to ~15 molecular layers (single layer thickness of $MoSe_2$ ~ 0.65nm).[93] Fig. 3.1 (c) shows the Raman spectrum of a representative flake (15 layers), acquired near its center (the laser spot size is ~1μm in diameter and hence could be well focused at the center of the flake whose area is few square micrometers). The two primary Raman peaks, measured at positions of 243.42cm^{-1} and 286.32cm^{-1}, are assigned to the A_{1g} and E^1_{2g} vibrational modes, corresponding to the out-of-plane and in-plane lattice vibration, respectively. The electrical characteristics were measured in ambient conditions with electromagnetic and light shielding (see 3.5.1 for more details). Note that the devices studied in the present work are back-gated SB-FETs having a fraction of the channel itself buried underneath the S/D contacts, consequently the contribution of these portions in the carrier transport is critical for the device analysis. [48] Models which include the impact of these channel segments on carrier transport in both the OFF state [48] and the ON state [61] are reported previously for WSe_2 FETs and MoS_2 FETs respectively. In the present work on $MoSe_2$ FETs we follow the ON state model for the transport data analysis and discussion. [61]

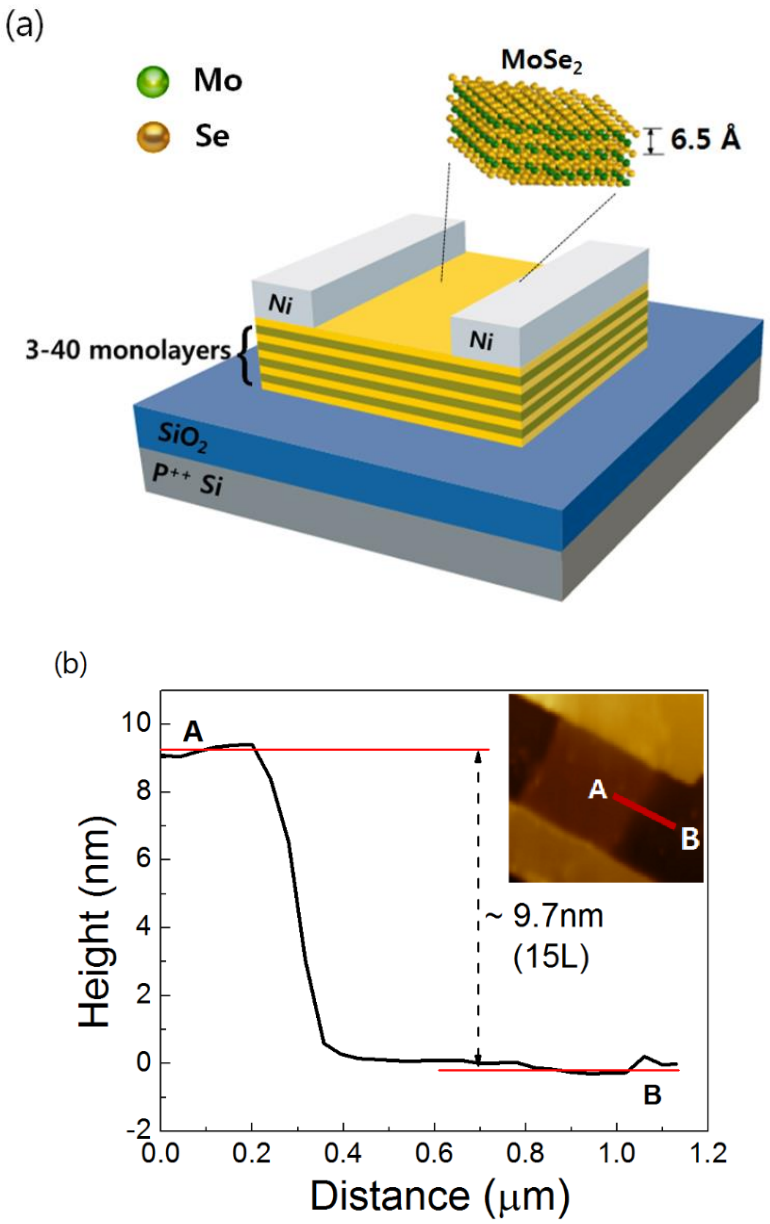


Fig. 3.1 (a) A schematic view of $MoSe_2$ field-effect transistor employed in the present work. $MoSe_2$ flakes with various numbers of atomic layers were used as transistor channels. The nickel S/D contact electrodes are fabricated on top of the back-gated channel. (b) AFM image and geometrical step profile of a $MoSe_2$ flake within a representative field-effect transistor channel. The thickness of $MoSe_2$ layer is approximately 9.7nm, corresponding to ~15 layers. (c) The corresponding Raman spectrum of $MoSe_2$ flake is shown collected using a 532-nm excitation source. The presence of two principal peaks A_{1g} and E^1_{2g} confirms a bonding environment corresponding to $MoSe_2$. The inset shows the optical microscope image of the device used in this study.

Fig. 3.1 continued

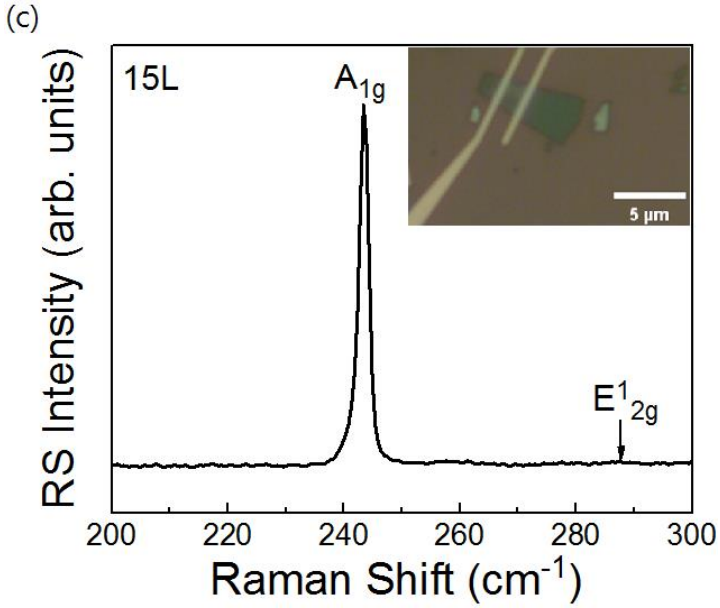


Fig. 3.2 (a) shows the measured low field (drain-source voltage (V_{ds}) of 0.2V) transfer characteristics of FETs with the indicated layer thicknesses. At a given gate-source voltage (V_{gs}), the drain current (I_d) increases with increasing layer thickness over the range of 3L to 15L. The 20L and 40L devices show saturation with increasing V_{gs}, consistent with series resistance effects. A similar trend in drain current maxima has been reported in MoS_2 FETs with low Schottky barrier height electrodes, with a ~ 9L thick channel producing the optimum current. [63] The threshold voltage (V_{th}) of each of the devices were obtained by extrapolating the low-field I_d-V_{gs} relationship to I_d=0.

The transconductance ($g_m = dI_{ds}/dV_{gs}$) is dependent on V_{gs}; the maximum value is used to calculate the extrinsic mobility ($\mu_{ext.}$) at low drain field (V_{ds} = 0.2V), using

$$\mu_{ext} = \frac{dI_{ds}}{dV_{gs}} * \frac{L}{W} * \frac{1}{C_{ox}} * \frac{1}{V_{ds}} \tag{3.1}$$

where L and W are the channel length and width, respectively, and C_{ox} is the gate oxide capacitance per unit area (3.84 x 10^{-4} F/m^2 for 90 nm SiO_2). (The extraction of $\mu_{ext.}$ is described in Fig. 3.8). Fig. 3.2 (b) shows the measured $\mu_{ext.}$ and the intrinsic mobility (μ_{int}, discussed later) as functions of $MoSe_2$ layer thickness. The rise of extrinsic field effect mobility with channel thickness (number of layers), observation of maximum value (at 15L) and decrease beyond 15L indicates the dominant role of the access resistances arising from S/D contacts and the interlayer

coupling beyond 15L. Comparable behavior has been observed by *Das et al.* in MoS_2 transistors and analytically modeled using a resistance network model. [61]

The measured *I-V* relationships and $\mu_{ext.}$ reflect extrinsic values, i.e. they contain contributions from series resistance (R_1) as well as from the channel. The total extrinsic resistance, R_{total}, is the sum of R_1, which is expected to be independent of V_{gs} in the ON state, and the channel resistance (R_{ch}), i.e.

$$R_{total} = R_1 + R_{ch} \tag{3.2}$$

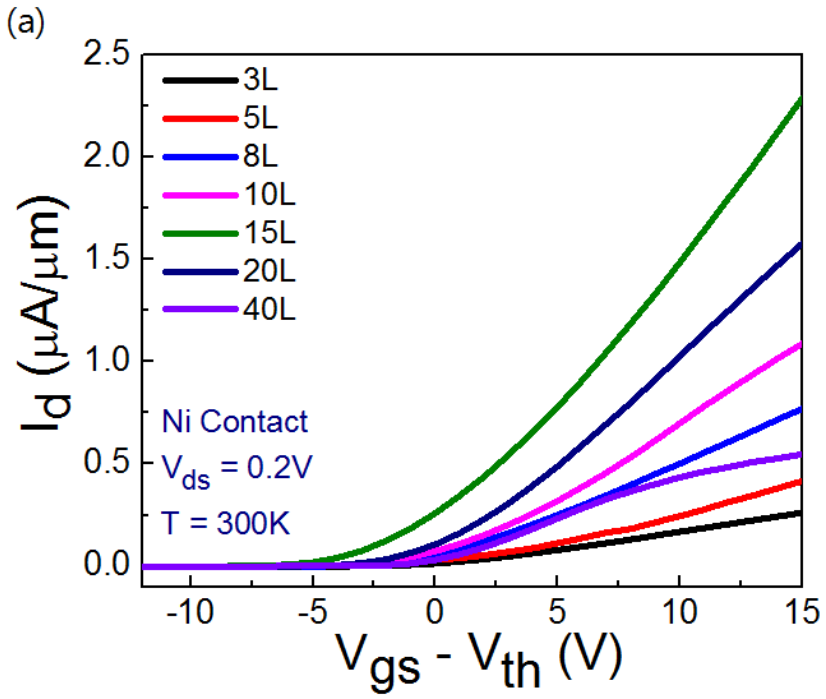
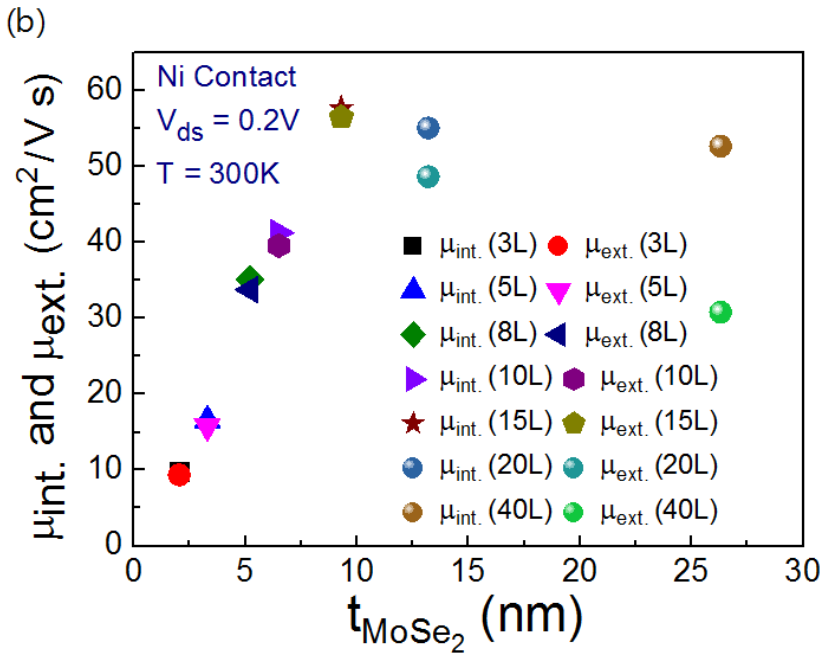


Fig. 3.2 Characteristics of $MoSe_2$ FETs with different layer thicknesses (N = 3, 5, 8, 10, 15, 20 and 40), including. (a) Transfer characteristics measured at V_{ds}=0.2V. (b) intrinsic and extrinsic field effect mobilities extracted at V_{ds}=0.2V as a function of the $MoSe_2$ layer thickness. For the 8L device, parameters are presented for the 2 μm channel length.

Fig. 3.2 continued



R_1 is calculated from the intercept of the relationship between R_{total} and the inverse of V_{gs}-V_{th} (shown in 3.5.2).[94] The extracted values of R_1, and R_1 normalized by W, are shown for devices with various thicknesses in Table 3.1. Given the nature of the 2D van der Waal's solids, in general, R_1 will contain contributions from the metal-semiconductor contact resistance (R_S) as well as the interlayer coupling resistance (R_{int}) between n number of layers. In a limit in which n is significantly larger than the number of layers contributing to channel conductance, one would expect a relationship comparable to:

$$R_1 = R_s + nR_{int} \tag{3.3}$$

In order to quantify the channel behavior, one needs to obtain intrinsic values, i.e. without the effects of contacts/access resistances. To calculate μ_{int} the actual drain voltage across the channel (V_{ds} ́) is calculated using

$$V'_{ds} = \frac{V_{ds}(R_{total}-R_1)}{R_{total}} \tag{3.4}$$

and

$$\mu_{int} = \frac{dI_{ds}}{dV_{gs}} * \frac{L}{W} * \frac{1}{C_{ox}} * \frac{1}{V'_{ds}} \quad (3.5)$$

where n is the number of $MoSe_2$ layers and R_{int} is the interlayer resistance. As shown in Fig. 3.2 (b), following this correction, $\mu_{int.}$ remains relatively constant for layer thicknesses above 15L (~ 55 $cm^2/V{\cdot}s$). For layer thicknesses below 15L, μ_{int} increases with increasing layer thickness. As discussed in prior studies, in few-layer devices, carrier scattering in the channel impacts the current injection as well as the mobility.[61] A number of atomic layers are required to screen such scattering effects and achieve the optimal mobility. Beyond this thickness, $\mu_{int.}$ should remain relatively constant, as observed. However, R_1 increases with increasing layer thickness due to effects of interlayer coupling, which leads to a decreasing μ_{ext}.

The 1/f noise characteristics, an ubiquitous yet a key limiting factor that needs to be addressed in low-dimensional electronic devices, are of interest in terms of both the properties of the channel, e.g. channel-oxide interface, and the contributions from series resistance. Absence of such a study systematically in 2D TMDC devices, particularly the one relating to the transport and noise in the same devices and with number of atomic layer channel thicknesses, would provide a direct correlation among these parameters insisting better and accurate design considerations of such devices for optimal performance.

Fig. 3.3 (a) shows the normalized noise current spectral density (S_I/I_d^2) vs. frequency (f) between 1 Hz and 1 kHz for $MoSe_2$ FETs with various channel thicknesses. The measurements were performed at V_{ds} = 50 mV, to maintain operation in the linear regime) and an over-drive voltage (V_{gs}-V_{th}) of 7V for all the devices. All the FETs follow a nominal 1/f relationship (dotted line). Fig. 3.3 (b) show the total noise amplitude ($f*S_I/I_d^2$), along with the channel and contact/access contributions (discussed later), at f=100 Hz vs. the number of layers. The total noise clearly demonstrates a significant decrease of 1/f noise with increasing channel thickness up to 15L. Beyond 15L, the total device noise increases gradually. The behavior for small number of layers is consistent with significant scattering from impurities and/or interface states (localized electronic states and Coulomb potentials from the substrate have been proposed earlier [95]). As the layer number increases to 15, the channel screens such effects (observation of a charge transport localization within several layers in TMDC channel has been shown previously [96]) Moreover, the increase in the total device noise beyond 15 layers most likely is associated

with access resistances involving the contact resistances, excess channel resistances, and interlayer coupling.

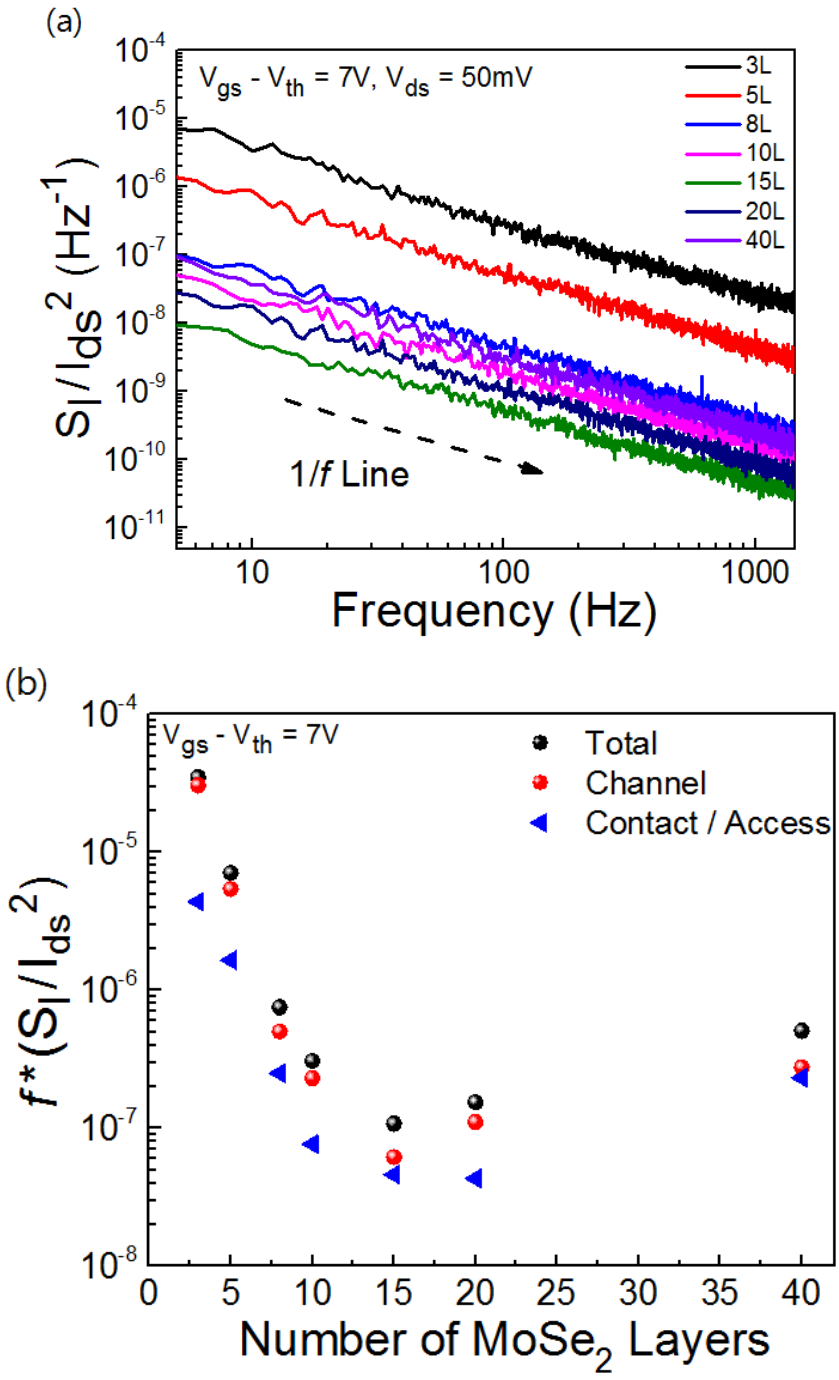


Fig. 3.3 (a) 1/*f* noise current power spectral density for FETs with different number of $MoSe_2$ layers as a function of frequency for various number of layers and (b) comparison of normalized noise amplitudes (Total noise, Channel noise, Contact/Access noise) for FETs with different number of $MoSe_2$ layers. Noise measurements are performed at V_{gs}-V_{th}=7V, frequency of 100Hz and at low drain bias (V_{ds}=50mV) and channel versus contact/access contributions are extracted as described in the text.

Fig. 3.4 (a) and (c) show the measured noise amplitude vs. (V_{gs}-V_{th}) for representative $MoSe_2$ FETs (15L and 40L respectively, black solid circles). In order to allow comparison to the experimental data, the corresponding model (discussed later) is also shown, with blue and red dotted lines representing terms associated with the channel and contact noise sources, respectively, and the green line representing the overall model. In order to compare our experimental data and model to that expected from a McWhorter model, we have included $(g_m/Id)^2$ vs V_{gs}-V_{th} curves in the same plots for 15L and 40L FETs. Corresponding figures for devices with all other channel thicknesses discussed in this work are shown in 3.5.4. Over the voltage range considered, the $(g_m/Id)^2$ relationship exhibits a different gate voltage dependence than the experimental noise amplitude. For layer thicknesses above 8L, this effect is prominent even if one restricts the voltage range to the channel-dominated regime. Similar conclusions can be reached if one considers the $(V_{gs}-V_{th})^{-2}$ dependence associated with a McWhorter mechanism [78], [79]; such behavior is not observed in the experimental data. The model considered in this study, which utilizes a Hooge noise model plus contact effects, fits the data much better than a McWhorter model.

For overdrive voltages below ~ 10V (~9V) for 15L (40L), the data follows approximately an inverse relation with overdrive voltage, as expected for noise dominated by mobility fluctuation (Hooge model).[67], [97] At large overdrive voltages, the noise amplitude saturates, as expected in regimes in which the series resistance dominates both noise and resistance.[67], [79], [97] Qualitatively similar behavior is observed for the FETs with other thicknesses in this study (3.5.4, Fig. 3.9, showing results for 3L, 5L, 8L, 10L and 20L). The dependencies on both voltage and layer thickness can be explained using a model considering the effects of both the channel and the series resistance, as shown by the green curve in Fig. 3.4 (a) and (c) and explained in the following section.

As with the conductance/mobility behavior, the noise behavior can be separated into contributions from the channel and from the series resistance. Following previous approaches for separating channel and contact noise contributions in transistors,[67], [79], [98] it is convenient to transform into resistance spectral power density for the overall device (S_{Rtotal}) and to consider contributions of noise sources and resistances associated with the channel and series resistance:

$$\frac{S_I}{I_d^2} = \frac{S_{Rtotal}}{R_{total}^2} = \frac{S_{R1}+S_{Rch}}{(R_1+R_{ch})^2} \tag{3.6}$$

which can be rearranged to:

$$\frac{S_I}{I_d^2} = \frac{S_{R1}}{R_1^2}.\frac{R_1^2}{(R_1+R_{ch})^2} + \frac{S_{Rch}}{R_{ch}^2}.\frac{R_{ch}^2}{(R_1+R_{ch})^2} \tag{3.7}$$

Here, $\frac{S_{Rch}}{R_{ch}^2}$ and $\frac{S_{R1}}{R_1^2}$ are the normalized noise resistance power spectral densities for the channel and series (contact and interlayer) resistance, respectively. For each device, the parameters on the right side of Eq. (3.7) are extracted at a common V_{ds} (0.2V) as follows. For resistances, R_{total} is determined at each V_{gs} (above threshold) from the corresponding measured I_{ds}. R_1 is determined as stated earlier and assumed to be independent of V_{gs}. At each V_{gs}, R_{ch} (V_{gs}) is determined from R_{total} (V_{gs}) and R_1, using Eq. (3.2). Fig. 3.4 (b) shows the extracted R_{ch} (Vgs) and R_1 for the representative 15L device, along with the corresponding noise power densities (discussed layer). A cross-over from channel-dominated ($R_{ch} > R_1$) to series-resistance dominated ($R_{ch} < R_1$) behavior is observed at approximately V_{gs}-V_{th} = 19V (additional devices shown in 3.5.4). Such a transition for 40L $MoSe_2$ FET is shown in Fig. 3.4 (d) with the resistance cross-over point at a much lower voltage (approximately 9V).

The total noise amplitude, e.g. the data in Fig. 3.4 (a) and (c) for 15L and 40L respectively, is used along with the resistances R_{total}, R_1 and R_{ch}, to calculate the noise sources S_{R1} and S_{Rch}. First, the Hooge parameter is extracted using the small overdrive voltage regime, in which the measured S_I/I_d^2 exhibits a voltage dependence of ~ $(V_{gs}$-$V_{th})^{-1}$ and therefore $S_{Rch} >> S_{R1}$ is a reasonable assumption. Next, the value of S_{Rch} at the maximum measured overdrive voltage is calculated using the Hooge relationship. The value of S_{R1} is obtained by evaluating Eq. (3.7) at this voltage, i.e. using the bias-independent R_1 and the R_{ch}, S_{Rch} and measured S_I/I_d^2 values corresponding to this voltage. Finally, S_{Rch} is determined at other gate voltages using Eq. (3.7) with the corresponding R_{ch} and measured S_I/I_d^2 values. The extracted S_{R1} and S_{Rch} values for the representative 15L device and 40L device are shown in Fig. 3.4 (b) and (d) respectively, and for devices with other thicknesses in 3.5.4. Several regimes are observed. For modest (V_{gs}-V_{th}) values, the total noise is dominated by the S_{Rch} term and follows a Hooge relationship, as evidenced by a gate voltage dependence close to $(V_{gs}$-$V_{th})^{-1}$. A noise crossover point ($S_{Rch} = S_{R1}$) is observed, occurring at approximately $V_{gs} - V_{th}$ = 21.5V for the 15L device. The region between the resistance cross-over point and the noise cross-over point, as indicated by shaded

region in Fig. 3.4 (b), represents a transition region in which ($R_{ch} < R_1$) but ($S_{Rch} > S_{R1}$). Within this region, the noise amplitude is expected to follow a voltage relationship different than either the low V_{gs} (channel dominated) regime or the high V_{gs} (series resistance dominated) limit.[66], [97] For the 40L device, qualitatively similar behavior is observed (Fig. 3.4 (d)), but with a noise crossover voltage at approximately $V_{gs} - V_{th}$ = 10V and a much narrower transition region. The effect of the narrower transition region is evident in Fig. 3.4 (c) where there is distinct variation from channel-dominated to contact-dominated noise regimes without a clear intermediate V_{gs} dependence. The availability of noise and resistance parameters allows calculation of the overall voltage dependence of the noise amplitude using Eq. (3.7). Fig. 3.4(b) and 4(d) show the contact/access (first term in Eq. (3.7)) and channel (second term) contributions to the noise amplitude, along with the overall amplitude (sum of the two terms) for 15L and 40L devices, respectively. Comparable plots for devices with other layer thicknesses are shown in Fig. 3.9 The overall amplitude, i.e. full right side of Eq. (3.7) (green line), matches well with the measured value over the entire voltage range. For overdrive voltages below ~ 15V, the behavior is dominated by the channel contribution and follows a $V_{gs}^{-1.1}$, consistent with a mobility fluctuation (Hooge) noise model. The channel contribution rolls off for V_{gs} values above ~ 15V due to the resistance factor in second term of Eq. (3.7); R_{ch} is monotonically decreasing while R_1 remains constant. The collective effect of the resistance and S_R transitions is a transition region in the noise amplitude, with~ $V_{gs}^{-2.75}$ dependence for this representative device. For voltages beyond this transition region, V_{gs}^{0} behavior is observed, as expected for a regime in which the series resistance dominates both noise and resistance. Similar channel and noise data extraction analysis was performed for all the devices, and the corresponding values are listed in Table 3.1.

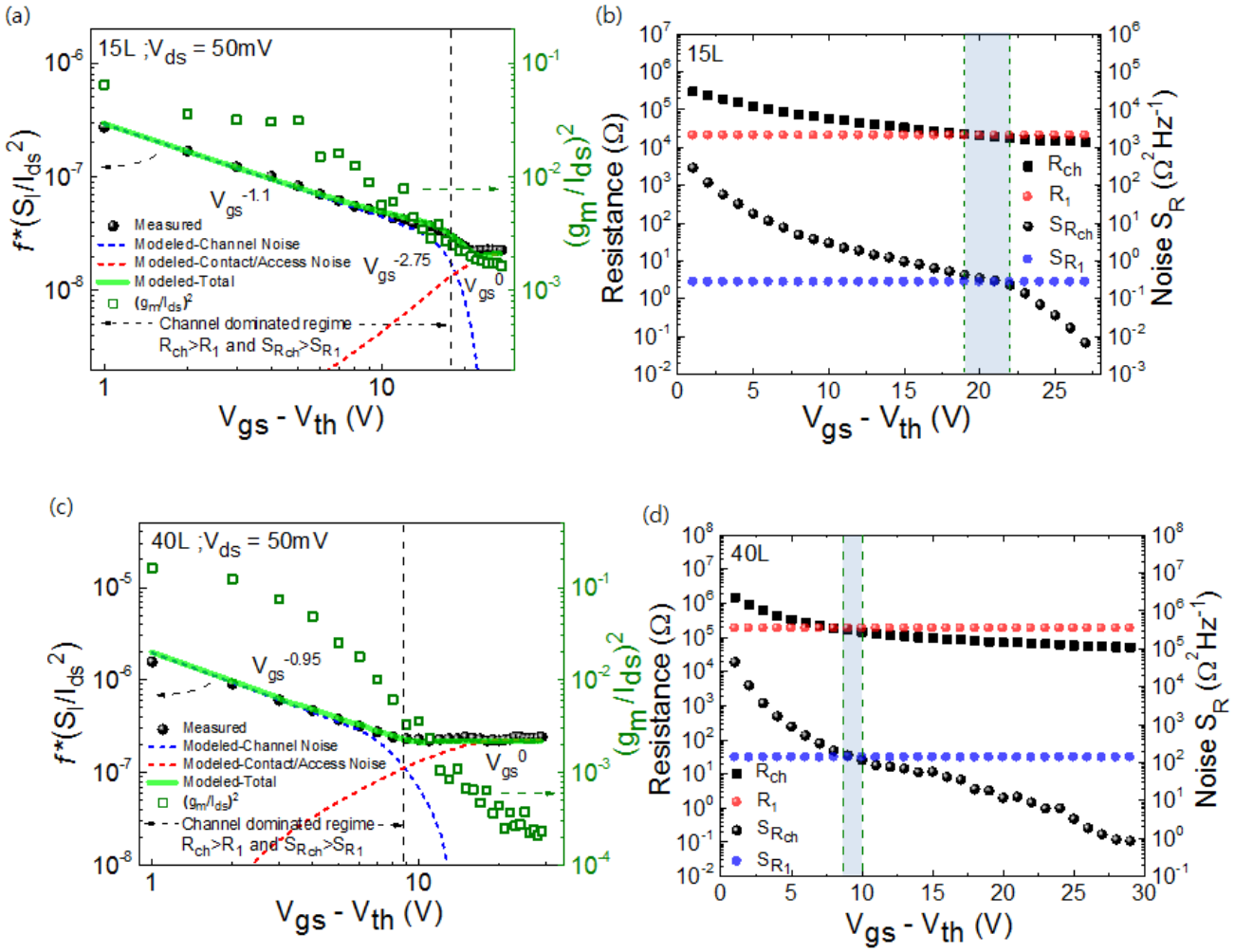


Fig. 3.4 (a) Measured and modeled 1/*f* noise response of 15L $MoSe_2$ FET. The round symbols represent the measured data points for the normalized noise current power spectral density, f^*S_I/I_{ds}^2, as a function of the gate bias. The dashed lines represent the model fitting for the noise dominated by the channel contribution and the contact contribution, respectively. The green line shows the sum of both contributions. Green opened square corresponds to $(g_m/I_{ds})^2$ in the right-sided y axis. The agreement between the modeled fitting and measured data indicates that the measured voltage dependence can be explained by a channel following Hooge's mobility fluctuation model, with a transition to contact/access dominated regime. (b) Contact and channel components of the noise and resistance for 15L $MoSe_2$ FET, obtained from measurements using procedure described in the text. Blue area represents 'transition regime' in which channel dominates noise but contact/access regions dominate resistance. (c) Measured, modeled 1/*f* noise response and $(g_m/I_{ds})^2$ of 40L $MoSe_2$ FET, using same symbols as (a). (d) Contact and channel components of the noise and resistance for 40L $MoSe_2$ FET, using same symbols as (b). In comparison to 15L FET, the transition voltages are lower, and the width of the transition region is smaller. The noise amplitudes of the channel-dominated regime (at same bias point) and the contact/channel dominated regime are also larger, corresponding to a larger Hooge parameter and an increased noise contribution from interlayer resistances, respectively.

The extracted channel, series resistance and total noise amplitudes are plotted along with the corresponding measured data in Fig. 3.6 (a). All the devices show a clear transition from a region following the Hooge relationship to a V_{gs}^{0} regime. However, the relationships are quantitatively different with respect to changes in transition voltages, voltage range and limiting values. In order to allow comparison of the channel and contact/access contributions to noise at a common bias point, the normalized noise amplitudes, transformed back to S_I/I_d^2 using Eq. (3.7), are plotted for an overdrive voltage of 7V in Fig. 3.3 (b). This overdrive voltage allows comparisons of all devices in the regime in which the channel noise term dominates, although the 40L device is at a bias point at which the R_1 term starts to contribute. As observed in Fig. 3.3 (b), the contact/access contribution is smaller than the channel term for all devices, as expected based on the choice of overdrive voltage. Qualitatively similar behavior would be expected at other bias points within the channel-dominated regime. The observation of a contact/access contribution that decreases significantly with layer thickness (3L to 15L) is consistent with an overall decrease in series resistance over that regime. The increase in this noise contribution at larger layer thicknesses is qualitatively consistent with expected dependence of adding noise sources corresponding to interlayer coupling resistances, both in terms of the observed increase in R_1 and the additional noise power spectral density (S_{R1}). However, as evidenced by the dependence of R_1 values versus layer thickness, which does not follow the simple model described in Eq. (3.3), attributing specific contributions to metallurgical contact versus interlayer resistance effects is somewhat difficult.

The observation of a clear channel-dominated regime, which follows the Hooge relationship [34], [84],

$$\frac{S_I}{I_d^2} = \frac{\alpha_H}{f \cdot N} \tag{3.8}$$

where S_I is the current noise power spectral density, I_d is the drain current in the channel, f is the frequency and $N = \frac{C_{ox}}{q} * \left(V_{gs} - V_{th}\right) * LW$ is the total number of charge carriers in the channel, allows quantitative comparison of channel noise properties through the α_H values. In this regard, a rearrangement of Eq. (3.8) in the channel-dominated regime gives

$$f * \frac{S_I}{I_d^2} = f * \frac{S_{Rch}}{R_{ch}^2} = \frac{q * \alpha_H}{C_{ox} * LW} * \frac{1}{(V_{gs} - V_{th})} \tag{3.9}$$

Using Eq. (3.9), the Hooge parameter, α_H, (quantifying channel noise property and excluding effects of R_1 and S_{R1}) can be extracted from linear fitting within the channel-dominated regime,

i.e. the region of Fig. 3.4 (a) and (c) showing a slope of ~ V_{gs}^{-1}. This analysis yields α_H value for each layer thickness. The corresponding values are tabulated in Table 3.1, along with values of R_1 and S_{R1}, which describe the contact/access resistance parameters. The Hooge's parameter vs. atomic layer number is shown in Fig. 3.6 (b). Hooge's constants were extracted in voltage region in which the channel is dominating both noise and resistance, i.e. in which the term containing S_{Rch} and R_{ch} dominates. The Hooge parameter is considered to be a figure of merit for the channel region and should be independent of contact/access resistances. Broadly, the decrease in Hooge parameter with increasing layer thickness (3L to 15L) can be attributed to decreasing interactions of the channel charge with oxide/interface trap states. Beyond 15L, the centroid of the channel distribution is not expected to change significantly, as evidenced by a relatively constant intrinsic mobility, so the Hooge parameter and the channel/interface trap interaction is expected to remain relatively constant. Fig. 3.6 (c) illustrates the equivalent circuit model involving case of a channel noise current source (S_{Ich}) in series with noise current sources representing the metal/semiconductor contact (S_{IS}) and multiple interlayer resistances (S_{Iint}), along with the associated parallel resistances. To add such series sources, it is necessary to convert to Thévenin equivalent resistance noise sources, such as the one illustrated in the Fig. 3.6 (d). The overall noise spectral power density is $S_{Rtotal} = S_{R1}+S_{Rch}$, where S_{R1} is expressed as $S_{R1}=S_{Rs}+n\cdot S_{Rint}$. The overall resistance can be obtained by adding the series-connected resistances. Because the contact resistance and interlayer coupling resistance are not negligible, we model that both the contact and the interlayer resistances contribute to the measured noise.

In order to investigate the channel length dependence of the noise, we fabricated 8L $MoSe_2$ FETs with different channel lengths (L_{ch}=0.5μm, 1μm and 2μm) on the same flake. The dimensions and contact electrical parameters are presented in Table 3.1. Fig. 3.5 presents the measured noise amplitude versus ($V_{gs} - V_{th}$) for the devices, along with the model (channel noise term, contact noise term and total) corresponding to the 2μm channel length. The measured $(g_m/I_d)^2$ relationship is also shown for the 2μm channel length; as with the devices shown in Fig. 3.4, this relationship did not fit the experimental data as well as the model which considered Hooge model and contact effects. Using comparable analysis to that described previously, values of S_{R1} and Hooge parameter are extracted for the devices and presented in Table 3.1. The observation of comparable Hooge parameters for devices with varying channel lengths is consistent with the behavior expected in a channel-dominated regime (as labeled in Fig. 3.5).

Qualitatively similar results are also observed in 3L FETs with different channel lengths. (See 3.5.5 for more details). In order to allow direct comparison between devices with various channel lengths, the area scaling of noise in 3L and 8L FETs is presented in 3.5.6. It is informative to compare the noise results in this study to both prior thickness-dependent mobility studies and noise studies. Prior studies have attributed the increasing mobility with increasing layer thickness to Thomas-Fermi screening, resulting in decreased scattering by interface states. [61] Since interface states are generally thought to be responsible for the noise, one would also expect a decreasing channel contribution to noise amplitude with increasing layer thickness. Noise amplitude can also be compared, e.g. to that of Paul, et al. [78] Although that study observed voltage-dependent noise that followed a carrier density fluctuation model, the noise amplitudes for few-layer devices for voltages just above threshold (as defined in the current study) are comparable to those observed in the 3L and 5L devices at comparable overdrive voltages in the current study. The devices in the current study employ a ~ 3x thinner SiO_2 gate dielectric, resulting in a ~ 3X larger sheet carrier density at a given overdrive voltage. Paul, et al. inferred metallic-regime behavior for gate voltages corresponding to an overdrive voltage of ~ 3V; for the devices in the current study, the sheet carrier density is at the corresponding level or higher for overdrive voltages above ~ 1V.

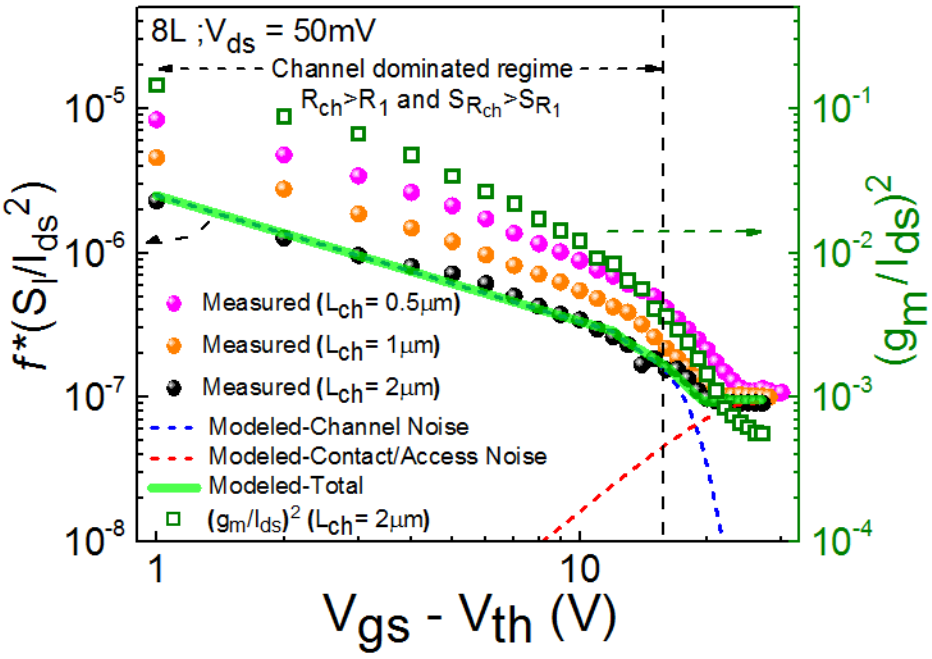


Fig. 3.5 The noise amplitudes ($f*S_I/I_{ds}^2$) and $(g_m/I_{ds})^2$ as a function of overdrive voltage in 8L $MoSe_2$ FETs. Pink, orange and black circle represent the noise amplitude of L_{ch}=0.5μm, 1μm and

2μm, respectively. The blue (red) dashed line indicates the model fitting for the noise in the channel (contact) regime. Green opened square corresponds to $(g_m/I_{ds})^2$. Arrows indicate the appropriate axis.

Prior studies on FETs with TMDC channels have observed comparable behavior in the transition regions between channel-dominated and contact/access dominated noise regimes.[76], [77] In some cases, the transition has been interpreted as a change in the dominant channel noise mechanism from a mobility-fluctuation (Hooge) mechanism to a carrier-density fluctuation (McWhorter) mechanism, which would exhibit a V_{gs}^{-2} dependence.[65], [79] However, the voltage-dependence of the noise amplitude can be modeled using the channel and contact/access contributions discussed above, with a single physical model for the channel contribution. The voltage dependence in the transition region can be explained by the sequential transitions of resistance and noise from channel-dominated to contact-dominated regimes. Such a model is found to be valid across the full range of layer thicknesses considered in this study, with the same channel noise mechanism in all devices.

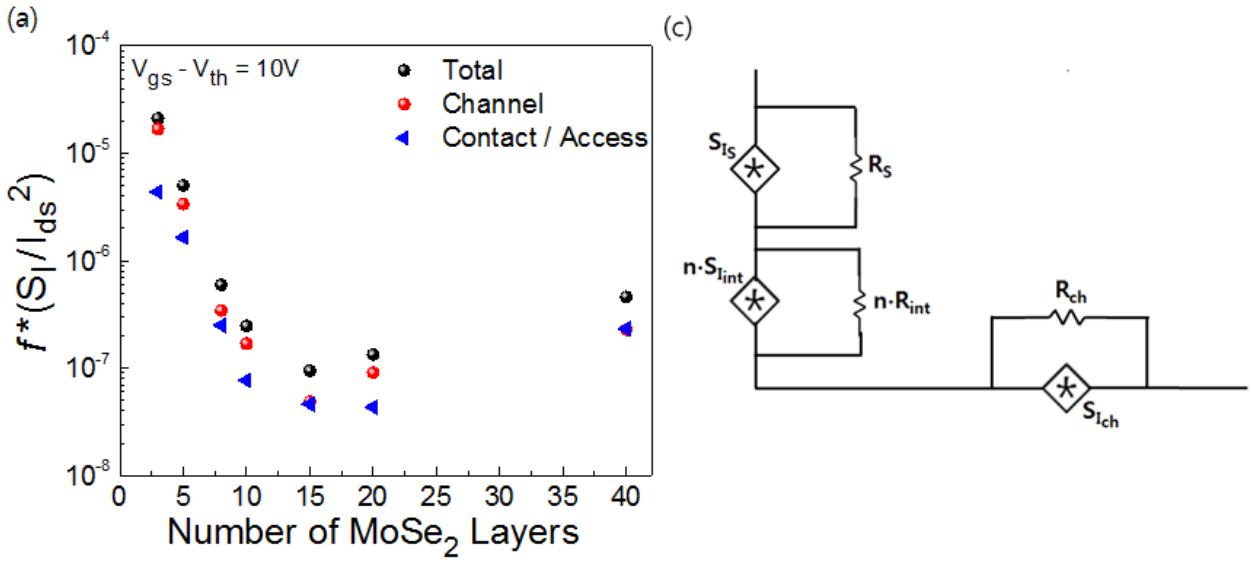
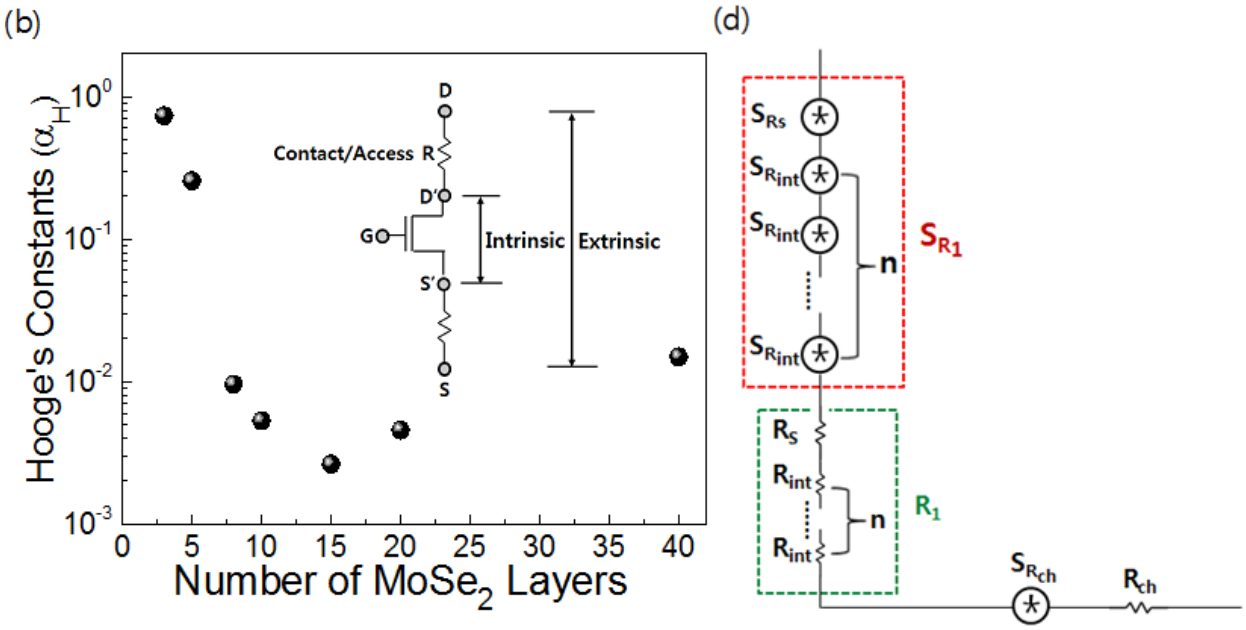


Fig. 3.6 Comparison of noise parameters at 10V overdrive voltage (a) The comparison of normalized noise amplitudes (Total, Channel, Contact/Access) for FETs with different number of $MoSe_2$ layers. All the noise measurements are performed at V_{gs}-V_{th}=10V, frequency of 100Hz and low drain bias (V_{ds}=50mV). (b) Hooge's constants (α_H) as a function of number of layers in $MoSe_2$ FETs. The inset shows schematic representation of the intrinsic and extrinsic FETs. (c) Representation of total noise originating from three independent current noise sources, namely, contact resistance, interlayer coupling resistance, and the channel resistance. (d) Thevenin equivalent resistance noise sources are shown.

Fig. 3.6 continued



3.4 Conclusion

In conclusion, in the present work we have provided a comprehensive study of the correlation between the electrical transport and 1/*f* noise studies in $MoSe_2$ FETs with varying channel layer thicknesses. The obtained mobility versus layer thickness of $MoSe_2$ FETs can be understood in terms of an intrinsic component associated with the channel and a component attributed to contact/interlayer coupling resistance, which both change with layer thickness. The gate-voltage dependence of the noise amplitude can be understood in terms of a voltage-dependent channel-dominated component and a voltage-independent contact/access dominated regime. A quantitative model is developed which adequately describes the observed voltage dependence, and which allows extraction of channel versus contact/access parameters for each layer thickness. Although previous studies on multi-layer TMDC FETs have attributed voltage dependence of noise amplitude to a transition from Hooge noise mechanism to McWhorter behavior, a model considering both channel and contact/access resistance contributions can fit the observed voltage dependence for devices across the full range of layer thicknesses using only one mechanism (Hooge's mobility fluctuation). The Hooge's constant (2.64×10^{-3}) extracted from

the channel-dominated regime for the 15-layer device is comparable to values reported for reliable nanoscale FETs.

Table 3.1 The electrical transport parameters and noise parameters of $MoSe_2$ field-effect transistors with various channel thicknesses studied in this work.

# of Layers	V_{th} (V)	L x W (μm^2)	R_1 (kΩ)	S_{R1} (Ω^2/Hz)	α_H	Voltage of Cross point (V)
3	9	1.9 x 3	141	1014	0.7	20
5	17	2 x 1.8	210	925	0.26	17
8	10	0.5 x 3	12	0.33	0.0098	22
8	12	1 x 3	20	0.82	0.0092	20
8	13	2 x 4	32	2.09	0.0095	19
10	18	1.9 x 2.1	54	5	0.005	16
15	13	2 x 1.8	21	0.275	0.0026	19
20	10	2 x 1.9	30	0.77	0.0045	20
40	11	1.8 x 2.2	187	137	0.0015	9

3.5 Supplementary Information

3.5.1 Device fabrication

Using mechanical exfoliation technique, high quality crystalline $MoSe_2$ flakes (from *2D Semiconductor, Inc.*) were transferred onto highly doped Si/SiO_2 wafers (SiO_2 thickness of 90nm) with pre-defined alignment markers. $MoSe_2$ flakes were first identified using an optical microscope, and the thickness of each flake was determined using an atomic force microscope (AFM). FETs were fabricated using seven of the $MoSe_2$ flakes, with thicknesses listed in Table 1, as the channel material. Source and drain (S/D) contact electrodes were defined by e-beam lithography (Raith e_LiNE) followed by 50 nm nickel e-beam evaporation and liftoff.

A Keithley 4200 semiconductor parameter analyzer and probe station were used for the transport measurements and an Agilent Technologies 35670A dynamic signal analyzer, low noise current pre-amplifier (Stanford Research SR570), and voltage source were used for the 1/*f* noise

measurement. All the grounding terminals from the equipment were connected to an instrument ground system.

3.5.2 Extraction of Series Resistance for the $MoSe_2$ FETs

The series resistance (R_1) is extracted from the measured device resistance versus gate voltage relationship, by plotting the total resistance (R_{total}) vs. 1 / (V_{gs}-V_{th}) and extrapolating the line to the y-axis (Fig. 3.7). The extracted R_1 was employed for the analysis of mobility and noise parameters. For 15L and 40L, the series resistances were 21 kΩ and 187 kΩ, respectively.

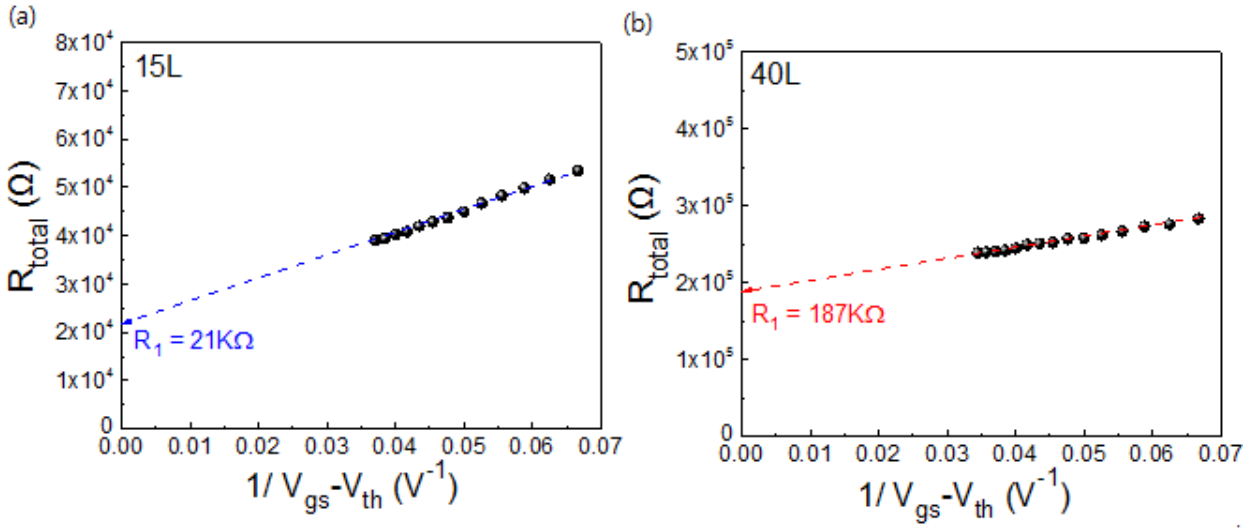


Fig. 3.7 Total resistance vs. 1 / (V_{gs}-V_{th}) for the extraction of series resistance, (a) 15L and (b) 40L.

3.5.3 Extraction of Field-Effect mobility for $MoSe_2$ FETs

The transconductance is obtained by first order differentiation of the transfer characteristic (Fig. 3.8). The peak g_m is then used to calculate the extrinsic field effect mobility was obtained by using the equation $\mu_{ext} = \frac{dI_{ds}}{dV_{gs}} * \frac{L}{W} * \frac{1}{C_{ox}} * \frac{1}{V_{ds}}$.

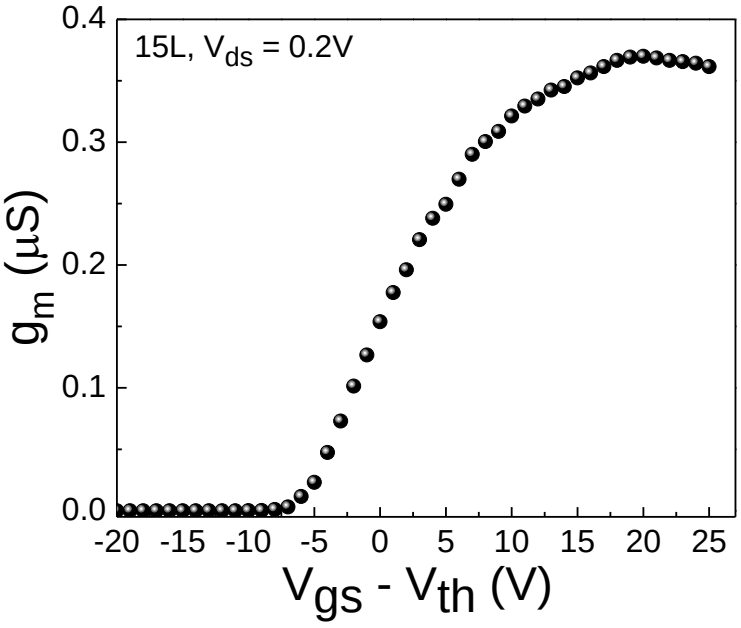


Fig. 3.8 Transconductance (g_m) as a function of the overdrive voltage (V_{gs}-V_{th}) at V_{ds}=0.2V for 15L $MoSe_2$ FET.

3.5.4 Noise amplitude and noise/resistance components in $MoSe_2$ FETs with various number of layers

The measured and modeled noise amplitudes are presented in this section for FETs with various layer thicknesses (15L and 40L results presented in main article). For each device, the $f*S_I/I_{ds}^2$ is shown versus (V_{gs}-V_{th}) and the resistances and noise resistance spectral power densities associated with channel and contact/access regions are presented.

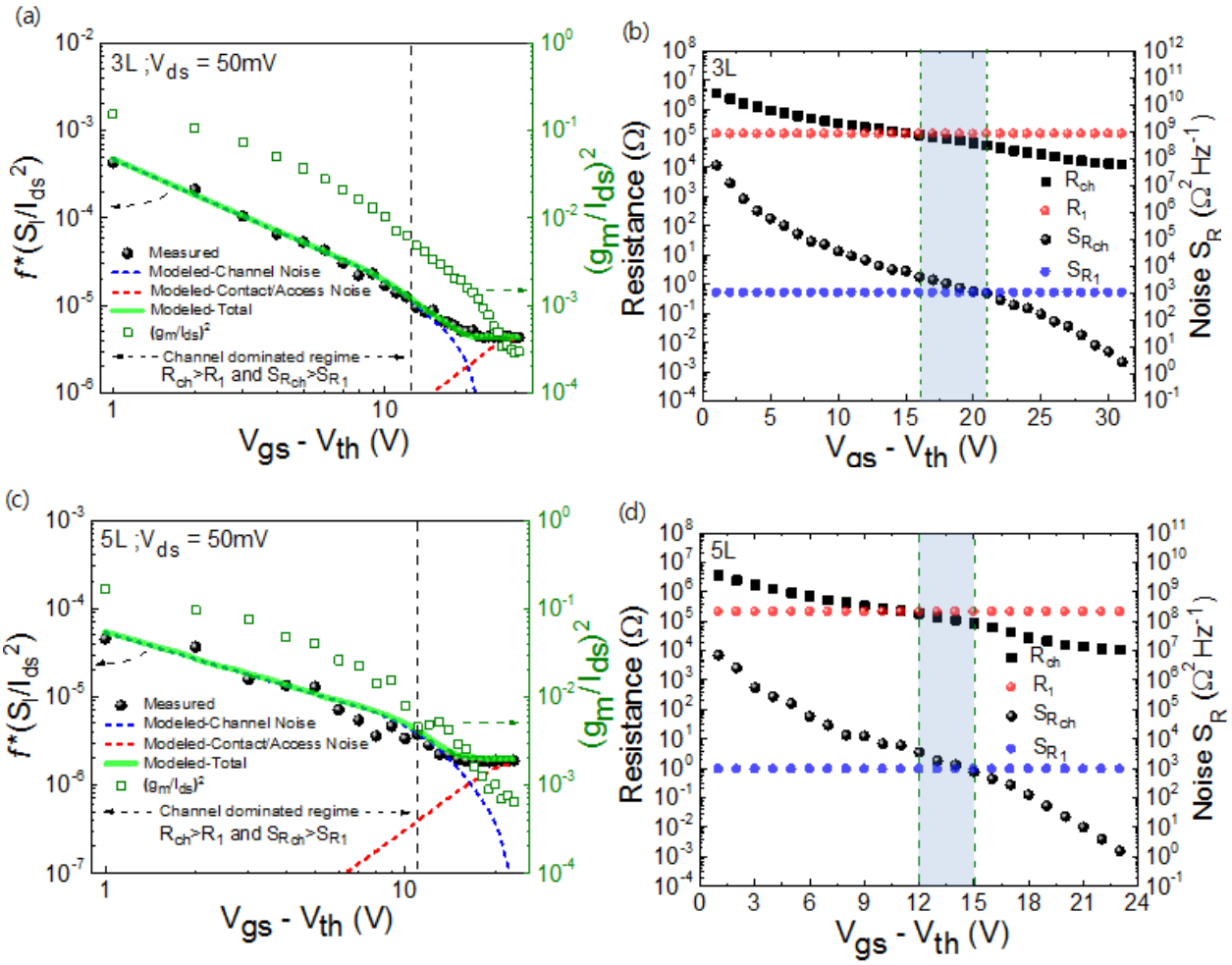
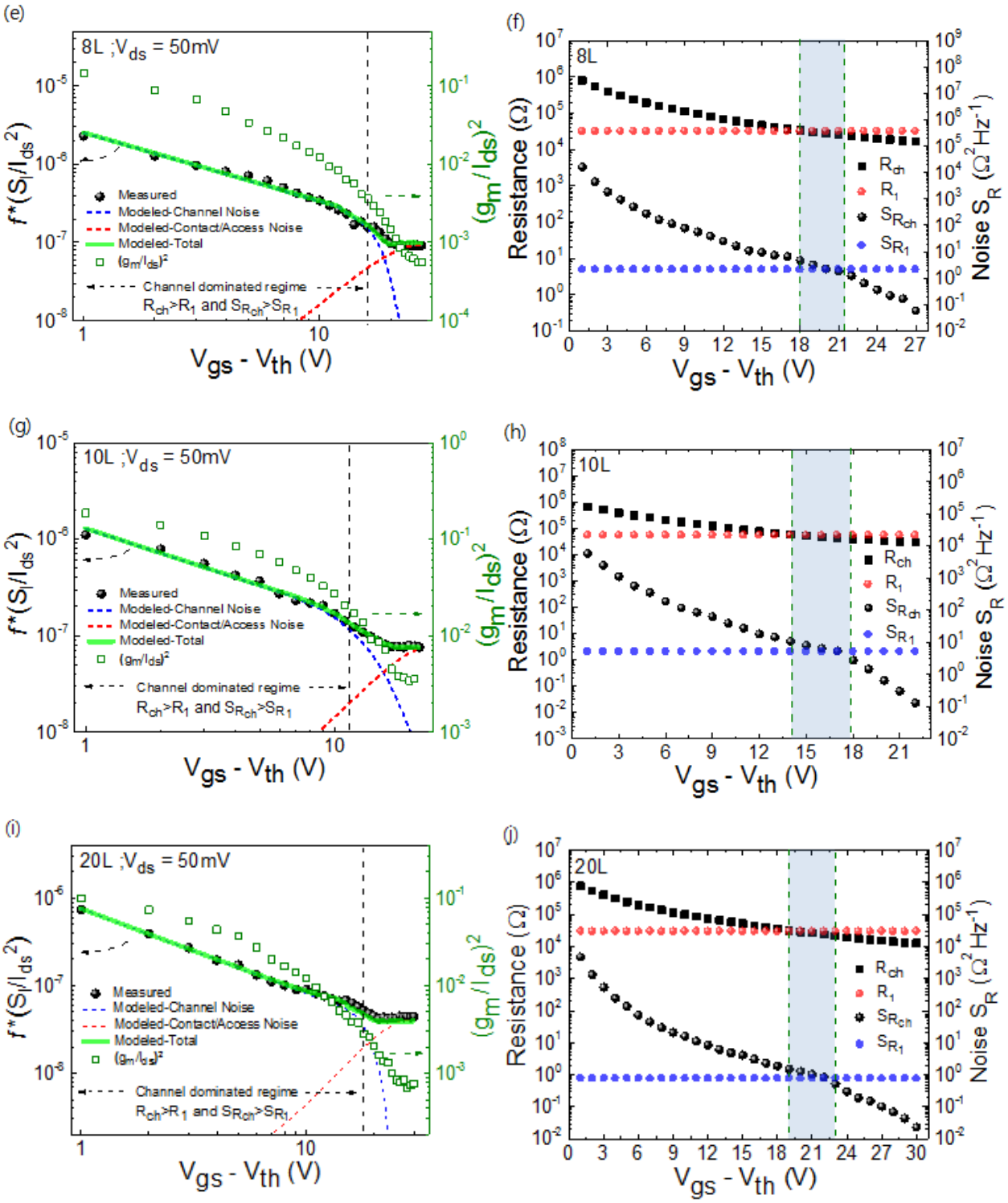


Fig. 3.9 (a), (c), (e), (g) and (i): Measured and modeled 1/*f* noise response of $MoSe_2$ FETs versus overdrive voltage. The round symbols represent the measured data points for the normalized noise current power spectral density, $f*S_I/I_{ds}^2$, as a function of the gate bias. The dashed lines represent the model fitting for the corresponding noise amplitude due to noise sources in the channel (Blue) and the contact contribution (Red). The green line shows the total modeled noise amplitude (sum of the two components). Green opened square corresponds to $(g_m/I_{ds})^2$ in the right-sided y axis. (b), (d), (f), (h) and (j): Contact and channel components of the resistance noise power density and resistance for $MoSe_2$ FET, obtained from measurements using procedure described in text. Blue area represents 'transition regime' in which channel dominates noise but contact/access regions dominate resistance. (a), (b) for 3L, (c),(d) for 5L, (e),(f) for 8L, (g),(h) for 10L and (i),(j) for 20L.

Fig. 3.9 continued



3.5.5 Noise amplitude and $(g_m/I_{ds})^2$ in 3L $MoSe_2$ FETs with various channel lengths

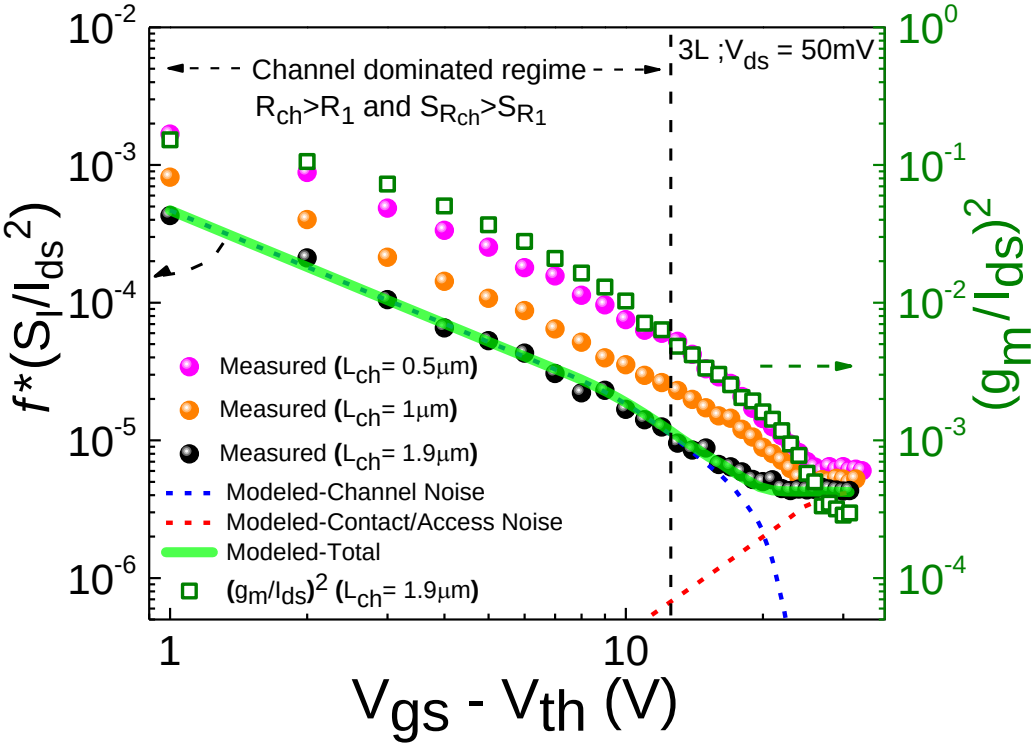


Fig. 3.10 The noise amplitudes $(f*S_I/I_{ds}^2)$ and $(g_m/I_{ds})^2$ as a function of overdrive voltage in 3L $MoSe_2$ FETs. Pink, orange and black circle represent the noise amplitude of $L_{ch.}$= 0.5μm, 1μm and 1.9μm, respectively. The blue (red) dashed line indicates the model fitting for the noise in the channel (contact) regime. Green opened square corresponds to $(g_m/I_{ds})^2$. Arrows indicate the appropriate axis.

Table 3.2 The parameters showing electrical properties and noise phenomenon in 3L $MoSe_2$ FETs with different channel lengths.

# of Layers	L x W (μm^2)	R_1 (kΩ)	V_{th} (V)	S_{R1} (Ω^2/Hz)	α_H
3	0.5 x 4	43	7	197.5	0.84
3	1 x 4	65	8	422	0.82
3	1.9 x 3	141	9	1014	0.7

3.5.6 The area-dependence of noise in 3L and 8L $MoSe_2$ FETs

In order to verify that the noise amplitude scales as expected with area in the channel-dominated regime, the area dependence of noise for 3L and 8L FETs is presented in this section. Figure F shows the noise parameter multiplied by area (Area*S_I/I_{ds}^2) versus the overdrive voltage (V_{gs}-V_{th}) in 3L and 8L FETs. For each set of devices, the curves for various channel lengths are comparable in the channel-dominated regime (at the low overdrive voltages) but reach different limiting values in the contact-dominated regime (at high overdrive voltages).

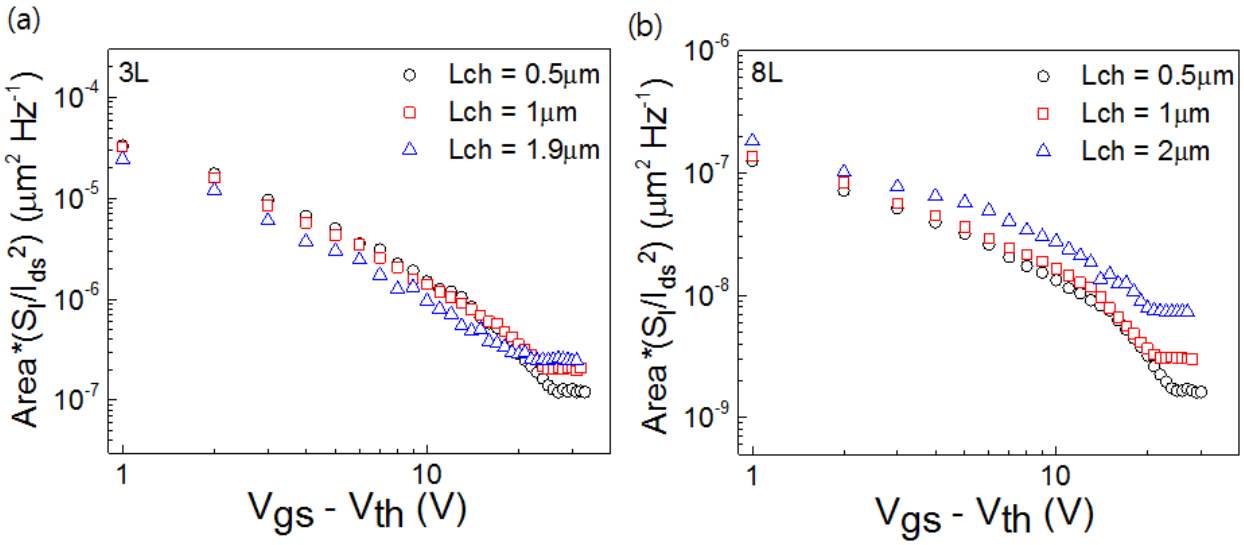


Fig. 3.11 The noise parameter (Area*S_I/I_{ds}^2) as a function of overdrive voltage in (a) 3L and (b) 8L $MoSe_2$ FETs. Black circle, red square and blue triangle represent the noise parameters of L_{ch} = 0.5μm (0.5μm), 1μm (1μm) and 1.9μm (2μm) in 3L (8L) $MoSe_2$ FETs, respectively.

4. NOISE RESPONSES IN HIGH-PERFORMCECE MO-CONTACTED MOS_2 FIELD-EFFECT TRANSISTORS

4.1 Transitions between Channel and Contact Regimes of Low-Frequency Noise in Many-Layer MoS_2 Field-Effect Transistors

4.1.1 Introduction

The isolation of van der Waal's solids scaled down to single atomic layers has allowed tunable electronic and optical properties of TMD materials, a topic of great scientific and technological interest [11], [12], [99]. MoS_2 is widely studied for FET application due to its tunable bandgap, with bulk indirect bandgap of ~1.2 eV and single layer direct bandgap of ~1.8 eV respectively.[12], [100] The 1/*f* noise, an ubiquitous phenomena in electronic materials and devices, is of interest for emerging transistor technologies, including low dimensional FETs such as nanowire transistors, carbon nanotube and graphene transistors,[67]–[70], [74], [101] both in terms of insights into physical/interface properties and in terms of potential circuit performance. Several key aspects of MoS_2-based FET performance have been studied. The extrinsic (measured) mobility increases as the number of atomic layers is increased from 1 to ~ 10 to 20, then decreases with increasing layer thickness due to series resistances associated with contacts and interlayer coupling.[61], [96] While the contact barrier height can be controlled to some extent by varying the metal contact work function, Fermi level pinning of contacts has been reported for MoS_2 channels, limiting the achievable contact resistivity and resulting in a contact-metal dependent peak mobility.[55], [102], [103] A number of studies have measured 1/*f* noise in FETs using MoS_2 or other TMDs as channel materials.[72], [73], [79], [82], [104] These studies have generally shown that devices with single/few layer channels exhibit larger levels of noise than those with multi-layer channels. However, there is disparity in the apparent noise mechanism; some studies have attributed the 1/*f* noise to mobility fluctuation, while others conclude that number fluctuation or correlated mobility/noise fluctuation models can explain the data. While a few studies have extracted the contributions of contacts/access regions to the measured resistance and noise, [79], [105] most studies do not explicitly consider these contributions. The use of extrinsic characteristics, which include both channel and contact/access region effects, makes it difficult to draw specific conclusions regarding the dominant noise mechanism in the channel, or even to identify the onset of contact-dominated

behavior in the measured noise or resistance. It is important to understand the intrinsic (channel-dominated) properties of MoS_2 FETs in order to design high performance and low noise 2D-FETs or to allow direct comparison between various device structures and passivation approaches. In this letter we report the current-voltage and low frequency noise properties of MoS_2 FETs using three devices fabricated on the same MoS_2 flake of uniform thickness and with different channel lengths (1 µm, 2 µm and 4 µm channels lengths, respectively). The MoS_2 was in the thick atomic layer limit (142 layers), allowing to study the effect of contact/access resistance and their impact on 1/*f* noise. Molybdenum source/drain (S/D) contacts are employed and found to provide contact properties comparable to those expected based on the contact work function. The gate-voltage dependence of the noise amplitudes can be understood in terms of a channel contribution, which follows a mobility fluctuation model with comparable Hooge parameter for the three devices, and a contact/access region contribution which is independent of gate voltage. The approach for separating channel contributions from those of contact/access region allows clear evaluation of the channel noise mechanism, and also can be used to explain qualitative differences which were observed in the transition regions between contact- and channel-dominated for various devices.

4.1.2 Experimental Details

The MoS_2 devices were fabricated following a standard mechanical exfoliation procedure on MoS_2 single crystals (SPI supplies). A heavily doped Si/SiO_2 (p^{++} silicon with 100 nm oxide thickness) with predefined alignment markers was used as substrate, where the markers were used to locate the flake of interest. In the present case, an intentionally thicker MoS_2 flake was chosen for device fabrication. The thickness of the flake was confirmed using atomic force microscopy (Veeco Dimension 3100 scanning probe microscope) in tapping mode of operation. The microscopic crystal structure of the 2D layers of MoS_2 (A_{1g} and E^1_{2g} modes) was confirmed by Raman spectroscopy, measured using a Horiba Lab spec spectrometer using 532nm excitation. The FET devices were fabricated using e-beam lithography patterning and development, metallization, and liftoff. The contact electrodes and measurement pads were deposited by DC sputtering of 20 nm of molybdenum followed by 100 nm of gold. A semiconductor parameter analyzer (Keithley 4200) and probe station were used to measure the output characteristics and transfer characteristics of MoS_2 FETs. The 1/*f* noise measurements were performed using an

Agilent dynamic signal analyzer (35670A), a low noise current pre-amplifier (SR570). A low pass filter was connected to a voltage source (Keithley 263 Calibrator/Source) to maximally get rid of the noise present in the input DC voltage. All equipment was grounded together to remove any fluctuation of the electrical signal.

4.1.3 Results and Discussion

Fig. 4.1 (a) shows the schematic diagram of a representative MoS2 FETs with a back-gate configuration and Fig. 4.1 (b) shows a ~ 15 µm x 5 µm MoS_2 flake with three fabricated devices of 1 µm, 2 µm and 4 µm channel lengths, respectively. Since the three devices are on the same flake (of uniform optical contrast), the device to device variation in the channel thickness and S/D contact properties are expected to be modest, providing for a direct comparison between devices with various channel lengths. This is further confirmed by atomic force microscopy measurements. Fig. 4.1 (c) shows the atomic force microscope image and the depth profile of the MoS_2 channel, indicating a layer thickness of ~92.5 nm, corresponding to ~ 142 atomic layers. We have chosen such a thick layer channel in this study to particularly study the thick MoS_2 channel limit, where the contact resistance and access resistance from interlayer coupling could significantly affect the mobility of the charge carriers.

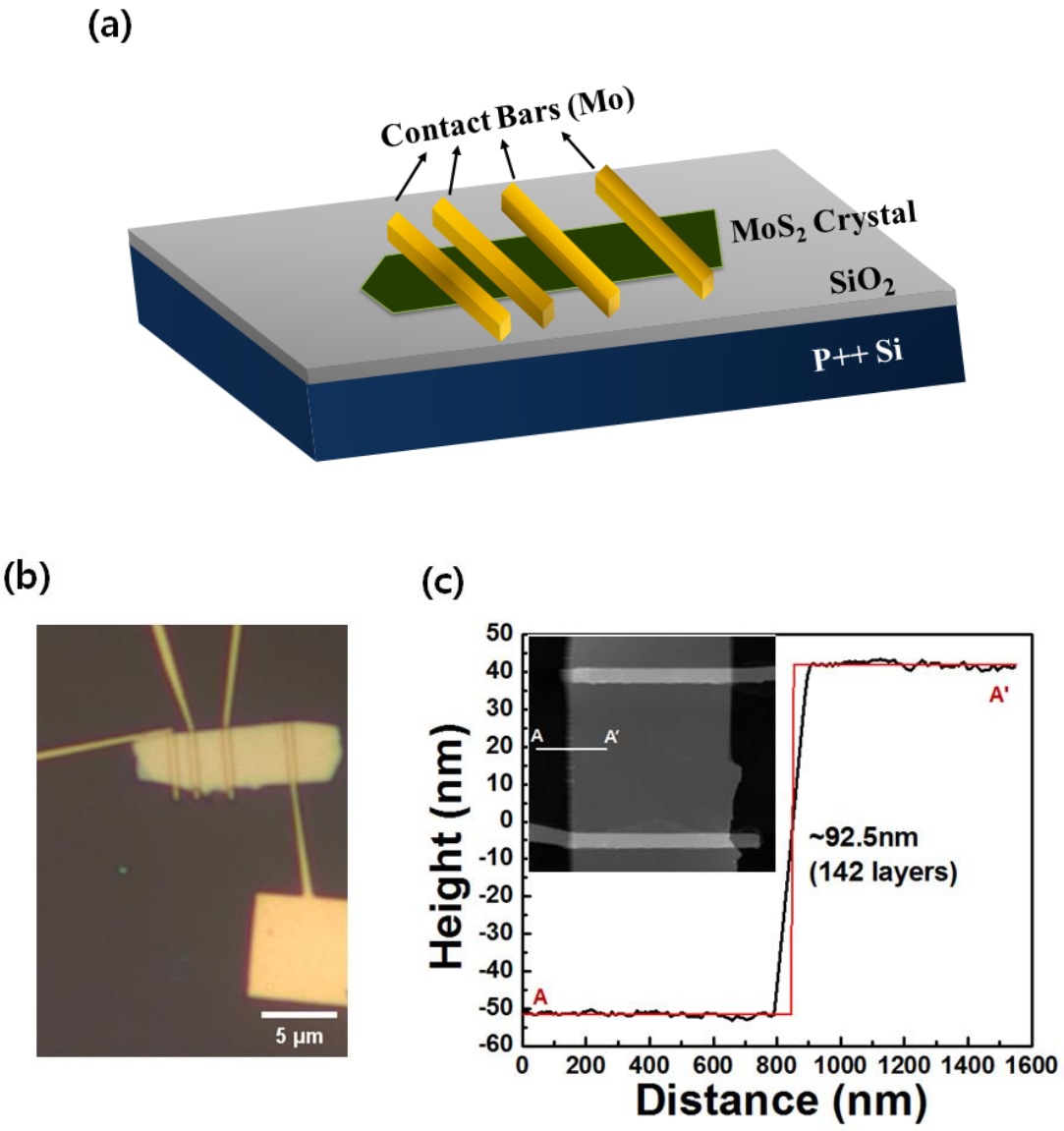


Fig. 4.1 (a) Schematic diagram of the back-gated MoS_2 Field-effect transistors (b) Optical image of multi-layer (142 Layers) MoS_2 field-effect transistors with different channel lengths of 1µm, 2µm and 4µm, respectively. (c) Cross sectional profile of MoS_2 flake. The inset shows the AFM image of the device along with the white line (A-A') showing the height of ~ 92.5nm (142 Layers).

Fig. 4.2 (a), Fig. 4.2 (c), and Fig. 4.2 (e) show the output characteristics of MoS_2 FETs with channel lengths (L_{ch}) of 1 µm, 2 µm and 4 µm respectively. For all three L_{ch} values, the devices show linear characteristics, indicating no Schottky barrier effects in I_d-V_{ds} characteristics. The drain currents decrease as L_{ch} increases, which is consistent with the MOSFET classical square-law model (i.e., $I_d \; \alpha \; 1/L_{ch}$). For all three devices, the screening length ($\lambda \sim \sqrt{t_{MoS_2} * t_{ox}}$) ~ 96 nm)

[61], [84] is much smaller than L_{ch}, indicating the long channel MOSFET model (with no current saturation at V_{gs} below or equal to V_{th}). However, the contacts and the interlayer coupling (characterized by device access resistance) as well as their noise contributions could be dominant at V_{gs} much beyond V_{th}. The noise characteristics in positive overdrive voltage will be discussed in later section. Fig. 4.2 (b), Fig. 4.2 (d), and Fig. 4.2 (f) show the transfer characteristics of MoS_2 FETs with 1 µm, 2 µm and 4 µm channel lengths respectively. A constant I_{on}/I_{off} of 10^5 is obtained for all devices with a slight decrease with shorter channel length. The field effect mobilities of the devices were calculated using $\mu_{FE,extrinsic} = \frac{\partial I_{ds}}{\partial V_{gs}} * \frac{L}{W} * \frac{1}{C_{ox}} * \frac{1}{V_{ds}}$, where L and W are the channel length and width, C_{ox} is the gate oxide capacitance per unit area ($3.4x10^{-4}$ F/m^2 for 100nm SiO_2) and are estimated to be 12.1 $cm^2/V{\cdot}s$, 13.4 $cm^2/V{\cdot}s$, and 15.8 $cm^2/V{\cdot}s$ for the devices with channel lengths of 1 µm, 2 µm and 4 µm respectively. These mobility values are much smaller than the field effect mobilities reported for multilayer MoS_2 FETs and are obtained due to the S/D contact resistance and the access resistances caused by the interlayer coupling of 2D semiconductor. However, the mobility value is comparable in the thick-layer limit from Das. et al. [61] The intrinsic mobility is calculated from the formula of the field effect mobility by using V_{ds}', where $V_{ds}' = V_{ds} * (R_{ch}/R_{total})$, R_{total} is the total device resistance and R_{ch} is the channel resistance). In fact, upon calculating the intrinsic channel mobilities, the values obtained are 26.7 $cm^2/V{\cdot}s$, 27.3 $cm^2/V{\cdot}s$, and 28.1 $cm^2/V{\cdot}s$ for the devices with channel lengths of 1 µm, 2 µm and 4 µm respectively. Such contact and access resistance of thick MoS_2 layer, as we will discuss, have distinct features in the $1/f$ noise characteristics at V_{gs} values above the threshold voltage of the devices.

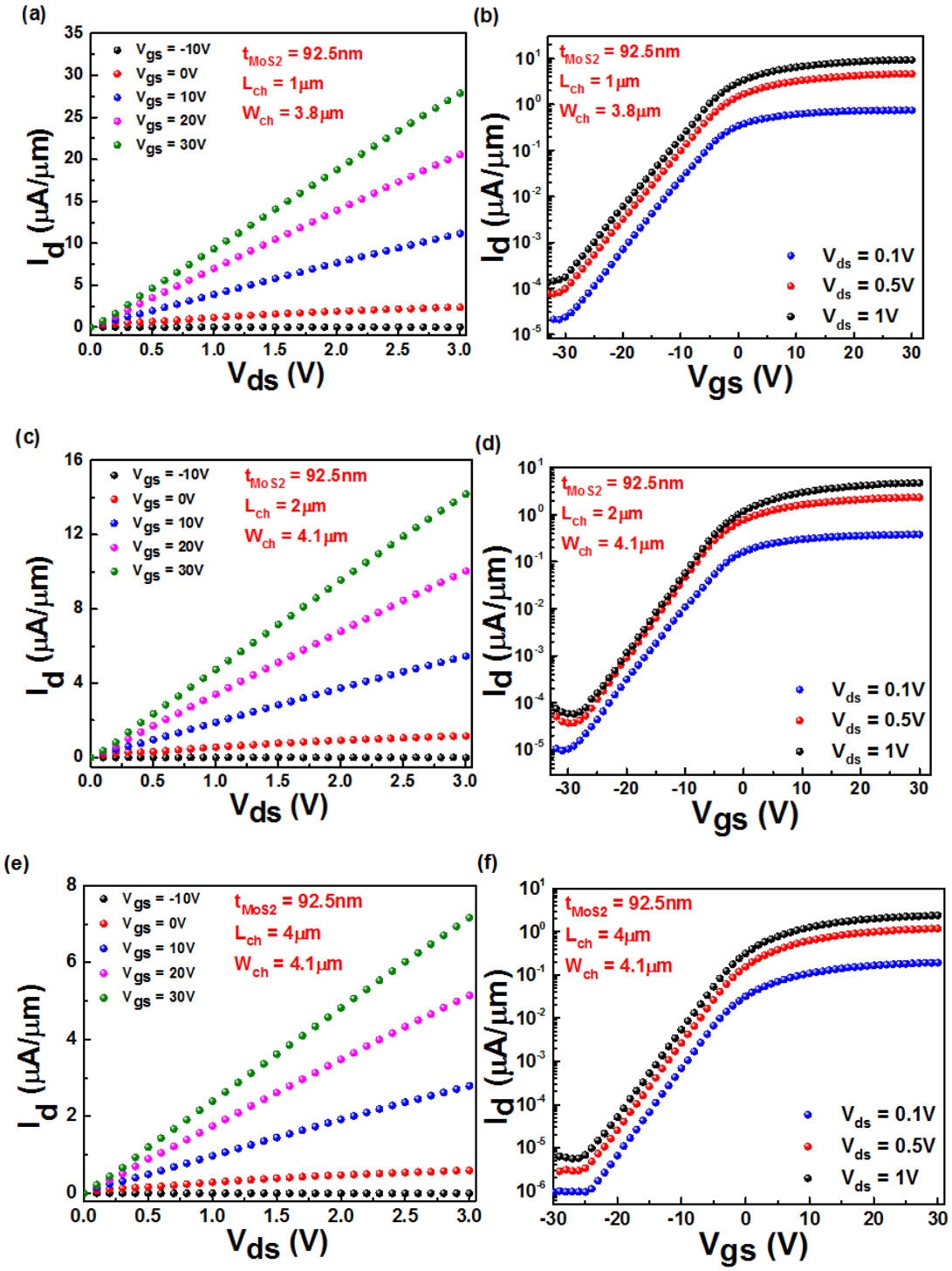


Fig. 4.2 (a), (b) and (c) Output characteristics of MoS_2 field-effect transistors with the channel lengths of 1μm, 2μm and 4μm, respectively. Back gate voltages are applied from 30V to -10V with a step of -10V. Drain voltages are swept from 0V to 3V. (d), (e) and (f) Transfer characteristics of the devices with the channel lengths of 1μm, 2μm and 4μm, respectively. Drain

voltages are applied from 0.1V to 1V with a step of 0.5V. Back gate voltages are swept from 30V to -30V.

Fig. 4.3 (a) shows the normalized noise current density vs. the frequency, where all three devices were operated at 50 mV drain bias and an over-drive voltage ($V_{GS} - V_{TH}$) of 6V. All three devices show 1/*f* noise characteristics (1/*f* relationship is shown (dotted line) for visual guidance). The inset shows the circuit configuration which will be used in subsequent analysis, including noise sources (S_{R1}: the resistance noise power spectral density for the series resistance (consisting of both contact resistance and the interlayer coupling) and S_{Rch}: the resistance noise power spectral density for the channel resistance) along with the series resistance (R_1) and the channel resistance (R_{ch}). Because the series resistance is very important to understand for MoS_2 devices and their noise, both the metal contacts and MoS_2 channel material contributions are considered to the noise analysis. The normalized device noise could be represented as a sum of the noise component as follows:

$$\frac{S_{Rtotal}}{R_{total}^2} = \frac{S_{R1}+S_{Rch}}{(R_1+R_{ch})^2} \tag{4.1}$$

with $R_{total} = R_1 + R_{ch}$. Under specific conditions, the device might have $S_{R1} > S_{Rch}$ or $S_{R1} < S_{Rch}$, and independently $R_1 > R_{ch}$ or $R_1 < R_{ch}$, exhibiting to four distinct regions of dominant behavior. To illustrate the normalized noise spectral density versus gate voltage, Fig. 4.3 (b) plots the noise measured at 100 Hz frequency vs. $V_{gs} - V_{th}$ of the three devices. Clearly, three different noise regimes are evident in these devices. In the first regime, at low over-drive voltages (up to 9V for device with 1 µm channel and 13V for device with 4 µm channel), the noise is inversely proportional to the overdrive voltage (i.e., noise ~ $(V_{gs}-V_{th})^{-1}$). This regime is associated with the channel dominating both the noise and resistance, and follows the behavior expected for a mobility-fluctuation (Hooge) model: ($f * S_I / I_d^2 \sim \alpha_{H,ch} / N_{ch} \sim V_{gs}^{-1}$). [84] Extracting the Hooge parameter in the channel-dominated regime yields $\alpha_{H,ch} \sim 5.13\text{x}10^{-2}$, $6.09\text{x}10^{-2}$, and $6.15\text{x}10^{-2}$ for the FETs with channel lengths of 1 µm, 2 µm and 4 µm respectively. The observation that the Hooge parameter is nearly independent of the channel length is as expected for mobility fluctuation model, in which $A \propto 1/N_{ch}$ ($\propto 1/L_{ch}$), where A is the noise amplitude and N_{ch} is the total number of carriers in the channel. In the second regime, at very high over-drive voltage values (beyond 20V), the normalized noise current density becomes gate voltage independent

(i.e., noise ~ V_{gs}^{0}), a characteristic that is attributed to the contact/access resistances dominating both resistance and noise. The third regime is a transition regime between channel-dominated (noise ~ V_{gs}^{-1}) and contact-dominated (noise ~ V_{gs}^{0}) behavior. The three devices exhibit qualitatively different behavior in this transition regime, indicating ~ V_{gs}^{-3} and ~ V_{gs}^{+2} regions for the 1 µm and 4 µm devices, respectively. The noise amplitude for the 2 µm device makes a more direct transition between the channel- and contact- dominated regimes, consistent with our prior studies of $MoSe_2$ FETs with a variety of channel thicknesses (thickness between 3 atomic layers to 40 atomic layers). [105]

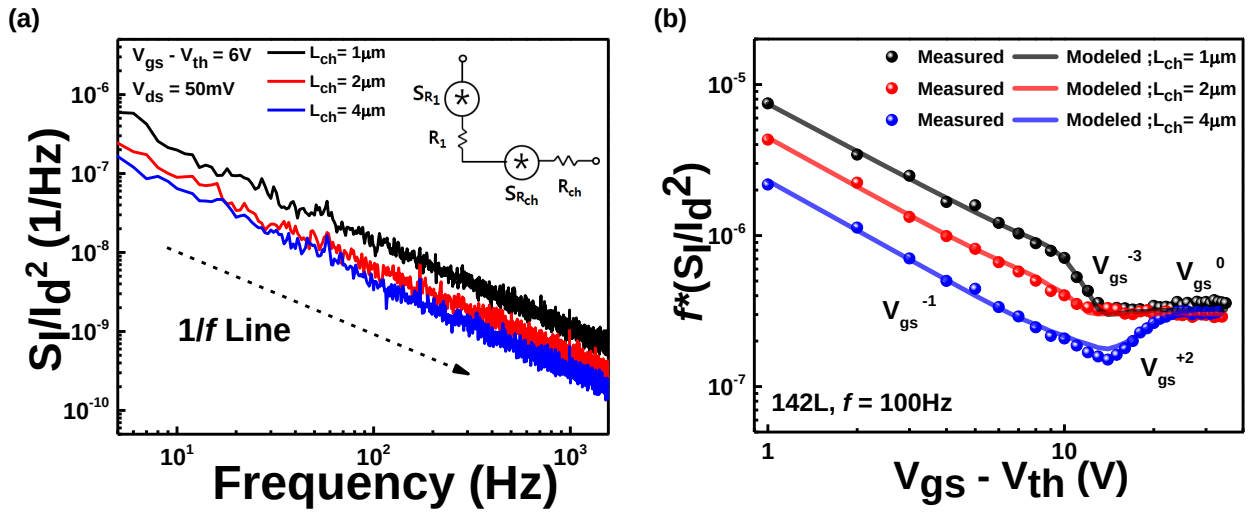


Fig. 4.3 (a) 1/*f* noise current power spectral density for MoS_2 FETs with various channel lengths as a function of frequency at V_{gs}-V_{th} = 6V (Channel contribution). The inset shows the circuit diagram representing the noise sources from the series resistance (R_1) and the channel resistance (R_{ch}). (b) Measured and modeled 1/*f* noise behaviors of MoS_2 FETs with various channel lengths [L_{ch} = 1µm (Black), 2µm (Red) and 4µm (Blue)]. The round symbols represent the measured data for the noise amplitude ($f*S_I/I_d^2$) in terms of the applied gate voltage. The solid lines mean the total of measured data for the contributions of contact/access and channel. Moreover, both results in the channel dominated regime (V_{gs}^{-1}) are explained with the mobility fluctuation model (Hooge's model).

To illustrate the relative contributions of channel and contact, and the V_{gs}^{m} dependence of noise spectral density (with m = -1, -3, +2 and 0), Fig. 4.4 shows the resistance and the noise sources extracted from the channel as well as the combination of S/D contact and interlayer coupling of MoS_2. Fig. 4.4 (a) – (c) show the contact/access and channel components of the noise (S_{R1} and S_{Rch}, respectively) and resistance (R_1 and R_{Ch}, respectively) parameters for devices

with 1 µm, 2 µm, and 4 µm channel lengths respectively. The shaded area (the blue area) in each of these graphs, Fig. 4.4 (a) and (b), indicates the transition between point at which the resistance (R) becomes dominated by R_1 but the noise (S) is still dominated by S_{Rch}. For the 4 µm device, the green area of Fig. 4.4 (c) shows the regime in which the noise is dominated by S_{R1} but the resistance is dominated by R_{ch}. These transition regions correspond to the approximate voltage ranges over which we observe the transitions between ~ V_{gs}^{-1} and ~ V_{gs}^{0}) regimes in Fig. 4.3 (b). The relative order of cross-over observed in the three devices (resistance first, noise and resistance at nearly same voltage, noise first) have previously been shown to yield the ~ V_{gs}^{-3}, direct transition, and ~ V_{gs}^{+2} behavior for plots comparable to Fig. 4.3 (b), respectively. [67], [97], [106] For comparison of 1/f noise mechanism in the three devices, the transition from channel dominated to contact dominated regime is shown in Fig. 4.4 (d). Four quadrants with different gate voltage exponent 'm', discussed earlier, are shown in this plot. For the comparison of the threshold voltages of the three devices, they are obtained by linearly fitting the low-filed transfer characteristic relationship to I_d=0. So V_{th} is -5V (-4V) (-3V) for L_{ch}=1µm (2µm) (4µm), respectively. In order to calculate the noise parameters S_{R1} and S_{Rch}, the total noise amplitude ($f \cdot S_I / I_d^2$) is used with the resistances R_{total}, R_1 and R_{ch}. First, Hooge's constant is extracted at small overdrive voltage regime. Then, the value of S_{Rch} at the highest overdrive voltage is calculated using the Hooge relationship. S_{R1} value is calculated by evaluating Eq. (4.1) at this overdrive voltage with R_1 and R_{ch}, S_{Rch} and S_I / I_d^2 at this voltage. Finally, S_{Rch} is determined at other overdrive voltage using Eq. (4.1) with the corresponding R_{ch} and measured S_I / I_d^2. The extracted S_{R1} and S_{Rch} in the devices with different channel lengths are shown in Fig. 4.4 (a) ~ (c).

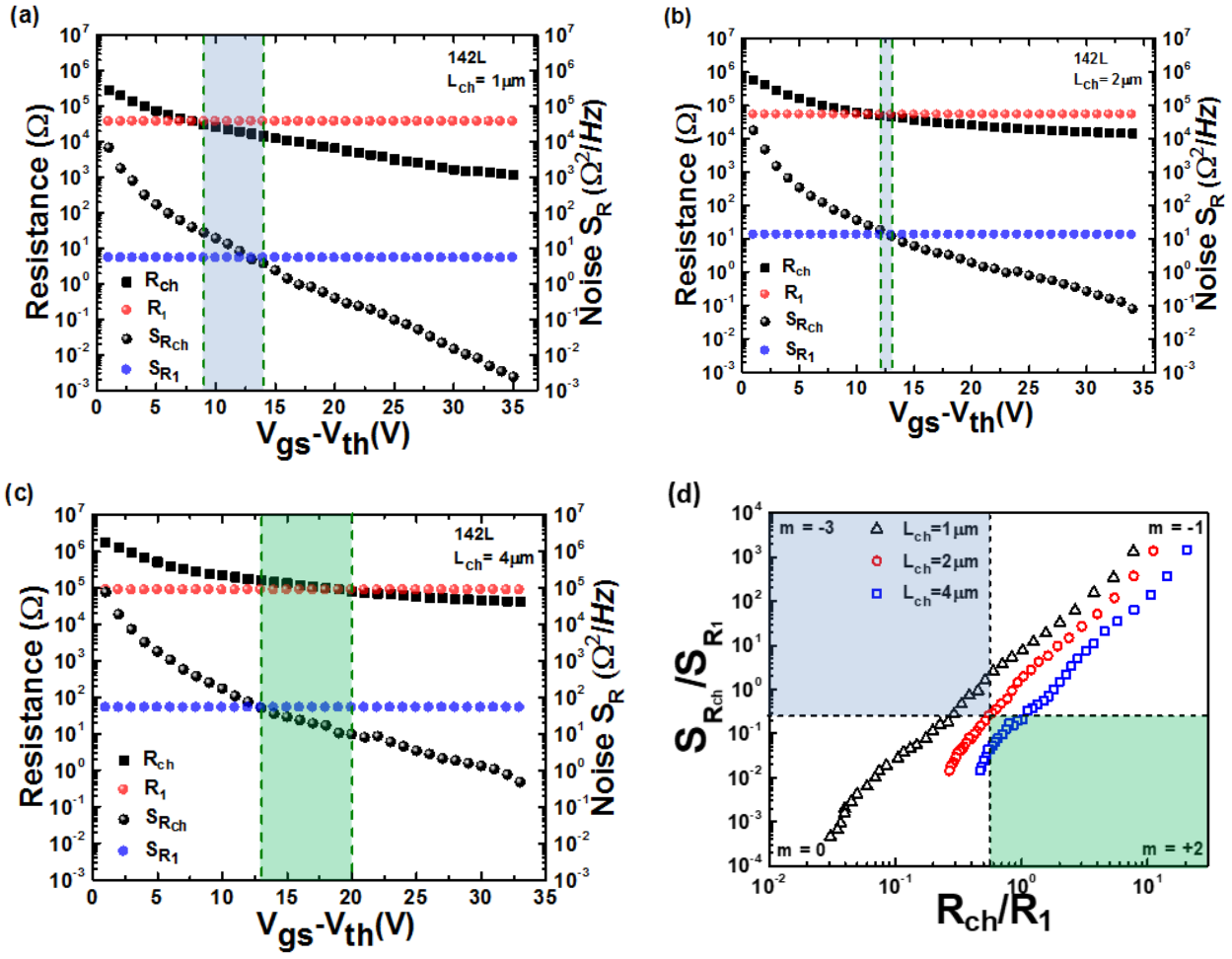


Fig. 4.4 Contact and channel components of the noise and resistance for MoS_2 FET (a) L_{ch} = 1μm, (b) L_{ch} = 2μm and (c) L_{ch} = 4μm. Blue area region (V_{gs}^{-3}) in Fig. 4.4 (a) and (b) represents the regime in which channel is dominating S_R but contact/access is dominating R. Green area region (V_{gs}^{+2}) in Fig. 4.4 (c) represents the regime in which contact/access is dominating S_R but channel is dominating R. Fig. 4.4 (d) represents the relation between normalized channel noise to contact/access noise vs. normalized channel resistance to contact/access resistance of the three devices, clearly showing the difference between the noise trend in devices with different channel length.

4.1.4 Conclusion

We examined the 1/*f* noise in MoS2 FETs with many-atomic layer channel and with various channel lengths. The thick channel is specifically chosen as it demonstrates contact/access resistance limited mobility. The voltage-dependent noise in each device exhibits a channel-dominated regime which follows clear Vgs^{-1}, corresponding to a mobility fluctuation (Hooge model) as the dominant noise mechanism. In this regime, the noise amplitude $A \propto 1/N_{ch}$ ($\propto 1/L_{ch}$),

indicating that the Hooge constant is independent of channel length. At large overdrive voltages, the noise and resistance behavior becomes dominated by contributions from the contact/access regions. The three devices show qualitatively different behavior in the transition region between channel- and contact/access- dominated regimes. The various gate voltage exponents in the transition regions can be explained in terms of the relative voltages at which the noise and resistance cross from channel to contact/access dominated behavior. While our present study demonstrates the validity of a single noise mechanism (i.e. mobility fluctuation) in these MoS2 FETs, it also provides further guidelines to effectively design high performance 2D-semiconductor FETs with low contact resistance and low noise characteristics.

4.2 Molybdenum Contacts to MoS_2 Field-Effect Transistors: Schottky-Barrier Extraction, Electrical Transport and Low-Frequency Noise

4.2.1 Introduction

Since the first reported FET on single atomic layer MoS_2, there have been great successes in the transition metal dichalcogenides (TMDCs) for the study of 2D FETs.[11], [107] While these materials and associated van der Waals (vdW) heterostructures are of interest for transistors and sensors, they also possess number of properties of interest for optoelectronics (e.g., phototransistors), spintronics, and valleytronics.[17], [108]–[111] TMDCs provide an ideal platform to study devices with atomic-thin channels, yet they are prone to issues associated with ambient conditions, defects generation during materials synthesis and interface traps in the device structure, including the choice of metals to form metallurgical contacts (e.g., source and drain electrodes) used in FETs.[103], [112]–[118] Therefore, understanding the above device details, including channel thickness (number of atomic layers), and their impact on transistor characteristics are key factors for their successful applications. For example, ambient operation of MoS_2 FETs has shown their surface sensitivity to adsorption of water molecules and subsequent desorption upon vacuum annealing and/or surface passivation, explaining the typical hysteresis observed in these FETs.[119] Recently, an alternative physical explanation of this hysteresis, in terms of the intrinsic nature of the atomic layers, has emerged. The hysteresis is shown as a result of the magnitude and duration of electrostatic stress generated and presented in the 2D membrane with a strong dependence on the number of layers present in the FET channel.[120] MoS_2 with its bulk energy gap of 1.2 eV and monolayer energy gap of 1.8 eV,

respectively at room temperature, possesses weak vdW coupling between adjacent layers that is key to the unique electronic and optical properties in the lower thickness limit, such as direct to indirect band gap transition and tunable band gap energies.[12], [121] Therefore, while in a sense MoS_2 FETs show atomic thin channel characteristics, the transport physics of FETs with multilayer MoS_2 necessitates understanding of layer number dependent transconductance (or mobility), contact resistance, etc. Recently, there has been a growing number of transport studies on MoS_2 devices with various channel thicknesses, addressing the impact of channel thickness on the above properties.[122], [123] A number of contact metals with different work function (WF) values have been used to understand the Schottky barrier effects arising from metal-MoS_2 interface,[55], [116], [124]–[126] including metals with high work function (e.g., gold, palladium, platinum, cobalt, nickel, etc.) and low work function (e.g., scandium, aluminum, titanium, etc.). Walia et al. have shown that metal contacts with WF between 4.5 to 5.7 eV (e.g., Al, W, Au, and Pt) always show a Schottky barrier effect.[124] The impact of these metals on Schottky barriers and the transport physics is critical in explaining the mechanism of charge carrier injection from the metal to the semiconductor. While a metal with high WF creates a higher Schottky barrier height, causing low electron thermionic emission (and hence low current injection into the conduction band), a metal with low WF is generally provide other challenges, namely, reactive nature, unreliable morphology formation (e.g., in case of Ti) at the contact interface and/or contact-induced doping (e.g., in case of Al).[127], [128] Molybdenum, with WF of 4.3-4.5 eV, has number of advantageous properties such as high strength and high melting point, low thermal expansion and low reactivity to ambient (e.g., oxygen, moisture etc.). Molybdenum has been studied previously for source and drain contacts for MoS_2 FETs.[129], [130] However, a complete picture of the behavior of these electrodes in MoS_2 FETs requires an understanding of the channel thickness dependence of the device properties. Earlier, our work on $MoSe_2$ FETs with Ni contacts has shown a mobility maximum when the channel thickness is between 10 and 15 atomic layers, consistent with reported results for studies with metal S/D of various WFs.[105] A mobility maximum, consistent with an earlier proposed interlayer coupling between the vdW layers, has not been shown in MoS_2 FETs with Mo S/D contact electrodes.[55], [105], [131] In this work we have extended the validity of the field effect mobility maximum with channel thickness and have studied the temperature dependent transport characteristics of the FET with optimum mobility to extract the Mo-MoS_2 Schottky barrier height and the

temperature dependent mobility effects. We have also studied the low frequency noise in the MoS_2 FETs with various channel thicknesses.

4.2.2 Experimental Details

Single crystal MoS_2 flakes (SPI supplies, Inc.) of tens of square micrometer area and with various atomic thickness, mechanically exfoliated, were first transferred onto heavily doped Si/SiO_2 (p^{++} silicon/100 nm oxide thickness) with predefined alignment markers. The layer numbers, represented by the flake thicknesses, were routinely characterized and determined by atomic force microscopy (AFM) imaging and Raman spectroscopy. Flakes of five thicknesses (10L, 12L, 20L, 45L, and 116L) were selected for the device fabrication, where L stands for a monolayer of MoS_2 (0.65 nm thick). Standard electron-beam lithographic processes, followed by metallization and liftoff, were conducted for the FET device fabrication. Molybdenum metal of 20 nm thick was directly deposited onto the S/D patterned region on MoS_2 using a DC sputtering, followed by a 100 nm gold deposition without breaking the high vacuum inside the sputtering chamber. A Lakeshore probe station with Keithley 4200 semiconductor parameter analyzer were used to measure the output characteristics and transfer characteristics of MoS_2 FETs. The probe station was equipped with both high temperature measurements and low temperature measurements using liquid nitrogen flow and a temperature controller arrangement. An Agilent Technology dynamic signal analyzer (35670A), low-noise current pre-amplifier (SR570) and a home-made low pass filter circuit connected to a voltage source (Keithley 263 Calibrator/Source) were used to measure the low-frequency noise in the devices. To avoid any fluctuations from the electrical supply, the equipment was grounded with the main ground potential.

4.2.3 Results and Discussion

Fig. 4.5 (a) shows the transfer characteristics (and inset shows the output characteristics) of the MoS_2 FETs with Mo S/D contact electrodes and with different channel thicknesses mentioned above. The device with a channel thickness of 7.97 nm thick (corresponding to 12 atomic layers of MoS_2) is shown in Fig. 4.5 (c) [optical microscope images of the flake, the device and the AFM step profile are shown]. All the devices were biased with a drain-source voltage (V_{DS}) of 500 mV voltage and the drain current (I_{ds}) was normalized with the width of the channel to compare the characteristics of the MoS_2/Mo FETs. As seen in the output characteristics, at an

overdrive voltage of 7V corresponding to the ON state of the devices, the drain current increases when the channel thickness increases from 10L to 12L, after which I_{ds} significantly decreases. Such trend in I_{ds} with channel thickness (t) and with other device parameters (e.g., channel length (L), channel width (W), oxide capacitance (C_{ox})) were further used to extract the field effect electronic mobility using $\mu_{FE,extrinsic} = \frac{\partial I_{ds}}{\partial V_{gs}} * \frac{L}{W} * \frac{1}{C_{ox}} * \frac{1}{V_{ds}}$, where $\mu_{FE,extrinsic}$ is extrinsic field effect mobility. The $\mu_{FE,extrinsic}$ increases as the MoS_2 thickness increases from 10L to 12L followed by a monotonic decrease as the channel thickness further increases (Fig. 4.5 (b)). The trends in $\mu_{FE,extrinsic}$ and I_{ds} were earlier seen in $Mo(S/Se)_2$ FETs with other metal S/D electrodes, including our recent work on $MoSe_2$ FETs.[103], [105], [116]–[118], [131] Earlier we have provided analysis of extrinsic and intrinsic mobilities in $MoSe_2$ FETs with nickel S/D metal contacts and extracted the contact resistance and access resistances caused by the vdW interlayer coupling. Therefore, the mobility vs. layer thickness nature observed in this study on Mo contacted MoS_2 FETs follows a general trend shown by previous TMDC materials and FET devices. We have extracted the contact resistance of the devices that are consistent with the conductivity and mobility trend. The contact resistance of the 10L, 12L, 20L, 45L, and 116L are 36 kΩ.µm, 32 kΩ.µm, 60 kΩ.µm, 120 kΩ.µm, and 192 kΩ.µm respectively. Previously the contact resistance of MoS_2 FETs with Mo contacts has been extracted in thin MoS_2 limits and/or a relatively thicker channel but a systematic nature of the thickness dependent contact resistance with Mo contact with wide thickness variation of MoS_2 has not been studied. [129], [130]

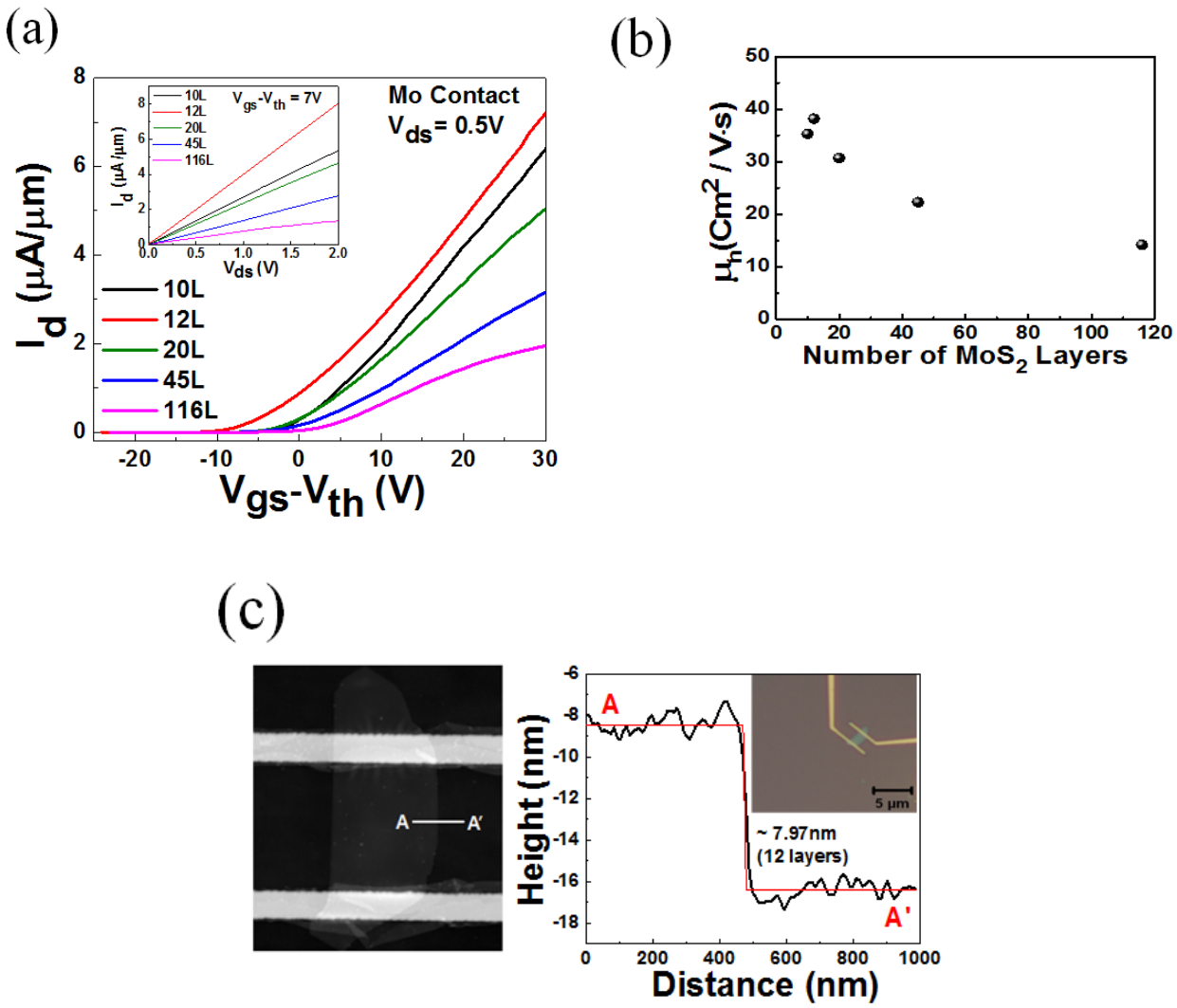


Fig. 4.5 (a) Transfer characteristics (linear scale) of molybdenum S/D contacted MoS_2 FETs with channel thicknesses of 10L, 12L, 20L, 45L, and 116L at 500 mV drain bias. Inset shows the output characteristics of the same devices at transistor ON state. (b) The extrinsic field-effect mobility vs. number of atomic layers in the FET channel. (c) AFM image of the FET device and height profile of the channel region (along AA'), showing a 12L MoS_2. The inset shows the optical image of the device (scale bar is ~5 μm).

Although the Hall mobility of bulk MoS_2 is predicted to be more than 100 cm^2/V s at room temperature (theoretical value of 400 cm^2/V s) with a temperature dependent mobility $\mu_{(Hall)} \alpha (T/T_0)^{-\gamma}$, with $\gamma \sim 2.6$, the device mobilities in MoS_2 FETs with channels of nanometer thin layers are limited by various factors.[132] Since in our case the 12L Mo-MoS_2 FET provided the highest mobility, highest electrical conductivity, and lowest contact resistance, we further analyze below the detailed characteristics of this device, including the study of field-effect

mobility and temperature dependence and the extraction of Schottky barrier height (SBH). Fig. 4.6 shows the temperature dependent I_d-V_{gs} characteristics (in both linear scale (Fig. 4.6 (a)) and semi-log scale (Fig. 4.6 (b) I_d-V_{gs}) of the device in temperature range of 100 K to 400 K. Same drain bias (of 500 mV), that was earlier applied to the devices at room temperature measurements, was used for 12L device for the temperature dependent transfer characteristics measurements. A 50 K interval temperature starting from 100 K up to 300 K and 30 K and 40 K intervals respectively beyond room temperature were used for the transistor measurements. From Fig. 4.6 (a), it is evident that with lowering the temperature the drain current (and hence the conductivity) consistently increases. Several observations are evident: First, the ON current gradually decreases and the OFF current increases, leading to a decrease in the (ON/OFF) switching ratio. However, the device shows appreciable ON/OFF ratio irrespective of the temperature of operation, an I_{on}/I_{off} of between more than 10^5 to more than 10^8 is obtained. The increase of the drain current with temperature in the subthreshold regime is governed by the thermionic emission (TE) through reverse biased Mo-MoS_2 Schottky barrier, i.e., $I_{d,\,TE}\,(V_{gs}) \propto T^2 \exp(-q\Phi_B(V_{gs})/\kappa T)$. At low gate voltages (subthreshold regime), the device shows semiconducting behavior (current increases with temperature). At higher gate voltages, the current decreases with temperature. This metals insulator transition (MIT) is manifestation of modulation in charge carrier density and mobility in the semiconductor. Secondly, there is a threshold voltage shift seen at higher temperatures (above 300^0 C) and the V_{th} shifts to lower V_{gs} values. This is due to the creation of interface traps in the insulator, leading to trapping and de-trapping of carriers at the interface of MoS_2 and the gate oxide. Knowing the flat-band voltage (V_{FB}) from Fig. 4.6, the number of interface trap density (N_{it}) at any given time, bias and temperature can be extracted from $V_{it} = (V_{th}\text{-}V_{FB}) = qN_{it} / C_{ox}$. C_{ox} is the gate oxide capacitance per unit area (in our case, it is $3.4\text{x}10^{-4}$ F/m^2 for 100 nm SiO_2, used for the device fabrication). The temperature dependent FET characteristics shown in Fig. 4.6 and MIT discussed above can further be analyzed to extract the SBH of Mo-MoS_2 FET.

The Arrhenius plots (I_{ds} *vs. 1/T*) are extracted from Fig. 4.6 in both the regimes (below subthreshold and above subthreshold regime) for various gate voltages and temperatures, as shown in Fig. 4.7 (a). As is evident, there are two sets of linear fitting of the data; one at higher temperatures and the other at lower temperatures. As the temperature becomes high, the device conductivity (drain current, I_{ds}) increases and the carriers overcome the Schottky barrier. This

thermionic emission (TE) effect has been mentioned earlier. Therefore, the linear fitting segments at high temperature regime are the ideal plots to extract the TE current. The fact that the slope of these straight-line fitting at various gate voltages (below threshold voltage the signature becomes more prominent) is dependent on applied gate voltages indicates the gate voltage dependent of the SBH (V_{gs}). Additionally, from the lower temperature regime, the drain current is proportional to the carriers with enough energy to just jump the metal-semiconductor contact barrier but without the TE processes. The drain current equation used for SBH follows $I_d (V_{gs}) = AT^2 \exp(-q\Phi_B/\kappa T) (\exp (qV_{ds})/\kappa T) - 1)$. "$A$" is a characteristic constant and κ is the Boltzmann constant. Fig. 4.7 (b) shows the SBH (Φ_B in eV) vs. V_{gs} (V), demonstrating TE regime, flat band regime, and tunneling regime. The SBH of the molybdenum contact to 12L MoS_2 FET is characterized by the tangent to the TE data at the flat band condition of MoS_2 band structure and the value is 0.13 eV. This value is lower than the noble and high work function metals such as platinum, gold etc. and slightly higher than soft metals such as titanium and aluminum.[55], [130], [133]–[136] Several contact metals, with their corresponding Schottky barrier height values including the value obtained above, are plotted in Fig. 4.7 (c).

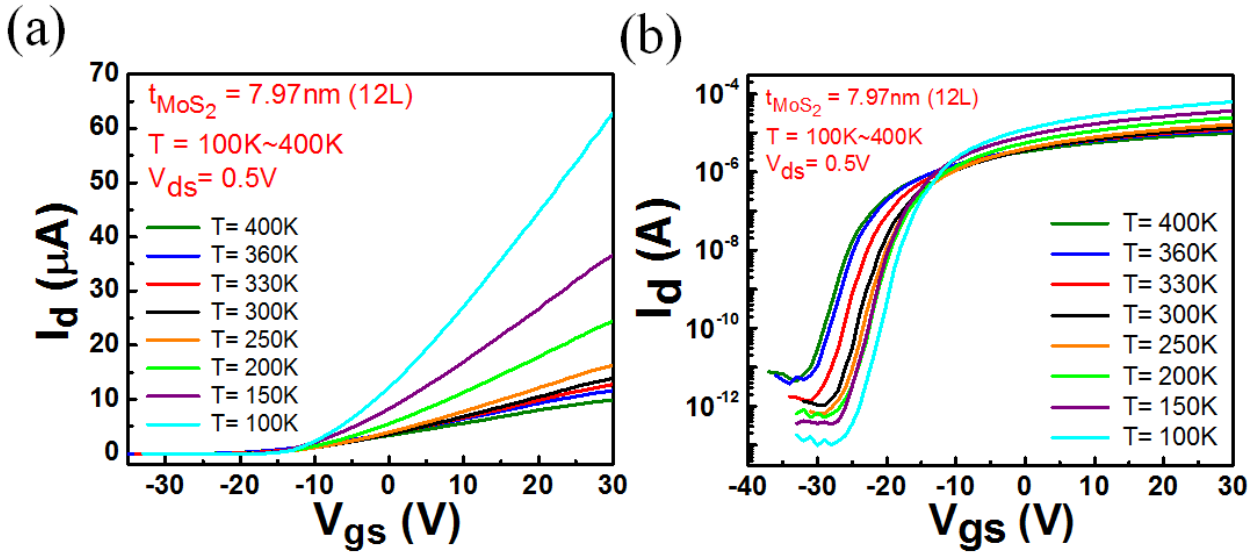


Fig. 4.6 The temperature dependent transfer characteristics of molybdenum S/D contacted MoS_2 FET with 12L channel thickness. 100K to 400K temperature range was used and the FET was drain biased with 500 mV (linear regime). Both linear scale (a) and log scale (b) plots are shown to illustrate the threshold voltage as well as the thermionic and field emission processes involved in the carrier injection from molybdenum to MoS_2.

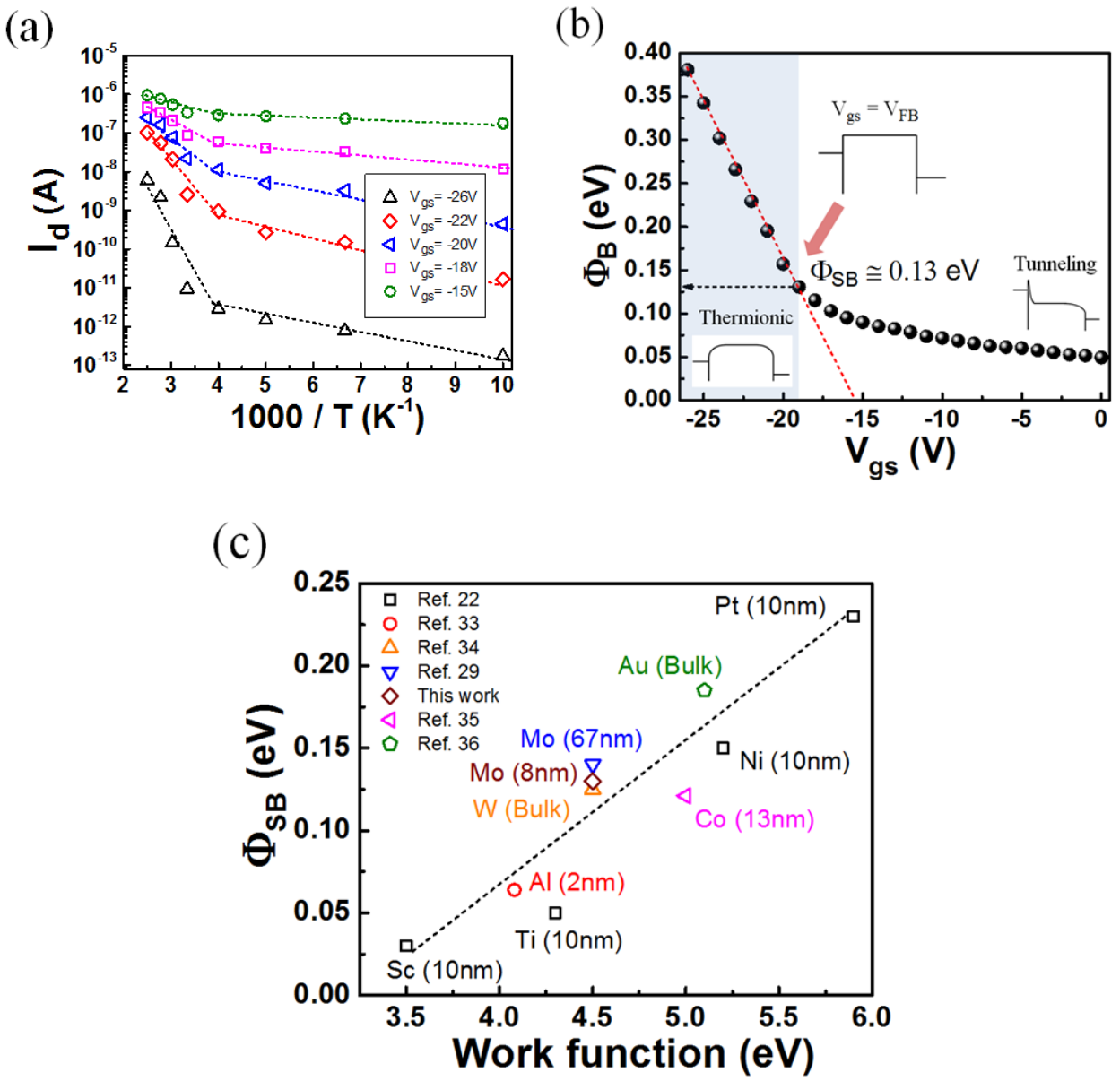


Fig. 4.7 (a) The gate voltage dependent Arrhenius plots at below subthreshold and above subthreshold voltage of 12L MoS_2 FET with S/D molybdenum contacts. (b) Gate voltage dependence of the SBH, showing carrier injection in the TE, flat band, and tunneling regime. Schottky barrier height of 0.13 eV is shown at flat band regime. (c) A metal work function (eV) vs. SBH (eV) plot made with S/D contact metals with high work functions to low work function metals. The value obtained in this work for molybdenum metal is shown with its relative position to the others.

It has been previously shown that in thin MoS_2 FETs (monolayer and few layers) the carrier mobility is limited by both charge impurity scattering and electron-phonon scattering.[131] Such

scattering events are key factors that are responsible for the transport physics in TMDC channel materials. Radisavljevic et al. showed a transition between regimes with increasing mobility with decreasing temperature (attributed to electron-phonon scattering, with $\mu \alpha T^{-1.4}$) and decreasing mobility with decreasing temperature (observed below ~ 200 K and attributed to charge-impurity scattering). In our case, Fig. 4.8 shows the temperature dependent mobility of the device between 400 K and 100 K temperature, with the mobility monotonically increasing from 25 cm^2/V s to 220 cm^2/V s with decreasing temperature. The mobility data exhibits electron-phonon scattering behavior over the entire temperature range, with no evidence of a cross-over to charge-impurity scattering. Linear fitting of the data yields an exponent $\mu \alpha T^{-1.55}$. With $\mu_{(Bulk)} \alpha T^{\gamma}$, with $\gamma \sim 2.6$, the obtained higher exponent value indicates the charge carriers are likely delocalized in multiple layers (instead of confining them in a specific layer in the 12L channel), leading to a correlated electron-phonon scattering. Future study is needed to understand its origin, particularly dependence on excited optical phonons of MoS_2, carrier concentration and coupling strength between the vdW layers, as well as the polar optical phonons from the oxide substrate. As we discussed earlier in Fig. 4.6 (b), the threshold voltage of the device remains largely unchanged from 100K to 300K, however, its shift at higher temperatures due to trapping and de-trapping of carriers makes the temperature dependent mobility more complicated.

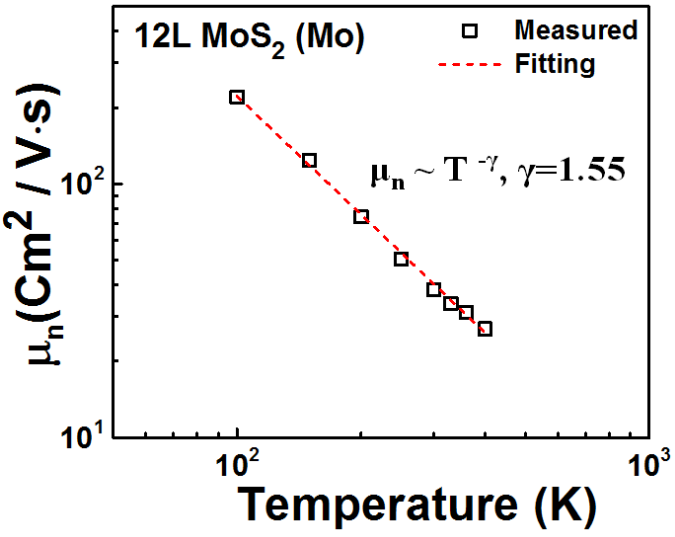


Fig. 4.8 The mobility vs. temperature plot of molybdenum S/D contacted MoS_2 FET with 12L channel in the operating temperature window between 100K and 400K. The power exponent of mobility with temperature with a $\gamma \sim 1.55$ in whole temperature range indicates the mobility is solely limited by the electron-phonon scattering and with an interlayer coupling among the atomic layers.

The contact resistance and access resistance discussed earlier as the limiting factors in the field effect mobility, the SBH, and the scattering parameters extracted from the mobility vs. temperature data are all very important physical parameters in FETs comprising of 2D TMDC channel materials, particularly the semiconducting phases such as 2H-MoS_2. One such important parameter, which is often not reported well yet constitutes a figure of merit for benchmarking new devices, is the low frequency noise (LFN) or 1/*f* noise. We have previously shown with a comprehensive extraction model the analysis of 1/*f* noise by correlating the transport in 2D-FETs (the device current, contact resistances, access resistances, etc.) with the noise spectrum [105], [137] In such an extraction method, knowing the nature of the access resistance (contact resistance plus the interlayer coupling resistances) and contact noise enables one to elucidate the channel conductance and the channel noise. Although we have demonstrated it for $MoSe_2$ FETs with nickel contacts and various channel thickness, the LFN study for wide thickness range of MoS_2 with molybdenum metal S/D electrodes has not been demonstrated. The noise measurement data for all the five Mo-MoS_2 FET devices studied in this work at the transistor ON state (overdrive voltage of 7 V) and at V_{ds} of 50mV is shown in Fig. 4.9 (a). As shown, the devices with all the thicknesses show 1/*f* noise characteristics. A closer observation indicates presence of a lower noise data for FETs with 10L and 12L MoS_2 with a lowest one for 12L. With earlier analysis on optimal transport characteristics, we have further analyzed the noise characteristics of 12L FET. Fig. 4.9 (b) shows the device noise (normalized current noise density at 100 Hz) of 12L Mo-MoS_2 FET vs. the overdrive voltage. As shown previously, [105], [137] the device shows three distinct noise regime characterized by different overdrive voltage dependence of the current noise spectral density; a $V_{gs}^{-1.1}$ indicates a channel regime (regime I), V_{gs}^{0} indicates a contact regime and V_{gs}^{-3} indicates a transition from channel to contact dominated noise regime as the device is gated. Relating this to Fig. 4.9 (c), regime I shows the channel dominating of both the noise and resistance (or conductance). In that case, a Hooge model on channel noise, involving a mobility-fluctuation events given by $f \cdot S_I / I_d^2 \sim (\alpha_{H,\,ch} / N_{ch}) \sim V_{gs}^{-1}$, could be used to extract the Hooge parameter. Similar protocol and fitting were made for all five devices to extract the channel Hooge parameters and is plotted in Fig. 4.9 (d). The FET with 12L shows the lowest Hooge parameter, indicating the low noise characteristics of the device compared to devices of lower and higher channel thicknesses. An obtained Hooge constant of

$\alpha_{H,\,ch}$ ~ 5.5x10^{-3} is greatly favored for the requirement of low noise nanoelectronic devices used for applications that involves precision electronic measurements and sensing.

4.2.4 Conclusion

In conclusion, we have fabricated and studied MoS_2 FETs of various channel thickness with molybdenum source and drain contact electrodes. The FETs show increase in mobility and conductivity as the channel thickness increases, followed by maxima at 12 layers, and then decreases significantly. The contact resistance follows an opposite trend to above signature with minimal contact resistance for the device with 12L. Finally, $1/f$ noise studied on the Mo-MoS_2 FETs shows a decreasing noise as the layer number increases until 12L optimal thickness is reached, after which the noise increases. The conductivity, mobility, contact resistance, in corroboration with lowest noise in 12L Mo-MoS_2 FET establishes the signature of 2D-vdW semiconductors with their impacts on device characteristics. Moreover, the conductivity and the noise in optimum layer thickness is limited by electron-phonon scattering as opposed by previously demonstrated competing mechanisms on electron-phonon scattering and impurity scattering in thin layer FETs.

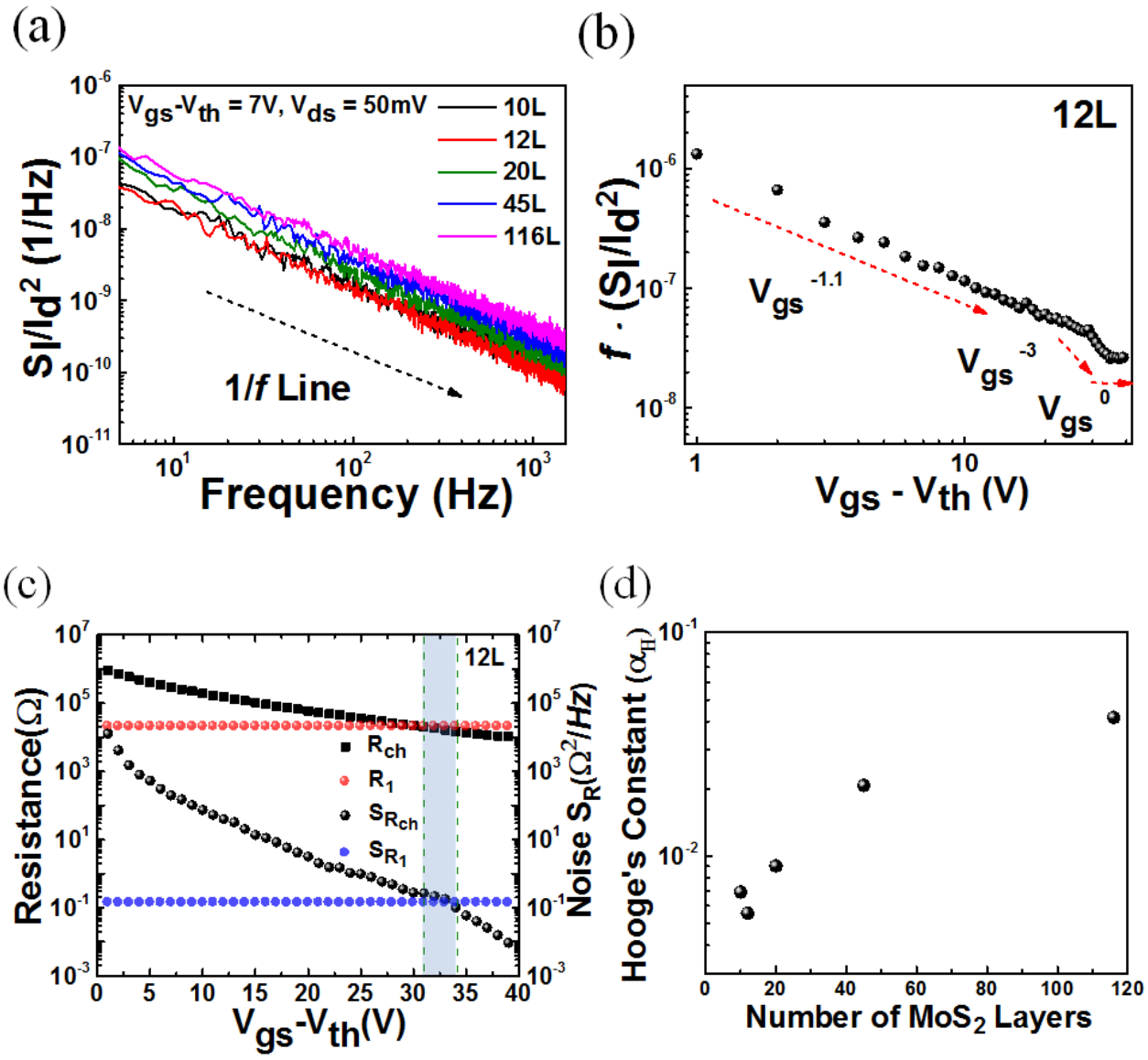


Fig. 4.9 (a) Low frequency device noise spectra of the molybdenum S/D contacted MoS_2 FETs with various channel thicknesses, showing a 1/*f* characteristic. All the devices are operated in the ON state with a source to drain bias of 50 mV. (b) Normalized current noise vs. overdrive voltage of the FET with 12L channel thickness at 100 Hz frequency, showing three distinct operating regimes characterized by the gate voltage dependent shown. (c) Contact and channel components of the noise and resistance for the 12L FET showing a narrow transition regime from channel dominated to contact dominated transport. (d) Extracted channel Hooge parameter vs. number of atomic layers in the molybdenum contacted MoS_2 FETs, showing the lowest 1/*f* noise in 12L FET.

5. EXPERIMENTAL AND MODELING STUDY OF 1/*F* NOISE MODEL IN MULTILAYER MOS_2 AND $MOSE_2$ FIELD-EFFECT TRANSISTORS

5.1 Introduction

Recently, the application of MX_2 (M ≡ Mo, W; X ≡ S, Se, Te) transition metal dichalcogenides (TMDCs) as electronic materials has offered an exciting roadway to practical nanoscale electronics such as chemical sensing, optoelectronics and nanophotonics.[11], [14], [15], [18], [42], [43] Among the TMDCs, for several electronic applications, the devices fabricated from MoS_2 and $MoSe_2$ are promising and considered good candidates. Their properties include high carrier mobility (up to 800 $cm^2/V{\cdot}s$), very thin atomic thickness (6.5A˚), and a relatively large bandgap (1.3–1.8 eV), leading to good switching behavior and mechanical flexibility.[11], [26], [55], [60], [138]–[140] These properties combined with high current *on/off* ratio ($> 10^6$) and steep subthreshold swing (~ 60 mV/decade) for MoS_2 and $MoSe_2$ field-effect transistors are attractive for the integrated circuit systems.[16], [53]–[56] However, fundamental low-frequency (1/*f*) noise could be an obstacle to reaching the ultimate performance of MoS_2 and $MoSe_2$ field-effect transistors for digital or analog electronic applications. On the other hand, low-frequency (1/*f*) noise, a basic technique in characterizing devices,[34], [65], [66] has also become important in characterizing nanoscale materials and devices, and offers a method to evaluate electronic states at the channel and oxide interface. The noise properties are dependent on the connection of carriers at the interface as well as the contact and access-region. Hence, it is important to measure the 1/*f* noise of devices in low-dimensional materials such as nanowires, carbon nanotube (CNT), graphene, and TMDCs.[67]–[72], [84], [105] Two-dimensional (2D) materials, especially graphene and TMDCs, are expected to exhibit unique noise behavior due to the existence of interlayer coupling resistances (R_{int}) between individual channel layers.

Prior studies,[55], [61], [141] Das et al. have already discussed how the contact resistance arising from the low and high Schottky barriers at the metal to MoS_2 interface for low (Φ_{Sc} = 3.5 eV, and Φ_{Ti} = 4.3 eV) and high (Φ_{Ni} = 5.0 eV, and Φ_{Pt} = 5.9 eV) workfunction metals, Thomas-Fermi charge screening, and the interlayer coupling resistances (R_{int}) between individual layers can significantly impact the extracted field-effect mobility values. A number of studies have measured 1/f noise in FETs using MoS_2 [72], [73], [79], [82], [104], $MoSe_2$ [84], and WSe_2 [78]

as channel materials. Various studies have observed behavior consistent with number-fluctuation mechanism, while others are better described by a mobility-fluctuation mechanism; consideration of threshold voltage and series resistance effects is essential in order to be able to isolate channel properties in order to accurately evaluate the noise mechanism.[105] While various studies have considered single layer, bilayer and multilayer FETs, comprehensive studies of noise properties versus channel thickness and material are not available.

In this work, with the motivation of improving the performance and reliability of sharply scaled patterned TMDC transistors, we present a systematic study on the current model and Hooge's constants in multilayer MoS_2 and $MoSe_2$ field-effect transistors. In particular, we focus on a theoretical framework to explain our experimental findings of the general trend in the hooge parameter vs. layer thickness (initially decreasing, and then saturating or gradually increasing) and its dependence on charge screening and interlayer coupling for various contact metals (Sc, Mo, Ni and Cr/Au) and channel materials (MoS_2 and $MoSe_2$). In particular, our $1/f$ noise results allow us to unravel new fundamental information about carrier transport and $1/f$ noise in two-dimensional layered systems that will likely play a very important role in the fulfillment of future electronics applications that have not been evaluated in the past. Moreover, our analysis is generic, and can be extended to other TMDCs materials and the reduction of noise level (the decrease of Hooge's constant (α_H)) is promising for designing TMDCs device applications.

5.2 Experimental Details

Bulk MoS_2 and $MoSe_2$ crystal flakes (SPI supplies and 2D Semiconductor, Inc.) were mechanically exfoliated directly onto a heavily doped Si/SiO_2, which were P^{++} silicon / 90 nm or 100 nm oxide thicknesses. The different thicknesses of the flakes were confirmed using atomic force microscopy (Veeco Dimension 3100 scanning probe microscope) with the tapping mode. The layer thicknesses vary from 3 layers to 142 layers. The devices with various metal contacts such as Sc, Mo, Ni, and Cr/Au were fabricated using e-beam lithography patterning (Raith e_LiNE) and development, metallization, and a lift-off process with acetone. A semiconductor parameter analyzer (Keithley 4200) and a probe station were used to measure the output and transfer characteristics of MoS_2 and $MoSe_2$ FETs. The 1/f noise measurements were performed using an Agilent dynamic signal analyzer (35670A) and a low noise current pre-amplifier (SR570). A low pass filter was connected to a voltage source (Keithley 263 Calibrator/Source) to

maximally remove the noise present in the input DC voltage. All the ground terminals are connected to the equipment–ground system. Fig. 5.1 (a) shows a 3-D schematic of a back-gated MoS_2 ($MoSe_2$) FET. In this study, MoS_2 and $MoSe_2$ were chosen as a channel material, and various metals like Sc, Mo, Ni, and Cr/Au were used as source/drain electrodes (S/D). In Fig. 5.1 (b), atomic force microscopy (AFM) measurements confirmed that the thickness of a MoS_2 flake in the representative field-effect transistor with Sc contacts, which is around 9.78 nm, corresponds to approximately 15 layers (single-layer MoS_2 ~ 0.65 nm).[11]

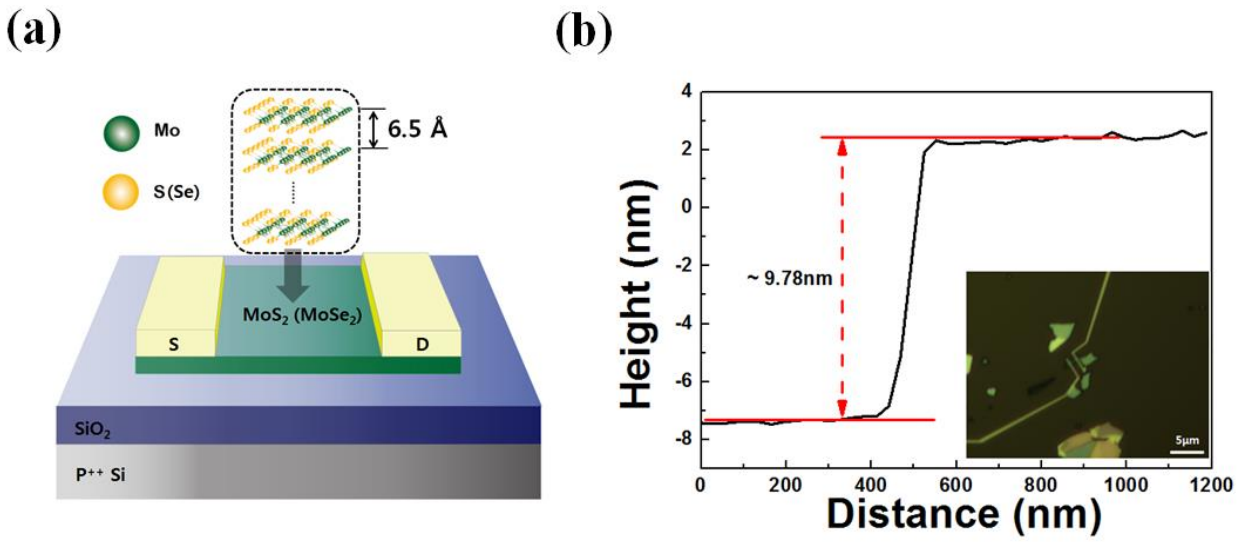


Fig. 5.1 (a) 3-D schematic of back-gated MoS_2 ($MoSe_2$) field-effect transistors with different contacts of Sc, Mo, Ni and Cr/Au. (b) Optical image and AFM step profile of a representative 15L-MoS_2 FET with Sc contacts.

5.3 Results and Discussion

Fig. 5.2 (a) shows the transfer characteristics of 10nm-thick multilayer MoS_2 FETs fabricated with Sc, Mo, Ni, and Cr/Au at a drain-to-source voltage (V_{DS}) of 0.5 V. In a previous study,[55] Sc contacts appeared very interesting because of a very small Schottky barrier height of 30 meV and thus gives rise to the highest carrier injection and the smallest contact resistance. In this same study, other workfunction metals like Mo, Ni, and Cr/Au were used for comparison. The inset of Fig. 5.2 (a) shows the alignment of the metal workfunction to the MoS_2 bands for the low and high workfunction metals in which we study here. Fig. 5.2 (b) shows the extracted field-effect mobility (μ_{ext}) as a function of number of MoS_2 layers for various metal contacts. As

discussed previously,[84], [105] for each device, the gate-voltage-dependent transconductance (g_m) was obtained by differentiating the transfer characteristic in Fig. 5.2 (a), and the maximum value of g_m ($g_{m,max}$) was used to calculated the extrinsic field-effect mobility (μ_{ext}) using:

$$g_{m,max} = \mu_{\text{ext}} C_{ox} \left(\frac{W}{L}\right) V_{DS,Total}, \tag{5.1}$$

where C_{ox} is the gate oxide capacitance per unit area (F/cm^2), W and L are the width and length of the channel, and $V_{DS,\ Total}$ is the total drain-source voltage. Throughout this paper, extrinsic values refer to those corresponding to terminal characteristics, i.e. including both the intrinsic channel properties and the effects of series/access resistances. The extracted values of μ_{ext} for MoS_2 devices with various contact metals are shown in Fig. 5.2 (b) as a function of layer thickness. For all contact metals, a maximum value of μ_{ext} is observed for a thickness of ~ 15 layers, with values of 62.5, 38.2, 31.1, and 30.2 cm^2 / (V s) for Sc, Mo, Ni, and Cr/Au, respectively. The results of mobilities explicitly indicate the importance of proper contact electrodes to reach the intrinsic properties of nano devices, and for typical FET structures utilizing Schottky-barrier (SB) contacts, the dependence of extrinsic channel mobility on the number of channel layers and contact workfunction can be well explained by the lack of sufficient screening of the substrate interface states, i.e., interfacial scattering (thin layers) and the finite interlayer coupling resistances (R_{int}) (thick layers).[61], [105]

In prior publications, approaches for separating channel resistance (gate voltage dependent) from series/access resistance have been described.[105] Given the quality of the 2D-TMDCs materials, in general, total contact/access resistance (R_1) will contain contributions from the Schottky barrier contact resistance (R_S) as well as the interlayer coupling resistance (R_{int}) between the total number of layers. In other words, this yields a layer-thickness dependent value for R_1. By considering the thickness-dependence of R_1 in the large-thickness regime, the resistance components can be described by

$$R_1 = R_S + nR_{int}, \tag{5.2}$$

where n is the total number of MoS_2 ($MoSe_2$) layers, and R_{int} is the interlayer coupling resistance associated with transport between the individual MoS_2 ($MoSe_2$) layers.[105] For the samples considered in this study, a value of R_{int} = 1.8 kΩ μm was obtained from the analysis of prior

study.[142] For the Mo-contacted samples, a R_S value of 16 kΩ μm was determined using previously reported methods[130], [143]; for all other samples, R_S values were employed to be 1.1, 21, 25 kΩ μm for Sc, Ni, Cr/Au from the literatures.[61], [144] The use of approximate analysis which considers the total interlayer resistance to be in series with the intrinsic channel, rather than the distributed network illustrated in Fig. 5.3 (a), was chosen to be consistent with prior approaches for analyzing experimental data.

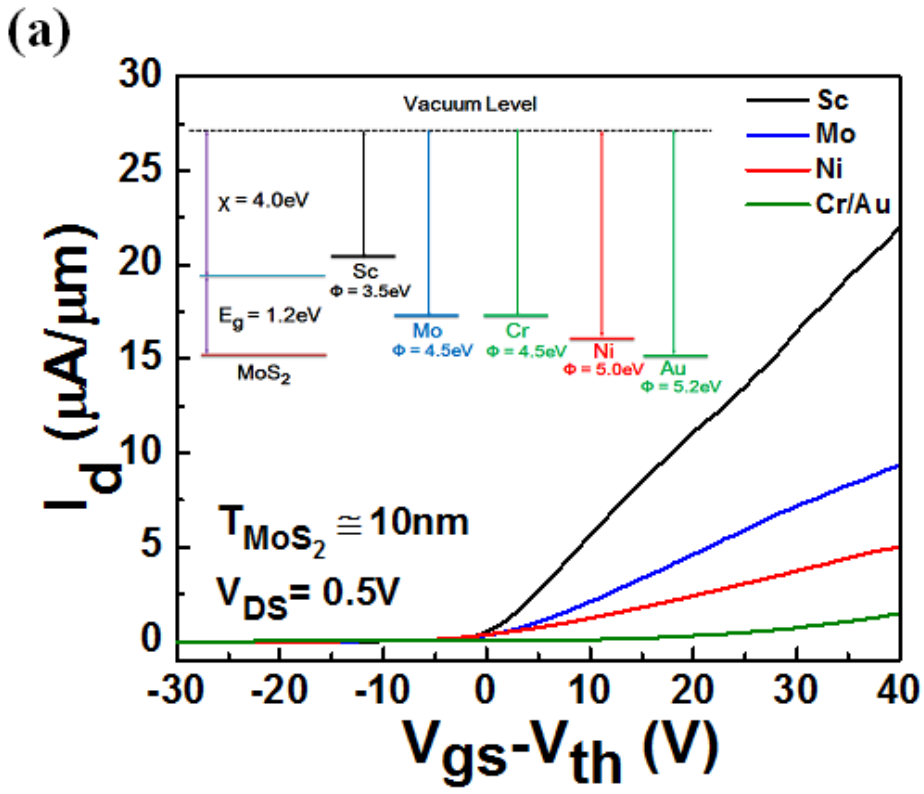


Fig. 5.2 (a) Transfer characteristic of around 10nm thick MoS_2 field-effect transistors with Sc, Mo, Ni, and Cr/Au metal contacts for V_{ds} = 0.2V. The inset shows band diagram of MoS_2 with Sc, Mo, Ni, and Cr/Au. (b) The extracted field-effect mobility (μ_{ext}) as a function of number of MoS_2 layers for Sc, Mo, Ni, and Cr/Au metal contacts. The direction of arrow indicates lower workfunction.

Fig. 5.2 continued

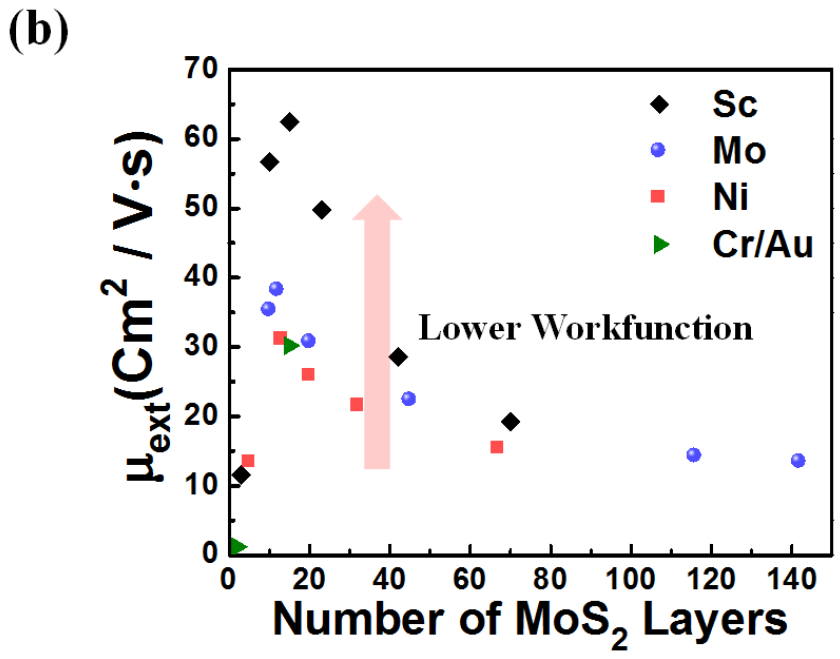


Fig. 5.4 shows the measured (symbols) Hooge's constants versus the number of layers for back-gated MoS_2 field-effect transistors with different contact metals. Results from modeling (discussed later) are also shown (dashed lines). Similar to our previous studies,[84], [105], [137] our experimental results of the total current-noise-power-spectral density ($S_{I_{D,Total}}$) in back-gate devices can be described by Hooge's empirical model,[34]

$$\frac{S_{I_{D,Total}}}{{I_{D,Total}}^2} = \frac{\alpha_{H,Total}}{f N_{Total}}. \tag{5.3}$$

Here, $\alpha_{H,Total}$ is the total Hooge parameter, f is the frequency, N_{Total} is the total number of carriers, and $I_{D,Total}$ is the total drain current. As with mobility, the Hooge parameter improves (decreases) with increasing layer thickness for thicknesses up to ~ 15 layers, then degrades (increases). The optimal Hooge parameter improves with decreasing contact work function.

We employed a previously developed model considering layer-thickness dependence and contributions from Schottky-barrier and interlayer-coupling resistances to μ_{ext} and have developed a physically-based model for low-frequency noise incorporating these effects. Collectively, these models can be used to explain the mobility and Hooge parameter behavior for

varying channel thickness and various metal contacts. Fig. 5.3 (a) shows a resistor network model of MoS_2 ($MoSe_2$) FETs. Here, R_{ch1}, R_{ch2}, R_{ch3} … R_{chi} denote the intralayer resistance of each MoS_2 ($MoSe_2$) layer, respectively. The model consists of a ladder network with individual layers connected by R_{int}. Here, α_{Hi}, μ_i, V_{DS_i}, and N_i represent parameters associated with the i^{th} layer, namely Hooge's constant, the mobility, the drain-source voltage across the channel, and the number of carriers, respectively.

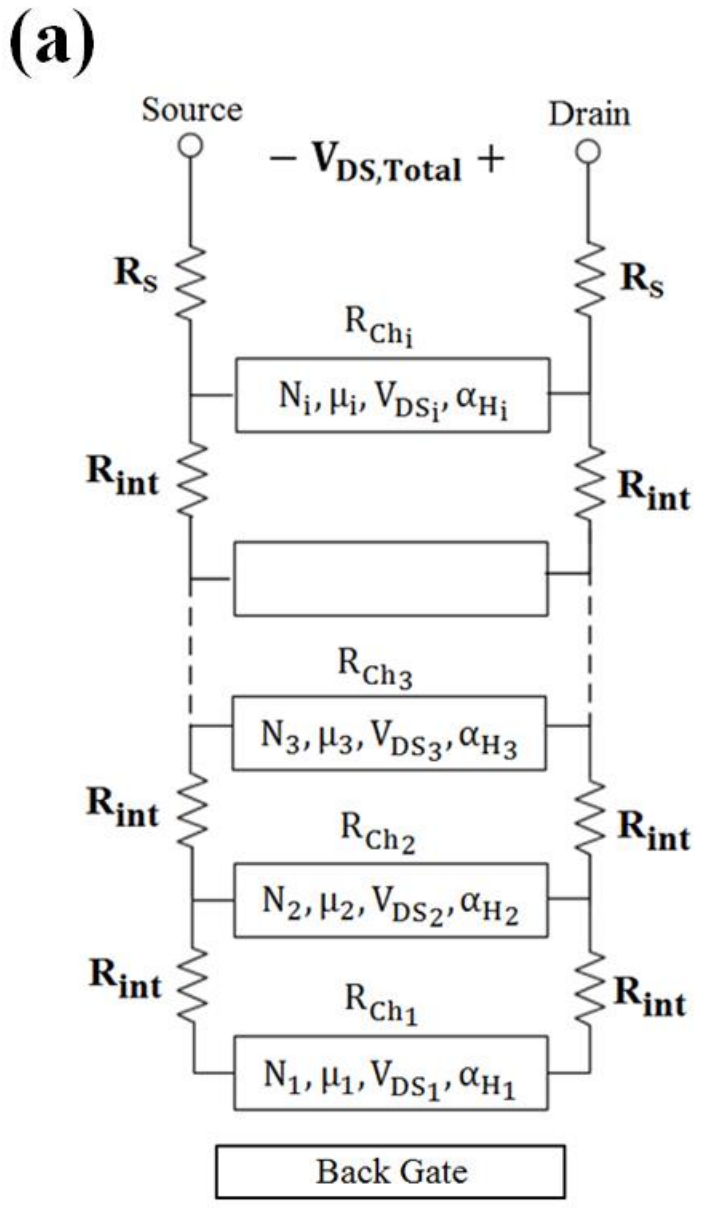


Fig. 5.3 (a) A resistor network model and the general topology for our noise model in multi-layer MoS_2 and $MoSe_2$ back-gated transistors.

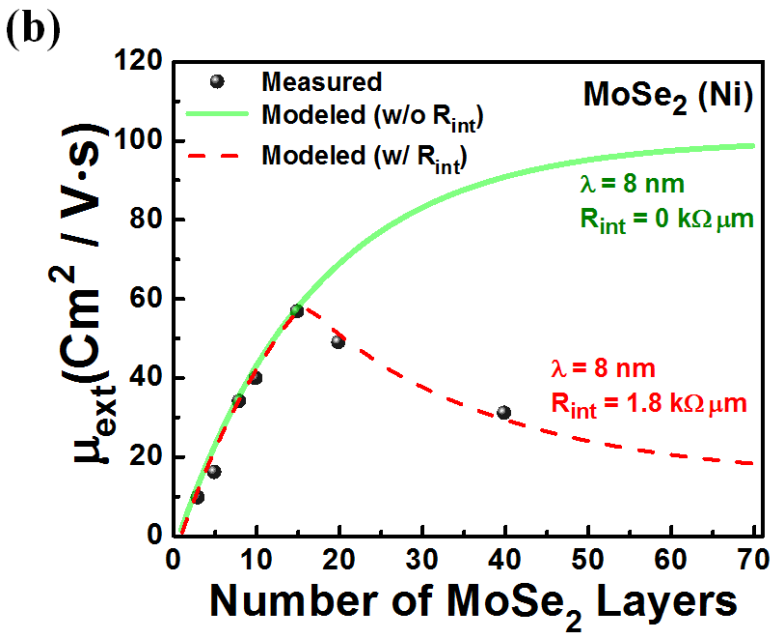


Fig. 5.3 (b) Field-effect mobility (μ_{ext}) vs. the number of $MoSe_2$ layers. Black circle shows the measured result, and solid (green) and dashed lines (red) indicate the modeled results. The simulation assumes λ = 8 nm, and R_{int} = 0 (1.8) kΩ μm for the green-solid line (the red-dashed line).

Fig. 5.3 (b) shows the field-effect mobility (μ_{ext}) versus the number of $MoSe_2$ layers. The black circles represent the measured result, and solid (green) and dashed (red) lines indicate the modeled results (discussed later). The mobility model follows the approach of Das et al.,[55], [61], [96]. In order to be consistent with subsequent noise analysis, the typical I-V relationship used to derive Eq. (5.1) (in which carrier density is expressed in terms of capacitance per unit area and overdrive voltage) can be re-written in terms of the total number of carriers (N_{Total}). The total modeled drain current ($I_{D,MOD}$) can be written as:

$$I_{D,MOD} = \mu_{MOD} N_{Total} V_{DS,MOD} \left(\frac{q}{L^2}\right) = \sum_{i=1}^{\#\ of\ Layers} I_{D_i}, \tag{5.4}$$

where μ_{MOD} is the total modeled mobility, $V_{DS,MOD}$ is the total modeled drain-source voltage, and q is the electron charge (1.6 x 10^{-19} C). The model involves calculating the individual contributions from the various channel layers, then summing these contributions in order to obtain $I_{D,MOD}$. The modeled drain current of the i^{th} layer (I_{D_i}) in the linear region is given by

$$I_{D_i} = \mu_i N_i V_{DS_i} (\frac{q}{L^2}). \tag{5.5}$$

The intralayer resistance of the i[th] layer is given by

$$R_{ch_i} = \frac{V_{DS_i}}{I_{D_i}} = \frac{L^2}{qN_i\mu_i}. \tag{5.6}$$

Initially, consider the case in which R_{int} =0. The total modeled intralayer resistance ($R_{ch,MOD}$) can be expressed by

$$R_{ch,MOD} = \frac{V_{DS,MOD}}{I_{D,MOD}} = \frac{L^2}{qN_{Total}\mu_{MOD}} = \sum_{i=1}^{\#\ of\ Layers} R_{ch_i}. \tag{5.7}$$

Expressions for N_i and μ_i are required in order to calculate I_{D_i} and R_{ch_i}. For a back-gated device, charge screening results in a decreasing number of charges for the top MoS_2 ($MoSe_2$) layers. This is a direct consequence of Thomas-Fermi (T-F) charge screening described by Eq. (5.8) where d_i denotes the distance from the bottom MoS_2 ($MoSe_2$) layers to the i[th] layer, λ is the T-F charge screening length, d_{ML} is the distance between MoS_2 ($MoSe_2$) layers.[61], [141]

$$\frac{N_i}{N_{i-1}} \approx exp\ \left(-\frac{d_i - d_{i-1}}{\lambda}\right) = exp\ \left(-\frac{d_{ML}}{\lambda}\right) = Const.$$

$$\sum_{i=1}^{\#\ of\ Layers} N_i = N_{Total} = \frac{C_{ox}(V_{gs} - V_{th})LW}{q}. \tag{5.8}$$

The μ_i can also be modeled using the exponential decay function in Eq. (5.9).[55], [61], [96]

$$\mu_i = \mu_1 + (\mu_\infty - \mu_1)\left(1 - \exp\left(-\frac{(i-1)d_{ML}}{\lambda}\right)\right). \tag{5.9}$$

While one would expect the λ value for charge screening (Eq. (5.8)) to be different from that for mobility variation (Eq. (5.9)), we follow the approach of Das, et al,[61] and use a single value for

the two cases. Under the condition that R_{int} and R_S are negligible, V_{DS_i} = $V_{DS,\,Total}$ for all layers, and at the overdrive voltage corresponding to the maximum transconductance ($g_{m,max}$), μ_{ext} (Green line in Fig. 5.3 (b)) is the same as μ_{MOD}, which can be calculated from a weighted average of the μ_i values:

$$\mu_{ext} = \mu_{MOD} = \sum_{i=1}^{\#\ of\ Layers} \frac{\mu_i N_i}{N_{Total}}. \tag{5.10}$$

The parameters in Eq. (5.9) are obtained by fitting the experimental data shown in Fig. 5.3 (b) (using Eq. (5.10)) over the range of thicknesses less than the value corresponding to maximum mobility point (0-15 layers for the representative device, $MoSe_2$ FETs, shown in Fig. 5.3 (b). In this regime, the intrinsic channel resistance is relatively large and the effects of R_{int} and R_S are negligible, resulting in $\mu_{ext} \approx$ the intrinsic mobility (μ_{int}). Values obtained from the literature include d_{ML} = 0.65 nm, μ_1 = 1 $cm^2/(V\ s)$, and μ_∞ = 100 $cm^2/(V\ s)$ in multilayer (Ni-Contact) $MoSe_2$ systems.[11], [26], [132] A value of λ = 8 nm provides a reasonable fit to the data in Fig. 5.3 (b) (green line).

The model can be extended by including the effects of R_{int} and R_S , which results in a roll-off in μ_{ext} with increasing layer thickness (beyond maximum mobility point). Due to voltage drops across these resistances, V_{DS_i} varies from layer to layer, and must be considered in (Eq. (5.5)). The total modeled drain-source voltage across the intrinsic channel ($V'_{DS,MOD}$) is calculated by using Eq. (5.11)

$$V'_{DS,MOD} = \frac{V_{DS,MOD}\,(R_{MOD} - R_1)}{R_{MOD}} = \frac{V_{DS,MOD}\,R_{ch,MOD}}{R_{MOD}}, \tag{5.11}$$

where R_{MOD} is the total modeled extrinsic resistance ($= R_{ch,MOD} + R_1$). The $R_{ch,MOD}$ is the total modeled resistance of channel from the modeled data at the overdrive voltage in the maximum transconductance ($g_{m,max}$) and calculated by using Eq. (5.6) and (5.7), using parameters described in the experimental section. Mobility values including series/access resistances are extracted by multiplying the values with no R_{int} by $\frac{V'_{DS,MOD}}{V_{DS,MOD}}$, namely, $\mu_{MOD}(R_{int} \neq 0) = \mu_{MOD}(R_{int} = 0) \cdot \frac{V'_{DS,MOD}}{V_{DS,MOD}}$. The resulting relationship (red dashed line in Fig. 5.3(b)) follows a

comparable thickness-dependence to that of the experimental data. Following similar procedures, the values of μ_1 and μ_∞ in multilayer $MoSe_2$ and MoS_2 FETs with different contact metals have been extracted and are listed in Table. 5.1. Mobility plots in MoS_2 FETs with various contact metals similar to the one shown above (in Fig. 5.3 (b)) are observed with the same fitting parameters (λ = 8 nm and R_{int} = 1.8 kΩ μm).

Table 5.1 The electrical transport and noise parameters of MoS_2 and $MoSe_2$ field-effect transistors with various metal contacts for our noise model.

Material	**Contact Metal**	**μ_1 (Cm^2/Vs)**	**μ_∞ (Cm^2/Vs)**	**λ_H (nm)**	**α_{H1}**	**$\alpha_{H\infty}$**
MoS_2	Sc	1	100	5	0.07	0.002
MoS_2	Mo	0.7	70	5	0.118	0.003
MoS_2	Ni	0.6	60	5	0.182	0.005
MoS_2	Cr/Au	0.6	60	5	1.4	0.04
$MoSe_2$	Ni	1	100	2	3	0.002

(Model – Noise)

A semi-empirical noise model can be developed for calculating the overall Hooge's constants versus layer thickness. The noise model represents the channel noise in terms of Hooge parameter for the i[th] layer (α_{H_i}), and initially, we ignore the interlayer coupling resistance (R_{int}). The total modeled current-noise-power-spectral density ($S_{I_{D,MOD}}$) can be written

$$S_{I_{D,MOD}} = \sum_{i=1}^{\#\ of\ Layers} S_{I_{D_i}} = \frac{1}{f}\sum_{i=1}^{\#\ of\ Layers} \frac{\alpha_{H_i}}{N_i}\left(I_{D_i}\right)^2, \quad (5.12)$$

where $S_{I_{D_i}}$ is the i[th] layer modeled current-noise-power-spectral density.

Using Eq. (5.5) for the terms of I_{D_i} Eq. (5.12) can be re-written as

$$S_{I_{D,MOD}} = \frac{1}{f}\left(\frac{q}{L^2}\right)^2 \sum_{i=1}^{\#\ of\ Layers} \alpha_{H_i} N_i \left(\mu_i V_{DS_i}\right)^2. \quad (5.13)$$

Using the ratio of $\frac{N_i}{N_{i-1}} \approx exp(-\frac{d_{ML}}{\lambda})$ in Eq. (5.8), so Eq. (5.13) can be expressed as

$$S_{I_{D,MOD}} = \frac{N_1}{f}\left(\frac{q}{L^2}\right)^2 \sum_{i=1}^{\#\ of\ Layers} \alpha_{H_i} exp\left(-\frac{d_{ML}}{\lambda}\right)^{i-1} \left(\mu_i V_{DS_i}\right)^2, \qquad (5.14)$$

where N_1 is the number of carriers of the first layer. Then, for the calculation of α_{H_i} in Eq. (5.14), Hooge's constant of the individual layers can be modeled using the exponential decay function in Eq. (5.15).

$$\alpha_{H_i} = \alpha_{H_\infty} + \left(\alpha_{H_1} - \alpha_{H_\infty}\right) exp\left(-\frac{(i-1)d_{ML}}{\lambda_H}\right), \qquad (5.15)$$

where α_{H_1} is Hooge parameter of the first layer, α_{H_∞} is Hooge parameter of a layer in the bulk (i.e. far away from the dielectric interface), and λ_H is the Hooge screening length. Here, using Eq. (5.14) and (5.15) with the resistor network model in Fig. 5.3 (a), under $R_{int} = 0$, we are fitting to experimental points of Hooge's constants for the number of layers or optimum in multilayer MoS_2 systems, and α_{H_1}, α_{H_∞} and λ_H (= 5 nm) are fitting parameters. Finally, the total modeled Hooge' constants ($\alpha_{H,MOD}$) are calculated by using Eq. (5.16),

$$\alpha_{H,MOD} = \frac{f S_{I_{D,MOD}} N_{Total}}{I_{D_{MOD}}^2}. \qquad (5.16)$$

The value of $I_{D,MOD}$ is determined from Eq. (5.5) and the rightmost part of Eq. (5.4), and $S_{I_{D,MOD}}$ from Eq. (5.14) and (5.15).). Under the condition that $R_{int} = 0$, $V_{DS_i} = V_{DS,\,MOD}$ for all layers. For a given channel material and contact metal, α_{H_1}, α_{H_∞} and λ_H (= 5 nm) are obtained by fitting $\alpha_{H,MOD}$ to corresponding experimental points for Hooge's constant (e.g. as shown in Fig. 5.4.) for various number of layers up to the optimum thickness point.

This model was used to fit the measured data for the various contact metals and channel materials, with extracted values of α_{H_1}, α_{H_∞}, and λ_H shown in Table 1. Based on the curves obtained from this model for various channel/contact materials (Fig. 5.4 and $R_{int} = 0$ curve in

Fig. 5.5), the general layer-thickness dependence/ (initially decreasing, then saturating) fits the experimental trend well. However, this model does not account for the increase in Hooge parameter within increasing layer thickness observed for thicknesses beyond the optimum point.

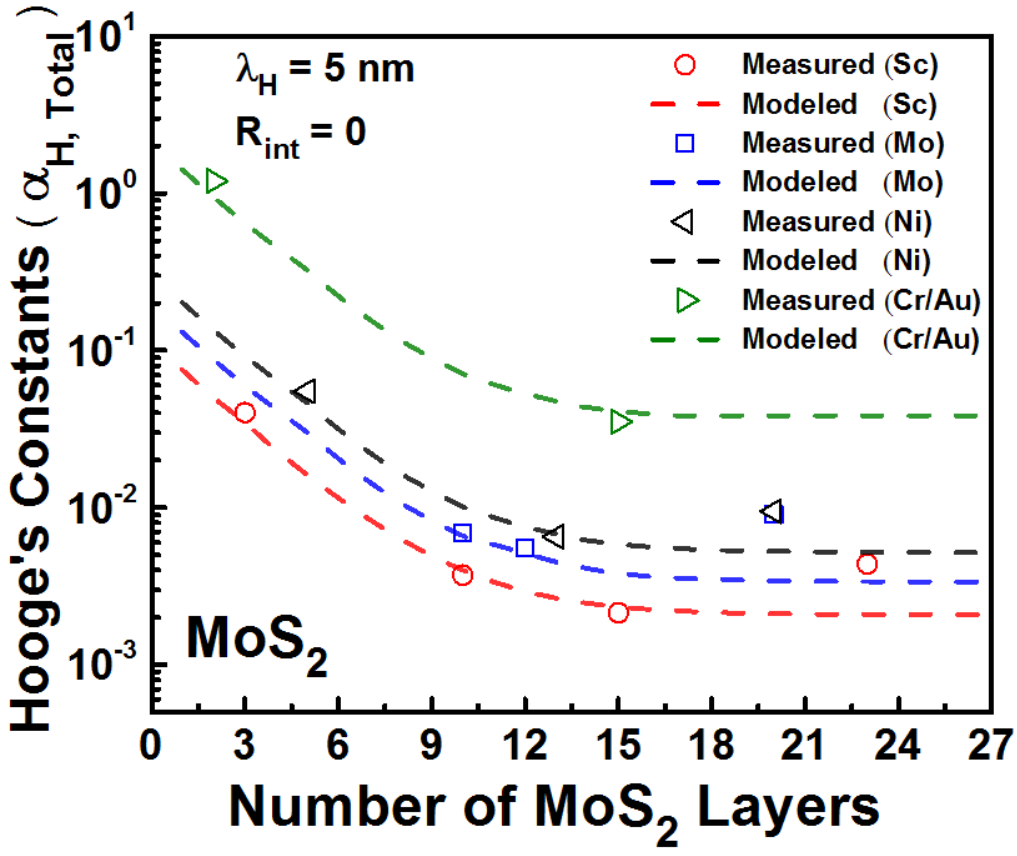


Fig. 5.4 Measured (symbols) and modeled (dashed lines) Hooge's constants for back-gated MoS_2 field-effect transistors with different contact metals. Model incorporates Hooge screening length for interactions of carriers with interface states; interlayer coupling effects not included (λ_H = 5 nm, and R_{int} = 0).

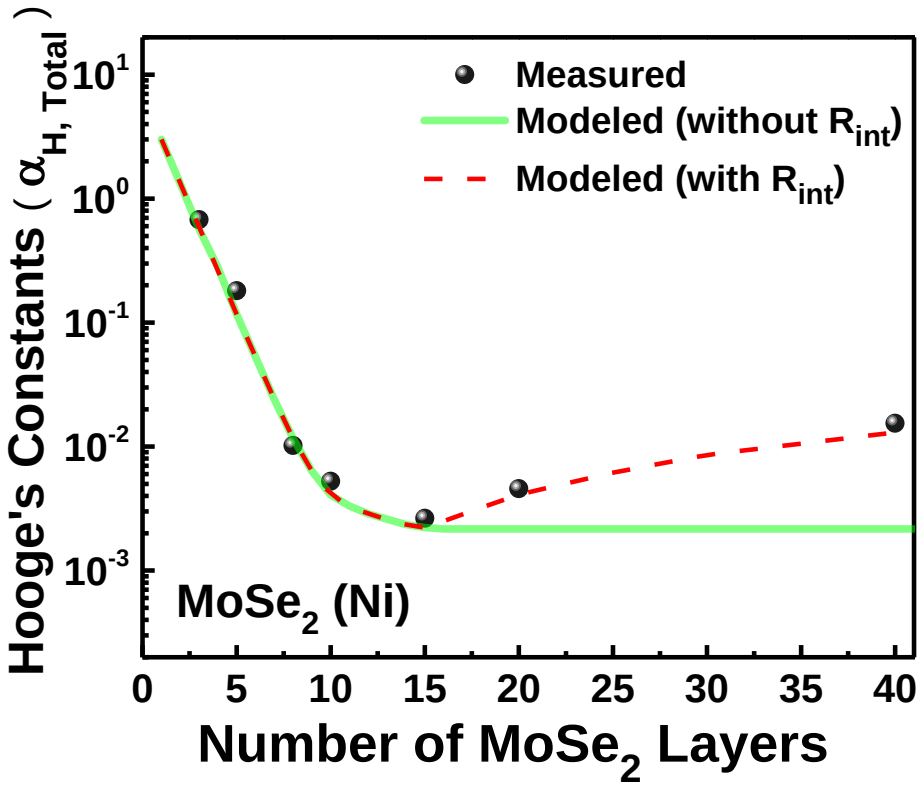


Fig. 5.5 Overall Hooge's constants vs. the number of $MoSe_2$ layers. Black circle shows the measured result, and solid (Green) and dashed (Red) lines indicate the modeled results. The simulation assumes λ_H = 2 nm, and R_{int} = 0 (1.8) kΩ μm for the green solid line (the red dashed line).

In order to develop a more comprehensive model, we add the effects of R_{int} in our noise model. While one would generally expect R_{int} to contribute additional noise as well as resistance, we have ignored the former in this analysis based on the observation that the associated noise sources would generally be interpreted as contributions from series/access resistances due to different voltage.[105] Starting from the ladder network model in Fig. 5.3(a), the analysis considers how the current divides between individual layers, and hence what current flows through each interlayer coupling resistance (R_{int}). For R_{int} = 0, we assumed that $V_{DS,MOD}$ = 0.05V for all layers. For $R_{int} \neq 0$, the values of V_{DS_i} in Eq. (5.14) are less than $V_{DS,MOD}$ due to voltage drops across R_{int} elements in the ladder network and are evaluated for representative cases using LTSPICE circuit simulator. This analysis used R_{int}, and R_{ch_i} from Eq. (5.6), evaluated at an

overdrive voltage comparable to the optimum point for noise, and yielded a set of V_{DS_i} values. The values obtained are reasonably approximated:

$$V_{DS_i} = (0.95)^{(n-i)} V_{DS,MOD}. \tag{5.17}$$

This yields values of $I_{D,MOD}$ (from Eq. (5.4), (5.5) and (5.17)) and $S_{I_{D,MOD}}$ (from Eq. (5.9), (5.14), (5.15) and (5.17)) for the case of $R_{int} \neq 0$. The associated value of $\alpha_{H,MOD}$ is obtained by inserting these values into Eq. (5.16). Fig. 5.5 shows the overall Hooge parameter as a function of layer thickness for $MoSe_2$ devices, including experimental data and values of $\alpha_{H,MOD}$ for the $R_{int} = 0$ and $R_{int} \neq 0$ are shown for a series of $MoSe_2$ devices in Fig. 5.5. Black circles indicate the measured data, and green solid line, and red dashed line represent the modeled results. The simulation results are implemented with λ_H = 2 nm and R_{int} = 0 kΩ μm or 1.8 kΩ μm. In devices with both types of channel materials, the model with $R_{int} \neq 0$ captures the effect of increasing Hooge parameter with increasing layer thickness. In comparison to the MoS_2 FETs (Fig. 5.4), the Hooge parameter in few-layers $MoSe_2$ FETs decreases more quickly with increasing layer thickness, which is associated with a smaller value of λ_H (= 2 nm).

The noise model with layer-dependent Hooge parameter is consistent with the physical descriptions in prior 1/f noise models for field-effect transistors.[34], [145] Following a prior analysis of number- and mobility- fluctuation contributions to noise in Si MOSFETs,[146] the mobility fluctuation contribution is expected to be proportional to the occupied trap density (N_T) and to the square of the product of the mobility and the scattering coefficient (α) associated with the interface trap scattering rate contribution to mobility. In the current work, the α_{H_i} can be interpreted in terms of an α which decreases with i, which is consistent with a local charge screening geometry in which a charged trap is partially screened by the lower layers. The improvement in both the noise and mobility with increasing i can be explained at least qualitatively by the variation of α with i.

5.4 Conclusion

In conclusion, recognizing the importance of 1/*f* noise impacting the high performance of back-gated MoS_2 and $MoSe_2$ FETs, we have implemented the first systematic experimental and modeled study for the charge (Q_i) and current flow on multilayer MoS_2 and $MoSe_2$ FETs to address the distribution of Hooge's constants in multilayer FETs. In order to demonstrate the compatibility of our noise model, we have developed a simulation-oriented noise model describing the interlayer coupling between MoS_2 ($MoSe_2$) layers and Thomas-Fermi charge screening. The results using our model are in good agreement with the experimental findings as well as prior studies in MoS_2 and $MoSe_2$ FETs.[61], [105] Comprehensive noise results in MoS_2 and $MoSe_2$ FETs are experimentally demonstrated and can be understood within this noise model using a resistor network in Fig. 5.3 (a) and considering adequate parameters such as λ, R_{int}, and λ_H between individual layers. Moreover, lower workfunction metal like scandium (Sc) has been utilized to form improved contacts with MoS_2 flakes, resulting in high carrier mobility and a lower Hooge's constant (2.14×10^{-3}), and in terms of other channel materials, the Hooge's constant (2.64×10^{-3}) of 15 layers $MoSe_2$ FET (Ni-contacts) is about 2.5 times lower than that (6.52×10^{-3}) of 13 layers MoS_2 FETs with same contacts (Ni).

6. CONCLUSIONS

From R. Feynman, "There*'s plenty of room at the bottom*", low-dimensional devices have opened up many challenges and possibilities in nanotechnology with their incredible physical features. Recently, many studies on low-dimensional devices have been carried out for the understanding of the electrical transport, such as *I-V* or *C-V* measurement. On the other hand, the measurement of low-frequency noise (LFN), which are commonly observed in most electronic devices, are known to be related to carrier movement, and their properties were used to provide some information about the traps of oxides. Although the noise origin is not clear in all cases, there are well-known models that describe noise based on existing MOSFETs. Here, low-dimensional structures such as 2D FETs using MoS_2 and $MoSe_2$ as channel materials have been explored for the electronic transports and low-frequency noise characteristics for the FET structures.

In Chapter 2, we summarize the basics and concepts of electronic noise to understand the low-frequency noise of 2D devices. The electronic noise can be classified into thermal, shot, generation-recombination (G-R), and 1/*f* noise. Among them, the G-R and 1/*f* noise are well observed in electronic devices. Generally, it is called as low frequency noise. There are two representative noise models which are useful to explain the low-frequency noise for FET structure: one is the mobility fluctuation model suggested by Hooge and the other is the carrier number fluctuation model involving the correlated mobility fluctuations by trapped charge carriers at the interface. Then, the details of setup and procedures for taking consistent noise measurements are described in the chapter.

In Chapter 3, we report 1/*f* noise properties in MoSe2 FETs with varying channel thicknesses (3 ~ 40 Layers). The results can be interpreted in terms of Hooge model associated with the channel noise, a transition regime, and the contact/access regime whose characteristics are determined by a voltage-independent conductance and noise source associated with the metal contact and interlayer resistance. Both the channel Hooge coefficient and the channel/access noise amplitude decrease with increasing channel thickness over the range of 3 to 15 atomic layers, with the former remaining approximately constant and the latter increasing over the range of 20 to 40 atomic layers. The analysis can be extended to devices based on other TMDCs.

In Chapter 4, we have fabricated and studied MoS_2 FETs of various channel thicknesses with molybdenum (Mo) source and drain contact electrodes. The devices increase in mobility and conductivity as channel thickness increases, then increase in maximum value in 12L and then decrease significantly. Finally, 1/*f* noise studied in the Mo-MoS_2 FETs shows that the noise decreases as the number of layers increases until it reaches the optimal layer of 12L. In addition, the conductivity and the noise at the optimum layer of 12L are limited by electron-phonon scattering based on the *I*-*V* characteristics with respect to the different temperatures. Next, we study the voltage-dependent 1/*f* noise and resistance correlation in MoS_2 FETs with ~ 142 atomic layer-thickness channel and three different lengths. The gate-voltage dependence of the noise can be separated into a channel contribution, with comparable Hooge parameter for the three devices, and a contact/access region contribution. Separation of these contributions allows evaluation of the channel noise mechanism, and can be used to explain the length-dependence of the transition region between contact- and channel-dominated regimes.

In Chapter 5, using source and drain metallurgical contacts with metals of high and low work function values, we have implemented the first systematic experimental study for the number of carriers (*N*) and current flow on multilayer MoS_2 and $MoSe_2$ FETs to address the distribution of Hooge's constants in low-frequency noise characteristics. We have developed a noise model describing the interlayer coupling between various layers in MoS_2 ($MoSe_2$) and Thomas-Fermi charge screening at the interface. The results using our model are in good agreement with the experimental findings as well as prior studies in MoS_2 and $MoSe_2$ FETs. Comprehensive noise results in MoS_2 and $MoSe_2$ FETs are experimentally demonstrated and can be understood within using a resistor network with parameters such as λ, R_{int}, and λ_H between individual layers. Moreover, a lower workfunction metal like scandium (Sc) has been utilized to form improved contacts with MoS_2 flakes, resulting in higher carrier mobility and a lower Hooge's constant (2.14×10^{-3}). In terms of other channel materials, Hooge's constant (2.64×10^{-3}) of a 15 layer $MoSe_2$ FET (Ni-contacts) is about 2.5 times lower than that (6.52×10^{-3}) of a 13 layer MoS_2 FETs with same contacts. Our noise analysis is fully comprehensive and, hence, could be applied to any two-dimensional (2D) layered systems.

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PUBLICATIONS

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