A LOW POWER FINFET CHARGE PUMP FOR ENERGY HARVESTING APPLICATIONS

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ABSTRACT

Whittaker, Kyle. M.S.E.C.E., Purdue University, May 2020. A Low Power FinFET Charge Pump for Energy Harvesting Applications. Major Professor: Maher E. Rizkalla.

With the growing popularity and use of devices under the great umbrella that is the Internet of Things (IoT), the need for devices that are smaller, faster, cheaper and require less power is at an all time high with no intentions of slowing down. This is why many current research efforts are very focused on energy harvesting. Energy harvesting is the process of storing energy from external and ambient sources and delivering a small amount of power to low power IoT devices such as wireless sensors or wearable electronics. A charge pumps is a circuit used to convert a power supply to a higher or lower voltage depending on the specific application. Charge pumps are generally seen in memory design as a verity of power supplies are required for the newer memory technologies. Charge pumps can be also be designed for low voltage operation and can convert a smaller energy harvesting voltage level output to one that may be needed for the IoT device to operate. In this work, an integrated FinFET (Field Effect Transistor) charge pump for low power energy harvesting applications is proposed.

The design and analysis of this system was conducted using Cadence Virtuoso Schematic L-Editing, Analog Design Environment and Spectre Circuit Simulator tools using the 7nm FinFETs from the ASAP7 7nm PDK. The research conducted here takes advantage of some inherent characteristics that are present in FinFET technologies, including low body effects, and faster switching speeds, lower threshold voltage and lower power consumption. The lower threshold voltage of the FinFET is key to get great performance at lower supply voltages.

The charge pump in this work is designed to pump a $150mV$ power supply, generated from an energy harvester, to a regulated $650mV$, while supplying $1\mu A$ of load current, with a $20mV$ voltage ripple in steady state (SS) operation. At these conditions, the systems power consumption is $4.85\mu W$ and is 31.76% efficient. Under no loading conditions, the charge pump reaches SS operation in $50\mu s$, giving it the fastest rise time of the compared state of the art efforts mentioned in this work. The minimum power supply voltage for the system to function is $93mV$ where it gives a regulated output voltage of $425mV$.

FinFET technology continues to be a very popular design choice and even though it has been in production since Intel's Ivy-Bridge processor in 2012, it seems that very few efforts have been made to use the advantages of FinFETs for charge pump design. This work shows though simulation that FinFET charge pumps can match the performance of charge pumps implemented in other technologies and should be considered for low power designs such as energy harvesting.

1. INTRODUCTION

1.1 Motivation

The IoT paradigm is expected to have a pervasive impact in the next years. The ubiquitous character of IoT nodes implies that they must be untethered and energy autonomous [1]. Every energy harvesting system has a power management circuit to convert the scavenged energy to a more usable power supply. Typically, designers use switched inductor or switched capacitor (SC) techniques to achieve this goal. "The switched-capacitor (SC) voltage multiplier is becoming one of the most critical Integrated Circuit (IC) blocks for energy harvesting in wireless sensor nodes to generate a voltage high enough for microwatt sensing and computing ICs in a nanometer complementary metal–oxide–semiconductor (CMOS) from environmental energy sources such as mechanical vibration, electromagnetic wave, and temperature gradient" [2]. A Charge Pump (CP) is a SC circuit that is heavily utilized in energy harvesting and memory circuit design to create multiple on-chip supply voltages. Most CPs use large and expensive capacitors that lead to larger chip areas, higher power consumption and potentially, off chip components. Current research is aimed at increasing the power efficiency of the CP and reducing the area that the CP occupies. Any improvements that are made with respect to these issues have a high impact on the performance of the entire IC because of how expensive the CP is. It is also expected that by the end of 2020 there will be 50 billion devices connected to IoT [3]. With this in mind, any efforts to improve CP performance can directly contribute to some of the most popular industries in today's day and age. There is no one figure of merit to describe the overall performance of a CP as generally each design has a set of constraints such as output requirements, area, rise time and power efficiency. Most of the recent research efforts for CP design have been in the volatile and flash

memory domain which generally have a power consumption magnitudes larger than what is seen in an energy harvesting domain. However, many of the efforts are able to extend across multiple domains and designs. Some of the more notable efforts are described as adiabatic design methods. The fundamental property of adiabatic design is to recycle charges that would otherwise be heading into the ground terminal. An example of an adiabatic design process is shown in [4] where charges are stored in a virtual ground capacitor and recycled into other circuits. Another adiabatic design strategy is to implement efficient gate controlling strategies, such as the ones seen in [5]. A Linear Charge Pump with adiabatic gate control is presented in this work.

1.2 Methodology

In this thesis an integrated energy harvesting $7nm$ FinFET (Field Effect Transistor) charge pump with adiabatic pumping strategies is proposed. The goal of this design is to convert a $150mV$ power supply generated from an energy harvester to a regulated $650mV$ pumped output voltage where it can supply $1\mu A$ of load current in steady state (SS) operation. The design and analysis of this system is conducted using Cadence Virtuoso Schematic L-Editing, Analog Design Environment and Spectre Circuit Simulator tools using the $7nm$ FinFETs from the ASAP7 $7nm$ PDK [6]. This experiment is confined to the schematic and simulation stage as the software tools were not available to verify layout vs schematic (LVS) or to extract parasitics from the netlist. To provide a general road-map of this work, the remainder of this thesis is structured as follows: Chapter 2 discusses some of the related research addressing the challenges facing energy harvesting CPs. Chapter 3 introduces FinFETs and discusses their general operation with respect to traditional CMOS devices. Chapter 4 discusses basic CP operation as the Dickson Charge Pump is analyzed. Chapter 5 discusses the circuits in this design that are required for the CP to function such as the clocks, pump drivers and the pumps themselves. Chapter 6 discusses the circuits in this design that perform the regulating aspect of this design as well as the results

and an objective comparison between this work and other state of the art CPs. Since the regulation circuits are not necessary for the CPs to perform their basic function, they are not included in Chapter 5 as they tend to vary across designs. Chapter 7 discusses some recommendations for future research and Chapter 8 is a summary of the work presented in this thesis.

2. RELATED WORK

2.1 Linear Charge Pumps and Adiabatic Principles

To combat these challenges mentioned above, newer and more complicated CP topologies have been invented to achieve higher efficiencies, lower supply voltage levels and lower power consumption. Linear charge pumps and cross coupled charge pumps are a couple of possible topologies that are commonly implemented in low voltage applications. Current research generally implements one of these low power topologies in combination with adiabatic design principles. One of the better topologies for ultra low voltage applications is the Linear Charge Pump (LCP) as it cancels out the threshold voltage drop when compared to other topologies. One of the ideas investigated in this thesis is to take advantage of some inherent characteristics that are present in FinFET technologies. The advantages of FinFETs include low body effects, faster switching speeds, lower threshold voltage and lower power consumption [7]. The lower threshold voltage is key to get great performance at lower supply voltages. These characteristics are exploited in the design of the CP system presented later in Chapter 5 of this thesis.

The CP that is used in this design is classified as a Linear Charge Pump (LCP). This style of CP was first explored in [5] where they used adiabatic gate control strategies proposed by [8] where an external inverter level shifter is added to control the gate of the charge transfer switches (CTS). [4] was first to propose the virtual ground solution to reduce the energy consumption in CPs. Their strategies resulted in a 46% leakage energy reduction in a 45nm process. Another interesting experiment performed in [9] shows that controlling the body potential of the CTS can reduce the threshold voltage of the device allowing the CP to work at even lower voltages. [10] proposed an adiabatic LCP capable of converting $390mV$ to $850mV$ at a very

high efficiency of 59.2%, however, can only provide 250nA. An extensive search was performed to try and find similar FinFET charge pumps to this design, however, only one was found and is presented in [11]. The work performed in [11] can convert $96mV$ to an output voltage of $475mV$ but also only at a very small load of 47.5nA which resulted in a 42.9% efficiency as well as having multiple off-chip inductors which is generally not desirable as inductors are very large. The research conducted in [12] designed a cross coupled CP that has an impressive conversion of $70mV$ to 1.25V at a very high efficiency of 58% with a large output current of $12\mu A$. These results are very impressive, however, an off chip capacitance of 10nF was used to achieve these results. For reference, that is 133 times bigger than the capacitance used in this design and other comparable research presented in this work. As the last few results suggest, many low voltage charge pumps are able to create high voltages with high power efficiencies, but most are only able power a small (nA) current load. Of the results found, the ones that can achieve an output current over $1\mu A$ has undesirable off-chip components. These results provide the basis for the design constraints set for this work to achieve $1\mu A$ of load current without any off-chip components while still converting a very small voltage of $150mV$ to near the maximum power supply that the FinFETs in the PDK used can handle which is $700mV$. This work also aims to provide the smallest rise-time of the compared designs. The adiabatic gate control strategies as well as the LCP topology and its specific operation that are implemented in this design are similar to [5], [8], [10], [13], [11] and [12] and are discussed in Chapter 5.

The top level block representation of the proposed design is shown in Figure 2.1 and will be referenced often in this work. It is offered well before discussing the individual aspects of each block to allow better familiarization. There is an ! attached to the pumped output voltage because this implies that it is a global node. Generally, this makes it easier to design larger circuits in Virtuoso as the connection to a power supply is inherited through the design hierarchy. The figure shows that an energy harvester is providing the power supply, V_{DD} to the rest of the circuits. The general

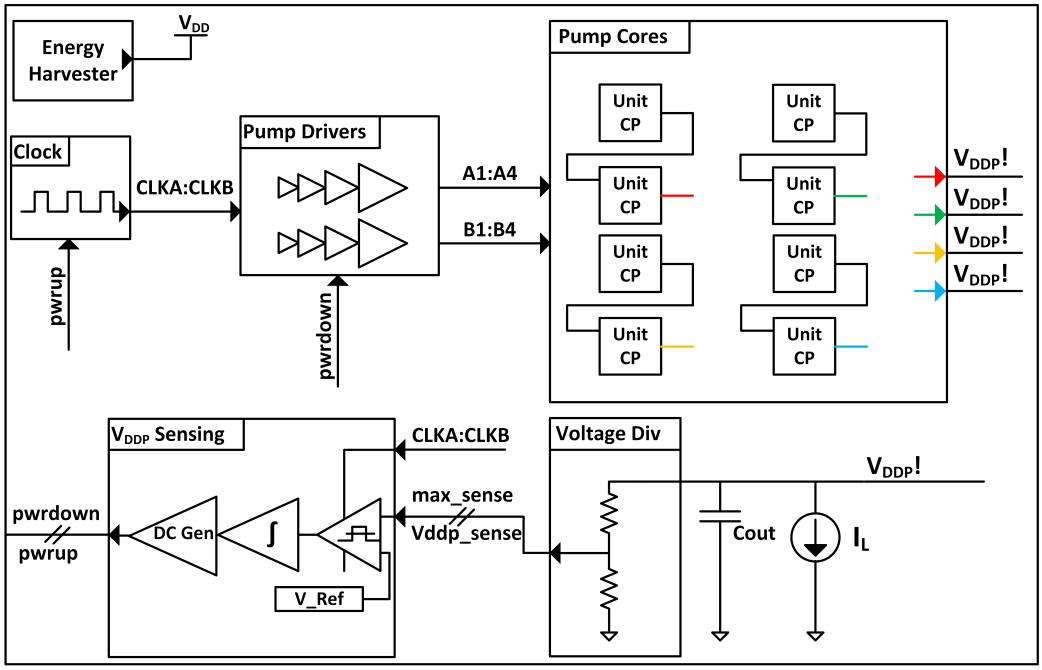

Fig. 2.1. Block Diagram of Proposed Charge Pump System

order in which this thesis presents the information regarding specific blocks and the circuits within Figure 2.1 can be viewed as a clockwise directional loop. For example, in Chapter 5, Clock is presented first, then Pump Drivers, then Pump Cores, where it wraps around to Voltage Div and VDDP Sensing, which then returns to the clock.

3. FINFETS

3.1 FinFET vs Traditional CMOS

The FinFET devices used in this work are from the ASAP7 $7nm$ Process Design Kit (PDK) that was developed by Arizona State University in partnership with ARM Ltd. to be used for academic purposes. This is a realistic PDK based on the assumptions for the $7nm$ technology node and is not tied to any foundry [14]. These are not to be confused with devices that are $7nm$ in length, the $7nm$ represents the width of a fin for one of these transistors. Figure 3.1 shows the general structure of a planar MOSFET to then illustrate the key differences in structure to the FinFET.

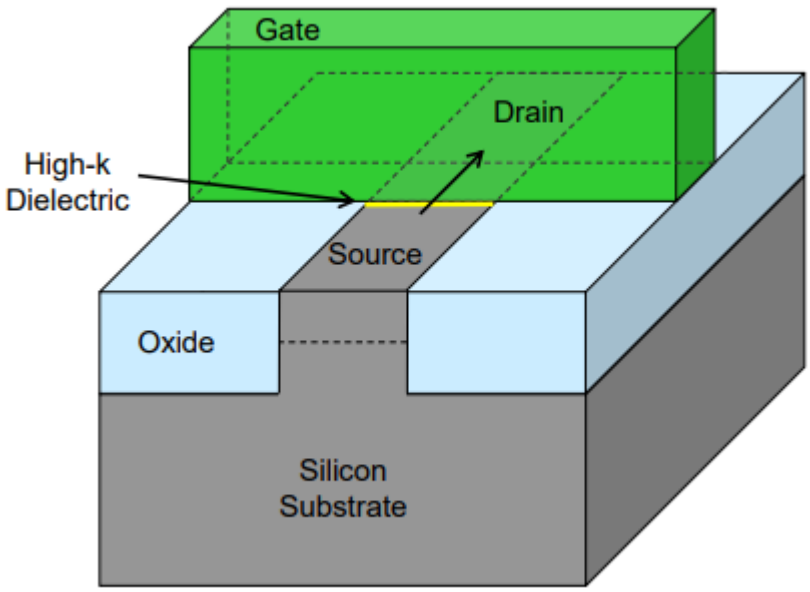

Fig. 3.1. Traditional Planar MOSFET Structure [15]

As shown, the planar transistor has a base layer of silicon, a layer of oxide grown on top of the silicon and a conductive metal gate over the oxide that separates the source and the drain. A conducting channel is formed under the gate and oxide in the silicon layer when the device is turned on and thus allows the flow of current through the device. A key feature to note is how the interaction of the gate and the substrate is planar, and there is only a singular dimension of control of the channel. Figure 3.2 shows the general structure of a FinFET with a single fin. It is fairly obvious that the planar MOSFET seen in Figure 3.1 and the FinFET in figure 3.2 have the same relative components. However, the key difference is the interaction of the gate and the substrate. Instead of a singular interaction, there are now 3. This helps provide better control of the channel that allows current flow. One of the biggest advantages of this fin feature, is that the conduction channel is now vertical and can be closely packed together as opposed to a standard planar MOSFET. Another advantage of

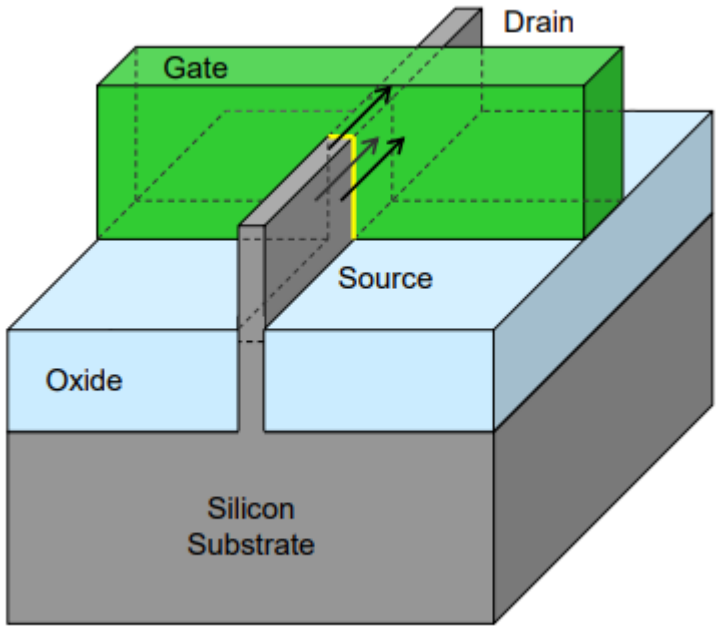

Fig. 3.2. Single Fin FinFET Structure [15]

the FinFET structure is shown in Figure 3.3 where a device with 3 fins is shown. By increasing the number of fins, an increase in drive strength is observed as this effectively increases the width of the device and allows more current to flow. With respect to the ASAP7 PDK, the designer has the option to increase or decrease the amount of fins, which actually scales the device width in the parameter file given by the PDK. The ability to easily increase the drive strength of FinFETs has allowed

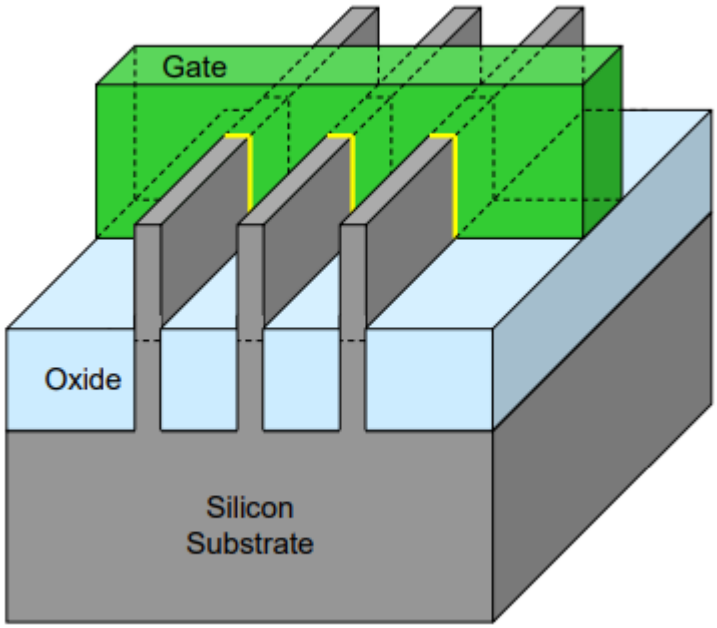

Fig. 3.3. Tri-Fin FinFET Structure [15]

transistor densities on silicon chips to increase significantly. FinFETs provide another path for the semiconductor industry to be able to keep up with Moore's Law, which states that the number of transistors on a dense IC doubles about every two years [7]. Another option to increase the drive strength of the FinFETs, instead of adding more fins, is to increase the height of the fins vertically. When reducing the size of the conventional Planar MOSFET to a similar $7nm$ node, the length of the gate is aggressively shrunk to around 12-14nm [16]. This process of decreasing the length of the gate, will increase short channel effects which lead to an increase in leakage current

and consequently an increase in static power consumption. This is why FinFETs are a desirably option right now is that relative scaling can be performed without drastically shrinking the gate length of the device. FinFETs are also able to reduce the amount of leakage current due to the more controllable nature of the channel. At a 1V power supply the FinFET is 18% faster than the planar MOSFET, however, at a 0.7V power supply, the FinFET is 37% faster than its planar cousin [7]. Being able to operate at lower power supply levels inherently decreases power consumption. However, manufacturing the FinFET can be a daunting task as the entire design flow of the IC changes. Fabrication methods are more complex which may require different, more expensive fab equipment and thus not be implementable for every company or foundry. An actual picture of a planar MOSFET is shown in Figure 3.4 whereas an actual picture of the FinFET is shown in Figure 3.5, which were taken with very high powered scanning electron microscopes.

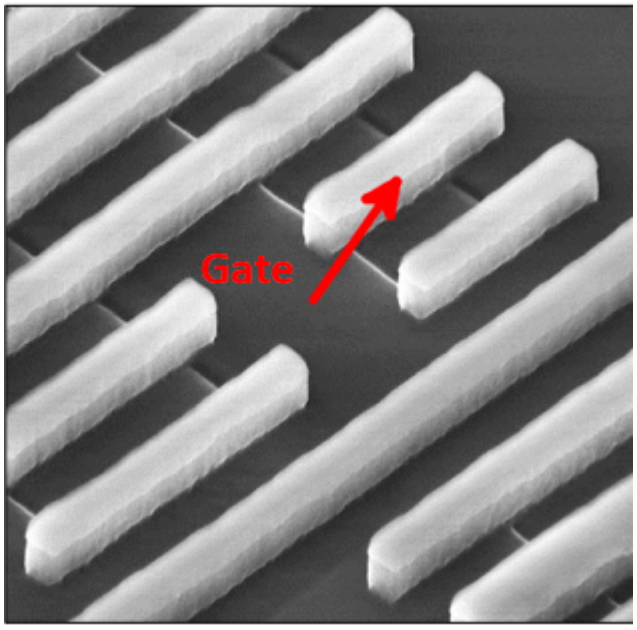

Fig. 3.4. Planar Transistor [15]

The advantages mentioned above could make FinFET devices prime candidates for low voltage energy harvesting applications as well as static random access memory

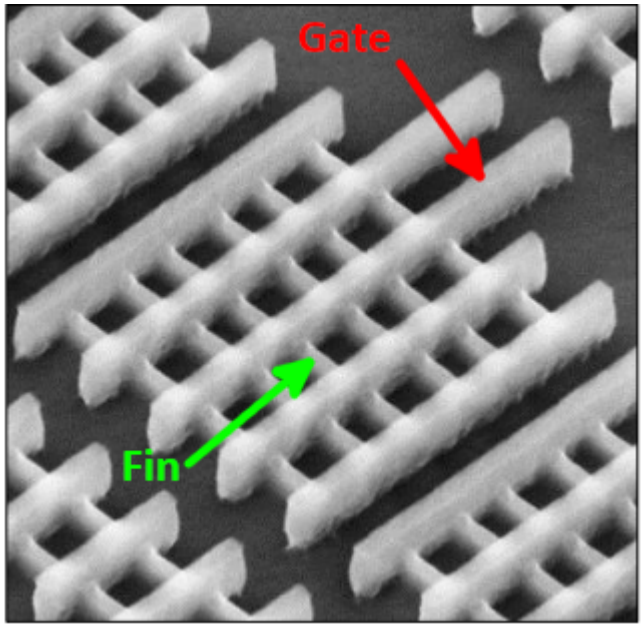

Fig. 3.5. Tri-Fin FinFET Transistor [15]

(SRAM) designs. A lot of effort has been put forth to research and design FinFET SRAM cells [17], [18], [19], [20]. However, one could argue that a full SRAM IC could not be implemented without the use of a FinFET CP. It seems, from extensive searching, that very little effort has been put forth for specific FinFET CPs with regards to any application. It was determined that the benefits of these devices outweigh the relative disadvantages, thus, this design will take advantage of the ASAP7 FinFETs for all of the circuits presented later in this work where the presented design is more suitable for energy harvesting applications, some small adjustments could make this a feasible design for an SRAM IC.

3.2 ASAP7 FinFET I-V Characteristics

In this section the I-V characteristics for 3 of the transistors in the ASAP7 PDK. In the PDK they provide an N-type and a P-type device where each has 4 different threshold voltages. There is a regular threshold device (RVT), a low threshold device (LVT), a super low threshold device (SLVT) and an SRAM device. The SRAM

device is not used in this work and thus, its characteristics are not discussed. It is shown in [14] that per each fin, the N-type device the saturation current for the RVT, LVT and SLVT are 37.85μA, 45.19μA and 50.79μA, respectively. For a 3 fin device, these currents will be multiplied by 3, which results in the RVT, LVT and SLVT at 113.6μA, 135.6μA and 152.9μA, respectively. These saturation currents match the results shown in Figures 3.6, 3.7 and 3.8 where the drain current is measured vs a sweep in V_{DS} at different values of V_{gs}. Keep in mind that the maximum power supply used in this work is a V_{DD} of 150mV. A key difference to notice is the drop

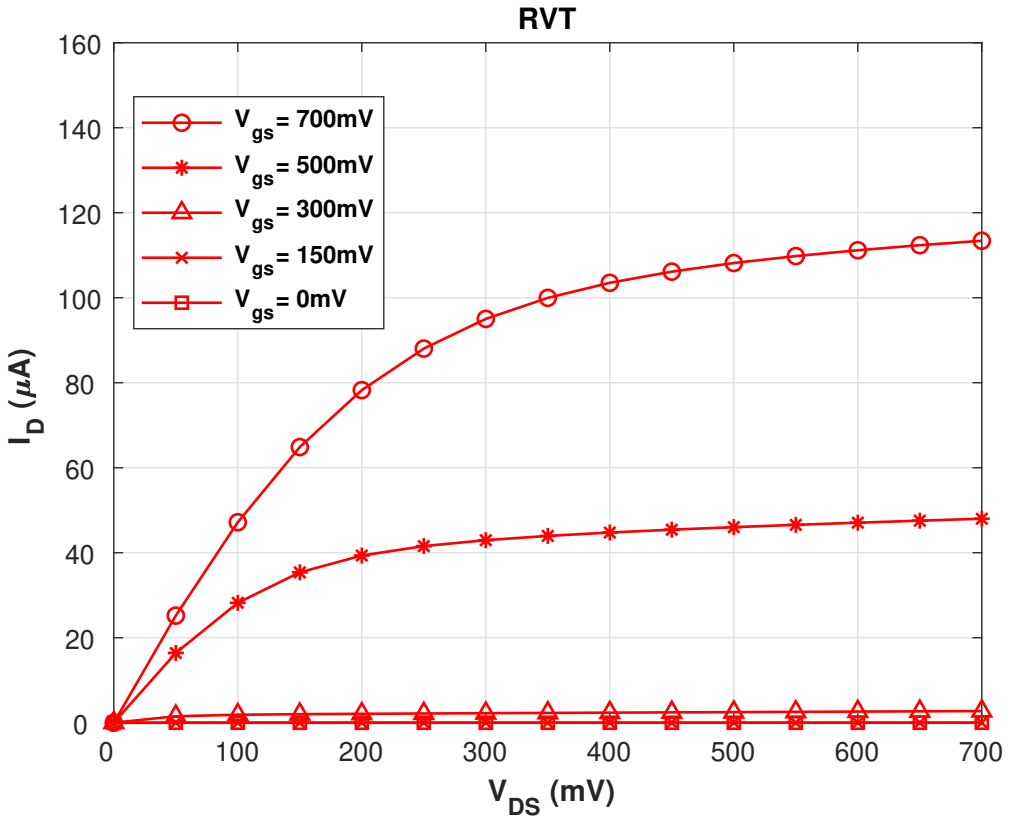

Fig. 3.6. I_D vs V_{DS} Characteristics of RVT 7nm N-FinFET

in threshold from the RVT device in Figure 3.6 to the LVT device in Figure 3.7 where for a V_{gs} of 300mV the drain current reaches a much higher value. This is very intentional design choice by the creators of the PDK and is the reason why LVT and SLVT devices perform better at lower voltages. The same pattern as above emerges

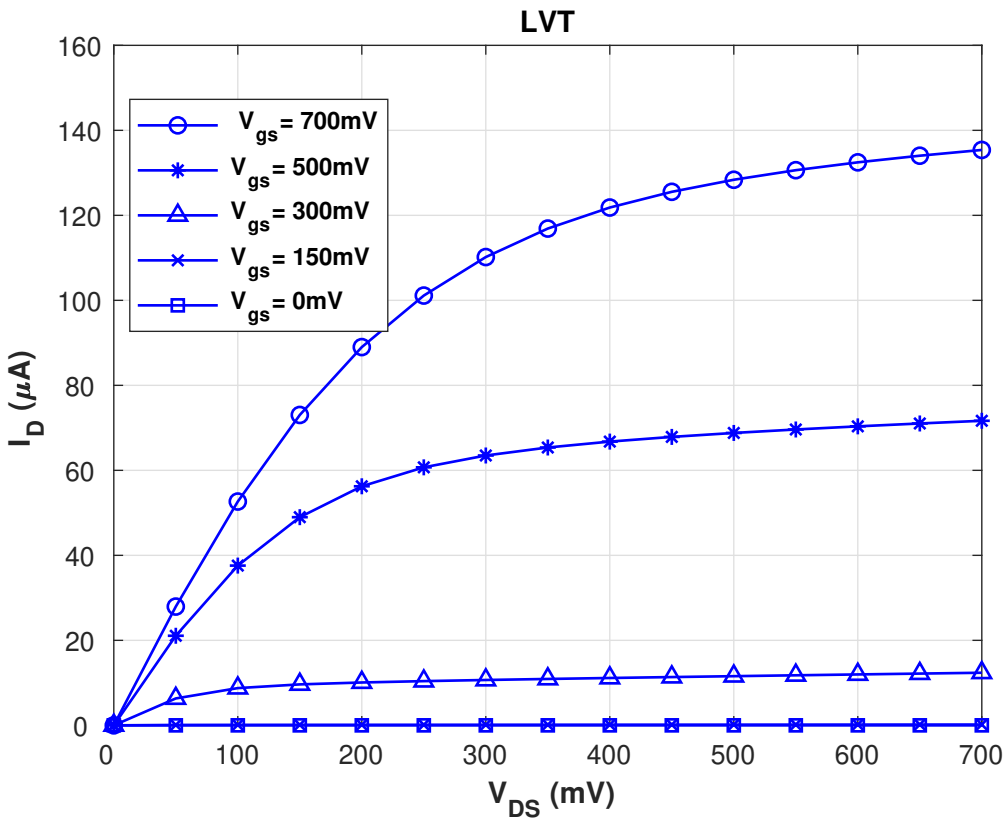

Fig. 3.7. I_D vs V_{DS} Characteristics of LVT $7nm$ N-FinFET

for Figures 3.7 and 3.8, which is also to be expected. If an SLVT device is used in a schematic later in this work, it will be distinguished from an LVT device with an extra red line with the gate of the device. This is also stated again when they appear and is very obvious to see. The SLVT devices are only used in two blocks, making the LVT device the most utilized device across the design. An interesting observation can be made from Figure 3.7 where $V_{gs} = V_{DS} = 150mV$, the LVT device still looks as if it is measuring $0\mu A$ current and thus the device would be off. However, this is not the case. Figure 3.9 shows a zoomed in plot where both the LVT and SLVT devices are plotted on the same axis to show their differences at the maximum V_{DD} used in this work of 150mV.

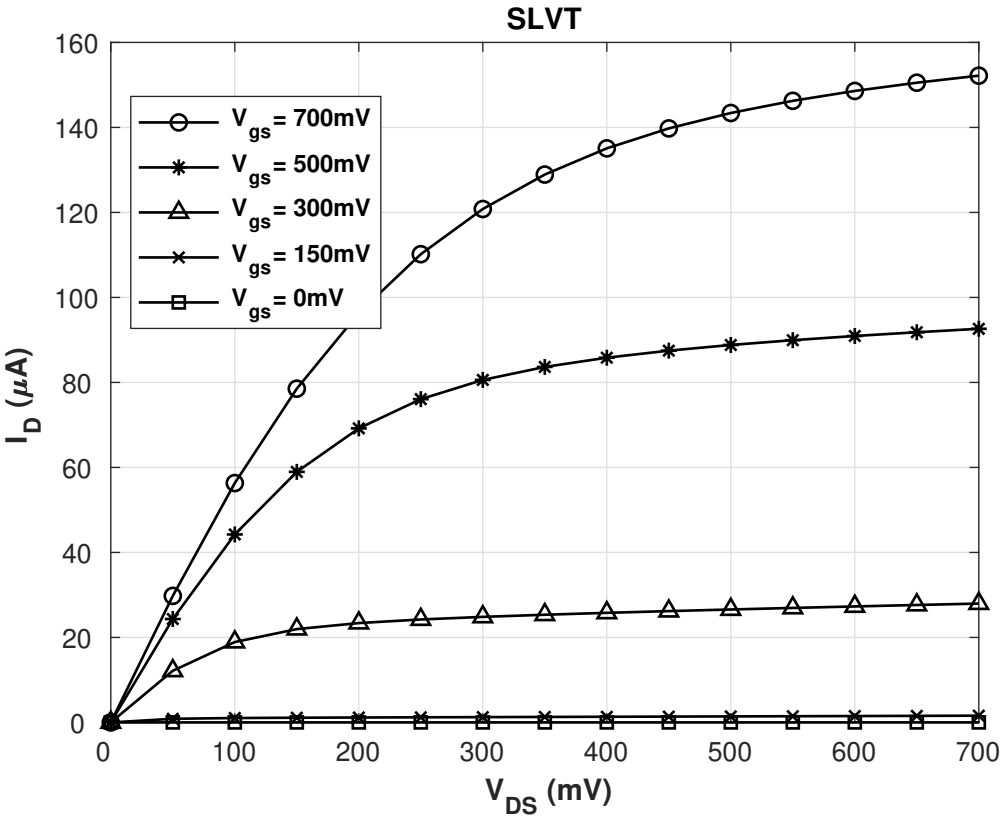

Fig. 3.8. I_D vs V_{DS} Characteristics of SLVT $7nm$ N-FinFET

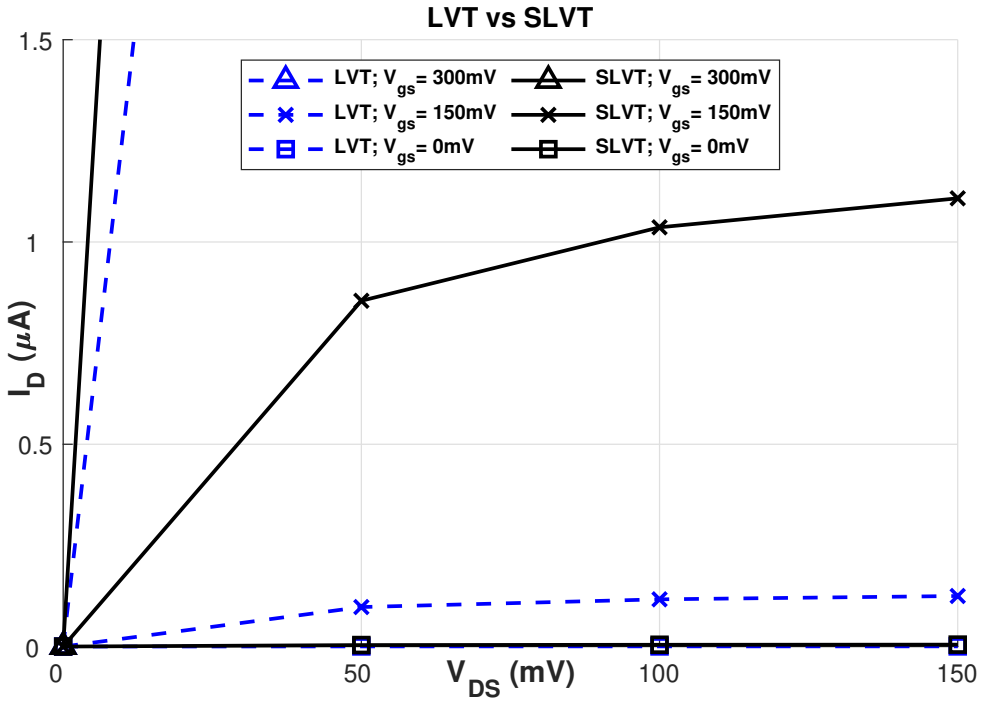

Fig. 3.9. I_D vs V_{DS} Characteristics of LVT and SLVT with max $V_{DD} = 150mV$

4. CHARGE PUMPS

4.1 Basic Charge Pump Operation: The Dickson Charge Pump

The basic principles of the CP circuit can be understood by examining the Dickson Charge Pump [21]. The Dickson Charge Pump, shown in Figure 4.1 is comprised of N

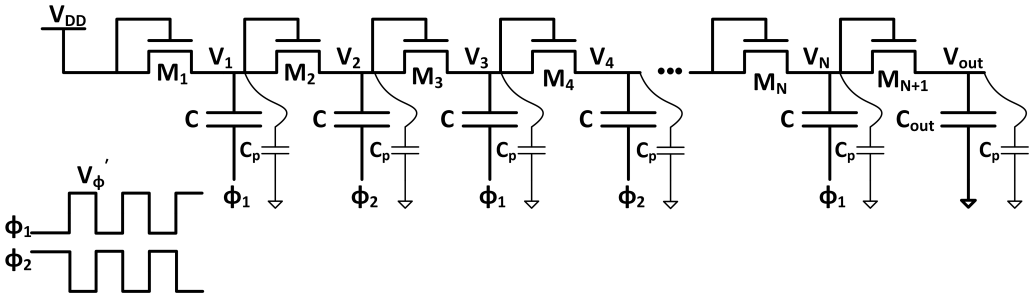

Fig. 4.1. N Stage Dickson Charge Pump

stages of diode-connected NMOS transistors and a chain of capacitors that are driven by non-overlapping clock phases ϕ_1 and ϕ_2. These clock phases oscillate between $0V$ and V_ϕ and allow the transfer of charge from the power supply to the output capacitor C_{out} by successively charging and discharging the chain of capacitors each half clock cycle. As seen in Figure 4.1, the difference of the node voltages V_N and V_{N+1} can be represented as:

$$\Delta V = V_{N+1} - V_N = V'_\phi - V_{TH} \tag{4.1}$$

where V'_ϕ is the voltage swing at each node due to the capacitive coupling from the clock [22]. Whenever the clock switches from low to high, assuming a long clock cycle, the coupled node is then increased by V'_ϕ which is a function of the charge shared

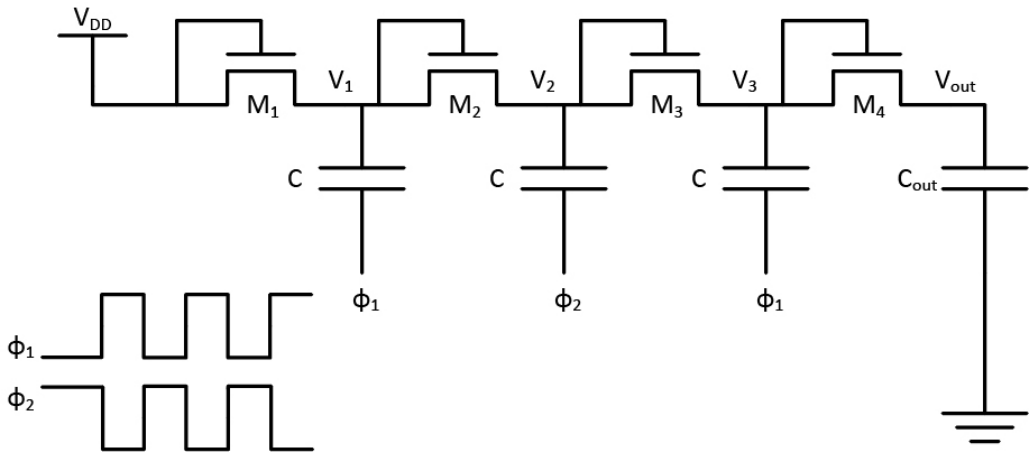

Fig. 4.2. 3 Stage Dickson Charge Pump

between the coupling capacitance C and parasitic capacitance C_p. This increase is from the principle that the voltage across a capacitor can not change instantaneously.

$$V'_\phi = \frac{C}{C + C_p} V_\phi \tag{4.2}$$

To illustrate the operation of the Dickson CP, take a simple example of 3 stages shown in Figure 4.2. Now assume an initial condition where ϕ_1 is low and ϕ_2 is high. Assuming a long clock cycle, while ϕ_1 is low, M_1 will be on, and the voltage at N_1 is charged to:

$$V_1 = V_{DD} - V_{TH} \tag{4.3}$$

where V_{TH} is the threshold voltage of the device. Next, when ϕ_1 goes high and ϕ_2 goes low, the voltage at N_1 is pumped to:

$$V'_1 = V_{DD} - V_{TH} + V'_\phi \tag{4.4}$$

As a result of the clocks switching, M_1 is off which prevents reverse current flow back into the power supply. M_2 will conduct until the voltage at N_2 is charged to:

$$V_2 = V_{DD} - 2V_{TH} + V'_\phi \tag{4.5}$$

Then, when $\phi 2$ switches from low to high, N_2 is pumped up to:

$$V'_2 = V_{DD} + 2(V'_\phi - V_{TH}) \tag{4.6}$$

This same process repeats for the 3^{rd} stage to give:

$$V_3' = V_{DD} + 3(V_\phi' - V_{TH}) \tag{4.7}$$

Then, M_4 acts as an isolating diode between the 3^{rd} stage and the output. As a result, under ideal conditions, the maximum output voltage of this 3 stage CP is:

$$V_{max} = V_{DD} - V_{TH} + 3(V_\phi' - V_{TH}) \tag{4.8}$$

This result can be generalized to give the maximum output voltage after N stages:

$$V_{max} = V_{DD} - V_{TH} + N(V_\phi' - V_{TH}) \tag{4.9}$$

Substituting equation (4.2) in to (4.9) gives the maximum voltage that can be obtained by this CP:

$$V_{max} = V_{DD} - V_{TH} + N\left[(\frac{C}{C + C_p})V_\phi - V_{TH}\right] \tag{4.10}$$

It is important to note that equation (4.10) is the result of an ideal scenario to illustrate the basic operation of a CP. Generally, there will be a load attached to the output stage that draws a current from the CP as it is acting as an on-chip power supply. The current that the CP can supply over one clock period can simply be represented as the charge transferred by each diode per clock period Q_s, multiplied by the clock frequency f.

$$I_{out} = Q_s \cdot f = V_L(C + C_s)f \tag{4.11}$$

where V_L is the voltage loss per stage to supply the average load current. Therefore, if a proper load is attached to the pump output, a more realistic output voltage is given by combining Equations (4.10) and (4.11) to give:

$$V_{out} = V_{DD} + N\left[(\frac{C}{C + C_p})V_\phi - V_{TH} - \frac{I_{out}}{(C + C_s)f}\right] - V_{TH} \tag{4.12}$$

5. CHARGE PUMP CIRCUITS

To validate the design of this CP, the components of the circuits used will be discussed with schematics, theory and waveforms.

5.1 Inverter

The inverter is a basic, yet very important circuit as it is one of the fundamental building blocks in any IC design. In this design, inverters are used to create and distribute the clock, general purpose buffers, the main CP core drivers and to guarantee the correct logic output for the comparator and in the feedback loop. The basic operating principle for the inverter is that the output will be the compliment of the input. Even though the transistors used in this design are from the ASAP7 7 nm PDK, and are a FinFET technology, they have similar functionality to standard CMOS devices. This inverter is made from one P-type device as the pull-up network and one N-type device as the pull-down network which is illustrated in Figure 5.1. An interesting characteristic that these FinFET devices have is that they do not follow standard convention when sizing the PMOS device to be twice the width of the NMOS device. The devices in the ASAP7 $7nm$ PDK are of $10:9$ NMOS to PMOS drive ratio. This follows trends reported for major foundries from 32nm planar to 16 and 14 nm FinFETs, where PMOS strain appears to be easier to obtain [6]. The width is shown in Figure 5.1 where both devices have the same number of fins, which effectively determines the width of the device. In the schematics that follow, it is assumed that all unlabeled devices are LVT and have 3 fins. The waveforms of this inverter are shown in Figure 5.2. The simulation results match the expectations of this circuit where we see the output as the compliment of the input.

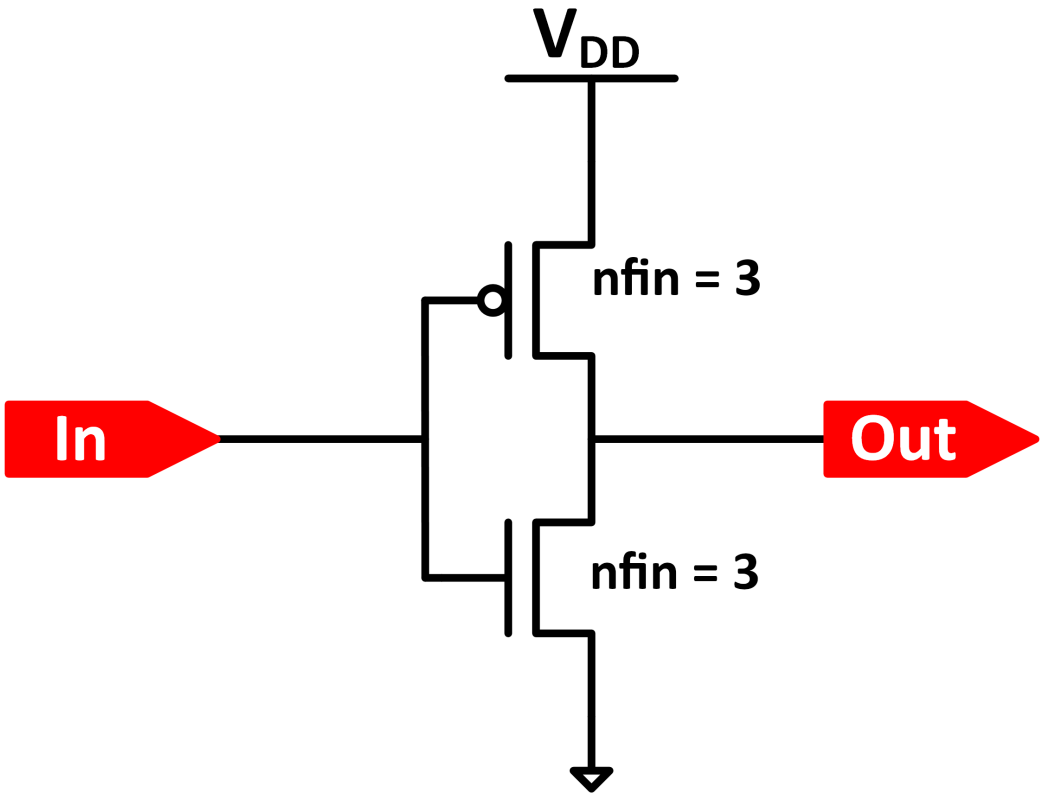

Fig. 5.1. Inverter Schematic

5.2 Clock

This section will talk about the circuits within the Clock hierarchy in Figure 2.1. This block takes the feedback control signal, called pwrup (power-up) as input which digitally selects the frequency of the output and will output two non-overlapping clock signals, CLKA and CLKB that are switching at the frequency pwrup selected. The main components of this block are the controllable ring oscillator, shown in Figure 5.5 and the non-overlapping clock generator (NOV). The other circuits included in this hierarchy are the mux, which selects the oscillating frequency of the oscillator and some buffers added between the output of the oscillator and the input of the NOV to ensure signal strength and quality. There are also buffers added to the output of the NOV to strengthen the signal before the next block distributes the clock to the

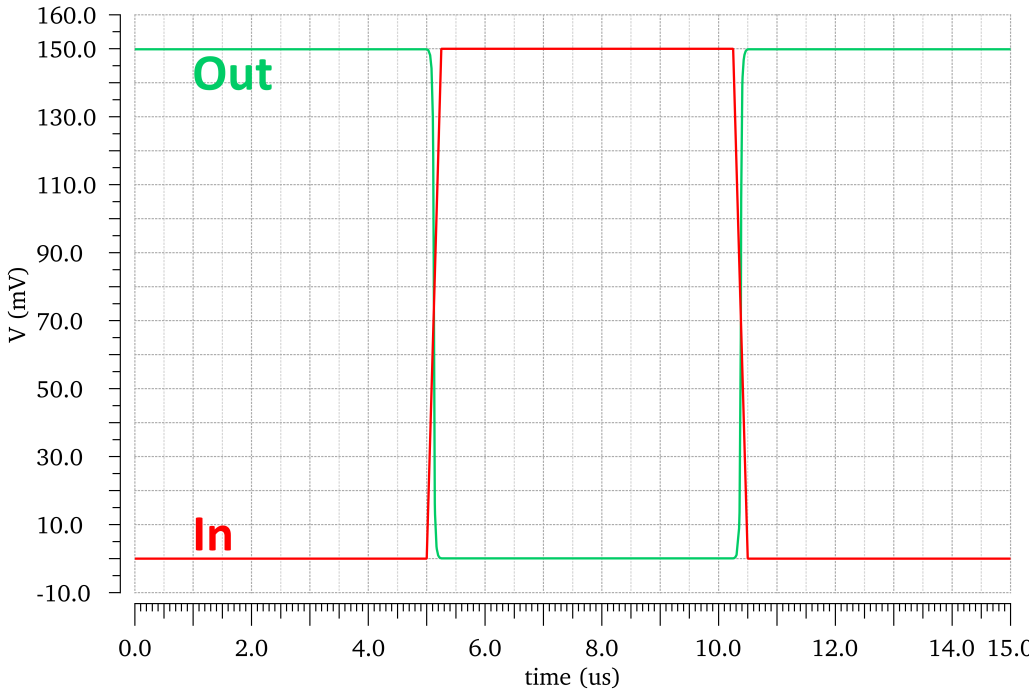

Fig. 5.2. Inverter Transient Response

Pump Cores. When pwrup is high, the selected frequency is 4MHz and when pwrup is low, the selected frequency will be 2MHz. The reason for having multiple frequency selections is to save power and to keep the CP output Voltage regulated near $650mV$ at a loading condition of $1u$A.

5.2.1 Optimum Pumping Frequency

The frequencies above were chosen by substituting ideal sources for the clock and sweeping their parameters to find an optimum pumping frequency. Some results of different frequencies and how the system responded are shown in Figure 5.3. 4MHz was chosen as it has less ripple variation and seems to be a relative max as increasing the frequency from there did not seem to improve the (SS) efficiency (η). η is defined as the ratio of the output power to the input power and is shown in Equation (5.1).

$$\eta = \frac{P_{out}}{Pin} = \frac{V_{DDP} \cdot I_{DDP}}{V_{DD} \cdot I_{DD}} \tag{5.1}$$

Where V_{DDP} is the pumped output voltage, and I_{DDP} is the pumped output current. V_{DD} and I_{DD} are the chip supply voltage and current.

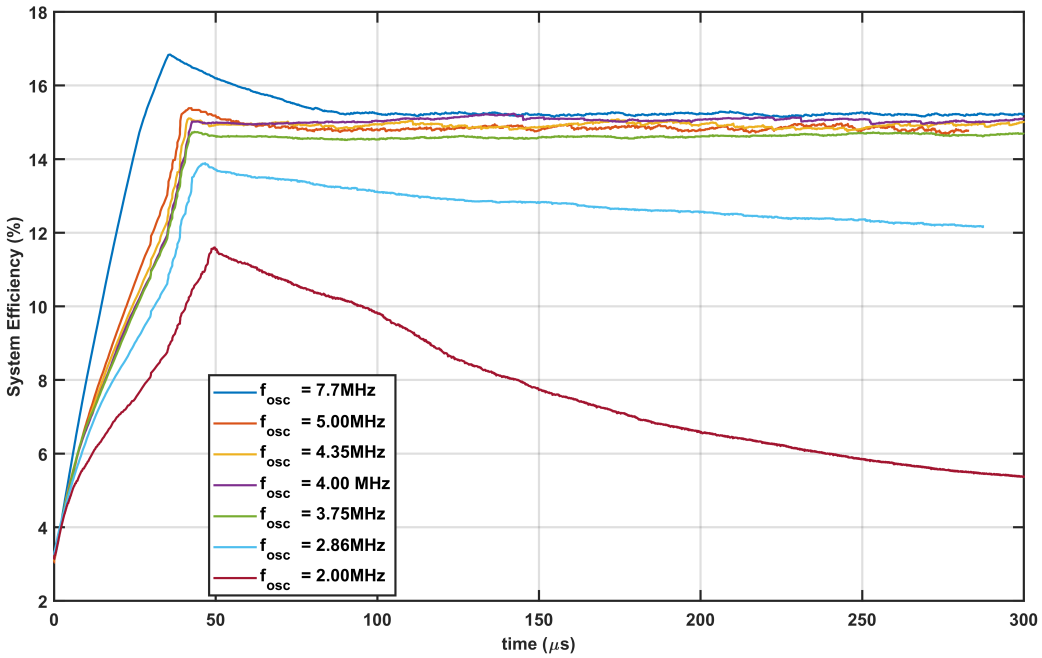

Fig. 5.3. System Efficiency at Different Clock Frequencies

5.2.2 Ring Oscillator With Feedback Control

Ring oscillators are very common circuits in CPs as they are a simple way to create the clock that is used to drive the CPs. A standard ring oscillator (RO) is shown in Figure 5.4. The operating principle of the RO is that it has an odd number of inverters connected in series where the output of the N_{th} inverter is fed to the input of the first inverter. Since there are an odd number of inverters in the chain, a high at the input, after some propagation delay, will represent a low at the output which is then fed back into the input creating the oscillating cycle. A simple RO is easy to implement but is not very practical in most designs because it can only output one

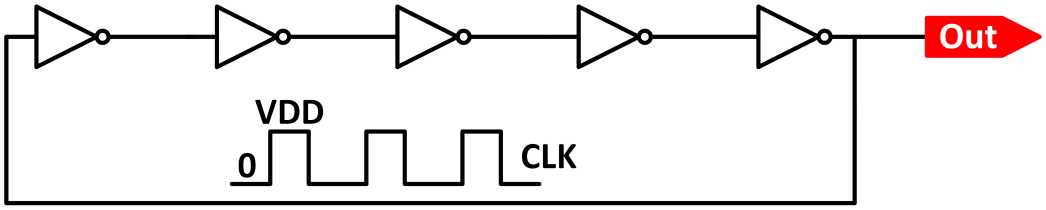

Fig. 5.4. Conventional Ring Oscillator

clock frequency. Generally, a voltage controlled oscillator (VCO) is used so that the clock frequency can be adapted automatically during operation. Figure 5.5 shows an adaptation of a general VCO from [23], however, it is not fair to say it is a VCO as it functions differently. A VCO's input is generally tied to a transistor that controls the reference current that is then mirrored into the repeated stages of the circuit. In this design, a mux is implemented to select the number of stages that the clock must travel through and thus, allowing the frequency to be controllable. The remainder of this work will refer to the oscillator discussed in this section as a mux controlled oscillator (MCO).

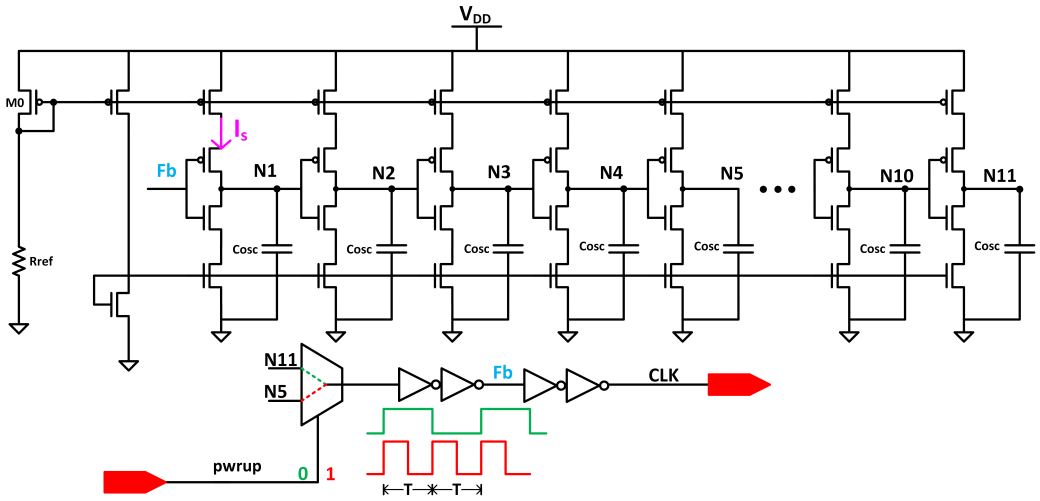

Fig. 5.5. MCO Schematic

The resistor, R_{ref}, effectively sets the current through M_0, which is then mirrored to the stages as I_s. This effects how fast the capacitance between stages charge and discharge and, as a result, the frequency of the output is changed. The oscillation frequency f of the output signal is given by Equation 5.2:

$$f = \frac{I_s}{2 \cdot N \cdot V_{DD} \cdot C_{osc}} \tag{5.2}$$

Where I_s is the current flowing through the branch, and C_{osc} is the total capacitance attached to the node joining the inverter stages. From Equation 5.2, C_{osc}, N and I_s were determined to be 8fF, 5 and 48nA respectively. Then, to still get some control of the frequency in the oscillator, a mux is added so that the selecting signal of the mux is the pwrup signal mentioned above. Based on the state of pwrup, if it is high, the mux selects the 5^{th} node to bypass the final 6 stages to give a faster frequency of 4MHz and if pwrup is low, all 11 stages are included to give 2MHz. Figure 5.6 shows the transient simulation output of the discussed MCO where it is shown that I_s is roughly 49nA, and the CLK signal responds as expected with pwrup changing. The idea for this functionality was adapted from [24] where they used a mux to control the frequency in a standard RO.

5.2.3 Mux

The mux is important for this design as it selects which frequency is given to the clock. The design for this circuit was two standard pass gates that have a selecting signal S that selects the output. A schematic of the designed mux is shown in Figure 5.7. The mux in this design was implemented with negative logic, which is less intuitive at times. If S is high, it selects the A input, if S is low it selects the B input. Because of the inverter at the input, S is pwrupF, where the 'F' designates it is the compliment of the signal pwrup while A and B are $\frac{f}{2}$ and f respectively. This logic supports that when pwrup is high, S goes low and the output of the mux, Y, is connected to B, which is the faster, 4MHz, frequency and thus, performs as expected.

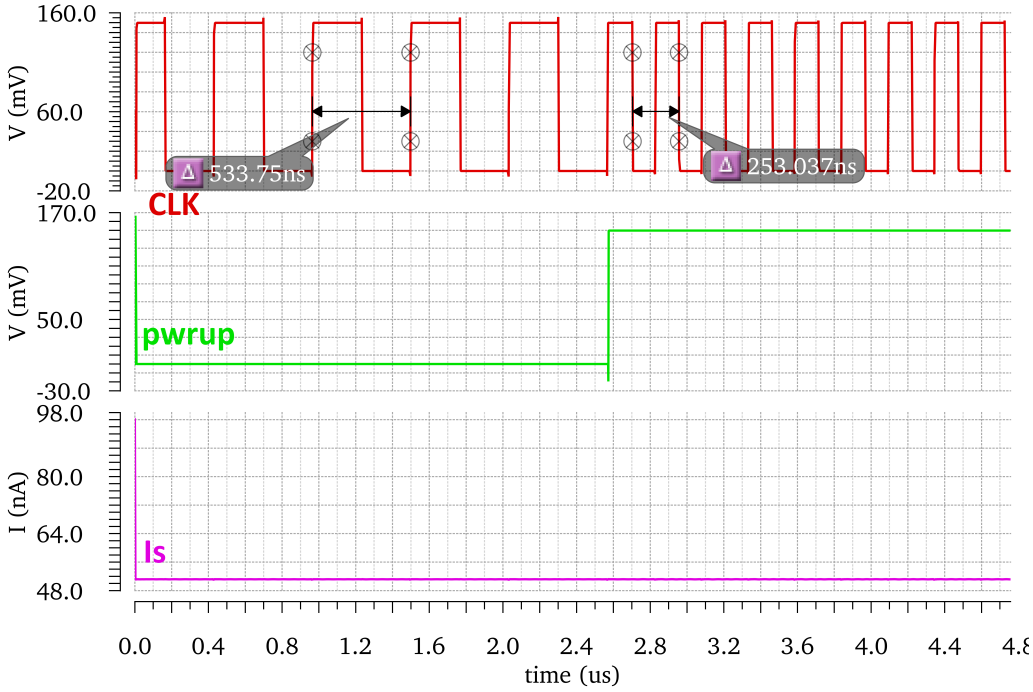

Fig. 5.6. MCO Transient Response

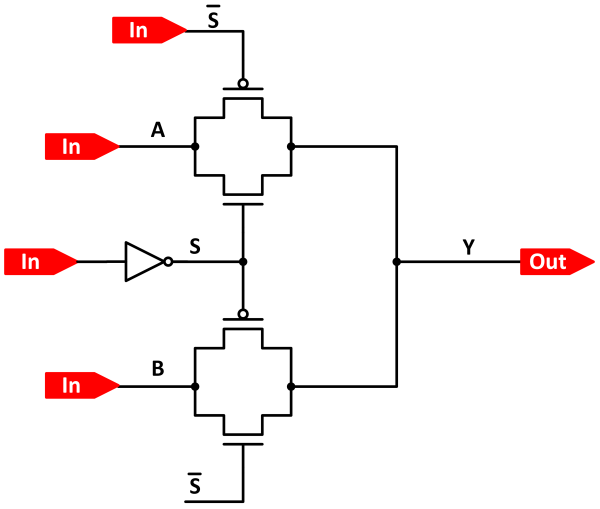

Fig. 5.7. Mux Schematic

5.2.4 Non-Overlapping Clock Phase Generator

The base for this circuit is a set-reset (SR) latch where the input is the clock generated from the MCO discussed in the previous section. This circuit will output

two clocks that are non-overlapping. This result is from the addition of the multiple buffers between the output of the nand gate and the output of the circuit. This is very key for CP design because if the clock phases overlap, reverse current will flow back through the CPs to the power supply and will negatively affect the performance of the CP. The output of the NOV is then buffered to the Pump Core Driver block, which is shown in Figure 2.1 and discussed in the next section. The schematic and transient response for the NOV are shown in Figures 5.8 and 5.9, respectively.

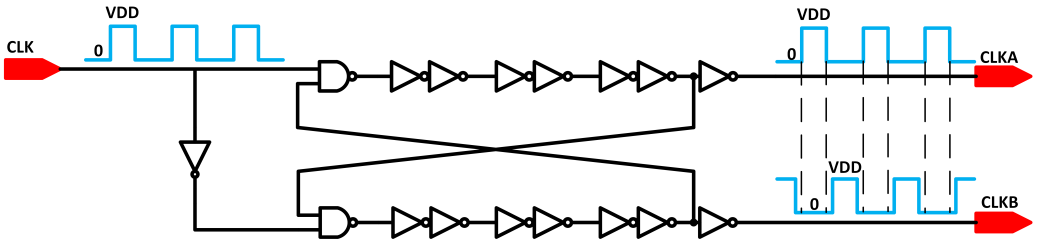

Fig. 5.8. NOV Schematic

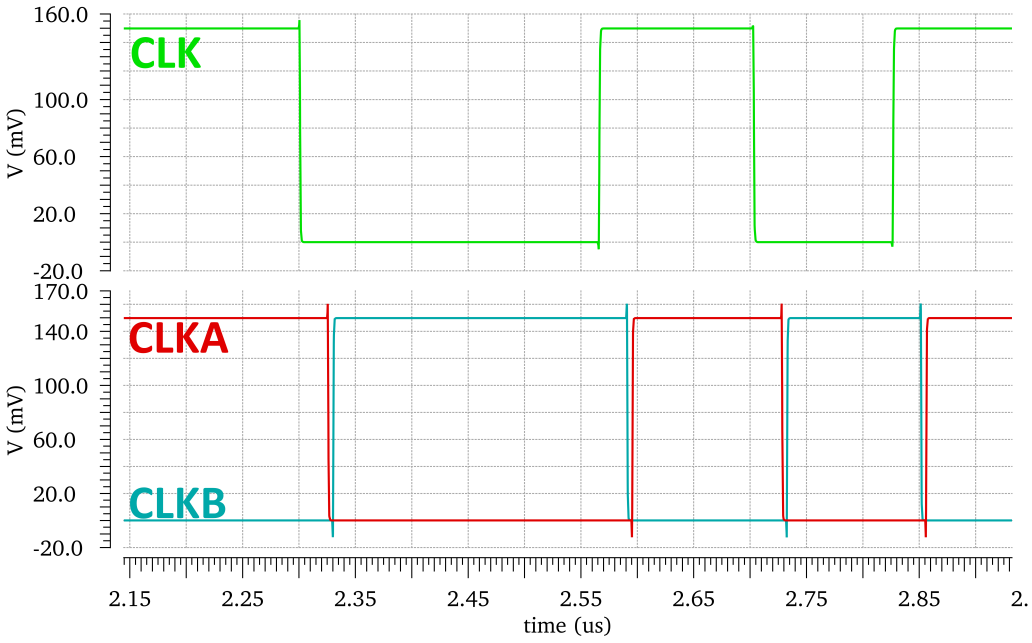

Fig. 5.9. NOV Transient Response

5.3 Pump Core Drivers

In this section, the next main block in Figure 2.1, Pump Core Drivers, is discussed. In summary, this block takes the NOV signals and distributes them to the CP cores. The other input to this block is the other feedback signal called pwrdown (power-down) that connect to the transmission gates shown in Figure 5.10. The pwrdown signal is discussed in detail later in this work but is important to introduce now as it is an input of this block. pwrdown a fail-safe to prevent V_{DDP} from going above $700mV$, which is the maximum power supply voltage for these transistors. If pwrdown is low, the transmission gates will not allow CLKA and CLKB to continue to the pumps, allowing V_{DDP} to fall to the desired regulated potential near $650mV$. This block also implements an additional instantaneous power reduction method of staggering the clocks from going high at the same time.

5.3.1 Clock Drivers

Between the output of the clock hierarchy and the input of the pumps are a series of buffers that increase in size with each additional buffer. This property is related to the drive strength of the device or fan-out (FO) and is illustrated in Figure 5.10 where a smaller inverter is followed by one of a larger size. For most designs, a minimum sized device can adequately drive 4 similarly sized devices. This is said to be a FO of 4. Since the supply voltage in this design is much lower than a conventional design, a FO of 4 degraded the clock signal enough to negatively impact the CP performance. Decreasing the maximum FO to 2 gave the clock signal very precise edges and increased the performance of the system.

5.3.2 Stagger Delay

In many designs, instantaneous power consumption can be an issue when meeting power requirements before fabrication. In this design, a delay is implemented so

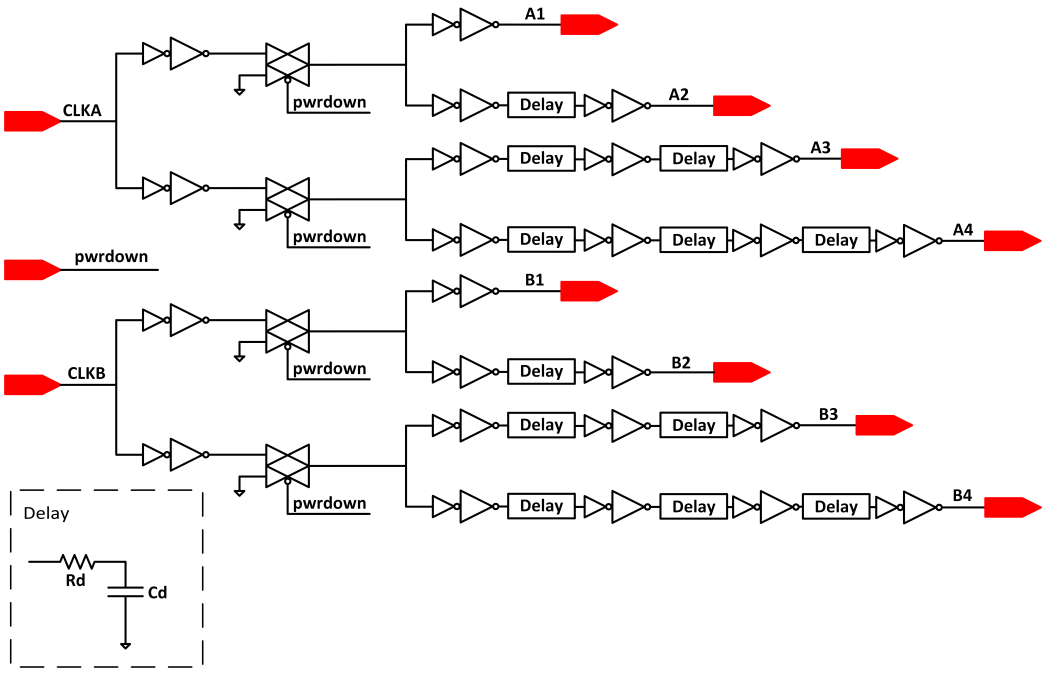

Fig. 5.10. Pump Core Drivers Schematic

that the firing of each CP is distributed, or staggered. Since the CP is transferring a sizeable amount of current on the edges of each clock, the instantaneous current drawn from the power supply required to do this is reduced by staggering the clocks. This principle is shown in Figure 5.11 with the addition of power supply current, I_{DD}, and the pumped current I_{DDP} to show their direct correlation with the distributed clocks. As shown in Figure 5.10 the stagger is created by the increased number of gates and delay blocks for each successive clock. In IC design, delays can be implemented in many different ways, one of the most common being gate delays, as these will stay consistent with variations in process and temperature. For this design, gate delays and a standard resistor-capacitor (RC) delay was implemented as it was easy to control and simulate the effect of the delay on the system. Equation 5.3 shows the time delay, t_d, of the RC pair one time constant, τ which is commonly referred

to by the Elmore time delay for lumped systems and is a representation of when the delayed signal reaches 63% of its potential.

$$t_d = \tau = R_d \cdot C_d \tag{5.3}$$

R_d and C_d were selected to be $16k\Omega$ and 200fF, respectively to give an additional 3.2ns delay to the respective gate delays for each output clock signal.

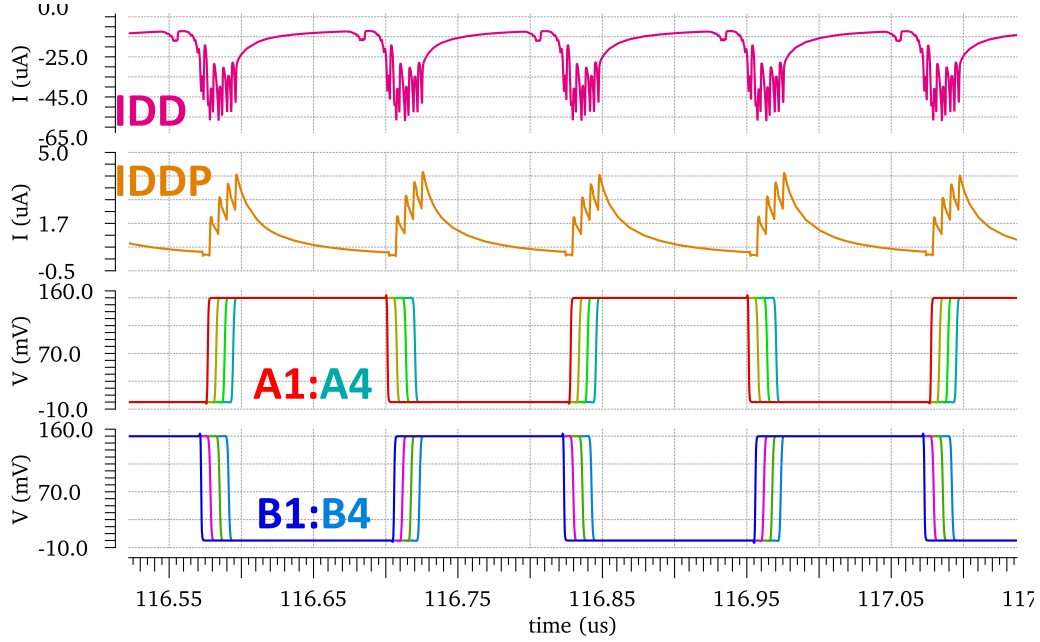

Fig. 5.11. Clock Stagger Effect

5.4 Pump Cores

In this section, the Pump Core block from Figure 2.1 is discussed. This block takes the power supply V_{DD} and the distributed clocks that were discussed in the previous section as inputs and outputs V_{DDP}, the pumped output voltage.

5.4.1 Charge Pump Unit Cell

As mentioned in Chapter 2, the CP unit cell that is used in this design is similar to the ones used in [5], [25], [8] and [26]. To make sure that the CP can operate in low voltage applications the CTS and level-shifters (LS) are replaced with SLVT devices. Replacing the SLVT devices provides better performance at low voltages since the V_T of these devices is lower than say an LVT or RVT device. The schematic for the unit cell is shown in Figure 5.12 with the accompanying waveforms to help illustrate the operation of this circuit. The first stage is a cross-coupled pair voltage

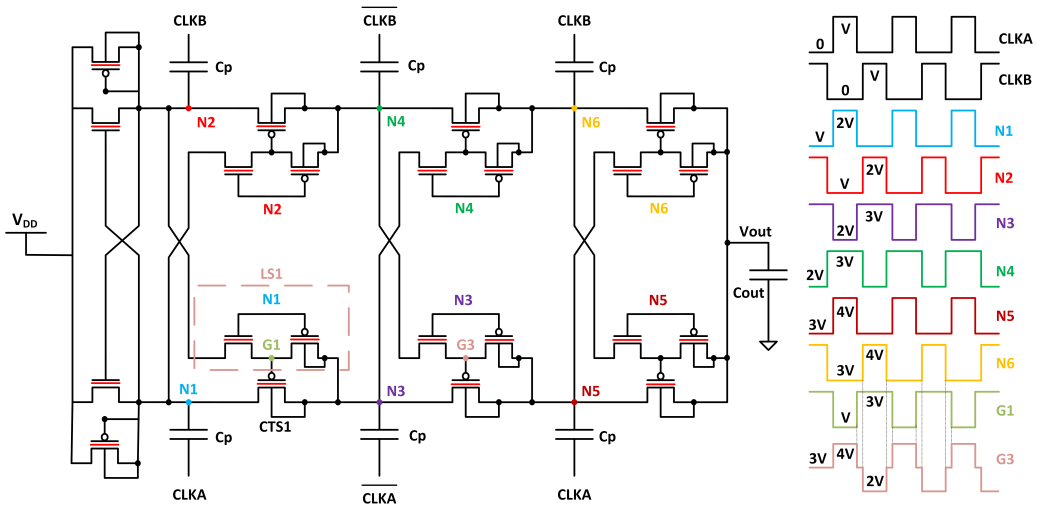

Fig. 5.12. Charge Pump Unit Cell Schematic

doubler [27] with the NMOS devices in parallel with diode connected PMOS devices that act as a startup circuit. The diode connected PMOS devices that are tied to the input, V_{DD}, allow sub-threshold current to bypass the first NMOS devices and charge the capacitors in the first stage and when the NMOS device has enough gate to source voltage, the diode connected PMOS devices are then bypassed for regular CP operation [5]. The CTS in the following stages are PMOS devices to avoid an increase

in device threshold voltage due to body effect and to reduce parasitic capacitance on the pumping nodes. The output voltage at the N-th stage can be approximated by

$$V_N = (N+1)V_{DD} - \Delta V \tag{5.4}$$

Where ΔV represents losses due to the parasitic leakage current and the voltage drop across the PMOS CTS due to it having a finite on resistance [5]. The reason this CP topology is often implemented in low voltage applications is that each LS controls the gate signal of accompanying CTS by utilizing a two-time step charge sharing strategy developed in [13]. This strategy is illustrated by the G3 waveform in Figure 5.12. This strategy allows CTS3 to take advantage of the fact that there is still charge on the capacitor from the previous stage, where the first time voltage step of G3 will initiate charge sharing between the capacitors of the two stages. This leads to a 50% reduction of the energy that is delivered by the source because the first half is coming from charge sharing. The second half is then transferred from the source when G3 is pumped up by CLKA. The total transferred energy E, is given by

$$E = \frac{1}{2}C_p(\frac{V_f}{2} - V_i)^2 + \frac{1}{2}C_p[V_f - (\frac{V_f}{2} + V_i)]^2 = C_p(\frac{V_f}{2} - V_i)^2 < \frac{1}{2}(V_f - V_i)^2 \tag{5.5}$$

where V_i and V_f are the initial and final capacitor voltage levels [1].

5.5 Output Stage

This section discusses the output stage of the CP. The output stage includes the output capacitor, C_{out} and a DC current source to act as the load current I_L. Initial design constraints of this system were set at converting a V_{DD} of $150mV$, providing a V_{DDP} near $700mV$ at an I_L of $1\mu A$ and to reach steady state (SS) in $50\mu s$.

5.5.1 Output Capacitor

The output capacitor acts as a big charge bank that holds all of the charge accumulated from the CPs which then supplies the demand from I_L. The output capacitor was selected at 75pF through simulation sweeps to meet a respectable rise time (RT) of $50\mu s$.

5.5.2 Output Voltage

The transient for the pumped output voltage, V_{DDP} at an I_L of $1\mu A$ and a V_{DD} of $150mV$ is shown in Figure 5.13 where it can be seen that the design constraints for the system were reasonably met. I_L is switched on during the transient simulation at $50\mu s$ to show the rise time of V_{DDP} and to show the functionality of the feedback loop where the maximum voltage doesn't go above $700mV$.

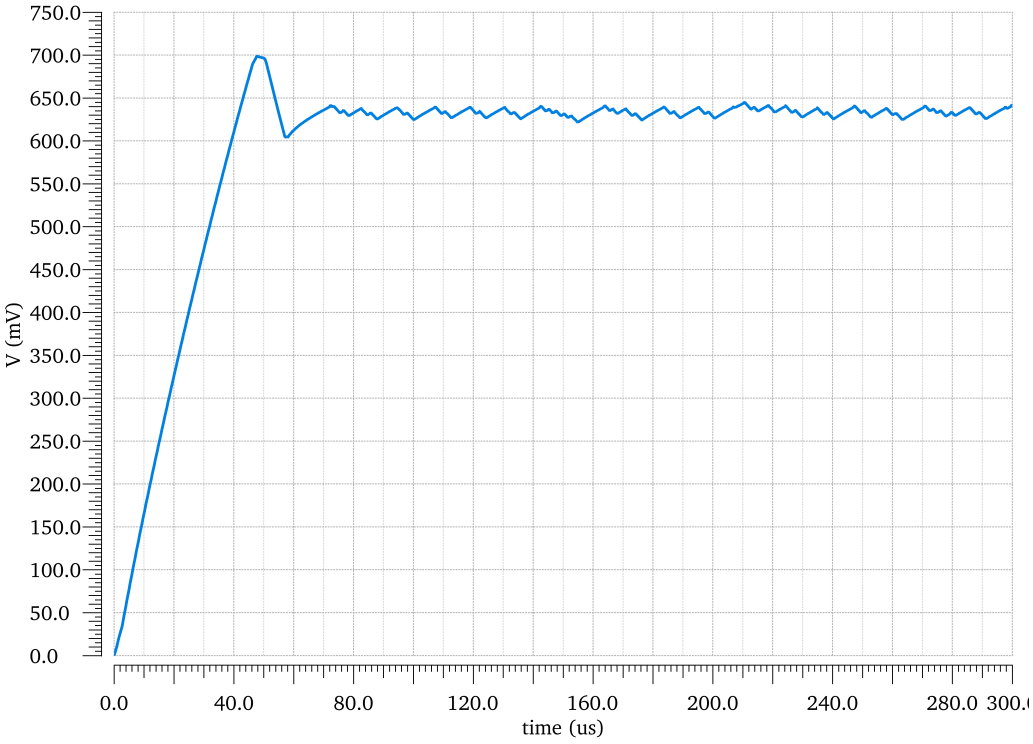

Fig. 5.13. Transient Response of V_{DDP} with $I_L = 1\mu A$

6. FEEDBACK LOOP

This Chapter discusses the remaining circuits that are referenced in Figure 2.1. These circuits are not essential for CP operation, but if the CP is going to be used in any design it should be accompanied by some sort of system feedback loop. In this work, that feedback loop consists of an output voltage divider block (Voltage Div) and the V_{DDP} Sensing block which creates the signals pwrup and pwrdown whose general purpose was discussed in the previous Chapter.

6.1 Voltage Divider

The main purpose of the voltage divider at the output is to convert the V_{DDP} signal to a lower voltage level that can be compared against some on chip reference voltages and sense what level its at. Since this design utilizes two feedback signals, two distinguishable voltage sensing signals are generated from this voltage divider called vddp_sense and max_sense. The diode stack was designed so that that when V_{DDP} is in SS, vddp_sense will be near $50mV$ and max_sense will be near $150mV$. Figure 6.1 shows the stack of diode connected PMOS devices (DCP) where it was calculated that 1 DCP is roughly $27.27M\Omega$. This technique is often used because since the equivalent resistance of the stack is so large, there is very little current flowing though the stack. Another obvious reason is that large resistors are tough to fit on ICs. A simple Ohm's law calculation gives $\frac{650mV}{11.25 \cdot 27.27M\Omega} = 2.11nA$ flowing through the stack. It is important to notice that each device has its body tied to its source rather than to V_{DD}. This is to ensure that each diode has the same bias conditions as the gate to source voltage across the devices is mirrored.

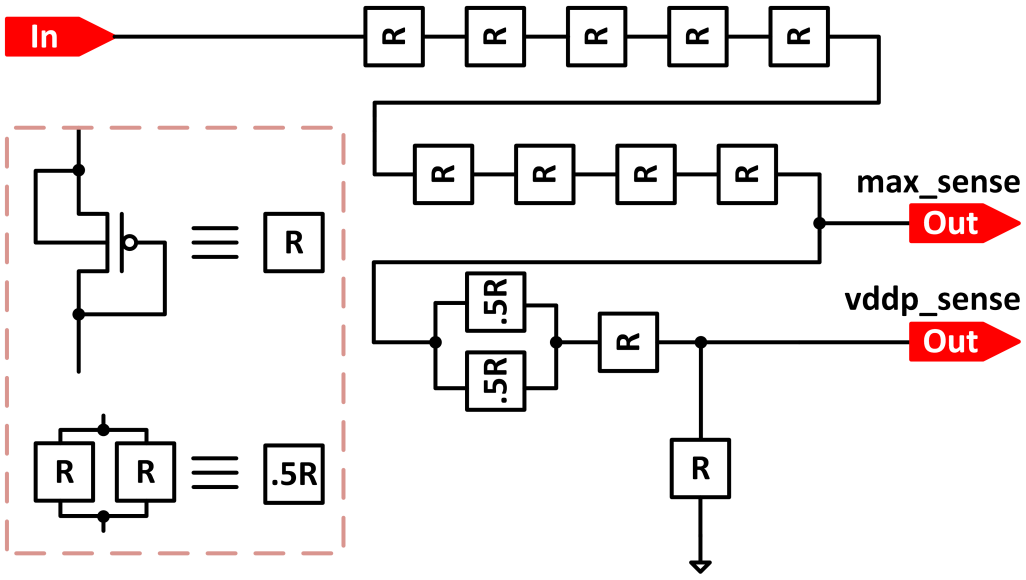

Fig. 6.1. Voltage Divider Schematic

6.2 VDDP Sensing

This section discusses the final top level block from Figure 2.1, VDDP Sensing. Figure 6.2 shows a more detailed schematic of this block than the one represented in Figure 2.1. In summary, this block takes vddp_sense, max_sense, CLKA and CLKB as inputs and generates the pwrup and pwrdown signals used to control the pumping of the cores. The main sub-blocks that are discussed in this section are the clocked comparator, beta multiplier, integrator, input buffer and the DC average generator. Throughout this section the upper half of Figure 6.2 is discussed as the process for converting vddp_sense and max_sense to a digital signal is the same for both. The only difference to note is the dc reference for the respective comparators. For this block in particular it seems logical to provide a visual of the signal progression through the stages before discussing the individual components. Figure 6.3 shows the signal input to the comparator (comp_in), in this case, vddp_sense, the reference voltage, and the resulting outputs of each stage, also labeled in Figure 6.2. It is important to note that the two signals comp_out and int_out are similar in shape and overlap on the graph which can be tough to see if skimming the figure.

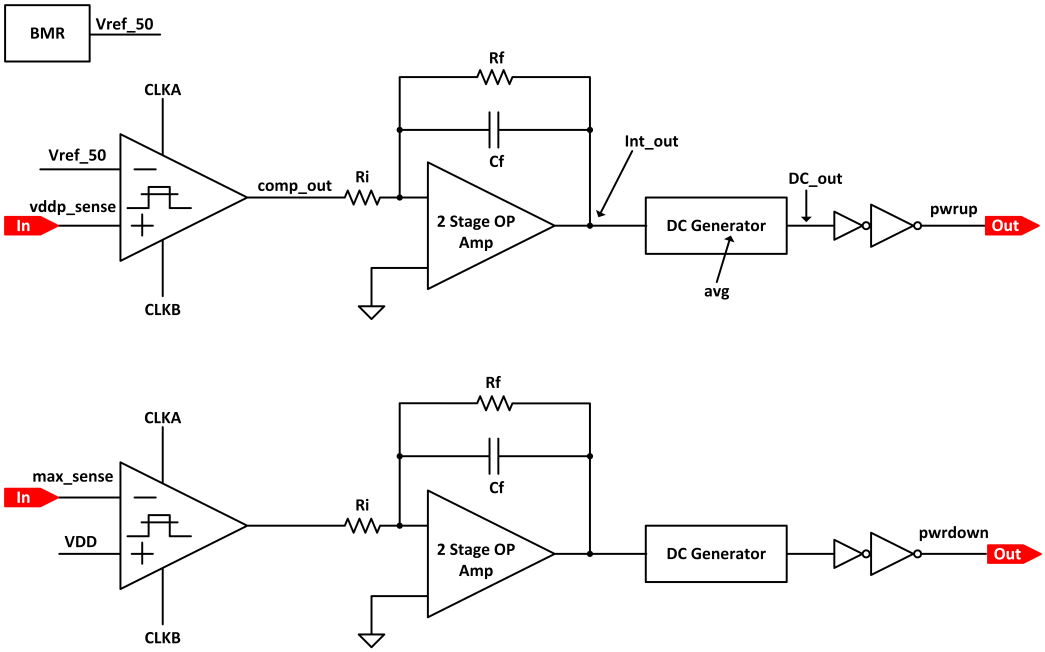

Fig. 6.2. VDDP Sensing Schematic

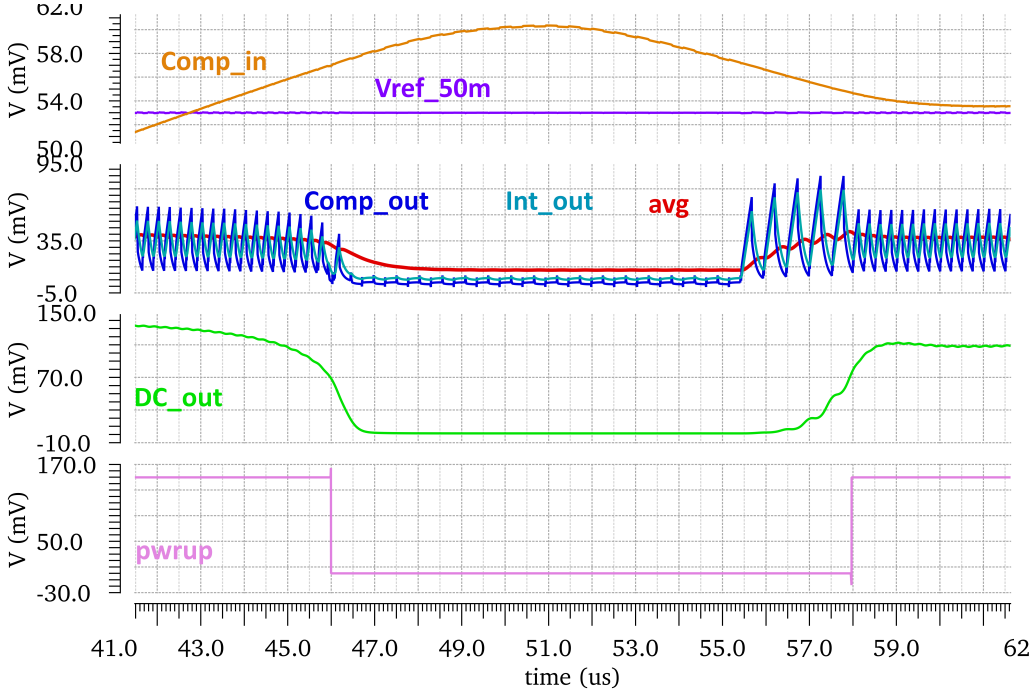

Fig. 6.3. VDDP Sense Transient Response

6.2.1 Clocked Comparator

Comparators are generally found in Analog to Digital Converters (ADCs) as they compare an analog input with a DC reference and provide a digital output that describes the relationship between the two inputs. The clocked comparator in this design was referenced from [28]. In this design, if the analog input to the comparator, vddp_sense goes above the $50mV$ reference then the output of the comparator should go from high to low. This principle holds true for the comparator used in this design which is a clocked comparator. Clocked comparators accomplish the same goal, however, the output is now a function of the input clock. As seen in Figure 6.3, the comp_out waveform oscillates at a relative 'logic' high when comp_in is below the reference but when the waveform crosses above the reference, after a short propagation delay there is a noticeable logic low. When CLKA is low, CLKB is high and the sleep transistors, S_n and S_p the comparator is said to be in a reset phase because P_1 and P_2 are on and pull the fn and fp nodes to V_{DD}, thus, turning on R_1 and R_2 which reset the outputs of the latch, OutN and OutP to ground [28]. The decision phase is when CLKA goes high, CLKB goes low, turning on S_n and S_p. At the beginning of this phase, fn and fp are both at V_{DD} and once S_n turns on, fn and fp drop with different rates based on the negative and positive inputs InN and InP. For example, when comp_in (InP) goes above the reference (InN), when CLKA goes high, N_2 will pull fn to ground faster than N_1 will pull fp to ground. fn being pulled to ground faster results in N_3 turning off and P_3 turning on. When P_3 turns on, fp is then pulled to V_{DD}, turning on R_1 which pulls OutN to ground. In summary, when InP crossed above the reference, OutN is pulled to ground. Then when CLKA goes low, OutN, is reset to ground and thus, has no impact on the state of OutN, keeping it low when comp_in is above the reference.

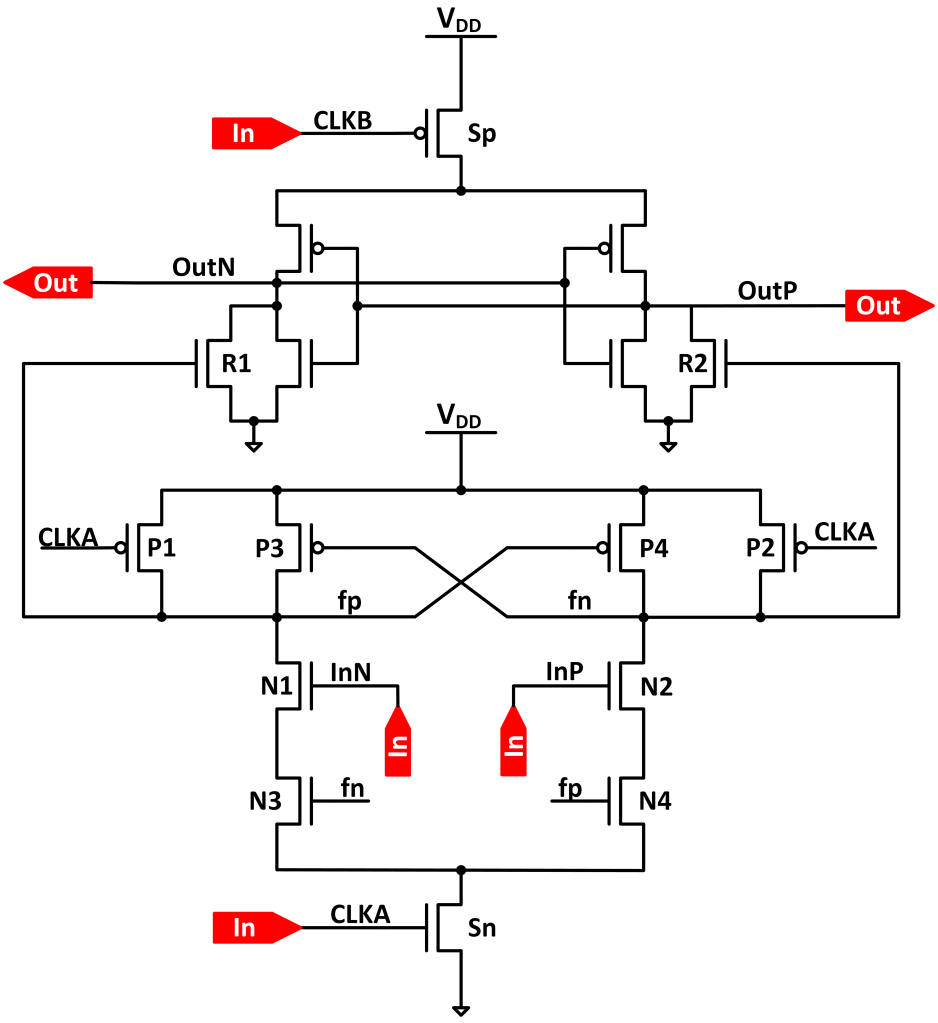

Fig. 6.4. Clocked Comparator Schematic

6.2.2 Voltage Reference (Beta Multiplier)

The Beta Multiplier (BMR) is a very common circuit used in [23] as it provides a supply independent current reference circuit that can be very useful almost anywhere on an IC. For this design, shown in Figure 6.5, every device in the circuit is SLVT as indicated by the red line though the device. The BMR is a current reference based on a PMOS current mirror and a differential amplifier in the center of the schematic. The differential amplifier inputs are V_{reg} and V_{biasn} where the output is V_{ref}. The PMOS devices create a current mirror and when V_{biasn} and V_{reg} are at the

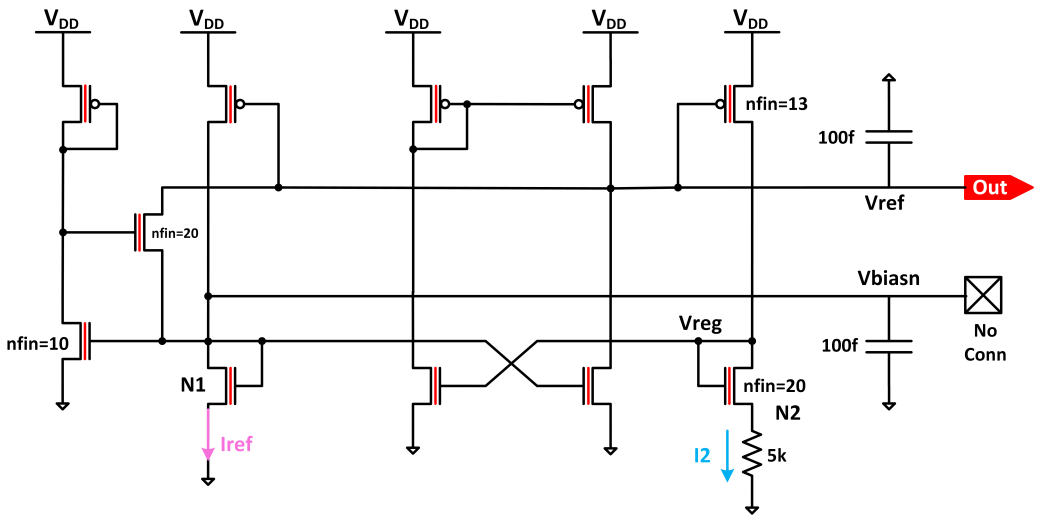

Fig. 6.5. Beta Multiplier Schematic

same potential, the NMOS devices mirror the current. If they are not at the same potential then the differential amplifier compensates for the change. SLVT devices were chosen to attempt to have supply independent biasing at such low potentials. For the BMR to act as a true current source, the reference currents should not vary with changes in V_{DD} [23]. Figure 6.6 shows the reference currents while sweeping V_{DD} to show that below $200mV$, the BMR will not act as a true supply independent current reference. The same situation occurred when initially testing the BMR with LVT devices, but the desired results were only achievable above $300mV$. With the simulations shown in 6.6, there are relatively no variations for the currents above a power supply of $200mV$, however, if this design were to be fabricated, the BMR should be re-investigated. Through simulation, the number of fins were determined and are shown in Figure 6.5 as they provided the desired voltage references of approximately $50mV$ and $30mV$ (used in the DC average generator circuit).

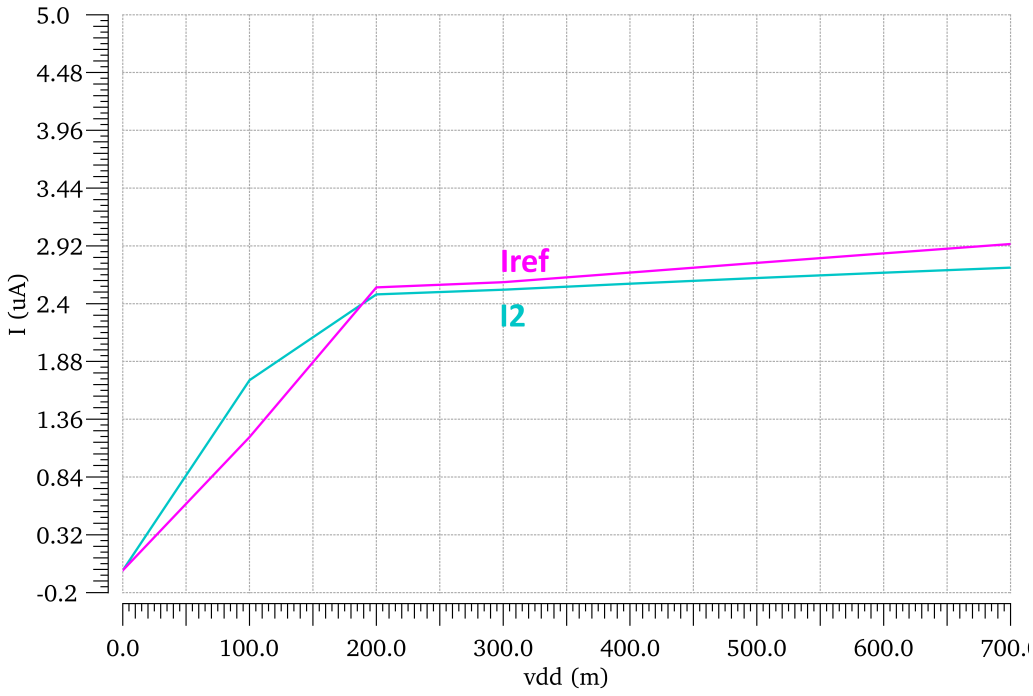

Fig. 6.6. Variation of Reference Currents with V_{DD} in the BMR

6.2.3 Integrator

The basic two stage operational amplifier is shown in Figure 6.7 and is also shown in Figure 6.2. The operational amplifier (op amp) is a fundamental building block in analog IC design as it can be configured in many different ways. Figure 6.2 shows that the op amps positive input terminal (V_p) is grounded and the negative input terminal, (V_N) is connected to the output of the comp_out and as seen in Figure 6.3, the int_out is much tighter and resembles more of a saw-tooth figure. At first, the integrator was tested to try and reduce the saw-tooth magnitude to a relative DC signal but the attempts were unsuccessful, however, with the addition of the DC average generator that is discussed in a later section it was very simple to convert int_out into a DC control signal.

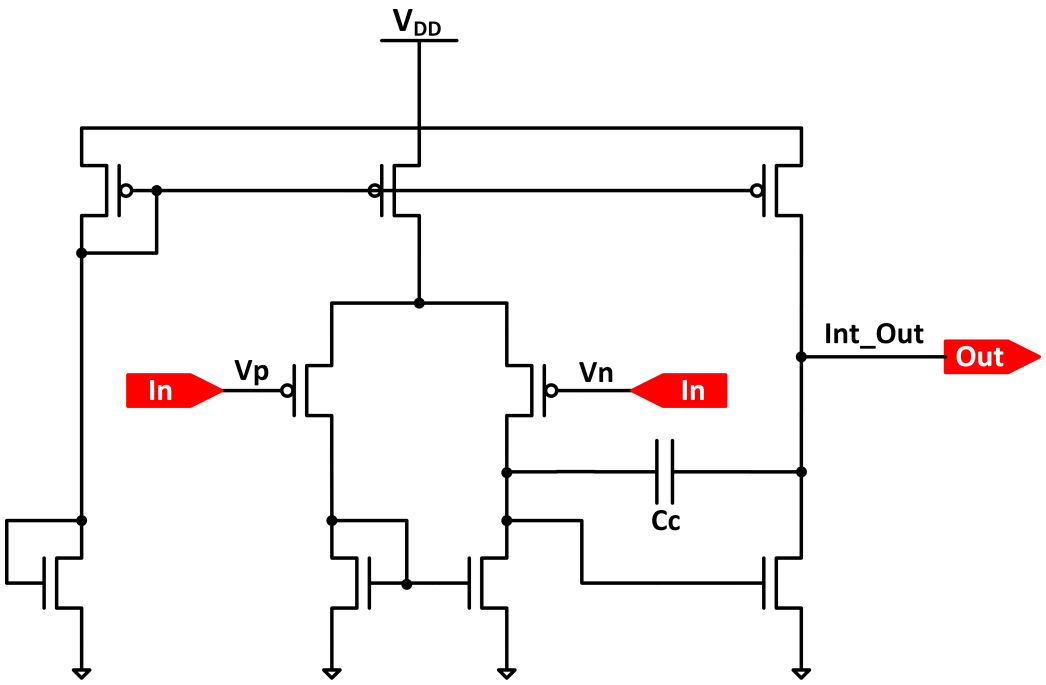

Fig. 6.7. 2 Stage Operational Amplifier

6.2.4 Input Buffer

Figure 6.8 shows a 'rail to rail' input buffer from [23] that takes advantage of two differential input buffers, one NMOS flavor and the other PMOS. As with the last few circuits discussed this circuit has differential input pairs and function similarly. The basic operation of this circuit is similar to a comparator where it has a reference voltage tied to V_n. If V_p is crossing above said reference, the PMOS device attached to V_p starts turning off and V_n becomes the dominating input, and in turn, connects the input of the inverter to ground, which pulls the output to V_{DD}. The two networks work in compliment to provide a fast response to both input signals approaching ground or V_{DD} with minimal offset.

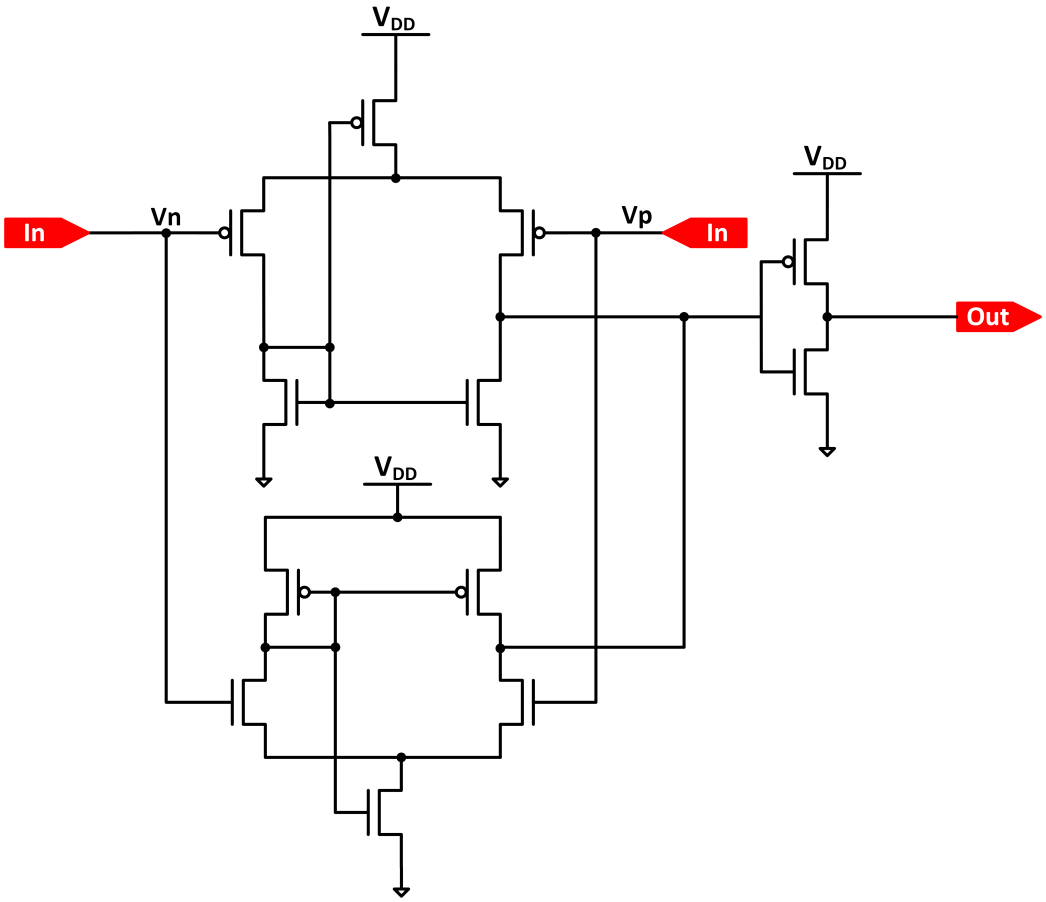

Fig. 6.8. Input Buffer Schematic

6.2.5 DC Average Generator

The final circuit in the extensive VDDP Sensing block is an adapted DC averaging circuit from [23] that is shown in Figure 6.9. When the input, DC_in, goes above the voltage stored on the capacitor, max, the output of the buffer will go low, turning on the PMOS device which pulls avg towards V_{DD}. As max starts approaching DC_in, the PMOS device starts to shut off. This results in the voltage across the capacitor, max, will correspond to the peak voltage of DC_in [23]. The same process will occur with min, except it will obviously be the minimum peak voltage from DC_in. The two resistors, R_b then form a voltage divider to average the max and min, feeding it to avg. Since the level of avg is easier to predict as a result of the integrator, the

BMR was replicated to form a $30mV$ reference and fed into a another buffer to give the signal full rail to rail potential. The resulting signal DC_out is then put through some standard buffers to drive the signal to become pwrup.

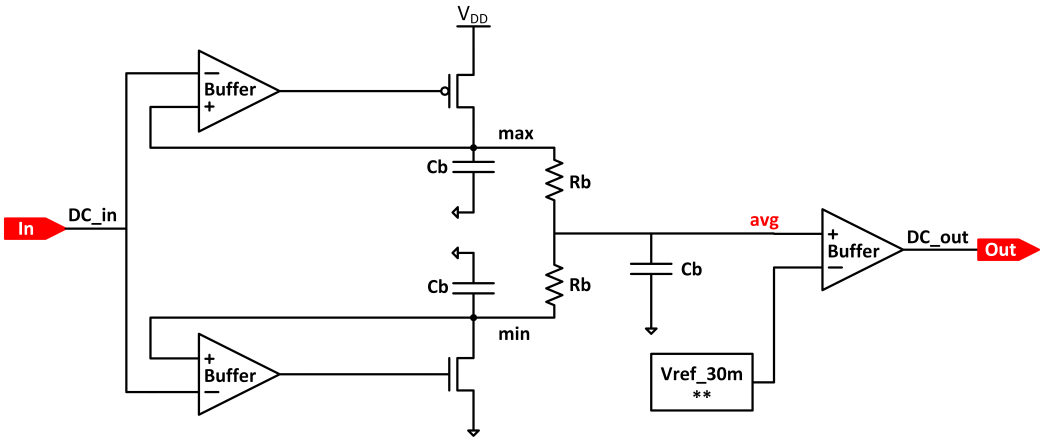

Fig. 6.9. DC Average Generator Schematic

6.2.6 VDDP Sensing Block Output Transient Response

Figures 6.10 and 6.11 show the transient response of the inputs and outputs of the VDDP Sensing block along with V_{DDP} and the clocks to show that even under zero loading conditions it does not go above $700mV$ and that both feedback control signals are accomplishing their designated tasks. As a reminder, pwrup will select the frequency of CLKA and CLKB and is shown in Figure 6.10. Figure 6.11 shows that pwrdown will prevent V_{DDP} from going above $700mV$ and that A1:B4 are not switching while pwrdown is low.

6.3 Estimated Area Calculation

A crude area approximation of the entire system was performed by plotting the layout areas of the inverters provided in the ASAP7 $7nm$ PDK and then extrapolated out using linear regression. Across the entire design presented in this work, the biggest

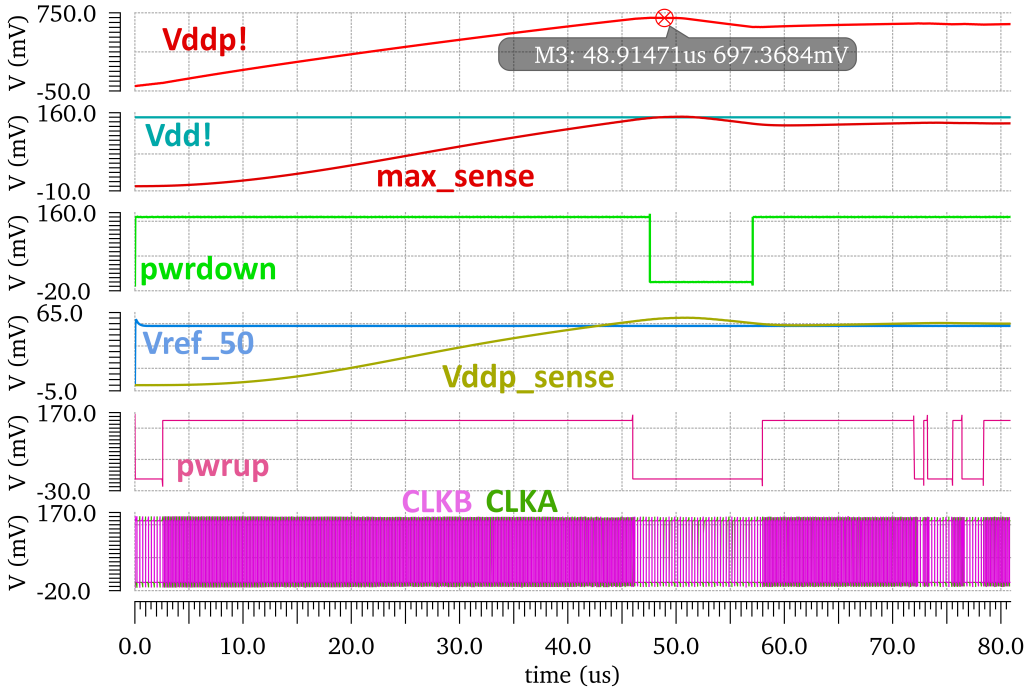

Fig. 6.10. VDDP and VDDP Sensing Transient Signals

cells are the buffers driving the pump cores. These buffers are made from a 256 sized inverter and a 512 sized inverter (invX256 and invX512). The multiple is with respect to the minimum sized inverter, which is $0.0547\mu m^2$. However, invX2 is not necessarily twice the area of an X1 because layout engineers have figured out ways to scale devices while providing the required amount of drive. As shown by Observation 2 in Figure 6.12, invX2 is $0.069\mu m^2$. The data in Figure 6.12 represents the measured layouts of the inverters provided by the PDK. Then a line of best fit was determined and extrapolated out as shown in Figure 6.13. From the data presented in Figure 6.13, it is determined that invX128, invX256 and invX512 are $2.1\mu m^2$, $4.2\mu m^2$ and $8.5\mu m^2$, respectively. In this design, there are 15 invX128 cells, 39 invX256 cells and 26 invX512. The other cells are negligible compared to these bigger cells and as seen in Figure 6.14 the estimated area of the circuits are quite small compared to the capacitors used. Since the ASAP7 PDK did not include any capacitor cells, a value of $8.65\frac{fF}{\mu m^2}$ was used in [29] as a capacitance per-area density. Assuming this can be

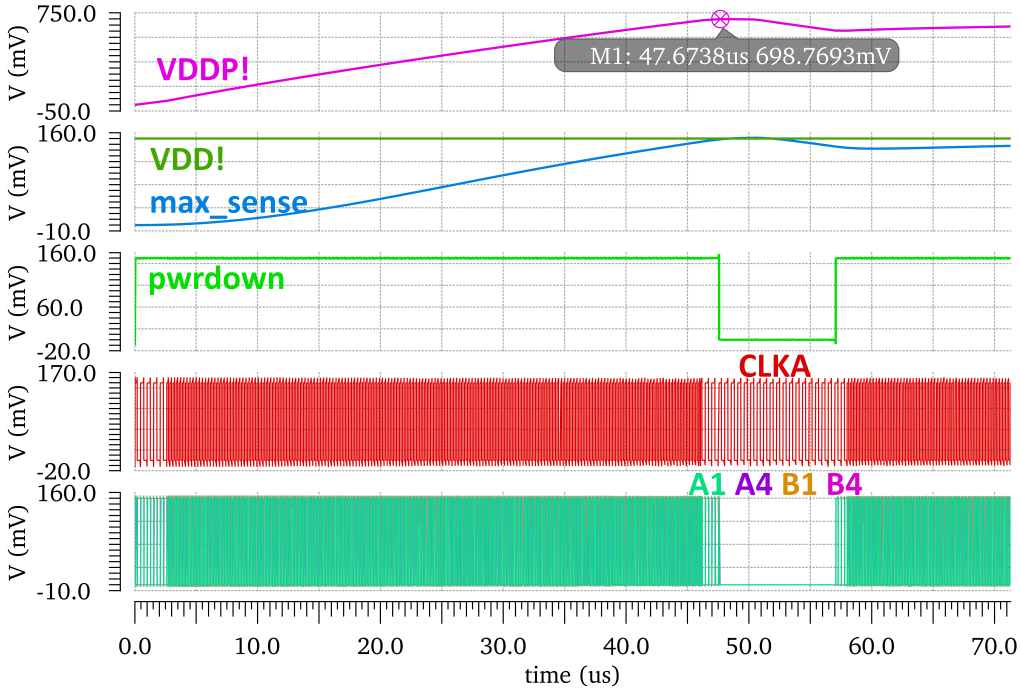

Fig. 6.11. Transient System Response to pwrdown

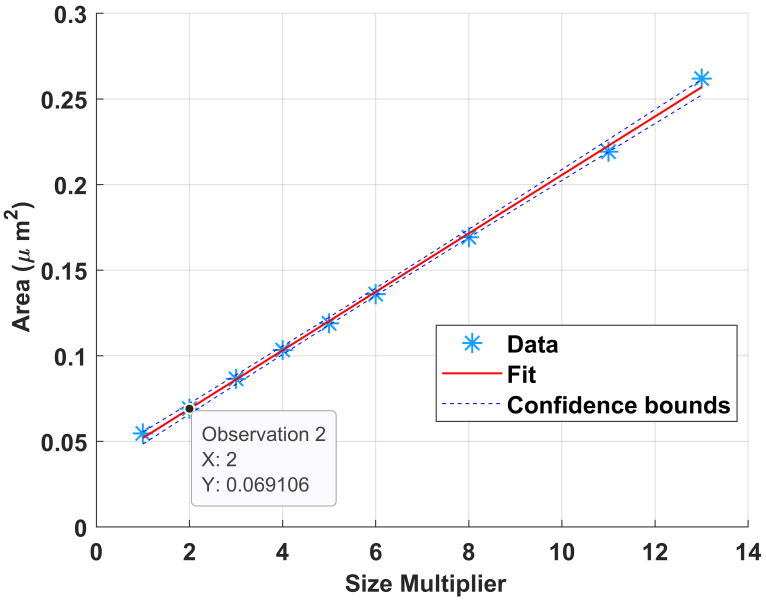

Fig. 6.12. Area vs Inverter Sizes With Linear Regression

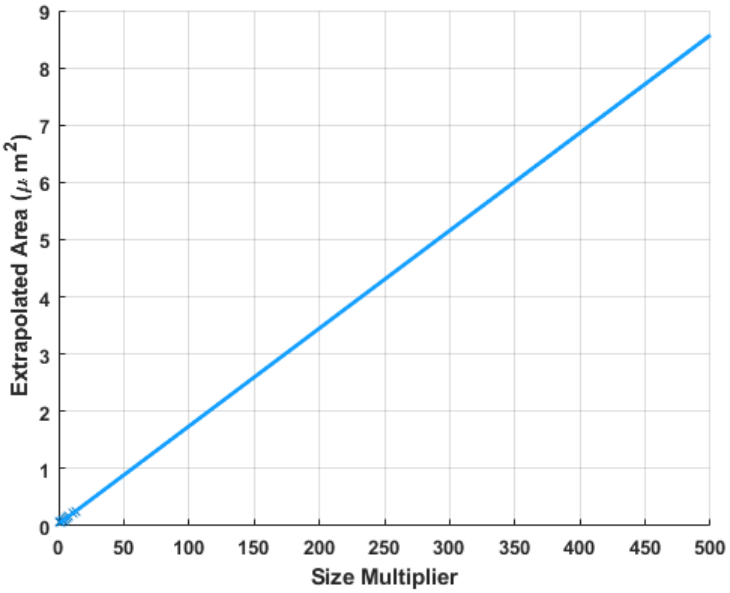

Fig. 6.13. Extrapolated Linear Regression from Figure 6.12

replicated, Figure 6.14 shows a potential configuration of the IC where Cout is 75pF and there are (40) 800fF which represent the pumping capacitors. This brings the estimated total area to $35,000\mu m^2$.

6.4 Minimum V_{DD} Required for Operation

To find the minimum V_{DD} that this system can operate at, the power supply was swept first by $10mV$ increments from $0mV$ to $150mV$ where a noticeable jump occurred between $90mV$ and $100mV$. Another sweep was then performed in increments of $2mV$ from $91mV$ to $99mV$ where the minimum power supply voltage is found to be a very competitive $93mV$. This is shown in Figure 6.15 where the more important simulations are solid lines to highlight the obvious switching point as well as those relative to the output with the $150mV$ V_{DD} being the design constraint. A value was only considered if the SS pumped voltage was larger than the V_{DD} supplied.

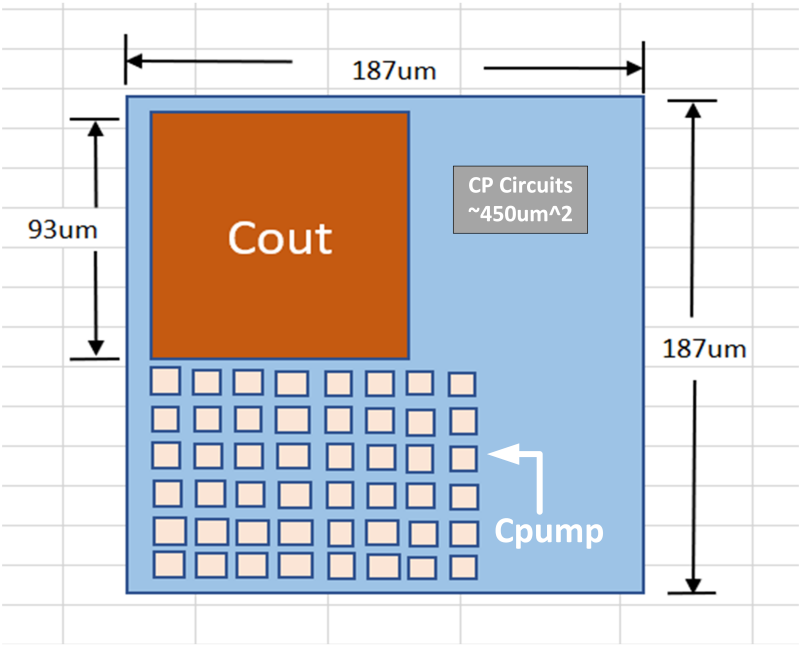

Fig. 6.14. Relative Scale Drawing of this Design

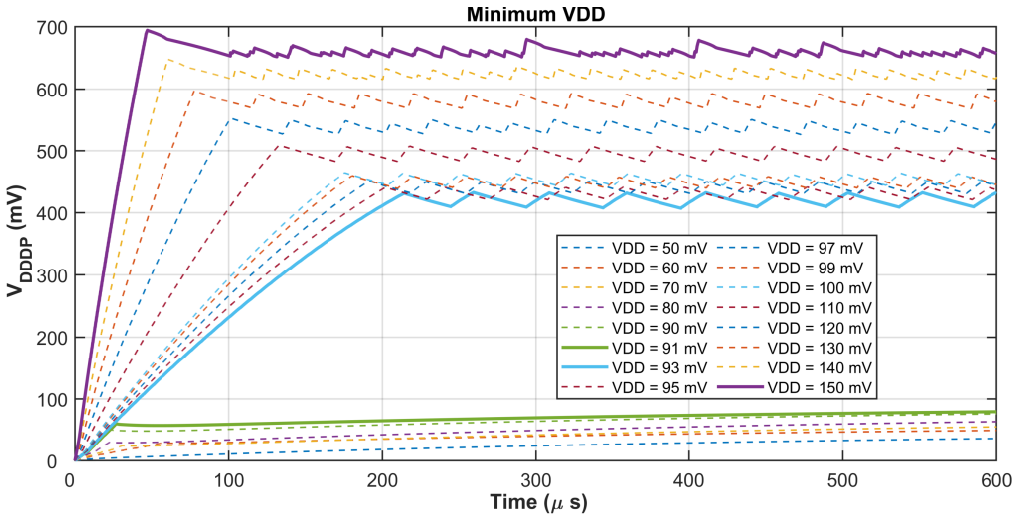

Fig. 6.15. Minimum V_{DD} Transient Simulation

6.5 Results

This section will discuss the simulation results obtained while also presenting a table that compares the results of this work to similar state of the art CPs. Figure 6.16

shows the transient response of V_{DDP} at different loading conditions. As mentioned before, I_L is turned off until $50\mu s$ to show the rise time and to show that even under zero loading conditions V_{DDP} does not cross $700mV$.

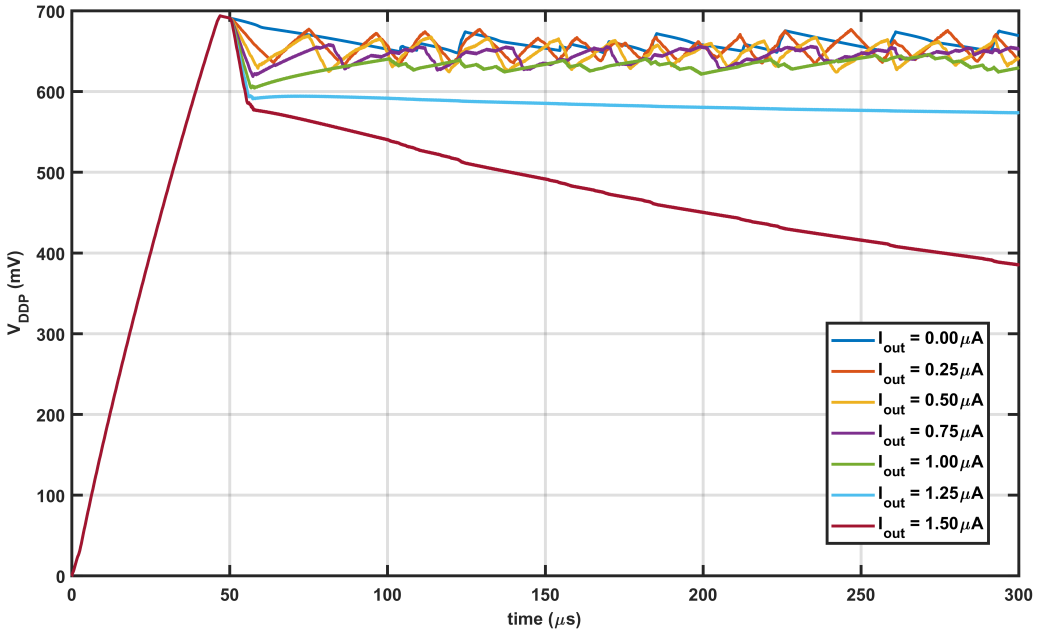

Fig. 6.16. VDDP Transient Response to Different Loading Conditions

The power consumed by each of the blocks in Figure 2.1 was calculated through simulation and is shown in Table 6.1. The information presented in Table 6.1 matches expectations as the Voltage Div block consumes almost negligible power, the pump cores consume the most power and the pump Drivers consume the second most as it has a majority of the larger devices in the design and each device is switching for almost the entirety of the simulation. A summary of the important parameters relating to this design is presented in Table 6.2. Table 6.3 compares the results from this work to other state of the art CPs that had similar characteristics. A large number of design metrics are reported to try and be as fair as possible when comparing this work to others. With examination, none of the CPs in this table are inherently better than the next. However, each provide desirable characteristics that another may not be restricted by. While this has been stated multiple times throughout this work, it

is important to note that the results presented in this are simulation only and could change based on completing the layout for this design. Some advantages of this work as compared to the others presented in Table 6.3, include the fastest rise time, no off-chip components, can provide $633mV$ at $1\mu A$ of load current while being able to function at the second smallest V_{DD} of $93mV$. Of the designs presented with no off-chip components, this work can handle 4 times the amount of load current as the next highest. Some of the disadvantages of this work include the largest output voltage ripple and the lowest efficiency of 31.76% where the next highest is 38.8%.

Table 6.1.
Power Consumption

System Block	**Avg Power Consumption**	% of Total
Clock	$0.45\mu W$	9.28
Pump Drivers	$1.73\mu W$	35.65
Pump Cores	$2.17\mu W$	44.73
Voltage Div	$0.0013\mu W$	.03
VDDP Sensing	$0.5\mu W$	10.31
Entire System	$4.85\mu W$	100

Table 6.2.
Important Charge Pump Parameters at $I_{out} = 1\mu A$

Parameter	**Entire Simulation**	**Steady State**
Minimum Input Voltage (mV)	93	93
Input Voltage (mV)	150	150
Avg Pumped Voltage (mV)	592	633
Average Pumped Current (μA)	1.05	1.07
Output Voltage Ripple (mV)	-	20
Rise Time (μs)	50	-
Clock Frequency (MHz)	2 or 4	2 or 4
Pump Core Efficiency (%)	28.75	31.76
System Efficiency (%)	12.86	14.12
Power Consumption (μW)	4.85	4.79
Number of Unit CP Stages	8	8
Total Stages (Including Startup)	32	32
Area Estimation (mm^2)	0.035	0.035

Table 6.3.
Comparison to State of the Art Charge Pumps

Ref	**[11]**	**[12]**	**[5]**	**[30]**	**[10]**	**This Work**
Year	2018	2015	2012	2018	2018	2020
No. of Stages	3	24	7	3	2	32
Aux. Circuit	L[a]	L[a]	-	C[a]	-	-
Technology	FinFET	CMOS	CMOS	CMOS	CMOS	FinFET
Process (nm)	18	130	130	65	180	7
Rise Time (μs)	250	10,000	1,000	117	33,000	50
Min V_{DD} (mV)	96	70	125	150	150	93
[d]V_{DD} (mV)	96	NR	200	190	390	150
Clock Freq (MHz)	19.96	0.04	0.36	15.2	0.077	4
Tot. Pump Cap. (pF)	0.9	46	112	22.5	21.6	25.6
Load Cap. (pF)	10	10,000	NR	30	NR	75
[d]**Load Current** (μA)	0.045	12	0.1	1.5	0.25	1
V_{out} (mV)	475	1250	610	870	850	633
V_{out} **Ripple** (mV)	0.12	NR	1.2	<1	NR	20
[d]**Output Power** (μW)	0.023	17	NR	6.6	.046	0.68
[d]**Tot. Power Dissipated** (μW)	0.03	NR	NR	NR	NR	4.85
Feedback Control	No	Yes	Yes	Yes	Yes	Yes
Area (mm^2)	-	0.6	0.15	0.032	0.1	0.035[c]
Fabricated	No	Yes	No[b]	Yes	Yes	No
Max η (%)	42.9	58	51	38.8	59.2	31.76

[a]Off Chip; [b]Layout Completed; [c]Estimation; [d]at Cited Efficiency; ^{NR}Not Reported

7. FUTURE WORK

As stated previously, this work was unable to include layout because the software was not readily available. One potential for future work is to proceed with the layout of this design and measure the results with parasitic extraction included in the design. Since this PDK is not connected with any foundries, the design will not be able to fabricated after the layout step. Some further investigation could be done to lower the minimum V_{DD} of $93mV$. While this CP does take advantage of high performance adiabatic clocking strategies, another option that could be considered is to boost the clock signal just before they hit the Pump Cores. Investigation into the BMR would be very beneficial to any low voltage or energy harvesting application. Further optimization of the clock frequency and output capacitance can be performed to reduce the ripple voltage seen at the output. This work has potential to be combined with a FinFET SRAM array and the necessary periphery circuits to contribute to low voltage memory applications for FinFET technology. Another potentially beneficial study could be to compare different emerging technologies, CMOS and FinFET on their relative performance with respect to low power charge pumps. This study would need to take proper steps to ensure that the technologies are given a fair comparison, as there are many variables that effect the performance of charge pumps.

8. SUMMARY

In this thesis, a low power FinFET charge pump for energy harvesting applications was presented and compared to multiple state of the art charge pumps. This work was simulated in Cadence Virtuoso where a $150mV$ supply voltage assumed to be taken from an energy harvester was converted to a $633mV$ pumped output voltage able to supply a wide range of current loads given that the clock frequency is controllable based on the pumped voltage level. Its minimum required supply voltage for operation is a very competitive $93mV$ as well as the fastest rise time of the compared designs at $50\mu s$. This system was designed for low voltage energy harvesting, however, with minor changes and optimizations, could be implemented in almost any low voltage design where a second on-chip power supply is needed. An area calculation was performed where this system was estimated to fit on a $35{,}000\mu m^2$ IC, although this result was an estimation based on reasonable assumptions, it was never tabbed as an advantage over other works because the layout was not performed. A power analysis was conducted to calculate the efficiency and to provide a numerical power analysis of the entire system as well as its major sub blocks. A wide variety of analog and digital circuits are presented throughout this thesis with the related waveforms to show validation of individual circuit and system level performance. The results of this thesis show that FinFET charge pumps are a viable solution for low power energy harvesting platforms and can replace a standard CMOS system based on the designers constraints.

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