VERTICAL TRIGATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR IN 4H - SILICON CARBIDE

A Dissertation

Submitted to the Faculty

of

Purdue University

by

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In Partial Fulfillment of the

Requirements for the Degree

of

Doctor of Philosophy

August 2020

Purdue University

West Lafayette, Indiana

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To Amma and Appa,

For you believe in me, I believe in myself...

ACKNOWLEDGMENTS

The journey to obtain this PhD has been a long and eventful one, the successful completion of which would not be possible without the involvement and support of many people. Hence, I would like to acknowledge several individuals each of whose contribution has made a significant impact in the culmination of this thesis.

First, I would like to thank Professor Dallas Morisette, for taking the chance with me as his first doctoral student, a gamble I hope this thesis justifies. The work that is represented here is only made possible because of the extraordinary support and exceptional guidance Prof. Dallas has provided. In addition to this, the opportunity to work on a number of very challenging and diverse problems has made for an intellectually stimulating and enjoyable PhD experience. I am also thankful to Prof Dallas for fostering and providing the resources to investigate some of the 'crazy' ideas I knocked on his door with. I will miss the countless hours spent in his office discussing out-of-the-box ideas and various aspects of solid-state physics.

I would also like to thank Professor James A. Cooper, Jr., for his outstanding technical guidance and valuable advice throughout this work. It has been an honor to work so closely with someone I so deeply admire and respect. The numerous insightful and thought-provoking discussions have not only added value to this project but also made me a better researcher. Thanks, are due to Professor Mark Lundstrom and Professor Scott Sudhoff for serving on my PhD committee and providing useful suggestions and inputs at critical junctures of this project.

I would like to thank Professor Michael Capano, Professor Sarit Dhar, Professor Len Feldman, Dr. Carl Johnson for the opportunity to collaborate on a number of interesting and challenging projects. I would like to express my gratitude to the staff members at the Birck Nanotechnology Centre, most notably Dan Hosler, Dave Lubelski, Kenny Schwartz, Bill Rowe, Jeremiah Shepard and Tim Miller for their

assistance and co-operation during the intensive lab work required for this project. My colleagues and fellow graduate students for the lively conversations, advice and for keeping me sane through the many all-nighters we spent in the lab. I would like to specially acknowledge two people, Naeem Islam for being an integral part of the work described in this thesis and Dr. Noah Opondo for his partnership in implementing innovative solutions to numerous difficult problems. I have been fortunate to make many good friends and I thank them for making my life at Purdue a wonderful experience.

This achievement was made possible by the everlasting support and guidance by my parents, Medha Ramamurthy and P.B Ramamurthy. My sister Ashwini and brother-in-law Vikram for their constant encouragement. Finally, and most importantly, a special tribute goes out to my beautiful wife and soul mate, Krishnakali Chaudhuri who I was fortunate to meet along this journey. It has been your encouragement, support and endless patience through the vicissitudes of graduate life that has made this dream a reality.

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ABSTRACT

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Advances in modern technology and recent demand for high power applications have motivated great interest in power electronics. Power semiconductor devices are key components that have enabled significant advances in power electronic systems. Historically, silicon has been the material of choice for power semiconductor devices such as diodes, transistors and thyristors. However, silicon devices are now reaching their fundamental limits, and a transition to wide bandgap semiconductors is critical to make further progress in the field. Among them, SiC has attracted increasing attention as a power semiconductor to replace silicon due to its superior properties and technological maturity. In fact, SiC power MOSFETs have been commercially available since 2011, and are actively replacing their silicon counterparts at blocking voltages above 1 kV. At these voltages, the specific on-resistance of SiC MOSFETs is 200-300x lower than that of silicon devices. However, conventional vertical SiC MOSFETs are still far from their theoretical performance at blocking voltages below 2 kV. In this regime, the channel resistance is the dominant limitation due to the relatively low channel mobility at the SiO_2/4H-SiC MOS interface.

In this thesis, the first successful demonstration of a novel power device in 4H-SiC called the trigate power DMOSFET (double diffused metal oxide semiconductor field effect transistor) is presented. This device is inspired by the FinFET concept, and reduces the channel resistance by a factor of 3-5$\times$ compared with the state-of-art commercial power DMOSFETs, without requiring an increase in the channel mobility. The trigate structure is applied to a power MOSFET for the first time

along with a self-aligned short channel process. This new structure utilizes both the conventional horizontal surface as well as the sidewalls of a trench to increase the effective width of the channel without increasing the device area. Conceptual design, optimization, process development and electrical results are presented. The trigate power MOSFET with a trench depth of $1\mu m$ designed for a blocking voltage of 650 V has a specific on-resistance of 1.98 mΩ cm^2 and a channel resistance of 0.67 mΩ cm^2. This corresponds to a $\sim 2\times$ reduction in the total specific on-resistance, and a $3.3\times$ reduction in the specific channel resistance as compared to a conventional DMOSFET with the same blocking voltage rating. This demonstration is a landmark that could help SiC technology compete successfully in the lower blocking voltage regime below 600 V, and access for the first time a completely new segment in the power electronics application space.

1. INTRODUCTION

Semiconductor materials and devices have been at the center of the modern technology revolution. Rapid development, large scale integration and an ever increasing appetite for new applications have challenged the fundamental limits of semiconductors in a variety of fields [1–3]. Power electronics is one such field where progress has mainly been limited by the performance of semiconductor devices. Silicon (Si), which is the dominant semiconductor for power electronics, has not been able to meet the stringent requirements of modern applications [4]. Silicon carbide (SiC), a compound wide-bandgap semiconductor, stands out as the most promising alternative, and recently SiC devices are beginning to replace silicon parts [5]. However, even within its theoretical limits SiC devices have some critical shortcomings. To overcome these limitations, my project will develop a device based on the Fin-FET or tri-gate concept, which is applied to vertical power devices for the first time.

This thesis has been organized into eight chapters. A brief introduction to power electronics, current status and prospects of SiC power devices is described in this chapter. In chapter 2, an introduction to SiC MOSFETs, their architecture, operational limits and the need for new innovation is also put forward. The concept, design and optimization of a trigate MOSFET that significantly improves performance over conventional devices through structural design will be presented in chapter 3. The design of a mask layout to fabricate the proposed trigate MOSFET is also described. The process development and fabrication steps required to realize these trigate devices are presented in chapter 4. Electrical measurements and an analysis of the trigate MOSFET characteristics, along with data from other test structures is discussed in chapter 5. A proposal for future work that is needed to further improve the performance and manufacturability of the trigate MOSFET is presented in chap-

ter 6. Conclusions drawn from the present work and the major results obtained are summarized in chapter 7.

1.1 Power Semiconductor Device

Power electronics involve the conversion of electric power by the use of power semiconductor devices and circuits [6]. For instance, household appliances use *adapters* that convert from AC to DC while *power inverters* convert from DC to AC voltage. Silicon (Si) has long been the dominant semiconductor of choice for high-voltage power electronics applications [7], and Si devices are widely used by power electronics and power systems [8–10]. But these devices are now approaching performance limits imposed by the fundamental material properties and the increased cost of cooling and integration [11–13]. To make further progress and meet the increasing demands on power electronic technology and applications, the need to migrate to a more optimal semiconductor material has become imperative.

Semiconductor devices based on wide-bandgap materials such as silicon carbide, gallium nitride (GaN), diamond, and gallium oxide ($\beta - Ga_2O_3$) offer multiple advantages over Si-based power electronic devices [14–16]. They possess superior physical and electrical properties that can serve as the basis for the high-voltage, low-loss power electronics of the future. Power devices are generally rated using two key parameters: blocking voltage (V_B) and specific on-resistance ($R_{ON,SP}$).

Blocking Voltage

The blocking voltage is the maximum voltage that can be applied to the device above which the device starts to conduct in the off-state and may result in failure. This is usually determined by avalanche breakdown, but could also be limited by the maximum permissible oxide field in the case of MOSFETs (metal oxide semiconductor field effect transistors). Power devices typically support the off-state terminal voltage with a reverse-biased P-N junction. A reverse biased one-sided step junction for two

different materials is shown in Figure 1.1. Here the Schottky metal acts like a heavily doped P-type region, and a space-charge (depletion) region and built-in potential exist at this junction in equilibrium. Since the metal has very high conductivity, and all the induced charge resides at the metal/semiconductor interface, the depletion region can be assumed to exist only in the lightly and uniformly doped N-type region. Under reverse bias, the applied voltage increases the electrostatic potential across the depletion region, expanding the depletion width. The electric field profile can be estimated using Guass's law to be:

$$\frac{dE}{dx} = \frac{\rho}{\epsilon_s} \tag{1.1}$$

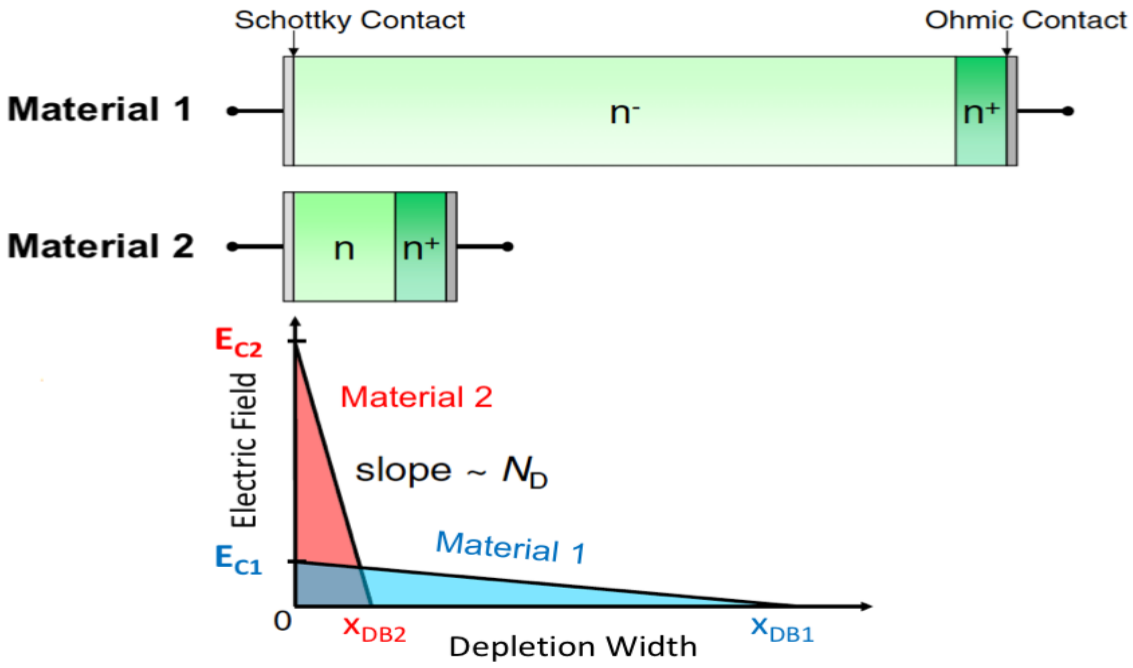


Figure 1.1.: Schottky diode in two material systems for the same blocking voltage and the electric field profile in reverse bias. Material 2 has a higher bandgap and critical electric field as compared to material 1.

Integrating this equation gives us the electric field distribution with respect to distance in the N-region:

$$E(x) = \frac{qN_D}{\epsilon_s}(x - x_d). \tag{1.2}$$

Here N_D is the doping concentration, ϵ is the di-electric constant of the semiconductor and x_d is the depletion width. Clearly, the magnitude of the maximum electric field ($|E_{max}|$) occurs at the metal-semiconductor interface (x = 0). E_{max} is given by:

$$E_{max} = -\frac{qN_D}{\epsilon_s}x_{db}. \tag{1.3}$$

Where x_{db} is the maximum depletion width corresponding to the blocking voltage(V_B). As a power device is designed to block the certain terminal voltage in the off-state, $N_D \times x_{db}$ in (1.3) is designed such that E_{max} equals the critical electric field (E_C). The critical electric field is the limiting field at which carriers in the semiconductor acquire sufficient energy to cause avalanche breakdown through impact ionization [17].

The electrostatic potential is defined as $\Psi = -\nabla V$, and when the blocking voltage (V_B) is much larger than the built-in voltage, it can be expressed in one-dimension as -

$$V_B = \int dV = -\frac{qN_D}{\epsilon_s}\int_0^{x_{db}}(x - x_{db})\,dx \tag{1.4}$$

$$V_B = \frac{qN_D}{2\epsilon_s}x_{db}^2 \tag{1.5}$$

Now, using Equation 1.3,

$$V_B = \frac{1}{2}E_C x_{db} \tag{1.6}$$

The expression for blocking voltage in Equation 1.6 is equivalent to that of the area under the triangle as seen in Figure 1.1. Thus for any given blocking voltage, the areas under the 'red' and 'blue' regions are equal. It can clearly be seen that, by virtue of its higher critical electric field, a thinner and more heavily doped layer of material 2 can be used to achieve the same blocking voltage.

To compare the blocking voltage between two materials, it is convenient to express Equation 1.6 in terms of material parameters. To do this, the depletion width, x_{db}, under blocking voltage V_B, can be expressed by rearranging Equation 1.3 as:

$$x_{db} = \sqrt{\frac{2\epsilon_s V_B}{qN_D}} \tag{1.7}$$

Using this expression for x_{db} in Equation 1.5, the blocking voltage can be expressed in terms of the material parameters as:

$$V_B = \frac{\epsilon_S E_C^2}{2qN_D} \tag{1.8}$$

This equation indicates that the blocking voltage of a P+/N junction of a given doping is proportional to the square of the critical field. Thus the critical electrical field is an extremely important material parameter for power devices.

Specific On-Resistance

The specific on resistance is another important parameter in the design of power devices. It is defined as the product of the resistance of the device in the 'on' state and die area:

$$R_{ON,SP}(\Omega\,\mathrm{cm}^2) = R_{ON}(\Omega) \times A_{DIE}(\mathrm{cm}^2) \tag{1.9}$$

In the case of a uniformly doped n-type semiconductor material, the specific on-resistance can be written as [17]:

$$R_{ON,SP} = \rho \cdot t = \frac{t}{q\mu_N N_D} \tag{1.10}$$

where μ_N is the electron mobility, t is the thickness of the material, and full dopant ionization has been assumed. In the case of a non-punch-through design, the depletion region x_{db} extends to the thickness t of the lightly doped region at the rated blocking voltage V_B. In order to express $R_{ON,SP}$ in terms of material parameters, (1.7) for x_{db}, and N_D from (1.5) are substituted into (1.10), to obtain:

$$R_{ON,SP} = \frac{4V_B^2}{\mu_N \epsilon_S E_C^3} \tag{1.11}$$

Table 1.1.: Physical properties of important power semiconductors [12, 18–20].

Material	E_g (eV)	n_i (cm^{-3})	ϵ_r	μ_n (cm^2/Vs)	E_c (MV/cm)	v_{sat} (10^7 cm/s)	λ (W/cmK)
Si	1.12	1.5×10^{10}	11.8	1350	0.3	1.0	1.5
GaAs	1.42	1.8×10^{6}	12.8	8500	0.4	2.0	0.5
GaP	1.12	1.5×10^{10}	11.8	1350	0.3	1.0	1.5
GaN	3.39	1.9×10^{-10}	9.0	900	3.3^d	2.7	1.3
3C-SiC	2.37	1×10^{-1}	9.6	900	1.2^d	2.0	3.3
4H-SiC	3.25	8.2×10^{-9}	10	$800^a, 1050^c$	2.0^d	2.2	3.3
6H-SiC	3.0	2.3×10^{-6}	9.7	$375^a, 100^c$	2.4^d	1.9	3.3
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0	13
AlN	6.2	1.0×10^{-31}	8.7	1100	11.7	1.8	2.5

^{a} mobility along a-axis, ^{c} mobility along c-axis, ^{d} E_C at doping of $1\times\ 10^{15}cm^{-3}$

Optimized power devices use a punch-through design as described in Section 2.2.2.1. Equations (1.6) and (1.11) establish the strong impact the critical electric field and carrier mobility parameters have on the performance of power devices. These are inherent material properties, and thus are critical to the choice of the right power semiconductor material.

Table 1.1 lists the common semiconductors used for high-voltage power devices, along with some of their important physical properties. Silicon has a relatively low critical electric field and thus Si power devices are bulky at high blocking voltages. This has lead to a push towards wide bandgap materials like gallium nitride (GaN) and silicon carbide (SiC). SiC currently presents the best alternative and the structure, properties and attributes that make it so attractive are discussed below.

1.2 Silicon Carbide

Silicon carbide (SiC) is a IV-IV compound material with a stoichiometry of equal parts silicon (Si) and carbon (C). The first synthesis of SiC was published nearly 200 years ago by J. J. Berzelius in 1824 [21]. Shortly after, E. G. Acheson discovered and patented a process to manufacture SiC crystals, which he named carborundum [22]. In fact, this was the very material which started the LED (light emitting diode) revolution [23,24]. The synthesized material, carborundum, contained a large number of defects which helped demonstrate the phenomena of electroluminescence and the LED for the first time [25].

The road to obtain defect free, high quality SiC crystals was an arduous one. In the words of William Shockley, "The SiC situation suffers from the very same thing that makes it good." [26] The strong chemical bonding between Si and C atoms gives this material its interesting and unique properties. However it also creates severe complications for crystal growth. It took a series of breakthroughs by Lely [27] and researchers Tairov and Tsvetkov [28, 29] nearly a century after its first synthesis to grow high quality SiC crystals. The sublimation and physical vapor transport (PVT) technique was used to grow SiC crystals at 2000-2800°C [30]. Around the same time, Matsunami *et al.* introduced a CVD technique for a high quality SiC epitaxy process called "step-controlled epitaxy" [31]. These advances in material growth technology combined with extremely low defect densities have made SiC-based technology commercially viable.

Back in 1893, B. W. Frazier discovered that the SiC crystals had different crystal symmetries or polytypes [32]. These polytypes are differentiated by the stacking sequence of the bi-atom layers of the SiC structure. While there are over 170 known polytypes, the most common are the cubic 3C, and the hexagonal 4H and 6H structures. 4H-SiC is the most common polytype of SiC for electronic purposes, mainly because of higher bulk electron and hole mobility and lower mobility anisotropy along different crystallographic directions [30].

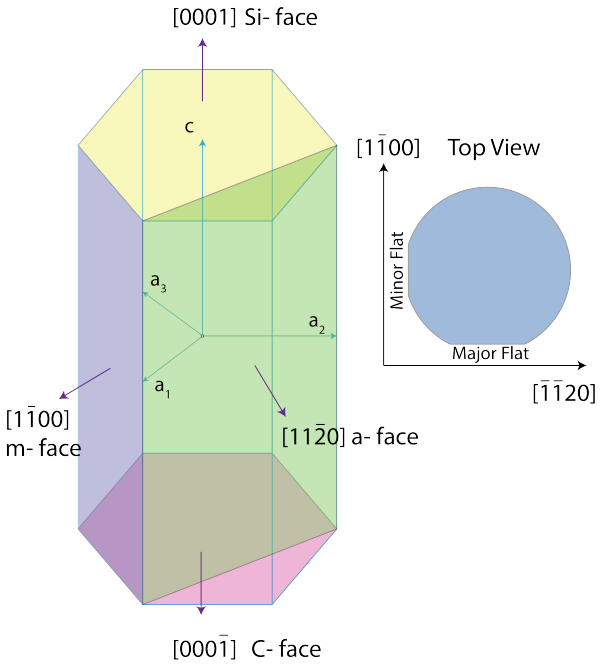


Figure 1.2.: Hexagonal unit cell in 4H-SiC with important faces highlighted. Typical SiC wafer orientation is also shown

4H-SiC is a hexagonal closely packed structure that consists of an equal number of cubic and hexagonal bonds with a stacking sequences of ABCB [33]. The important faces of the 4H-SiC hexagonal structure are shown in Figure 1.2. The usual wafer orientation of (0001) or Si-face is also shown in the figure.

Changing of the stacking sequence has a profound effect on the electrical properties of SiC. For example the bandgap varies between 2.36–3.8 eV, depending on the polytype [34,35]. 4H-SiC exhibits a bandgap of 3.26 eV, and has a saturation velocity at room temperature of 2×10^7 cm/s [36], which is almost twice that of Si. This property is very attractive for high frequency electronic applications. In addition, its high thermal conductivity of 3.3 W/cmK enhances heat dissipation and enables high power densities while maintaining an acceptable junction temperature. In addition, the wide bandgap energy allows for power efficient high temperature operation [37].

The critical electric field also varies with polytype as seen in Table 1.1. Moreover, since the carrier acceleration and scattering are strongly influenced by the energy

band structure, the critical field depends on the crystallographic orientation. Accurate values of the critical electric field can thus only be obtained numerically by solving the ionization integral for each specific case. However, good approximates can be obtained empirically. For a simple planar structure with a constant doping structure, the critical electric field of SiC and Si at room temperature can be approximated by the following expressions and are plotted in Figure 1.3 [38].

$$E_{CR.SiC} = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log_{10}(N/10^{16})} \tag{1.12}$$

$$E_{CR.Si} = \frac{4 \times 10^5}{1 - \frac{1}{3}\log_{10}(N/10^{16})} \tag{1.13}$$

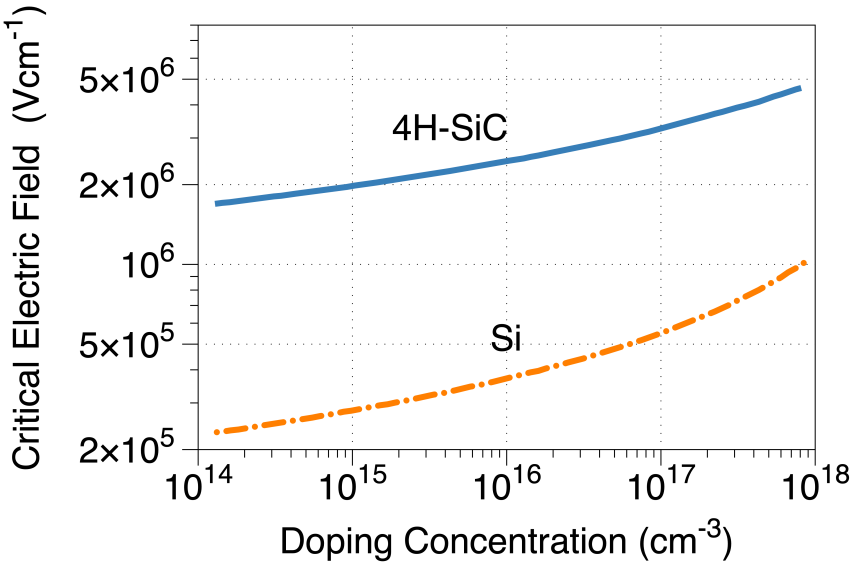


Figure 1.3.: Critical electric field of SiC and Si as a function of doping

First, it can be easily seen from this figure that the critical electric field of SiC is higher than that of Si for all doping concentrations. It is up to 7 times higher for light doping, and about 5 times higher for heavier doping. The higher critical field of SiC directly provides an advantage in achieving high blocking voltages.

In the case of power devices, to obtain a certain blocking voltage, SiC can be doped much more heavily than Si, and the drift region can be made much thinner, resulting in significantly reduced on-resistance. SiC can be thought of as material 2 in Figure 1.1, and Si as material 1.

A doping dependence in the critical field is also evident from Figure 1.3. At higher doping concentration, the increased charge density causes the electric field to decrease faster with distance. Thus a higher peak field is required to cause significant ionization and bring the ionization integral equal to one [30]. Another secondary effect is that of the carrier mobility. The higher critical field of SiC compared with Si at all doping concentrations has a significant impact in the design of power devices. For example, at a doping of $1 \times 10^{14}\text{cm}^{-3}$, the 7× higher critical electric field in SiC contributes a factor of about 250× in lowering the on-resistance in SiC as compared to Si for the same blocking voltage.

1.3 Current Status of SiC Technology

1.3.1 Material Growth

Innovation in material growth techniques and significant improvements in the quality of crystalline SiC growth have taken place in the last two decades [39]. This makes silicon carbide (SiC) technology by far the most mature among the other wide band gap alternatives. Today, high-quality SiC wafers are commercially available

Table 1.2.: Major extended defects in SiC epitaxial layers.

Extended Defects in SiC	Typical Density (cm^{-2})
Micropipe	0-0.02
Threading Screw Dislocation (TSD)	300-1000
Threading Edge Dislocation (TED)	2000-5000
Basal Plane Dislocation (BPD)	0.1-10
inclusions (downfall, triangular-3C defects) and stacking faults (SFs)	0.1-1

up to 150 mm in diameter [40]. In fact, 150 mm wafers have become the industry standard, and 200 mm wafers have already been demonstrated [41, 42].

However, SiC is not entirely defect free, and wafers employed for device fabrication contain a variety of crystal imperfections, both extended and point defects. Additional defects are generated during device processing steps such as ion implantation and dry etching [43]. Though the total defect density is very low, the impact on long term reliability and performance is still being studied [44–46].

In terms of extended defects, micropipes have been identified as the most critical killer defect for power devices [47]. A micropipe is a micron-size pinhole extending along the <0001>direction through the entire SiC wafer. Currently availabile material has a very low density of micropipes ($< 0.1\text{cm}^{-2}$ - see Table 1.2). Extensive studies have been conducted aimed at reducing other extended defects such as threading screw and edge dislocations (TSD, TED) which are common in compound semiconductors [48]. Through innovative techniques such as the repeated a–face growth (RAF) method [49], total dislocation density of commercial wafers is also low (Table 1.2). However work on further reduction is being done to improve long term reliability and increase yield.

Point defects such as carbon vacancies are another important type of defect in SiC epitaxial layers, and are known to create deep level traps within the bandgap. This is particularly harmful for bipolar devices such as BJTs and IGBTs (Figure 1.4), where the lifetime of the injected minority carriers is greatly impacted. Several techniques to quench such point defects have been demonstrated, and research in this field is ongoing to obtain improved results [50–52].

1.3.2 Power Devices

The first solid-state detector was a point contact diode made of SiC, and was used to receive radio signals in 1906 [53]. This device was characterized to have "unilateral conductivity" as it showed typical diode behavior. Further progress in

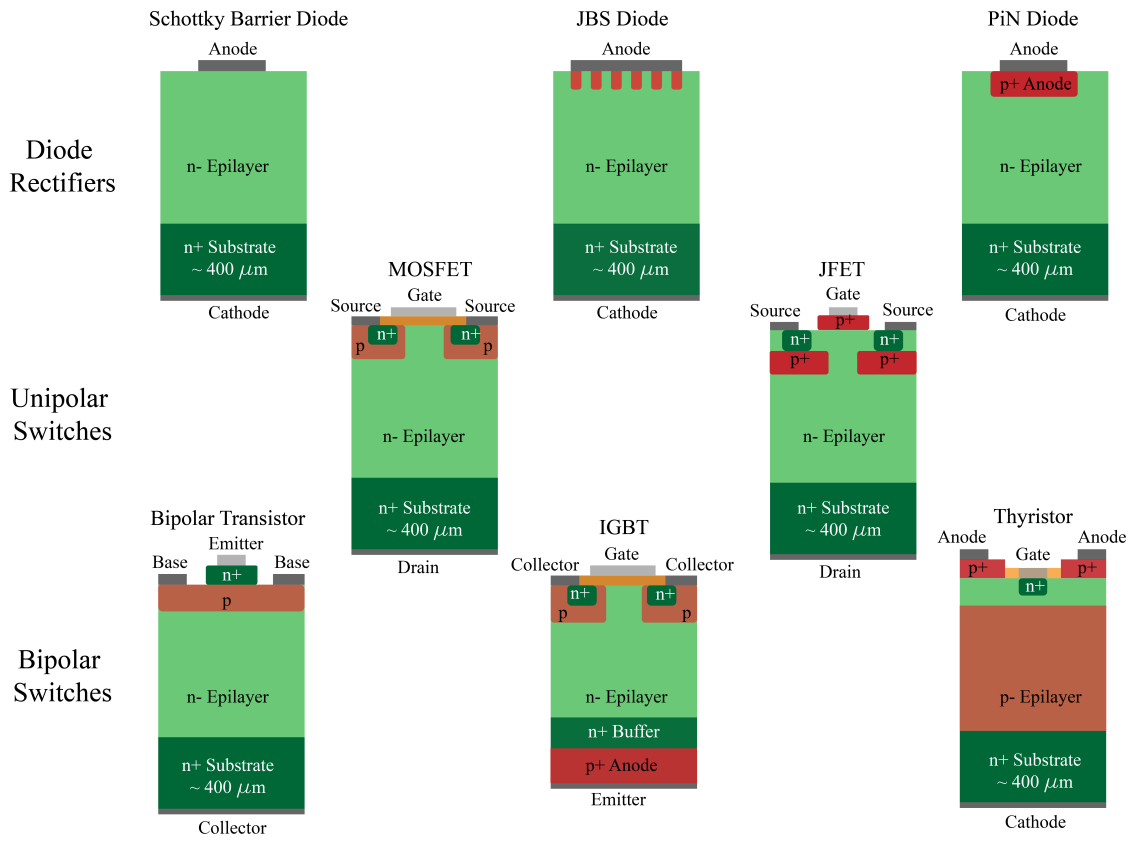


Figure 1.4.: Schematic structures of various SiC power devices currently developed

SiC power devices was only possible with the advancement in material growth in the early 1990s. Since then there has been significant work on a host of SiC power devices including bipolar devices such as P-N junction diodes [54], bipolar junction transistors (BJTs) [55]), insulated gate bipolar transistor(IGBT), gate turn-off thyristor(GTO), schottky barrier diodes [56,57] as well as unipolar MOSFET devices as seen in Figure 1.4.

SiC power devices can be classfied in terms of their applications in three broad categories - high (>6.5kV), medium (1.2kV-6.5kV) and low voltage (<1.2kV). In the high voltage regime, the performance of the device is limited by the thickness of the drift layer (Equation 1.7), and it is more efficient to use bipolar devices such as BJTs or IGBTs. Conductivity modulation can be achieved in these devices by injecting

minority carriers into the drift region, thereby reducing its resistivity in the on-state. However, this charge needs to be removed during the turn-off transient, and a penalty is paid in terms of higher switching losses.

Unipolar devices, especially 4H-SiC MOSFETs, are very popular in the medium voltage regime and have been widely adopted in the industry. The first planar channel SiC MOSFETs (DMOSFETs) were built here at Purdue University [58]. SiC MOSFET technology has seen a great deal of work, leading to improvements in device characteristics, gate oxide reliability, body diode reliability and avalanche ruggedness, with eventual commercialization in 2011 [5]. Various aspects of SiC power MOSFETs, state-of-the-art device design, and current challenges are the topics of the next chapter.

The low voltage regime presents a unique problem for SiC technology today. There exists a large industry segment and a wide variety of applications in the low voltage regime where adoption of SiC technology has been limited. While its theoretical performance (Equation. 1.6) is significantly better than Si in this regime, the performance of SiC MOSFETs is limited by channel resistance. A unique solution to this problem and a proposal of an innovative new SiC power MOSFET is put forward in the forthcoming chapters.

2. POWER MOSFETs - THE SiC WORKHORSE

Unipolar SiC devices have become very popular and widely adopted in the power electronics industry today [59]. This is mainly due to the fact that the drift-layer resistance in unipolar devices can be reduced by at least 2-3 orders of magnitude at any given blocking voltage by utilizing SiC instead of Si. Among the unipolar devices, SiC MOSFETs now constitute the fastest-growing segment of the SiC market [60].

Power MOSFETs in SiC offer several advantages over other materials such as GaN, and other device technologies such as Si superjunctions. With steady progress in process technology, SiC power MOSFETs entered commercial production in 2011 and are available at blocking voltages from 650V - 3300 V [40, 61]. However there are some key issues that limit the performance of SiC MOSFETs. This chapter describes the design features of SiC power MOSFETs, the basis of their limitations, and the need for innovation to overcome them. To do this, the figure of merit most often used to evaluate the performance of power MOSFETs is introduced, and design considerations to optimize performance are discussed.

2.1 Evolution

From a semiconductor point of view, SiC first excited interest in the late fifties as an alternative to germanium (Ge) for high temperature applications [62]. However it was not until the early 1990's that the potential of SiC for power devices was explored in much detail. The availability of good quality material combined with a good theoretical understanding [63, 64] and the extensive knowledge base from the established silicon technology [65] led to accelerated development of SiC devices.

Taking lead from the Si counterpart, a vertical trench MOSFET in 6H-SiC was demonstrated by Palmour *et al*. [66]. The first planar double-implanted metal-oxide-

semiconductor field effect transistor (DMOSFET) in SiC with a blocking voltage of 760V and low on-resistance was reported by Purdue University in 1996 [67]. Shortly after, an accumulation channel MOSFET or ACCUFET was also demonstrated [68]. Trench MOSFETs, also called UMOSFETs due to the shape of the gate trench, were initially more popular [69, 70]. After steady improvement of the MOS channel mobility, oxide reliability and other system integration factors. Planar 4H-SiC power MOSFETs have been commercially available since 2011. [40].

2.2 Design of Power MOSFETs

SiC MOSFETs are primarily used as power switching devices, and are designed to emulate an ideal switch. The goal is to carry a high current in the on-state with low energy loss, block a high voltage with zero leakage current in the off-state and switch between these two states with the least time and energy loss. The degree to which a power semiconductor device is able to achieve these goals is indicated by its performance specifications, of which the most important are blocking voltage, maximum on-state current, and on-state, off-state and switching power dissipation. Since maximizing performance involves trade-offs between parameters, figures of merit (FOMs) need to be defined that quantify the extent to which actual devices approach the theoretical limits. The figure of merit for unipolar devices is discussed in next subsection.

2.2.1 Unipolar Figure of Merit

A schematic of the current–voltage characteristics of a switching device is shown in Figure 2.1, where the ideal and real characteristics are compared. In the ideal case, the on current I_{on} and the blocking voltage V_B are achieved at zero power loss. A common FOM for a power switch is the product of these two parameters.

$$FOM = I_{ON} \times V_B \tag{2.1}$$

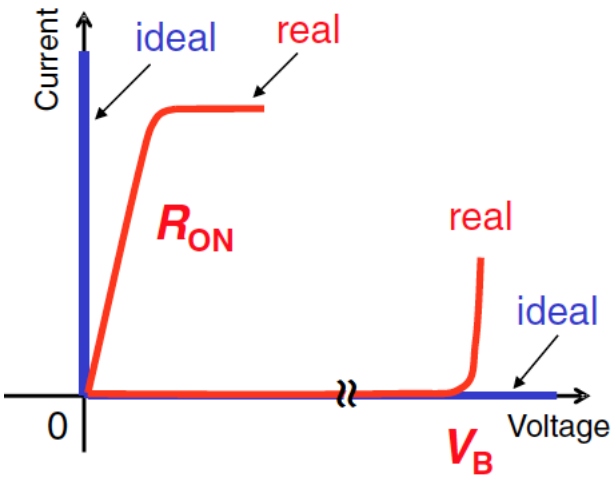


Figure 2.1.: Current−voltage characteristics of power switch

The maximum current through a power device in the on-state needs to be limited in order to maintain an allowable junction temperature, and is practically determined by the heat transfer capability of the package. For a unipolar device, the on-state power dissipation per unit area within the device can be written as -

$$P_{MAX} = J_{ON}^2 \times R_{on,sp} \tag{2.2}$$

where J_{ON} is the current density and $R_{on,sp}$ is the specific on-resistance. The maximum J_{ON} is given by:

$$J_{ON} = \sqrt{\frac{P_{MAX}}{R_{on,sp}}} \tag{2.3}$$

Inserting this expression into (2.1) and noting that $I_{ON} = \mathrm{A} \times J_{ON}$, the FOM for SiC MOSFETs can be defined as:

$$FOM = A \times \sqrt{P_{MAX}\left(\frac{V_B^2}{R_{on,sp}}\right)} \tag{2.4}$$

The factor, $V_B^2/R_{on,sp}$ represents the unipolar device FOM, and SiC MOSFETs are designed such that this ratio is maximized. Rearranging the equation for the specific

on-resistance of a unipolar device with a non-punch-through design (Equation 1.11), we arrive at the following equation for the FOM:

$$\frac{V_B^2}{R_{on,sp}} = \frac{1}{4}\mu_N \epsilon_s E_C^3 \tag{2.5}$$

Interestingly, the maximum theoretical FOM is entirely defined by material properties. Real devices can only tend to this theoretical limit, and comparing the actual measured $V_B^2/R_{on,sp}$ to the theoretical limit is a useful indication of design and process optimization.

2.2.2 SiC Power MOSFETs

State of the art SiC MOSFETs are comprised mainly of two structural designs- 1) Double Implanted (DMOSFET) and 2) Trench Gate MOSFET (UMOSFET). The difference between the two is the directionality of the channel formed by the base region near the interface underneath the gate electrode. In the DMOSFET, the channel is parallel to the surface of the wafer, while the UMOSFET has a vertical channel along the sidewall of the trench perpendicular to the wafer surface as seen in Figure 2.2(b).

The design of both of these MOSFETs are somewhat different due to the device geometry, but the basic methodology remains the same. To illustrate this, consider the SiC DMOSFET device as seen in Figure 2.2(a). As described earlier, the device FOM is given by the ratio of $V_B^2/R_{on,sp}$ in (2.4). The blocking voltage V_B is determined by the desired rating of the device, and thus $R_{on,sp}$ is the parameter that must be minimized in the design of a power MOSFET.

The resistance components and some critical dimensions of a SiC DMOSFET are illustrated in Figure 2.3: t_J, t_D and t_{SUB} are the thickness of the JFET, drift and substrate layers respectively, while S and L_J are the cell pitch and JFET width of a given unit cell. The current spreading layer or CSL efficiently spreads the current exiting the JFET region over the whole area of the drift region. Also, the higher doping of the JFET region prevents pinch-off between adjacent base regions.

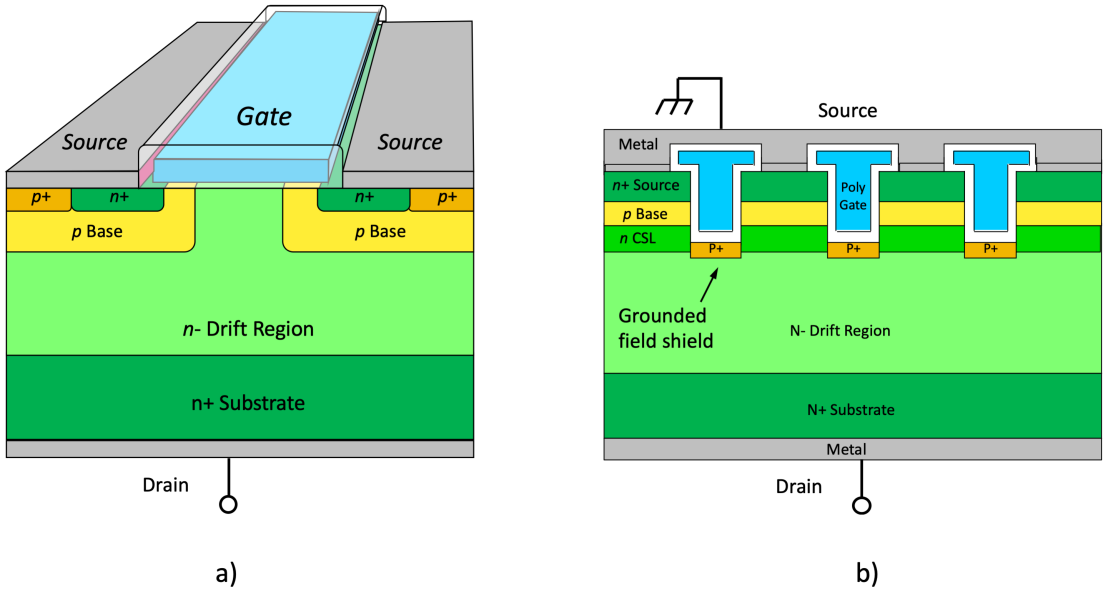


Figure 2.2.: Two different types of SiC MOSFETs: (a) DMOSFET and (b) UMOSFET

2.2.2.1 Components of total on-state resistance

In the on-state, current flows between source and drain. The primary resistance components in this current path are shown in Figure 2.3. These are source contact and implant (R_{SOURCE}), channel (R_{CHAN}), JFET (R_{JFET}), drift (R_{DRIFT}) and substrate (R_{SUB}). The total resistance of the device can be written as -

$$R_{ON}[\Omega] = R_{CONTACT} + R_{SOURCE} + R_{CHAN} + R_{JFET} + R_{DRIFT} + R_{SUB} \tag{2.6}$$

Assuming the width of the device to be W, the specific on-resistance is -

$$R_{ON.SP}[\Omega\text{cm}^2] = R_{ON} \times (SW) \tag{2.7}$$

The resistances are in series as seen in the equation above and discussed in detail below.

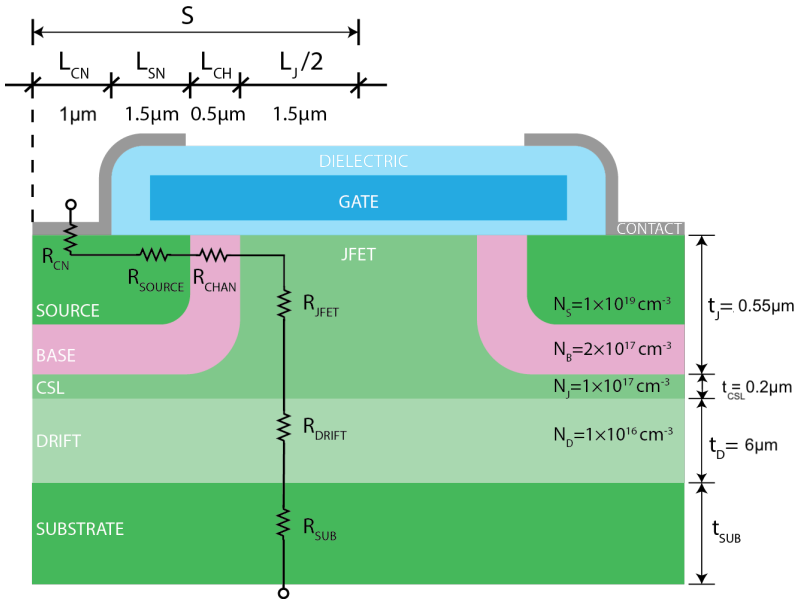


Figure 2.3.: Resistance components of DMOSFET device

Contact Resistance

For a power device, a good ohmic contact is important in order to deliver the rated current with a voltage drop that is insignificant compared to the drop across the active region. In order to form low-resistivity ohmic contacts on 4H-SiC, a high temperature silidication process (Ni_2Si) is normally used. The dominant current transport in these contacts is thermionic field emission. Thus the doping concentration should be made as high as practical, e.g. $1 \times 10^{19}\text{cm}^{-3}$ in order to produce a thin barrier and a high tunneling probability density. Metals which form a silicide, such as nickel (Ni) and titanium (Ti), are typically used to make ohmic contact. Study has shown that 100-200 nm thick Ni is sufficient for making reliable contact with n-type SiC [71]. Low contact resistivity is achieved by sintering the deposited Ni contact at 1,000°C for 2 min by rapid thermal processing (RTP) [30]. During this RTP process, Ni reacts with the SiC surface to form nickel silicide (Ni_2Si) reducing barrier height, and excess carbon accumulates near the surface. This process reduces contact resistivity to as low as $1 \times 10^{-6}\ \Omega\,\text{cm}^2$ and the corresponding contact specific resistance for a typical

DMOSFET with a cell pitch of 3 µm and a contact width of 1 µm to 3.5×10^{-3} m$\Omega\,$cm^3. This contributes less than 1% of the total resistance of a typical DMOSFET, and thus can often be neglected when calculating the total specific on-resistance.

In terms of design, as long as the dimensions of the contact are greater than the transfer length, the low contact resisitivity allows the contact area at the source contact to be made small, thereby shrinking the cell pitch and reducing $R_{on,sp}$. The design constraints are more relaxed at the drain contact due to the large contact area.

Source Resistance

During the on-state, electrons are injected from metal source contact, then flow through the source region to the channel. This source region, depending on the implant concentration, exhibits a finite resistivity. The specific on-resistance due to source region alone can be expressed as -

$$\begin{aligned} R_{S.SP} &= \left(\rho_S \frac{L_{SN}}{W \times t_{src}}\right)\ (SW) \\ &= \rho_S\ \frac{L_{SN}}{t_{src}}\ S \end{aligned} \tag{2.8}$$

where L_{SN} is the total length of the gate to source contact gap and the gate source overlap regions,t_{src} is the thickness of the source region and ρ_S is the resistivity of the source. With a typical source doping of 2 $\times10^{19}$ cm^{-3} and a thickness of 0.3 µm,the sheet resistivity is approximately 700 Ω/sq. Assuming L_{SN} and S be 1 µm and 3 µm respectively, the resistance contribution from only the source regions without considering current crowding is around 0.01 m$\Omega\,$cm^2.

Channel Resistance

Under typical on-state bias conditions, the source and p-implanted base regions are grounded, and a positive voltage is applied to the drain. Thus the drain-base

junction is reverse biased and no current flows through the body of the base region. Since the source-base PN junction is grounded there is no current flow between them. As a result, the source and drain regions are electrically isolated. If a sufficiently positive voltage is applied at the gate electrode, then electrons from the source "spill over", forming an electron-rich layer called the channel. The channel forms a continuous electron bridge between source and drain only at the surface of the p-base, under the entire width of the gate oxide. The resistance of this region to current flow is the channel resistance. In current SiC MOSFETs, especially those designed for applications rated for 1 kV or below, this component contributes a significant percentage of the total resistance [72]. The channel resistance can be expressed as -

$$R_{CH,SP} = \left(\rho_{CH}\frac{L_{CH}}{W_{CH}}\right)\ (SW) \tag{2.9}$$

As the channel is formed locally only at the surface of the p-base, its sheet resistivity ρ_{CH} is different than that of the bulk.

$$R_{CH,SP} = \left(\frac{1}{q\mu_{CH}n_S}\right)\left(\frac{W}{W_{CH}}\right)\ (L_{CH}S) \tag{2.10}$$

Here, L_{CH} is the channel length as shown in Figure 2.3, μ_{CH} is the mobility of the majority carrier in the channel, and n_S is the channel carrier concentration in cm^{-2} at a given gate voltage.

The channel mobility depends on various factors, and a detailed discussion is included in the next chapter. In terms of its contribution to the FOM, the channel resistance is independent of blocking voltage as seen in Equation 2.10, and appears as a horizontal line in Figure 2.5.

The field effect mobility in SiC MOSFETs is more than a order of magnitude lower than the bulk moblity and this significantly impacts the channel resistance [30]. At an overdrive voltage ($V_{GS}-V_{TH}$) of 15 V, an oxide field of 4 MV/cm, a cell pitch of 3 µm, and a 0.5 µm long channel, a DMOSFET would exhibit a $\mathrm{R}_{CH,SP}$ of 1.55 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ with an assumption of 15 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for channel mobility. For a device designed for 1 kV or less, this component contributes at least 70% of the total resistance. A novel

approach to counter this issue will be proposed later in chapter 3 to minimize this dominant component of resistance.

JFET Resistance

The inherent JFET region in a DMOSFET plays an important role in determining its total specific on-resistance. The design of the JFET region, such as the geometry and doping, requires careful consideration since it has a cascading effect on the other parameters. At a given doping, the JFET width must be optimized to achieve minimum specific on-resistance. An increase in the JFET width increases total cell pitch thus increasing the specific on-resistance. In addition, the electric field in the off-state will fall more steeply from the gate oxide towards the drain, reducing the blocking voltage. On the other hand, aggressive reduction is constrained by pinch-off of the JFET region and thus would require higher doping in the JFET. Higher doping in a narrow JFET is possible due to the additional shielding by the adjescent p-base regions that protect the oxide-JFET interface from high fields. Therefore the optimized JFET thickness and width must be found for a device at a given doping concentration using an iterative design approach.

Typically, the JFET region can be doped as high as 1×10^{17} cm^{-3}, and may extend below the base region. This extension is known as a current spreading layer (CSL), and its purpose is to efficiently spread the current over the whole area of the drift layer. This effectively reduces the drift layer resistance by increasing the current conducting area. The JFET specific on-resistance of a device with the dimensions specified in Figure 2.3 can be expressed as

$$\begin{aligned} R_{J,SP} &= \rho_J \frac{t_J}{(L_J/2 - x_{dj})W} \, (SW) \\ &= \rho_J \frac{t_J S}{(L_J/2 - x_{dj})} \end{aligned} \tag{2.11}$$

In this expression ρ_J is the resistivity at the JFET region defined by doping concentration and the mobility, and x_{dj} is the width of the space charge region at the p-base to JFET junction, can be written as

$$x_{dj} = \sqrt{\frac{2\,\epsilon_S}{q\,N_J}\,(V_{BI} + V_J)} \tag{2.12}$$

where ϵ_S is the permittivity of SiC, N_J is the JFET doping concentration, V_{BI} is the built in potential at base-JFET junction and V_J is the voltage drop at a given position in the JFET region at a certain current with respect to the grounded source.

The resistivity of the JFET region with mobility μ_J can be expressed as -

$$\rho_J = \frac{1}{q\mu_J N_J} \tag{2.13}$$

The mobility in JFET region can be expressed as [73]-

$$\mu_J = \frac{1141(T/300)^{-1.884}}{1 + (N_J/1.94 \times 10^{17})^{0.61}} \tag{2.14}$$

With the nominal values of the parameters as shown in the Figure 2.3, the JFET resistance can be approximated at around 0.08 $\mathrm{m\Omega\,cm^2}$.

Drift Resistance

The drift layer resistance is defined by its thickness and doping concentration, which are determined by the desired blocking voltage [30]. The case of an abrupt one sided PN junction with a non-punch-through design was discussed in Chapter 1 (Figure 1.1). For such a case, the optimum doping can be obtained by rearranging the terms of (1.1):

$$N_D = \frac{\epsilon_s E_C^2}{2qV_B} \tag{2.15}$$

The minimum drift-layer resistance is given by [7, 11, 30] -

$$R_{drift,sp}[\mathrm{m\Omega\,cm^2}] = \frac{4V_B^2}{\eta\epsilon\mu E_C^3} \tag{2.16}$$

where ϵ, μ, and E_C are the semiconductor dielectric constant, mobility, and critical field, respectively, and η is the ionization ratio for the drift layer dopants. This is

especially important for SiC, where incomplete ionization of dopants is often observed at room temperature. Nitrogen is a relatively shallow donor in 4H-SiC, and for N doping of 10^{17} to 10^{15} , η is about 0.9 - 1.0.

In practice, a punch-through device is the optimal design to maximize the FOM [57]. As stated earlier, the blocking voltage is the area under the electric field profile across the width of the device. In the case of the triangular electric field profile (Figure 1.1), the most of the potential drop occurs near the junction and the contribution decreases away from it. The extent of the depletion region away from the junction is a function of doping. The electric field profile for a device with a fixed width W_N at various doping levels is shown in Figure 2.4.

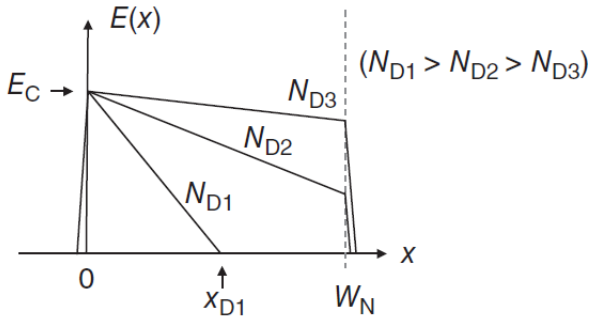


Figure 2.4.: Electric field profile under punch-through at lower doping concentrations

In comparison with the triangular electric field distribution, the electric field for the punch-through design takes on a trapezoidal shape, and varies more gradually with distance. Thus the idea of the punch-through design is to decrease the doping for the same blocking voltage by adjusting the thickness of the drift region. In the optimal case the electric field at the drift-substrate junction is equal to $E_C/3$. For example, it is possible to obtain a breakdown voltage of 1,000 V with a drift region thickness of about 5 µm. In contrast, a drift region thickness of 8 µm would be required in the non-punch-through case.

The FOM for the punch-through scheme is given by -

$$\frac{V_B^2}{R_{on,sp}} = \left(\frac{2}{3}\right)^3 \mu_n \epsilon_s E_C^3 \tag{2.17}$$

By employing a punch-through design, an additional 18.5% benefit can be achieved in the FOM. In this case, the optimal drift resistance is given by the empirical relation -

$$R_{drift,sp}[\mathrm{m\Omega\,cm^2}] \approx 2.8 \times 10^{-8} \left(T/300\right)^{2.8} V_B^{2.29} \tag{2.18}$$

Although the drift resistance (R_{drift}) is proportional to V_B^2 in Equation 2.16 and 2.17, the empirical resistance increases in proportion to $V_B^{2.3}$ because the breakdown field strength and electron mobility have a doping dependence (Figure 1.3). For example, it decreases in the lightly-doped materials employed for high-voltage devices.

Table 2.1 lists the optimized drift region design equations. As seen, the drift resistance is a power law function of the blocking voltage V_B, and is illustrated in Figure 2.5. As expected, the drift resistance becomes the dominating factor for high blocking

Table 2.1.: Optimal drift region design equations

Non Punch-through Design (Triangular Field)	Punch-through Design (Trapezoidal Field)
$W_N = 2\left(\frac{V_B}{E_C}\right)$	$W_N = \left(\frac{3}{2}\right)\left(\frac{V_B}{E_C}\right)$
$N_D = \left(\frac{\epsilon_s E_C^2}{2qV_B}\right)$	$W_N = \left(\frac{2}{3}\right)^2\left(\frac{\epsilon_s E_c^2}{2qV_B}\right)$
$R_{on,sp} = \left(\frac{4V_B^2}{\mu_N \epsilon_s E_C^3}\right)$	$R_{on,sp} = \left(\frac{3}{2}\right)^3\left(\frac{V_B^2}{\mu_N \epsilon_s E_C^3}\right)$

voltages above 2 kV. It should be noted that the mobility of the drift layer depends on both temperature and doping concentration and can be empirically expressed as [73]

$$\mu_N = \frac{1141(T/300)^{-2.582}}{1 + (N_D/1.94 \times 10^{17})^{0.61}} \tag{2.19}$$

At room temperature, with the dimensions and doping specified in Figure 2.3, the drift layer specific on-resistance contribution is 0.6 $\mathrm{m\Omega\,cm^2}$ for a blocking voltage of 1.2 kV.

Substrate Resistance

The nominal thickness of a SiC wafer is generally 350 µm [74]. The substrate plays an important role in the total specific on-resistance in devices designed for low voltage applications. The region is heavily doped to minimize the resistance and to provide a good ohmic drain contact. The substrate resistivity is given as a specification with the wafer, and is generally between 15-28 $\mathrm{m\Omega\,cm}$ at room temperature, corresponding to a doping concentration of 10^{18}-10^{19} $\mathrm{cm^{-3}}$. The specific on-resistance due to the substrate can be written as –

$$\begin{aligned} R_{SUB.SP} &= \left(\rho_{SUB}\frac{t_{SUB}}{SW}\right)\,(SW) \\ &= \rho_{SUB}t_{SUB} \end{aligned} \tag{2.20}$$

In this equation, ρ_{SUB} is the resistivity, and t_{SUB} is the thickness of the substrate. With a thickness of 350 µm and a resistivity of 28 $\mathrm{m\Omega\,cm}$, the specific on-resistance contribution from the substrate is around 0.98 $\mathrm{m\Omega\,cm^2}$. Special consideration should be given to minimizing this dominant resistance component for devices designed to block less than about 2 kV. This may include thinning the wafer to as low as 120 µm after device fabrication thus reducing the substrate specific resistance to 0.3$\mathrm{m\Omega\,cm^2}$ as shown in Figure 2.5 for a substrate with doping of $10^{19}\mathrm{cm^{-3}}$.

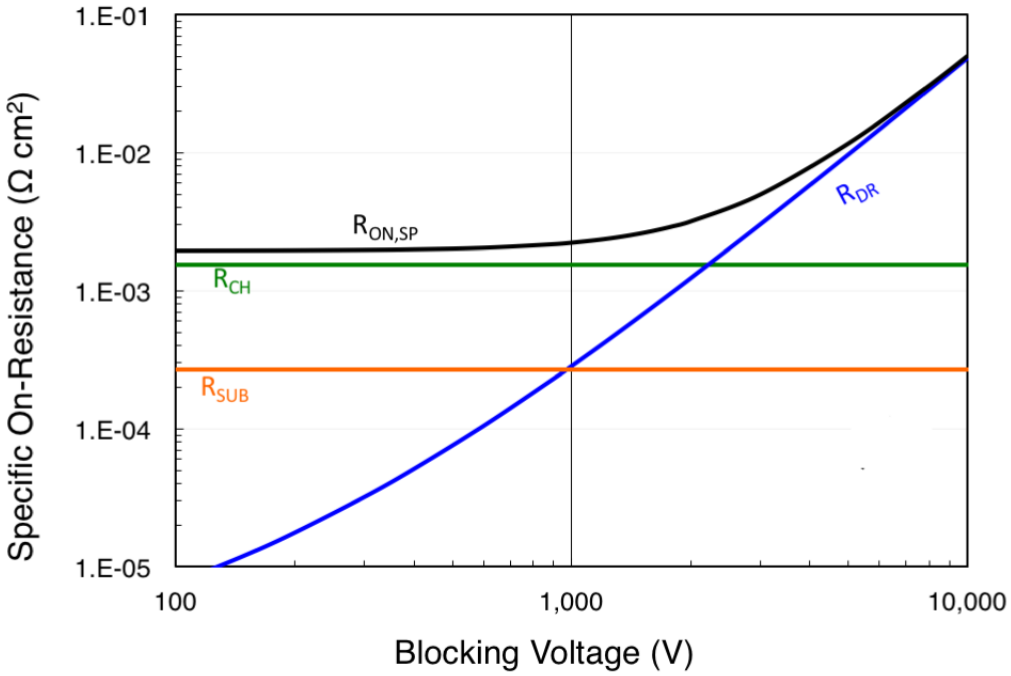


Figure 2.5.: Series resistance components in a DMOSFET

2.3 Challenges and Limitations of SiC MOSFETs

From the point of view of the theoretical FOM (Equation 2.5), SiC MOSFETs outperform their Si counterparts at all blocking voltages. However SiC MOSFETs are primarily used in the blocking voltage range of 1kV-6.5kV [7, 74]. At high blocking voltages (>6.5kV), the drift layer thickness increases and the corresponding extra resistance adds significantly to the total resistance in the on-state. In this regime, bipolar devices such as the bipolar junction transistor (BJT) and the insulated gate bipolar transistor (IGBT) have been developed, both of which utilize conductivity modulation to reduce the resistance of the drift layer. In the lower blocking voltage regime however, the channel resistance severely limits the performance of the SiC MOSFETs as seen in Figure 2.8.

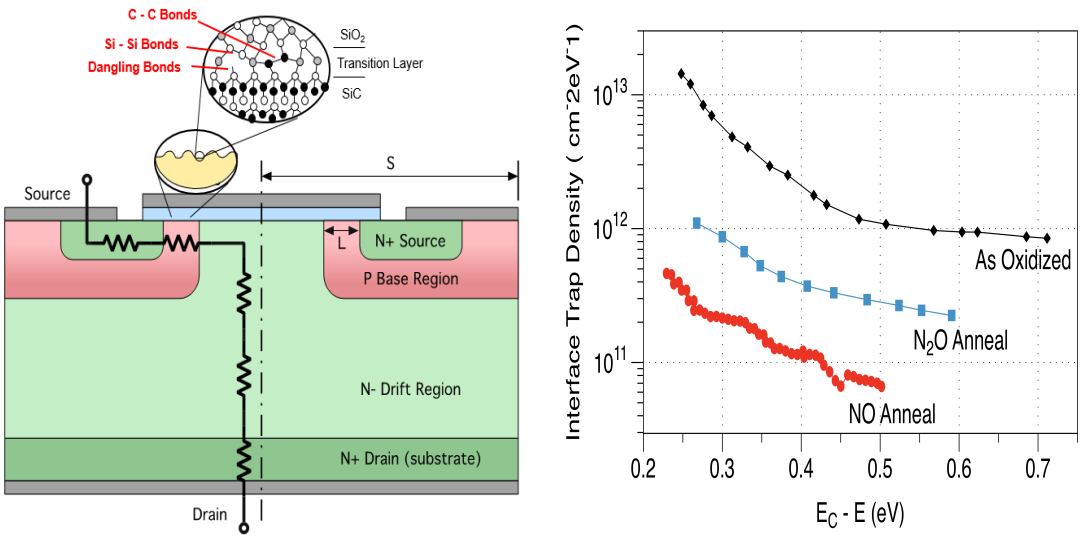
The channel resistance is severely impaired by the poor quality interface between SiC-SiO_2 [71, 75], compared with silicon devices. This reduces the channel mobility,

as well the mobile charge in the channel, both of which contribute to increasing the channel resistance of the device. The key challenges in enhancement of the channel mobility and the current status and understanding of the interface properties of SiC MOS structures are discussed in the next section.

Properties of SiC-SiO_2 interface

One major advantage of SiC over other wide band gap semiconductors is that it can be oxidized to grow a dielectric on the surface. Thermal oxides of SiC are commonly employed as a gate dielectrics in MOS devices as well as to passivate the SiC surface [76]. However, the most striking difference from Si technology is the presence of carbon, one of the host elements in SiC. This adds significant complexity to the MOS properties of thermal oxides and its understanding is still an open question in the scientific community [77,78]. Conventional dry oxidation usually yields a high density of interface states as shown in Figure 2.6(b). The standard process to improve the properties of SiC MOS structures is post-oxidation nitridation in a nitrogen containing gas such as nitric oxide (NO) [79–81] or nitrous oxide (N_2O) [82,83]. This technique is widely employed in academic research as well as in the mass production of SiC power MOSFETs. Figure 2.6(b) depicts the distribution of the interface state density (D_{IT}) near the conduction obtained from n-SiC (0001) MOS capacitors exposed to different post-oxidation treatments.

The interface state density shown in the figure was evaluated by the conventional high (1 MHz)-low method. Clearly, a reduction in the interface state density over a considerable range of energies near the conduction band edge is achieved by nitridation, and is consistent with data published in literature [84,85]. As a result, the peak effective mobility of n-channel SiC(0001) MOSFETs fabricated on lightly-doped p-type epitaxial layers is enhanced from 8 $cm^2\,V^{-1}\,s^{-1}$ for dry oxides to 45 $cm^2\,V^{-1}\,s^{-1}$ for NO-nitrided oxides [86].



(a) (b)

Figure 2.6.: (Non-idealities at the SiC/SiO_2 interface. a) Various defects and impurities at the SiC-SiO_2 interface leads to electronic defects in the MOSFET channel region and increases the channel resistance (b) Interface trap density in 4H-SiC MOS structures near conduction band measured using high-low method

While the reduction in D_{IT} improves the channel mobility, it is still an order of magnitude lower than that of the bulk. The physical reason for the low channel mobility of SiC MOSFETs is still under investigation without a conclusive theory [87]. In Si MOSFETs, the main factors limiting the channel mobility are the fixed charge and surface roughness because the interface state density in Si MOS structures is typically low enough not to limit the channel mobility [88]. This is not the case in SiC, where the electrons trapped in interface states, even after the post oxidation NO anneal, have a significant effect on the mobility.

The high interface trap density has a two fold effect on the channel mobility. It not only increases the rate of coulomb scattering of carriers in the channel, but it also reduces the number of electrons that contribute to the current in the device. The

total charge (n_{total}) induced in the channel at a specific gate voltage ($C_{ox}(V_G - V_T)$) can be divided into two constituents and expressed as [17]-

$$n_{total} = n_{channel} + n_{interface} \tag{2.21}$$

Here, $n_{channel}$ is the mobile charge in the channel and $n_{interface}$ is the charge that is trapped in interface defects and does not contribute to the total current of the device. In this case, the apparent channel mobility can be written as -

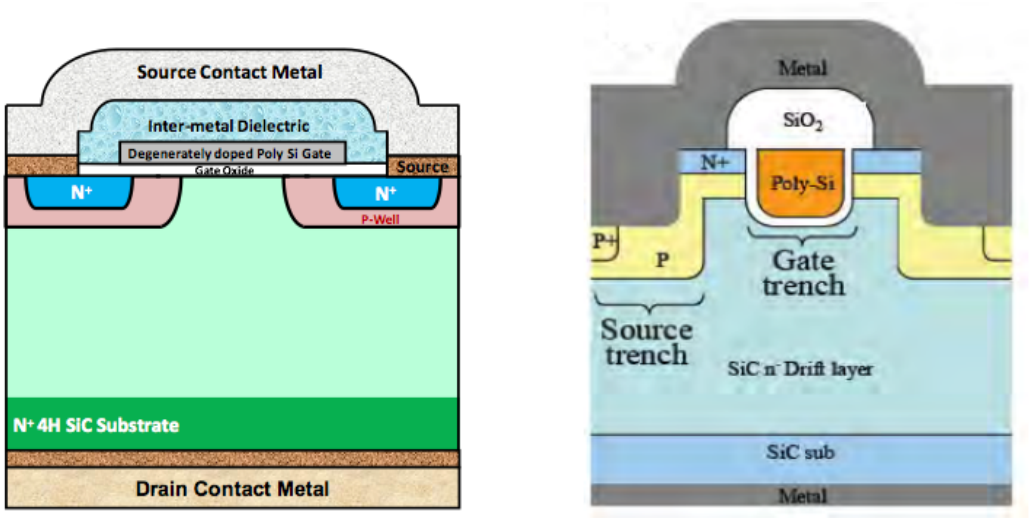
$$\mu_{ch} = \mu_{surface} \left(\frac{n_{channel}}{n_{channel} + n_{interface}} \right) \tag{2.22}$$

where $\mu_{surface}$ is the mobility corresponding to the maximum charge in channel at a certain gate voltage. In SiC MOSFETs, the contribution of $n_{interface}$ cannot be neglected and thus acts to reduce the measured channel mobility. Measurements have shown that the channel mobility increases at elevated temperatures and this is largely due to the fact that the trapped electrons ($n_{interface}$) thermalize and can now contribute to the measured current [89, 90]. Recent results have shown that reduction of the interface trap density eliminates this behavior and the channel mobility decreases with increased temperature due to increased phonon scattering [30].

Power MOSFETs are operated high oxide fields where the contribution of the surface roughness scattering becomes important [91, 92]. Therefore at sufficiently low interface trap densities, the contribution of the surface roughness may become prominent at room temperature. Experimental evidence of such a dependence has yet to be established and the effective channel mobility in current devices is limited by the high density of interface traps [89].

2.4 Current State-of-the-Art MOSFETs

The current state-of-the-art 4H-SiC MOSFETs include several innovations [93]. This includes (i) a self-aligned sub-micron MOS channel, (ii) a more heavily doped



(a) (b)

Figure 2.7.: Cross section illustration of commercially available SiC Power MOSFETs (a) Wolfspeed 3rd Generation DMOSFET (Released 2016) and (b) Rohm double-trench UMOSFET

JFET region, (iii) a current spreading layer (CSL), (iv) source ohmic contacts that are self-aligned to the polysilicon gate, and (v) p base contacts that are segmented along the length of the fingers. A DMOSFET structure with these features is shown in Figure 2.7(a).

With these features, MOSFETs have been commercialized since 2011. DMOSFETs with blocking voltages from 650 V-6.5 kV are now available with a $R_{on,sp}$ of 2.3m$\Omega\,$cm^2 to 110m$\Omega\,$cm^2 respectively. Recently, trench UMOSFETs have also been commercialized and are available with a blocking voltage up to 1700V. The lowest $R_{on,sp}$ for a device rated 690V is 1m$\Omega\,$cm^2. Results from some of these MOSFETs are overlaid on the same V_B vs $R_{on,sp}$ plot seen earlier and is shown in Figure 2.8. The comprehensive list of companies who manufacture SiC MOSFETs and their specification is listed in Appendix I. With the development and advancement in SiC technology, performance of the SiC MOSFETs have approached the theoretical limit at

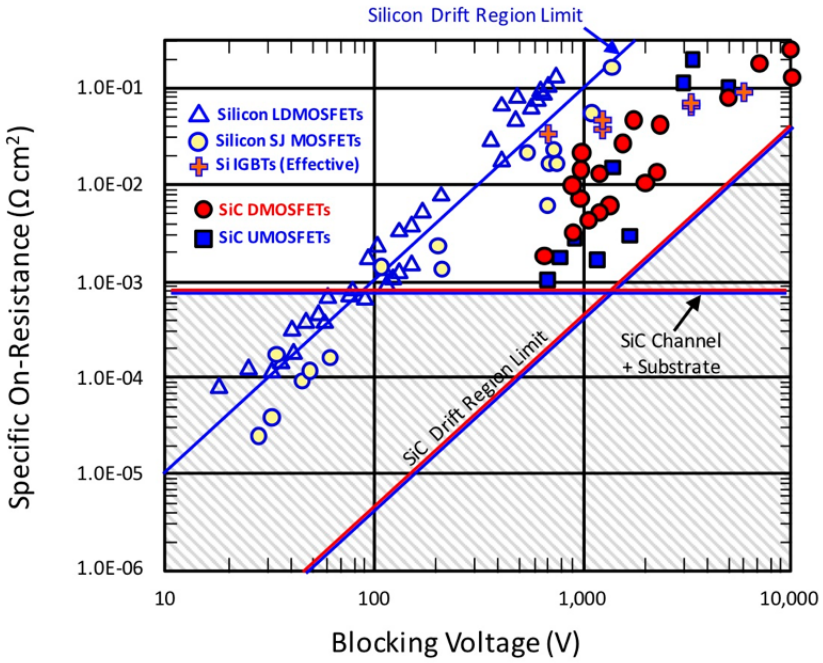


Figure 2.8.: Performance of silicon MOSFETs and IGBTs compared to the SiC MOSFETs. The limits imposed by channel, substrate and drift region resistances are also depicted

blocking voltage above 2kV as seen in Figure 2.8. New devices are introduced to the market on a regular basis and have been adopted in a number of applications. However SiC MOSFETs have yet to meet their full potential and a number of challenges need to be addressed.

2.5 Need for innovation in the low voltage regime

The low voltage regime presents a unique problem for SiC technology today. Theoretically, SiC unipolar devices (MOSFETs) outperform Si in this regime (Equation. 1.6). There also exists a formidable body of work in terms of theoretical and experimental understanding of the design, operation and integration of SiC MOSFETs. There has been continuous work on the reliability aspects of SiC MOSFETs over the

last decade and important features of device and MOS reliability have been worked out. Above all, there exists a large industry segment of low voltage applications where Si devices are still widely used. With all this in place, SiC MOSFETs appears poised to compete and win in the low voltage regime. However, there has not been considerable penetration of SiC in the market for devices at 900V and below. As seen earlier, this has been limited mainly by channel resistance.

Since the commercialization of SiC MOSFETs, the main focus has been on reduction of cell pitch, JFET design optimization, process development and reliability. With respect to reduction of channel resistance, most of the work in the last two decades has been towards achieving a better interface quality and it still remains a hot topic both in industry and academia. The NO anneal still remains the most stable and reliable interface passivation technique, and the channel mobility is still an order of magnitude lower than that of the bulk. Though there have been recent demonstrations of new interface passivation techniques, but they must pass the stringent requirements of MOS reliability and the road to their commercial integration is long.

Currently, the channel resistance contributes over 70% of total specific on-resistance at blocking voltages below 1.2 kV. Thus there exists a strong motivation to think outside the box in order to make SiC MOSFETs feasible in the low voltage regime. A strategy and proposal to do so is discussed in the next chapter.

3. THE TRIGATE SiC MOSFET

To utilize the capabilities and advantages of SiC power MOSFETs at blocking voltages below 1000V, the specific channel resistance must be improved as pointed out in the previous chapter. In this chapter, a new and unique SiC power device is proposed which achieves a dramatic reduction in channel resistance, and hence enables SiC MOSFETs to compete in the low voltage regime.

3.1 Channel Resistance Reduction - Approach

Consider the typical dimensions of a state-of-the-art DMOSFET as shown in Figure 3.1, and recall that $R_{ch,sp} = R_{ch} \times (W \cdot S)$. In the on-state, a small drain voltage (V_D) is applied and the gate voltage (V_G) is such that there exists a continuous sheet of electrons (inversion layer) along the channel (L_{ch}) in the y-direction and throughout the width W in the z-direction. Thus, the specific channel resistance is expressed as

$$R_{ch,sp} = \frac{L_{CH}}{\mu_{ch} C_{ox} W_{ch} (V_G - V_T)} \times (W_{cell} \cdot S) \tag{3.1}$$

The terms in the equation above can be rearranged and expressed as following.

$$R_{ch,sp} = \left[\frac{1}{\mu_{ch} \epsilon_{ox} \frac{(V_G - V_T)}{t_{ox}}} \right] \times \left[L_{ch} S \left({}^{W_{cell}}/_{W_{ch}} \right) \right] \tag{3.2}$$

The terms in the first square bracket are related to electron transport in the channel and properties of the SiC-SiO_2 interface. While there have been recent advances and research activity on this front, progress has been limited as described in the previous chapter. Thus at given gate voltage, crystal orientation and a maximum operating field in the oxide of 4 MV/cm, the terms in the first bracket are assumed to be constant. The terms in the second bracket correspond to the geometry of the device as seen in Figure 3.1. The goal is to reduce the specific channel resistance and a

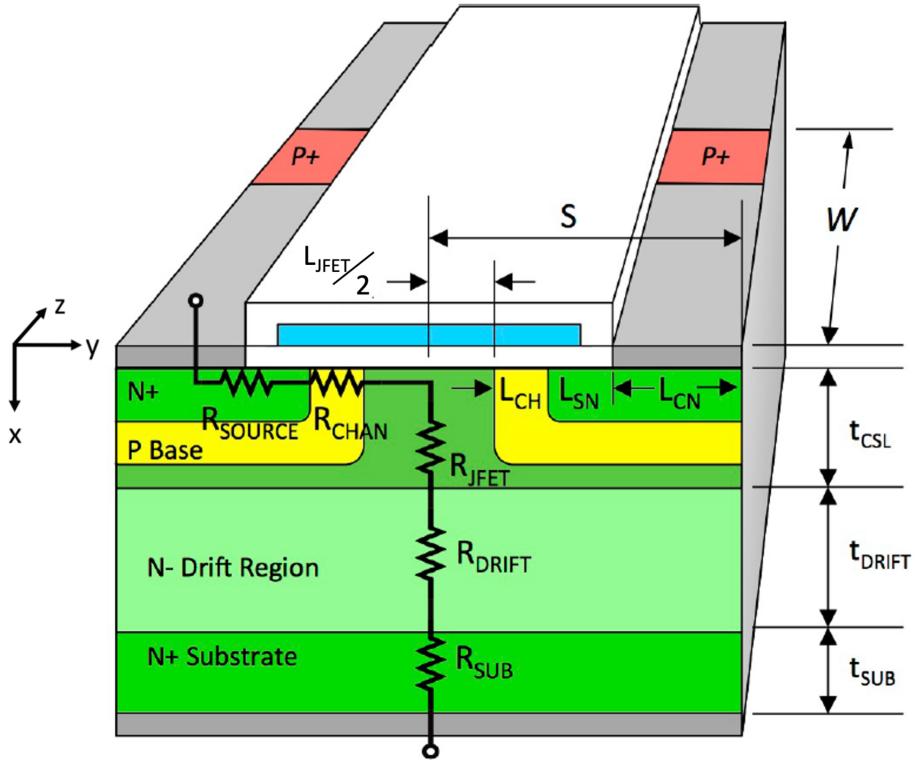


Figure 3.1.: Components of specific channel resistance in a vertical SiC DMOSFET

method to do so by minimizing the contribution from the geometry of the device is proposed in the next section.

3.2 Trigate Power DMOSFET - Concept

The approach in this proposal is a novel structure in which the channel width W_{CH} is larger than the unit cell width W. This is achieved without increasing the total device area, thus reducing the specific on-resistance by a factor of 3 or more.

In the conventional DMOSFET or UMOSFET, the channel width W_{CH} is made as large as possible in the z-direction and essentially is same as the total width of the device, W. Thus the ratio of these two widths is unity, and the channel specific on-resistance does not depend on any additional parameter. However, if these two

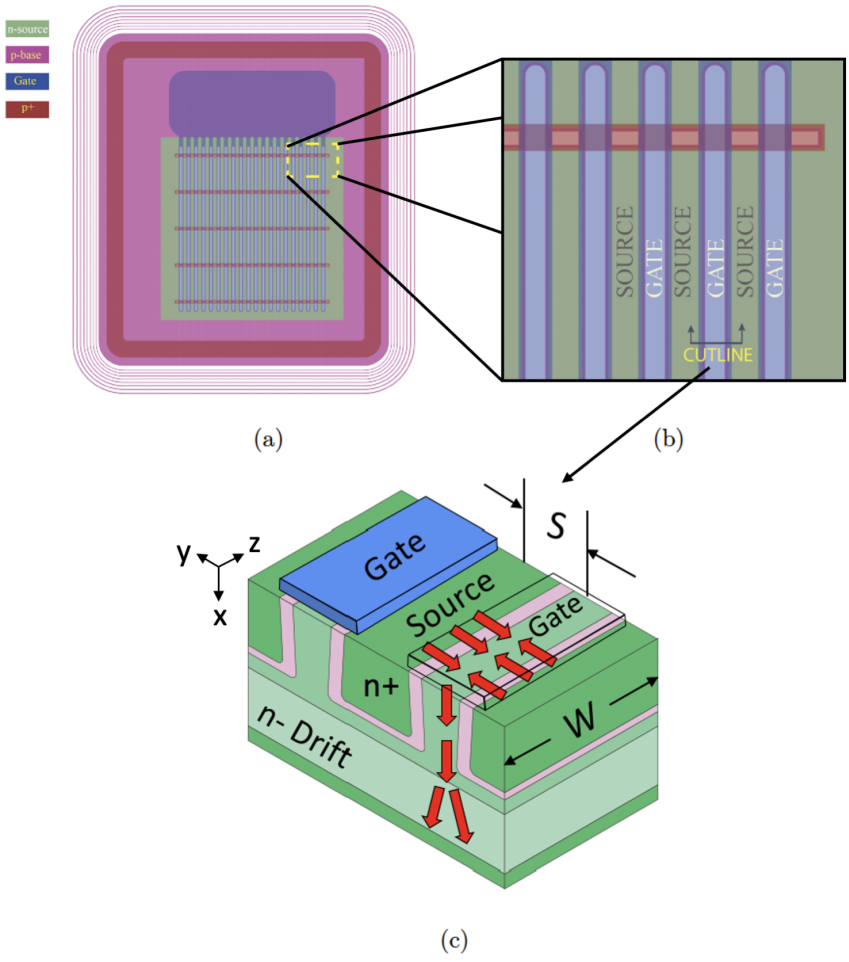


Figure 3.2.: DMOSFET design structure (a) Complete device, (b) Close-up view (c) An isometric view from the cut-line of (b)

parameters can be decoupled, a significant reduction in channel resistance is possible. To do this, additional channel width along the x-direction can be created such that W_{CH} is higher than W. The proposed structure is similar to the FinFET originally demonstrated at U. C. Berkeley [94] and later utilized by Intel in their 22 nm node for improved gate control and reduced drain induced barrier lowering [95]. We use it in power MOSFETs for an entirely different reason: to increase the width of the current-carrying channel without increasing the area of the cell.

The idea is explained by first depicting the structure of a conventional DMOSFET in Figure 3.2. Each device consists of interdigitated source and gate fingers as shown in Figure 3.2(a). As illustrated in the isometric image of Figure 3.2(c) we see that electrons flow from the N^+ source, across the inversion layer, into the n-type JFET region, and then downward through the n- drift layer into the N^+ substrate. From this figure it is clear that the width of the channel and the device is the same, giving a unity W/W_{CH} factor.

A new alternative trigate MOSFET structure for a power DMOSFET is illustrated in Figure 3.3. As seen in the figure, narrow fins and trenches are formed perpendicular to the source and gate fingers before gate oxidation. An isometric view of such a design is shown in Figure 3.3(c). The trench opens up an additional current path along the sidewall of the trench, along a $(11\bar{2}0)$ face, in addition to the current paths on the top and the bottom of the trench along (0001), similar to the conventional case. The additional current path is shown in 3.3(c) by yellow arrows. The channel width is effectively increased without increasing the cell width of the device, and this geometric benefit translates to a decrease in the specific on-resistance. As there is an increase in the current per unit width, proportionately more die can be accommodated on the SiC wafer which brings down cost.

The equivalent circuit containing the series resistance components in the case of the trigate is depicted in Figure 3.3(d). The effective channel resistance is therefore the parallel combination of the resistance contribution from the top, side and bottom transistors. The specific channel resistance for each component is similar to the

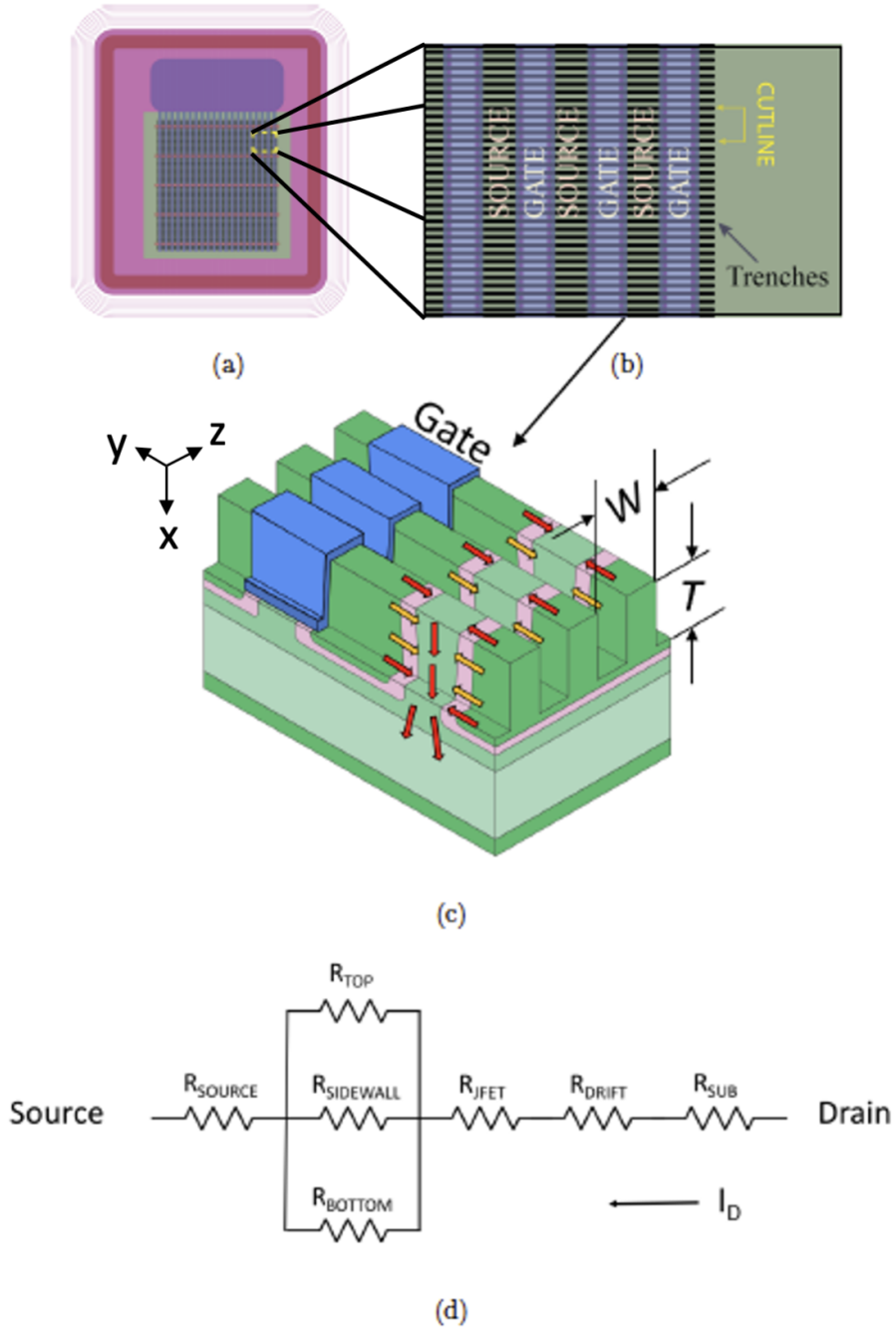


Figure 3.3.: Trigate MOSFET structure: (a) Complete device, (b) Close-up view of (a), and (c) An isometric view from the cut-line, and (d) Equivalent resistance circuit between source and drain.

Equation 3.2, but with the respective channel widths and channel mobilities. The equation can be rearranged and expressed as -

$$\frac{1}{R_{ch,sp}} = \frac{1}{R_{ch,sp,Top}} + \frac{1}{R_{ch,sp,Sidewall}} + \frac{1}{R_{ch,sp,Bottom}}$$

$$R_{ch,sp} = \left(\frac{L_{ch}W_{cell}S}{C_{ox}\,(V_G - V_T)}\right)\left[\frac{1}{\mu_{top}W_{top} + \mu_{sidewall}W_{sidewall} + \mu_{bottom}W_{bottom}}\right] \quad (3.3)$$

As seen in Figure 3.3(c), if vertical sidewalls are assumed, the top and bottom channels widths are essentially equal to the total horizontal width W_{cell}. Therefore the terms in the square brackets of Equation 3.3 can be replaced with -

$$W_{CH}\;\mu_N = W_{cell}\;\mu_{horiz} + W_{sidewall}\;\mu_{sidewall}$$

Here, the second term on the right represents the additional current paths provided by the trigate structure. The specific on resistance of the trigate can now be expressed as -

$$R_{ch,sp} = \left(\frac{L_{ch}W_{cell}S}{C_{ox}\,(V_G - V_T)}\right)\left[\frac{1}{W_{cell}\;\mu_{horiz} + W_{sidewall}\;\mu_{sidewall}}\right] \quad (3.4)$$

3.2.1 Performance Benefit

The trigate structure reduces the specific channel resistance by increasing the current-carrying width of the inversion layer without increasing the active device area. The performance benefit is compared to the conventional planar DMOSFET by taking the ratio of the respective specific on-resistances. As pointed out earlier, the W_{cell}/W_{ch} ratio for the planar case is equal to one. Thus the specific on-resistance is equal to -

$$R_{ch,sp\ (Planar)} = \left(\frac{L_{ch}S}{C_{ox}(V_G - V_{TH})}\right)\left[\frac{1}{\mu_{horiz}}\right] \quad (3.5)$$

The ratio of Equation 3.4 and Equation 3.5 indicates the performance benefit. The term in the first bracket is common in both equations and cancels out.

$$\begin{aligned}\frac{R_{ch,sp\ (3G)}}{R_{ch,sp\ (Planar)}} &= \frac{\mu_{horiz} W_{cell}}{W_{cell}\ \mu_{horiz} + W_{sidewall}\ \mu_{sidewall}} \\ &= \frac{1}{1 + \left(\frac{W_{sidewall}}{W_{cell}}\right)\left(\frac{\mu_{sidewall}}{\mu_{horiz}}\right)}\end{aligned} \tag{3.6}$$

Performance Benefit from Width Ratio

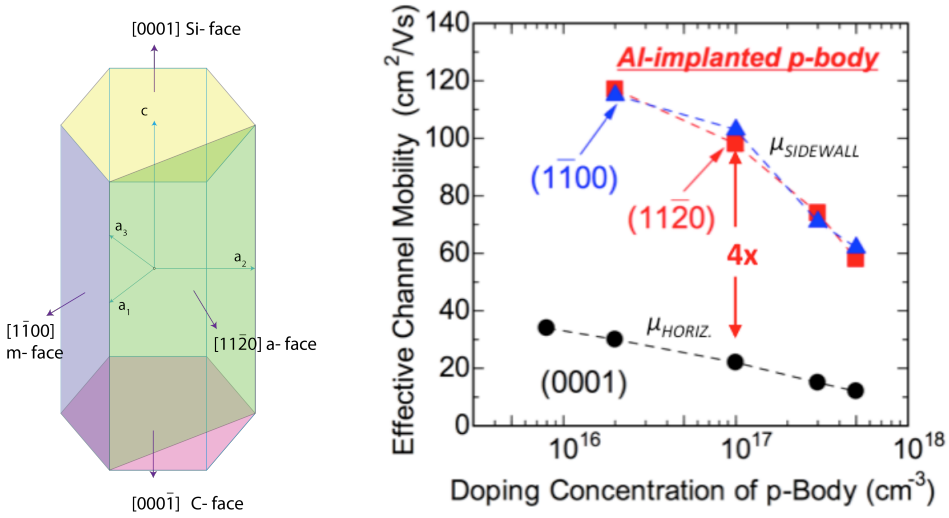
As seen in Equation 3.6, maximizing the width ratio increases the performance benefit. The cross section of the unit cell is illustrated in Figure 3.3(c). The side wall W_{side} is equal to height of the trench T. Also, there are two vertical side walls per unit cell which means two parallel conducting paths. Thus the geometric width ratio is $2T/W$, and the performance gain in specific on-resistance is -

$$\frac{R_{ch,sp\ (3G)}}{R_{ch,sp\ (Planar)}} = \frac{1}{1 + 2\left(\frac{\mu_{sidewall}}{\mu_{horiz}}\right)\left(\frac{T}{W_{cell}}\right)} \tag{3.7}$$

For instance, if $T = W = 1$ µm, and $\mu_{sidewall}/\mu_{horiz} = 1$, the reduction factor is 3:1. The channel resistance reduction for a 2 µm trench depth is approximately 5:1.

Performance Benefit from Carrier Mobility Anisotropy

The electronic properties of SiC are different along different crystal planes, as described earlier. This includes the field effect mobility, which also varies with the orientation of the inversion channel with respect to the crystal plane in SiC n-channel MOSFETs [96]. Low interface state density and a high inversion layer mobility compared to the Si-face (0001) has been observed on MOSFETs with the inversion channel on epitaxially grown and polished $(11\bar{2}0)$ face. If the trigate device is fabricated such



(a) (b)

Figure 3.4.: Hexagonal unit cell of 4H-SiC and carrier mobility on differnt crystal planes. (a) Important crystal planes in SiC unit cell (b) Channel mobility along different crystal planes as a function of doping [8]

that the channels on the horizontal (Si-face) surface (in Figure 3.3) are aligned perpendicular to the a-face (secondary flat) then the etched trenches would be in the (11$\bar{2}$0) plane or a-face. The carrier mobilities obtained from MOSFETs fabricated on epitaxially grown layers on these two faces are shown in Figure 3.4(b) [59]. As seen in the figure, an additional factor of 3 to 5 to the reduction in the specific on-resistance can be obtained by the higher mobility on the (11$\bar{2}$0) plane as compared to the (0001) Si-face. However, in the trigate device, the a-face is exposed by selective RIE etch from the top surface. Therefore the carrier mobility in the inversion channel on this surface is expected to be lower than the values reported in Figure 3.4(b) due sidewall roughness and additional electronic defects induced during the RIE etch process.

Figure 3.5 shows the expected overall reduction in specific on-resistance of the trigate MOSFET with a trench depth of 2 µm compared to a conventional DMOSFET and UMOSFET as a function of blocking voltage, assuming a channel mobility to be

2x higher on the sidewall as compared to the horizontal surfaces, and both substrates have been thinned to 110 µm. Including all the resistances in the device, the overall resistance is reduced by a factor of 2.5 at V_B = 900 V and 3.6 at V_B= 500 V. This is significant because die area scales inversely with on-resistance, and the die cost is usually directly proportional to die area. Thus for the same specification, a reduction in the total specific on-resistance leads to a proportional reduction in cost.

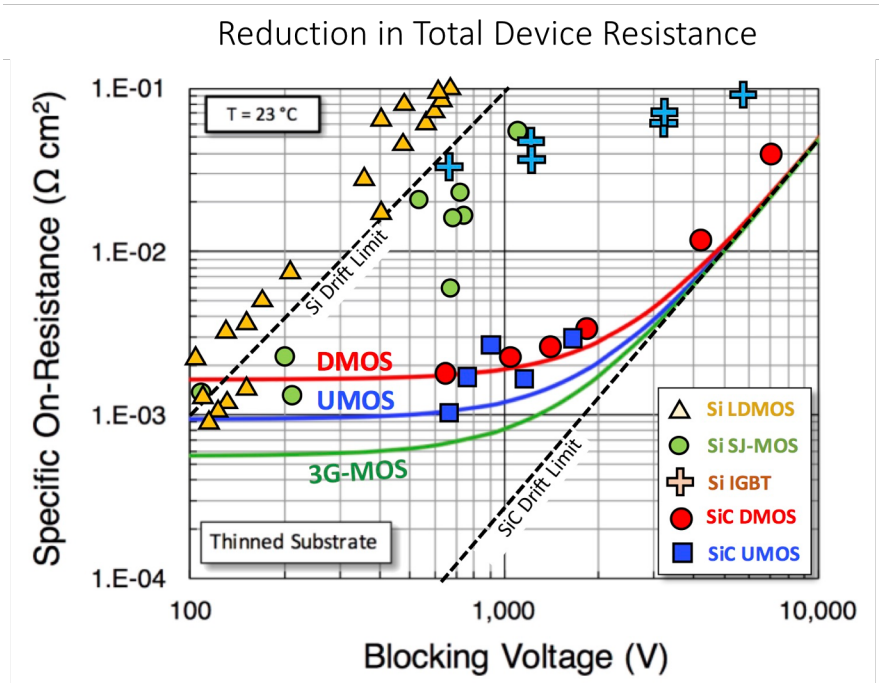


Figure 3.5.: Performance of SiC trigate MOSFET compared to DMOSFETs and UMOSFETs, along with silicon power devices

3.3 Trigate DMOSFET Performance Optimization

Performance optimization of SiC trigate MOSFETs was done through 3D numerical simulations using Sentaurus Device and related tools from Synopsis, Inc. Several key performance parameters are studied with the goal of maximixing the figure of merit (V_B^2/R_{ON}). In power devices, a fundamental unit cell, as shown in Figure 3.6,

is repeated and connected in parallel to make up the overall device. It is thus desirable to achieve the minimum practical unit cell pitch while minimizing specific on-resistance, in order to accommodate as many of these cells as possible in a given die area. However, compactness of the design may lead to an unwanted increase in resistance. The design trade offs with respect to trench height, JFET length, JFET and CSL (current spreading layer) doping and thickness, and source contact length are described below.

As seen in Figure 3.6, the unit cell pitch of the trigate MOSFET can be written as –

$$S = L_{CN} + L_{SN} + L_{CH} + \frac{L_{JFET}}{2} \tag{3.8}$$

3.3.1 Trigate Trench Height

The trigate device reduces specific on-resistance by increasing the current-carrying width of the channel without increasing the cell pitch. As seen in (3.7), the geometric ratio of the trench height to width of the unit cell and the difference in channel

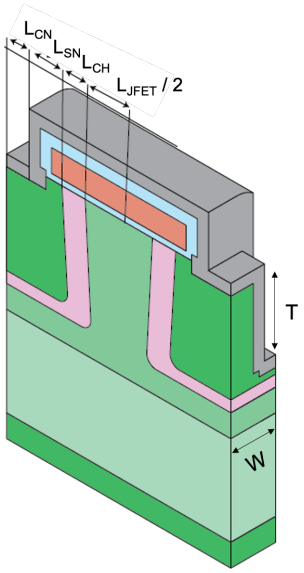


Figure 3.6.: Unit cell of a device and different dimensional components

mobility between the horizontal and sidewall surfaces determines the reduction in $R_{ch,sp}$. The trench height is determined by the trench etch process which is done after the P-well and n-source have been formed. Clearly, deeper trenches increase the width of the sidewall channel leading to lower $R_{ch,sp}$. Numerical simulations of the trigate structure with various trench depths were performed using Sentaurus Device.

Figure 3.7(a) shows the unit cell of the trigate simulation and Figure 3.7(b) shows the same unit cell when the device in is on-state. Here a positive voltage is applied on the drain with the source and body grounded, and a gate voltage that is +6V greater than the threshold voltage is applied. Figure 3.7(c) shows the drain current ratio as a function of the gate width ratio when the device is in on-state (assuming equal mobilities on the sidewalls and horizontal surfaces). In the figure, the drain current ratio plotted in the y-axis is the same factor by which the on-resistance is reduced by the trigate structure as compared to a planar DMOSFET. The dashed line is the linear relationship between the geometric width ratios and the current in the channel. As seen in the figure, the total drain current ratio follows the expectation (dashed line) up to trench depths of ~ 2 µm. As the channel resistance is reduced by deeper trenches, other resistance components such as the JFET resistance, which increases with trench depth, begins to dominate the on-resistance, and the improvement tapers off. Equal mobilities on the sidewalls and horizontal surfaces are assumed, whereas a 2 – 3x higher mobility on the a-axis sidewalls in real devices may be possible due to the carrier mobility anisotropy with respect to the crystal face. This would result in an even greater reduction in on-resistance.

The expected reduction in specific on-resistance of the trigate DMOSFET as compared to the conventional planar DMOSFET is shown in Figure 3.8. Similar to the drain current ratio in Figure 3.7(c), the on-resistance ratio between the two MOSFETs is plotted on the y-axis for different trigate trench depths. The plot shows the expected resistance reduction for several different blocking voltages. As discussed earlier, deeper trenches provide larger sidewall area without increasing the cell pitch, and therefore reduce the specific on-resistance. The total specific on-resistance at

700 V can be reduced by 3x with 2 µm deep trenches. However, deep trenches require very high energy implants which add to the fabrication complexity and cost. Thus a trade-off can be made by designing the trigate with shallower trenches. For example, a trigate device with a 1 µm deep trench will reduce the specific on-resistance by a factor of 2.5x at a blocking voltage of 700 V. To validate these numerical simulations and evaluate the performance benefits at different trench depths, trigate devices with both 2 µm and 1 µm deep trenches are fabricated as discussed in chapter 5.

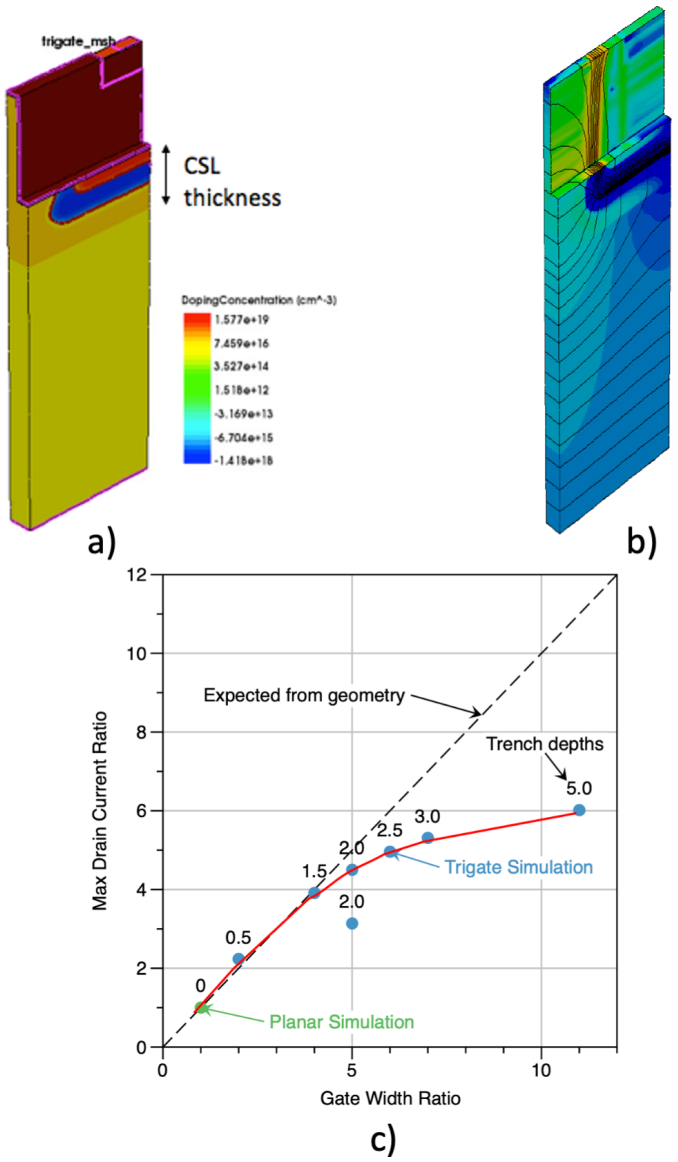


Figure 3.7.: Numerical simulation results of Trigate DMOSFET (a) Simulated unit cell. (b) Unit cell in the on-state; color indicates current density and contours are electron quasi-Fermi levels. The gate oxide thickness is 40 nm. The applied gate voltage is V_T + 6 V, and the drain bias is 0.2 V (c) Drain current ratio vs. gate width ratio as trench depth is increased from zero (a planar device) to 5 µm. The JFET width is 3 µm for all points except the lower point at a trench depth of 2 µm. For this point the JFET half-width is 1 µm. Any current ratio greater than unity represents an improvement over the conventional planar DMOSFET.

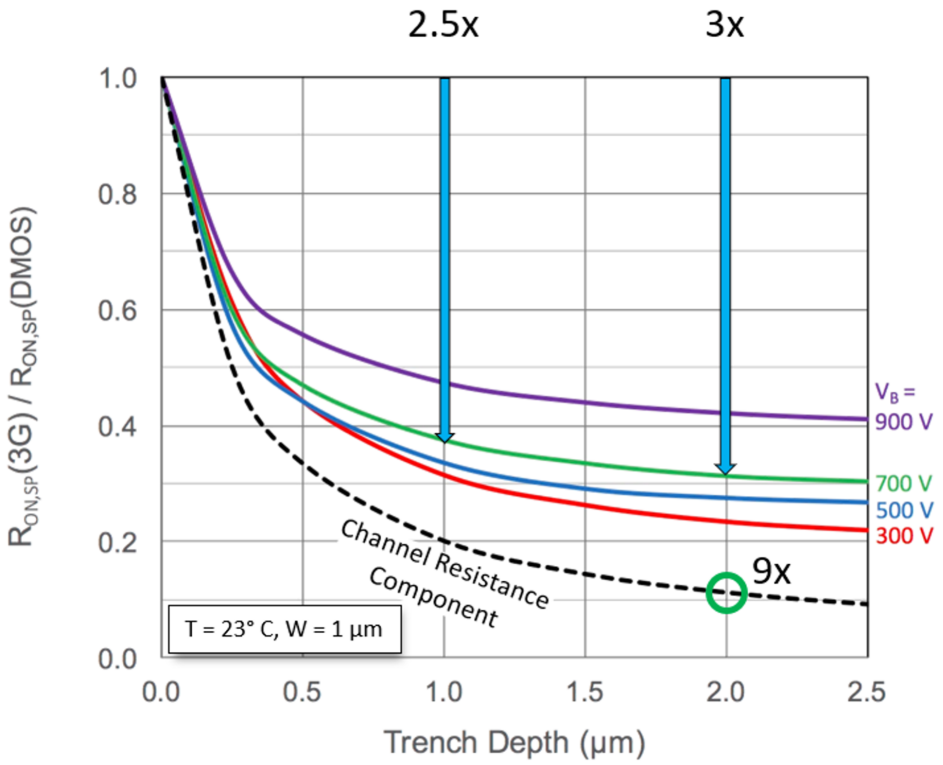


Figure 3.8.: Trigate MOSFET specific on-resistance compared with that of a standard DMOSFET as a function of trigate trench depth. Substrate is assumed to be thinned to 100µm

3.4 JFET Width Optimization

As pointed out in Section 2.2.2.1, the JFET region is inherent in a power DMOSFET and the JFET width is a critical dimension that requires careful optimization. Reduction in the JFET width reduces the cell pitch, which is desirable. However, as the JFET width is reduced, the region becomes pinched-off by depletion regions surrounding the adjacent P-wells, thus increasing the JFET resistance. On the other hand, as the JFET width is increased the cell pitch increases proportionately which increases the active area of the device, again increasing the specific on-resistance (resistance-area product). Also, in the the blocking state the peak oxide field at the center of the JFET increases as JFET width increases, due to reduced shielding from the p-type base implants. The peak oxide field needs to be kept within the safe operating limit (< 4 MV/cm) for long-term reliability. Therefore, there is an optimum point between these extremes where the contribution of the JFET region to the overall specific on-resistance is minimized, as illustrated in Figure 3.9.

A TCAD simulation of the trigate MOSFET was done to estimate the optimal JFET length. In the study, the trench depth was held constant at 1 µm, with a 0.5 µm cell pitch perpendicular to the cross section shown in Figure 3.6. Trench and

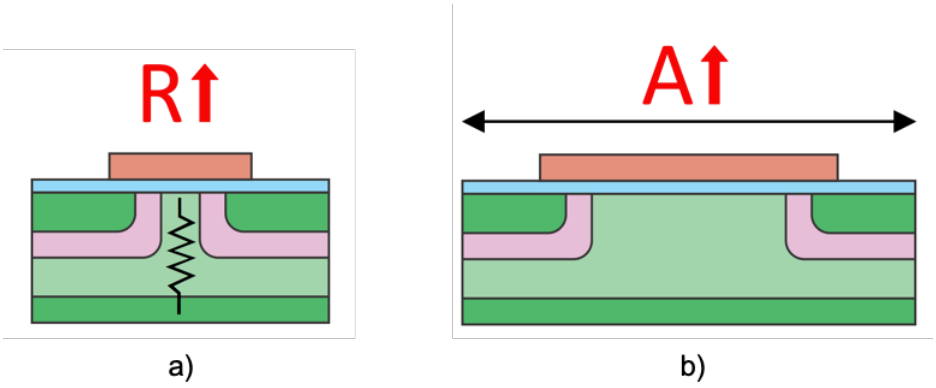


Figure 3.9.: Specific on-resistance due to non-optimum JFET region widths: (a) too narrow leads to high resistance (b) too wide leads to large area.

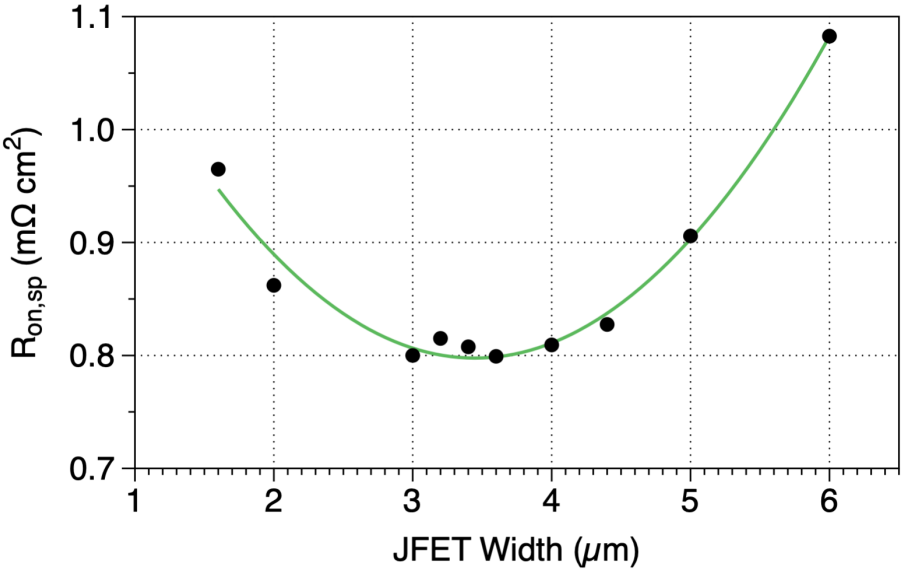


Figure 3.10.: Simulated specific on-resistance of a trigate MOSFET with variations in JFET width(LJFET)

fin widths are both assumed to be 0.5 µm. It is also assumed that the doping of the JFET region is 1×10^{17} cm^3. In the calculation of the on-resistance, the gate voltage is set such that the field in the 50 nm thick gate oxide is constant at 4 MV/cm.

From the analysis it can be concluded that aggressive scaling, such as $L_{JFET} < 2$ µm, results in pinch-off, while $L_{JFET} > 4.5$ µm results in an excessive increase in device area and thus increased specific on-resistance. The lowest specific on-resistance occurs at a JFET width of approximately 3.5 µm for this JFET doping. To experimentally verify the optimum design, JFET widths between $2.0-4.5$ µm in increments of 0.5 µm are included in the mask design.

3.4.1 Current Spreading Layer (CSL) Thickness and Doping

The half unit cell of a trigate MOSFET was simulated to identify the optimum CSL design in terms of specific on-resistance and blocking voltage. Here, an approximate breakdown analysis model that is available in Sentaurus Device is used for calculating

the blocking voltage of the trigate MOSFET. This model solves Poisson's equation and calculates the resulting ionization integral, and produces reasonably accurate results with dramatic reductions in computation time. The accuracy was verified by comparison with simulations which include the hole and electron continuity equations.

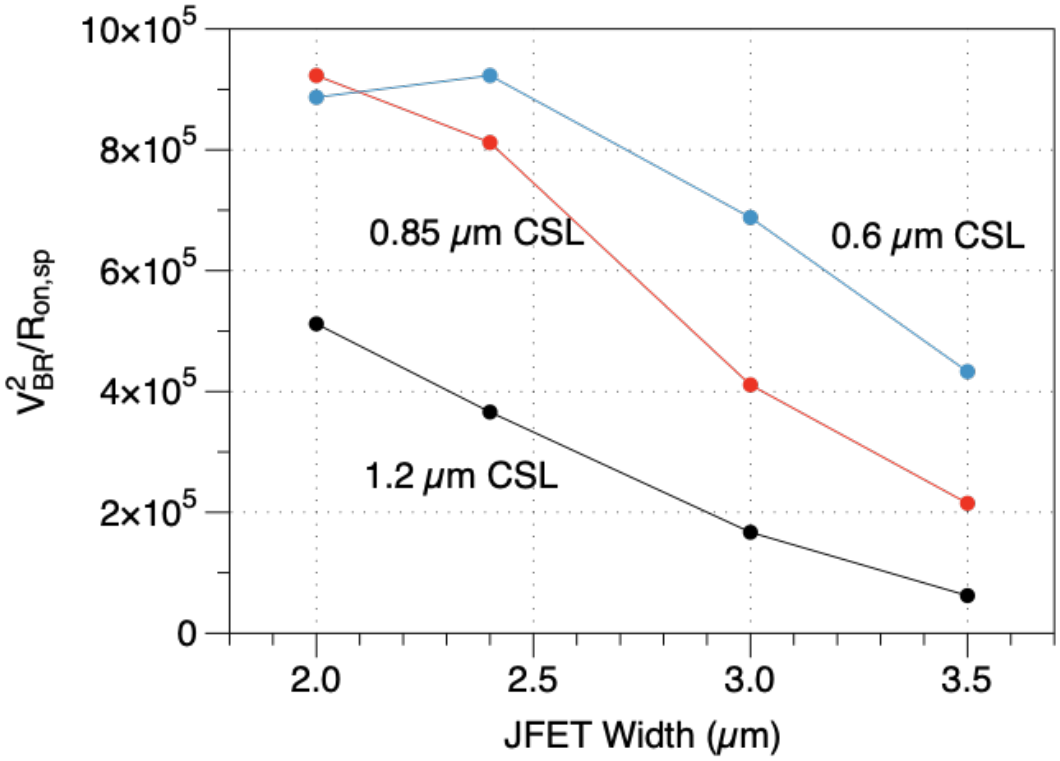


Figure 3.11.: Figure of merit vs. JFET width for different CSL thicknesses with a trench depth of 2 µm and a CSL doping of $1 \times 10^{17}\text{cm}^3$

The n-type current spreading layer (CSL) plays an important role in determining the blocking voltage of the MOSFET. The unit cell in Figure 3.7(a) should have a breakdown voltage of 930 V based on a planar one-sided step junction model, but the simulated breakdown voltage is only 640 V. However, when the thickness of the CSL layer is reduced so it doesn't extend below the base implant, the blocking voltage rises to 900 V, and when the CSL layer entirely removed from the structure the blocking voltage is 950 V. The oxide field at the centre of the JFET is below 3 MV/cm, so the breakdown voltage is determined by the electric field at the edge of the P-base region

under the trenches. The higher doping of the CSL layer is compared with the drift region produces a steeper gradient in the electric field just below the p base junction, resulting in a lower breakdown voltage. To increase the blocking voltage, either the doping or the thickness of the CSL region needs to be reduced. However, the purpose of the CSL layer is to spread the current from the JFET region more efficiently into the drift region, so reducing the CSL doping or thickness also increases the specific on-resistance. This trade off was investigated to find the optimum thickness of the CSL layer by maximizing the figure-of-merit $(V_{BR}^2)/R_{on,sp})$. Figure 3.11 shows the variation of $(V_{BR}^2)/R_{on,sp})$ vs. JFET width for different CSL thicknesses for a trigate device with a trench depth of 2 µm. The CSL thickness measured from bottom of the trench as shown in Figure 3.7. A total CSL thickness 0.6 µm provides the highest figure of merit for nearly all JFET widths. The CSL region below the P-base is not required in the trigate devices due the low drift resistance and sufficiently small cell pitch. However, when the cell pitch is high or the drift resistance is large the current spreading as the current exits the JFET region can be significant and a CSL layer is needed to reduce this resistance component.

To investigate further, the JFET width was held constant at 2 µm and the CSL thickness was varied to find the maximum figure of merit. Figure 3.12 shows the variation of specific on-resistance, blocking voltage, and figure of merit as a function of CSL thickness. The plot shows that the maximum figure of merit occurs at a thickness of 0.85 µm, but in this region the blocking voltage is very sensitive to CSL thickness. If for example the CSL thickness is slightly higher than the optimum of 0.85 µm, the breakdown voltage is drastically reduced. Therefore, it is better to select 0.6 µm, giving up a slight increase in figure of merit to make the blocking voltage less sensitive to variations in CSL thickness that may occur in a real device.

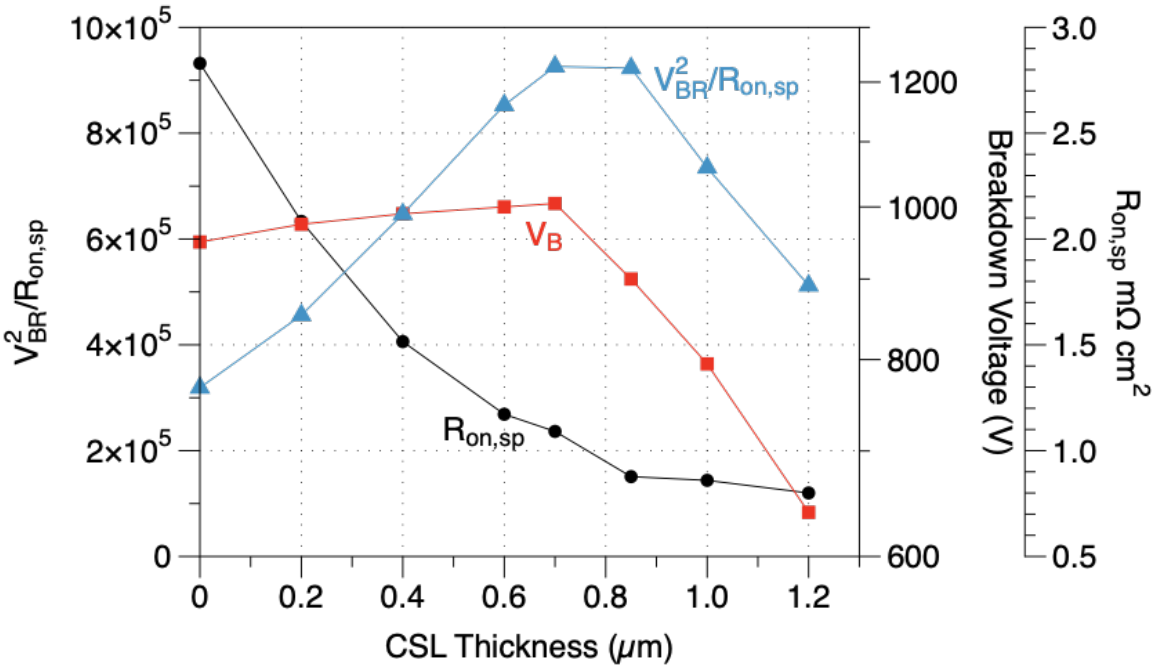


Figure 3.12.: Performance vs CSL thickness for a JFET width of 2.0 µm, trench depth of 2.0 µm and CSL doping of $1 \times 10^{17}\text{cm}^{-3}$.

3.5 Trigate Device Design and Mask Layout

Two important cross sections through the trigate MOSFET, along with some of the key dimensions are shown in Figure 3.13. Two blocking voltages are targeted where the trigate MOSFET will have a significant impact: (a) 650 V specification (930 V breakdown), and (b) 930 V specification (1,300 V breakdown). The corresponding drift regions will be (a) 5.4 µm, doped 1.4×10^{16} cm^{-3}, and (b) 8.4 µm, doped $1 \times 10^{16}\text{cm}^{-3}$. In both cases, the JFET region and current spreading layer will be doped 1×10^{17} cm^{-3}, with the latter extending 0.5 µm below the bottom of the P-base implant.

The devices will be fabricated on one quarter of a 4 inch SiC wafer, which was purchased from Cree, Inc. The overall mask layout including both the active trigate devices as well as the test structures are shown in Figure 3.14. Each wafer will be diced into quarters to accommodate the Karl Suss MJB-3 aligner's maximum 3 inch

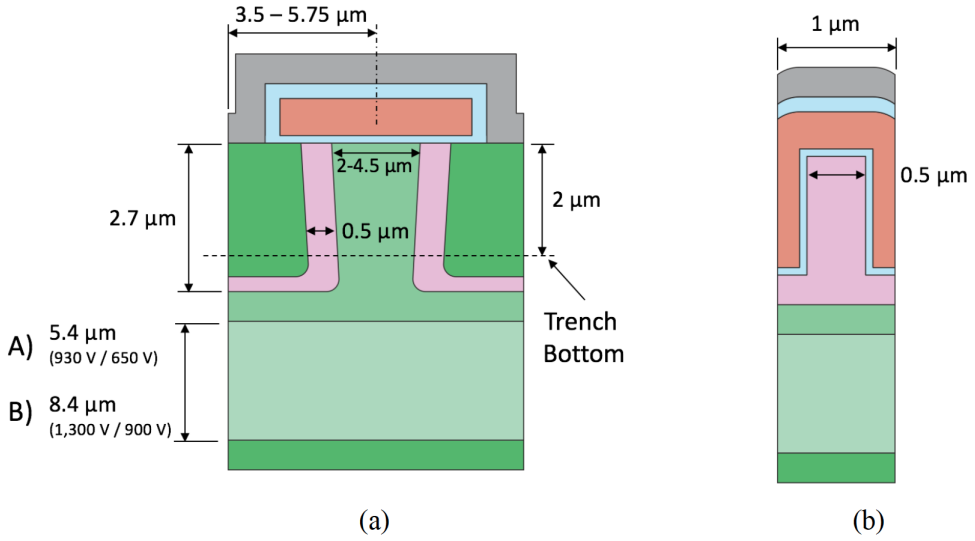


Figure 3.13.: Cross section of trigate MOSFET (a) through the fin centerline, and (b) perpendicular to the fin through the channel region.

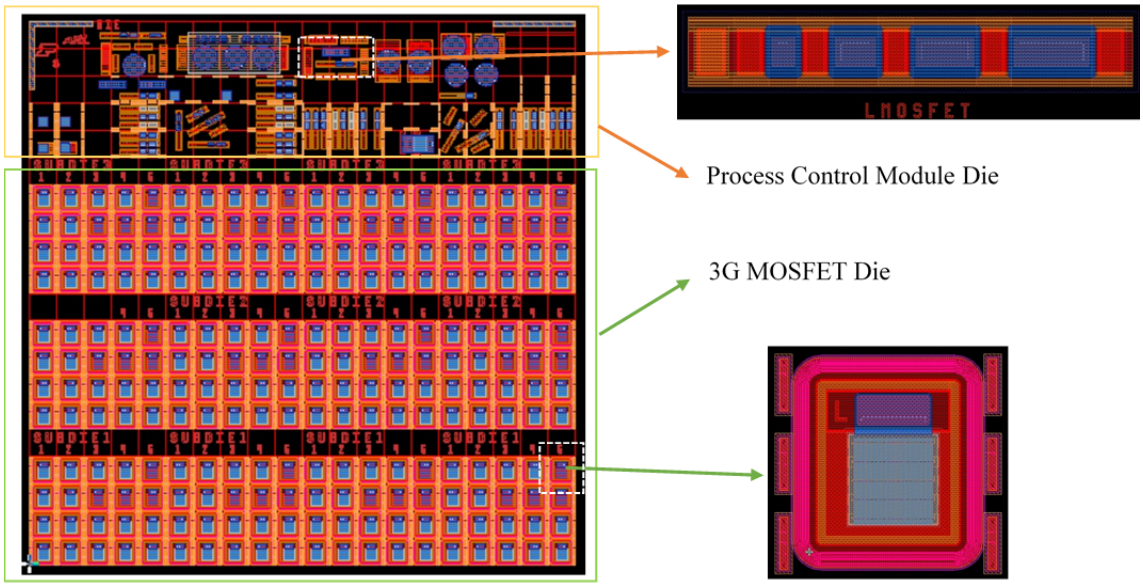
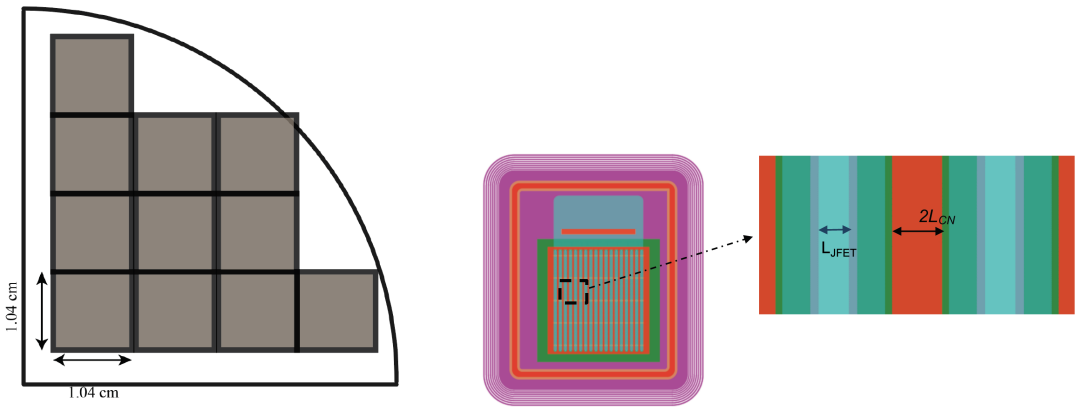


Figure 3.14.: The mask layout die containing both the device module and the process control module

sample size. Each die is 1.04 cm square, and a matrix of 11 die is included in each quarter, as illustrated in the Figure 3.15(a). Each of these die is then divided into

three rows of 1.3 mm sub-die. Each sub-die contains a 5x5 matrix of 520 µm square write fields. Each device is contained within a single write field, corresponding to smallest write field for the electron beam lithography system available at the time of the design. The overall layout of die is shown Figure 3.15.



(a) (b)

Figure 3.15.: Mask layout of trigate devices (a) Die distribution in a wafer quarter (b) Device module parameter definition.

Every die contains two modules —a **device module** and a **process control module** (PCM). The features in the device module can be classified into two broad categories. The areas containing features with minimum dimensions less than 2 µm are considered "fine" category, and will be written by e-beam lithography. All other areas will be defined by optical lithography. In some cases, for an example the gate layer, the features require both e-beam and optical lithography. To insure a smooth transition, the e-beam features are overlapped with an optically defined layer by 5 µm.

The device module contains active devices in various combinations. Based on the 3D simulations of the trigate described in the previous chapter, the optimum JFET width L_{JFET} is approximately 3.5 µm. To verify this experimentally, six devices with JFET widths ranging between 2.0 and 4.5 µm, in steps of 0.5 µm are included in the device module. Based on the discussion in Section 2.2.2.1, a 0.5 µm source

Table 3.1.: Variation of JFET width and contact length within die

JFET Width	Contact Length L_{CN}	
	0.5 μm	1.5μm
2.0μm	Device 1	Device 2
2.5μm	Device 3	Device 4
3.0μm	Device 5	Device 6
3.5μm	Device 7	Device 8
4.0μm	Device 9	Device 10
4.5μm	Device 11	Device 12

ohmic contact width L_{CN} will provide sufficiently low contact resistance. However, alternative devices with a L_{CN} = 1.5 µm are also included in case of higher than expected contact resistivity. The resulting cell pitch will range from 3.5 to 5.75 µm. The different variations of these parameters included in the design are listed in the Table 5.1. Figure 3.15(b) shows where JFET width and source contact lengths are measured on the mask.

Our device is designed to fit within a single 524 µm square sub-die, corresponding to the smallest write field area of the electron beam lithography tool available at the time the mask was designed. Each combination of L_{JFET} and L_{CN} described above will be fabricated, for a total of 12 devices in each die, as illustrated in Figure 3.16.

The mask layouts for both optical and electron beam lithography were prepared using the Pyxis layout tool from Mentor Graphics. Fabrication of the trigate MOSFET involves a total of 14 mask layers with 11 optical and 3 electron beam lithography steps. The major mask layers used in the fabrication of the trigate DMOSFET are described below.

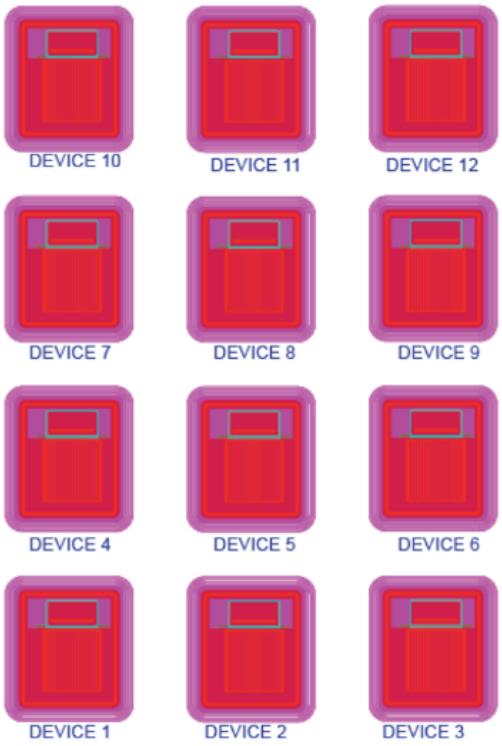


Figure 3.16.: Test die layout including variations in JFET width L_{JFET} and source contact length L_{CN}.

Mask 1: P-Well Implant

The first step in the trigate MOSFET fabrication process is to define the P-well, having a 2.7µm junction depth and a surface doping of $2 \times 10^{17}\text{cm}^{-3}$. This is done by high energy Al ion implantation using polysilicon as the implant mask. The P-well implant mask is shown in Figure 3.17.

A series of P-well implants will be included at the periphery of the device to form a floating-field-ring (FFR) edge termination. As an alternative, an option to use a simple trench termination, which would involve removing all material adjacent to the device to a depth of approximately 1/3 of the drift layer thickness is also included. This etch would be inset from the edge of the floating-field-rings so that either technique may be applied. The floating-field-ring termination consists of eight concentric rings

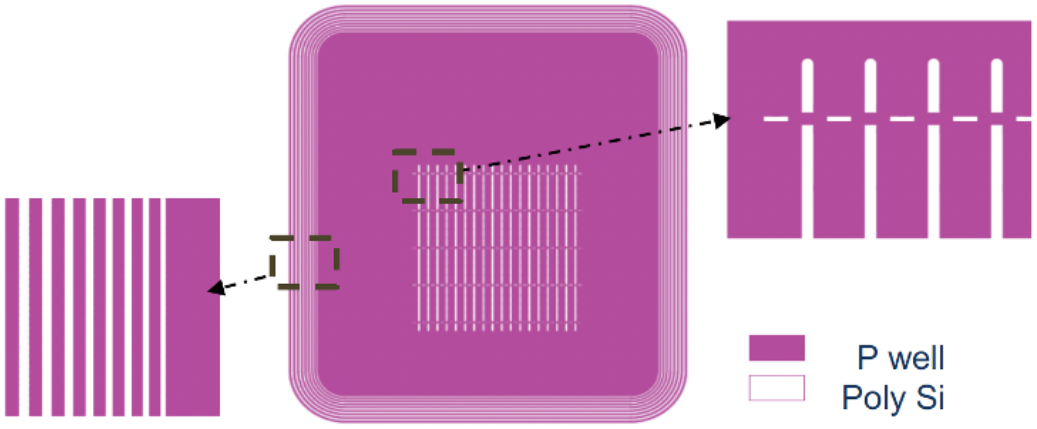


Figure 3.17.: P-well implant mask. The left-hand detail shows the floating field-ring edge termination, and the right-hand detail shows the interior of the active device. Aluminum will be implanted in the purple-shaded regions.

with an initial spacing of 1.0 µm and width of 2.25 µm. The spacing and width increase by 5% in each subsequent ring, and the entire array extends beyond the edge of the P-well by approximately 3× the drift layer thickness, or ∼30 µm.

Mask 2: N Implant-Allow

After P-well implantation, the existing polysilicon implant mask is oxidized, expanding the pattern by 0.5µm on each side. The expanded mask will then act as a mask for the self-aligned N^+ source implantation in the active area. This self-aligned process will result in a nominal channel length of 0.5µm. The depth of this nitrogen implant will be 2.2µm. To prevent unwanted nitrogen implants in the areas outside the active area, an additional implant mask of thick electroplated or sputterd metal will be deposited. An alternative is using SU-8 photoresist that can be applied using conventional optical lithography. Since the drawn regions of this mask are the areas where the nitrogen implant is desired, this mask is referred to as the "N-Allow" mask.

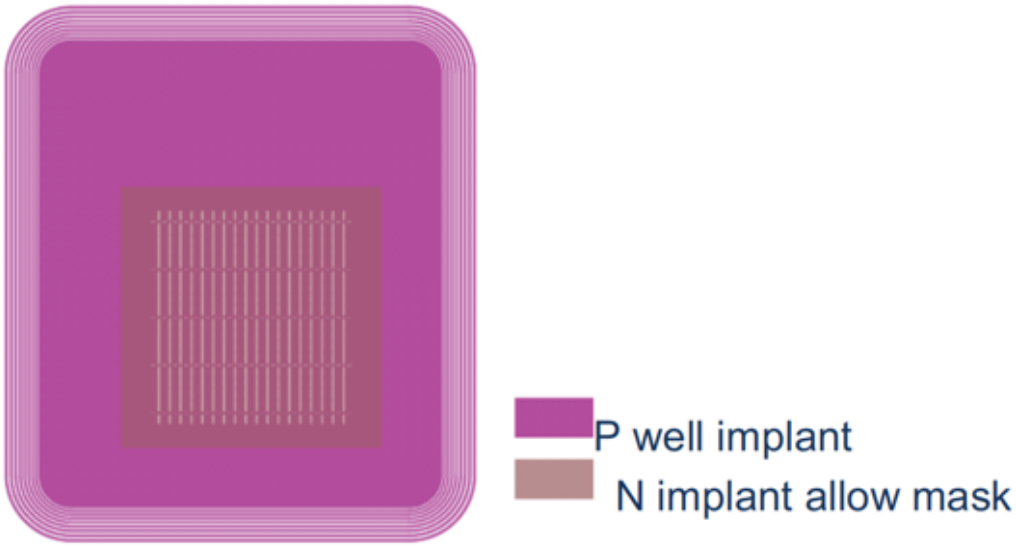


Figure 3.18.: N-implantation is allowed inside the light red region, where it is self aligned to the P-well implant to form the 0.5 µm channel.

The N-Allow mask is shown in Figure 3.18. With the N-Allow mask and the expanded polysilicon P-well mask in place, the high-energy nitrogen implant can be done. The implanted regions are illustrated in Figure 3.19.

Mask 3: P^+ Implant

To prevent the P-well from floating to an undefined potential, it is necessary to tie them to the source with an ohmic contact. This is accomplished by performing a P^+ implant after the source and P-well masks are removed. Since this is a shallow implant and will be done on a planar surface, the Ni implant mask will be formed by ebeam liftoff lithography.

Figure. 3.20 shows the mask layout of a trigate device and the P^+ contact area both in the field and active area. In the field area, an 18 µm wide P^+ guard ring surrounds the active area, while a series of P^+ stripes each 4 µm wide is patterned inside the active area. The number of stripes is kept at a minimum as it consumes

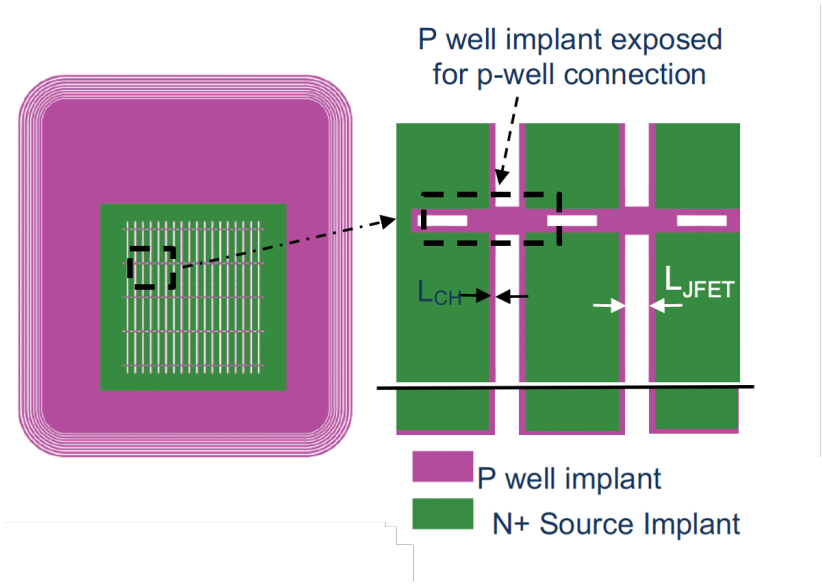


Figure 3.19.: Top view of the active region where he N^+ source implantation goes into the green regions. The P-well underlines the N^+ implants.

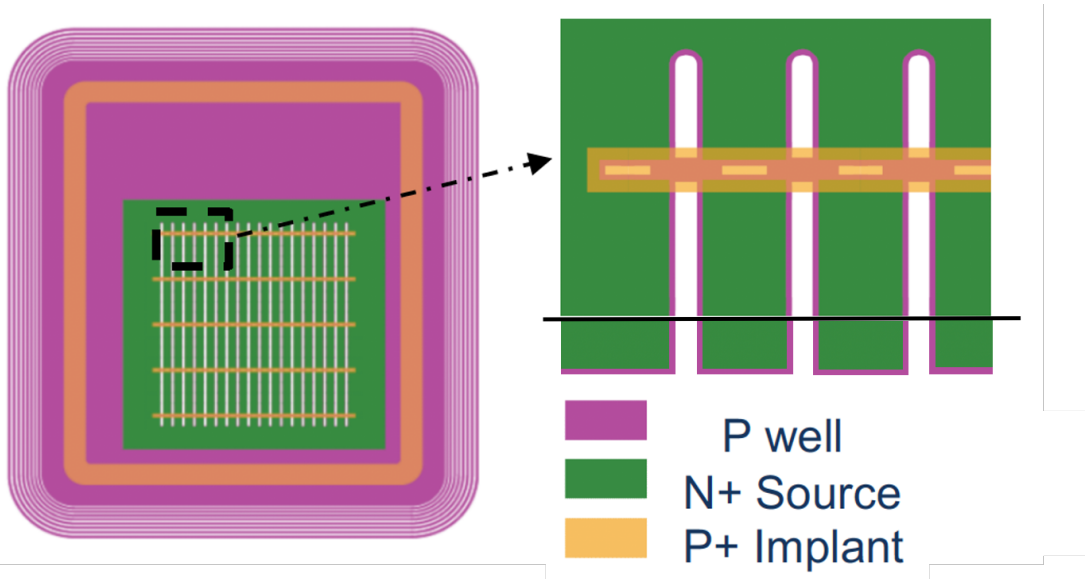


Figure 3.20.: The P^+ contact implant region is shown in gold. The detail at the right shows P^+ contact stripes running across the active area to ground the P-well.

active area of the transistor. In our design, the adjacent stripe separation is 40 µm,

and there are five P^+ stripes in the 0.04 mm^2 (200µm × 200µm) active area as shown in Fig. 3.20.

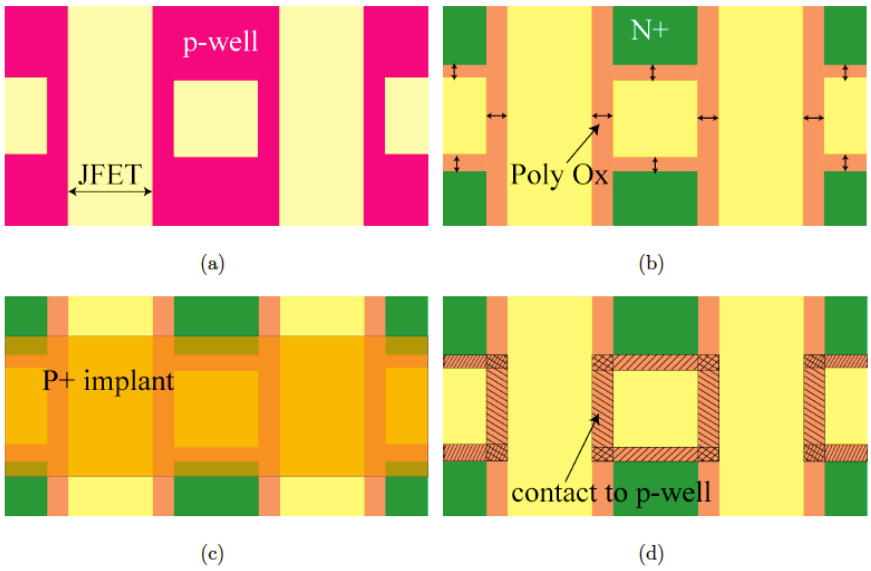


Figure 3.21.: P^+ implant formation (a) P-well implant and JFET region; (b) self-aligned 0.5 µm poly oxidation and source implantation; (c) P^+ implantation, and (d) P^+/P-well overlap region.

The contact areas in each stripe are defined from the P-well implantation mask pattern as shown in Figure 3.21(a). Here, the polysilicon mask defines the JFET region in P-well implantation process. In the P^+ stripe area, a shorter isolated polysilicon block has been patterned with a space of 1 µm from the adjacent JFET finger. The spacing between the poly block to the JFET finger is sealed during the 1 µm poly oxidation before the nitrogen implant as seen in Figure 3.21(b). Therefore this region does not receive the n-source implant but does receive the P-base implant. The P^+ implant is allowed along the orange stripe as shown in Figure 3.21(c) and contacts the P-base regions at the surface. The shaded region in Figure 3.21(d) shows the overlap between the P^+ implant and the P-well region.

To further illustrate the P^+ contact in the trigate device, a cross-section along the P^+ implant strip is shown in Figure 3.22. As seen in the figure, the adjecent P-wells

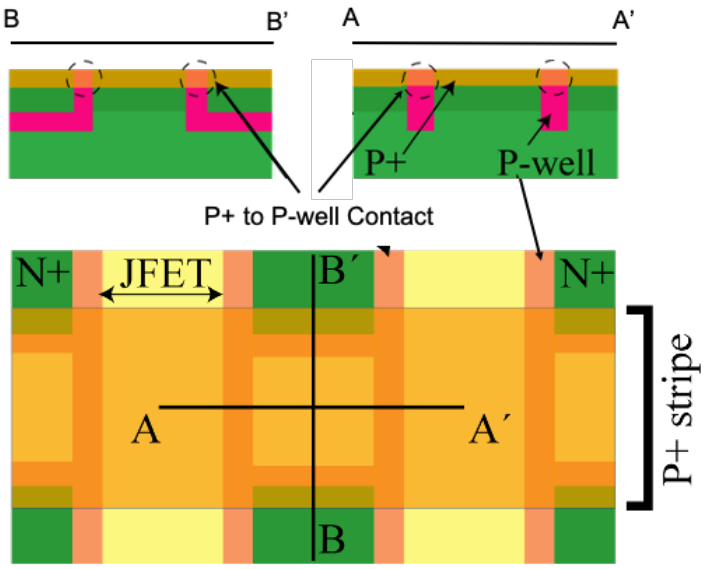


Figure 3.22.: P^+ implant strip in the active area of the trigate DMOSFET and cross-section view to illustrate the overlap of the P^+ and P-well regions.

are connected by the P^+ implant at the surface. An ohmic contact is then formed at the surface over the P^+ region. The top metal which is then deposited over the active areas connects the P^+ and the source.

Mask 4: Trench Etch

The trenches of the trigate structure run perpendicular to the gate and source fingers, and are 0.5 µm wide, spaced 0.5 µm apart. Trench RIE will be masked with a 150 nm Ni metal layer defined by e-beam lithography using the features illustrated in Figure 3.23.

Mask 5: Field Oxide

After the trench etch is performed, an optional process is the field oxide. Here, a 1 µm thick SiO_2 layer can be deposited over the entire sample. However, the oxide needs to be removed in the active area by wet etching and therefore a mask

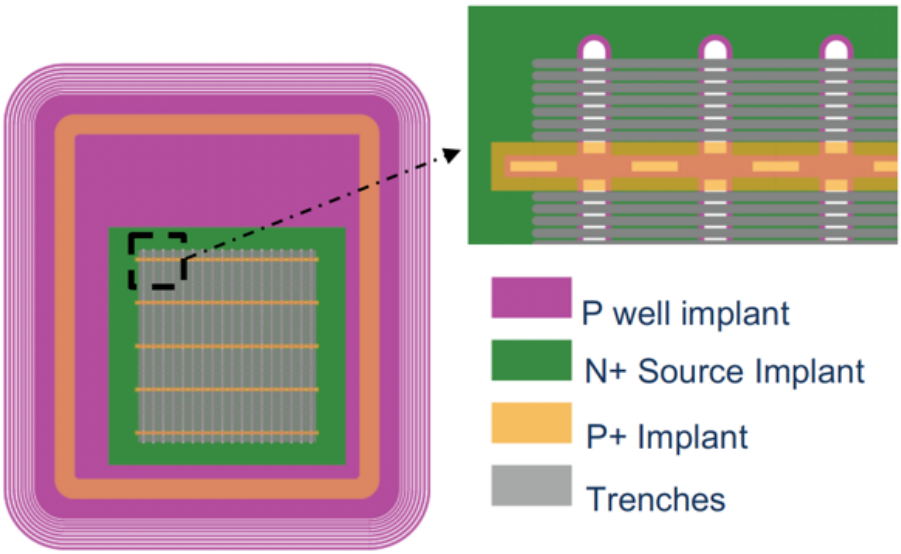


Figure 3.23.: Trench mask showing 0.5 µm wide trenches running horizontally.

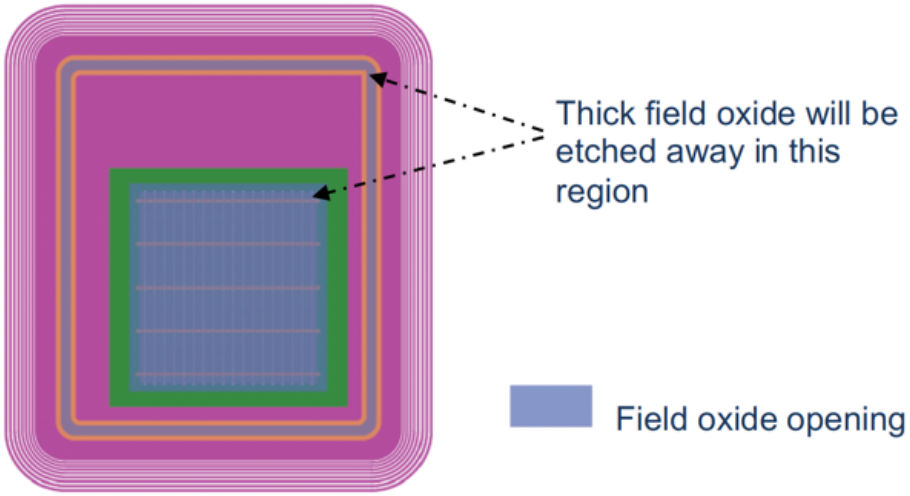


Figure 3.24.: Field oxide will be removed in the blue-shaded regions.

is required to form a window around the active area using photolithography as seen using in Figure 3.24. The field oxide passivates the SiC surface outside the active area and provides a thick oxide under the gate probe pad to prevent gate-to-source shorts during probe testing or wire bonding.

Mask 6: Gate Etch

The next step after the trench etch and field oxide is the gate stack process. The only step in the gate stack process that requires a mask to be included in the layout is the patterning of the polysilicon gate runners. Here, the heavily doped polysilicon gate is etched by RIE using the BOSCH process to form gate runners that run perpendicular to the trenches. The alignment of the gate to the source is extremely critical and therefore the patterning of the gate runners is done using e-beam lithography. The gate fully covers the JFET and channel regions, and overlaps the source region by 0.5 µm as illustrated in Figure 3.25.

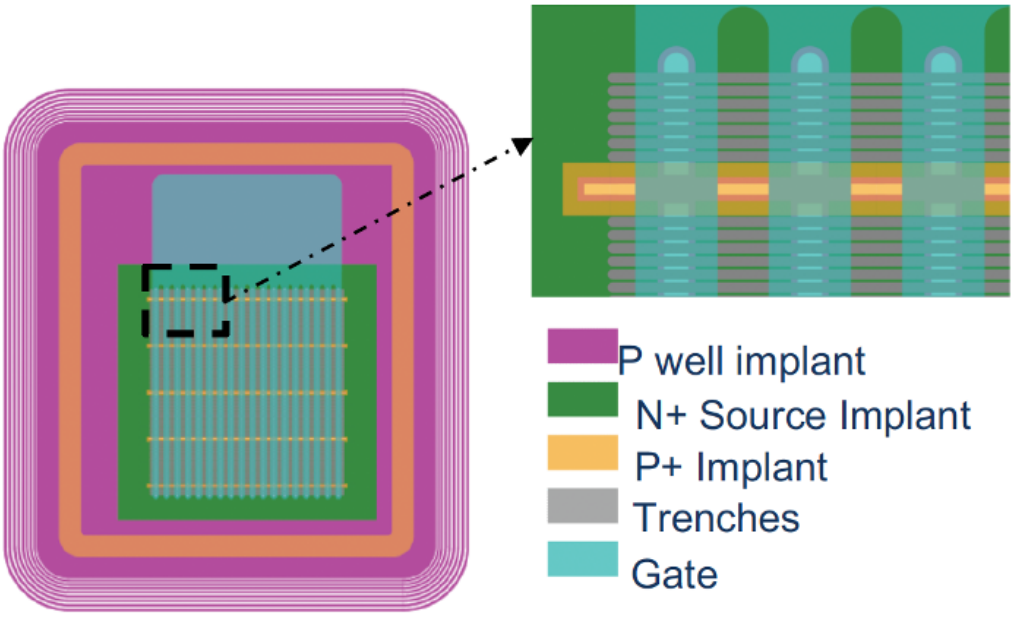


Figure 3.25.: Etched polysilicon gate, shown in light blue. The detail on the right shows the gate runner in the active area.

Once the gate runners are patterend, a self aligned process is used to form the source contact and therefore no mask layer is required. After the defining the polysilicon gate, the polysilicon is thermally oxidized to form a 1 µm intermediate-layer

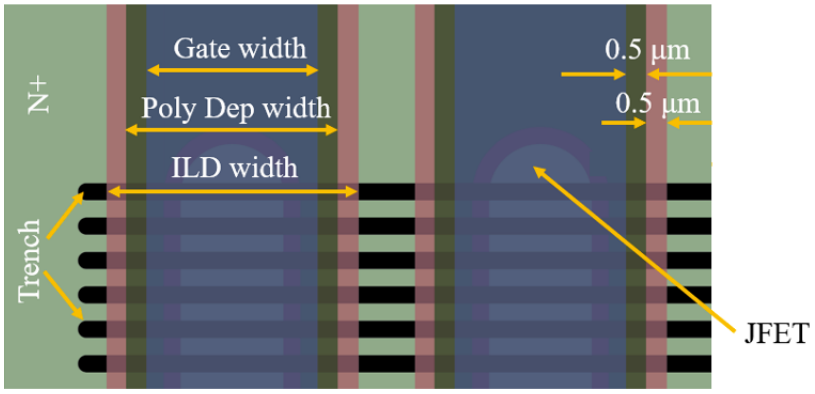


Figure 3.26.: Design and expected dimensions of the trigate MOSFET active area after the ILD oxidation.

dielectric (ILD) that surrounds the gate and insulates it from the source as seen in Figure 3.26.

Mask 7: Ohmic contact

The thin oxide that forms in the source contact areas during the ILD oxidation is removed by a short BHF dip without the need for lithography. This insures that the source ohmic metal is self-aligned to the edge of the gate, while the thicker ILD covering the polysilicon gate insulates it from both the source ohmic metal and top metal. This process minimizes the spacing between the source ohmic contact and the gate, thereby reducing the cell pitch.

Nickel is deposited on the top side by e-beam evaporation or sputtering, and patterned by optical lift-off lithography to form source and gate ohmic contacts. Back-side ohmic metal is deposited immediately after the top-side ohmic metal. The samples are then annealed, forming nickel silicide (NiSi) ohmic contacts to the N^+ source, P^+ base contacts on the top side, and the N^+ drain on the back side. The same mask is then re-used to define a thicker layer of metal on the top side for probe testing or wire bonding. Thick metal is also deposited on the back side. The ohmic metal mask is shown in Figure 3.27.

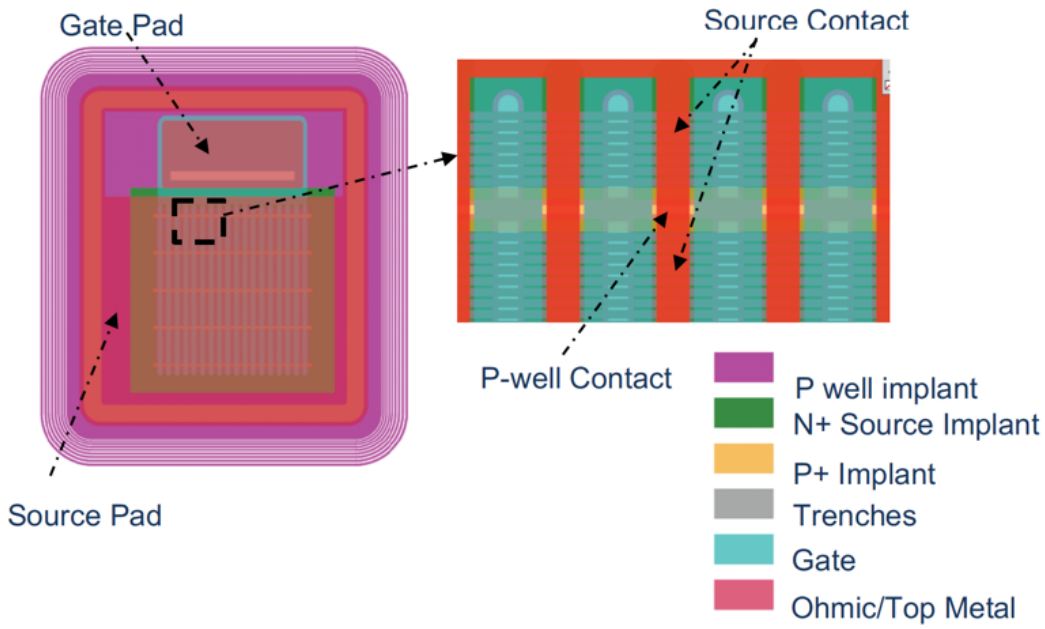


Figure 3.27.: Ohmic contacts and top metal mask.

Mask 8: Gate Contact Window

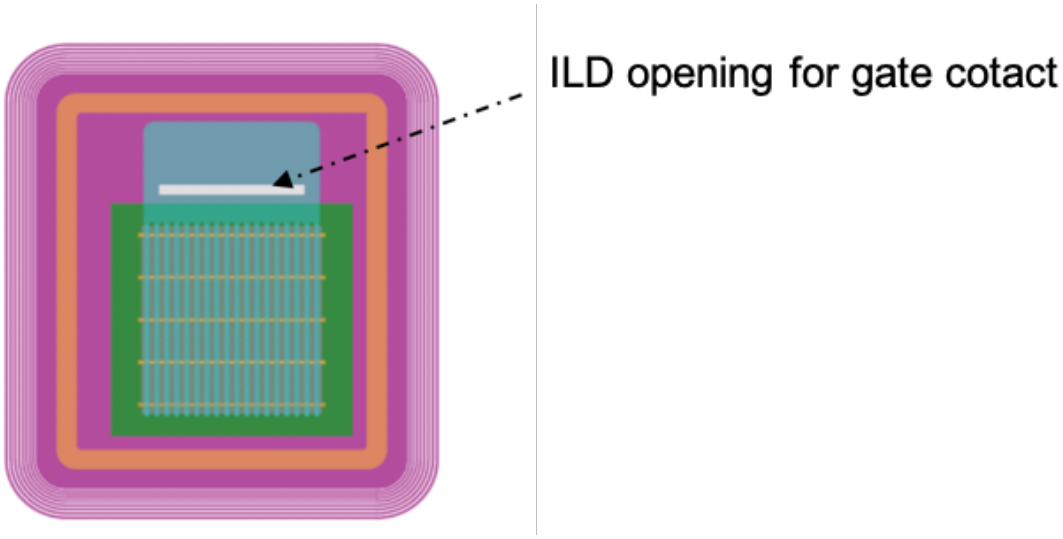


Figure 3.28.: Interlayer dielectric is removed in the white shaded region to provide contact to the gate polysilicon.

Once the ohmic anneal process is complete, an opening in the ILD over the gate contact is made to access the underlying polysilicon gate as seen in Figure 3.28. This can either be done using an oxide RIE or wet etch. Sufficient margin is provided in the mask to accommodate any lateral etch of the oxide in case of a wet etch. The top metal bonding pad lies over ILD, the polysilicon gate pad, and the field oxide, and connects to the underlying polysilicon through the gate contact window in the ILD. The ILD window is made narrow so that a thick ILD remains under the metal bond pad. This helps prevent damage to the underlying field oxide that could create a gate-source short.

Mask 9: Top Metal

The last step in the process is the deposition of top metal. A metal stack consisting of 30 nm of titanium and 1.2 µm of gold is sputtered over the entire sample. The top metal is then patterned using a wet chemical etch to isolate adjacent devices both in the active area as illustrated in Figure 3.29

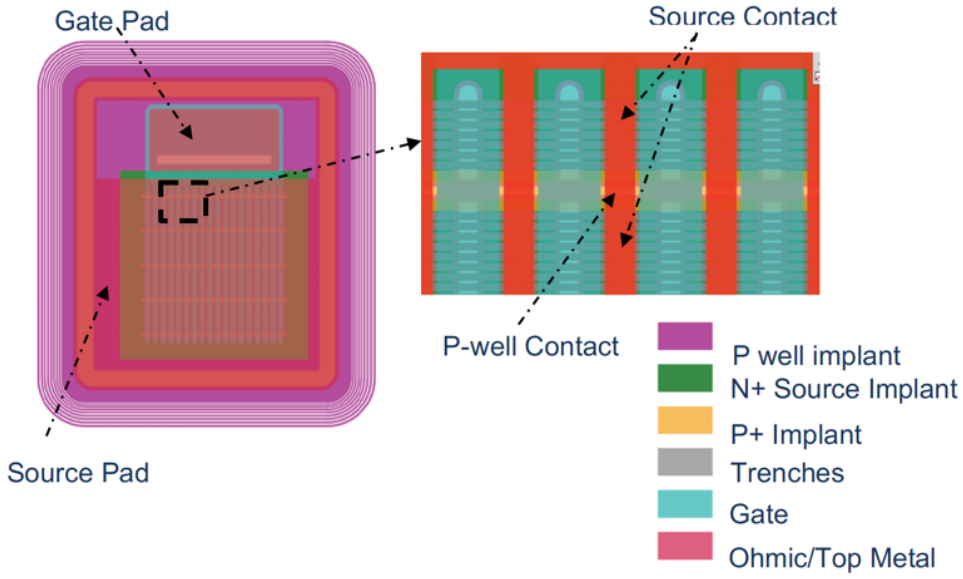


Figure 3.29.: Top metal mask that is used to isolate adjacent devices in the active area.

Process Control Modules and Test Structures

The process control module (PCM) consists of test device structures that are each uniquely designed to verify a particular step in the trigate MOSFET fabrication process. The 3D geometry of the trigate structure requires test devices on the top, bottom, and sidewall surfaces to extract information such as mobility and contact resistance. The PCM includes TLM, MOSCAP, MOSFET, interlayer dielectric (ILD) breakdown, and P-well spacing test devices. Some of the PCM devices contain e-beam defined features, and these are contained within the minimum write field of 520 µm square. A comprehensive list of the PCM testers, their placement, and utility is provided in Table 3.2.

Table 3.2.: List of test structures in process control module region of the trigate mask layout.

Test Device	Layer	Top	Bottom	Trench	Primary Purpose
TLM	N^+	✓			Source ohmic contact resistance
	N^+	✓			P+ ohmic contact resistance
	P-Well	✓			P-Well sheet resistance
	Doped Polysilicon	✓			Polygate sheet resistance
MOSCAP	N^+	✓	✓	✓	Oxide breakdown field
	P^+	✓			Oxide breakdown at the P^+ / gate overlap
	N-CSL	✓	✓	✓	MOS interface properties (D_{it},Q_F, etc)
	P-Well	✓	✓	✓	MOS interface properties and oxide breakdown field(especially at trench bottom)
		✓			Gate controlled diode
Lateral MOSFET	P-Well	✓	✓		Channel mobility on top and bottom surface
				✓	Devices with varying ratio of planar width to sidewall width to determine channel mobility on sidewall and bottom surface.
P-well Array	P-Well	✓			P-well with different spacing to determine lateral straggle.
ILD Breakdown	ILD	✓			Breakdown strength of the interlayer dielectric spacer.

4. FABRICATION OF SIC TRIGATE MOSFETS

Utilizing the mask layout and device design described in the previous chapter, the fabrication of the vertical trigate power MOSFET is described in this chapter. The trigate MOSFET can be viewed as a DMOSFET with trenches in the active area. Therefore, some of the existing process technology developed and widely used for SiC planar DMOSFETs and UMOSFETs can be readily adapted for the fabrication of the trigate device. For example, an optical micrograph image of the active area of a conventional DMOSFET is shown in Figure 4.1(a). Here, interdigitated source and gate fingers run vertically, and the granular fingers are the annealed Ni ohmic contacts to the N+ source regions. In this view, the modification for the trigate MOSFET involves etching narrow fins and trenches in the SiC in the horizontal direction, perpendicular to the source and gate fingers as shown in Figure 4.1(b). The trenches are etched prior to gate oxide formation, and therefore all subsequent fabrication steps will involve this three dimensional topology. Therefore, the process flow for the trigate MOSFET requires rigorous development of new process technology, some of which has never been applied to SiC power MOSFETs.

In this chapter, the fabrication of the trigate devices is discussed in two sections:

1. Process technology development

2. Process integration into single trigate MOSFET process flow

In the first section, the development of the critical unit steps that are the building blocks of the trigate devices is discussed. The process for each of these steps are developed independently and each step consists of several process parameters and therefore the process development involves optimization of these parameters by fabrication of test samples. Measurement and analysis of the test samples are done and the process is repeated until an optimal condition is reached. In the second section,

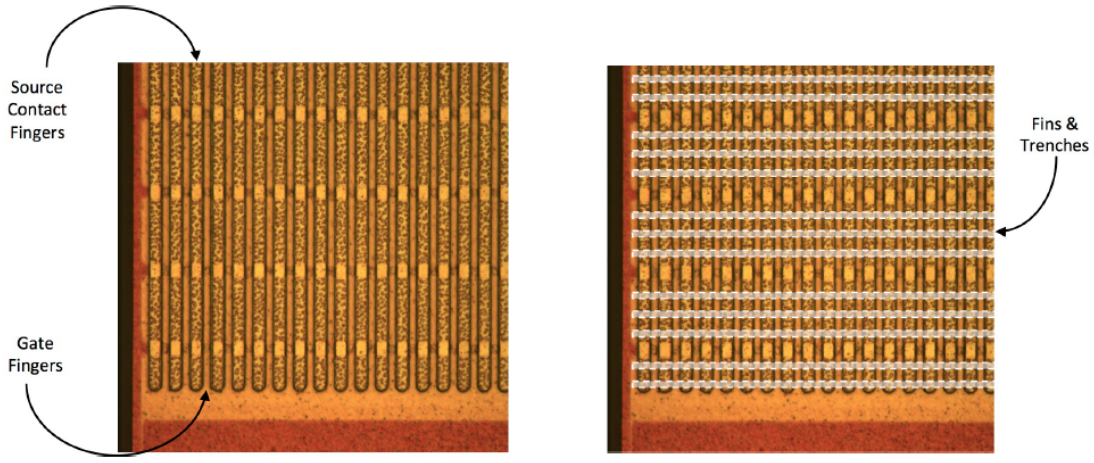


Figure 4.1.: Photo of a conventional planar DMOSFET (left) and the same device with fins and trenches etched across the source and gate fingers (right). The structure on the right is the proposed trigate (3G) MOSFET.

the integration of the individual unit steps into a single process flow that is applied to the fabrication of functional trigate devices is described.

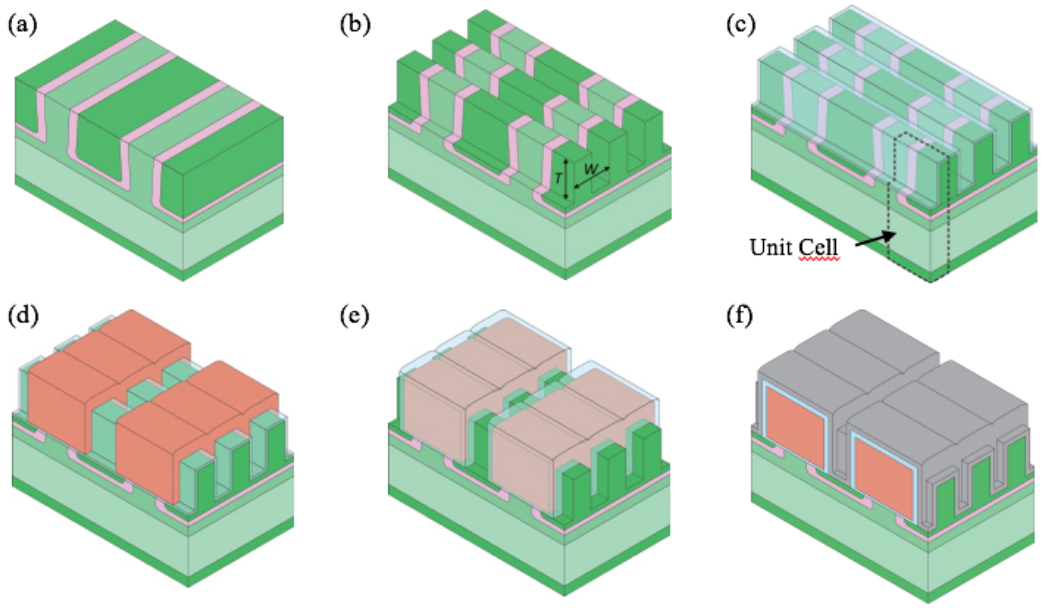


Figure 4.2.: Steps in the fabrication of the trigate power MOSFET: (a) implant P-base and N+ source using a self-aligned process, (b) etch trenches perpendicular to the source stripes, (c) deposit gate oxide and anneal, (d) deposit and dope polysilicon gates to fill the trenches, then pattern poly into stripes, (e) form a thick oxide over the gates by thermal oxidation and clear the oxide over the exposed SiC by a short BHF dip, (f) deposit ohmic metal and anneal to form source and base contacts, then deposit top metal over entire active area.

4.1 Process technology development

The main fabrication challenges of the trigate structure are: (1) masking deep, high energy source and base implants, (2) forming vertical trenches with the required dimensions, (3) forming a conformal oxide with uniform thickness on top, sidewall, and bottom surfaces, (4) filling the trenches with polysilicon, (5) patterning gate fingers over the fins and trenches, and (6) opening windows in the dielectric for the source contact stripes using a self-aligned process. The main fabrication steps of the trigate MOSFET process are depicted in Figure 4.2. Key unit steps that require significant process development are identified as follows:

1. High energy ion implantation and masking.
2. SiC trench etch
3. Gate stack for the trigate geometry
   (a) H_2 etch of SiC trenches.
   (b) Conformal gate oxide over trenches.
   (c) Gate polysilicon deposition: Trench fill and planarization
   (d) Gate polysilicon doping
   (e) Polysilicon gate etch and alignment.
4. Ohmic contacts over trench geometry

4.1.1 High energy ion implantation and masking

The N+ source and P-base regions of the conventional power DMOSFET in Si are formed by the diffusion of n- and p-type impurities applied through the same mask. As diffusion rates of impurities are significantly lower in SiC [7], the impurities are instead introduced using ion implantation. For a typical SiC DMOSFET, the P-base junction is about ∼0.5 µm deep and an aluminum ion implant with a maximum energy of 320 keV with the appropriate dose is required to form the P-base. The trigate device however, has trenches in the active area which need to lie inside the P-base region so that an inversion channel can be formed on the top and sidewalls of the trench. Therefore, the trigate MOSFET requires deep P-base and source regions that extend below the bottom of the trench. This is accomplished by high energy implantation in the MeV range, which poses a major challenge in the development of the trigate MOSFET process, since such high energy implants are being used in a SiC DMOSFET for the first time. In this section, the design, calibration and process development of the ion implantation and masking process for the P-base, N+ source, and P+ regions are described.

4.1.1.1 Design of high energy implants for the trigate MOSFET

Implantation profiles in SiC can be predicted by Monte-Carlo simulations performed using tools such as SRIM/TRIM [97] and Sentaurus Process. Initial design of the required implant profiles was performed using profiles calculated as Pearson IV distributions using moments from Janson *et al.* [98].

Calibration of high energy implants

As mentioned earlier, the deepest implants require MeV implantations, both for aluminum to form the P-base, and nitrogen to form the N+ source. The Janson model [98] was developed using secondary ion mass spectroscopy (SIMS) data from relatively low energy implants. Therefore the first step was to verify and calibrate the model with experimental data from high energy deep implants.

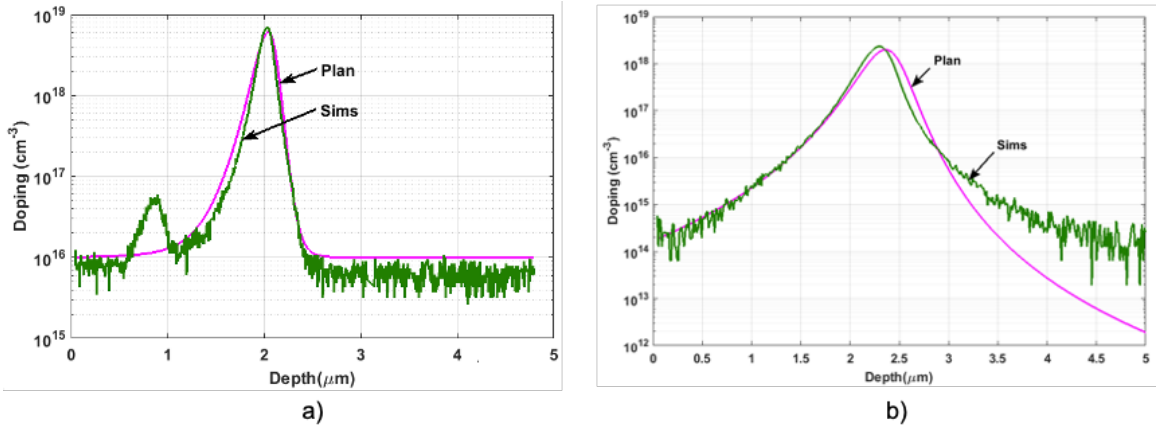


Figure 4.3.: Calibration of high energy implants with measured SIMS profiles. The purple lines are predictions using the Janson model [98], and the green curves are the measured profiles a) Implant profile of Al in SiC at a dose of 7.73×10^{13} cm^{-2} and an energy of 4.25 MeV, b) Implant profile of N in SiC at a dose of 1.35×10^{14} cm^{-2} and energy of 3.0 MeV.

Two calibration samples with an N-type SiC epilayer doping of 1×10^{16} cm^{-3} were prepared for aluminum and nitrogen implantation with energies 4.25 and 3.0 MeV, respectively. For this test we only implanted the highest anticipated energy to verify the depth and profile in SiC. The samples were first cleaned using the RCA procedure, and a 20 nm sacrificial oxide was grown by thermal oxidation. The samples were then implanted at room temperature by Ion Beam Services (IBS) of Peynier, France. The doses were 7.73×10^{13} cm^{-2} and 1.35×10^{14} cm^{-2} for Al and N respectively, corresponding to peak dopant concentrations of 2×10^{18} cm^{-3} for Al and 6×10^{18} cm^{-3} for N. After implantation, the samples were sent to Evans Analytical Group for SIMS profiling. Figure 4.3 shows the measured SIMS profile of the implants in SiC along with the predicted profile using the Jason model [98]. The model closely matches the measured profile for both aluminum and nitrogen implants, and therefore the model can be used with confidence to design the high energy implants needed in the trigate MOSFET.

Design of the P-type base implant

The standard DMOSFET utilizes a retrograde profile [58] in the P-base region, allowing the channel to have a suitably low doping concentration ($\sim 2 \times 10^{17}$ cm^{-3}), while providing sufficient punch-through protection with a higher concentration near the base-drift junction. The same effect is accomplished in the trigate device by using a box profile through and below the fin, followed by a single energy "base stop" implant of higher ($\sim 2 \times 10^{18}$ cm^{-3}) peak concentration. The base stop implant needs to be located below the bottom of source under the trenches and therefore is the highest energy implant in the implant schedule of the trigate device. The background doping of the substrate is the CSL epilayer doping of $\sim 1 \times 10^{17}$ cm^{-3} and therefore an average doping of 3×10^{17} cm^{-3} in the aluminum implanted box profile for the P-base region is required. The total dose of the P-base implant is therefore 1.3×10^{14} cm^{-2}.

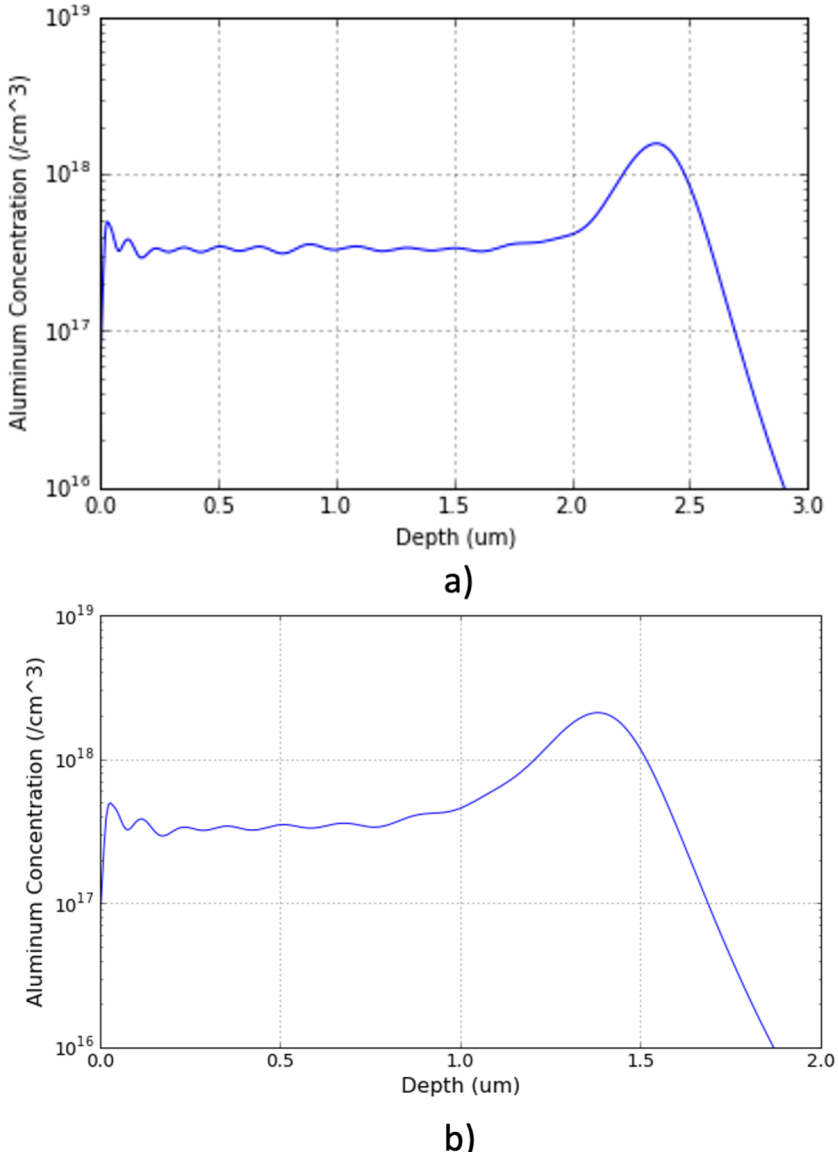


Figure 4.4.: Complete aluminum implant (P-base) profile for the trigate MOSFETs a) Gen-1 with 2 µm trench depth, b) Gen-2 with 1 µm trench depth.

The above features have been incorporated in the trigate samples. The Gen-1 trigate devices have a 2 µm trench depth, while the Gen-2 devices have a trench depth of 1 µm and their respective P-base implant profile are shown in Figure. 4.4. The P-base implant schedules for the Gen-1 and Gen-2 samples are listed in Table 4.1 below.

Table 4.1.: P-type Base aluminum implant schedules

Trigate Gen-1		**Trigate Gen-2**	
Energy (keV)	**Dose** (cm^{-2}) $\times 10^{12}$	**Energy (keV)**	**Dose** (cm^{-2}) $\times 10^{12}$
20	0.80	20	0.8
40	1.50	40	1.5
100	3.00	100	3.0
200	3.40	200	3.4
320	4.25	320	4.25
480	5.10	480	5.10
680	5.95	680	5.95
950	6.80	950	6.80
1250	6.80	1250	6.80
1600	6.80	1800	7
2000	7.32		
2500	7.32		
3000	7.32		
4248	60		

Screen Oxide

A sacrificial screen oxide is typically utilized on the SiC surface during the implantation process. The screen oxide mainly serves two purposes: 1) it absorbs secondary metallic ions introduced during the implantation and maintains a clean SiC surface and 2) it shifts the peak of implant and absorbs the low concentration tail that occurs near the surface. The P-base implant in SiC without a screen oxide is shown in Figure 4.5 and a low energy tail is observed near the surface. The inversion layer of the MOSFET is formed at the surface of the base region and therefore control of the doping in this region is important. Another important function of the sacrificial

screen oxide is that it acts as an etch stop during the polysilicon implant mask etch that is described in the process development section.

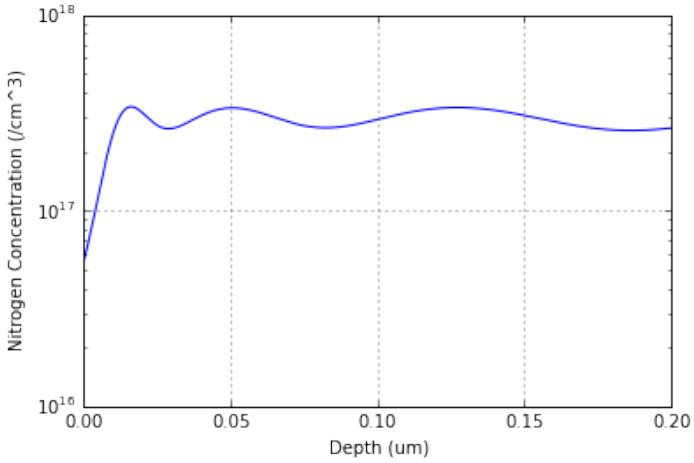


Figure 4.5.: Aluminum P-well implant profile at the surface of SiC without a screen oxide showing the tail of the low energy implant near the surface.

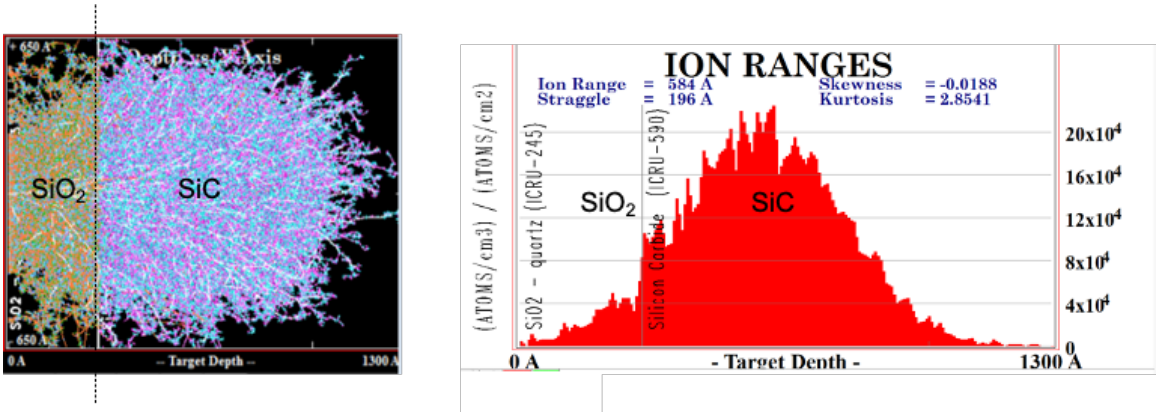


Figure 4.6.: Monte Carlo simulation of an aluminum implant using TRIM [97] with 30 nm SiO_2 screen oxide and an implantation energy of 20 keV

Monte Carlo simulations of the implants were performed using TRIM to determine the thickness of the oxide that should be used to absorb this low energy tail. As seen in Figure 4.6, 30 nm of screen oxide is sufficient to absorb the implant tail at the

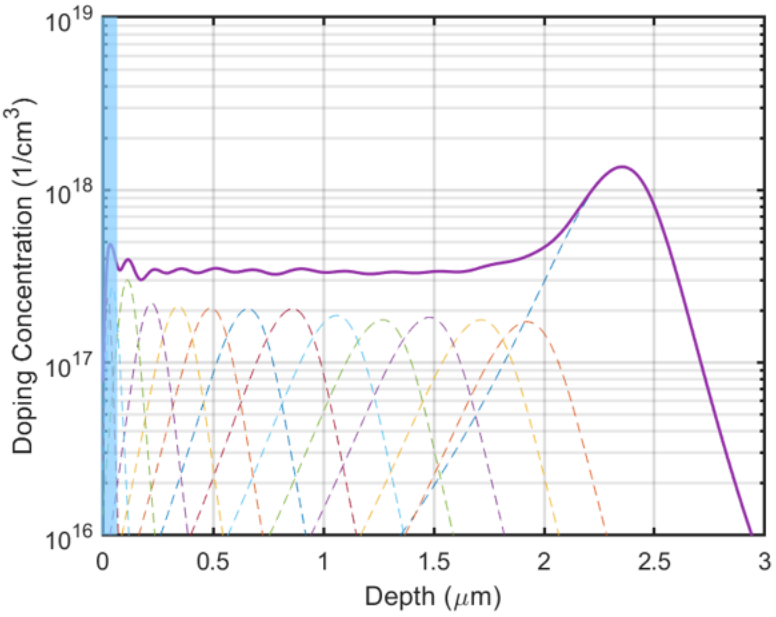


Figure 4.7.: Aluminum P-well implant profile. The dashed lines show the profile of each individual implant energy, while the solid line shows the resulting total concentration profile. The blue region represents the screen oxide

surface and produces a constant doping profile up to the surface of the SiC when the minimum implantation energy is 20 keV. The resulting base implant profile of the Gen-1 trigate is shown in Figure 4.7.

Design of the N+ source implant

The source implant presents a more challenging design problem. While the implant only has to extend ∼0.25 µm below the bottom of the trench, it needs to be of sufficiently high concentration to 1) counter-dope the base implant, 2) provide sufficiently low resistivity to minimize source spreading resistance, and 3) be sufficiently high concentration to provide a low contact resistance.

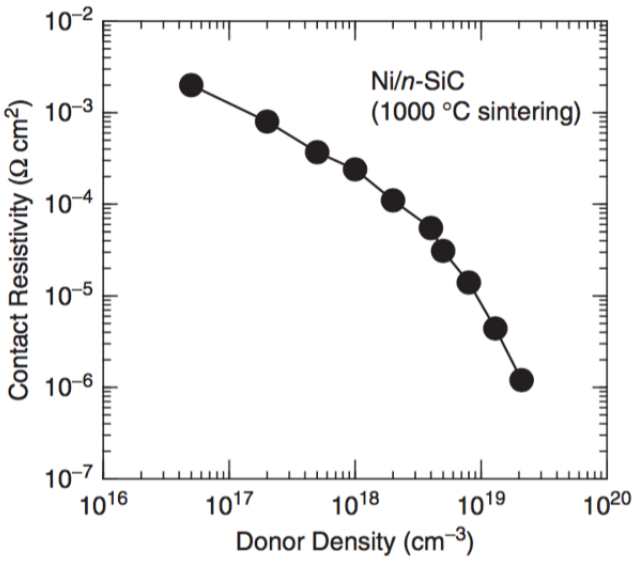


Figure 4.8.: Nickel silicide contact resistivity to N+ SiC [30]

Figure 4.8, reprinted from [30], shows that obtaining a contact resistivity below $1 \times 10^{-6}\Omega\text{cm}^2$ requires about 2×10^{19} cm^{-3}. The source-base junction depths are 2.2 µm and 1.2 µm for the Gen-1 and Gen-2 trigate devices, respectfully. Therefore, for a uniform doping profile the total dose would be 4.25×10^{15} cm^{-2} and 2.25×10^{15} cm^{-2} for the Gen-1 and Gen-2 devices. Both of these doses exceed the amorphization threshold for the room temperature implants as shown in Figure 4.9, also adopted from [30]. Performing the implantation at high temperature would solve this problem, however the implantation vendors available as of this report provide the service of a heated stage only for lower energy implants. Therefore, suitable adjustments are made to the implantation profile to solve the problem of amorphization.

First, a shallow, high-dose box implant profile with a nominal concentration of 2.5×10^{19} cm^{-3} and dose of 9.4×10^{14} cm^{-2} at a maximum energy of 380 keV and a temperature of 650°C is performed. The deeper implants, with a maximum energy of 3.15 MeV and dose of 6.2×10^{14} cm^{-2}, are performed at room temperature. The combination of these implants keeps the dose below the amorphization limit, and still provides a shallow region with sufficiently high concentration for a low resistance

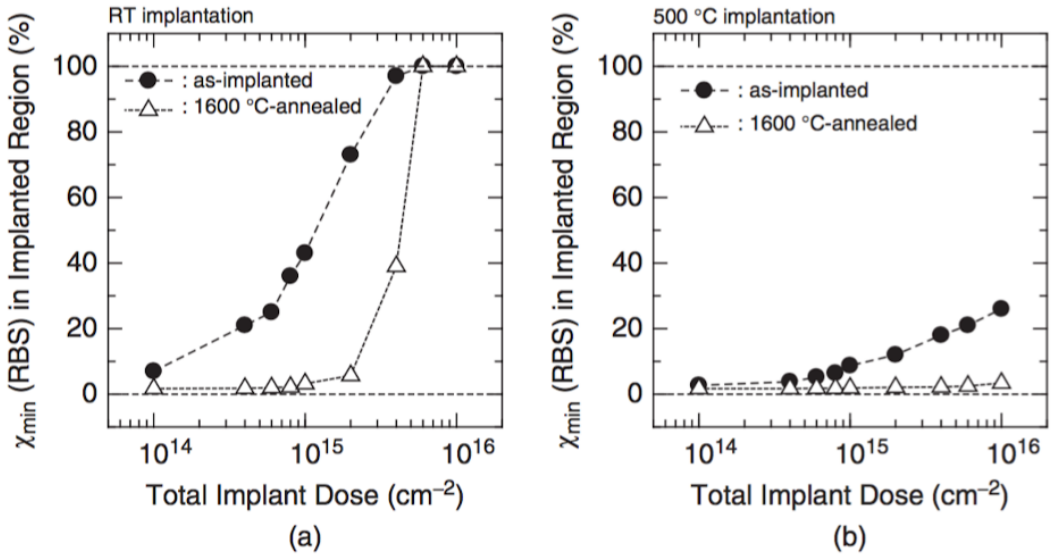


Figure 4.9.: Amorphization of SiC vs. dose and implant temperature of nitrogen implant. [30]

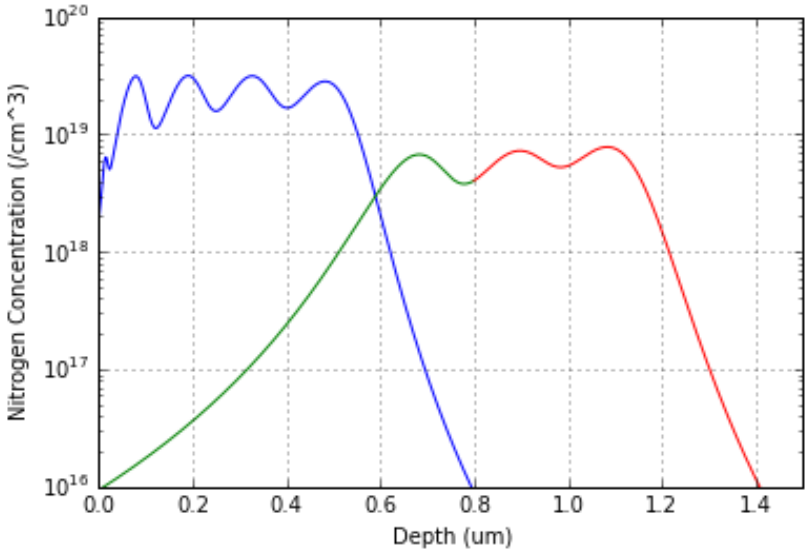


Figure 4.10.: Source region nitrogen implantation profile with the split high and low energy implantation schedules illustrated for the trigate Gen-2 samples with a 1 µm trench depth

ohmic contact. For example, the source implantation profile for the Gen-2 device is shown in Figure 4.10. The complete implant schedule for both Gen-1 and Gen-2 samples is listed in Table 4.2.

Table 4.2.: Complete implant schedule of high energy nitrogen implant for n-source in the trigate Gen-1 and Gen-2 samples.

Trigate Gen-1		**Trigate Gen-2**	
Energy (keV)	**Dose**(cm^{-2})	**Energy (keV)**	**Dose**(cm^{-2})
33	1.35	8	0.05
47	1.32	30	0.1
123	1.28	47	1.53
235	1.22	123	2.63
380	1.13	235	3.49
604	1.02	388	4.19
923	4.19	605	1.02
1336	3.49	875	1.13
1840	2.63	1160	1.52
2412	1.53		
3010	0.10		

4.1.1.2 Process Development

P-base implant

The high energy ion implantions described above need to be masked to define the edges of the P-base and N+ source regions. The implant mask also needs to be compatible with the self-aligned, short channel process [58], where polysilicon is used as the implant mask. Monte Carlo simulations using TRIM indicate that a 4 µm thick silicon film is required to block the highest energy implant of 4.25 MeV. A

calibration run was carried out to experimentally ensure that 4.5 µm thick polysilcon mask is sufficient to block the implants.

To do this, a 5 µm polysilicon film is first deposited on a SiC sample. Aluminum and nitrogen ion implantations were then carried out at room temperature at energies of 4.25 and 3.0 MeV respectively. A SIMS measurement was then done on the polysilicon film to measure the aluminum and nitrogen profiles. As seen in Figure 4.11, a 4.5 µm thick polysilicon film is sufficient to stop the implantation species well before the polysilicon/SiC interface, indicated by the vertical magenta line. The quantification of nitrogen near the polysilicon / SiC interface is distorted due to the secondary ion yield-matrix effect [99], and there is some ambiguity in both the location of the interface and the concentration of the target species on either side. However, the nitrogen peak as both predicted and observed at a depth of 3 µm from the polysilicon surface is well-contained in the polysilicon and none of the implanted nitrogen actually penetrates into the SiC.

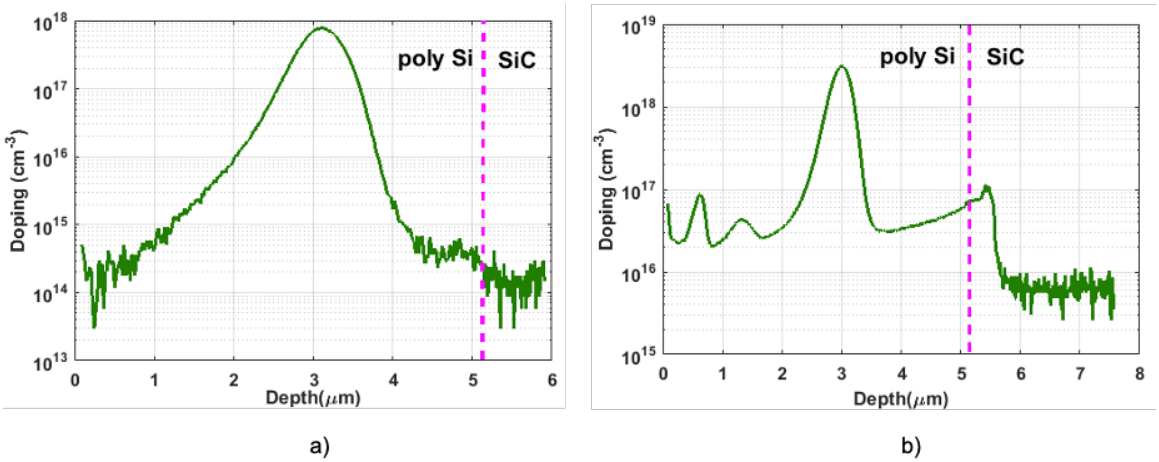


Figure 4.11.: Calibration of ion implantation into polysilicon with highest energies for aluminum and nitrogen used in the trigate MOSFETs. a) Measured profile of Al in a polysilicon mask with a dose of 7.73×10^{13} cm^{-2} and an energy of 4.25 MeV, b) Measured profile of N in a polysilicon mask with a dose of 1.35×10^{14} cm^{-2} and an energy of 3.0 MeV.

Though polysilicon has been used as an implant mask as part of the self-aligned process previously [100], the polysilicon was less than 2 µm. Owing to the high energy implantation required, the trigate MOSFET requires a significantly thicker film of polysilicon. To achieve the lowest on-resistance, the spacing between base implants (the width of the polysilicon mask) should be in the range of 1 – 1.5 µm. The high energy Al implant also defines the floating field ring (FFR) edge termination regions, which has a minimum spacing of 1 µm. The challenge is to define 1 µm features in a polysilicon layer that is $\sim$ 5 µm thick for the Gen-1 samples and $\sim$ 4 µm for the Gen-2 samples.

Ideally the 1 µm features would be defined by optical lithography using a stepper. However, since our lab does not have access to this type of lithography equipment, electron beam lithography is used to define the FFR rings and JFET regions. However, electron beam lithography with the conventional PMMA resist is not feasable due to unrealistically long exposure time even at the highest available electron beam current (100 nA). Two process flows have been developed to successfully pattern the polysilicon implant mask. The first method is applied to the Gen-1 samples and the second method is applied to the Gen-2 samples.

Method 1

In method 1, a combination of electron beam lithography to define the active areas, and optical lithography to define the test structures is used. As this is the first lithography step, global alignment marks in the SiC are not defined and temporary alignment marks to align the electron beam and optical lithography steps must be defined. This is done by etching an alignment pattern in the polysilicon film. A thermally grown 200 nm thick oxide layer is used to mask the alignment mark etch. The oxide mask also defines the edges of the P-base region in the test structures. To accommodate the alignment mark etch and the required thermal oxidation, the polysilicon thickness must be increased accordingly. This is then followed by an e-

beam lithography step to pattern the JFET regions and FFR rings in the active area. The e-beam lithography is done using a negative tone HSQ based resist called FOX-16 from Dow Corning. This is an inorganic compound composed of $[HSiO_{3/2}]_n$ clusters. Under electron irradiation, the material converts to SiO_2 thus resulting in an all-oxide mask for the polysilicon etch. Details of the resist application and exposure conditions are described in Appendix A. The polysilicon etch is then performed using the Bosch process SF_6/O_2 as the etch species and C_4F_8 as a protective polymer deposition species. An STS ASE tool is used for the polysilicon etch for both the alignment mark and the implant mask patterning. The baseline process used for the polysilicon etch is outlined in Table 4.3.

Table 4.3.: Polysilicon etch recipe in STS-ASE ICP-RIE

Parameter	Etch	Deposit
Gas (sccm)	SF_6/O_2 (130/13)	C_4F_8 (100)
ICP power (W)	500	600
Bias power (W)	20	0
Pressure (mT)	18	18
Cycle (sec)	5	5

The etch rate of silicon and polysilicon using the above recipe is 650 nm/min while the oxide mask etches at ∼20 nm/min. The entire process flow for method 1 is illustrated in Figure 4.12. Further details regarding the polysilicon etch and an alternative RIE etch process are described in [101].

Method 2

Method 2 is based on a single step, all e-beam lithography process flow. This is possible due to a highly sensitive and high contrast e-beam resist called AR-P 6200 CSAR. The exposure time is drastically reduced with this resist, enabling the

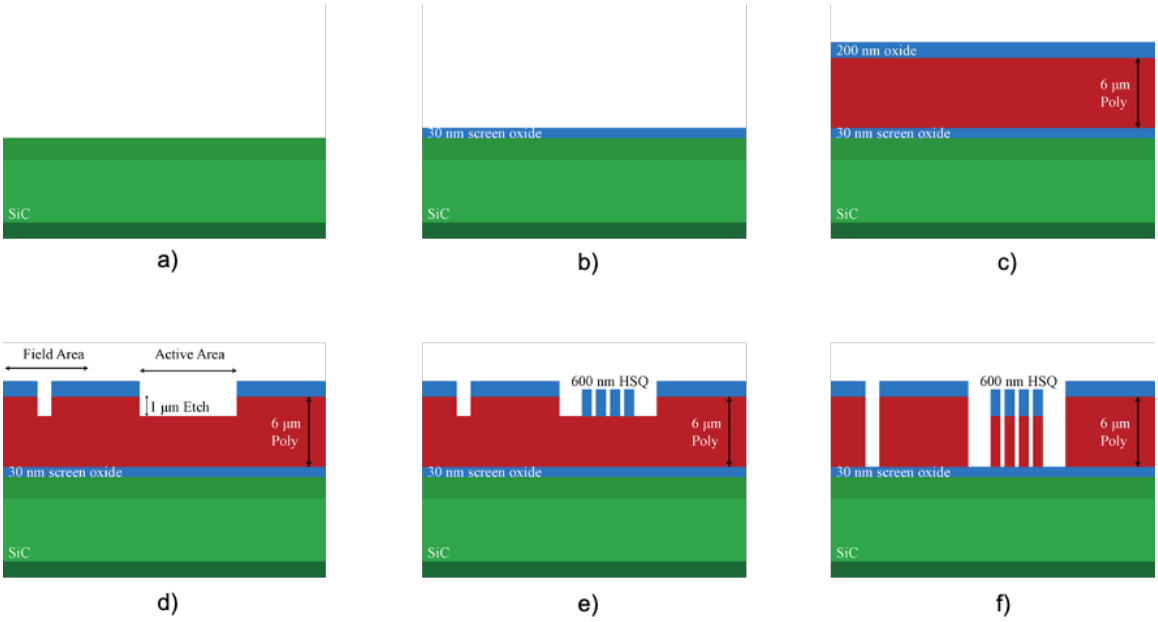


Figure 4.12.: Schematic images depicting the process flow to pattern the polysilicon mask using method-1. a)Clean SiC wafer, b)Screen oxide grown by thermal oxidation, c) Deposition of polysilicon by LPCVD and thermal oxidation to form 200nm of oxide, d)Optical lithography and polysilicon etch to form temporary alignment marks, e) E-beam lithography to pattern the polysilicon mask in the active area using the alignment marks defined in the previous step, f) Polysilicon etch to form the polysilicon mask for the P-base implant.

entire P-base region to be defined with e-beam lithography. However, to use this process, the CSAR resist must be able to act as a mask during the polysilicon RIE etch. A test was thus performed to determine the etch rate of the CSAR resist in the Bosch process with the parameters in Table 4.3, and the etch rate was found to be 50 nm/min. Therefore, an etch selectivity of 13:1 between the polysilicon and CSAR e-beam resist can be achieved. The process flow for method 2 is illustrated in Figure 4.13, and is applied to the Gen-2 samples. Details of the process parameters such as spin coat speed, baking temperature and e-beam exposure conditions, can be found in the run sheet in the appendix.

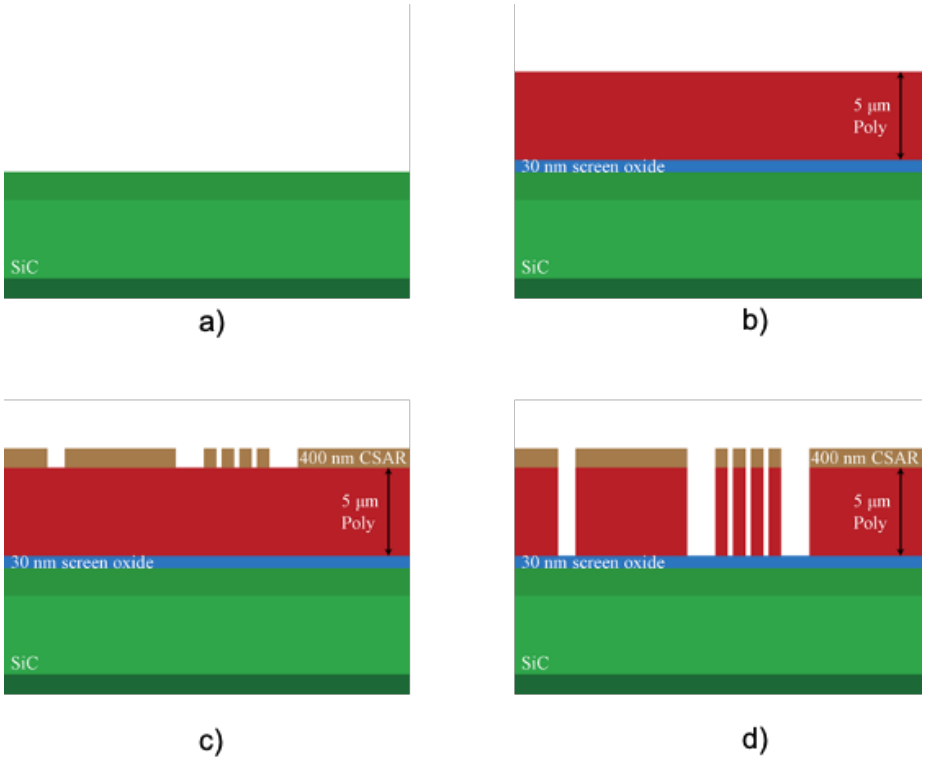


Figure 4.13.: Schematic images depicting the process flow to pattern the polysilicon mask using method-2. a) Clean SiC wafer, b) Screen oxide and deposition of 5 µm thick polysilicon by LPCVD, c)Electron beam lithography in the active and field areas using CSAR resist, d)Polysilicon etch to form the polysilicon mask for the P-base implant.

The Bosch polysilicon etch parameters are identical with either masking method. Figure 4.14 illustrates the highly anisotropic and high aspect ratio polysilicon patterns achievable using either of the methods described above.

Source implant

The source implant is performed in two steps: high-dose, low energy implants at 650 celsius, and lower-dose, high energy (MeV) implants at room temperature. The two major process development challenges for the n-source implants are: 1) self-

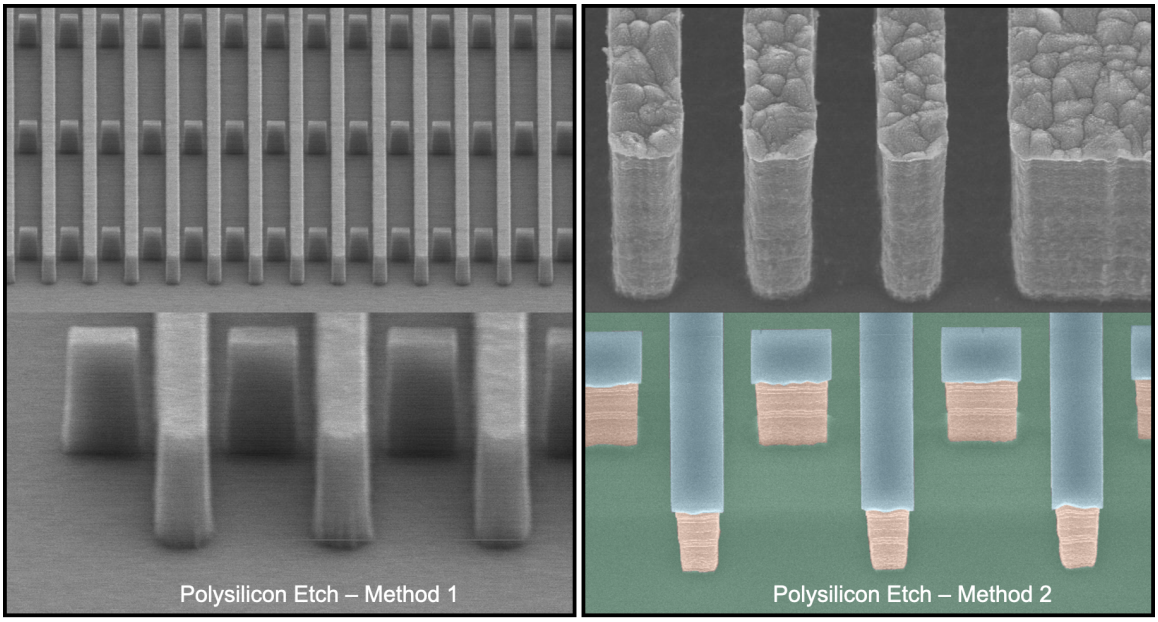


Figure 4.14.: SEM images of the polysilicon etch using the Bosch process in the ICP STS ASE for method-1 and method-2

aligned process in the active area, and 2) thick metal N+ block mask for the PCM test structures.

Self-aligned process in the active area

In the active area, a self-aligned process is used to form the channel region by blocking the high energy N+ implant that forms the source regions. A sidewall spacer is formed by thermal oxidation of the polysilicon implant mask pillars, creating a gap between the P-type base implant and the subsequent N+ source implant, thus defining the channel length of the MOSFET as illustrated in Figure 4.15.

A pyrogenic wet thermal oxidation at 1100°C and atmospheric pressure is employed to create a 0.5 µm lateral expansion of the polysilicon implant mask. During development of the process, a crystalline silicon<100> sample and a patterned polysilicon test sample were loaded together to calibrate the oxidation rate. As seen in Figure 4.16, the oxidation rate of polysilicon is slightly higher than crystalline silicon,

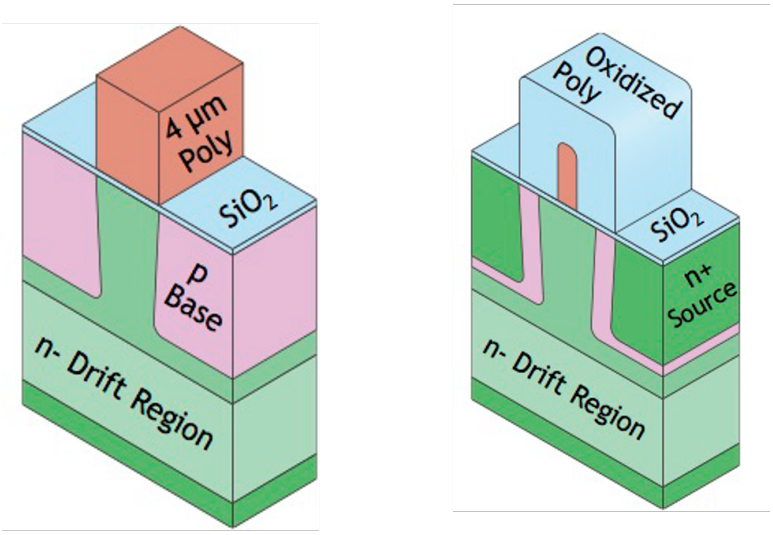


Figure 4.15.: Illustration of the n-source implant self-aligned to the P-base. a) Polysilicon mask pattern during the aluminum P-base implant, b) Thermal expansion of the polysilicon mask to self-align the n-source implant to the P-base implant

as expected. The low oxidation rate of polysilicon at the initial stages could be due to the presence of polymer residue from the Bosch process used to etch the polysilicon. During the oxidation, the thermal oxide expands both vertically and laterally with respect to the original surface, and the thickness of the resulting silicon dioxide is proportional to the amount of silicon consumed.

By the law of mass conservation,

$$t_{Si} \times N_{Si} = t_{SiO_2} \times N_{SiO_2}$$

Where t_{Si} is the thickness of the original polysilicon, t_{SiO_2} is the final thickness of the silicon dioxide, N_{Si} and N_{SiO_2} is the molecular density of the silicon (5×10^{22} cm^{-3}) and silicon dioxide (2.3×10^{22} cm^{-3}), respectfully. Substituting these values into the above equation,

$$t_{SiO_2} = t_{Si} \times (N_{Si}/N_{SiO_2}) = t_{Si} \times 2.174 \tag{4.1}$$

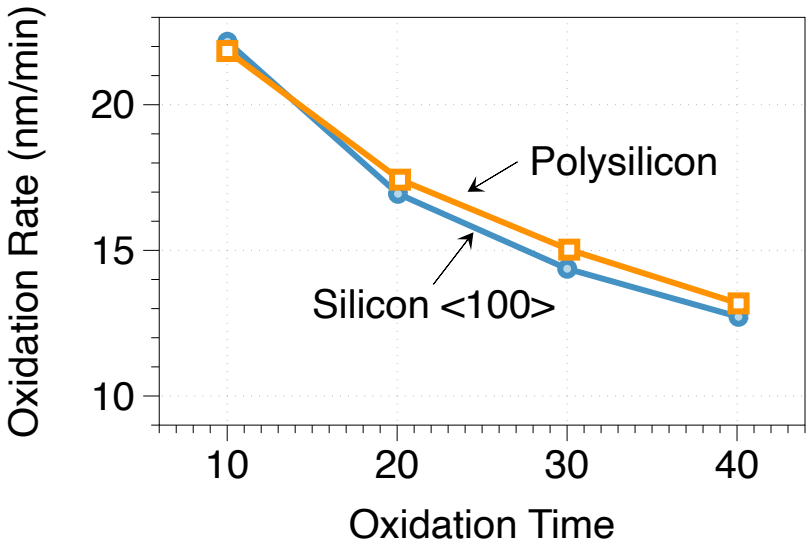


Figure 4.16.: Pyrogenic oxidation of polysilicon and crystalline silicon <100> at 1100°C.

To achieve a lateral expansion of 0.5 µm, a total oxide thickness of 0.925 µm is required by using (4.1). Now using the oxidation rate from Figure 4.16, the total oxidation time of 2 hours is required to form the 0.5 µm oxide spacer using pyrogenic oxidation at 1100°C. Figure 4.17 shows the polysilcon mask before and after the thermal expansion using the above process.

Metal N+ block for the PCM and test structures

The self aligned process will not work in the PCM and test structures where the channel length greater than 0.5 µm is required, and therefore a separate masking scheme is developed using a metal mask. Monte Carlo simulations of the high energy nitrogen implant are used to determined the required thickness of Ni to be 2 µm. But the main challenge is to pattern this thick metal film over the preexisting polysilicon mask topology in the active area. Experiments determined that a lift-off process using thick photoresist and electron beam evaporation of nickel is not feasible, as there is a

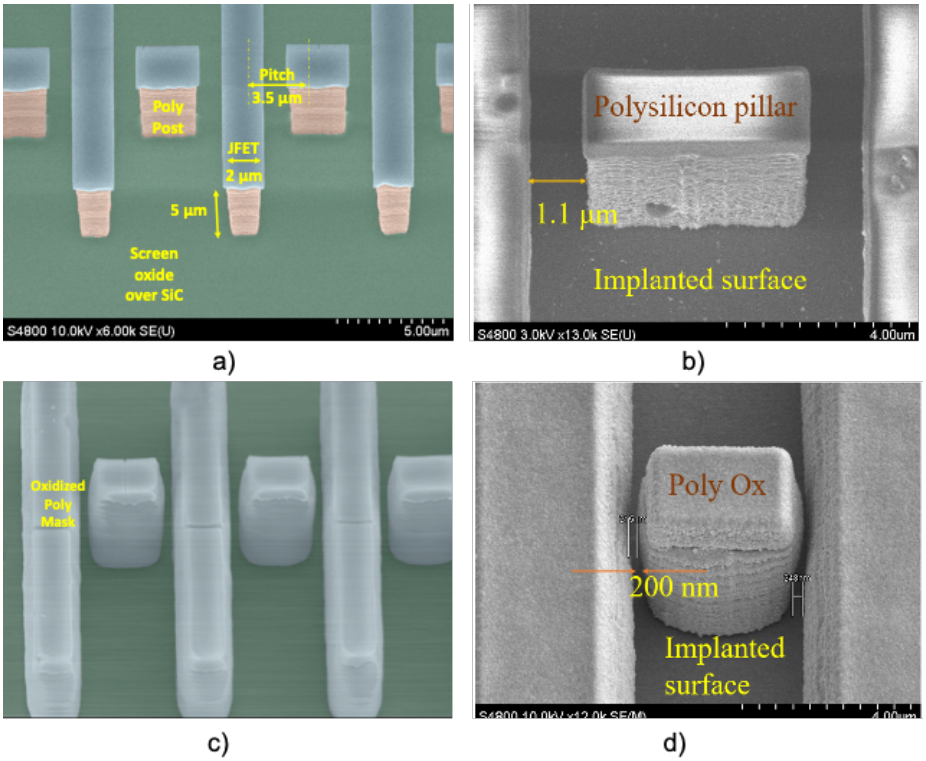


Figure 4.17.: SEM images of polysilicon used to mask base and source implants. a) Polysilicon pillars and post mask used for base implant, b) Expansion of polysilicon mask after thermal oxidation as part of the self-aligned short-channel process.

high probability of gaps at the edges of the pattern which would allow the implantation of areas intended to be masked. Therefore a conformal deposition technique such as sputtering or electroplating must be used. Sputtering is not practical, as a very thick metal film is required, and therefore an electroplating process is developed. A custom setup has been built for Ni electroplating using a solution comprised of nickel sulphate, nickel carbonate, boric acid, and DI water. Details of the electroplating setup and process conditions are described in [101]. SEM images in the PCM areas after the N+ block Ni electroplating process is shown in Figure 4.18. A clear wrap around of existing polysilicon topology is clearly seen in Figure 4.19 and no gaps at the edges are observed.

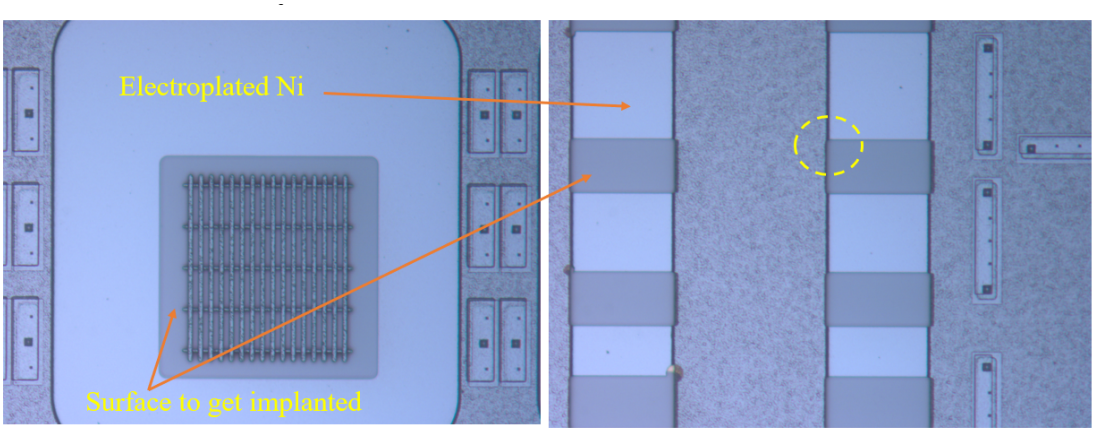


Figure 4.18.: Photomicrograph image of the electroplated Ni N+ block mask for the trigate (left) and PCM test structures (right).

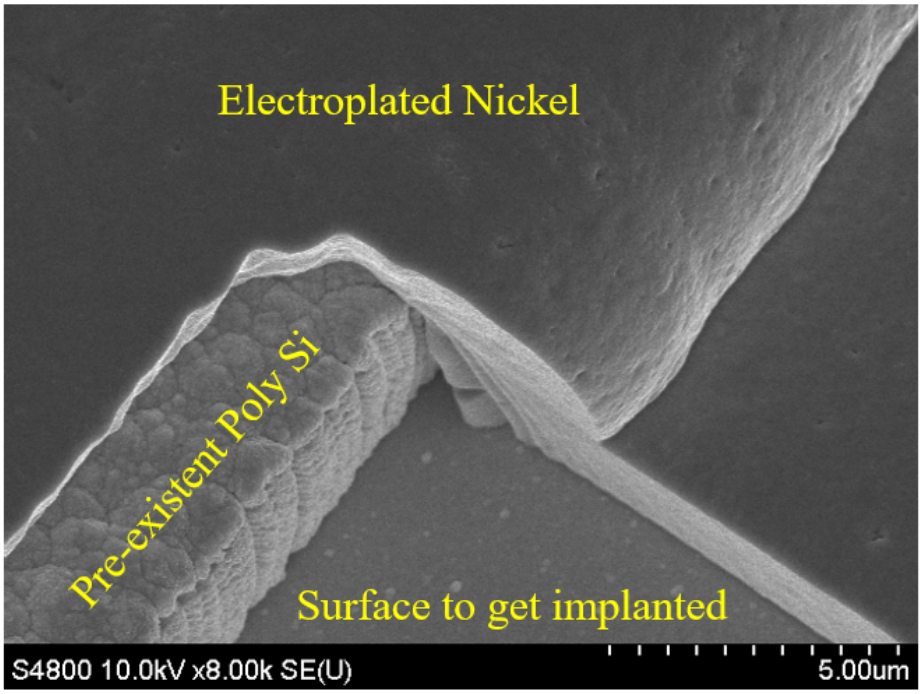


Figure 4.19.: SEM image of circled region in Figure 4.18.

P+ Implant

Another important implantation step that follows the high energy base and source implants is the P+ implant. The P+ implant forms an electrical connection between the P-base and N+ source regions such that these regions are maintained at the same electrostatic potential with respect to the drain terminal.

Figure 4.20 illustrates the method by which contact is made between the base region and the source ohmic metal contacts. The self-aligned channel process uses the same mask for both the base implant (shown in purple), and the source implant (shown in green). The polysilicon mask used to block the base implant is expanded by oxidation to block the source implant, creating a nominal 0.5 µm wide channel at the edges of the base implant. These channel regions at the edges of the base implant are covered by the gate (blue stripes in Figure 4.20(c)). Segmented P+ base contact implants are placed occasionally across the array to make contact with the source ohmic contact metal as shown in Figure 4.20(b). However, the area where this P+ implant would cross the source ohmic metal would normally be heavily doped with nitrogen. It is not possible for a P+ implant to overwhelm the background N+ doping in these regions, due to the high activation energy of aluminum dopant atoms in SiC. Therefore the N+ source implant must be blocked in the P+/source metal overlap region highlighted in Figure 4.20(c). This is done by adding posts in-between base implant mask stripes, as shown in the SEM image at the bottom of Figure 4.20(a). This prevents both the base and source implants in the overlap area, allowing the P+ implant to convert the surface from the light N-type CSL doping to P-type.

As the P+ implant is shallow, it does not require as thick a mask as the previous two implants. A 320 nm thick Ni layer is sufficient to block the highest energy in the P+ implantation profile. The process used is similar to the P-base implant mask where the fine features are patterned using electron beam lithography and the coarse features in the test structures and PCM are patterned using optical lithography. This process has been applied to the Gen-1 samples. An update in the tool set available

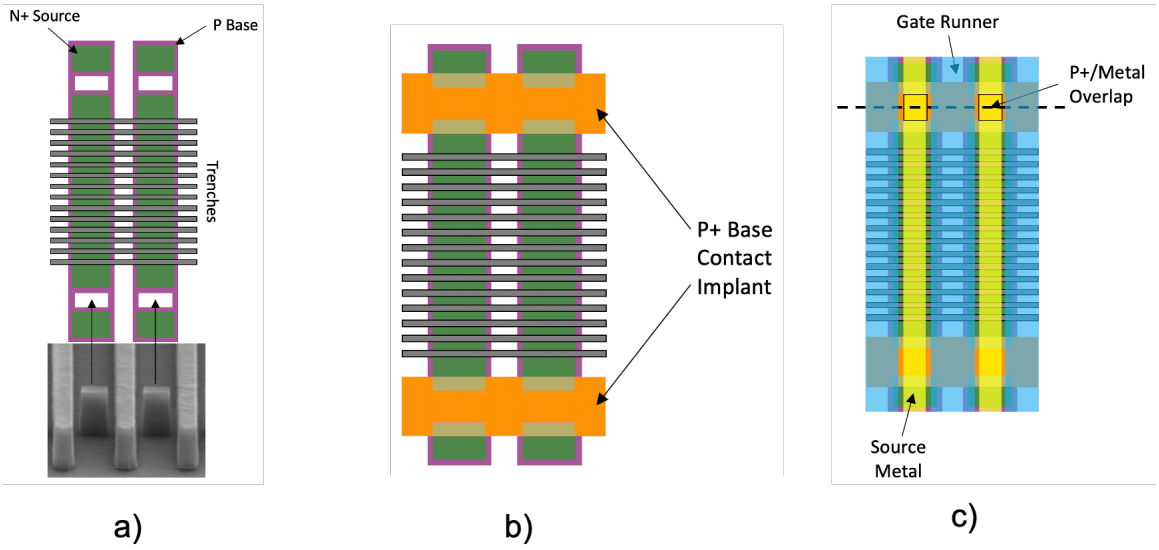


Figure 4.20.: Schematic illustration of the trigate active area. a) Base and source implants, b) Segmented P+ base contact implant, c) Completed device with gate runners and source ILD windows.

in the Birck cleanroom allowed an improvement to the above process. A maskless direct laser write tool (Heidelberg MLA) allows optical lithography to be done with alignment error less than 0.5 µm, and definition of critical features on the order of 1-2 µm. Therefore, the P+ implant mask pattern can be done in a single step using optical lithography, and this has been carried out in the Gen-2 samples. A detailed description of the process development of this step is provided in [101] and process details can be found in the run sheet in Appendix B.

Implant Anneal

Following the completion of all ion implantation steps, the implanted dopants are activated by annealing at 1700°C. The SiC surface must be protected from migration of surface atoms and silicon sublimation during this anneal, which is accomplished by using a carbon capping layer. To do this, the samples are first spin-coated with 2.5 µm of positive photoresist (AZ1518). An anneal in argon at 650°C for 20 min. is then

performed to pyrolyze the photoresist and form a carbon cap. After this anneal, the carbon cap becomes black, mirror like, and thinner than the original photoresist film. The implant activation anneal is conducted in the Epigress VP508 reactor at 1700°C in argon at 400 mbar for 10 min. The carbon cap is then removed by oxidation, and the surface morphology and roughness are measured using atomic force microscopy to determine the effect of the high temperature anneal on the SiC surface. Figure 4.21 shows a 3D plot and a 2D cross section of such a measurement. The surface roughness is below 1 nm, which corresponds to a smooth SiC surface without any evidence of residual damage from the high-energy ion implantation.

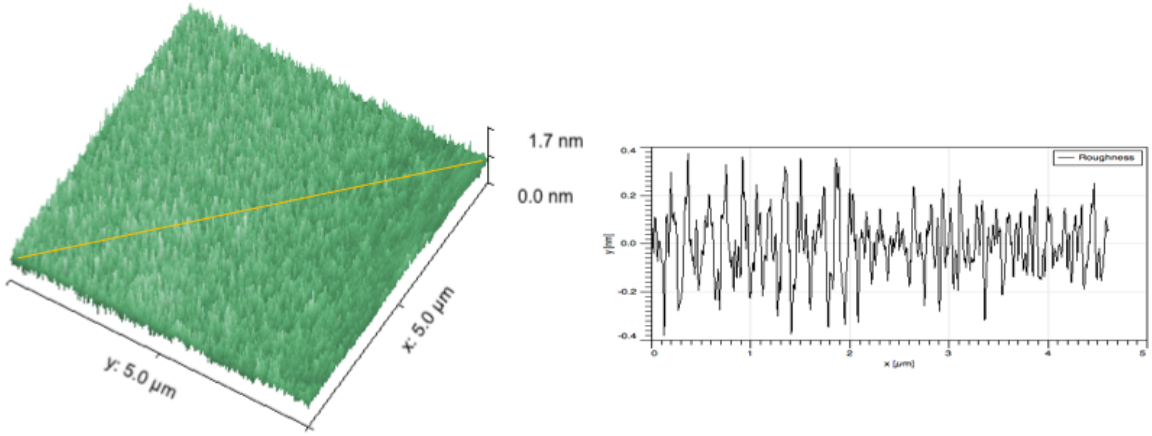


Figure 4.21.: 3D AFM image of across the source and base regions after high energy implantation and activation anneal. The roughness along the cutline (a) is shown in (b). A smooth SiC surface is recovered after the activation anneal process with a surface roughness(RMS) of 0.24 nm.

4.1.2 Sub-micron Gate Trenches

The trigate device contains sub-micron trenches in the active area that are etched perpendicular to the source and gate fingers. To take advantage of the potential performance benefit from the mobility anisotropy, the trench sidewalls should be on

$\{11\bar{2}0\}$ crystal faces. This is accomplished by defining alignment marks during the base implant process, aligning the JFET fingers parallel to the primary flat of the wafer along the $[11\bar{2}0]$ direction. The alignment accuracy of the e-beam lithography process is within 0.1 °. However, inherit alignment errors also exist such as the 4 ° offcut of the SiC surface and the curvature and orientation error of the primary flat. Figure 4.22 shows the source fingers with respect to the crystallographic orientation of the wafer. SiC trenches are etched perpendicular to the source fingers which exposes $\{11\bar{2}0\}$ faces, or a-faces, for current conduction on the trench sidewalls as shown in Figure 4.22(b). The electron mobility on the a-face in 4H-SiC is reported to be 4 times higher compared to the {0001} or Si-face [59], which would contribute to reduced specific on-resistance.

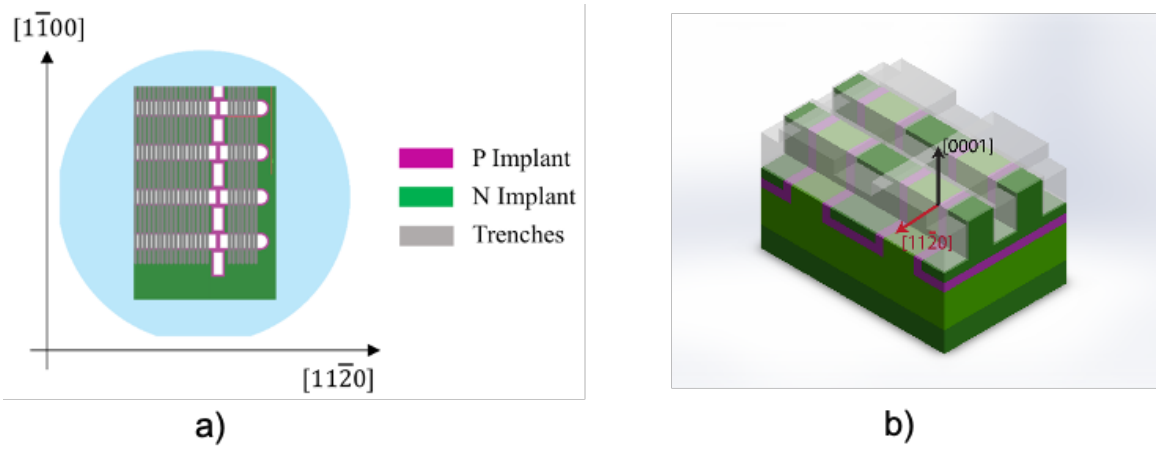


Figure 4.22.: Trench etch for trigate devices (a) JFET, source, and trench orientation with respect to the wafer flats and crystallographic directions. Trench sidewalls lie nominally on $\{11\bar{2}0\}$, or a-face planes, (b) 3D isometric view of a unit cell of the trigate MOSFET, showing the relative orientation of these features with respect to primary crystollographic directions

The process development of the trench etch has been exhaustively described in my colleague Naeem Islam's thesis [101], and only the final and optimized process conditions used for the actual trigate MOSFET samples are described here. The

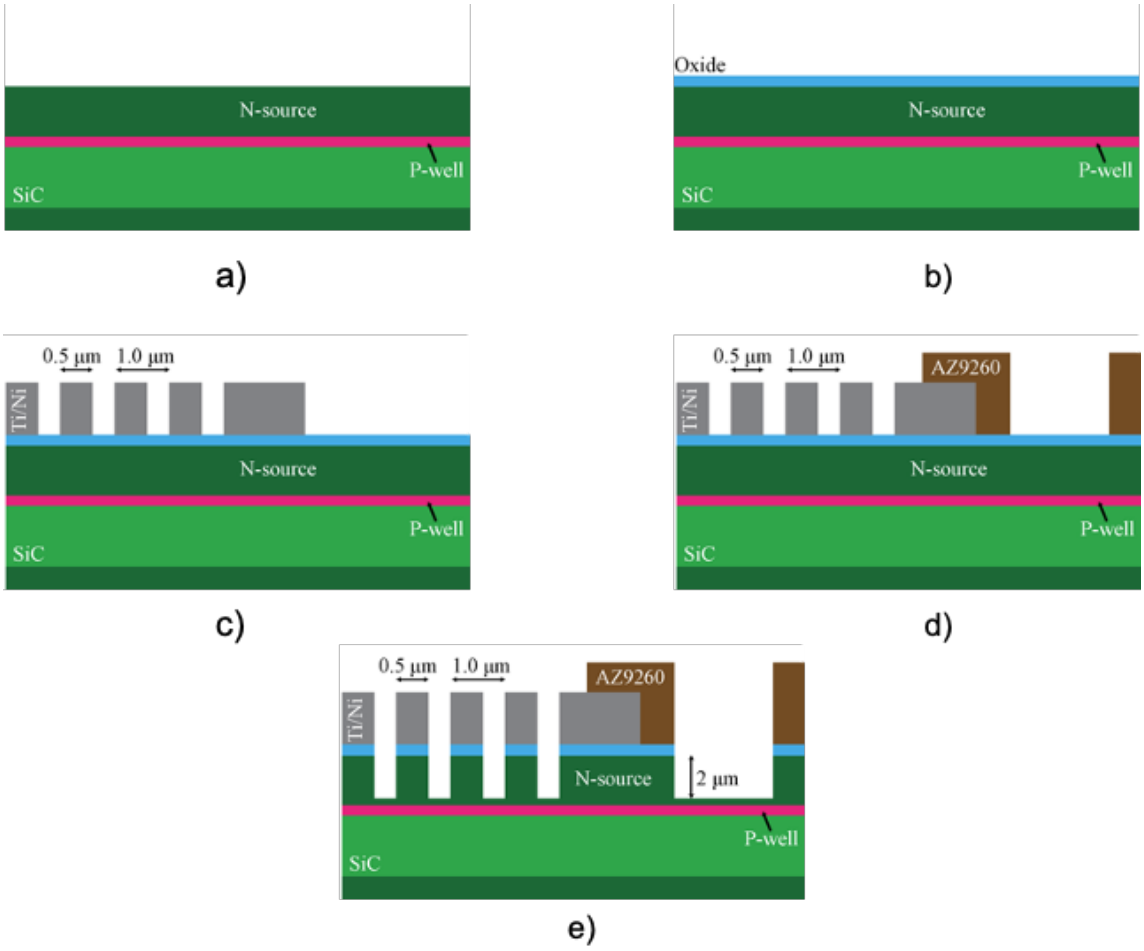


Figure 4.23.: Trench etch proess flow: (a) Wafer with n-source and P-well implant, (b) Growth of thin layer sacrificial oxide, (c) e-beam lithography and Ti/Ni (10/200 nm) metal liftoff in the active region, (d) 8-10 µm thick AZ9260 photoresist pattern in the field and PCM regions, (e) SiC plasma etch.

SiC trench pattern is created by defining a high-resolution nickel hard mask. The width of the fins and trenches are each 0.5 µm, for a 1 µm unit cell pitch. The etch mask is patterned using the JEOL JBX 8100 FS electron beam lithography system in the Birck Nanotechnology Center using a conventional bilayer of PMMA resist (495 PMMA below high resolution 950 PMMA). After developing the resist in PMMA developer (MIBK:IPA 1:3) for 45 seconds, the metal mask is deposited using

an electron beam evaporation system. The metal mask consists of a bilayer of 10 nm Ti and 200 nm Ni and is lifted off in PG remover in a hot bath at 60°C.

The resulting patterned metal layer is used as the hard mask during the trench etch, and therefore effects such as edge roughness, edge rounding, breaks or continuity in the Ni mask pattern will translate into the SiC during the etch, leading to non-ideal trench geometry. Therefore, careful dose test optimization is carried out just before each trench etch run, and the process is recalibrated to remove any drift in the key parameters. Similar to the base lithography approach, a two step process

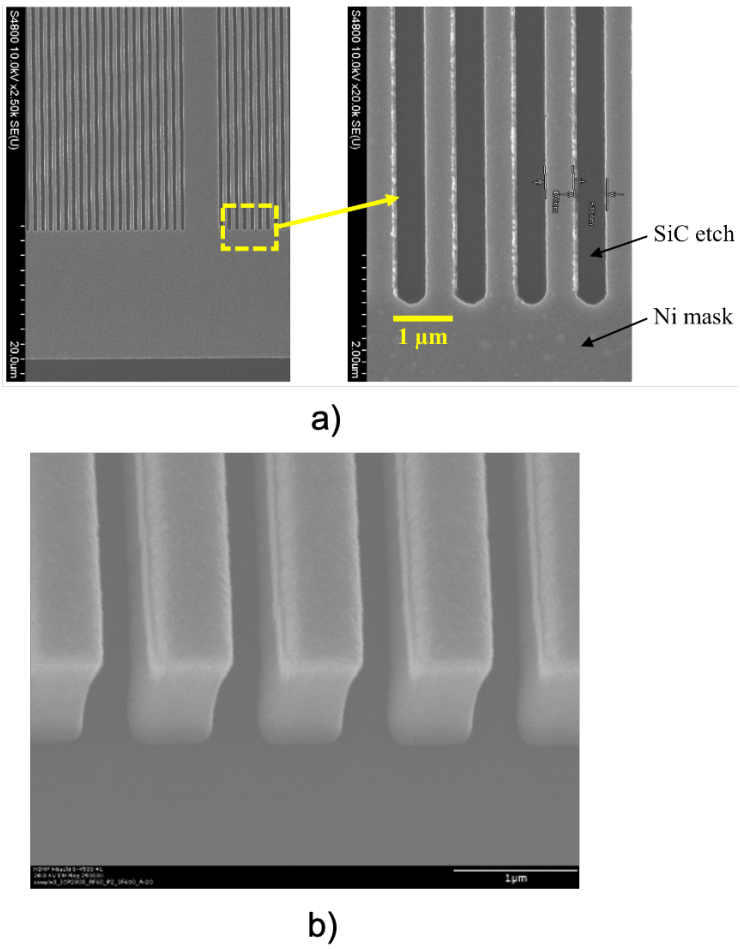


Figure 4.24.: SEM images of SiC trenches. a) Top view, b) Tilted SEM image of the SiC trench etch to form the trigate devices

comprised of both e-beam and optical lithography is used in the active and test areas, respectively. Here, once the metal is patterned in the active area using e-beam lithography and metal lift-off, the metal mask in the test structures are patterened using optical lithography. The process flow for the trench etch using the Ni mask is illustrated in Figure 4.23.

There are two major process challenges for a successful trench etch recipe: 1) vertical sidewalls and, 2) absence micro-trenching or bowing at the bottom of the trench. An optimized recipe developed for SiC in an STS-AOE ICP-RIE etch system uses 5 mTorr sulphur hexafluoride (SF_6) at 2500 W ICP power and 0.6 W/cm^2 bias power density. This produces a SiC etch rate of approximately 0.5 µm/min. An important aspect of the trench etch is the dependence of the SiC etch rate on trench width [102]. It is found that 0.5 µm wide trenches etch 20% slower compared with trenches that are more than 5 µm wide. Therefore, care is taken to calibrate the etch rate accurately to determine the etch time for the desired trench depth for both Gen-1 and Gen-2 trigate samples. Figure 4.24 shows SEM images of 0.5 µm wide SiC trenches etched using the optimized recipe to a depth of 2 µm. Vertical sidewalls and no micro-masking or micro-trenching is observed in the optimized process.

4.1.3 Gate Stack

The process development for the gate stack in the trigate device is comprised of four steps.

1. H_2 etch of SiC trenches.
2. Conformal gate oxide
3. Polysilicon deposition and doping
4. Gate patterning and etch

1) H_2 etch of SiC trenches

Reactive ion etching, which is required to form the trenches of both trigate and UMOSFET devices, is known to create surface roughness that reduces the mobility of electrons in inversion layers formed on these surfaces. In the trigate device, a majority of the current flows through channels formed on etched surfaces, and in addition to the channel geometry, the ratio of the sidewall mobility to planar mobility factors into the reduction of channel specific on-resistance. Therefore it is important to improve the mobility on RIE etched surfaces.

One possible method to improve the sidewall mobility is to remove a thin layer of the RIE etched surface using a high temperature (1400°C – 1700°C), low pressure (∼70 mTorr) anneal in a hydrogen ambient. This concept was successfully demonstrated by Liu, *et al.* [103], where they reported a 3X improvement in peak mobility after hydrogen etching an RIE etched surface, compared to RIE etching alone. This experiment was carried out on planar epitaxially grown surfaces, and there are no available reports on the effect of H_2 etching on the mobility on the trench sidewall. Several reports have shown that trench corners can be rounded by the right conditions during the H_2 etch process. This effect can be beneficial in the trigate device to reduce the oxide electric field at the trench corner, and thus to prevent early turn-on of the transistor. Though the H_2 etch is not part of the baseline trigate process, initial process development has been done as described in this section.

Hydrogen etching of SiC is comprised of competing vaporization and dissociation reactions, both of which are functions of temperature, pressure, and time [104]. Temperatures in the range of 1400°C to 1600°C are best suited for H_2 etching of SiC trenches [105], while the process pressure is subject to the equipment setup and ramp conditions. Experiments have shown that process pressure in the range of 60 to 400 mbar is most effective in achieving smooth SiC surfaces without step bunching. [106]. At a particular temperature and pressure, the etch depth is expected to be linearly dependent on time. In the trigate fabrication process flow, the H_2 etch can

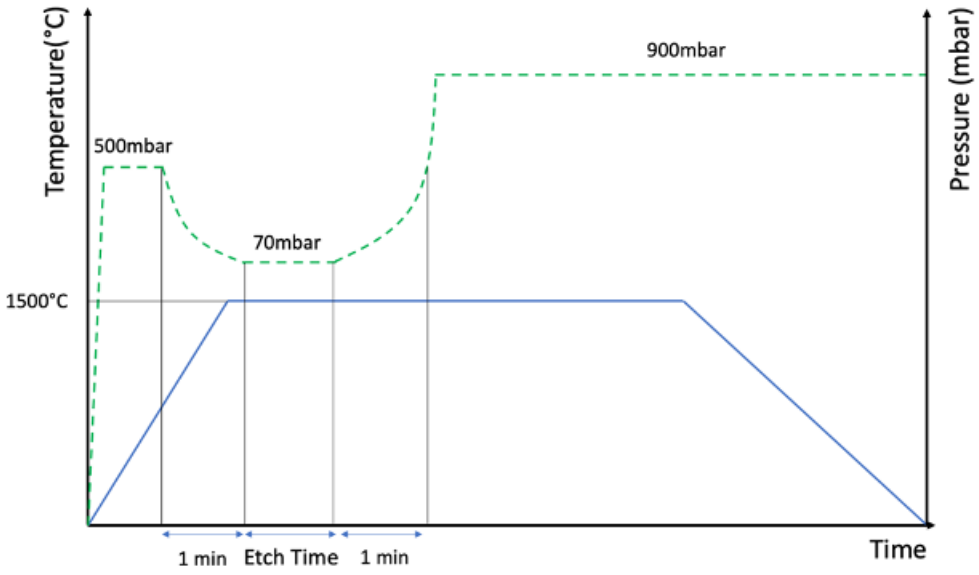


Figure 4.25.: Process flow of the H_2 etch process using the Epigress CVD chamber

only be done after the source and base implantation, and thus careful characterization of the etch rate and trench shape transformation needs to be carried out.

An experiment was carried out to determine the etch rate of the planar surface using carbon as a mask during the H_2 etch process. First, a carbon film was formed on a sample using the standard carbon-cap process described in Appendix A. The sample was then etched in the Epigress VP40 reactor in H_2 at 1600°C and 70 mbar for 10 min. The carbon cap was found to be intact after the etch process, and therefore this etch selectivity could be used to determine the H_2 etch rate of SiC. Four N-type samples were RCA cleaned, coated with 2 µm of AZ1518 photoresist and patterned using optical lithography. The pattern is made up of 50 µm square openings in an otherwise photoresist covered surface. The sample was then baked at 100°C for 2 minutes and then ramped to 150°C at a rate of 1.5°C/min. The slow temperature ramp helps to minimize the reflow of the photoresist in the patterned areas beyond the glass transition temperature. The sample was then baked at 200°C for 30 min, then pyrolyzed at 650°C for 30 min. The height between the top of the carbon film (h_0) and the SiC surface was measured using a profilometer and found to be 640 nm.

The H_2 etch is performed in the Epigress hotwall CVD chamber and the process is shown in Figure 4.25. Pressure is used to activate and de-activate the etch, as the SiC etch rate is negligible at high pressure [107] and responds much faster to pressure changes than temperature. The temperature ramp is performed at a pressure of 500 mbar in a pure H_2 ambient. Once the temperature stabilizes at 1500°C, the pressure is ramped down from 500 mbar to 70 mbar in one minute. As shown in Figure 4.25, the steady-state time the sample is subjected to a temperature of 1500°C at 70 mbar is defined as the etch time. The pressure is then increased to 500 mbar to quench the etch and then the temperature is ramped down in a H_2 ambient.

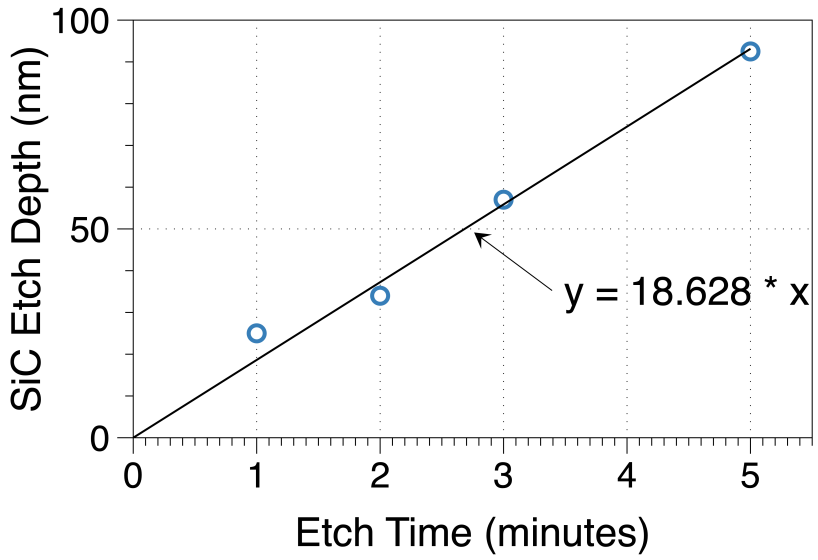


Figure 4.26.: SiC etch depth in H_2 ambient at 1500°C and 70 mbar as a function of etch time. The etch time is defined in Figure 4.25

The four samples were etched at different etch times while all other parameters were kept identical as described above. Once the etch was completed, the step height between the top of the carbon film and the SiC surface was measured (h_1) using a profilometer. The carbon film was then removed by oxidizing the samples as 700°C for 35 minutes and a BOE etch was done for 1 minute to remove any residual oxide. Now, the step height at the same location (h_2) indicates the total SiC etched during

the H_2 etch process and is plotted in Figure 4.26 for the four samples. The etch rate is found to be 0.31 nm/sec or 18.6 nm/min. The amount of carbon cap removed during the etch is given by height difference $h_0 - (h_1 - h_2)$. This value was found to be very small and within the measurement error of ~ 5 nm.

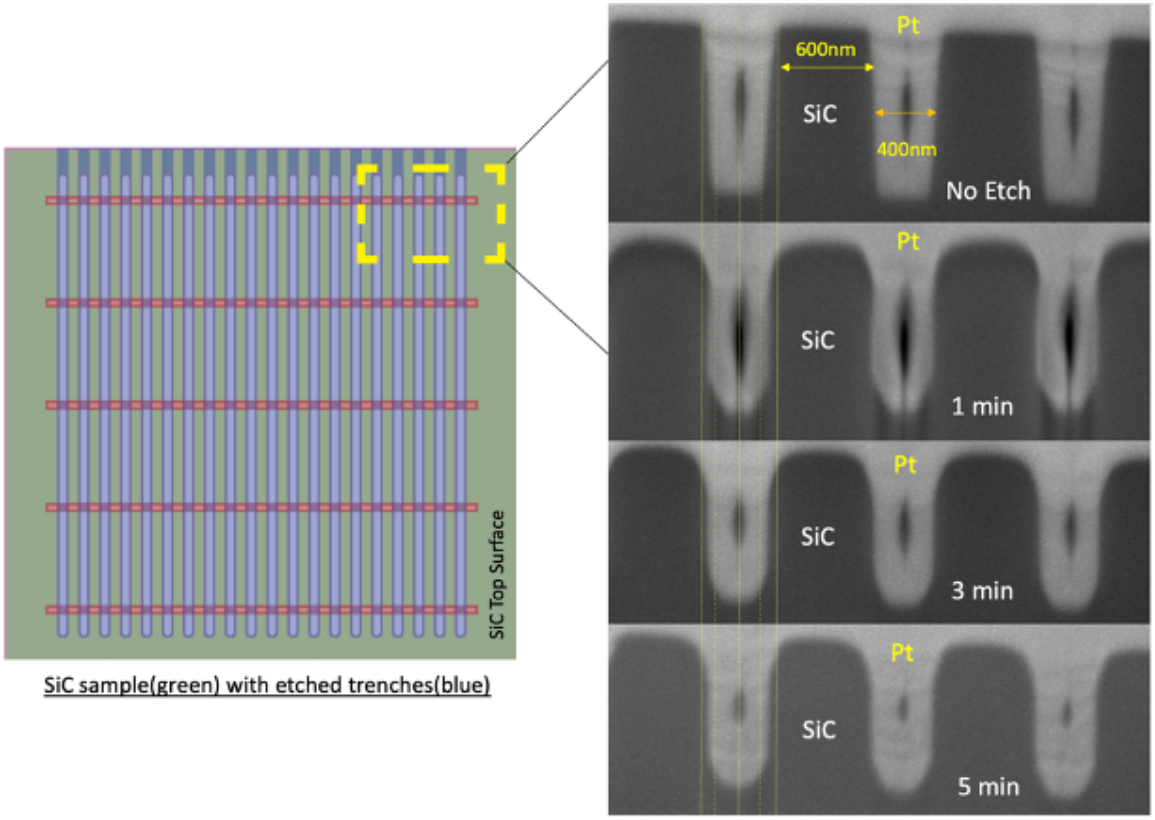


Figure 4.27.: FIB cross section of H_2 etched trenches at 1500°C and 70mbarr for different etch time. The etch time is defined in Figure 4.25. Trench corner rounding is observed as the etch time is increased.

To study the impact of the H_2 etch on trench geometry, and also to determine the etch rate of the sidewall, a study on etching a trigate-like trench structure was carried out. Trenches were etched in N-type SiC samples in the Panasonic E620 ICP-RIE etcher using SF_6 and Ar at a ratio of 1:5. The samples were then etched in H_2 using the process described in Figure 4.25. SEM cross-sections across the trenches after the H_2 etch process are shown in Figure 4.27. The lateral etch rate is minimal

(∼ 3 nm/min) as compared to the vertical etch rate of 18.6 nm/min. Significant rounding of the trench corners is evident, but the sidewalls appear to become more vertical as the etch progresses. This indicates the presence of a crystal face selective etch rate and further work needs to be done to characterize and understand this etch anistropy.

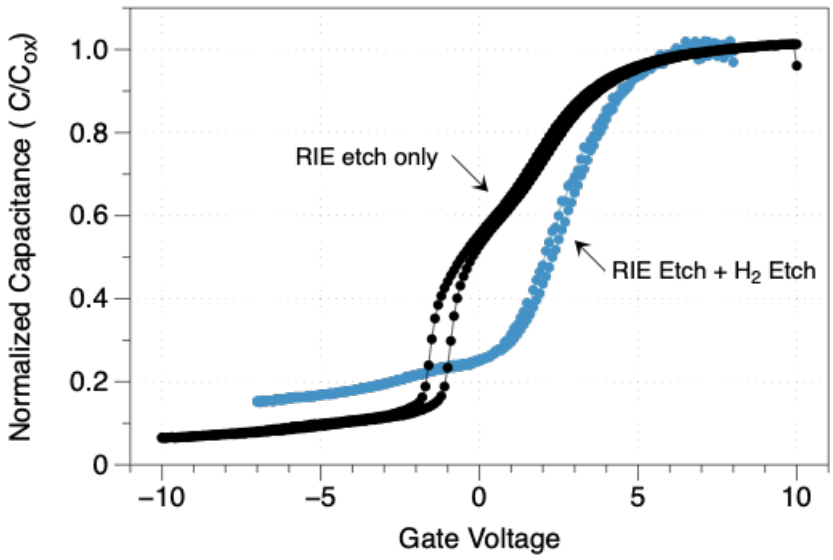


Figure 4.28.: CV characteristics measured at 100 kHz for H_2 etched and unetched trench MOSCAPs.

Trench MOS capacitors were fabricated on a samples with an N-type epilayer and a doping of 2×10^{16} cm^{-3}. The trench etch was carried out in the Panasonic E620 ICP etcher to a depth of 1 µm. A sacrificial oxidation was carried out on both the samples at 1100°C for 3 hours in a pyrogenic oxidation furnace and BOE etch was done remove the oxide with an aim to reduce the surface roughness caused during the RIE. Sample 1 was then subjected to H_2 etch at 1500°C and 70 mbar for 1 minute while Sample 2 did not receive a H_2 etch. Gate oxide was formed on both the samples using the poly-ox process discussed in Section 4.1.3, resulting in a 43 nm oxide on Sample 1 and 59 nm on Sample 2. An NO anneal was not performed in this experiment. Polysilicon was then deposited to planarize the surface and the film was doped using

a phosphorous spin-on-dopant and a drive-in temperature of 1000°C for 30 minutes. The CV response of both devices are shown in Figure 4.28. The electrical data shows an improvement in the basic CV characteristics of SiC trench MOSCAPs with H_2 etch. Without a H_2 etch process, capacitors exhibit a "double hump" characteristic, suggesting that the capacitor is composed of two different capacitors in parallel with different net interface charge densities. These may correspond to the etched and unetched areas, or to the sidewall and horizontal surfaces of the trench MOSCAP. In samples with a H_2 etch, the "double hump" feature disappears, and the CV shows closer to ideal characteristics.

2) Conformal gate oxide

The formation of a reliable, high-quality gate oxide wrapped uniformly around the transistor fins is one of the keys to successful fabrication of trigate MOSFETs. Thermal oxidation cannot be used for this purpose due to the different oxidation rates of the top and sidewalls of the trench. Therefore a deposited oxide process that has been successfully employed to build planar DMOSFETs [108] and trench UMOSFETS [58] has been employed. This process, known as the "poly-ox" process, involves thermal oxidation of a thin LPCVD-deposited conformal polysilicon film. Other alternative SiO_2 deposition methods based on either TEOS LPCVD or TDMAS atomic layer deposition(ALD) have also been investigated. However, process development on these alternatives is not yet complete, and this is discussed in Section 6.1 as part of suggestions for future work.

The poly-ox process is comprised of two steps i) Conformal deposition of polysilicon and ii) Polysilicon oxidation and NO anneal. These two processes are described separately below.

i) Polysilicon deposition

The polysilicon film was deposited by a hot-wall, resistance heated, horizontal, fused-silica tube chemical vapor deposition(CVD) furnace designed by ProTemp Products, Inc., as depicted in Figure 4.29. Silane (SiH_4) is used as the source gas, which readily decomposes onto the substrate, leading to the deposition of a thin film of silicon. The LPCVD deposition process can be broadly classified into reaction- and diffusion-limited regimes. For conformal deposition of polysilicon over the surface topology of the trigate, it is important to operate in the reaction-limited regime, as the deposition rate is then determined by the surface reaction rate rather than the arrival rate of the source gas. To ensure the polysilicon deposition is carried out in the surface reaction regime, 6 dummy wafers were placed in the quartz boat facing the input stream of source gas as seen in Figure 4.29, and the process conditions were optimized as discussed below.

The LPCVD deposition process in the reaction-limited regime is known to take place in the non-epitaxial Volmer-Weber mode through a stagnant boundary layer [109]. The deposition rate is primarily dependent on the gas flux at the boundary layer and the deposition temperature. The gas flux or reactant concentration is controlled by the chamber pressure. High pressure increases the deposition rate, but also increases the roughness of the deposited film due to non-uniform gas phase reactions driven by the desorption rate of hydrogen. Low pressure usually leads to more uniform, conformal and smooth films but decreases the deposition rate. The best compromise was found to be a chamber pressure in the range of 100-130 mTorr to maintain a practical deposition rate and to ensure a smooth, conformal film of polysilicon. Temperature also has a significant impact on the deposition rate. Higher deposition temperature increases the reaction rate, and as the deposition is within the reaction-limited regime, higher reaction rate leads to higher deposition rate. The deposition rate of polysilicon was measured at various temperatures as shown in Figure 4.30. As seen in the figure, the deposition rate increases exponentially with

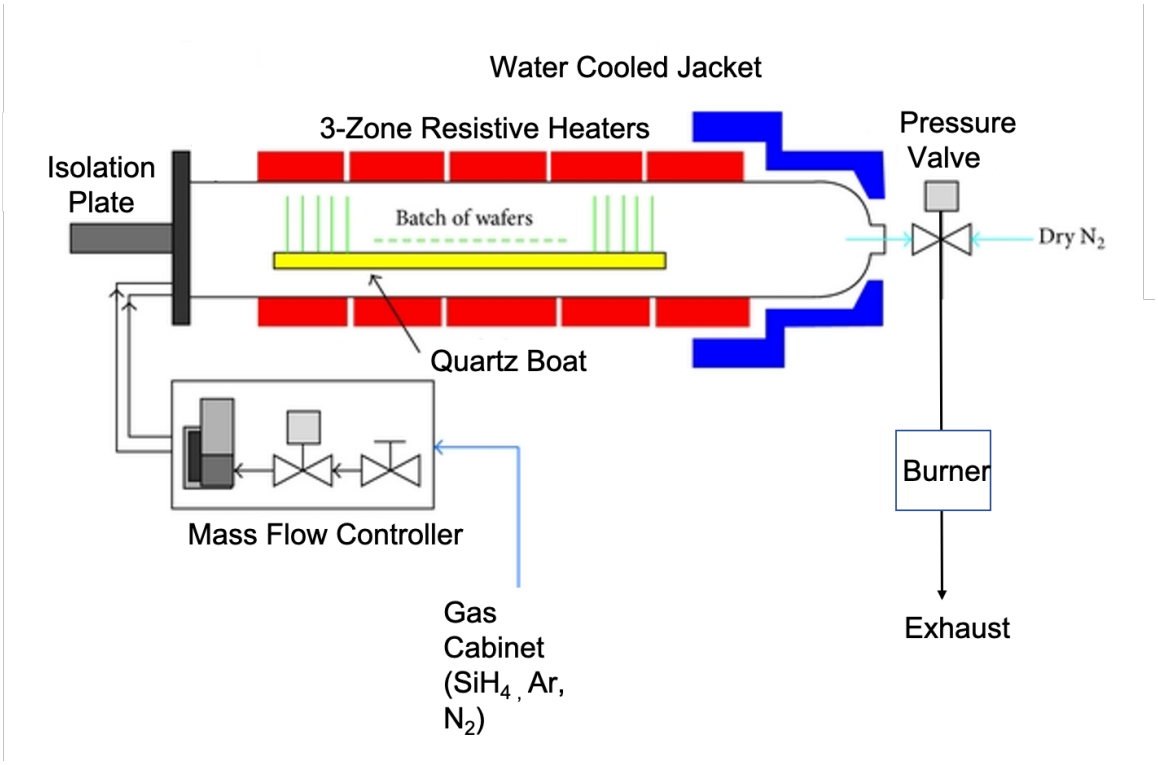


Figure 4.29.: Apparatus for LPCVD deposition of polysilicon using a quartz tube furnace.

temperature as expected from an Arrhenius relationship in a reaction-limited process. In a CVD process, a smooth film of polysilicon is obtained by allowing sufficient diffusion of the deposition precursor on the surface of the sample [110]. Experiments have shown a strong dependence of surface roughness on substrate temperatures and growth rates [111]. In this case, it is the physisorption and surface trasport of the SiH_3 radical that determines the surface roughness of the polysilicon film. The surface roughness of the polysilicon film grown at two temperatures and same pressure of 130 mTorr was measured using AFM. The RMS roughness is found to decrease with increased deposition temperature as seen in Figure 4.31.

Temperature and pressure also influence the structure of the polysilicon film. For a stable and repeatable process, a polysilicon film with defined columnar structures [112] is desired. To determine the right conditions for deposition, the polysilicon

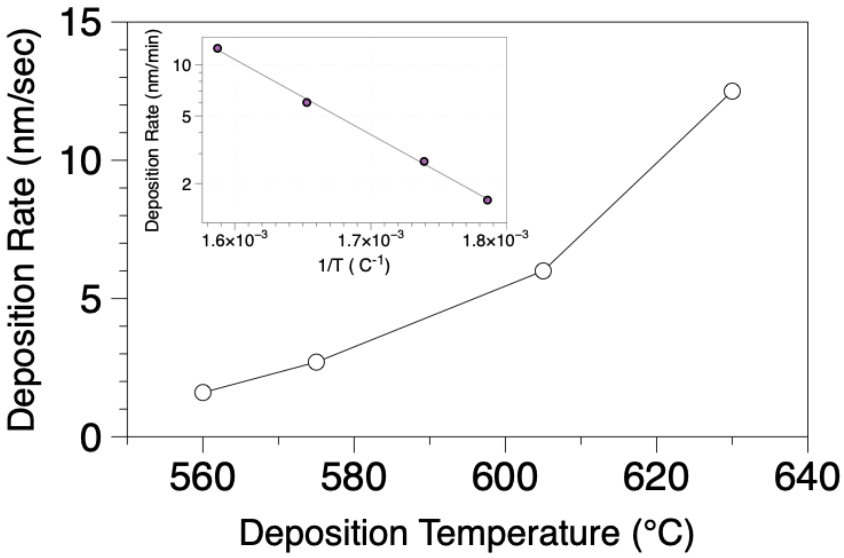


Figure 4.30.: Deposition rate of LPCVD polysilicon at a deposition pressure of 130 mTorr for different deposition temperatures

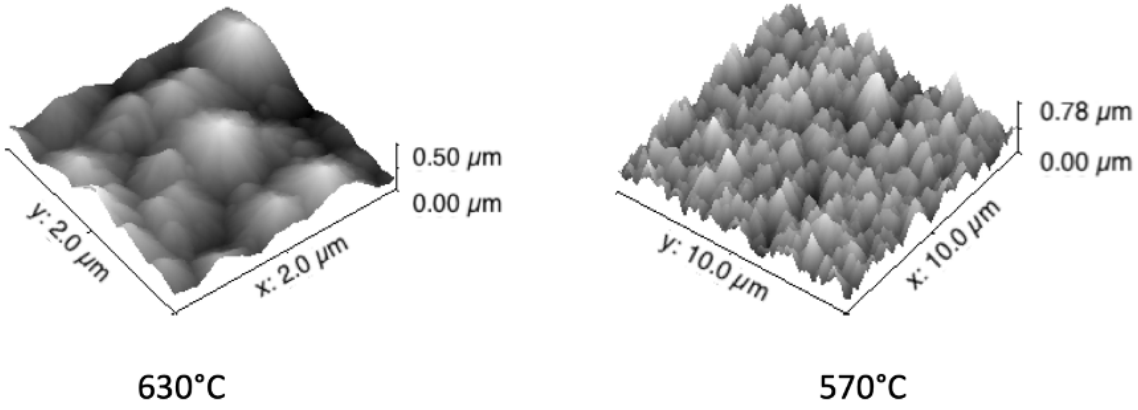


Figure 4.31.: Surface roughness of the LPCVD polysilicon film deposited at 630°C and 570°C

film was deposited on an oxidized silicon surface at various temperatures and the crystallinity was measured using the XRD technique. The Panalytical XRD system with 2θ capability was used and the results are seen in Figure 4.32. A large amorphous signal is detected below 620°C, and a columnar structure is observed at 630°C. It must

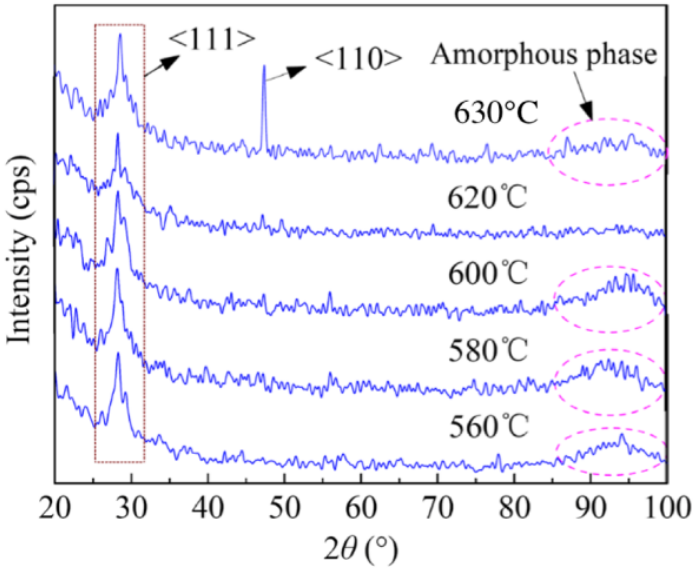


Figure 4.32.: XRD diffraction signal of LPCVD polysilicon film deposited at differnt temperatures. Signal from all the crystal faces is seen at 630°C

be noted that due to drift in the pressure of the LPCVD deposition tube, this process was re-optimized using the approach described in this section before applying it to the fabrication of the trigate samples. A deposition temperature of 580°C was used and is discussed in Section 4.2.3.

ii) Polysilicon oxidation to form gate oxide

Once the polysilicon is deposited, the thin film is thermally oxidized to form the gate oxide. Careful calibration of the polysilicon oxidation rate is done to prevent unintended oxidation of the SiC underneath the polysilicon film. On the other hard, it is important to ensure that the entire film of polysilicon is consumed during the oxidation, as even a thin layer of polysilicon at the SiC-oxide interface could severely degrade the MOS characteristics of the MOSFET. This calibration is done by depositing polysilicon of the same thickness on both a SiC and a Si sample, with both undergoing thermal oxidation together in the same run. The thickness of the polysil-

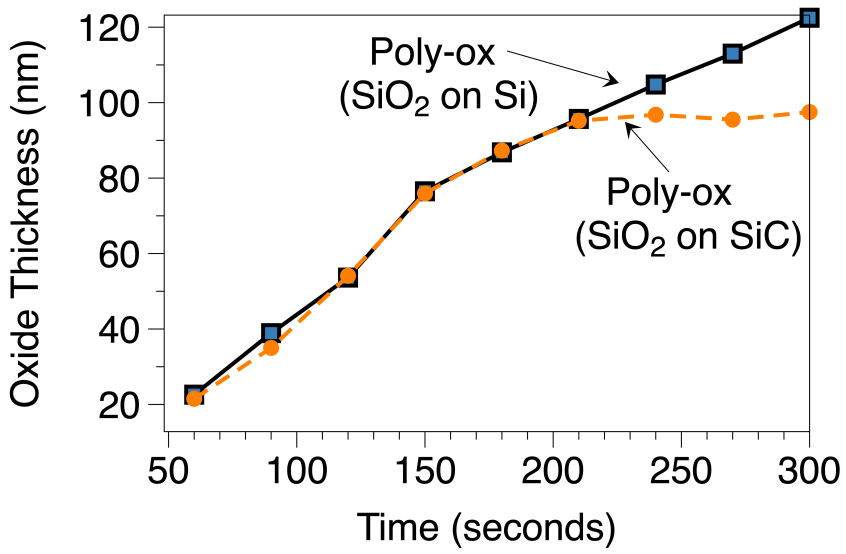


Figure 4.33.: Calibration of polysilicon oxidation on Si and SiC samples to ensure complete but not excess oxidation of the deposited polysilicon film.

icon film is 45 nm and is deposited at 580°C. This is repeated for several oxidation times and the resulting oxide thickness is plotted in Figure 4.33. Initially, the oxide thicknesses on both samples are identical (within measurement error), since in this regime only the deposited polysilicon film is being oxidized. However, once the polysilicon film is completely consumed, the oxide thickness on the SiC sample saturates as seen in Figure 4.33 due to the fact that the oxidation rate of the SiC is about two orders of magnitude lower than Si. This does not happen on the Si sample because the oxidation rate changes only marginally (refer Figure 4.16) when the oxidation front moves from polysilicon to single crystal silicon. The deposited polysilicon is completely consumed at 205 seconds in Figure 4.33 and the oxide thickness is 98 nm. The oxidation time is thus adjusted for the required oxide thickness in the actual trigate samples, and the oxidation on the planar and sidewall surfaces is assumed to be the same. This assumption is consistent with process simulations using Sentaurus Process with the above conditions.

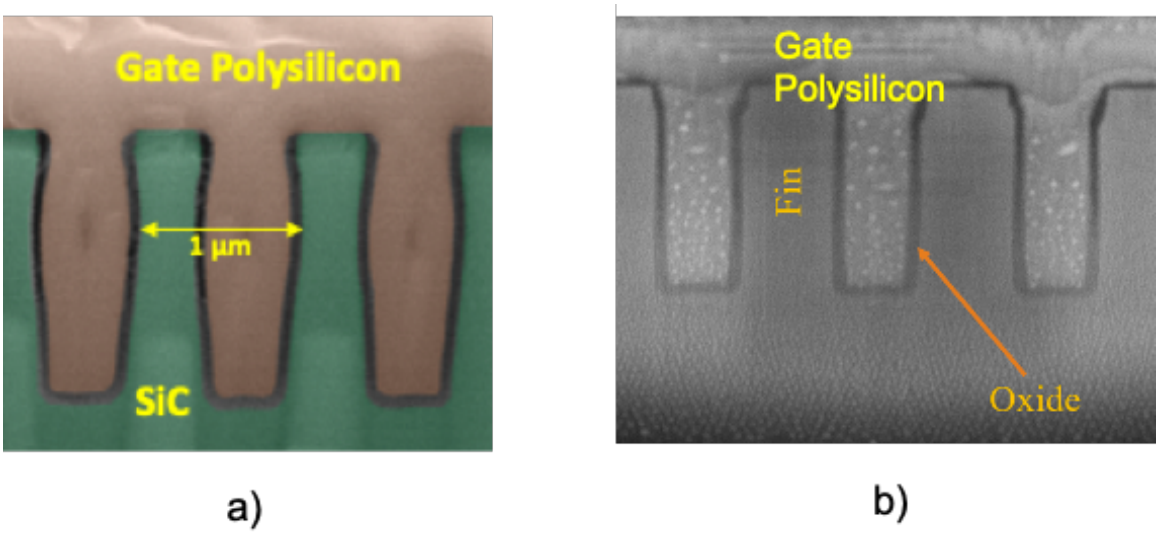


Figure 4.34.: Cross section SEM images showing conformal oxide over SiC trenches using the poly-ox process a) Trench depth of 2 µm b)Trench depth of 1 µm.

Conformal deposition of oxide over the trenches is an important aspect of the poly-ox process. During device operation, a positive voltage is applied on the gate to turn on the transistor, and the electric field in the oxide is expected to be the highest at the top and bottom corners of the trench due to field crowding. In the blocking state, some part of the electric field is expected to terminate in the oxide at the bottom of the trench. Thinning of the oxide near these corners could lead to excess gate leakage or premature failure of the device. In addition, the resulting channel includes regions on the top, sides, and bottom of the fins, and it is important that these regions have similar threshold voltages. Conformal deposition of the oxide on the trench geometry is therefore crucial. To determine the uniformity of the resulting oxide thickness, we took several cross-sectional SEM images. First, trenches were etched in SiC using an e-beam-defined metal mask and an ICP-RIE process using an SF_6-based chemistry. The trenches were 2 µm deep and 0.5 µm wide, with a pitch of 1 µm. The samples were then cleaned using the standard wet chemical RCA process and gate oxide was formed using the poly-ox process.

The trenched area was milled on a test sample to create a cross-section using the Quanta FEG focused ion beam (FIB), after filling the trenches with polysilicon. The ion beam energy and accelerating voltage were carefully adjusted to ensure the integrity of the $SiC - SiO_2$ interface. Figure 4.34 shows SEM images of the resulting cross-sections taken using a cold field-emission microscope at a rotation angle of 70°. To obtain good contrast during imaging, the samples in Figure 4.34 were subjected to a 30 sec HF dip to recess the oxide under the gate. This is done to eliminate electron build up in the oxide film during SEM imaging which causes the "charging effect" [113] and diminishes the contrast between the polysilicon gate and gate oxide regions. As seen in the figure, the poly-ox coverage is 100%, and a conformal gate oxide is present both the top and bottom of the trench. It was also observed that the oxide on the top of the fin is 1.15x thicker than that at the bottom of the trench.

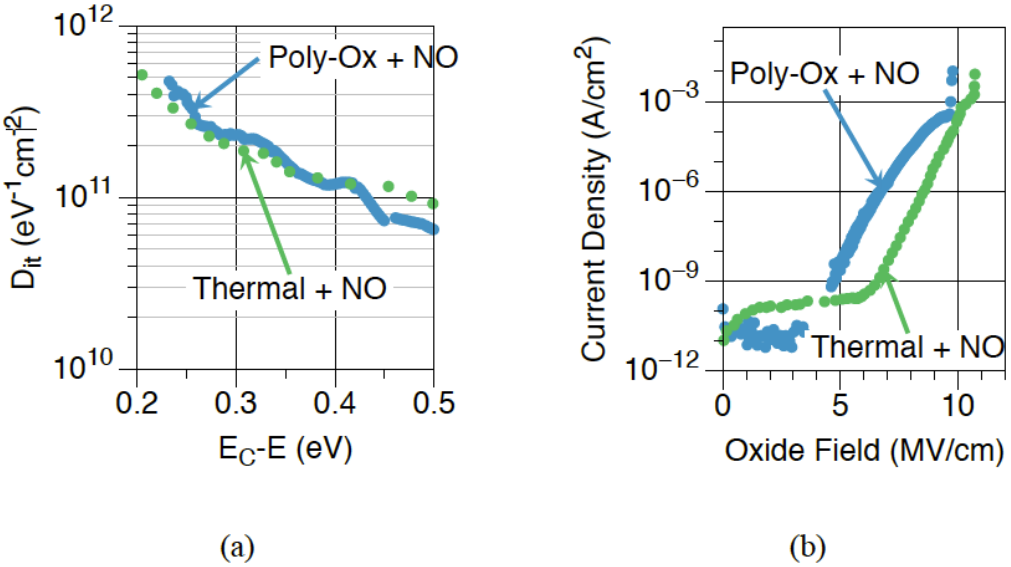


Figure 4.35.: Electrical characterization of an oxidized polysilicon gate oxide with an NO anneal. a) Interface trap density(D_{it}) vs energy with respect to conduction band measured using high-low technique, b) Gate leakage current as a function of oxide field. The measured D_{it} and dielectric breakdown of the poly-ox process is comparable to the standard thermal oxide, b)

Process development and optimization of the poly-ox process has been done to have a) low gate leakage current, b) high oxide breakdown field comparable to thermal oxide, and c) low density of interface traps at the $SiC-SiO_2$ interface. To achieve this the samples are annealed in a nitric oxide (NO) ambient at 1175°C for 2 hours. This is a MOS capacitors were then fabricated and the oxides were electrically characterized to determine leakage current, fixed charge, interface trap density, and oxide breakdown field. The effective fixed charge is positive and calculated from the lateral shift in the flat band voltage to be $q \times 8.5 \times 10^{10}$ cm^{-2}. The interface state density (D_{IT}) measured using the high-low C-V and C-ψ techniques is shown in Figure 4.35(a). The sample shows an interface trap density comparable to typical published data for thermally oxidized and NO-annealed SiC MOS capacitors [75]. The D_{IT} at flatband ($E_C - E_F = 0.21$ eV) is 6×10^{11} cm^{-2}eV^{-1}. The breakdown field is approximately 9 MV/cm based on the I-V data shown in Figure 4.35(b). These values correspond to interfaces on planar surfaces and the values on the trench sidewall and trench bottom in the case of the tirgate structure may be different.

3) Polysilicon gate

A highly doped polysilicon film is used as the gate electrode in trigate devices. There are two main requirements for choosing the gate material:

(a) Ability to conformally fill and planarize the trench geometry.

(b) Compatibility with a self-aligned source contact process

Polysilicon is the best choice of material to meet both these criteria. It can be deposited by LPCVD, and the deposition conditions can be controlled to achieve conformal deposition and planarization of the trench topology. Polysilicon is also compatible with the self-aligned source process, as it can be patterned and thermally oxidized to form an interlayer dielectric (ILD). The thermal oxide that forms over the SiC is much thinner than the ILD that forms on the polysilicon and can be selectively

removed by a short BHF dip without the need for a photomask. This clears the oxide over the N+ source contacts and P+ base contacts. Any gate material needs to be highly conductive, and this can be achieved with polysilicon by using a well understood and widely used spin-on-dopant process. The polysilicon gate process is comprised of three major steps described below.

i) Polysilicon deposition and trench planarization

Polysilicon is deposited by using the LPCVD process described in Section 4.1.3. While a thin layer of polysilicon is sufficient in the poly-ox process, a thick polysilicon film is required to form the gate over the trench geometry in the trigate devices. The ability to uniformly fill and planarize the trenches without any voids is important for good functionality of the gate. High deposition rates lead to higher growth rates near the top of the trenches, which cause pinch-off of the growth and cause voids in the trenched regions. Therefore, the deposition rate needs to be maintained below 15 nm/min for conformal deposition. Process pressure also plays a crucial role. Though the partial pressure at the surface boundary layer determines the deposition parameters, to first order this can be estimated to be proportional to the chamber pressure. High pressure leads to a dense boundary layer closer to the surface that enhances deposition near the top of the trenches and could potentially form voids in the trenches as the deposition progresses. However, very low pressure causes isolated island growth that could cause non uniform deposition on non-planar surfaces such as sidewalls and lead to voids. The process was therefore optimized to operate at a pressure range of 100 mbar to 150 mbar with a temperature window of 570°C to 630°C. Figure 4.36 compares trench filling at two chamber pressure and it can be clearly seen that the higher pressure leads to voids in the trench. The polysilicon needs to fully fill the trenches in order to form the gate, and it must be of sufficient thickness to merge into an essentially planar top surface for further processing. To verify the planarity of the resulting film, polysilicon was deposited on a sample with

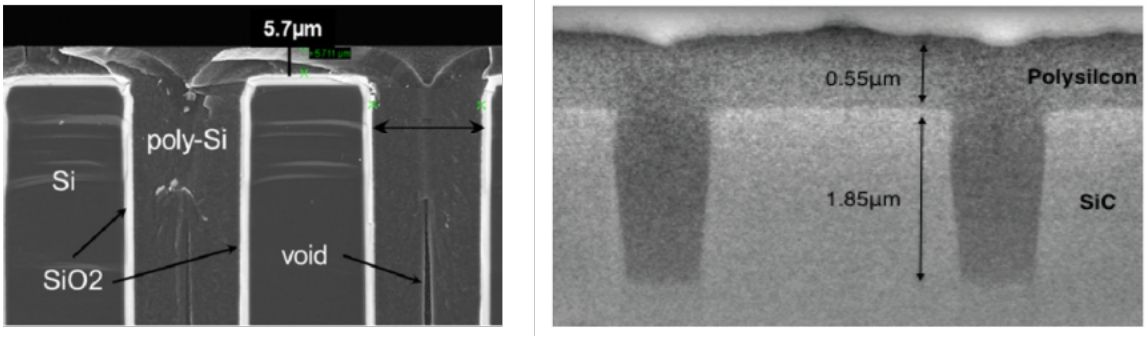


Figure 4.36.: Cross section SEM images of SiC trenches after polysilicon depositon and planarization.a) Polysilicon deposited at 630°C and 500mbarr, b) Polysilicon deposited at 630°C and 150mbarr.

2 µm deep trenches, spaced 0.5 µm and 2 µm apart. The surface was then imaged using atomic force microscopy (AFM), and the results are shown in Figure 4.37. As seen in the figure, the surface above the 0.5 µm wide trenches and fins is planar to within 100 nm. This is sufficiently planar to perform subsequent e-beam lithography steps on the top surface.

ii) Degenerate Polysilicon Doping

Dopants can be introduced into the polysilicon in a number of ways. The most commonly used methods are ion-implantation, spin coating, and solid state sources [114]. All these methods require a high temperature drive in process to diffuse and activate the dopant. For N-type doping using phosphorus, another popular method that is used is the introduction of phosphene gas as part of the gas mixture during LPCVD polysilicon deposition [115]. We use the spin-on dopant approach, since uniform high doping concentrations can be achieved without using a highly toxic gas such as phosphene. This process is carried out after the polysilicon film deposition and planarization of the trench structures and is described below.

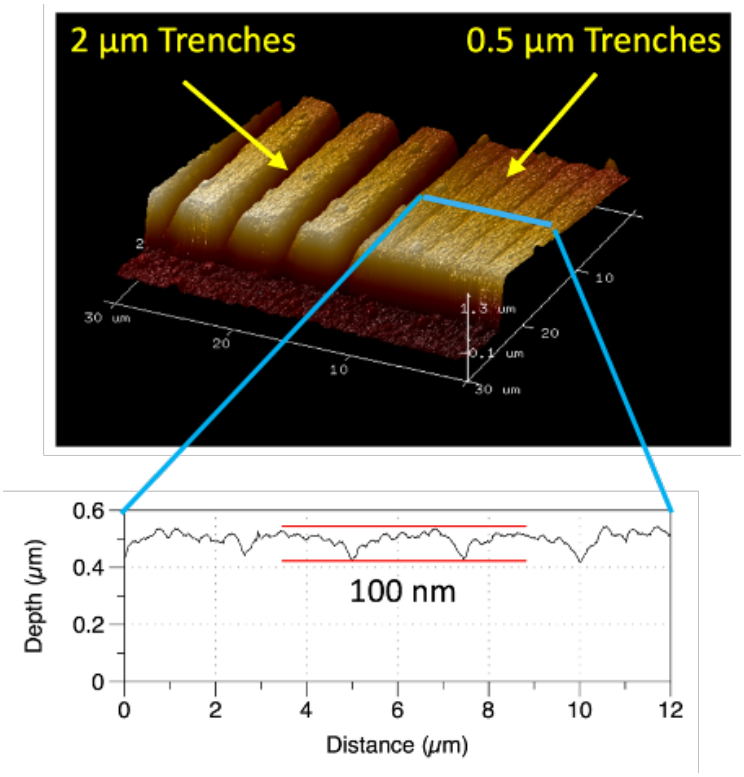


Figure 4.37.: AFM scan of SiC trenches after polysilicon deposition and planarizaiton

Sample Preparation:

Two main factors need to be addressed for sample preparation prior to the doping process. These are i) surface termination, and ii) surface dehydration. Polysilicon surface termination makes the sample either hydrophobic or hydrophilic. A hydrophilic surface is desirable, as it enables uniform wetting of the surface. To achieve this, the polysilicon coated sample is solvent cleaned, followed by two acid cleaning steps. First, a BOE dip is done to strip any non-uniform native oxide from the surface. This is followed by a piranha clean which removes any organic impurities, and creates a thin native oxide which makes the surface hydrophilic. However, hydrophilic surfaces tend to adsorb moisture, which is not ideal since spin-on dopants are highly hygroscopic in nature. Therefore the surface of the sample must be dehydrated prior to spin coating. This is done by baking the sample at 120°C on a clean hot plate, and allowing the sample to cool down to room temperature in a ventilated hood.

Spin Coating and Bake:

The spin-on dopant bottle is usually stored in a refrigerator, and must be removed and placed in a solvent hood for 5 hours to bring the liquid to room temperature before spin coating. To increase the shelf life of the dopant, the liquid is stored in multiple small ($2 - 5$ mL) containers which are discarded after a single use. The smaller bottles require a shorter time to reach room temperature, which is estimated roughly to be one hour. It is important to make sure the dopant reaches room temperature before spin coating. This ensures that moisture does not condense in the bottle and damage the hygroscopic SOD solution. If spin coated while still cold, the coated film thickness is lower, and this causes high sheet resistance. Also, moisture could condense on the sample and this severely impacts the resulting sheet resistance.

Once spin coated, the sample is handled using non-metallic Teflon coated or carbon coated tweezers. A plastic pipette is used to drop the dopant onto the sample. A glass pipette could be used, but more consistent results are obtained by using a plastic pipette. The spinner is carefully covered in aluminum foil such that no metallic surface is exposed. A dedicated spinner chuck is used for this purpose, and the spinner apparatus is thoroughly cleaned with acetone after each run. The spin coat parameters are mentioned in the run sheet (Appendix A and Appendix B). The sample is immediately transferred from the spinner to the hot plate and baked at 200°C for 20 mins. It is important to transfer the sample to the hot plate immediately after spin coating. Fumes lasting for 10-20 seconds are frequently observed as soon as the sample is placed on the hot plate.

Dopant Drive-in:

The dopant drive-in process is carried out at 1000°C in a ProTemp quartz tube furnace, specifically tube 8 in the Birck Nanotechnology Center clean room. The drive-in process flow is shown in Figure 4.38. An experiment was carried out to measure the sheet resistance of 2 µm thick polysilicon films grown on Si-SiO_2 samples,

doped by the spin-on diffusion technique, and driven in at 1000°C for various times. The same dopant bottle was used for all the samples in this run. The result is plotted in Figure 4.39. To independently measure the dopant concentration, SIMS analysis

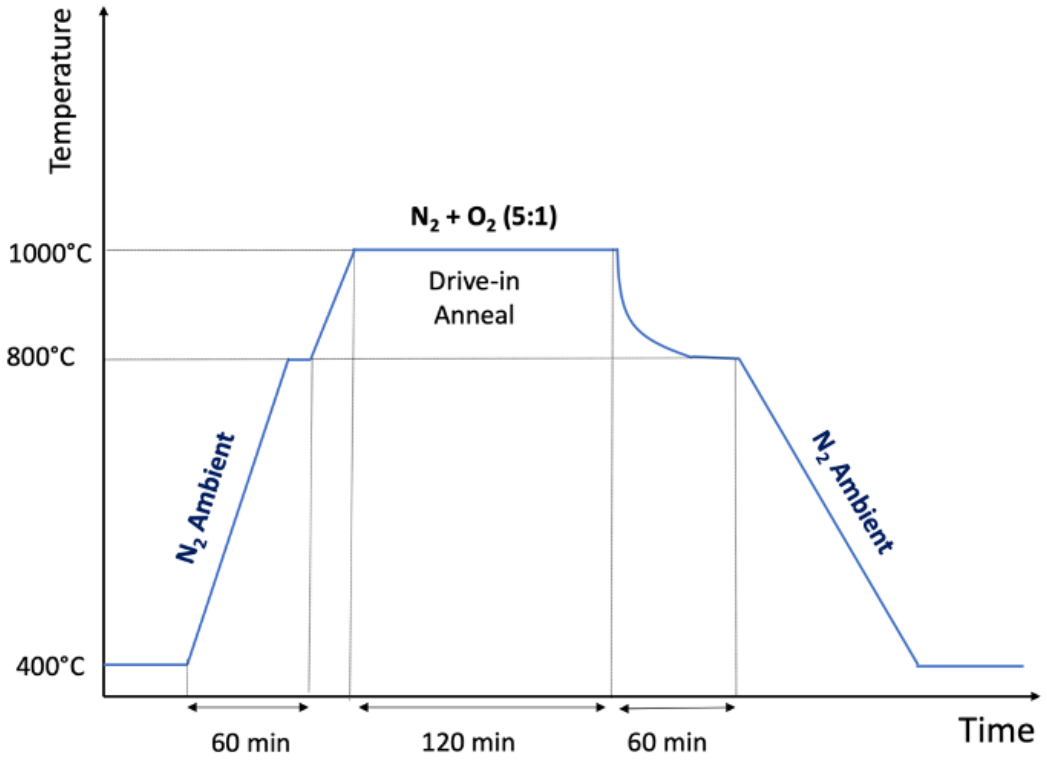


Figure 4.38.: Spin-on dopant drive-in process flow used for polysilicon gates.

was done on one of the samples with a drive-in time of 30 min. A plot of carrier concentration as a function of depth is shown in Figure 4.40. The doping concentration is relatively constant throughout the polysilicon film, and a slight pile-up of dopants on the polysilicon side of the poly-SiO_2 interface is observed. The following practices are critical to the successful doping of polysilicon films using the spin-on diffusion process:

(i) Warming the dopant up to room temperature before spin coating.

(ii) Dehydration of sample surface just prior to spinning of dopant, pipette used to dispense the dopant.

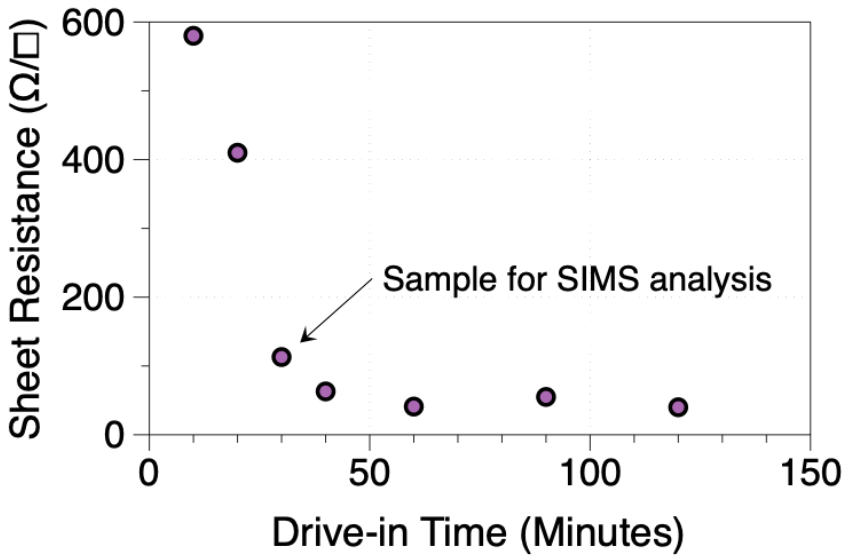


Figure 4.39.: Sheet resistance of a 2 µm thick polysilicon layer as a function of drive-in time at 1000°C.

(iii) Immediate transfer of sample between spinner and 200°C hot plate.

Single and double diffusion of polysilicon

Ideally, the potential drop in the gate electrode should be negligible. However, a low doping concentration at the trench bottom could cause depletion in the polysilicon gate and could lead to a significant potential drop in this region. As seen in the SIMS profile in Figure 4.40, the doping at the bottom of the 2 µm film is about 1×10^{18} cm^{-3}. An experiment was carried out to determine the extent of polysilicon depletion that might occur in the trigate devices by using the doped polysilicon of similar thickness as the gate electrode on MOS capacitors fabricated on N-type SiC samples. The gate oxide was 55 nm thick, and was formed by the poly-ox process described in the previous section. A 2 µm thick polysilicon film was deposited by LPCVD at 630°C and the film was doped using the spin-on dopant process with a drive-in temperature of 1000°C for 60 minutes. C-V measurements were then done on the MOS capacitor

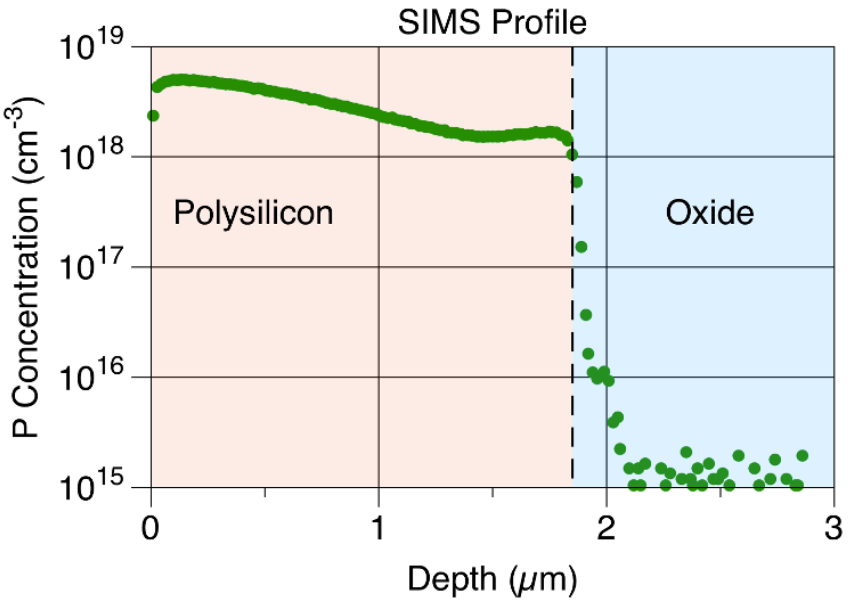


Figure 4.40.: SIMS profile of phosphorus in a $\sim$ 2 µm thick LPCVD deposited polysilicon film doped by diffusion from a spin-on dopant source at 1000°C for 30 minutes using the process depicted in Figure 4.38.

using an HP4284 LCR meter at a frequency of 100 kHz and a small signal amplitude of 20 mV. The same samples were then solvent cleaned, and the doping process was carried out for a second time on the patterned polysilicon gates. C-V measurements were once again performed, and the results from both the singly- and doubly-diffused samples are shown in Figure 4.41.

When a positive voltage is applied to the gate, the positive gate charge images onto negative charge in the SiC from the electrons in the accumulation region at the surface. This sets up a positive field in the oxide, and therefore to maintain the continuity of the displacement field at the polysilicon-oxide interface, there is an electric field and a positive slope to the conduction band (i.e. a depletion region) in the N-type polysilicon. In other words, the electrons in the accumulated SiC image onto positive charges in the space-charge that resides in the depletion region of the polysilicon gate.

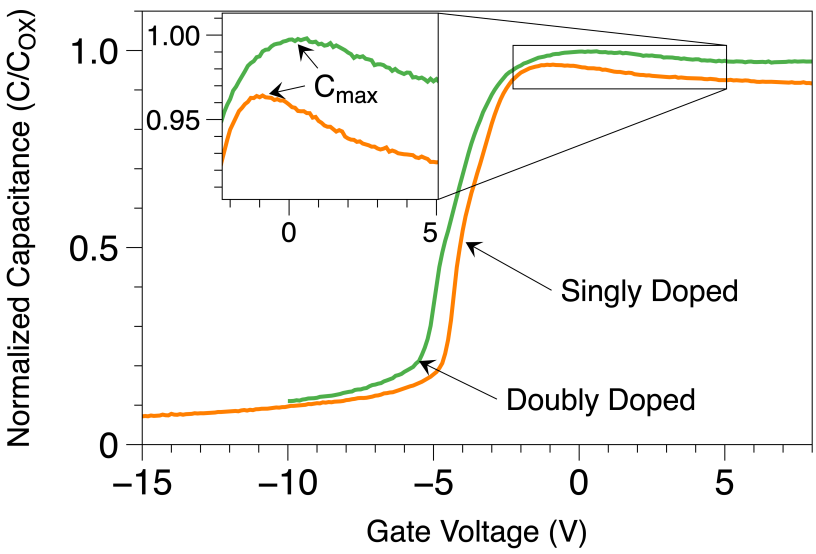


Figure 4.41.: Capacitance vs Gate Voltage for single and double doping of polysilicon gate.

The band diagram of an N-type MOS capacitor with a doped polysilicon gate is shown in Figure 4.42. Therefore, assuming no charge in the oxide or in interface states, the gate voltage can be expressed as the sum of the potential drop in the polysilicon (ψ_{poly}), oxide (ψ_{OX}) and the SiC substrate (ψ_{SiC}), plus the work function difference between the gate and substrate (ϕ_{ms}):

$$V_G = \psi_{OX} + \psi_{SiC} + \psi_{poly} + \phi_{ms} \tag{4.2}$$

where ψ_{OX} is the potential drop across the oxide, ψ_{SiC} is the surface potential or potential drop in the semiconductor, and ψ_{poly} is the surface potential in the polysilicon gate. The potential drop in the oxide is given by $\psi_{OX} = -Q_{SiC}/C_{OX}$. The measured capacitance as a function of gate voltage is given by

$$C_{measured} = -\frac{\partial Q_{SiC}}{\partial V_G} \tag{4.3}$$

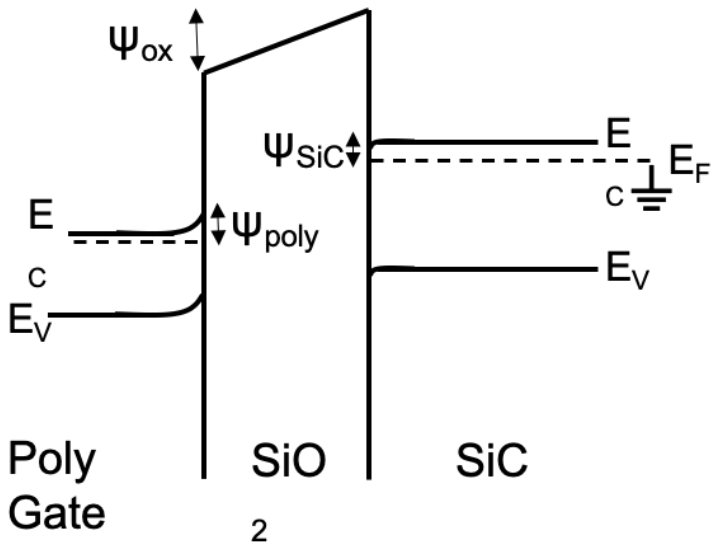


Figure 4.42.: Band diagram of a polysilicon gated N-type MOS capacitor in accumulation.

Now substituting the expression for V_G we get

$$C_{measured} = \frac{-1}{\frac{\partial \psi_{OX}}{\partial Q_{SiC}} + \frac{\partial \psi_{SiC}}{\partial Q_{SiC}} + \frac{\partial \psi_{poly}}{\partial Q_{SiC}}} \tag{4.4}$$

Assuming that all the additional charge in the resides in the accumulation layer at the surface and no charge resides in interface states or in the oxide, the above equation can be written as

$$C_{measured} = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_{SiC}} + \frac{1}{C_{poly}}} \tag{4.5}$$

Here C_{OX} is the oxide capacitance, C_{SiC} is the accumulation layer capacitance and C_{poly} is the capacitance of the polysilicon depletion region. Accumulation charge increases exponentially with surface potential [116] and the corresponding accumulation capacitance is given by

$$Q_{SiC} \propto e^{-\frac{q\psi_{SiC}}{2kT}}$$

$$C_{SiC} = -\frac{\partial Q_{SiC}}{\partial \psi_{SiC}} = \left(\frac{q}{2kT}\right)|Q_{poly}| \tag{4.6}$$

Assuming no charge in the oxide and interface states, by condition of charge neutrality, the depletion charge the polysilicon is equal in magnitude to the charge in the SiC accumulation layer. The depletion charge in the polysilicon gate and the corresponding capacitance can be expressed as

$$Q_{poly} = \sqrt{2\varepsilon_{Si} q N_D \psi_{poly}} \tag{4.7}$$

$$C_{poly} = -\frac{\partial Q_{SiC}}{\partial \psi_{poly}} = \frac{\partial Q_{poly}}{\partial \psi_{poly}} = \frac{\sqrt{2\varepsilon_{Si} q N_D}}{2\sqrt{\psi_{poly}}} \tag{4.8}$$

$$C_{poly} = \frac{\sqrt{2\varepsilon_{Si} q N_D}}{2\left[\frac{Q_{poly}}{\sqrt{2\varepsilon_{Si} q N_D}}\right]} = \frac{\varepsilon_{Si} q N_D}{Q_{poly}} \tag{4.9}$$

When the gate voltage is increased above flat band, the thickness of depletion region in the SiC collapses and the measured capacitance increases towards the oxide capacitance. However, there are two competing capacitance components in series with the oxide capacitance as seen in (4.5). With an increase in gate voltage, accumulation charge, and therefore the corresponding depletion charge Q_{poly} in the polysilicon increases. The accumulation capacitance C_{SiC} increases as it is proportional to Q_{poly} (4.6) while the polysilicon depletion capacitance is proportional to $^1/_{Q_{poly}}$ (4.9) and therefore decreases. In (4.5), as C_{OX} is a constant for a given oxide thickness, a maximum capacitance is reached when C_{poly} is equal to C_{SiC}.

The expression for the maximum capacitance is obtained by equating the expressions for C_{poly} and C_{SiC} substituting in (4.5) to get,

$$C_{measured,max} = \frac{1}{\frac{1}{C_{OX}} + \left[2 \times \sqrt{\frac{2kT}{\varepsilon_{Si} q^2 N_D}}\right]} \tag{4.10}$$

Equation 4.10 indicates that in the presence of polysilicon gate depletion, the capacitance never reaches the value of C_{OX} in accumulation. Once the capacitance reaches the value of $C_{measured,max}$ given by (4.10), it starts to decrease as the voltage is further increased. If the doping in the polysilicon(N_D) is high, then the second term in the denominator of (4.10) becomes negligible and the measured capacitance approaches the true value of C_{OX}.

The maximum capacitance feature in accumulation is clearly visible in both the singly- and doubly-doped samples as seen in the inset of Figure 4.41. The effect is however significantly reduced by doping the polysilicon gate twice. By determining the maximum measured capacitance in accumulation and then using (4.10), the polysilicon doping for the singly doped sample is found to be 4×10^{18} cm^{-3}. Using the same technique, the polysilicon doping after doping twice is found to be 1.2×10^{19} cm^{-3}.

Another technique that can be used to measure the polysilicon is the plot of $1/C^2$ as a function of gate voltage [117]. Usually, this technique is used to measure the doping of the semiconductor by using the slope of the $1/C^2$ vs. gate voltage in the depletion regime. To determine the doping of the polysilicon, the same technique is employed in the accumulation regime when the polysilicon is in depletion. This can be thought as using the N -type substrate as a gate to modulate the depletion capacitance of the polysilicon region. Such a plot for the singly- and doubly-doped polysilicon is shown in Figure 4.43. The polysilicon dopings extracted with this method are consistent with those extracted using the maximum capacitance as described above. Both of these methods do not account for charges in the oxide and in interface traps, and

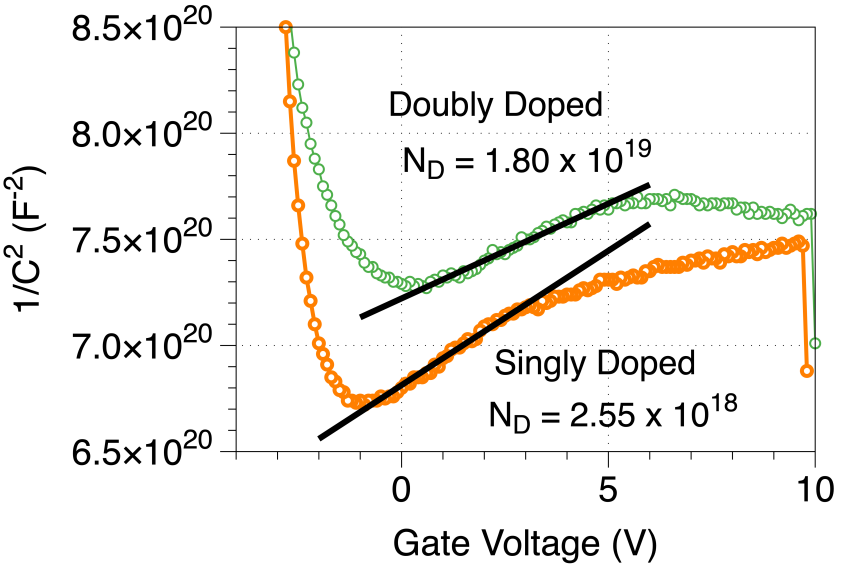


Figure 4.43.: Plot of $1/C^2$ vs gate voltage for a N-type MOS capacitor with a signly and doubly doped polysilicon gate.

therefore slightly overestimate the polysilicon doping. The presence of charge in the interface traps and the corresponding capacitance(C_{it}) adds an additional term in the denominator of (4.5). In accumulation, the contribution of C_{it} which is in parallel to a large accumulation capacitance C_{SiC} would be small.

The above analysis shows that double diffusion doping of the gate polysilicon is required to achieve a sufficiently high doping concentration at the bottom of the trigate trench to minimize polysilicon depletion effects.

4) Gate patterning and etch

The last step in the gate stack process is the patterning and etching of the gate fingers. Once the topology of the SiC trenches is planarized by polysilicon deposition, lithography for the gate etch is done in two steps, where the gate fingers in the active area are patterned using electron beam lithography, while optical lithography is used to pattern the field areas and test structures. Electron beam lithography is required

to obtain good alignment between the gate fingers and implanted P-base regions in the active area. The process flow of the polysilicon gate etch is illustrated in Figure 4.44.

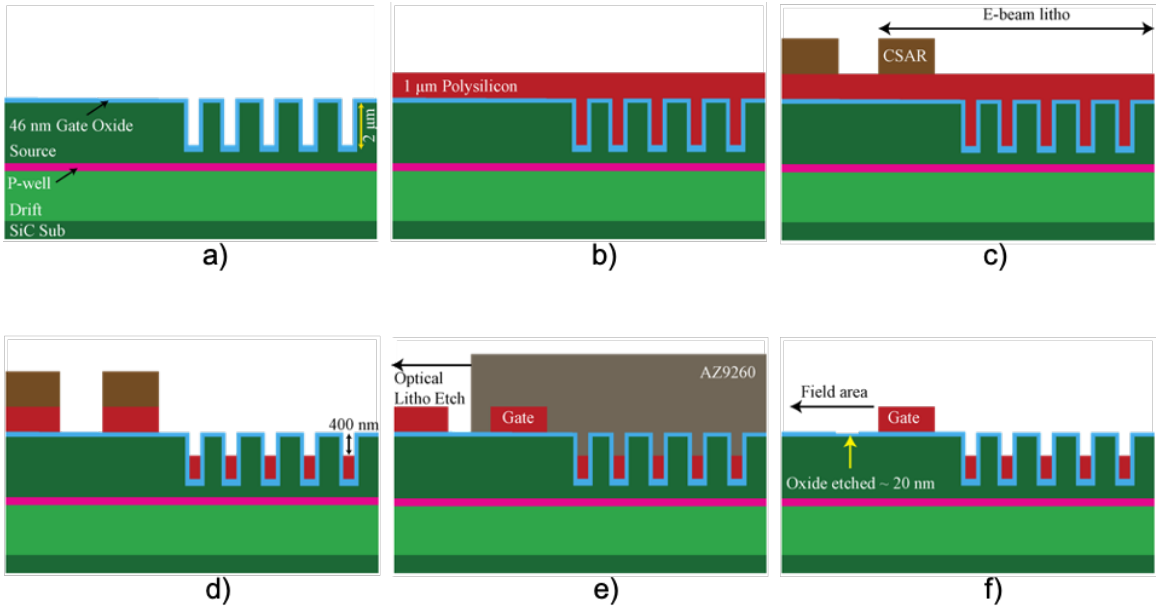


Figure 4.44.: Polysilicon gate etch process flow illustrated by cross-sections along the line A-A' in Figure 3.24 (a) trench etch and poly-ox gate oxide deposition, (b) 1 µm thick polysilicon deposition using LPCVD and degenerate doping by spin-coating and diffusion, (c) e-beam lithography using CSAR resist and 30 nA exposure, (d) poly gate etch using the Bosch process and the CSAR mask, (e) AZ9260 pattern for field area polysilicon etch, and (f) Polysilicon etch in field and test structure areas.

The polysilicon etch process was originally developed for the high energy implantation mask, and is described in Section 4.1.1.2. The same process is used for the polysilicon gate etch, since no difference is found between the etching of doped and undoped polysilicon films. An STS ASE ICP-RIE tool is used for the polysilicon etch with the conditions listed in Table 4.3 for 125 sec. The photoresist mask may become hardened during this step, and a long soak in PG remover for more than 5 hours at 80°C is usually required to remove the resist. An ashing step in the Branson barrel

etch tool is also done with Ar/O_2 (120/6 sccm) plasma and a power 300 W for 3 min. A consistent and accurate etch rate and vertical sidewalls are obtained using this process, as seen in Figure 4.45.

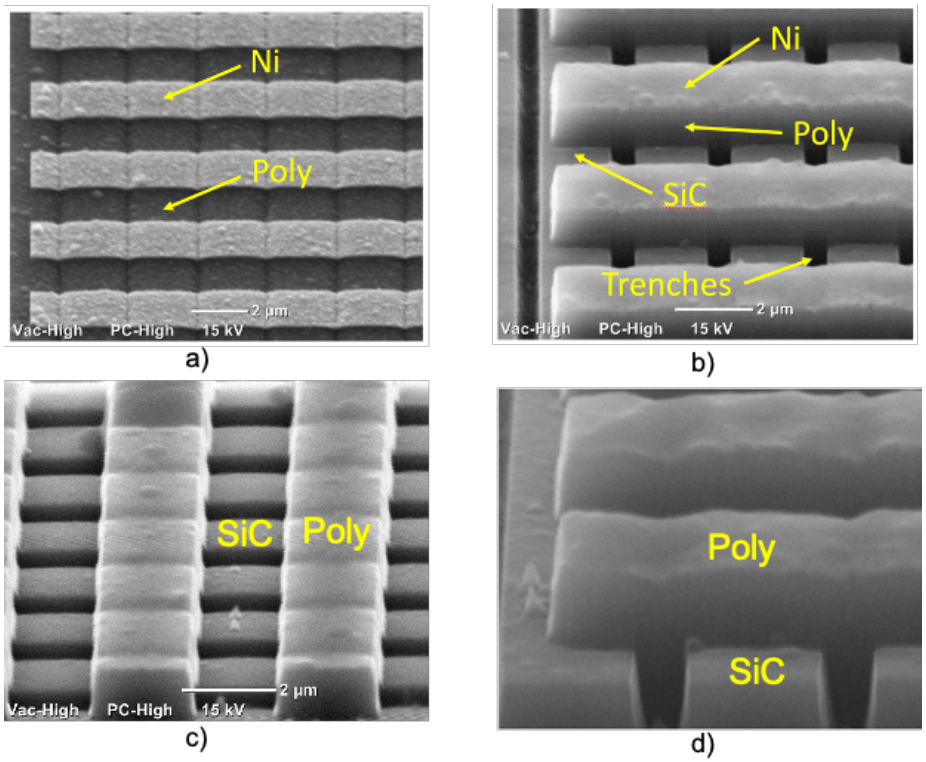


Figure 4.45.: SEM images of the polysilicon gate etch using SF_6/O_2 RIE is the STS-AOE ICP. (a) Nickel mask patterned using e-beam lithography over planarized SiC trenches, (b)-(d) Polysilicon gate fingers defined over SiC trenches.

The gate polysilicon is first etched to just below the top the the trench to expose the source regions. The etch is then continued until polysilicon is recessed 400 nm from the top of the trench as shown in Figure 4.44(f). This is done to ensure that the silicon dioxide grown thermally in the following step does not balloon out of the trenches and reduce the effective source contact opening. Another option is to completely remove the polysilicon from the trenches, but there are two advantages of not doing so. First is a reduction in unintentional etching of SiC in the source regions, and second is the fact that SiO_2 formed in the trenches during the ILD

oxidation increases the gate-source capacitance, which may be beneficial in improved balancing of the gate-drain capacitance [118].

4.1.4 Ohmic Contacts

Low resistivity ohmic contacts to the source region are important to the operation of the trigate MOSFET. In trigate devices, the source ohnmic contacts are self-aligned to the gate, and are formed using the nickel silicide process. In this process a thin film of Ni is first deposited over the entire active area. The nickel is now over the exposed SiC in the source windows and also over the ILD oxide. This is followed by an anneal at ($> 700°C$) is done to form the silicide in the exposed SiC windows. The Ni does not react with the oxide, and is removed from these regions by a blanket wet etch. Finally, a high temperature anneal at 1000°C is done to achieve low contact resistance.

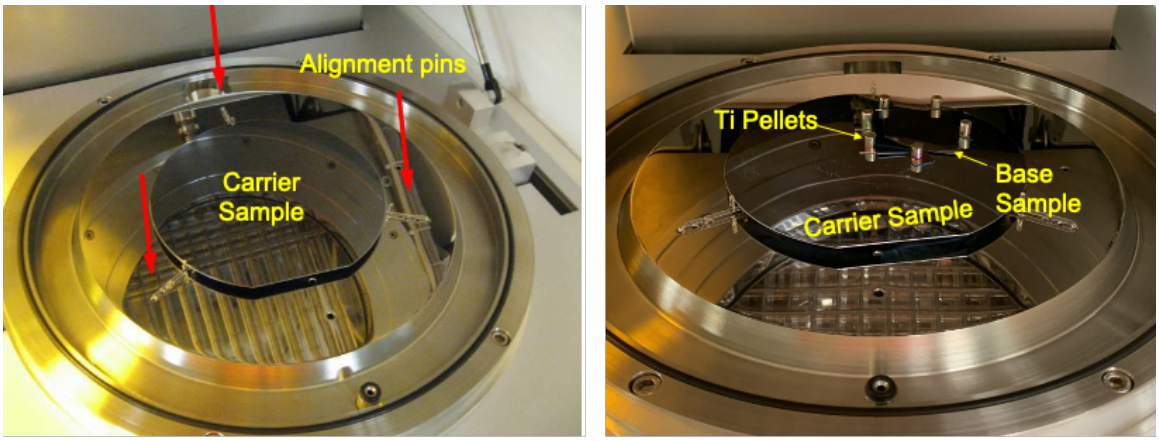


Figure 4.46.: Sample loading sequence in the Jipelec RTA for ohmic anneal. a) Carrier wafer loading and alignment, b) Base sample with Ti pellets for O_2 gettering

It has been observed that the contact resistivity obtained using the nickel silicide (NiSi) process in SiC is quite sensitive to surface preparation. Sample preparation prior to Ni deposition is performed as follows. First, the sample is solvent cleaned in

toluene, acetone, and methanol for ~ 10 min each to remove any inorganic contaminants. Only optical lithography is required to pattern the test and PCM regions, and therefore a bi-layer resist of 0.4 µm thick LOR-3B and 1.8 µm AZ1518 are spin-coated on the sample. The LOR-3B resist is baked at 190°C to minimize undercut. Exposure is then carried out in a Heidelberg laser writer tool with a dose of 225 mJ/cm^2, and the sample is developed in MF26A for $\sim$ 30 sec. Next, an O_2 barrel etch is done using Ar/O_2 plasma at 100 W for 1 min to remove any photoresist residue on the SiC surface. The next step is to remove all oxide on the surface where the nickel silicide will be formed. This is done by a wet chemical etch in BOE for 45 sec to remove the $\sim 46 - 50$ nm thick gate oxide. This exposes the source regions in both the active area and the test structures. To increase the surface area in these areas, an RIE etch is done using the Jupiter RIE tool for 30 seconds with the parameters listed in Appendix A. This is a physical etch which also removes oxide at the rate of $\sim$ 30 nm/min and ensures that any remaining oxide after the wet etch is completely removed. There is a possibility of the formation of flourinated polymers (C_xF_y) during the above RIE etch due to the presence of SF_6, O_2 and C. Therefore, a second O_2 barrel etch is done at 200 W using the Branson etcher to oxidize away the polymer residues. Finally, a wet chemical etch in BOE is done for 20 seconds to remove any residual oxide that may have formed on the surface during the ashing step. The sample is then immediately loaded into the e-beam evaporator chamber where Ni is deposited at 1.5 Å/sec rate. The pressure of the chamber is maintained below 1×10^{-6} Torr during the deposition to ensure minimum exposure of the SiC surface to O_2.

The high temperature NiSi anneal is done using a rapid thermal anneal (RTA) furnace at temperatures in the 700°C - 900°C window in an inert ambient. It is important not to allow any oxidation of the surface during the sintering process, as it significantly increases the contact resistivity. Therefore the following procedure is followed in order to obtain low contact resistivity using the Jipelec Jetfirst 2000 RTA tool in the Birck Nanotechnology Center. First, a 6 inch Si carrier wafer used in the RTA tool is solvent cleaned, followed by a piranha clean. The carrier wafer is then

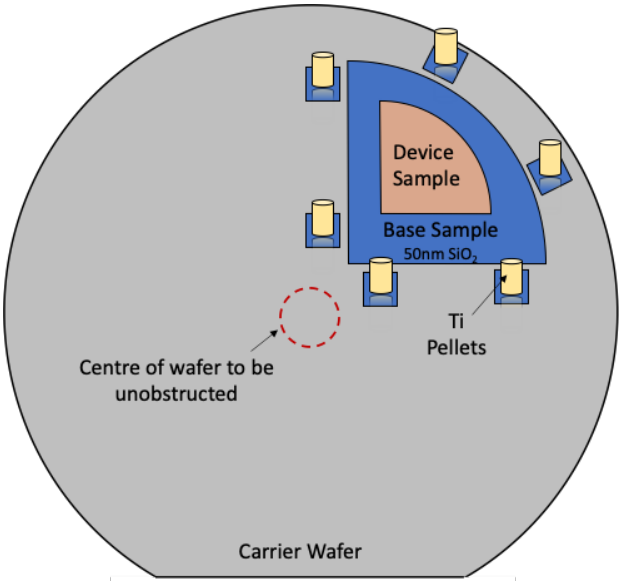


Figure 4.47.: Sample arrangement and setup in the Jipelec RTA for ohmic anneal

placed on a hot plate and baked at 150°C to dehydrate the surface. Another "base sample" carrier wafer which could be either Si or SiC sample with a freshly grown clean thermal oxide is also prepared and cleaned using the same procedure described above. The carrier is first loaded into the RTA chamber as shown in Figure 4.46(a) and the chamber is heated to 1000°C for 5 min to dehydrate any moisture. The chamber is then allowed to cool down with a constant flow of argon. The base sample is loaded with the clean oxide covered surface facing up. Additionally, titanium (Ti) pellets each placed on $\sim 1 \times 1$ cm^2 Si pieces are loaded around the base sample as seen in Figure 4.46(b). The Ti pellets are used to getter oxygen in the chamber. A multi-cycle Ar pump and purge at 550°C for $\sim$ 40 min is also performed to clean and dry the chamber. Once completed, the device sample is loaded face down onto the base sample as illustrated in Figure 4.47. Another multi-cycle pump and purge with Ar flow is performed, but now with the device sample loaded and the chamber temperature at 250°C. The high temperature RTA anneal is then done once the pump and purge cycles are complete.

Using the sample preparation and loading sequence above, an experiment was carried out to determine the contact resistivity as a function of temperature. To do this, TLM test structures were fabricated on N+ implanted wells on a P-type substrate. A 100 nm thick nickel film was deposited, patterned, and annealed as described above, followed by deposition and patterning of a titanium and gold as top metal. The resulting contact resistivity is plotted in Figure 4.48, which shows that a contact resistivity below $1 \times 10^{-5}\ \Omega\,\mathrm{cm}^2$ can be achieved by sintering at temperatures above 850°C. The effects of not applying some of the described sample preparation procedures are also shown in the figure.

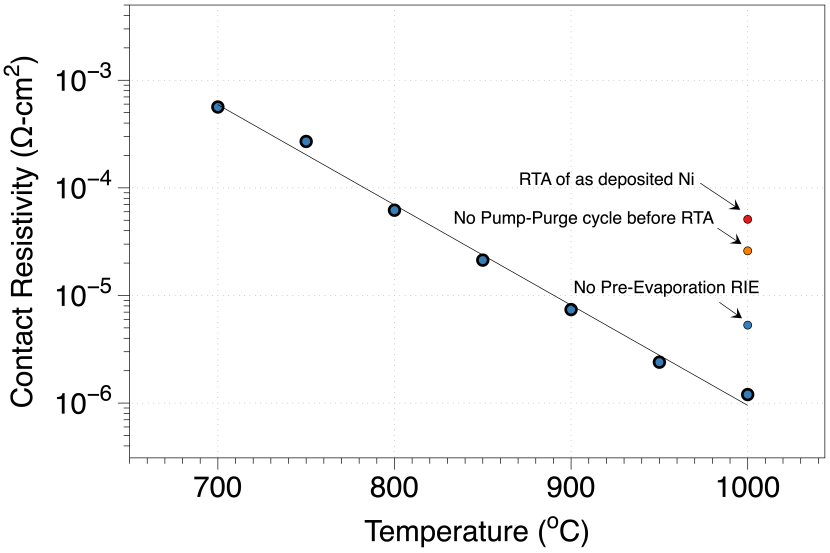


Figure 4.48.: Contact resistivity as a function of annealing temperature

The deposited Ni is consumed during this process, and the penetration into the SiC surface is found to be $\sim 1.3 - 1.4\times$ the original Ni thickness. Therefore the thickness of the deposited Ni film needs to be adjusted to ensure that the silicide does not punch through any underlying junctions and cause unintentional shorts. The initial process development was done with 100 nm of Ni, but the process was later modified to use only 50 nm as discussed in Section 4.2.3.

During the silicidation process, nickel reacts with silicon to form NiSi, but does not react with carbon. Part of the unreacted carbon forms a film on the metal surface and must be removed before top metal deposition. This is done by using a O_2 plasma at 200 W, a pressure of 250 mTorr for 2 minutes, and a flow of 50 sccm in the Jupyter III etch tool.

4.2 Integration into unified trigate MOSFET process

The unit processes developed for the trigate MOSFET are described in the previous section. The integration of the unit processes into a single process for the fabrication of the trigate MOSFET is described in this section. The fabricated devices are designed for two blocking voltages where the trigate MOSFET will have a significant impact: (a) 650 V specification (930 V breakdown), and (b) 900 V specification (1,300 V breakdown). The corresponding drift regions will be (a) 5 µm, doped 1.4×10^{16} cm^{-3}, and (b) 8.4 µm, doped 1×10^{16} cm^{-3}. This assumes a 30% derating factor to account for imperfect edge termination.

In both the cases, an optimized JFET doping of 1×10^{17} cm^{-3} is used, and the JFET region extends to the bottom edge of the P-base region. Two important cross sections through the trigate MOSFET, along with some of the key dimensions are shown in Figure 4.49.

Table 4.4.: Trigate Gen-1 sample information and nomenclature

Sample #	**Wafer #**	**Manufacturer #**	**Drift Layer Thickness**	**Target Blocking Voltage**
1Q3	PU 391	NE0256-28	8.3 µm	900 V
2Q4	PU 397	GY1672-17	5.2 µm	650 V
3Q2	PU 393	NE0256-30	8.5 µm	900 V
4Q2	PU 399	NE0256-06	5.4 µm	650 V

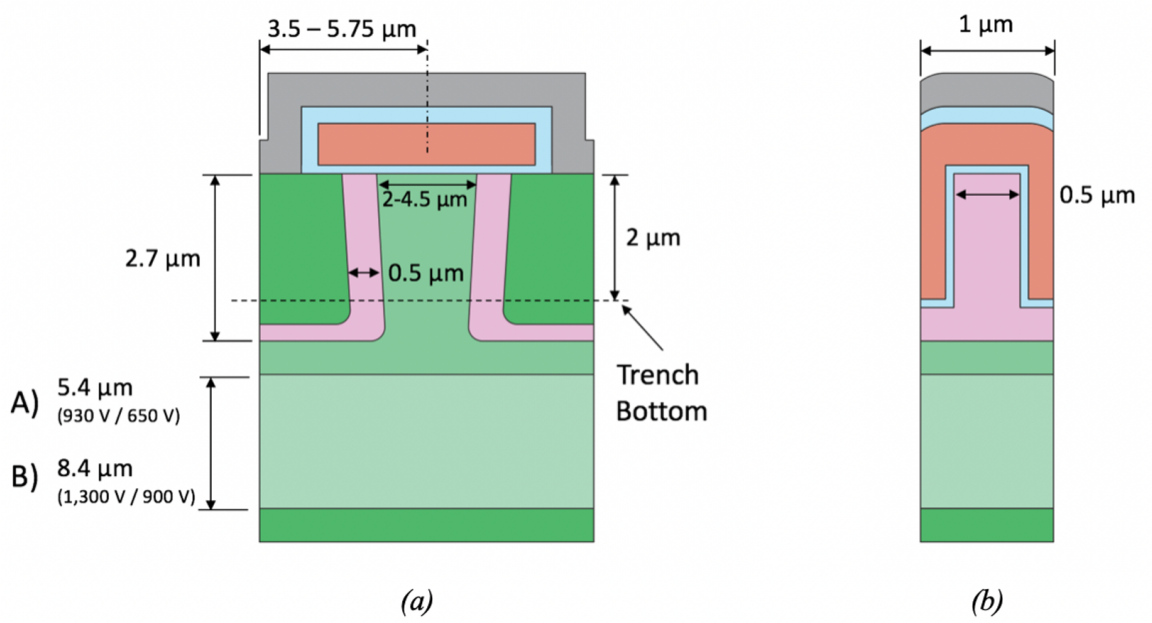


Figure 4.49.: Cross sections of the trigate MOSFET (a) through the fin centerline and (b) perpendicular to the fin through the channel region.

The devices are fabricated on pieces cut from 4 inch SiC wafers, which were purchased from Cree, Inc. The fabrication of the trigate devices is carried out in two waves: generation 1 (Gen-1) with a trench depth of 2 µm and generation 2 (Gen-2) with a trench depth of 1 µm. Gen-1 and Gen-2 are each comprised of four samples, and each sample is a quarter of a 4 inch wafer to accommodate them in the NO anneal 3 inch diameter furnace tube. Each trigate sample is labelled with a unique sample number that is scribed into the back (C-face) using a diamond scriber, and a wafer number for bookkeeping as listed in Table 4.4 and Table 4.5.

The integrated process flow of the trigate MOSFET is illustrated in Figure 4.50. All of the steps, except the ion implantations, are done at the Birck Nanotechnology Center at Purdue University. The optimized process described in Section 4.1 is applied at each step. However, a test run is carried out using the same equipment and process conditions prior to every step applied to the trigate samples. Only when satisfactory

Table 4.5.: Trigate Gen-2 sample information and nomenclature

Sample #	**Wafer #**	**Manufacturer #**	**Drift Layer Thickness**	**Target Blocking Voltage**
400Q1	PU 400	NE0256-07	5.3.0 µm	650 V
400Q4	PU 400	NE0256-07	5.3 µm	650 V
394Q1	PU 394	NE0256-31	8.4 µm	900 V
394Q4	PU 394	NE0256-31	8.4 µm	900 V

results are obtained and the results are consistent with the previously developed processes are the trigate samples processed.

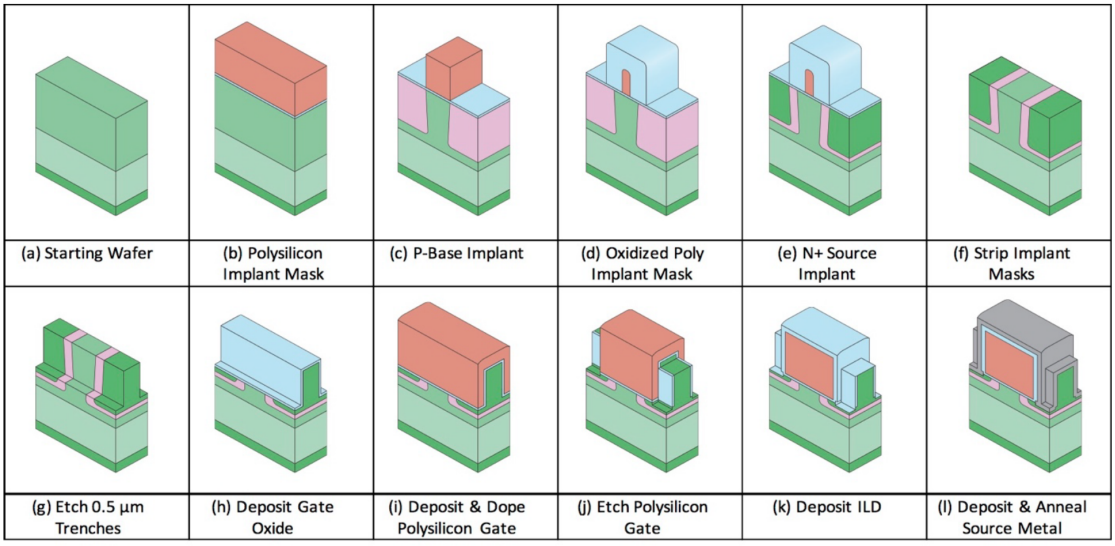


Figure 4.50.: Pictorial depiction of the major process steps in the fabrication of trigate MOSFETs

The high aspect ratio polysilicon implant mask and high energy ion implantation are the most time consuming process steps in the Gen-1 and Gen-2 samples, and therefore all the four samples in each generation have been processed together through these steps. To ensure the trench etch is consistent and uniform in all the samples,

the trench etch step is also carried out in parallel. But once the trenches are formed, fabrication is done in a staggered sequence, providing backup samples in case of an unrecoverable failure or damage in any single process step. This also enables process or design changes based on learning from the leading lot to be applied to other samples in the queue. The fabrication sequence for both Gen-1 and Gen-2 trigate samples is illustrated in Figure 4.51.

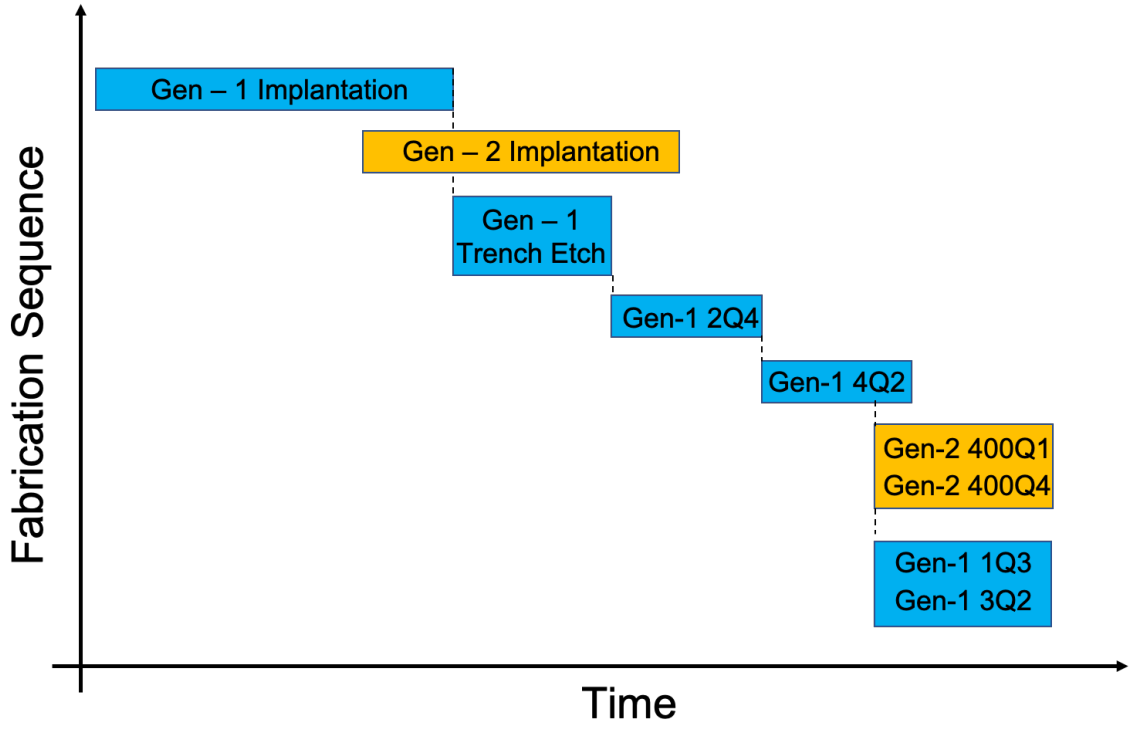


Figure 4.51.: Fabrication sequence of the Gen-1 and Gen-2 trigate samples.

Details of the process integration of each generation are described in this section, and a detailed run sheet for the entire process flow is provided in Appendix A and Appendix B. Fabrication of the Gen-1 trigate MOSFETs is first discussed, followed by the Gen-2 samples, and does not necessarily reflect the timeline in which the samples were processed.

4.2.1 Trigate Gen-1 Fabrication

The Gen-1 trigate lot is comprised of the four samples listed in Table 4.4, and has a trench depth of 2 µm. The wafers purchased from Cree, Inc., have a CSL thickness of 3.2 µm. An additional split relating to CSL thickness was included, where the CSL thickness in one sample from each blocking voltage is thinned to 2.6 µm. The sample details are listed in Table 4.6. The thinner CSL thickness is obtained by etching the top surface of the wafer by 0.6 µm. The blanket etch was performed in an E-620 Panasonic E620 ICP-RIE etcher after calibrating the etch rate using test samples. The samples are then RCA cleaned and a sacrificial oxide is grown by thermal oxidation.

Table 4.6.: CSL thickness information in Gen-1 trigate samples.

Sample #	**CSL Thickness**	**Drift Layer Thickness**
2Q4	3.2 µm	5.2 µm
4Q2	2.6 µm	5.4 µm
3Q2	2.5 µm	8.5 µm
1Q3	3.1 µm	8.3 µm

4.2.1.1 P-type base implant

Polysilcon is used as a mask for the high energy implants. A total thickness of 5.8 µm of polysilicon is deposited by LPCVD at 630°C at 130 mTorr. The polysilicon film is patterned in a two step electron beam and optical lithography process as illustrated in Figure 4.12. An STS ASE ICP-RIE is then used with the parameters listed in Table 4.3 to etch the polysilicon film. SEM images of the etched polysilicon

mask in the active area and floating field rings are shown in Figure 4.52 and Figure 4.53 respectively.

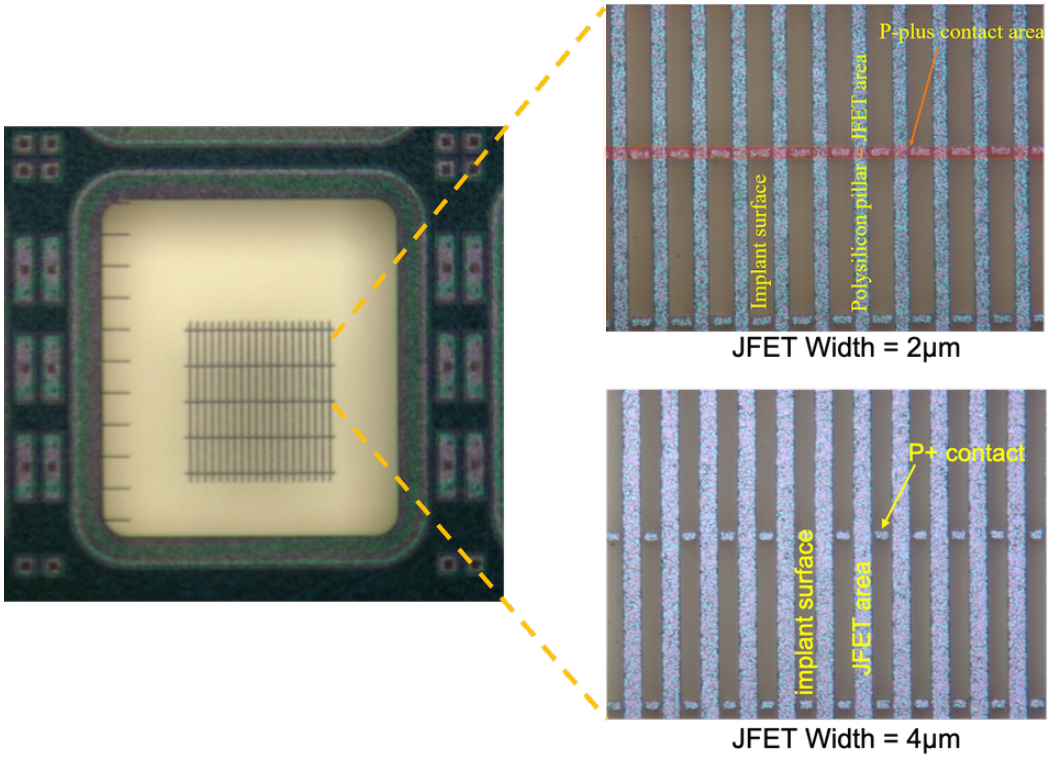


Figure 4.52.: Polysilicon patterned in the active area for the P-base implant mask

The samples are then mounted onto a 5 inch Si carrier wafer and shipped to Ion Beam Services, Inc., in France for the high energy Al implants as shown in Figure 4.54. One SiC test sample and one Si sample with 200 nm SiO_2 and 4.5 µm polysilicon were also loaded onto the same carrier wafer to verify the implant profile by SIMS analysis.

The complete implant schedule and expected profile for the Gen-1 samples is listed in Table 4.1 in Section 4.1.1.1. Due to equipment up-time issues, the implantation was done using two different vendors, and in two steps. First, high energy implants from 680–4248 keV were performed at Ion Beam Services (IBS), and the shallow implant energies from 20–480 keV were then performed at CuttingEdge Ions in Anaheim,CA. All implantations are done at room temperature with 0° tilt and twist angles.

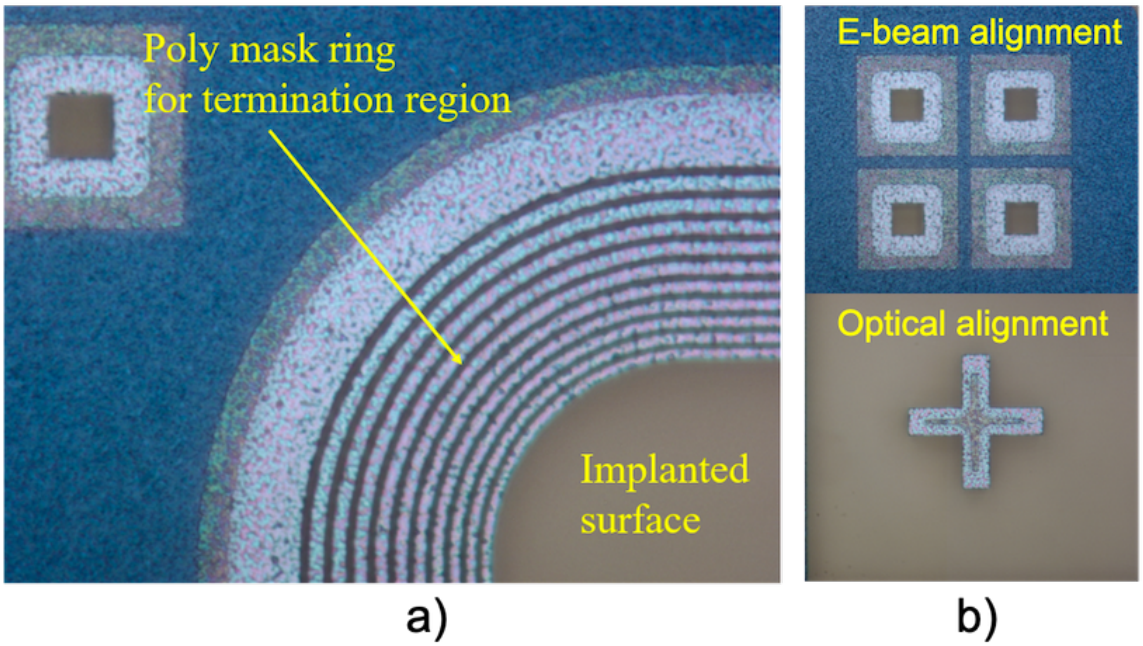


Figure 4.53.: SEM images of floating field rings and alignment marks in Gen-1 sample 4Q2 (a) P-type islands patterned by e-beam lithography in the FFR region, (b) SEM image of the alignment between the optical and electron beam layers. The process parameters and alignment is discussed in Section 4.1.1.2.

4.2.1.2 N-type source implant

The polysilicon pillars created during the base implant mask process are thermally oxidized to mask the nitrogen N+ source implant in the active areas. Careful calibration of the oxidation rate is done just prior to oxidizing the trigate samples, since over oxidation cannot be reworked at this step. Oxidation rates similar to that shown in Figure 4.16 were found, and the trigate samples were oxidized for a total of 4 hours and 20 minutes. Top view SEM images of the oxidized polysilicon pillars before and after oxidation are shown in Figure 4.55.

As described in Section 4.1.1.2, a thick film of electroplated Ni is used as the implantation mask in the test areas and PCM structures. Since the surface is oxidized, a conductive seed layer of titanium (Ti) / gold (Au) is evaporated on the sample.

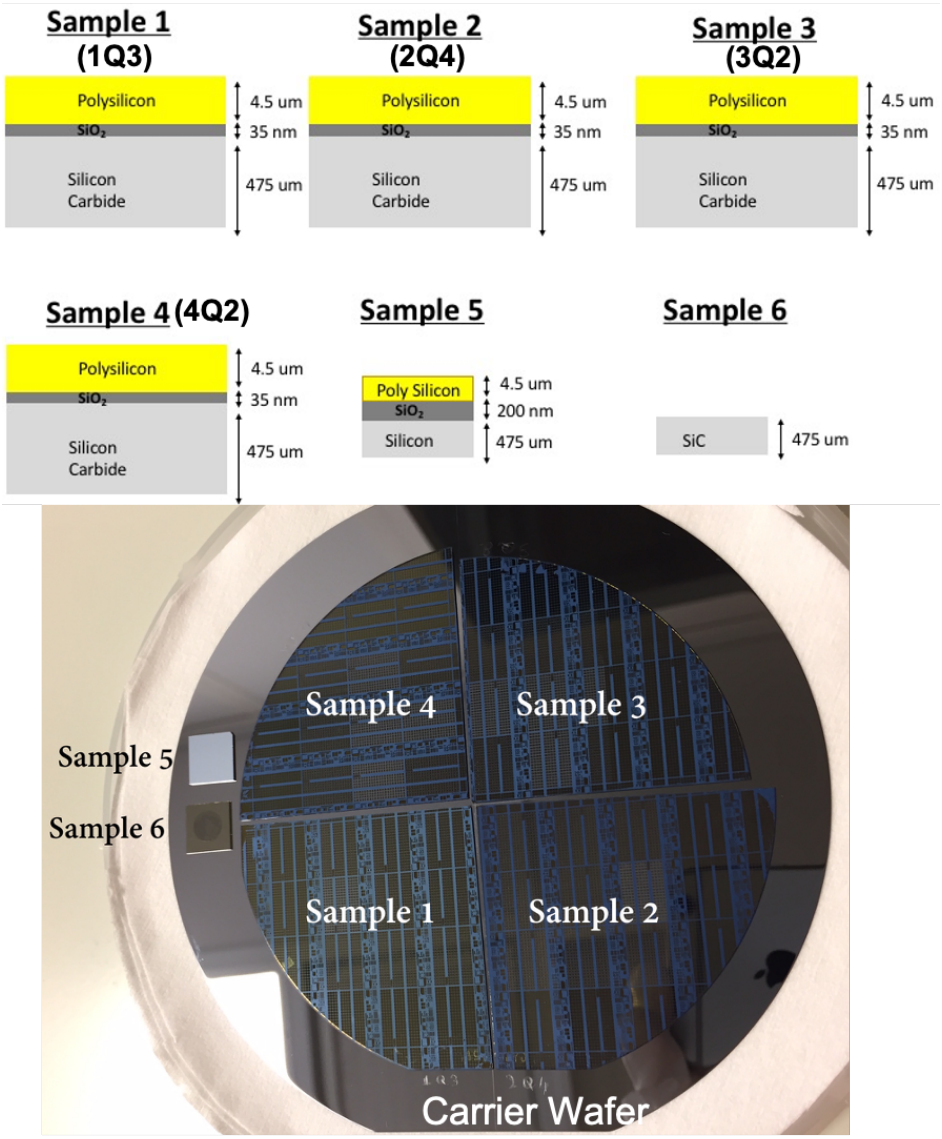


Figure 4.54.: Trigate Gen-1 samples loaded onto a 5 inch carrier wafer for P-base aluminum implant at Ion Beam Services.

Optical lithography is then done to pattern the field and PCM areas using AZ9260 photoresist ($6-8$ µm). The pattern is such that the areas where the nitrogen implant is required are covered by the resist. Electroplating is then done using the custom setup described in [101], and a 3.5 µm thick film of Ni is deposited. The final step is to strip the resist using PG remover at 60°C for 1 hour, followed by removal of the

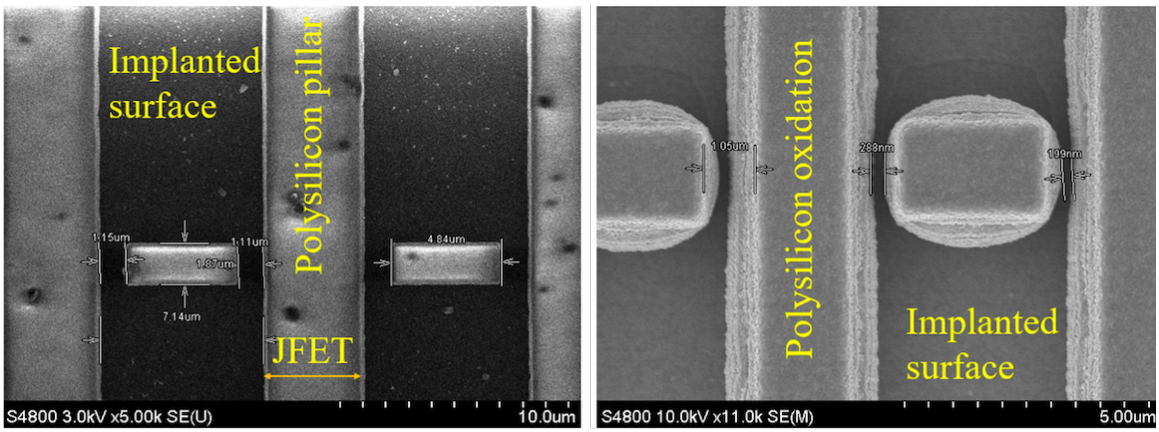


Figure 4.55.: Top view SEM images of polysilicon pillars before and after thermal oxidation to block the nitrogen N+ implant in the active area.

Au seed layer using a Transene GE-8148 Au etch solution. The thin film of titanium on the sample is left unetched to avoid thinning of the oxide mask, as most of the Ti wet etchants are not selective to SiO_2.

The samples are then mounted onto a 5 inch Si carrier wafer similar to Figure 4.54 for nitrogen ion implantation. As discussed in 4.1.1.1, the nitrogen implant is done in two steps, with the high energy, lower dose implants done at room temperature, and the low energy, higher dose implants done at 500°C. The first implants, in the energy range 604–300 keV are done at mi2-GmbH in Germany, and the remaining implants in the energy range 33–380 keV are done at CuttingEdge Ions on a 500°C heated stage. The complete implant schedule for the nitrogen N+ implant is listed in Table 4.2. SIMS analysis is done by Evans Analytical on sample 6 in Figure 4.54, and the aluminum and nitrogen impurity concentrations are shown in Figure 4.56.

Once the base and source implants were completed, the polysilicon mask was stripped using $HF+HNO_3$, which also removes the sacrificial oxide. Therefore a thermal oxidation was done to regrow the sacrificial oxide in preparation for the P+ implant. At this point, the regions with the high energy implants are visible under

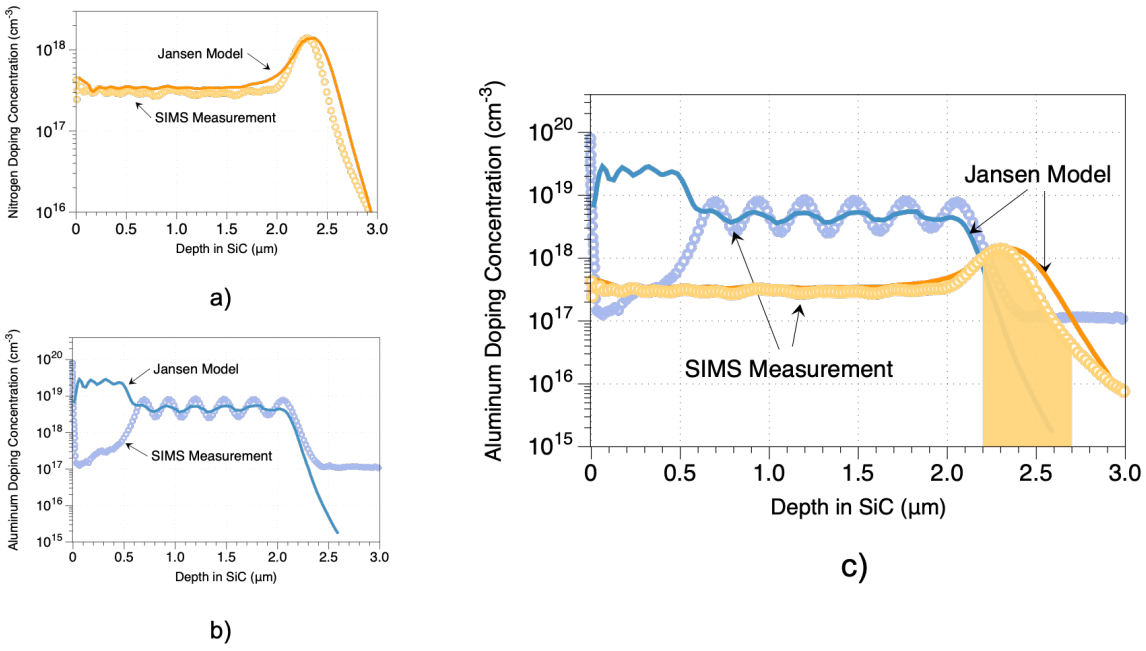


Figure 4.56.: SIMS analysis of high energy ion implants in SiC for the Gen-1 trigate samples. a) Aluminum implant for the P-base, b) Nitrogen source implant for the n-source. The SIMS measurement does not include the low energy implant done at CuttingEdge Ions Inc, while the Janson model does. c) Both aluminum and nitrogen implants. The shaded region is the high dose base implant below the trigate trench.

both optical and electron microscopes before the implant anneal as seen in Figure 4.57.

4.2.1.3 P+ contact implant

A high dose of aluminum is implanted to form the P+ contact regions in the trigate devices using a two step lithography process similar to the P-base implant. In this case, a 350 nm thick nickel mask is used. The active areas are patterned using ebeam lithograhy, and optical lithography is used to define the field and test structures as shown in Figure 4.58. The samples are then mounted on a Si carrier

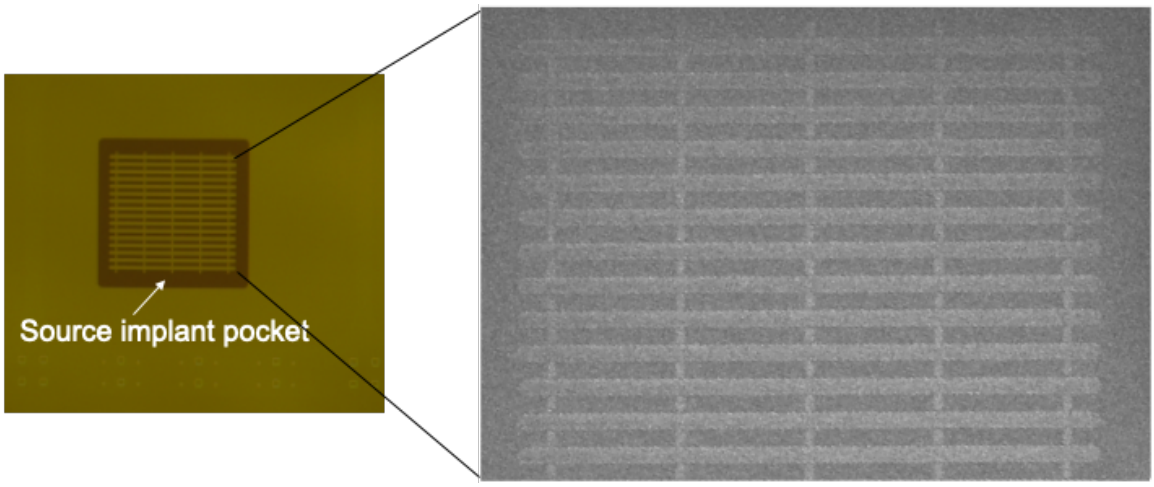


Figure 4.57.: Optical micrograph and SEM images of the active area after the high energy base and source implants, but before the high temperature implant anneal.

wafer and the aluminum implantation is done at CuttingEdge Ions using the implant schedule listed in Table 4.7.

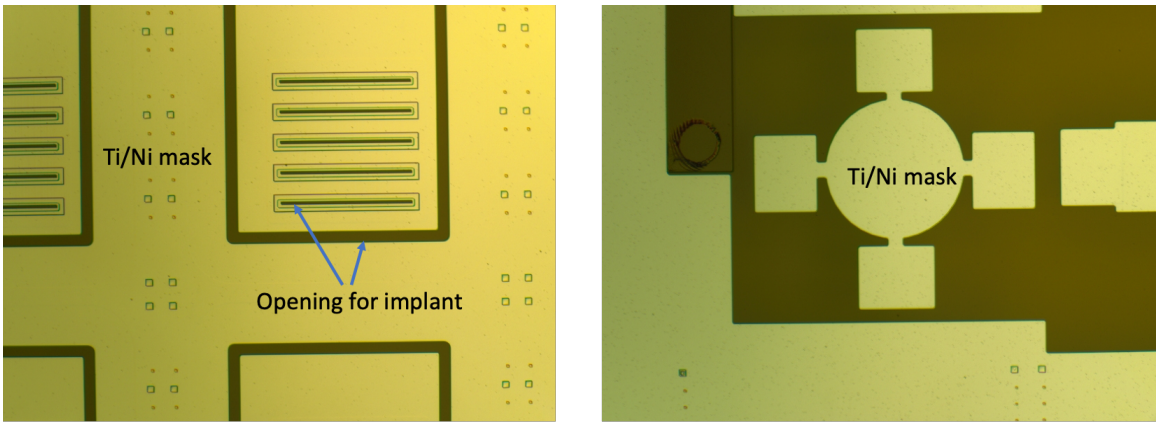


Figure 4.58.: Optical micrograph images of Gen-1 trigate samples with a nickel mask prior to P+ implantation.

Table 4.7.: Gen-1 trigate – P^+ implant profile

Energy (keV)	Dose $(\#/cm^2) \times 10^{14}$
40	0.70
87	1.32
150	1.28
220	1.22

4.2.1.4 Implant Anneal

Once all the implantations are completed, the metal mask is removed from the sample by wet chemical etching using a piranha solution(1:1 - H_2O_2:H_2SO_4) at 70°C. The sacrificial oxide is then etched with HF prior to the implant anneal process. Photoresist (AZ1518) is then spin coated onto the sample and pyrolyzed at 650°C to form a carbon cap on the surface as seen in Figure 4.59. An implant anneal is then performed at 1700°C for 20 min in an argon ambient at a pressure of 400 mTorr.

Swelling in the implanted SiC regions

Once all the high energy implants are completed, the polysilicon and Ni masks are stripped off the sample. Swelling was observed on the bare SiC in regions that were subjected to the high energy implantation. Figure 4.60 shows surface roughness scans using the KLA Tencor P7 stylus profilometer over the implanted regions before and after the high energy P-well and n-source implantations are completed.

A step height of 9 nm is observed over the surface of the n-source regions as seen in Figure 4.60(a). The nitrogen n-source implant has the highest dose in the entire implant schedule of the trigate MOSFET and therefore the combination of high energy and high-dose ion bombardment during the implantation could cause

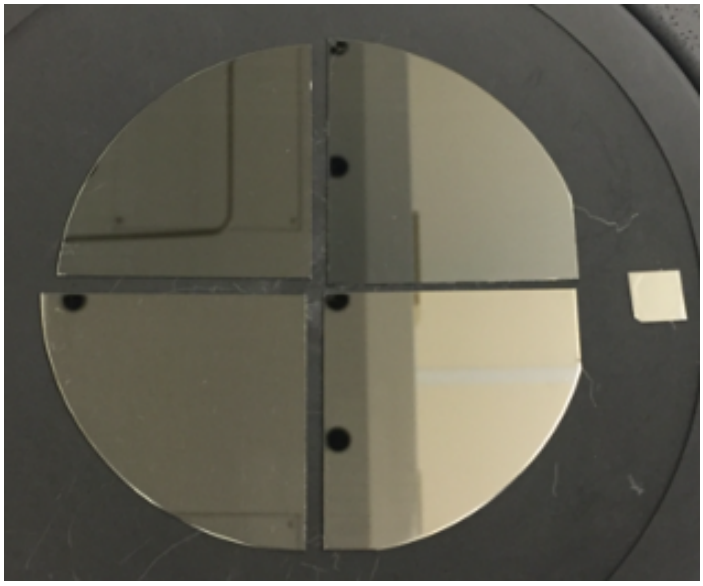


Figure 4.59.: Carbon cap formed on Gen-1 samples prior to implant anneal in the Epigress hotwall CVD reactor at 1700°C for 20 minutes in an argon ambient.

damage and swelling in the underlying exposed SiC regions. The damage can be recovered after the high temperature implant anneal as seen in Figure 4.60(b).

In the P-base regions, a recess from the surface is observed as seen in Figure 4.60(c). This is due to an etch of the SiC surface in these regions during the polysilicon implant mask etch in Figure 4.12. Over etching the polysilicon at this step could be due to insufficient screen oxide thickness or diminished selectivity to oxide under the polysilicon trench area due to insufficient polymer deposition during the Bosch process used to etch the polysilicon. This leads to unintended etch of the SiC surface unprotected by the polysilicon mask. To mitigate this, a thicker screen oxide is needed on the SiC surface before the polysilicon is deposited.

4.2.2 Trench Etch

The trench etch is another key, irreversible process step in the trigate process flow, and therefore calibration for etch depth and uniformity is done on multiple test

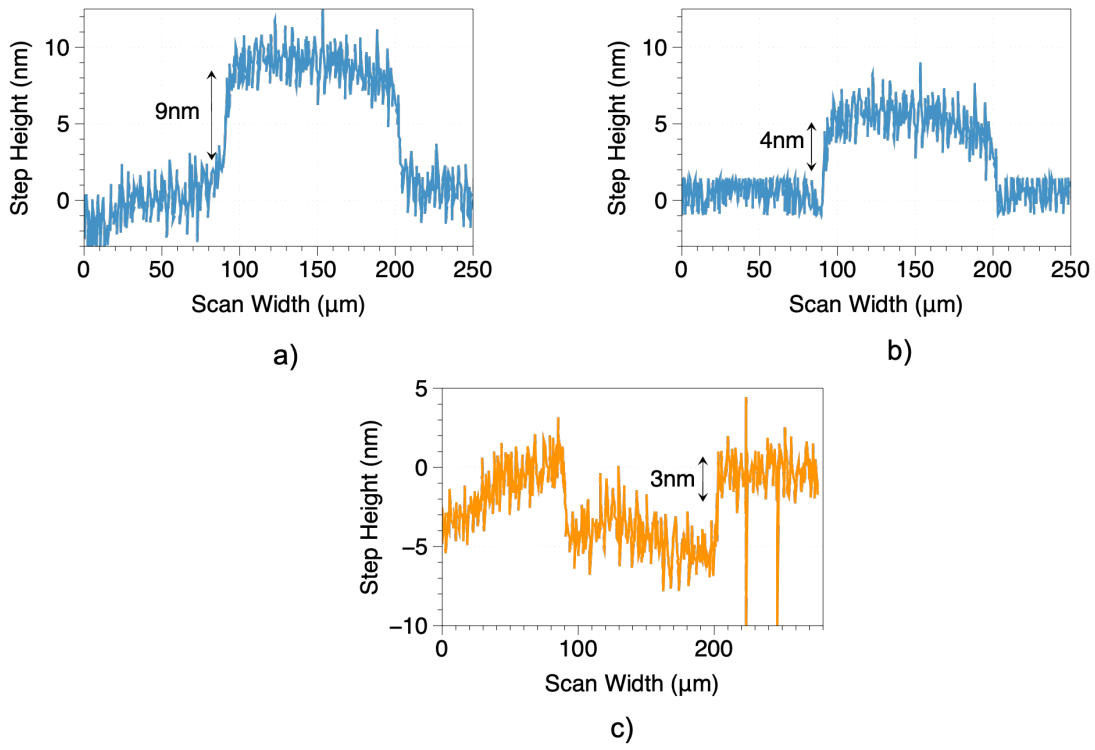


Figure 4.60.: Step height of implanted regions after high energy implants using a stylus profilometer a) Scan across the source implant before anneal, b) Scan across the source implant after anneal, c) Scan across the base implant before anneal

samples just prior to processing the trigate samples. Due to repairs and equipment maintenance, the Panasonic E620 ICP-RIE etcher, which was used to develop the baseline recipe, was unavailable during the timeline of this process for the Gen-1 samples. Therefore, the Oxford Plasmapro 100 ICP-RIE at Notre Dame University was used for the trench etch. Details of the process development using this etcher is discussed in my colleague Naeem Islam's thesis [101].

Nickel is used as a hard mask for the trench etch, and is patterned by a dual step of e-beam lithography in the active area and optical lithography in the field area as described in Section 4.1.2. The four trigate Gen-1 samples are etched in two batches. First, samples 1Q3 and 4Q2 were etched using the parameters listed in Table 4.8 for 4 minutes and 25 seconds, resulting in a trench depth of 1.5 µm in the active areas.

The etch time was chosen such that the test structures in the PCM areas are not over etched and made unusable. The second batch of samples (2Q4 and 3Q2) were etched to a trench depth of 1.9 µm in the active area, which is closer to the Gen-1 target of 2 µm.

Table 4.8.: SiC etch recipe in Oxford Plasmapro 100 ICP-RIE

Parameter	Set Point
Gas Flow (SF_6)	10 sccm
ICP power	2800 W
Bias power	200 W
Pressure	5 mTorr
V_{DC}	255 V
Temperature	10°C

4.2.3 Gate stack and Metal Contacts

After the trench etch, the fabrication of the Gen-1 samples are split into 3 runs as illustrated in Figure 4.51. First, sample 2Q4 is processed and taken through the gate stack and ohmic contact process. Each of these unit processes are described in Section 4.1, and parameters for every step is listed in the run sheet in Appendix A. Once the fabrication is complete, the trigate MOSFETs are measured, and any error or learning from each of the samples is applied to the following samples.

Optical images of the sample at the end of the patterned poly gate, ILD oxidation, ohmic contact anneal, and top metal processes for sample 4Q2 is shown in Figure 4.61. Electrical measurements on the completed device were done using the Keithley 4200 parameter analyzer. First, the devices were tested for functionality by grounding the source terminal and applying 100 mV on the drain. The gate voltage is then swept from -10 V to 10 V while measuring the drain current.

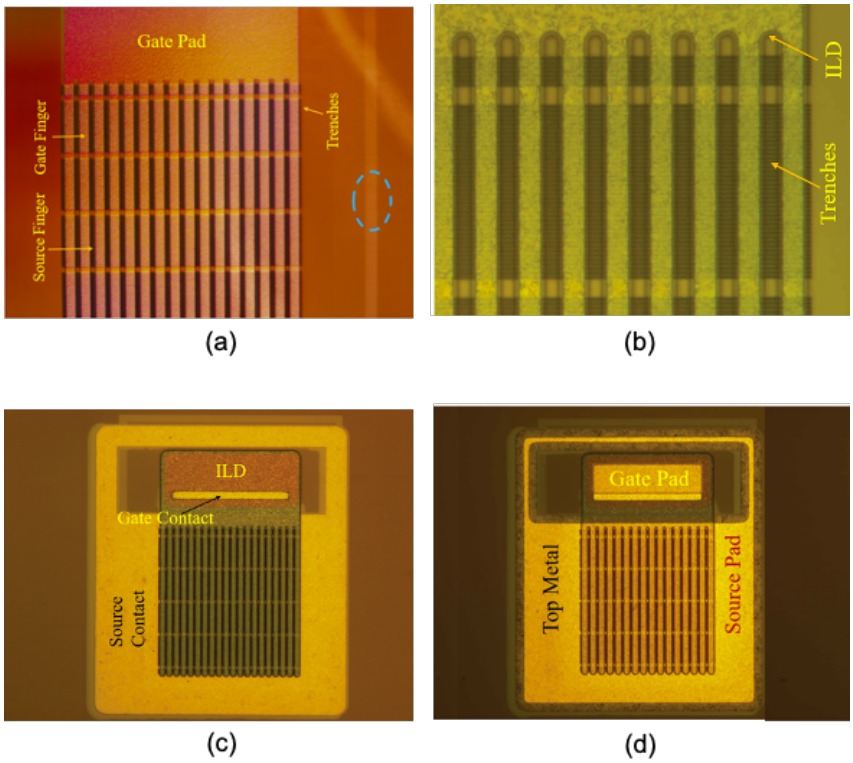
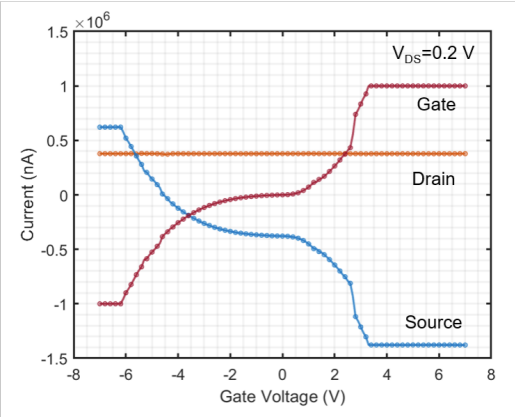


Figure 4.61.: Optical images of the Gen-1 trigate sample after a) Polysilicon gate doping and etch b) ILD pyrogenic oxidation at 1100°C for 4 hours and 20 minutes. c) Ohmic anneal at 1000°C for 3 minutes in argon d) Top metal deposition (Ti/Au)

High gate leakage current in trigate MOSFET Sample 4Q2

High gate leakage current was measured on the trigate MOSFETs on sample 4Q2 as seen in Figure 4.62. The drain current is constant irrespective of the magnitude of the gate-source voltage and this suggests the presence of a leakage path from source to drain. The source current is likely then the sum of the gate leakage current and the constant drain current. As the high gate leakage current prohibits gate control of the MOSFET, the functionality of both the trigate and planar MOSFETs could not be measured in this sample. A failure analysis determined the likely cause to be a drift in the process pressure that gives rise to large grains in the thin polysilicon film used to form a conformal gate oxide, leading to a highly rough gate oxide. The

polysilicon deposition as part of the poly-ox process was optimized and a solution was identified to reduce the deposition temperature of the polysilicon from 630°C to 580°C. A detailed description of the process optimization and electrical characterization is discussed in my collegue Naeem Islam's thesis [101]. This revised process produces amorphous, rather than poly-crystalline silicon, and the corresponding oxide grown from this material is much smoother. Short loop experiments confirmed that it is suitable for use as a gate oxide.



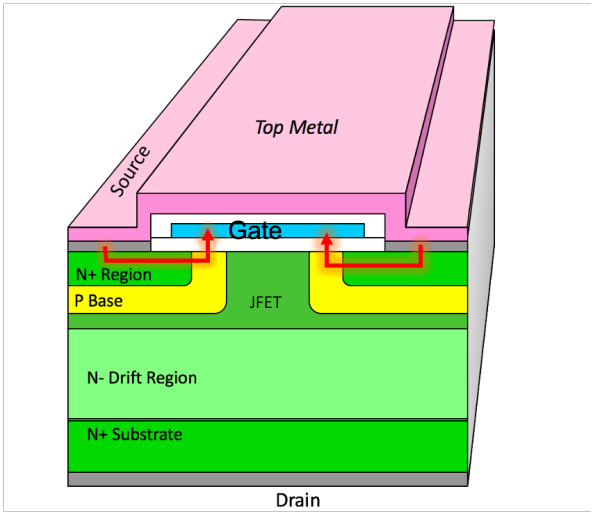


Figure 4.62.: Measured current at the source, drain and gate terminals plotted as a function of gate voltage. High gate leakage current is observed that indicates failed MOSFET devices.

This process modification was then incorporated on sample 2Q4, while other unit processes such as polysilicon gate, ILD formation, ohmic contacts and top metal remain unchanged.

Source-Drain electrical shorts in trigate MOSFET sample 2Q4

While the gate leakage problem observed in sample 4Q2 was solved as described above and a new gate oxide process applied to sample 2Q4, it subsequently exhibited

source-to-drain shorts, even with a large negative voltage on the gate. A plot of the source and drain terminal currents as a function of gate voltage with the source grounded and 20 mV applied on the drain terminal is shown in Figure 4.63. As seen in the figure, drain current hits compliance (10 µA) for all values of gate voltage, and the source current is equal in magnitude but opposite in sign as compared to the drain current. This indicates that there exists a current path from source to drain that is not subject to gate control. The gate leakage is very small, indicating an alternative parasitic current path from source to drain, rather than the previously described gate short. Through exhaustive failure analysis, two possible causes for the source-drain short have been identified and are discussed below:

1. Excessive penetration of nickel-silicide through P+ / CSL junction
2. Missing polysilicon posts in implant mask during the n-source implantation

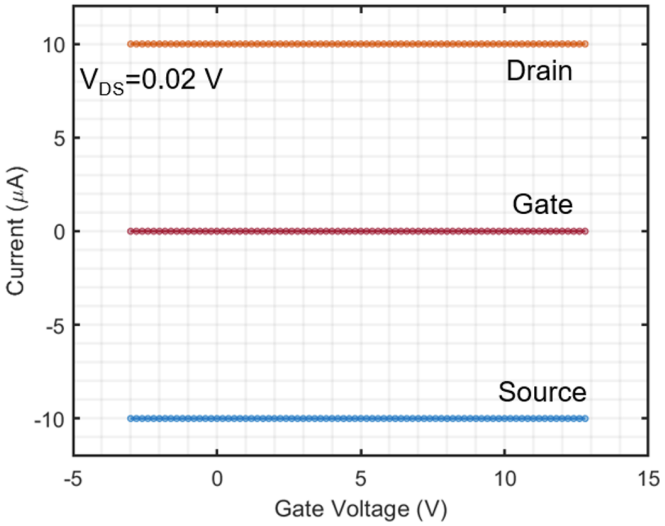


Figure 4.63.: Source and drain current as a function of gate voltage for a trigate MOSFET on sample 2Q4.

Figure 4.64 shows an SEM of a FIB cross section taken in the Apreo FEI of the trigate structure in sample 2Q4. This image was taken from a planar (non-trenched)

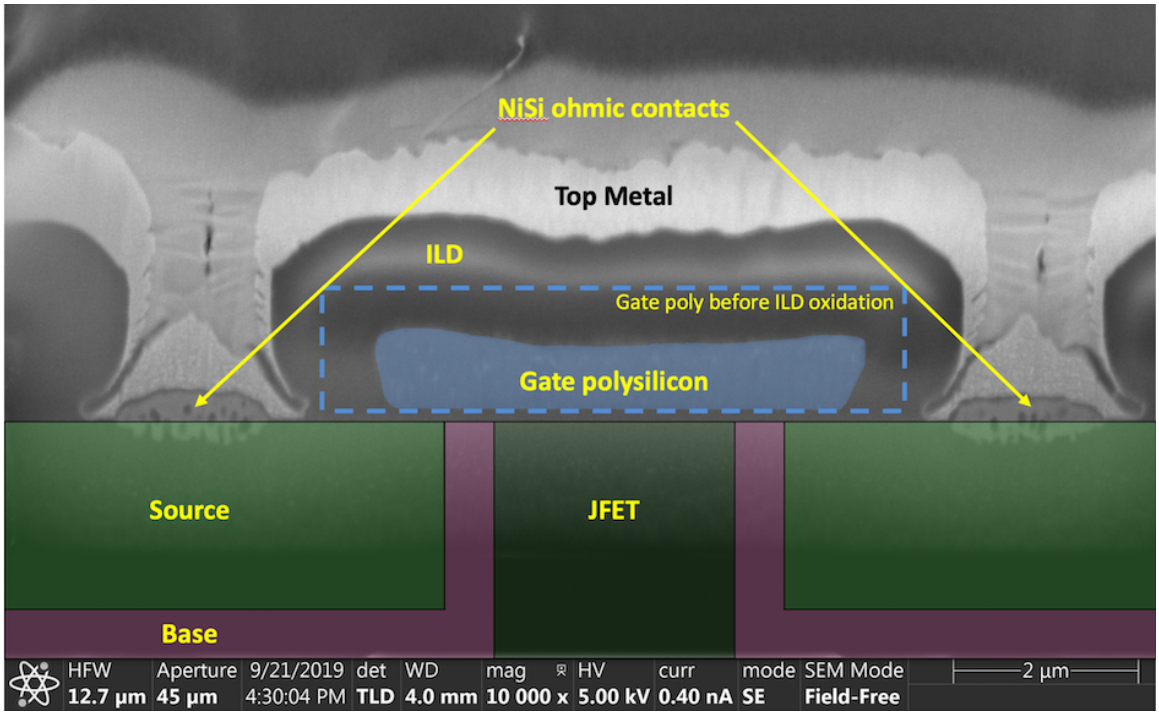


Figure 4.64.: SEM of a FIB cross-section of a planar Gen-1 MOSFET. False color schematically illustrates the location of the source and base implants and the gate

version of the trigate devices, but is identical to what would be found down the center-line of a trigate fin. The false colors illustrate the approximate location of the source (green) and base (pink) implanted regions. The gate polysilicon is highlighted in blue, with the dotted blue line showing the approximate size of the gate poly before oxidation to form the interlayer dielectric which surrounds the gate. The nickel silicide ohmic contact regions are clearly visible to the left and right of the ILD.

Figure 4.65 shows the same SEM image shown in Figure 4.64, recolored to match the cross-section through the center of the P+ base contact implant stripe. The P+ implant profile through the cross-section indicated by the yellow dashed line in Figure 4.65 is plotted in Figure 4.66. The red curve is the P+ implant profile, while the green horizontal line represents the background CSL doping. The intersection of these two lines is the PN junction, which occurs at a depth of ~ 0.5 µm below the original surface. The gray box indicates the penetration depth of the nickel silicide

region formed during the ohmic contact anneal, after taking into account the material removed during previous processing steps.

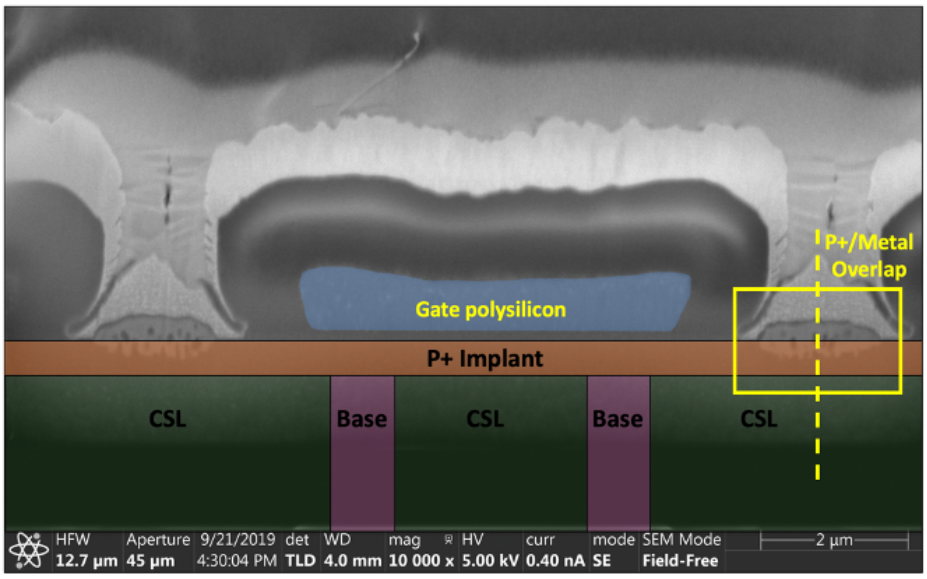


Figure 4.65.: SEM image from Figure 4.64, recolored to match cross-section through the center of the P+ base contact implant stripe

The SiC consumed during the silicidation process is proportional to the thickness of Ni deposited, and therefore a source-drain short caused by excessive penetration of NiSi during the ohnmic contact process could be mitigated by using a thinner Ni film. To ensure this change does not negatively impact the contact resistance, TLM test structures were fabricated on N+ implanted wells on a P-type substrate using 100 nm and 50 nm Ni films. The results, shown in Figure 4.67, indicate that the specific contact resistance of the 100 nm nickel silicide process is equivalent to the previously used 200 nm process.

The 50 nm nickel-silicide process has a specific contact resistivity of 6×10^{-6} Ωcm^2. Though reducing the deposited nickel thickness increases the contact resistivity by a factor of 6, it is still sufficiently low to make the source contact resistance a negligible contribution to the total trigate specific on-resistance. For instance, using the 50 nm nickel silicide process on our most aggressive source contact length of 1 µm would

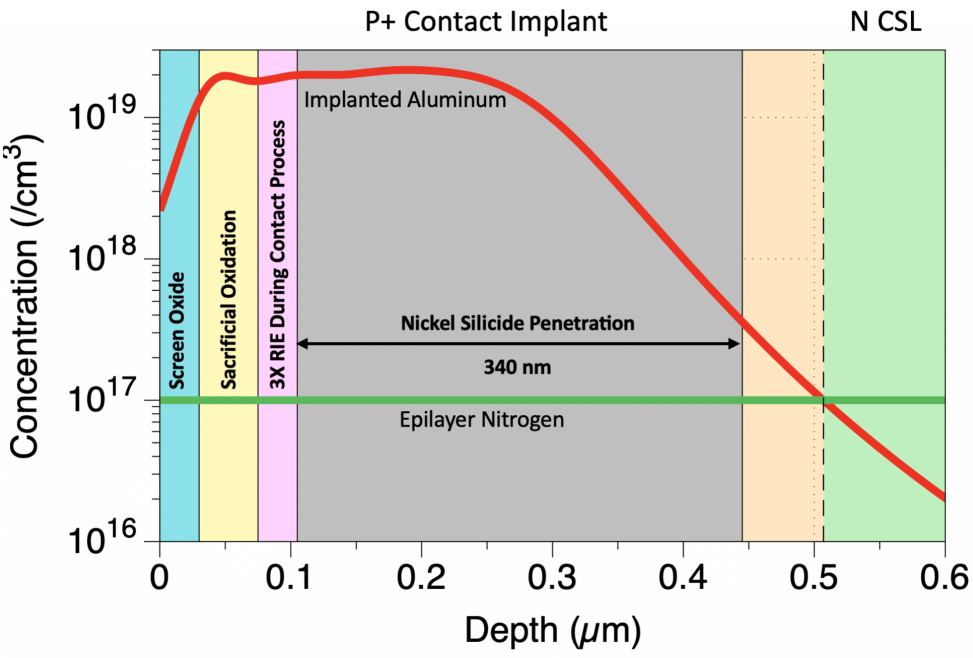


Figure 4.66.: P+ contact implant profile (red), and the background CSL doping (green). The PN junction occurs at the intersection,∼ 0.5 µm below the original surface. The gray box indicates the measured penetration depth of the NiSi ohmic contact region.

result is the specific contact resistance of $2 \times 10^{-5}\ \Omega\,\mathrm{cm}^2$ which translates to about 1% of the total resistance of the trigate in the on-state.

A second possible failure mechanism that would cause source-drain shorts has been identified using secondary electron potential contrast microscopy [119]. The proper combination of low accelerating voltage and secondary electron detector is used to image doped regions, as illustrated in Figure 4.68. P-type areas appear as bright, nearly white regions, while N-type areas appear as darker gray. The darkest horizontal lines in the image are the trenches. Two missing features are observed in the image (circled in red) that are related to the small polysilicon posts described above, which block both the P-type base implant and the N+ source implant inside the source contact stripes.

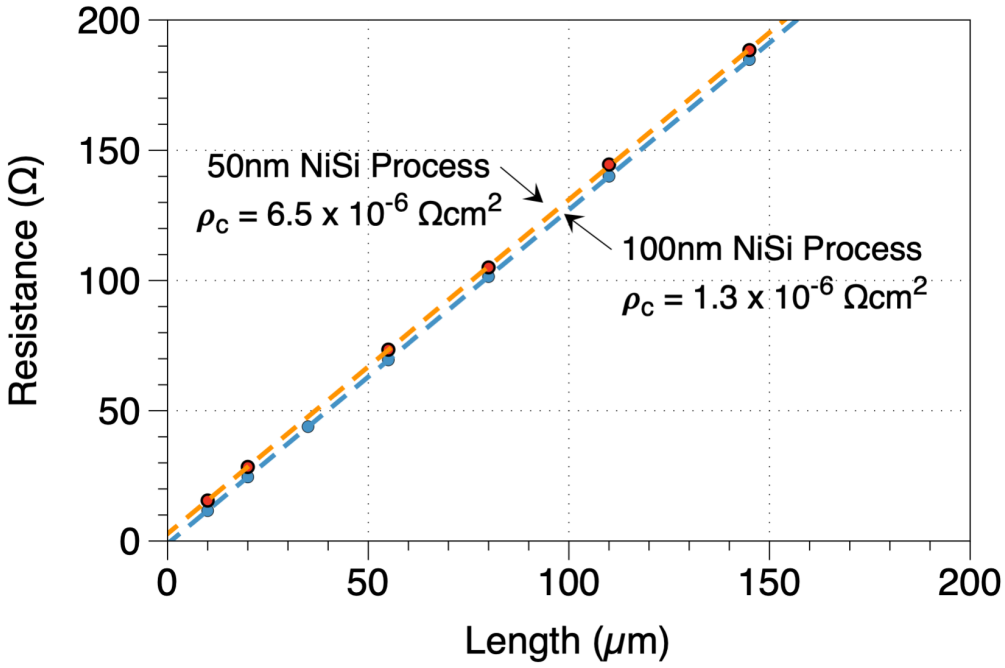


Figure 4.67.: TLM contact resistance measurements using the 50 nm and 100 nm nickel silicide processes.

As the polysilicon posts have a high aspect ratio and are not supported by an interconnected network, there is apparently a significant probability that these features will break off from the surface between the base and source implants, possibly due to stress created when these poly features are oxidized to create the self-aligned source implant mask as seen in Figure 4.68(a). At the location of this failure, the source implant is directly in contact with the CSL epilayer, since the polysilicon post was present during the base implant, thus preventing the p-type base implant, but absent during the N+ implant. As described above, the P+ base contact implant is incapable of overwhelming an N+ implant, leaving these regions strongly N-type. This creates a direct short between source and drain whenever these features break off between the base and source implants.

To eliminate this problem, a change in the design of the high energy implant mask is required and is discussed in Section 6.1.1. This can only be applied to the next

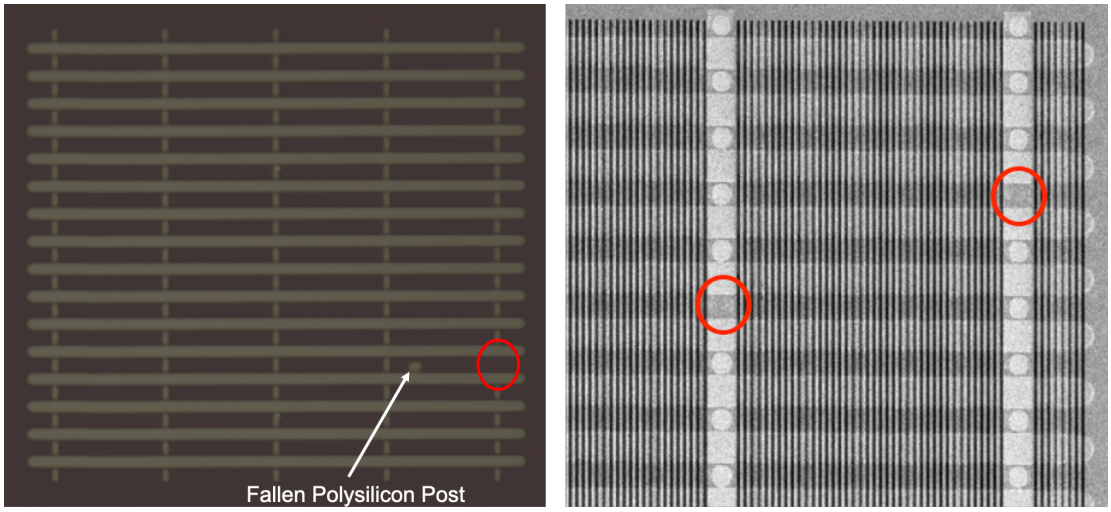


Figure 4.68.: Source-drain shorts caused by missing polysilicon posts after the P-type base implant and before the N+ source implant. a) Optical micrograph image showing fallen polysilicon post after the thermal oxidation process for the source implant, b) Secondary electron potential contrast SEM image of the active area of a trigate device after all implantation is complete. Light regions are P-type, gray regions are N-type, while trenches appear nearly black.

set of samples as all the high energy implants on the Gen-1 and Gen-2 samples have already been completed with the current implant mask design. Therefore a low device yield is expected in the remaining trigate samples.

Low Field-Effect Mobility on Sample 2Q4

Though the trigate devices are not functional, each die in the trigate layout contains several lateral MOSFET PCM's that allow accurate measurement of channel resistance without interference from other series resistance components such as the JFET, drift, and substrate resistances that are present in vertical devices. These devices are also used to obtain the electron field-effect mobility. Output and transfer

characteristics, as well as the derived field-effect mobility as a function of gate voltage of such a device (LM102Q4) is shown in Figure 4.69. The peak field-effect mobility is less than 1 cm^2/Vs and is exceptionally low as compared to reported field-effect mobility values in literature with the same doping concentration [30]. To investigate this further, measurements were made on other PCM devices present on the same die, such as MOS capacitors and gate-controlled diodes.

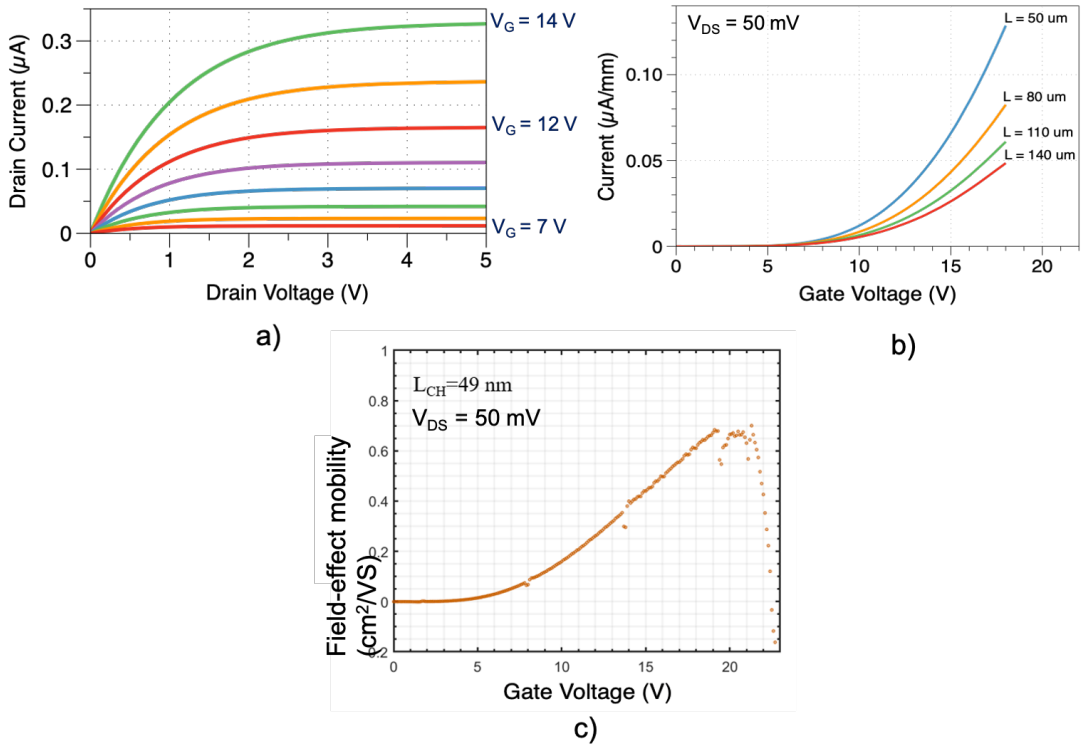


Figure 4.69.: Electrical measurements on lateral planar MOSFETs on sample 2Q4. (a) Drain current vs. drain voltage charectaristics, (b) Drain current vs. gate voltage characteristics, (c) Field-effect mobiltiy vs. gate voltage.

High frequency (100 kHz) C-V characteristics of a P-type MOS capacitor fabricated on a base implanted region is shown in Figure 4.70(a). As seen in the figure, there is a large negative shift in the flat band voltage, as well significant stretch-out in the capacitance as the voltage is swept from flatband to deep depletion. This is characteristic of a large number of holes trapped in empty interface states above

the Fermi level in SiC P-type MOS structures. However, the measurement of interface trap density using either high-low or C-ψ techniques was not possible as there was significant gate leakage current at voltages beyond -25 V that inhibited accurate capacitance measurements. Therefore, one of the planar long channel MOSFETs (LM102Q4) with a channel length of 50 µm whose output characteristics are plotted in Figure 4.69 was connected in a gate controlled diode configuration and used to determine the interface trap density.

For the gate controlled diode measurement, the source and drain terminals are shorted together and connected to the grounded P-base terminal. The measured gate capacitance as a function of the swept gate voltage is shown in Figure 4.70(b). Similar to the MOS capacitors on P-base, the accumulation capacitance could not be reached due to excessive gate leakage current. However, as the voltage is swept positive towards point X, the base region below the gate electrode goes into deep depletion while the interface traps at the surface are in non-equilibrium with the applied voltage. At a sufficient positive voltage, the interface traps at the edge of the channel near the source can come to equilibrium by capture of electrons across the PN junction. At point X, the channel area near the source region inverts, allowing electrons to flow beneath the gate electrode, some of which are captured by interface traps, and increasing the capacitance to that of point Y. At this point, the surface band bending $\psi_S = 2\psi_b$, and as the gate voltage is increased further the minority carrier concentration under the gate increases, and capacitance increases toward inversion at point Z. A significant stretch-out in capacitance is observed as the gate voltage is increased from point Y to Z. This is attributed to the filling of interface traps energetically located above $2\psi_b$ whose total number is given by $C_{ox}(V_Z - V_Y)/(qA)$ and is equal to 9.6 $\times 10^{12}$ cm^{-2}.

High gate leakage current and C-V measurements indicate an unusually high density of interface states on implanted P-wells as compared to the epitaxial grown N-type CSL regions. One possible reason for this could be surface contamination during the implant process. Only the P-wells were exposed during the implant process, while

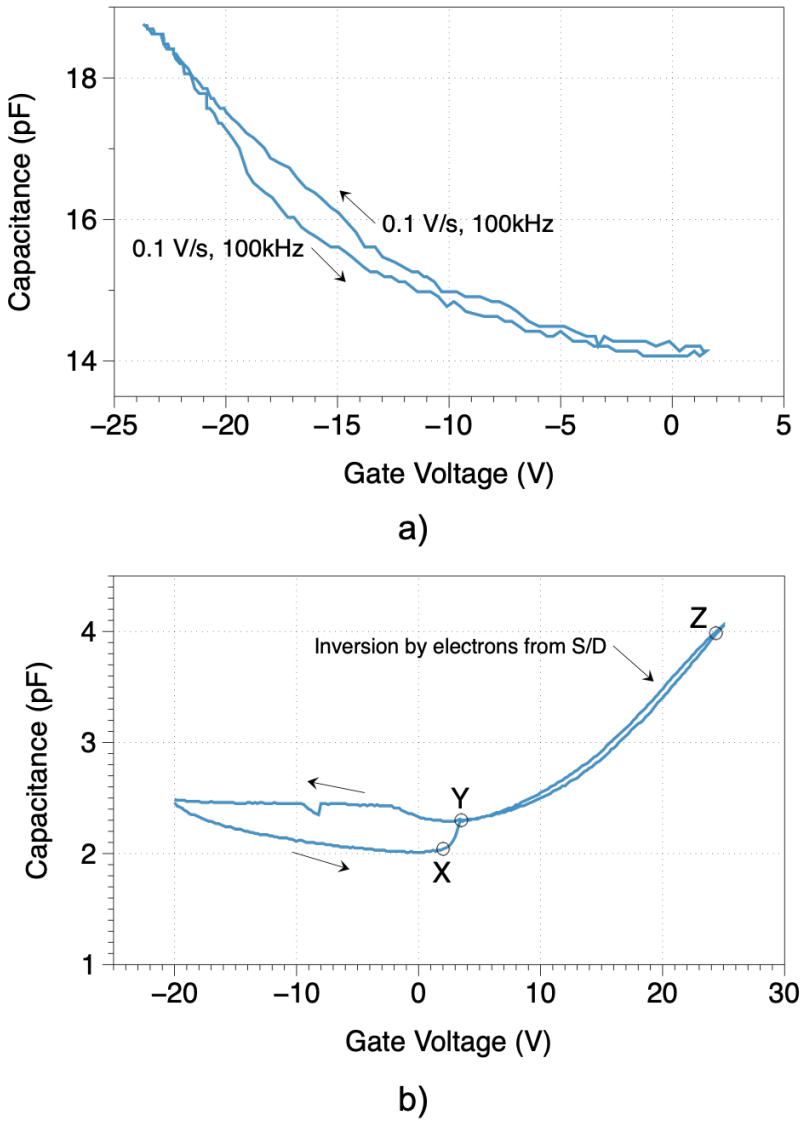


Figure 4.70.: C-V characteristics on sample 2Q4. (a) MOS capacitors on P-base, (b) Diode controlled MOSFET measurements on a lateral planar MOSFET at 1 kHz.

the N-type epilayers were protected by the 5 µm polysilicon implant mask. Metallic contamination from the stainless steel of the implant chamber could have become embedded in the upper surface of the sample during implantation. On the trigate samples, we implant through a screen oxide to prevent these contaminants from reaching the semiconductor. However, the screen oxide could have been thinned (or removed)

during the polysilicon etch process just prior to the implantation. The high energy implants (4.3 MeV) may have driven these contaminants through this thinned screen oxide. This hypothesis can be verified in the next run by comparing the planar MOSFET characteristics of the H_2 etched (1Q3) and unetched (3Q2) samples. The hydrogen etch is primarily done to smooth the sidewalls of the RIE etch trenches in SiC. On a planar surface that has not been RIE etched, the only effect of the H_2 etch is the removal of the top $25 - 30$ nm of SiC material.

Optimization of poly-ox gate oxide to improve field-effect mobility

All previous process development on the poly-ox gate oxidation process was done on lightly doped N-type substrates. Therefore, an experiment was conducted to verify the field-effect mobility on a P-type substrate. To obtain baseline performance parameters, such as field-effect mobility and oxide breakdown field, long channel lateral MOSFETs were fabricated on a lightly doped (1×10^{16} cm^{-3}) epitaxially grown layer on a heavily doped P-type substrate with implanted source and drain regions. Three samples were first RCA cleaned, and a 30 nm sacrificial oxide was grown on all the samples by wet oxidation in tube 4. The oxide was then stripped, and 21 nm of polysilicon was deposited using LPCVD at 580°C and 150 mTorr. The gate oxide was then formed in tube 1 using three alternative processes 1) wet thermal oxidation, 2) poly-ox wet thermal oxidation and, 3) poly-ox dry thermal oxidation. The pyrogenic process for the wet oxidation used for the standard thermal and the poly-ox processes is shown in Figure 4.71. Dry oxidation was carried out at 1100°C in an oxygen ambient for 28 minutes. A total of 46 nm of oxide was formed on all three samples. The samples then received an NO anneal at 1175°C for 2 hours. Ohmic contacts were formed at the source and drain terminals by a nickel-silicide process, and nickel was used as both a top and gate metal.

The drain current of the long channel MOSFETs was measured as a function of gate voltage with channel lengths of 50, 80, 100, and 140 µm. The source and drain

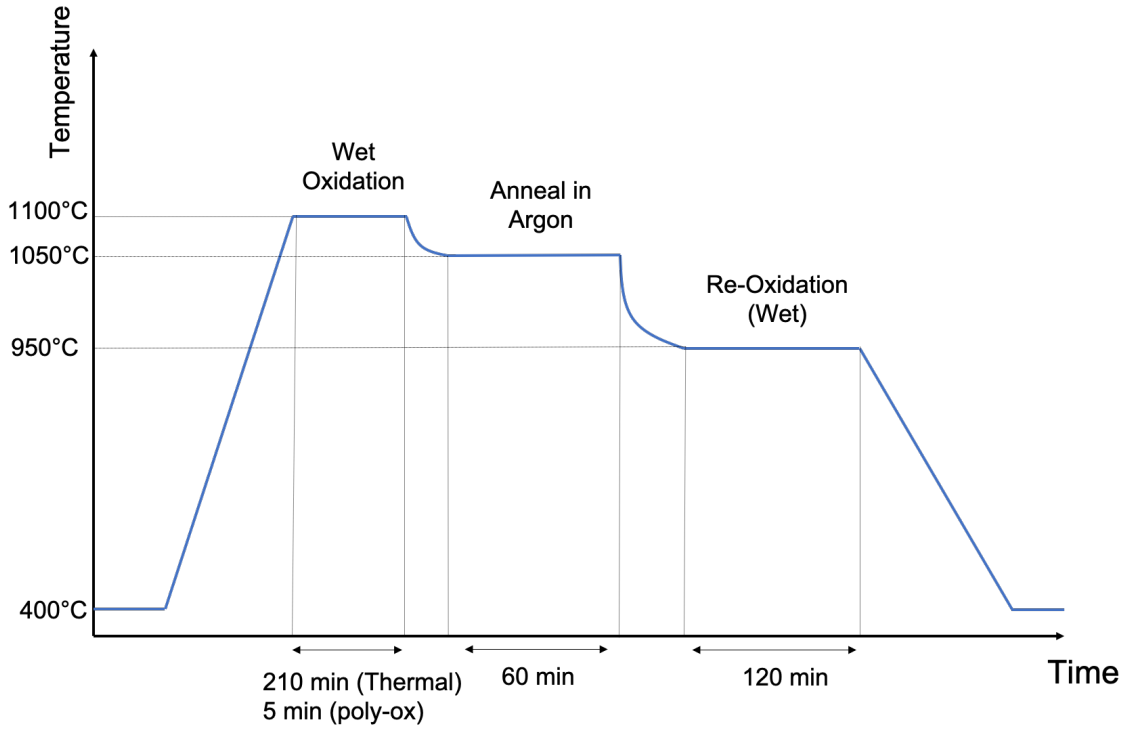


Figure 4.71.: Process flow for pyrogenic wet oxidation carried out for both thermal and poly-ox gate oxide processes.

contact resistivity was measured using the TLM structures to be $2 \times 10^{-6}\ \Omega\,\mathrm{cm}^{-2}$, sufficiently low that the voltage drop across the contacts can be neglected. The extracted field-effect mobility as a function of gate voltage is shown in Figure 4.72(a). As seen in the figure, the mobility of the poly-ox wet oxidation process is comparable to conventional thermal wet oxidation, while the poly-ox dry oxidation process has a lower peak mobility and more gradual slope. The thermal and poly-ox wet oxidation results are also comparable to other reports of field-effect mobility on Si-face NO annealed thermal oxide [120]. A number of factors including the post-oxidation anneal in argon at 1050°C and the re-oxidation at 950°C could be contributing to the superior performance of the wet oxidation process. Further, the gate leakage and oxide breakdown field was measured on N-type MOS capacitors processed in parallel with the MOSFETs as shown in Figure 4.72(b). The MOS capacitors were biased

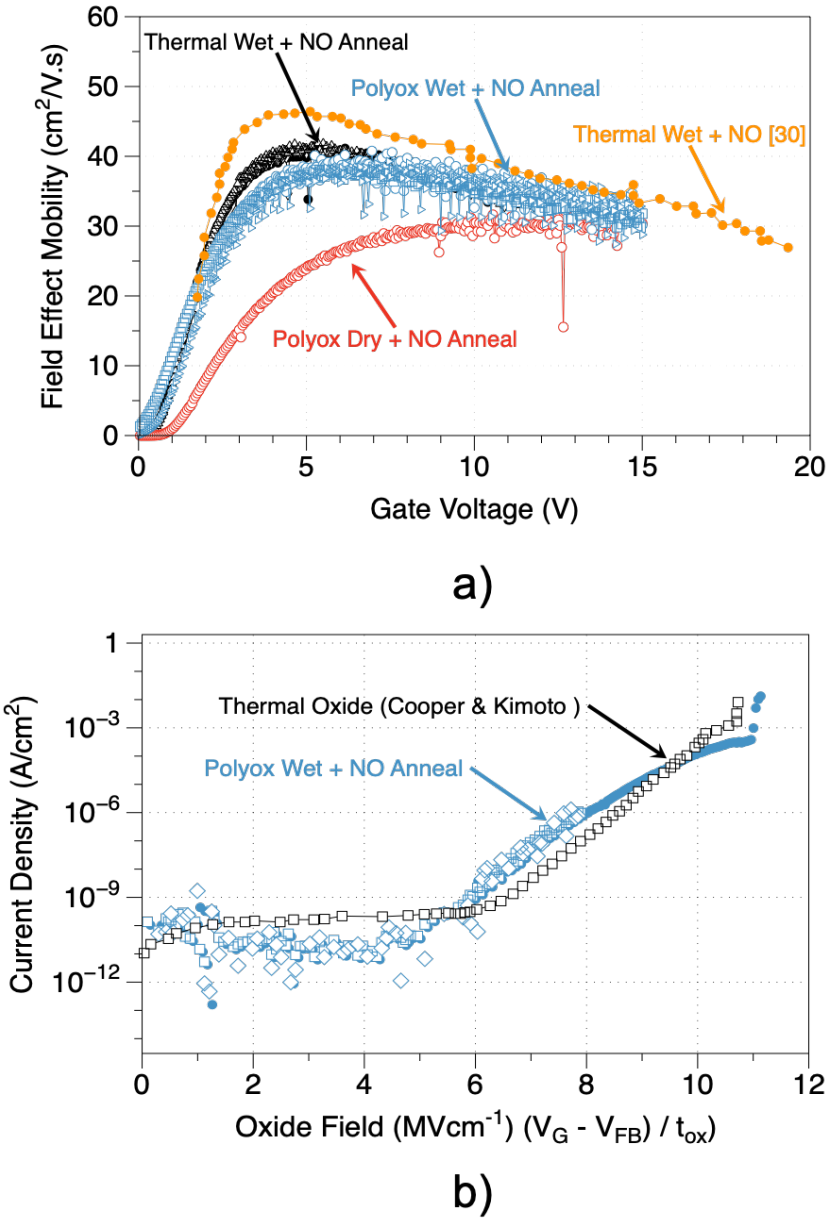


Figure 4.72.: Electrical measurements from polyox optimization experiment. (a) Field-effect mobility of long channel lateral MOSFETs as a function of gate voltage, and (b) Leakage current and breakdown as a function of oxide field for the poly-ox wet oxidation process compared with thermal oxide reported in literature [30]

in accumulation by sweeping the gate voltage from flatband to +50 V while measuring the gate current. As seen in the figure, the breakdown field of the poly-ox wet oxidation process is comparable to thermally grown oxide.

The optimized wet oxidation process yields higher field-effect mobility, lower gate leakage and higher oxide breakdown field as compared to the poly-ox dry oxidation process. Therefore, this process is used to form the gate oxide in the next set of samples both for samples 1Q3 and 3Q2. A split experiment was conducted between the remaining two samples of Gen-1 (1Q3 and 3Q2). Sample 3Q2 had a hydrogen etch before the gate stack was deposited, while only the optimized poly-ox process was applied to sample 1Q3. The 50 nm nickel silicide process was carried out on both samples while all other processes were unchanged. Results from sample 1Q3 are discussed in the next chapter. Sample 3Q2 is processed until the ohmic contact step, and awaits the 50 nm nickel silicide process. The fabrication summary and status of the Gen-1 trigate samples is summarized in Figure 4.73 below.

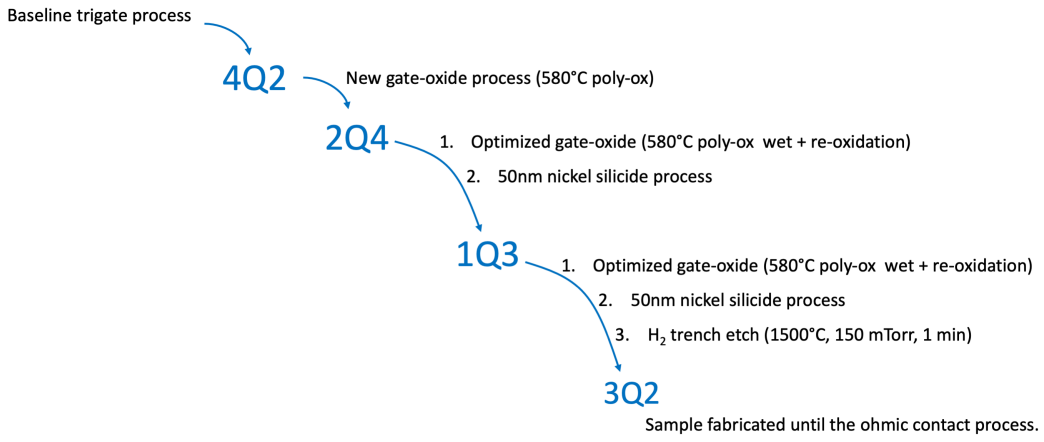


Figure 4.73.: Fabrication sequence and major process changes applied to Gen-1 trigate samples.

4.2.4 Trigate Gen-2 Fabrication

The Gen-2 trigate MOSFETs are designed for a trench depth of 1 µm, and are comprised of four samples, two designed for 900 V and two for 650 V applications as listed in Table 4.5. Identical to the Gen-1 samples, the CSL is thinned such that it extends only until the bottom of the base region. This is carried out on all four samples, and therefore all the Gen-2 samples have a CSL thickness of 1.6 µm. The samples are RCA cleaned and a 45 nm thick sacrificial oxide is thermally grown on all the samples. The sacrificial oxide prior to the base implant is thicker than that used in Gen-1 to prevent over-etching during the polysilicon patterning step as discussed in Section 4.2.1.4. The shallower base and source junctions of the Gen-2 devices will require less than half the maximum implant energy and therefore that results in lower implant cost and less lattice damage.

4.2.4.1 Base implant

The lithography for the base implant is done in a single step using e-beam lithography. First, a 4.5 µm thick layer of polysilicon is deposited by LPCVD at 630°C and 150 mTorr. This is followed by an e-beam lithography step to pattern the polysilicon using AR-P 6200 CSAR resist as discussed in Section 4.1.1.2. The details of the resist application and e-beam lithography is provided in the run sheet in Appendix B. Polysilicon is then etched in the STS ASE system using the recipe listed in Table 4.3. SEM images of the patterned polysilicon for the P-base implant are shown in Figure 4.74.

The samples are mounted onto a Si carrier wafer, and the high energy implantation is done at mi-2 GmbH, Germany. The complete implant schedule for the base implant is listed in Table 4.1, and the target implant profile is shown in Figure 4.75.

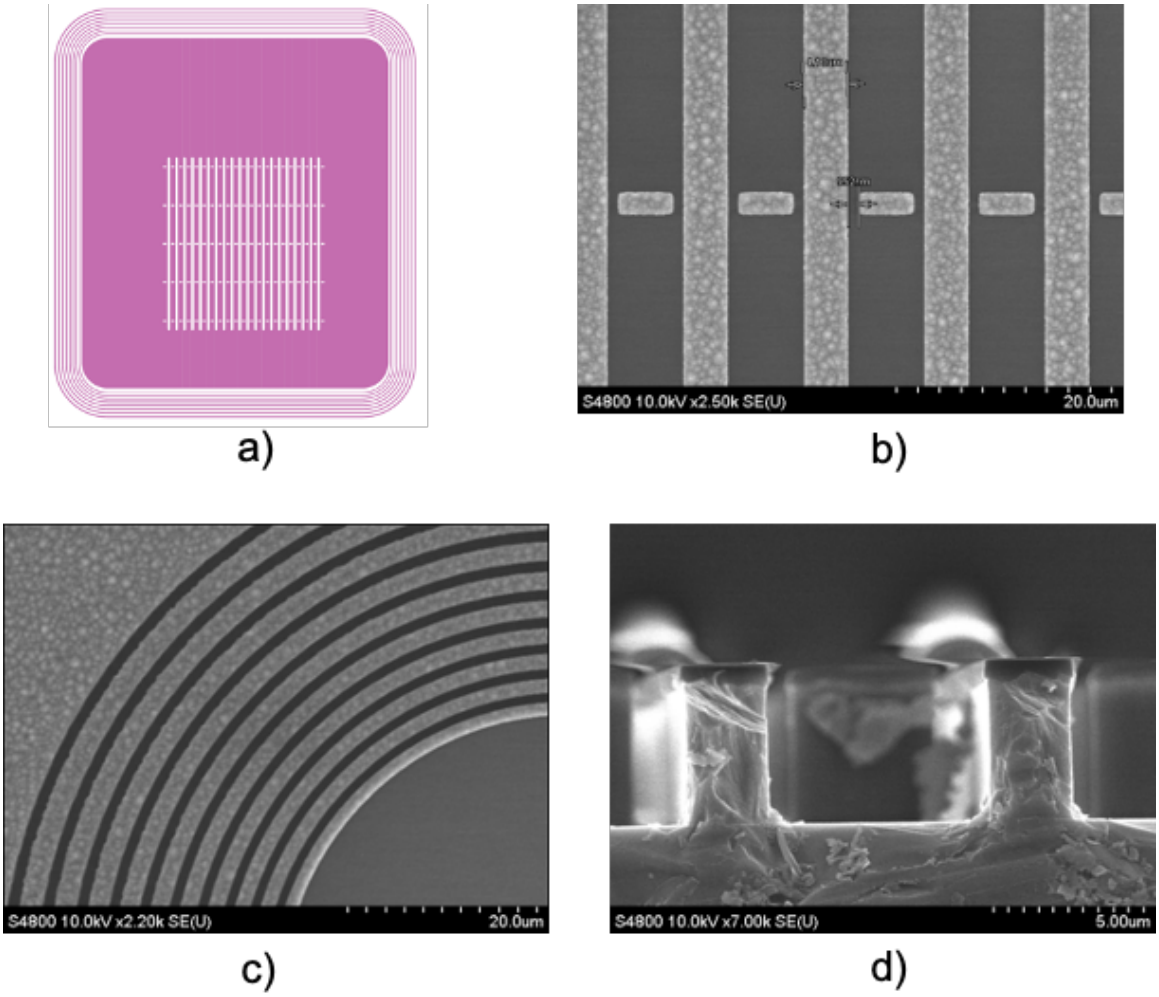


Figure 4.74.: SEM images of the polysilicon mask for the base implant in Gen-2 samples. (a) Mask layout of the JFET fingers; purple regions are to be implanted, (b) Active area with polysilicon runners and posts, (c) Floating field ring areas, (d) cross-sectional SEM of a test device processed with the trigate devices, showing a good vertical, highly anisotropic polysilicon etch.

4.2.4.2 Source implant

The exact process carried out for the source implant mask in the trigate Gen-1 samples was applied to the Gen-2 samples. The patterned 4.5 µm thick polysilicon layer which defines the P-well regions in the preceding step serves as the implantation

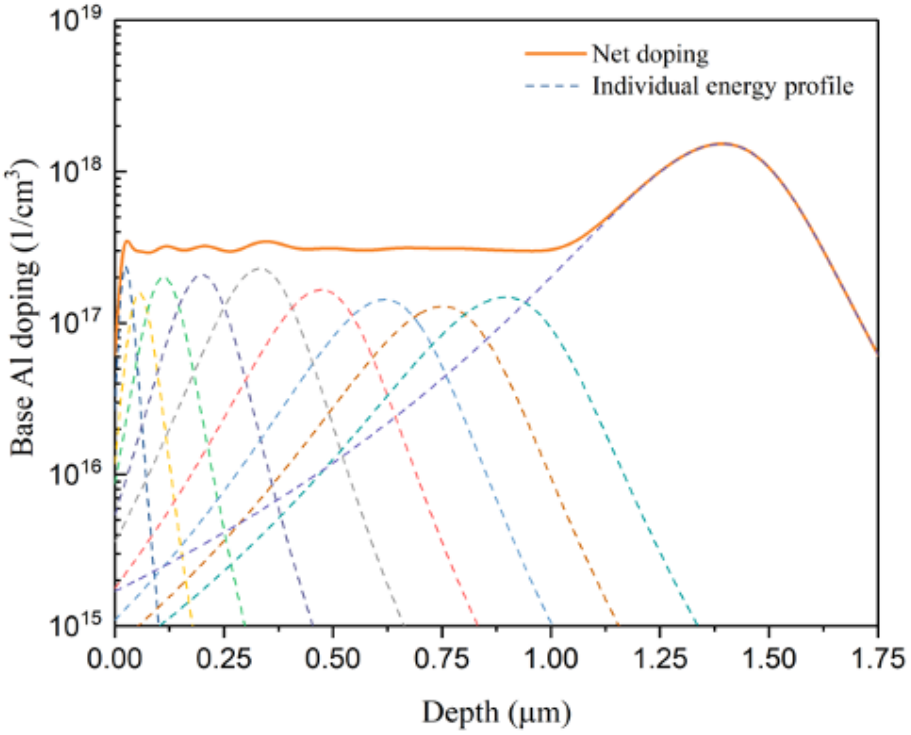


Figure 4.75.: Target implant schedule for Gen-2 trigate samples modelled using an analytical implant model [98].

mask for the nitrogen source implant as well. In the active region, the polysilicon pillars are oxidized to expand the pattern laterally by 0.5 µm in a pyrogenic oxidation furnace at 1100°C at atmospheric pressure. This oxidized polysilicon acts as a self-aligned source implantation mask in the active area, giving an accurate control on channel length without any mask alignment error.

In the process control modules, long channel MOSFETs, transmission line contact resistance test structures, and other features are defined by ∼2 µm of electroplated nickel. After the polysilicon oxidation, a seed layer of 0.5 µm thick gold is sputtered to cover the topology. This is followed by patterning AZ9260 optical photoresist, which acts as a mold. The sample is then immersed in a custom made Ni electroplating bath comprised of nickel sulphamate, nickel carbonate, boric acid, and nickel chloride. The deposition is done at a constant pH of 4.4-4.6, with a current of 10 mA using

a 99% pure Ni anode. The deposition rate at the specified condition is found to be around 700 nm/hr. According to a TRIM simulation, a 1 µm thick Ni mask is required to block the highest nitrogen implant energy. The deposited metal thickness is measured to be 2-3 µm. After the Ni deposition, the AZ9260 resist is stripped in a hot PG remover bath, and the Au seed layer is chemically etched in the openings. SEM images of the source implantation mask process are shown in Figure 4.76.

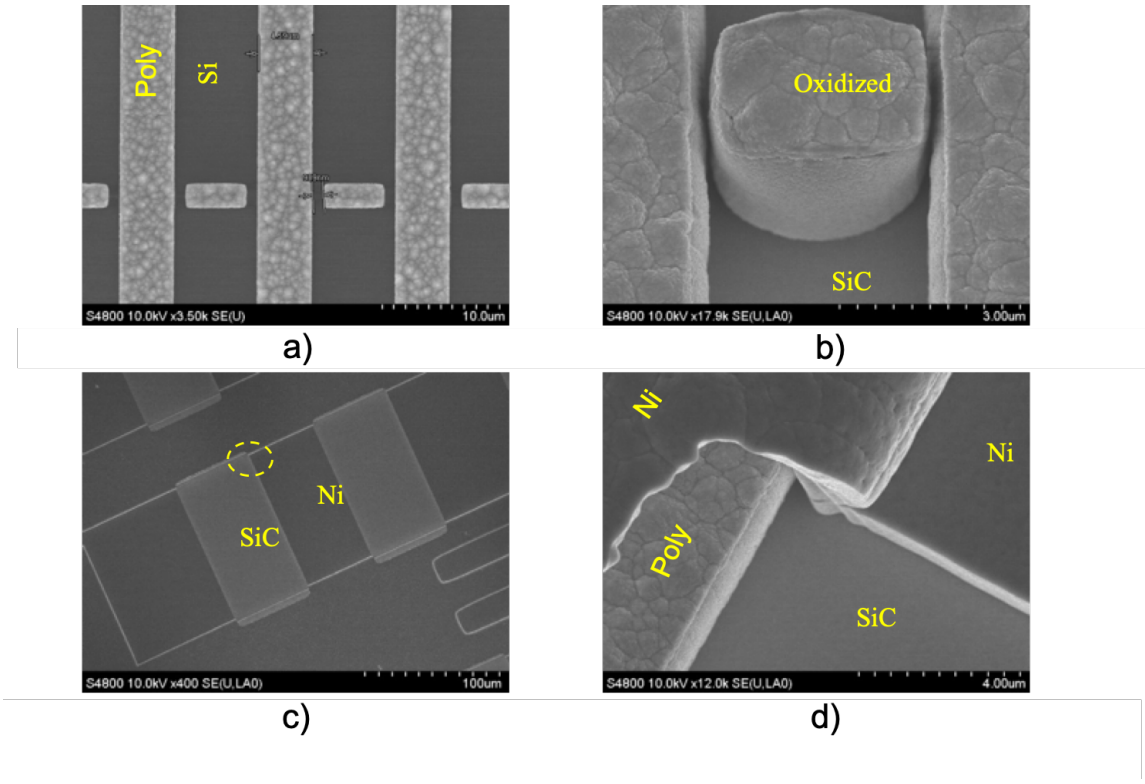


Figure 4.76.: SEM images of the N+ implant mask process. (a) Poly mask before oxidation, (b) Poly oxidized by 0.5µm, closing the 1µm gap (c) Ni electroplating pattern in a long channel MOSFET, (d) Closer view as indicated in (c), illustrating step coverage of the electroplated Ni over the polysilicon topology.

The Gen-2 trigate source implantation is designed to have a 1.25 µm junction depth, with high doping near the surface to produce low resistance ohmic contacts, as shown in Figure 4.77. The highest implantation energy of the profile is 1.3 MeV. The complete implantation schedule for the n-source implant is listed in Table 4.2.

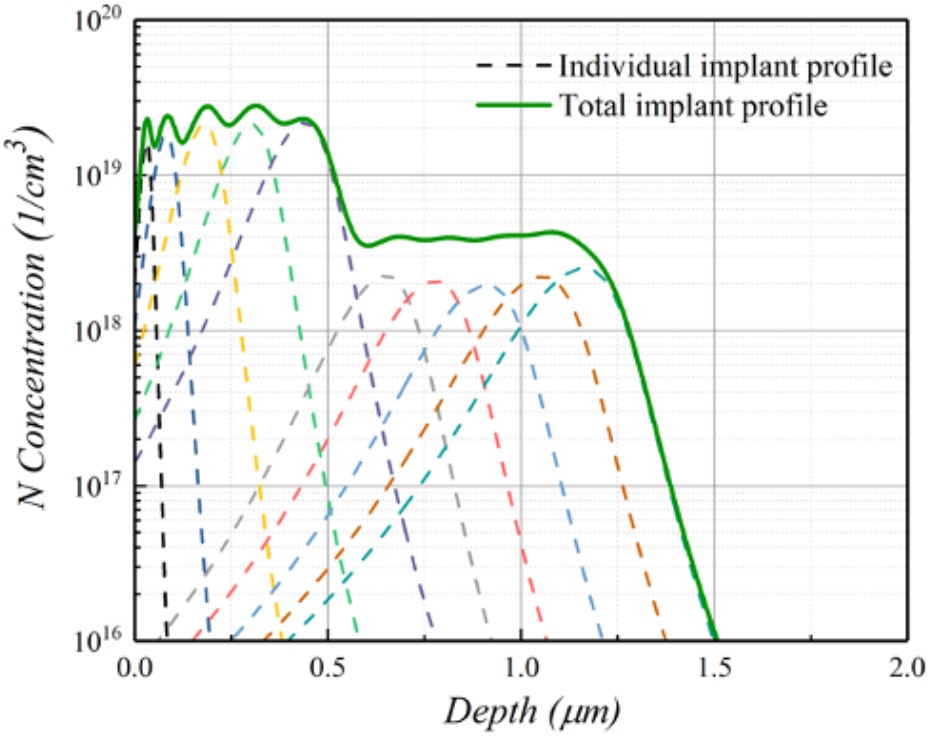


Figure 4.77.: Target N-type source implant schedule for Gen-2 trigate samples modelled using an analytical implant model [98]

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4.2.4.3 P+ implant

The P+ implant in the Gen-1 trigate samples was done using a combination of e-beam and optical lithography. However, the availability of a new optical maskless laser writing tool (Heidelberg MLA150) enabled the lithography for the P+ implants to be done in a single step. A metal lift off process is used, and a 500 nm thick Ni mask is deposited on the sample as shown in Figure 4.78(a).

The implantation is carried out at 500°C at CuttingEdge Ions. SEM images of the active area after the implant is shown in Figure 4.78(b), where the areas with the P+ implanted regions appear bright in color.

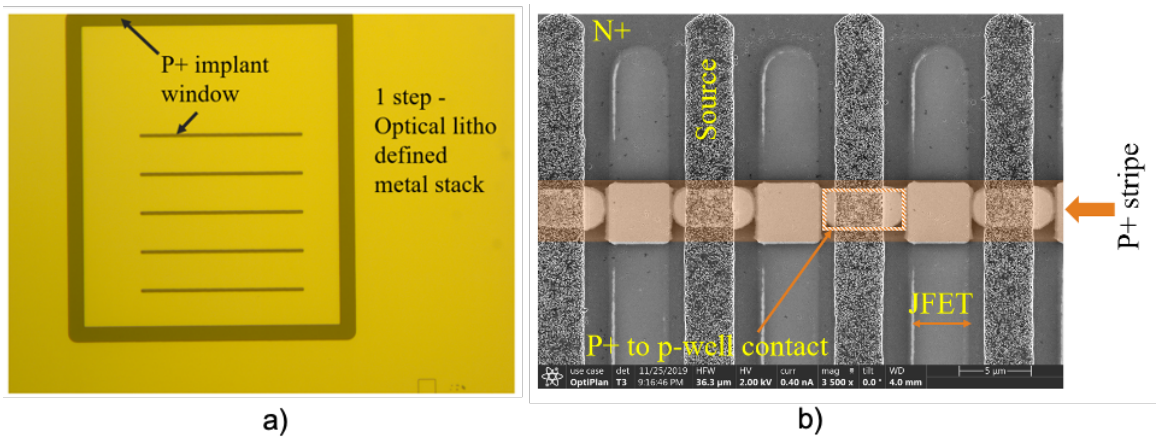


Figure 4.78.: P+ implantation for the Gen-2 trigate MOSFETs. (a) Metal mask defined by a one step optical lithography process, (b) SEM image of the active area after the P+ implantation.

Once all the implants are completed, the mask is stripped off and the implant anneal is done using the exact same process as described for the Gen-1 samples in Section 4.2.1.4.

4.2.4.4 Trench Etch

Two out of the four trigate Gen-2 samples (400Q1 and 400Q4) were carried forward to completion, while the remaining two samples (394Q1 and 394Q4) are stored for future completion. The trigate Gen-2 samples have a trench depth of 1µm and use the same trench etch process as the Gen-1 samples. This process involves the use of a metal mask that is patterned in the active area using e-beam lithography, and the field and test structure areas are patterned using optical lithography as discussed in Section 4.1.2.

Both the Gen-2 trigate samples are etched using the STS AOE ICP-RIE system. First, a test run is done to calibrate and verify the etch rate. The trigate samples are then loaded onto a carrier wafer, ensuring good thermal contact by using uniformly applied crystal bond on the back surface, and trenches are etched using the recipe

listed in Appendix B. The trench depths on samples 400Q1 and 400Q4 are 0.8 µm and 0.92 µm, respectively.

4.2.4.5 Gate stack and metal contacts

After the trench etch, a sacrificial oxide as grown and immediately etched on both samples to remove any surface roughness, defects and impurities introduced during the etch. A split experiment was conducted on the Gen-2 samples: Sample 400Q1 was subjected to a hydrogen etch at 1500°C and 150 mTorr for 3 minutes, while sample 400Q4 did not undergo this etch.

The optimized poly-ox process discussed in Section 4.2.3 was used, and the polysilicon gate was patterened using ebeam lithography as shown in Figure 4.79(a) and (b). This is followed by thermal oxidation to form a 1 µm thick ILD as seen in Figure 4.79(c). At this point, sample 400Q4 is stored in a dry box. On sample 400Q1, ohmic contacts were formed using a 50 nm nickel silicide process as described in Section 4.2.3, and then a thick metal stack comprising of 30nm of titanium and 500 nm of gold was sputtered to form the top metal. The top metal was then patterned to isolate individual devices and test structures by using optical lithography and wet chemical etch as described in Appendix B. A top view optical micrograph image of sample 400Q1 after completion of all fabrication steps is shown in Figure 4.79(d). Results from electrical measurements of this sample are discussed in the next chapter.

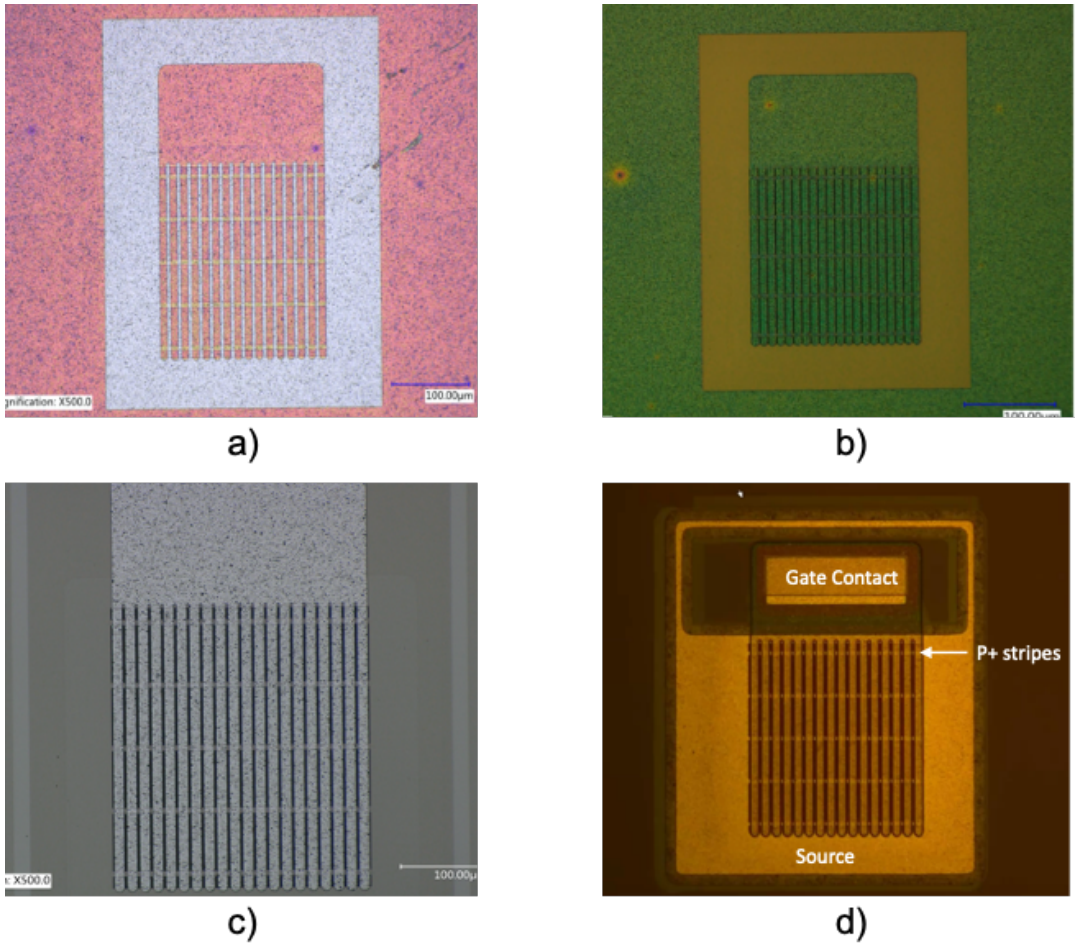


Figure 4.79.: Optical images of the Gen-2 trigate sample 400Q1 after a) e-beam exposure and development to define the gate fingers, b) Polysilicon etch using the Bosch process to form the gate runners, c) ILD pyrogenic oxidation at 1100°C for 4 hours and 20 minutes, d) Completed device with ohmic anneal at 1000°C for 3 minutes in argon and top metal deposition (Ti/Au).

5. ELECTRICAL CHARACTERIZATION OF TRIGATE DMOSFETS

This chapter discusses the results of measurements and analysis of fully fabricated and functional trigate DMOSFETs. The sample number and details of these samples are listed in Table 5.1. Failure analysis and insights from non-functional trigate devices on sample 4Q2 and 2Q4 are reported in the previous chapter.

The discussion of electrical measurements and analysis in this chapter is organized as follows:

1. On-state device performance.
   (a) Specific-on-resistance ($R_{on,sp}$)

   $R_{on,sp}$ from MOSFET output (I_D vs V_D) and transfer (I_D vs V_G) characteristics.

   (b) $R_{on,sp}$ for different JFET width.
   (c) Specific channel resistance
      i. Method 1 - Resistance derivative in strong inversion.
      ii. Method 2 - Variable Separation.
   (d) Gate leakage
2. Blocking voltage

Table 5.1.: List of trigate device samples reported in this chapter

Sample Name	**Generation**	**Trench Depth**	**Rated Blocking Voltage**	**H_2 Etch**
1Q3	Gen-1	2 µm	900 V	None
400Q1	Gen-2	1 µm	650 V	1500°C,70∼mbarr,3 mins.

3. Comparison of trigate $R_{on,sp}$ to state-of-the-art SiC MOSFETs.

4. Parameter extraction from the PCMs and test structures.

   (a) N+ ohmic contact resistivity.

   (b) Ohmic contact to polysilicon gate.

   (c) Gate oxide thickness on planar and trench sidewall surfaces.

   (d) N+ ohmic contact resistivity.

   (e) P-type base doping.

   (f) ILD breakdown test.

   (g) Effective and field-effect mobility.

      i. Mobility on planar surfaces.

      ii. Mobility on trench sidewalls.

   (h) Interface trap density on planar and trench devices.

5.1 On-state Device Performance

Measurements were carried out to evaluate the on-state performance of the two completed trigate samples. These I-V measurements were performed using a Keithley 4200 parameter analyzer with the probes assembled in a Kelvin configuration to eliminate parasitic voltage drops external to the device. The Kelvin probe wiring arrangement and the implementation during the measurement of the trigate devices is shown in the Figure 5.1 below. The resistance of the device at the operating point in the on-state is on the order of $\sim 5\ \Omega$, and in this range it becomes important to eliminate parasitic series resistances to effectively interpret the measured data.

For example, the measured drain current vs. gate voltage of a trigate device with and without the Kelvin configuration is plotted in Figure 5.2. The elimination of the parasitic resistance by the Kelvin configuration, especially at large drain currents, is clearly visible. Some external parasitic resistances are still present even with the

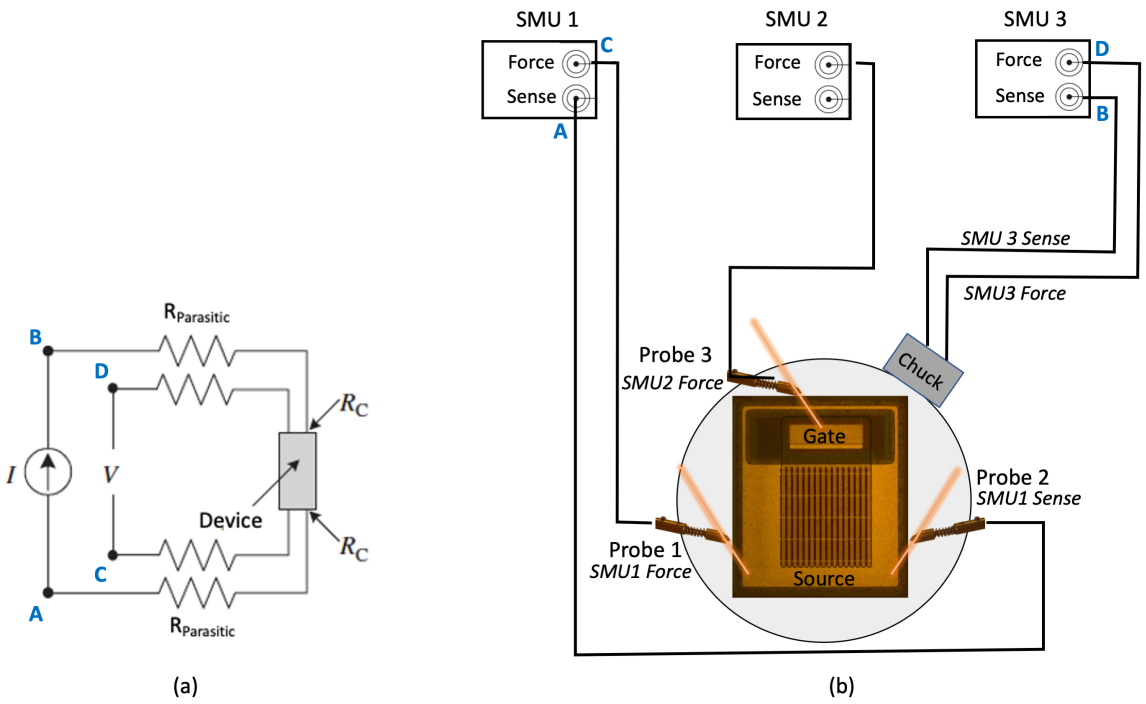


Figure 5.1.: Kelvin probe configuration and wiring diagram for measuring the on-state static IV characteristics

Kelvin setup. It is therefore useful to conduct a 'short' measurement with the kelvin setup to verify and account for these resistances.

5.1.1 Measurement of Total Specific On-Resistance

As described in the previous chapter, two main causes for source-drain shorts were identified in devices 4Q2 and 2Q4. Though we eliminated one possible source of this problem by using the 50 nm nickel silicide process, our wafers still suffer from the "missing post" problem. A few of the "post" features on the first implant mask seem to have broken off after the p-base implant, but before the n+ source implant. As all the Gen-1 and Gen-2 samples have already been implanted, no change to alleviate this problem could be made, and therefore we expect a low yield on all the trigate samples fabricated to-date. Mask design improvements to remove the isolated posts

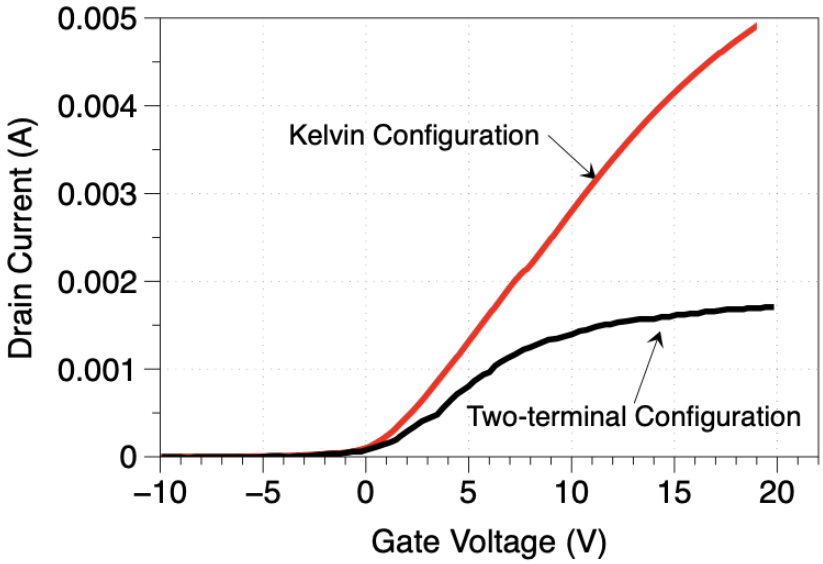


Figure 5.2.: Drain current vs. gate voltage characteristics of a trigate DMOSFET with two probe and Kelvin configuration. The effects of parasitic resistance is nullified by using the Kelvin configuration.

and therefore eliminate this problem have been suggested in Section 6.1.1. Output characteristics of trigate DMOSFETs on samples 3Q2 and 400Q1 are discussed below.

Sample 3Q2 (Gen-1)

First, functionality tests on these devices were done by measuring the drain current while sweeping the drain voltage from -0.1 V to +0.1 V with the source terminal grounded and -10 V applied to the gate terminal. Over 900 devices were tested on sample 3Q2 (Gen-1), and only four devices were found to be functional in the on-state. The failed devices showed a resistor-like linear I-V response. The output characteristic (drain current vs. drain voltage) for one such device is shown in Figure 5.3. Though the device exhibits a nominal on-state behavior, the presence of a source-drain short is evident from a residual constant drain current measured in the off-state. This can be clearly seen in the inset of Figure 5.3, which shows the drain current as a function

of gate voltage at a fixed drain voltage of 30 mV. However, this does not appear to be an inability to turn off the channel by the gate, since the drain current curves at different gate voltage compress as they approach the leakage floor. One possible source of this leakage current could be the missing post which would form a parasitic, gate independent leakage path from source to drain in parallel with the MOSFET channel.

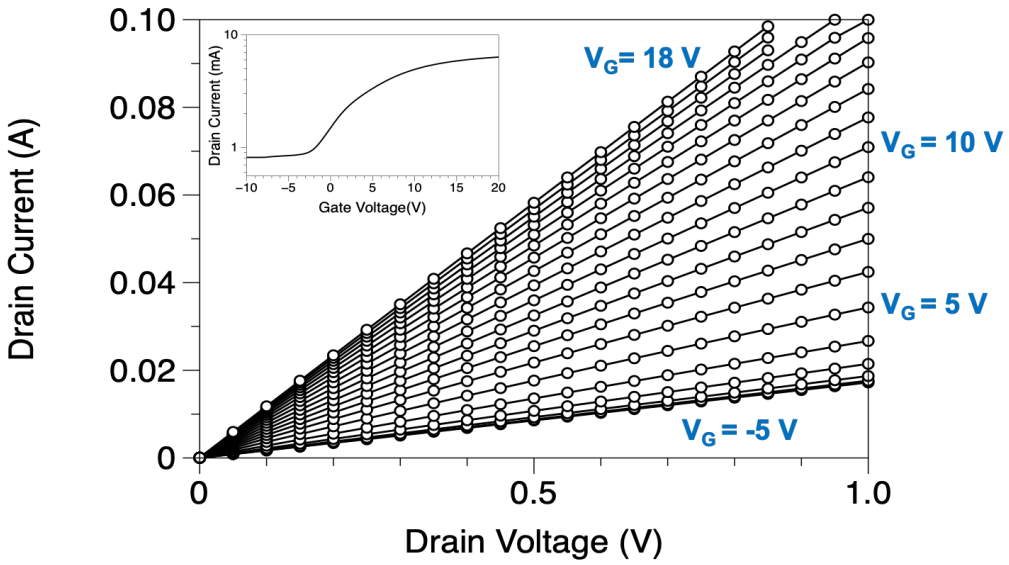


Figure 5.3.: Drain current vs. drain voltage characteristics of a trigate DMOSFET (device I) with area of 3.465×10^{-4} cm^2 on sample 3Q2 for various gate voltages. (Inset) Drain current vs. gate voltage at a fixed drain voltage of 30 mV. The parasitic leakage is evident at negative gate voltages in the off-state.

Sample 400Q1 (Gen-2)

A higher yield and a greater number of working devices were found on the second sample, 400Q1, in which 46 out of the 114 devices tested were found to be working normally. This is a Gen-2 sample with a 5.2 µm thick epi layer designed for a blocking voltage of 650 V, and 1 µm deep trenches. We have a total of 12 device variations

in the sample with different JFET and source contact widths as discussed in Section 3.5. We were able to measure devices corresponding to all the 12 variations.

I-V measurements were carried out with the source grounded and a voltage sweep applied to the drain. The current in the drain terminal was measured for each gate voltage stepped from -5V to 18V. As these measurements are done in a quasi-static mode, care was taken to keep the power dissipation less than 500 W/cm^2. High power dissipation leads to internal heating, which leads to increased resistance and reduced threshold voltage. A plot of drain current vs. drain voltage at low gate voltages (-5 V to 5 V) for device type I with total area of 3.465×10^{-4} cm^2 is shown in Figure 5.4. This device is representative of the measured sample set. To obtain the on-resistance of the device in the operating region corresponding to an oxide field of 4 MV/cm, the drain current sweep is limited from 0 V to 1 V, while the gate voltage is stepped from -8 to 18 V as shown in Figure 5.5.

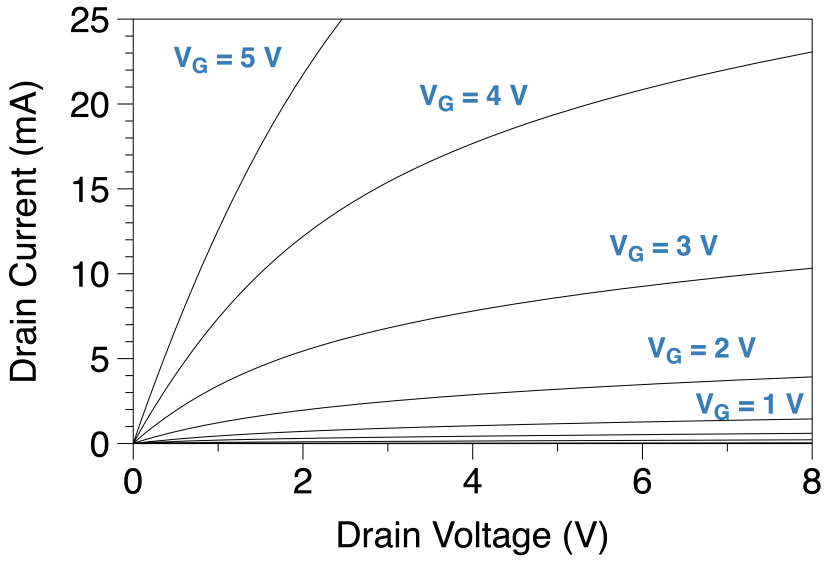


Figure 5.4.: Drain current vs. drain voltage characteristics of a trigate DMOSFET (device type I) with area of 3.465×10^{-4} cm^2 on sample 400Q1. The gate voltage is stepped from -5 V to +5 V.

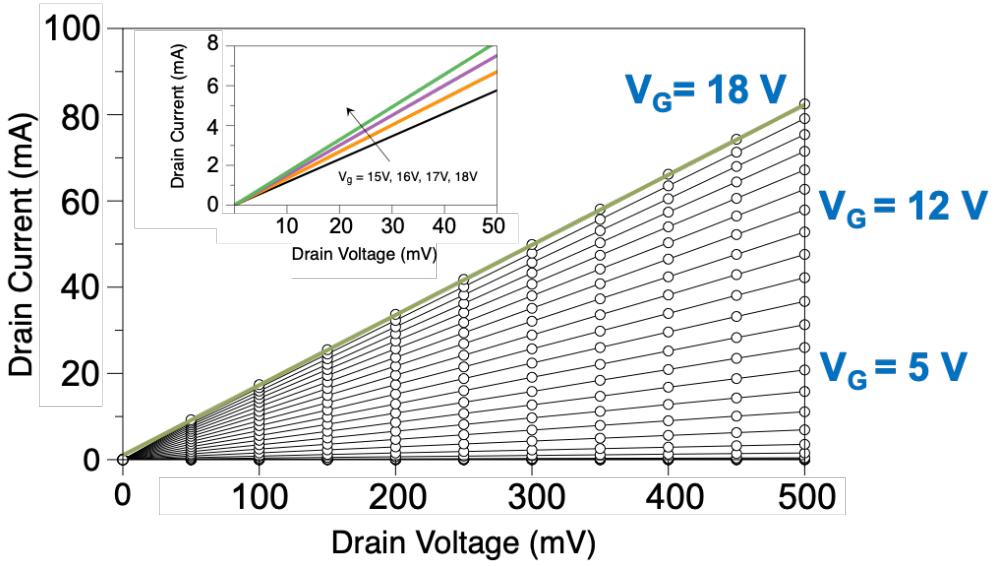


Figure 5.5.: Drain current vs. drain voltage characteristics of a trigate DMOSFET (device type I) with area of 3.465×10^{-4} cm^2 on sample 400Q1. The gate voltage is stepped from -8 V to +18 V. The green line is the gate voltage step that corresponding to an oxide field of 4 MV/cm, and the specific-on resistance is found to be 2.19 mΩ cm^2.

The specific-on resistance is calculated from the slope of the I_D-V_D curve near the origin (see inset of Figure 5.5) using (5.1). The curve corresponding to the gate voltage of 18 V (green line in Figure 5.5) that translates to an oxide field of 4 MV/cm is chosen, and the specific-on resistance is found to be 2.19 mΩ cm^2.

$$R_{on,sp} = \frac{A}{\frac{dI_D}{dV_D}\big|_{V_D\to 0}} \tag{5.1}$$

Here, A is the active area of the device. The transfer characteristics (drain current vs. gate voltage) for the same device are shown in Figure 5.6. This represents the locus of the points on the I_D-V_D curves corresponding to the drain voltage of 30 mV. The threshold voltage is calculated by linear extrapolation from the point of peak

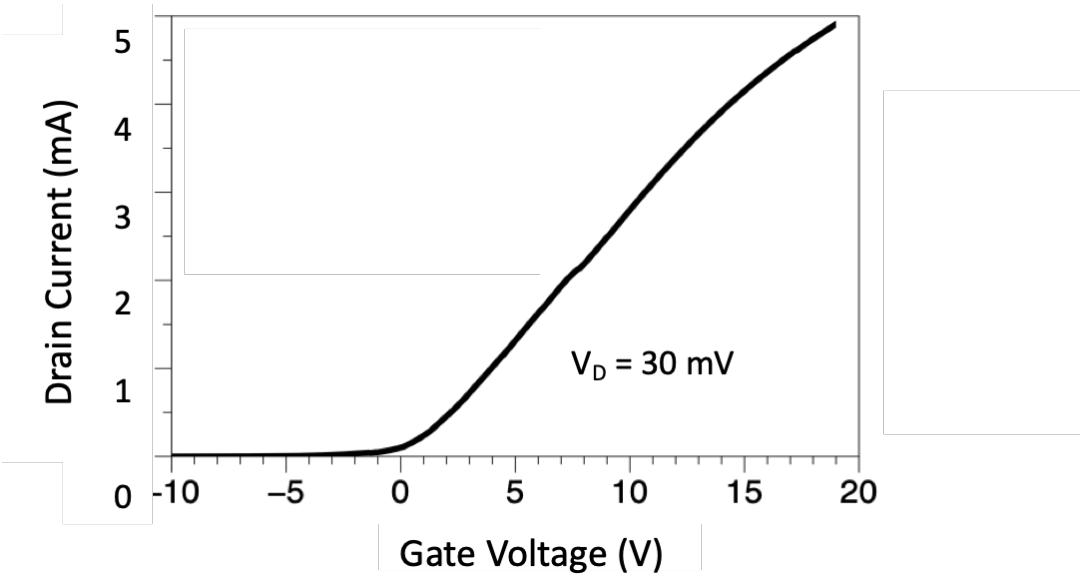


Figure 5.6.: Drain current vs. gate voltage curve of a trigate DMOSFET (device type I) with area of 3.465×10^{-4} cm^2 on sample 400Q1. The drain voltage is kept constant at 30 mV and the source terminal is grounded.

transconductance to be 0.5 V. Further, Equation 5.1 can be used to calculate the specific on-resistance as a function of gate voltage.

Specific on-resistances of the same trigate MOSFET and a planar DMOSFET of the same area, formed using the same design rules on the same wafer, are shown in Figure 5.7. When the gate voltage is negative, the transistor is in off-state and the on-resistance is high. As the gate voltage is increased beyond threshold, the channel resistance decreases until eventually being limited by the gate-independent series resistance component as seen in Figure 5.7.

5.1.2 Specific On-Resistance vs. JFET Width

Numerical simulations were performed to estimate the effect of three-dimensional current spreading and arrive at a design with an optimum JFET width as discussed in Section 3.4. To experimentally verify the simulation results, we fabricated devices

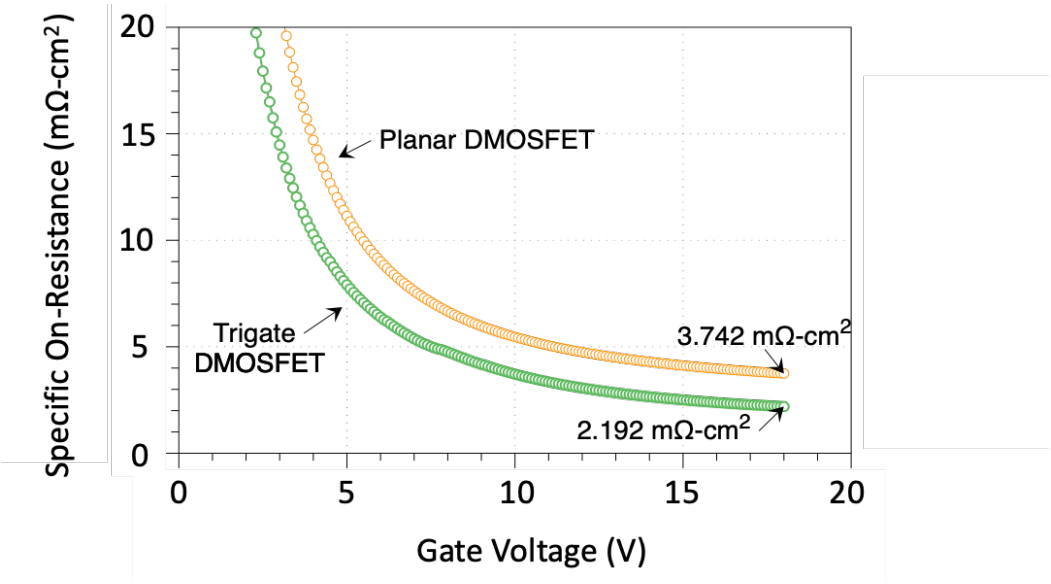


Figure 5.7.: Specific on-resistance as a function of gate voltage calculated using Equation 5.1 at a drain voltage of 30 mV.

with several JFET widths and two source contact widths. The measured on-resistance as a function of gate voltage for all JFET width variations and source lengths of 1 µm and 3 µm are shown in Figure 5.8(a) and Figure 5.8(b), respectively.

Multiple devices of each type were measured, and the mean value for each device type is listed in Table 5.2, along with the device variations. The specific on-resistance for all the variations of JFET width and source contact width in the design has been measured on the sample 400Q1. The resistance of the device is reduced as the gate voltage is increased, and at a maximuim gate voltage corresponding to an oxide field of 4 MV/cm, the measured total resistance becomes sensitive to parasitic resistances in the measurement setup. This could lead to some spread in the measured specific-on resistance as seen in Figure 5.9. As the same gate voltage is used to calculate specific on resistance, variation of threshold voltage from device to device could also contribute to the observed spread in the calculated on-resistance. Here the measured specific on-resistance is plotted for devices with different JFET widths and a source contact width of 1 µm.

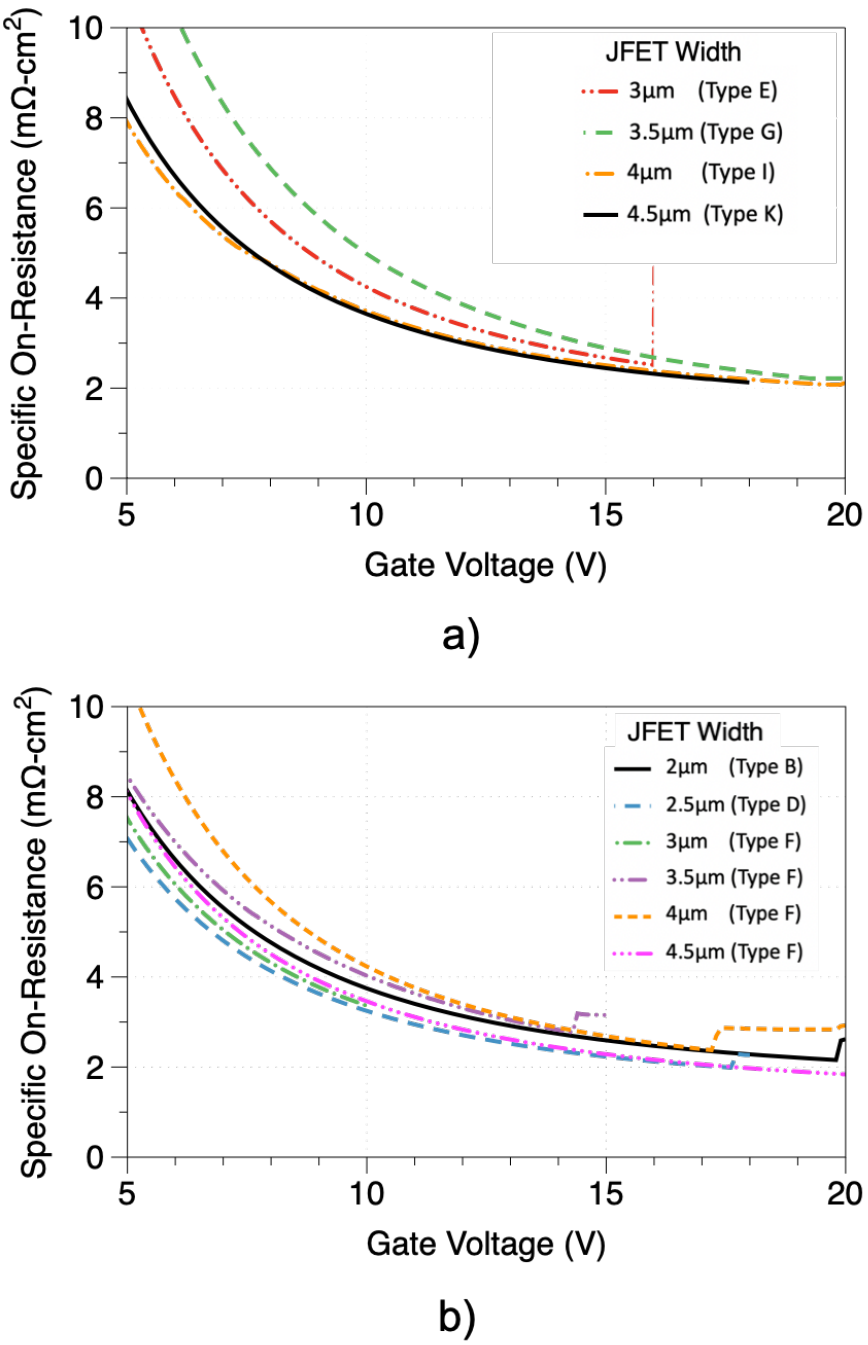


Figure 5.8.: Specific on-resistance as a function of gate voltage for a number of JFET widths. a) Source contact length of 1 µm, b) Source contact length of 3 µm.

Table 5.2.: Measured specific on-resistance at $V_G = 18$ V of trigate MOSFETs for all device variations. Multiple MOSFETs for each device variation were measured and the mean value for each is tabulated.

Device ID	**JFET Width** (µm)	**Source Length** (µm)	**Cell Pitch** (µm)	$\mathbf{R}_{on,sp}$ ($m\Omega\,cm^2$)
A	2.00	1.00	3.50	2.45
C	2.50	1.00	3.75	2.33
E	3.00	1.00	4.00	2.33
G	3.50	1.00	4.25	2.28
I	4.00	1.00	4.50	2.34
K	4.50	1.00	4.75	2.28
B	2.00	3.00	4.50	2.66
D	2.50	3.00	4.75	2.42
F	3.00	3.00	5.00	2.48
H	3.50	3.00	5.25	2.36
J	4.00	3.00	5.50	2.47
L	4.50	3.00	5.75	2.42

The mean value of the measured specific on-resistance is plotted for each device variation and compared to the corresponding result obtained by numerical simulations as seen in Figure 5.10. The substrate thickness is 350 µm in both the simulation and measured device. The trend of specific on-resistance for different JFET widths is similar between the simulated and measured values. Both the measured and simulated parameters suggests a weak dependence of JFET width on the specific on-resistance except for the lowest JFET width design.

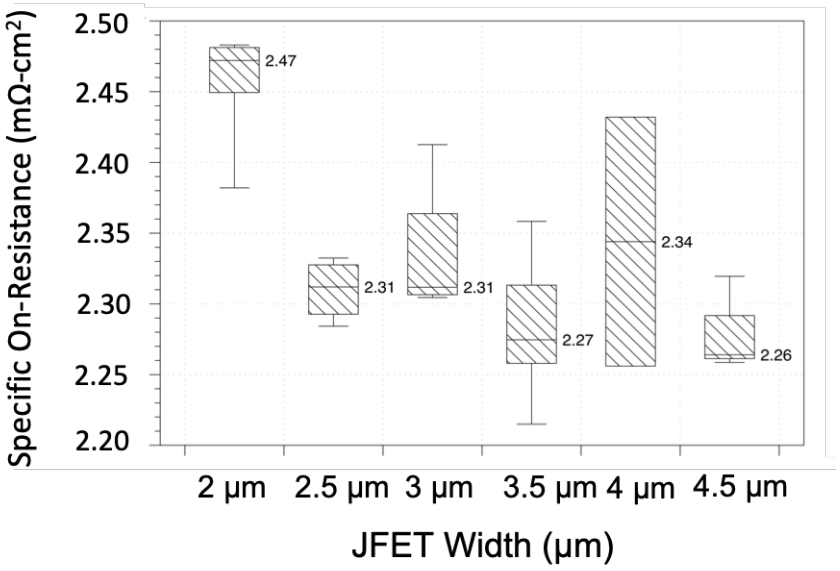


Figure 5.9.: Distribution of the measured specific on-resistance at an oxide field of 4 MV/cm for various devices with different JFET widths and source contact length of 1 µm.

There appears to be an offset between the measured and simulated values. This offset, $\sim$0.97 m$\Omega\,$cm^2, is essentially constant for all JFET widths, suggesting that the resistance component contributing to the offset is outside the JFET region, such as the source or channel resistance. Ideal source contacts are assumed in the simulation but the measured contact resistivity is about 1 $\times 10^{-5}$ $\Omega\,$cm^2, which accounts for 0.3 m$\Omega\,$cm^2. Inaccuracies in the modelling of inversion layer mobility and parasitic resistances that are present during measurements on real devices, but which are not accounted for in the simulation could be contributing to the rest of the resistance offset. Measurements on trenched lateral MOSFETs indicate that mobility in the experimental devices is lower than was assumed in the simulations by a factor of ~ 2 and is discussed in Section 5.3.4.

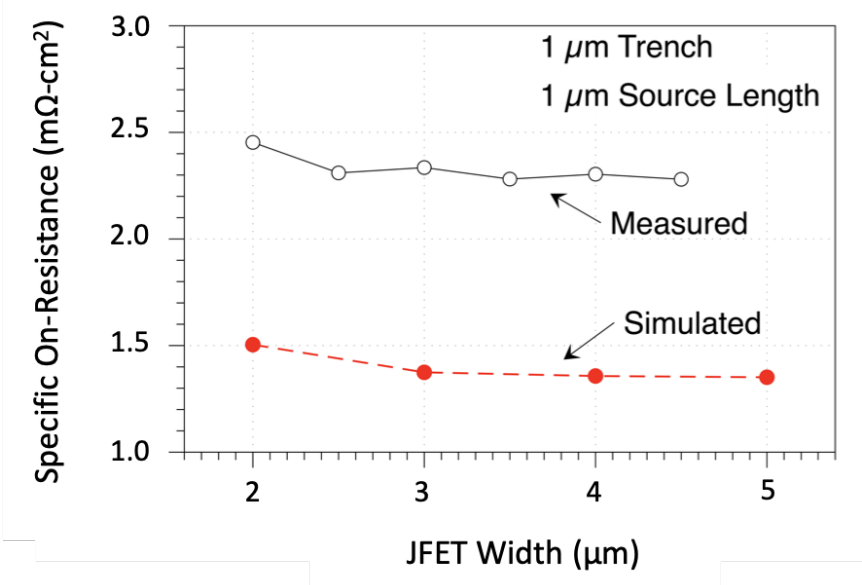


Figure 5.10.: Mean value of the measured and simulated specific on-resistance at an oxide field of 4 MV/cm for different JFET widths.

5.1.3 Specific Channel Resistance

Measured specific on-resistances of the trigate MOSFET are $\sim 1.8\times$ lower compared to a planar DMOSFET of the same area, as shown in Figure 5.8. The true benefit of the trigate device is the reduction of the channel specific resistance by the additional channel width created by the trigate geometry as discussed in Section 3.2.1. The total measured on-resistance given by (5.2) consists of various resistance components related to the flow of current from the source to the drain in a DMOSFET structure as illustrated in Figure 5.11. The total specific on-resistance can be approximated by using a lumped model given by,

$$R_{on,sp} = R_{source,sp} + R_{ch,sp} + R_{jfet,sp} + R_{drift,sp} + R_{sub,sp} \tag{5.2}$$

To evaluate the true benefit of the trigate device, two methods to separate the specific channel resistance from the measured total specific on-resistance are described below.

5.1.3.1 Method 1: On-Resistance Derivative

The total specific on-resistance, $R_{on,sp}$, of a power MOSFET given by (5.2) can be re-written as,

$$R_{on,sp} = R_{series,sp} + \ R_{ch,sp} \tag{5.3}$$

where $R_{ch,sp}$, given by (5.4), is the specific resistance of the MOS channel for the tri-gate device, and all other gate voltage independent resistances are collectively denoted as $R_{series,sp}$.

$$R_{ch,sp} = \frac{L_{ch} \times S \times \frac{W_{Cell}}{W_{ch}}}{\mu_{eff} \times C_{OX} \times (V_{GS} - V_T)} \tag{5.4}$$

Here L_{ch} is the channel length, S is the cell pitch, μ_{eff} is the effective mobility in the channel, C_{OX} is the oxide capacitance per unit area, V_g is the applied gate voltage and V_T is the threshold voltage extracted using the linear extrapolation technique

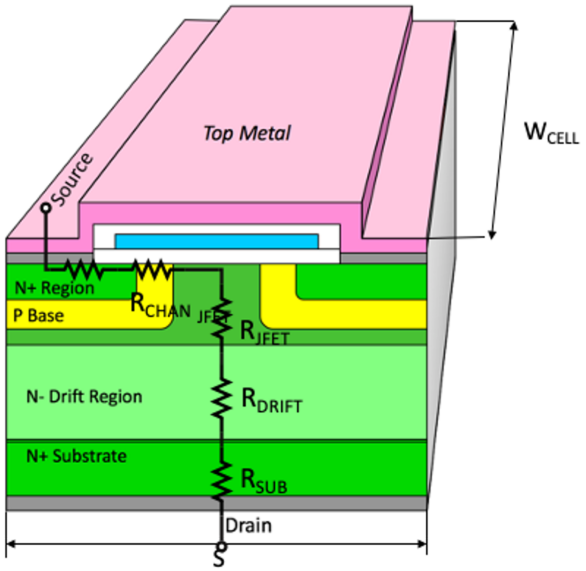


Figure 5.11.: Cross-section of a DMOSFET cell showing the most important resistance components.

[117]. Now substituting (5.4) into (5.3) the measured on-resistance can be expressed as,

$$R_{on,sp} = R_{series,sp} + \frac{K}{V_g - V_T} \tag{5.5}$$

$$\text{where } R_{ch,sp} = \frac{K}{V_g - V_T} \text{ and } K = \frac{L_{ch} \times S \times \frac{W_{Cell}}{W_{ch}}}{\mu_{eff} \times C_{OX}}.$$

As the applied gate voltage increases, the channel resistance is reduced as seen in (5.4), and when the channel resistance becomes negligible the total resistance saturates at $R_{series,sp}$. Therefore, the series resistance can be obtained from the asymptote of the measured $R_{on,sp}$ vs. V_g plot. However, the measured data-set includes on-resistance in a limited gate voltage range. Therefore (5.5) is used to fit the measured data and obtain the series resistance component.

To eliminate the series resistance component from the fit, (5.5) is differentiated with respect to gate voltage,

$$\frac{\partial R_{on,sp}}{\partial V_g} = -\frac{K}{(V_g - V_T)^2} \tag{5.6}$$

and

$$\frac{-1}{\frac{\partial R_{on,sp}}{\partial V_g}} = \frac{(V_g - V_T)^2}{K} \tag{5.7}$$

Now, the measured data is fit with (5.6) with K and V_T as the fit parameters. The parameters obtained from the result of the fit are denoted by K_{fit} and $V_{T(fit)}$ as illustrated in Figure 5.12(a). The constant K_{fit} is then used to find the expected channel specific resistance using (5.4) to get,

$$R_{ch,sp(fit)} = \frac{K_{fit}}{\left(V_g - V_{T(fit)}\right)} \tag{5.8}$$

The calculated specific channel resistance is then subtracted from the measured specific on-resistance to obtain the estimated specific series resistance using (5.3).

$$R_{series,sp(fit)} = R_{on,sp} - R_{ch,sp(fit)} \tag{5.9}$$

The value of $R_{series,sp(fit)}$ obtained from (5.9) is constant and independent of gate voltage in the region well above the threshold voltage as seen in Figure 5.12(b). This constant value of $R_{series,sp(fit)}$ is subtracted from the on-resistance obtained from the measured data to get get the specific channel resistance.

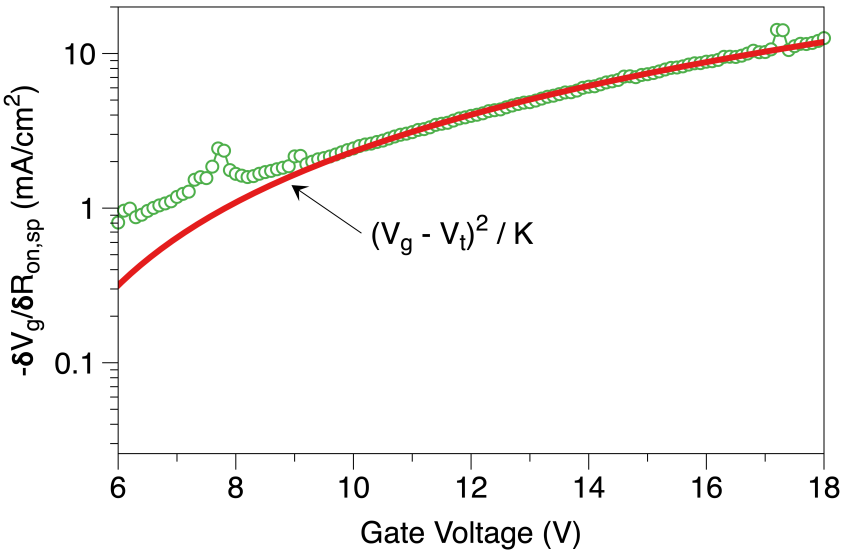
$$R_{ch,sp} = R_{on,sp} - R_{series,sp(fit)} \tag{5.10}$$

The above method was applied to a trigate and a planar DMOSFET of equal area and design, and the result is shown in Figure 5.13. The extracted specific series resistance for the trigate and DMOSFET was found to be 1.61 $\mathrm{m\Omega\,cm^2}$ and 1.55 $\mathrm{m\Omega\,cm^2}$, respectively. As these devices have the same design except for the trenches, we expect the series resistances to be the nearly the same, and therefore this result helps validate the extraction technique. The specific channel resistance corresponding to an oxide field of 4 MV/cm is 0.582 $\mathrm{m\Omega\,cm^2}$ and 2.192 $\mathrm{m\Omega\,cm^2}$ for the trigate and planar DMOSFET respectively.

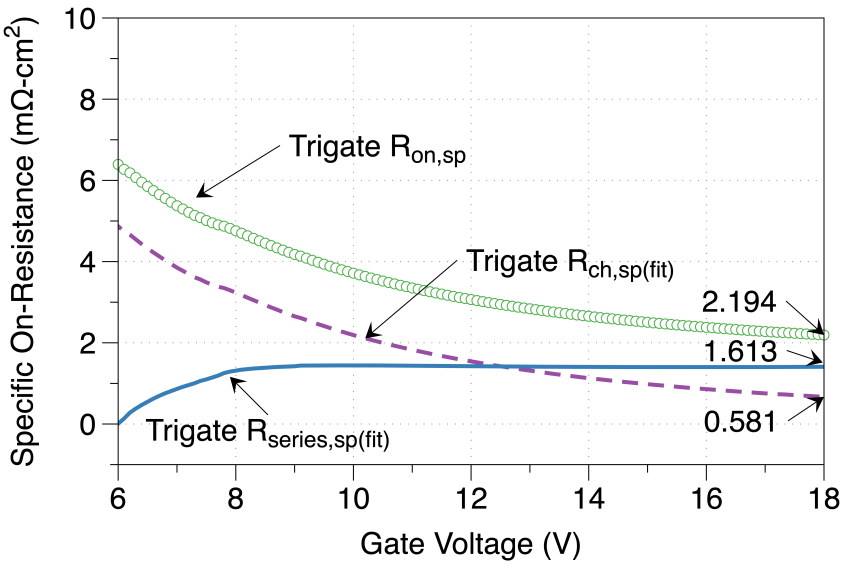
This method is useful, and can be quickly applied to the measured data to extract the channel resistance component. However, it has one major drawback. Channel mobility is assumed to be a constant in (5.5) which is used to fit the measured data and obtain the value of K_{fit}. This assumption does not hold in practice, as there is always a decrease in mobility associated with scattering at high gate voltages. Therefore, this method gives good estimate of the channel resistance in the regime where the effective mobility is a weak function of gate voltage.

5.1.3.2 Method 2: Variable Separation

An alternative method was developed to include mobility degradation at high gate voltages, and therefore overcome the main limitation of the first method. This method uses the effect variations in cell pitch have on the various resistance components. The



(a)



(b)

Figure 5.12.: Extraction of specific channel resistance from total resistance using method 1: (a) Equation (5.5) is fit to extract specific on-resistance; (b) Specific channel resistance and specific series resistance as calculated using (5.8) and (5.9). The total on-resistance of the trigate device is also shown for comparison.

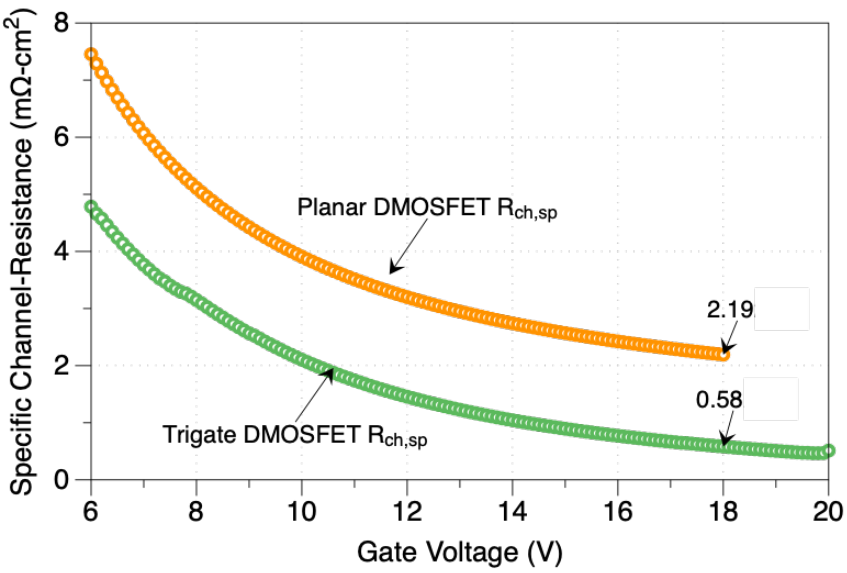


Figure 5.13.: Specific channel resistance estimated by method 1 for trigate and planar DMOSFETs of equal area.

expression for the total specific on-resistance and specific channel resistance of the trigate MOSFET is given by (5.3) and (5.4) and is repeated below:

$$R_{on,sp} = R_{series,sp} + \ R_{ch,sp}$$

$$R_{ch,sp} = \frac{L_{ch} \times S \times \frac{W_{Cell}}{W_{ch}}}{\mu_{eff} \times C_{OX} \times (V_g - V_T)}$$

Here, L_{CH} is the channel length, S is the cell pitch of the device, μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance and V_T is the threshold voltage calculated by the linear interpolation method.

As discussed in the previous section, the series resistance is independent of gate voltage, and is dominated by the drift and substrate resistances. To first order, the current flow in the drift and substrate regions is vertical, and therefore the corresponding resistances are independent of changes in the lateral dimensions such as cell pitch S. Therefore, the series resistance is assumed to be the same for all devices on the same sample, regardless of their cell pitch. However, the channel mobility is not

assumed to be a constant. The effective mobility as a function of gate voltage is often modeled by the empirical equation given by,

$$\mu_{eff} = \frac{\mu_0}{1 + \theta\ (V_G\ -\ V_T)} \tag{5.11}$$

Where μ_0 is the peak mobility at threshold and θ is the mobility degradation factor. Substituting (5.11) into the expression for specific on-resistance, we can re-write (5.3) as,

$$R_{on,sp} =\ R_{series,sp} + \frac{L_{CH} \times \frac{W_{Cell}}{W_{ch}} * S\left[1 + \theta\left(V_G - V_T\right)\right]}{\mu_0 C_{ox}\left(V_G - V_T\right)} \tag{5.12}$$

$$R_{on,sp} =\ R_{series,sp} + \frac{L_{CH} \times \frac{W_{Cell}}{W_{ch}} * S}{\mu_0 C_{ox}\left(V_G - V_T\right)} + \frac{L_{CH} \times \frac{W_{Cell}}{W_{ch}} * S * \theta}{\mu_0 C_{ox}} \tag{5.13}$$

$$R_{on,sp} = \frac{K_0}{\left(V_G - V_T\right)} + R^*_{series,sp} \tag{5.14}$$

Where,

$$K_0 = \frac{L_{CH} \times \frac{W_{Cell}}{W_{ch}}\ \times\ S}{\mu_0 C_{ox}} \tag{5.15}$$

$$\text{and,}\quad R^*_{series,sp} = K_0\theta + R_{series,sp} \tag{5.16}$$

Here, $R^*_{series,sp}$ is an *effective* series specific resistance that includes the gate voltage dependence of the channel mobility, which is described by the parameter (θ). Now the measured $R_{on,sp}$ is plotted vs. $^1/_{(V_G - V_T)}$, and a linear plot with an intercept of $R^*_{series,sp}$ and slope K_0 is obtained. This method is similar to the approach by Chung

et al. [121]. This process is repeated for all the device variations on the mask, and we obtain a series of linear curves and the value of $R^*_{series,sp}$ corresponding to each cell pitch S can be obtained from the y-intercepts.

Further, (5.15) shows that a plot of $R^*_{series,sp}$ vs. K_0 is a linear plot with slope equal to θ and y-intercept equal to $R_{series,sp}$. In this way, the series resistance component related to the mobility degradation at high gate voltage can be separated from the series resistance of the device. This method was carried out for the trigate devices with different cell pitch as seen in Figure 5.14 below. The variation in the cell pitch is due to devices with different JFET and source contact widths.

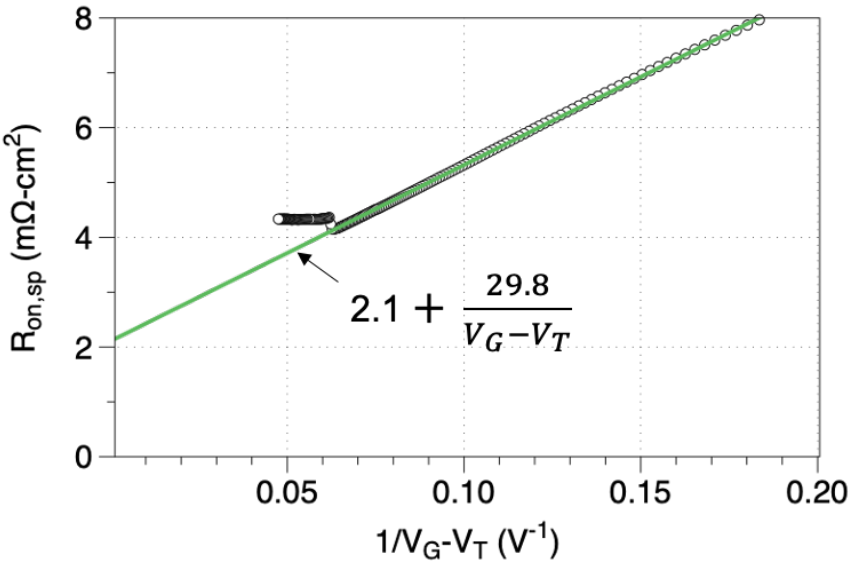
The extracted series resistance $R_{series,sp}$ is 1.53 $\mathrm{m\Omega\,cm^2}$ while the mobility degradation factor is 0.021 $\mathrm{V^{-1}}$. This factor is about a factor 2X lower than that reported in Si devices [116, 117]. The parasitic series resistance would be nearly identical in both the trigate and planar DMOSFET devices, especially when located side-by-side on the wafer. Therefore, subtracting the constant series resistance of 1.53 $\mathrm{m\Omega\,cm^2}$ from the measured specific on-resistance, the channel specific resistance is obtained. The channel specific resistance obtained by this technique on both trigate and DMOSFET devices with the same area is shown in Figure 5.16.

5.1.4 Trigate MOSFET resistance reduction

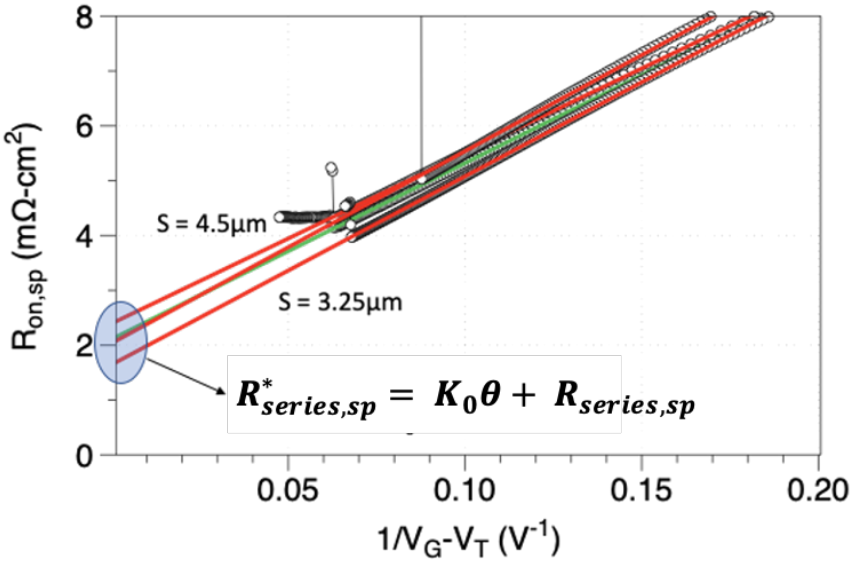
The channel specific resistance obtained by both the methods described above are similar. The value of $R_{chan,sp}$ corresponding to an oxide field of ~ 4 MV/cm is listed in Table 5.3. The trigate MOSFET reduces the channel resistance by a factor of 3.5 compared to a planar DMOSFET.

In theory, the trigate MOSFET should reduce the channel resistance by a factor proportional to the ratio of unit cell width W and the trench depth T, given by the expression below.

$$\frac{R_{chan,sp}\,(Trigate)}{R_{chan,sp}\,(Planar)} = \frac{1}{1 + \left[\ \frac{2T}{W} \times \frac{\mu_{\mathrm{horizontal}}}{\mu_{\mathrm{sidewall}}}\ \right]} \tag{5.17}$$



(a)



(b)

Figure 5.14.: Extraction of specific channel resistance from total measured resistance using method 2: (a) Example fit of the data to (5.14). (b) Measured specific on-resistance of different device variations corresponding to different cell pitches

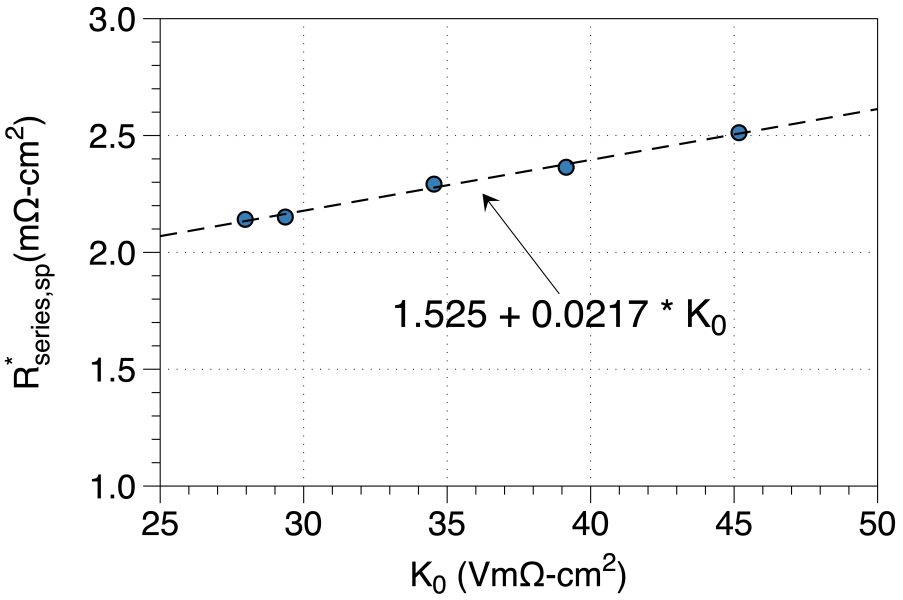


Figure 5.15.: Separation of series resistance component from mobility degradation factor

Table 5.3.: Specific series and channel resistances of device I determined by method 1 and method 2. Performance benefit is defined by the ratio of the planar and trigate specific channel resistances.

		Method 1	Method 2
$R_{series,sp}$ (mΩcm^2)	Planar DMOSFET	1.55	1.53
	Trigate DMOSFET	1.61	1.53
$R_{ch,sp}$ (mΩcm^2)	Planar DMOSFET	2.19	2.21
	Trigate DMOSFET	0.58	0.68
	R_{CH} reduction factor	3.77	3.34

The measured channel resistance ratio is consistent with the expected reduction predicted by the above equation assuming equal horizontal and sidewall mobilities. Therefore, the trigate device has a huge performance advantage over the conventional

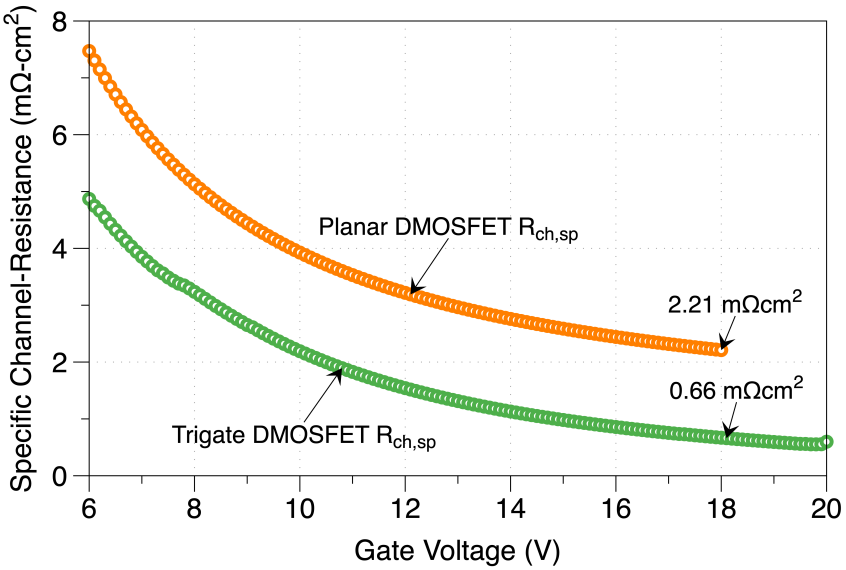


Figure 5.16.: Specific channel resistance of trigate and planar DMOSFET extracted from their respective I_D vs V_G characteristics using the above technique for device type I.

DMOSFET. In other words, employing the current trigate process with 1 µm deep trenches has the same benefit as increasing the channel mobility of a DMOSFET by $\sim 3\times$.

5.1.5 Gate leakage current and oxide breakdown field

The gate leakage using the poly-ox process on planar lateral MOSFETs is reported in Section 4.1.3. The trigate devices employ the poly-ox process, but the oxide now wraps over the topology of the trenches. The gate leakage and oxide breakdown field of both the planar and trench MOSFETs were measured and are compared in this section.

The measurement was done by grounding the source, base and drain terminals of the MOSFETs and measuring the gate current by applying a negative voltage on the gate electrode. The N+ source-gate overlap region and the N-CSL JFET region

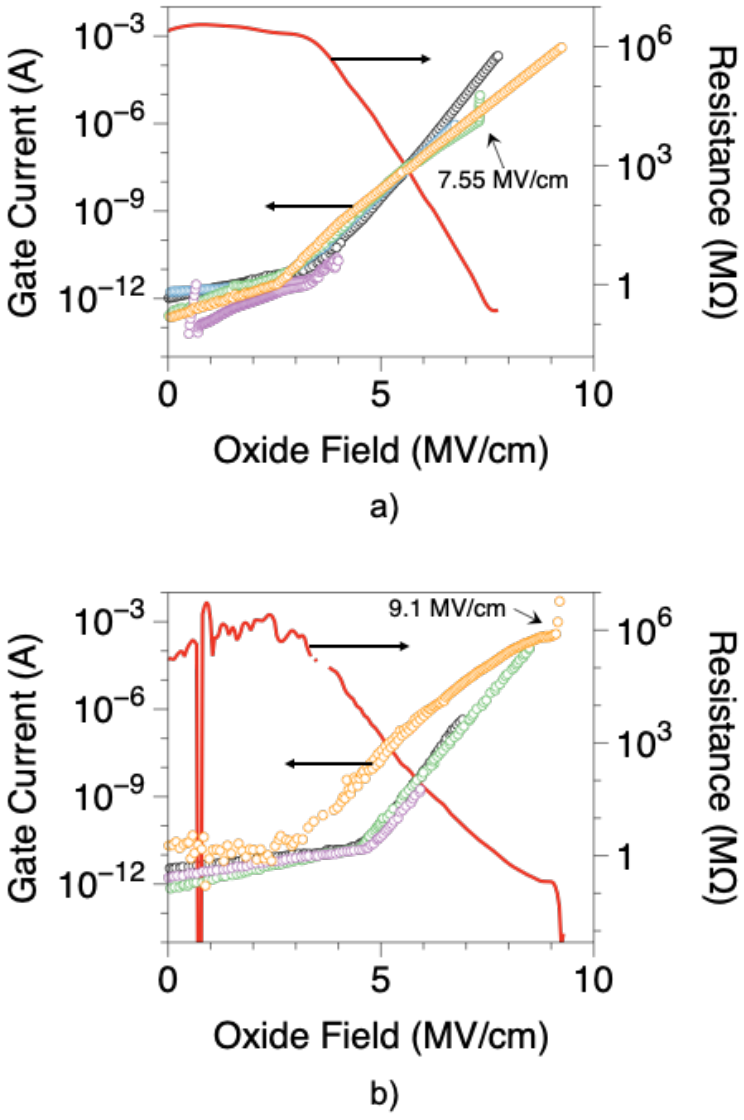


Figure 5.17.: Gate leakage current as a function of oxide field with device biased in accumulation. Oxide field calculated as $(V_G - \phi_{MS})/t_{ox}$. a) Trigate DMOSFET, b) Planar DMOSFET.

under the gate are biased towards inversion and any measured gate current must be due to transport of carriers through the gate oxide and the grounded p-base. The negative voltage applied at the gate images onto positive holes in the accumulation layer that forms over the p-base and therefore, to first order, the voltage drop can

be assumed to entirely drop across the gate oxide. The measured gate current as a function of the oxide field is plotted in Figure 5.17. The oxide field is given by $V_G - \phi_{MS} - \psi_S / t_{OX}$ where ϕ_{MS} is the work function difference between the polysilicon gate and SiC and ψ_S is the surface potential at the SiC surface. As this measurement is done in accumulation, ψ_S is assumed to be zero.

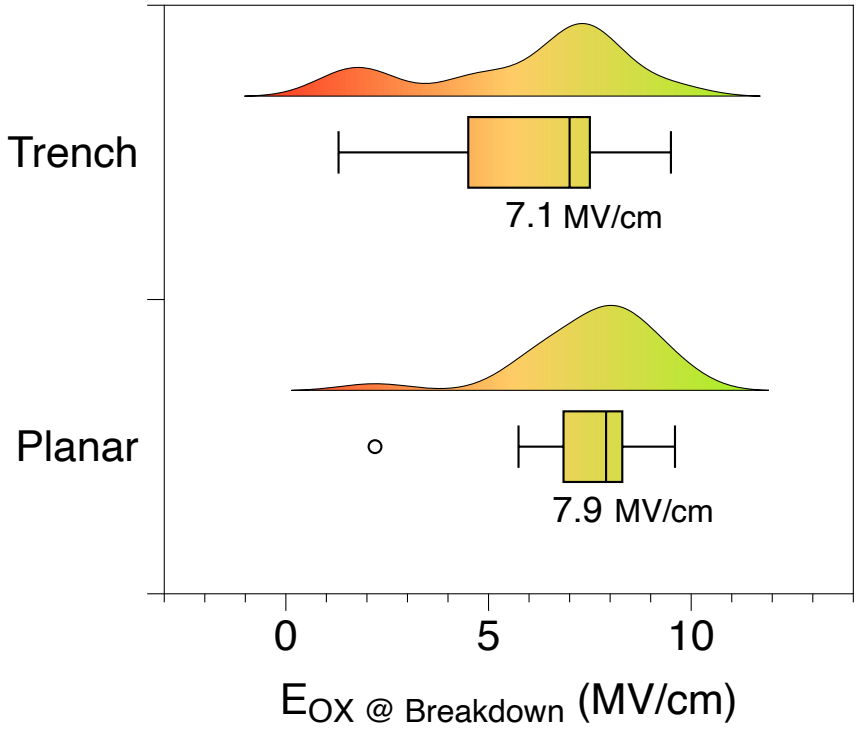


Figure 5.18.: Distribution of oxide breakdown in trench and planar trench LMOSFET devices.

As seen in the figure, the oxide on both the planar and trench devices exhibits good dielectric properties, with a resistance of over 100 GΩ at low fields. The oxide leakage current in the trigate MOSFETs is higher compared to the planar devices. Owing to its geometry, the SiC-SiO_2 interface in the trigate device is 3X larger than the planar device and therefore the corresponding gate leakage current is also expected to be higher. This could be due the higher electric field localized at the trench corners leading to higher stress induced [95] and tunneling current [122]. The current

in the high field region is usually associated with the *Fowler-Nordheim* (FN) tunneling mechanism [30]. The onset of the FN regime is usually observed to be 5-6 MV/cm in nitrided thermal oxides on SiC. This is consistent with the measured leakage observed in the planar devices. In the trigate devices, the signigicant increase in gate leakage current is observed to be around 3 MV/cm, and this could be dominated by the tunneling current due to the high electric field at the trench corner. The breakdown field of several devices was measured and the median breakdown oxide field is 7.9 MV/cm while that of trenched devices was found to be 7.1 MV/cm as seen in Figure 5.18.

5.2 Blocking Voltage Measurement

The blocking voltage and leakage current in the off-state of sample 400Q1 was measured using a custom setup where a Keithley 2410 source meter is used to apply up to 1200 V and its internal ammeter, capable of measuring currents as low as 50 pA, is used to monitor the current. A separate voltage supply is used to apply a fixed voltage(-10 V) on the gate terminal. This setup does not allow measurement of current in the gate terminal.

The leakage current through the device was measured with the gate and source grounded, while applying a reverse voltage(positive) to the drain. Standard probe arm and tip was used to probe the source and gate terminal while a high voltage probe arm with a ceramic collet holder and an in-built tip was used to probe the drain terminal. The high voltage arm was procured from *Micromanipulator Inc* with a part number: SPP20190807 and is connected to the source meter using high-voltage coaxial cable. The current compliance was set to 10 µA and a linear voltage sweep was applied. During the measurement, the wafer was immersed in Flourinert^{TM}, which is a liquid with high dielectric strength, to avoid flashover caused by breakdown of air either at the surface of the sample or between the probes.

The current in the drain terminal as a function of voltage is measured for three trigate devices of type K on sample 400Q1 as these device had the lowest $R_{on,sp}$

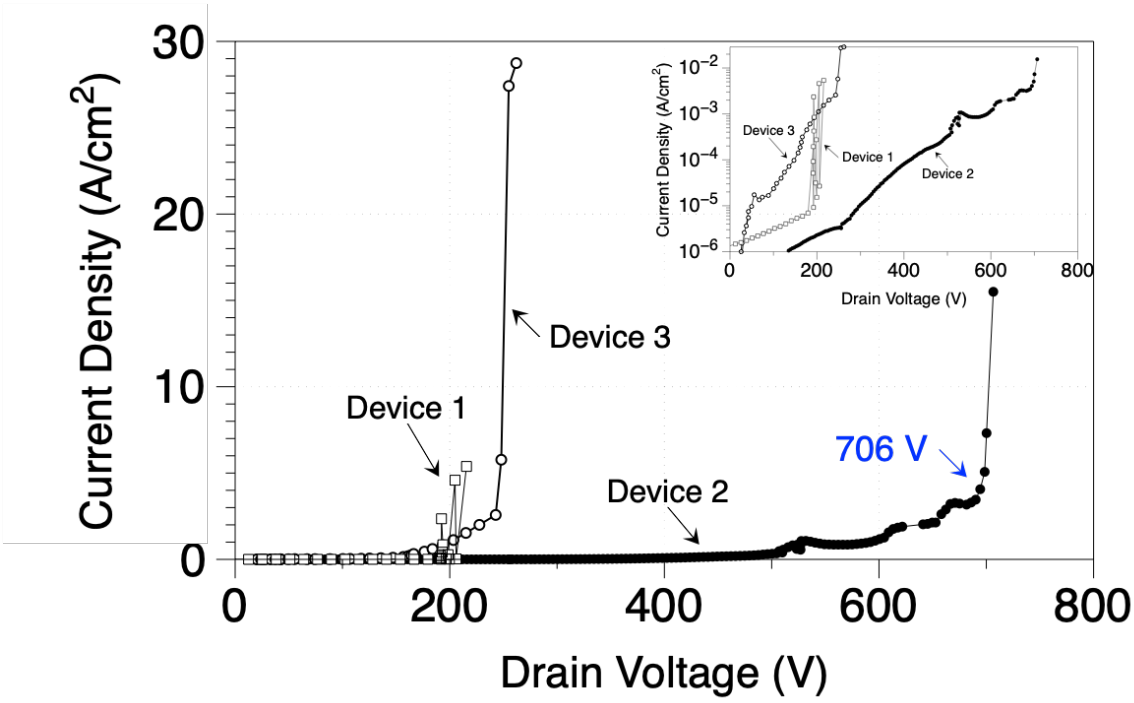


Figure 5.19.: Reverse drain current vs drain current characteristics in the blocking state in linear and log scale(inset) on trigate devices of type I on sample 400Q1.The gate voltage is held constant at -10 V during.

(Table 5.2) and is shown in Figure 5.19. As seen in the figure, the highest blocking voltage achieved among the measured devices is 706V. Sample 400Q1 is designed for a theoretical plane-junction blocking voltage of $\sim$ 900 V and therefore, the measured blocking voltage of 706 V is $\sim$78% of the theoretical value. Numerical simulation results of the floating field rings used in these devices and comparison to measurement is discussed in my colleague Naeem Islam's thesis [101].

5.2.1 Comparison of trigate $R_{on,sp}$ to state-of-the-art planar DMOSFETs and UMOSFETs.

The trigate MOSFET increases the effective width of the channel without increasing the cell pitch, and therefore is able to achieve a significant reduction in channel

resistance compared to a planar DMOSFET. The performance improvement of the trigate device compared to a planar device of the same area, fabricated on the same die is shown in Figure 5.7. Here, the planar DMOSFET is not optimally designed, as it has the same ion implant schedule as the trigate MOSFET. For instance, the p-base and source regions that are much deeper in the planar DMOSFETs fabricated in the trigate process compared with conventional planar DMOSFETs, and this introduces additional JFET resistance. The specific on-resistance of an optimally designed planar DMOSFET with a blocking voltage of 650 V, channel length of 0.5 µm and channel mobility og 20 $\mathrm{cm\,V^{-1}\,s^{-1}}$ is 3.1 $\mathrm{m\Omega\,cm^2}$ with a channel specific resistance of 1.85 $\mathrm{m\Omega\,cm^2}$ [108]. The measured trigate device 400Q1 with trench depth of 1 µm reduces the specific channel resistance by a factor of 2.7× as compared to the optimized planar DMOSFET device and therefore the overall on-resistance by 30%. Reduction in the on-resistance is limited by the substrate resistance and a thinned wafer or a waffle substrate are required to take full advantage of the trigate concept as discussed in Section 6.0.2.

The specific on-resistance of the trigate device is compared to the state of the art SiC MOSFETs as shown in Figure 5.20. The trigate device has the lowest specific on resistance of all of the DMOSFETs with a blocking voltage of 650 V. Further, the substrate in the commercial MOSFETs are usually thinned to $\sim$ 110 µm or less to reduce the substrate resistance. However,the trigate DMOSFET here has a full substrate thickness of 350 µm and therefore a further reduction of $\sim$ 0.4 $\mathrm{m\Omega\,cm^2}$ is possible with the substrate thinned to 110 µm. Further reduction in the substrate resistance by over 0.55 $\mathrm{m\Omega\,cm^2}$ is possible with the integration of a waffle substrate as described in Section 6.0.2.

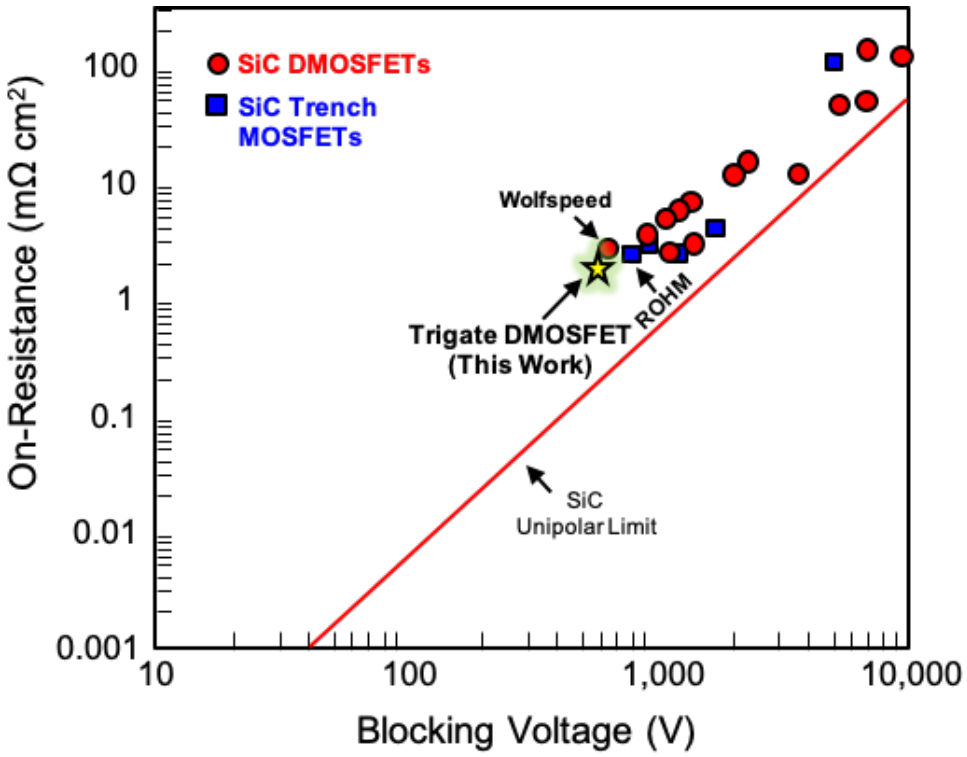


Figure 5.20.: Specific on-resistance of the trigate MOSFET compared to state-of-the-art SiC DMOSFETs [123, 124].

5.3 Parameter Extraction From PCMs and Test Structures

A number of test structures and process control monitors (PCM) are incorporated in the mask design and fabricated on the same die as the active trigate devices. A comprehensive list of the test structures included is available is Table 3.2. The extraction of a variety of device and process related parameters using the test structures is discussed in this section.

5.3.1 Specific contact resistance

The N-type source contact resistance was measured using integrated TLM test structures [117]. The layout schematic as well as the Kelvin measurement configuration for the TLM test structure is shown in Figure 5.21.

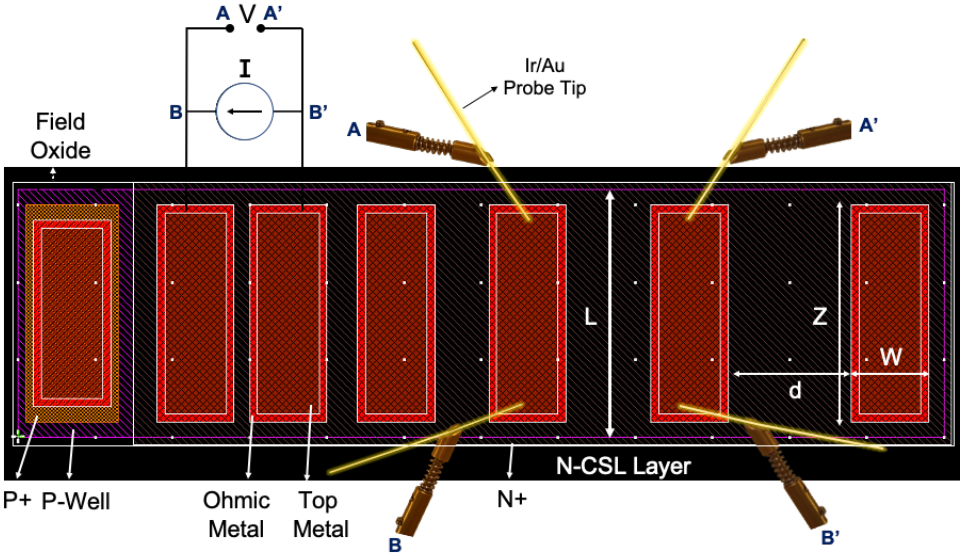


Figure 5.21.: Schematic and wiring configuration of N^+ TLM test structures used to measure source contact resistivity.

With one of the contacts grounded, the current through the probes was measured voltage while the voltage was swept from -1V to +1V on a separate set of probes. This was done for each pair of contacts in the N+ source region spaced at 80 µm, 55 µm, 35 µm, 20 µm and 10 µm. The measured I-V curves are shown in Figure 5.22.

The current flow between the two probes encounters the contact resistance at each contact and the sheet resistance of the N+ layer. The measured resistance is therefore given by the sum of these two components. From a plot of measured resistance as a function of contact spacing, the specific contact resistivity and transfer length are determined as shown in Figure 5.23. The measured contact resistivities for the 3Q2 and 400Q1 samples are $6\times10^{-6}\ \Omega\,\mathrm{cm}^2$ and $1\times10^{-5}\ \Omega\,\mathrm{cm}^2$, respectively.

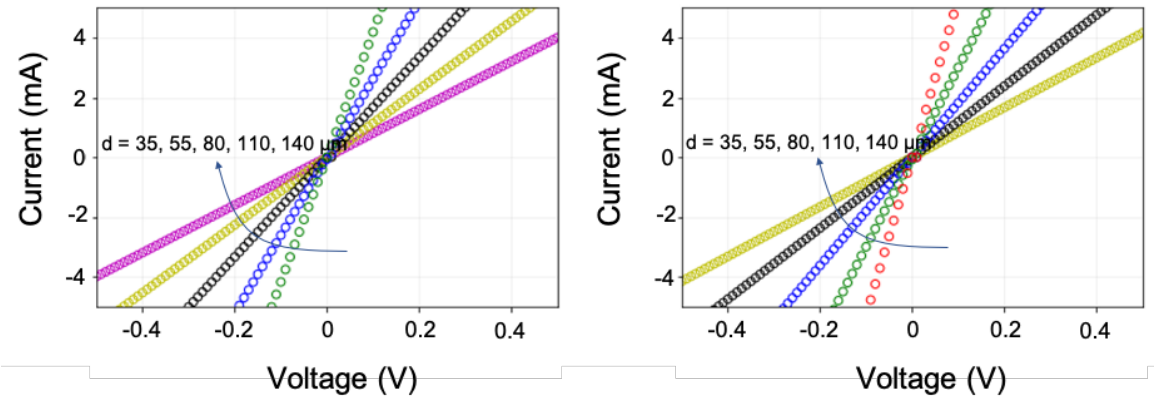


Figure 5.22.: Measured IV curves for different contact spacing on the same N+ TLM. a) Trigate sample 3Q2, b) Trigate sample 400Q1.

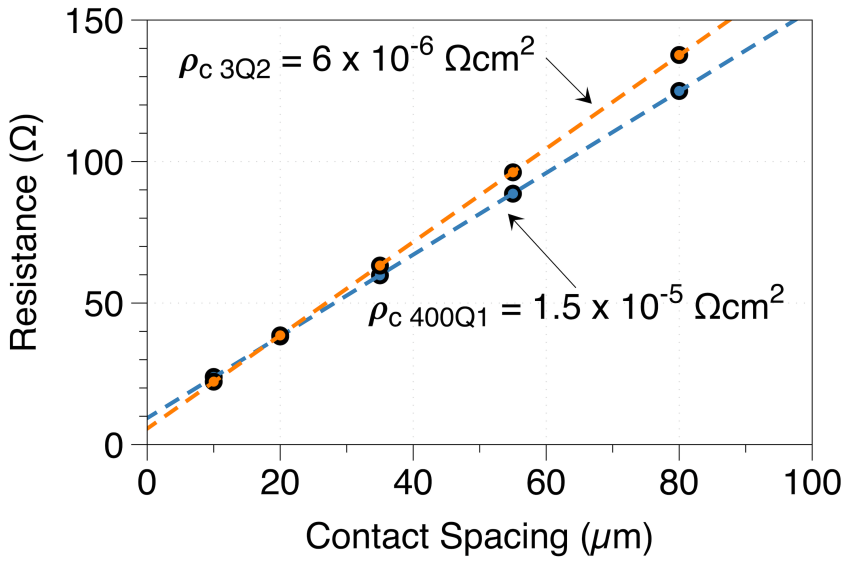


Figure 5.23.: Measured total resistance as function of contact spacing.

5.3.1.1 Ohmic contact to polysilicon gate

In the trigate devices, electrical contact to the polysilicon gate is done by etching a window in the ILD to expose the underlying polysilicon film. A thick layer of top metal (Ti/Au) is then deposited over the exposed polysilicon gate area. As this

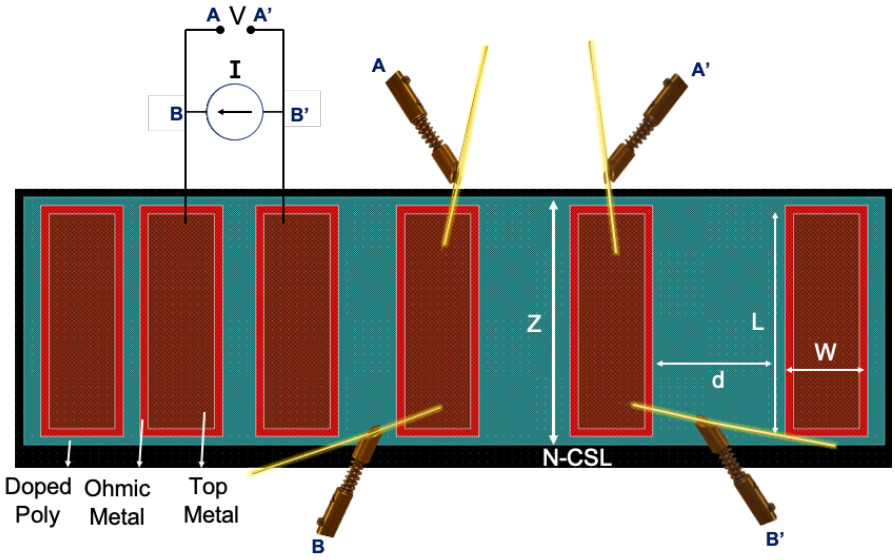
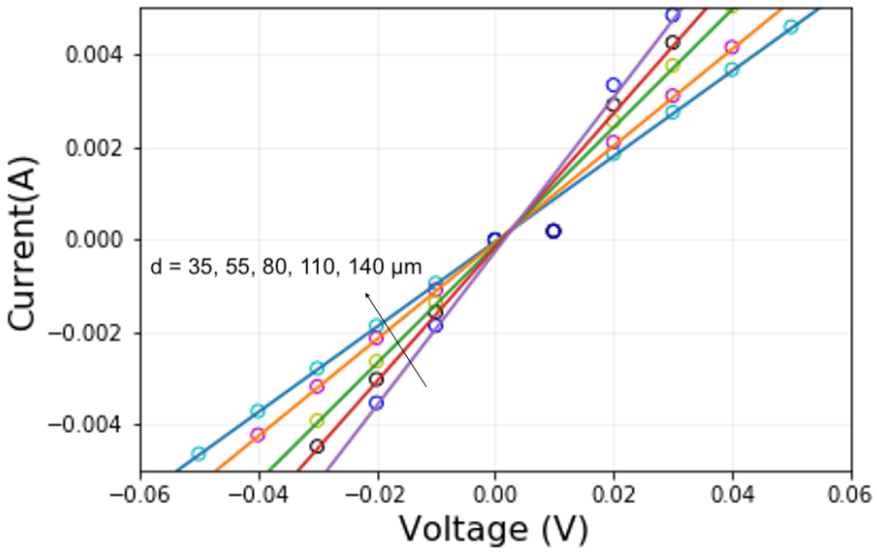


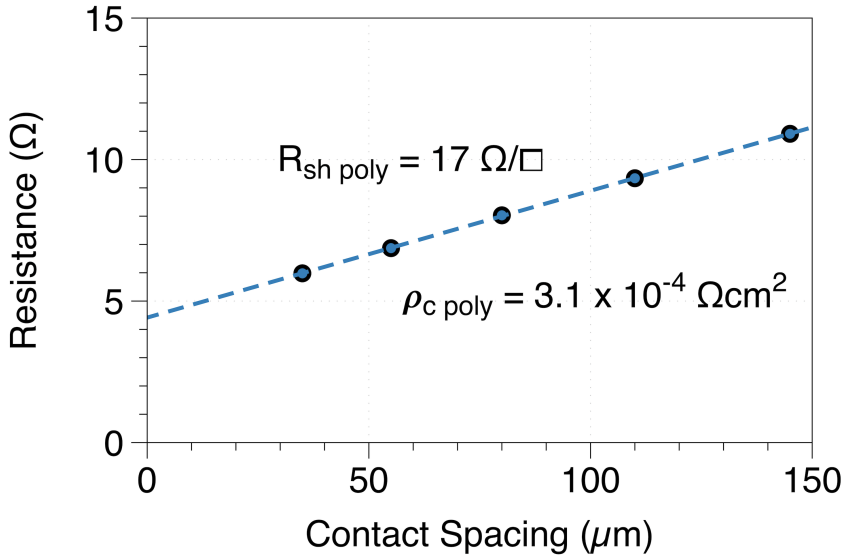
Figure 5.24.: Layout schematic of the polysilicon gate TLM and wiring configuration used to measure the linearity and sheet resistance of the doped polysilicon film

process is carried out after the source and p+ ohmic anneal step, the polysilicon gate contact is not the conventional nickel-silicide ohmic contact. Therefore the linearity of the gate contact is verified and the sheet resistance of the doped polysilicon film is determined using a polysilicon TLM test structure. The layout schematic and wiring configuration is shown in Figure 5.24.

The measured I-V curves, as seen in Figure 5.25(a), show good linearity and low resistance. The sheet resistance is calculated using the procedure described in Section.13iv and was found to be 17Ω/□ as seen in Figure 5.25(b). As the current in the gate terminal is very small, the corresponding voltage drop is also low and can be ignored during the static I-V analysis. However, the gate resistance is an important parameter for the switching characteristics of the device. In this case, the RC time constant to charge the input Miller capacitance is directly proportional to the gate resistance along with the drift and substrate resistances.



(a)



(b)

Figure 5.25.: Current vs voltage characteristics of the polysilicon gate TLM showing good linearity of the gate contact: (a) Measure I-V of the polysilicon TLM structure (b) Total resistance vs contact spacing.

5.3.2 Gate oxide thickness on planar and trench sidewall surfaces

In the trigate DMOSFET, the gate oxide is conformally deposited on the planar and sidewall surfaces of the trenches under the gate electrode. The oxide thickness on the planar surface is measured during fabrication of the devices using interference spectroscopy. The final thickness of the gate oxide on the planar and sidewall surfaces is measured using MOS capacitors fabricated with and without trenches on the N-CSL substrate.

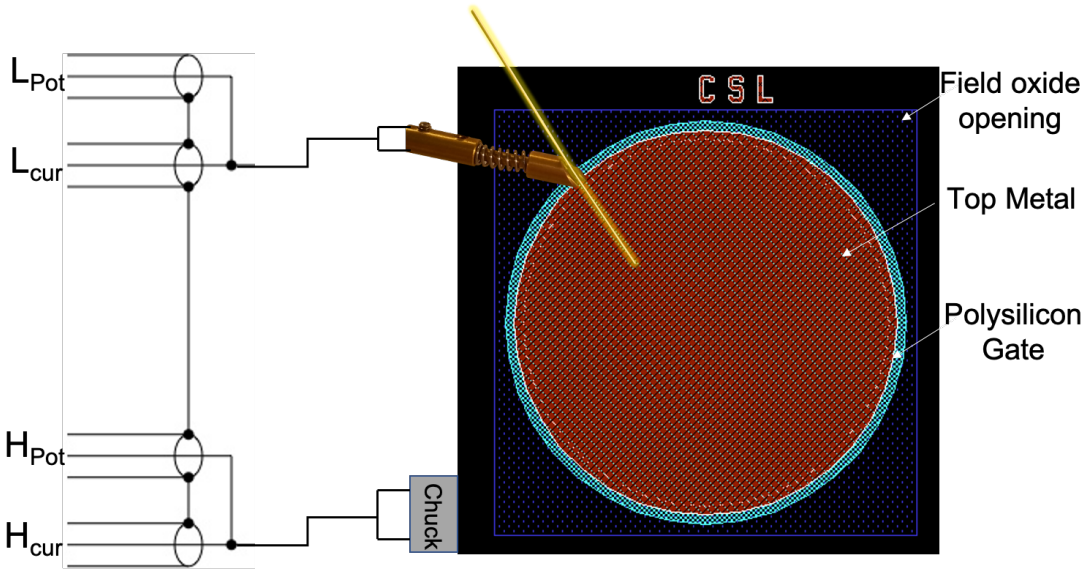


Figure 5.26.: Schematic of N-CSL MOS capacitor and wiring configuration used to measure capacitance vs. voltage.

The layout schematic of the planar capacitor on N-CSL substrate is shown in Figure 5.26. As shown in the figure, the positive voltage is applied to the 'Hi-pot' and 'Hi-cur' terminal which is connected to the chuck. The capacitance of the device is usually measured by sweeping the gate voltage from strong accumulation into deep depletion. This is implemented by sweeping the gate voltage from +10 V to -15 V in this particular measurement. The measured gate capacitance as a function of gate bias at a frequency of 100 kHz and a small signal AC voltage of 20 mV is shown

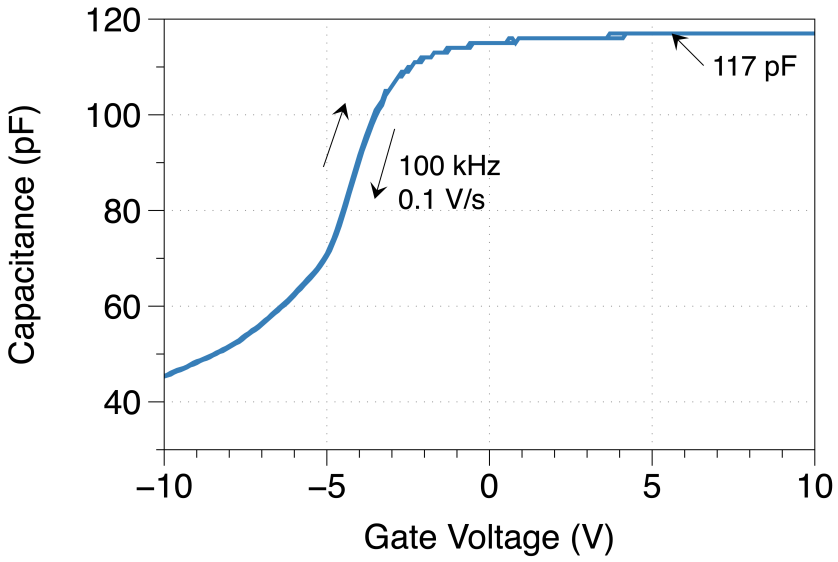


Figure 5.27.: Measured C-V response on a planar N-CSL MOSCAP at a frequency of 100 kHz and small signal voltage of 20 mV. The oxide capacitance is obtained from the accumulation region at positive gate voltage.

in Figure 5.27. The oxide capacitance is assumed to be equal to the capacitance of the device in accumulation, where the device can be thought of as a parallel plate capacitor with all the gate voltage being dropped across the oxide. As seen in the figure, oxide capacitance at large positive gate voltage is 117 pF, and the area of the gate electrode is 1.59×10^{-3} cm^2. These values are used in (5.18) to find the oxide thickness to be 47 nm.

$$C_{OX} = \frac{\epsilon_{ox}}{t_{ox}} \times A \tag{5.18}$$

Here C_{OX} is the oxide capacitance, A is the gate area, ϵ_{ox} is the permitivity of the oxide, which is 3.9 for SiO_2, and t_{ox} is the gate oxide thickness.

In the trigate device, the gate oxide wraps around the fin, and uniform thickness over this 3D geometry is important to ensure that the inversion channel is formed at the same gate voltage on both the planar and sidewall surfaces. To verify this, trench MOS capacitors on the N-CSL and p-base regions with polysilicon gates are measured. The layout schematic of the trench MOS capacitors is shown in Figure 5.28.

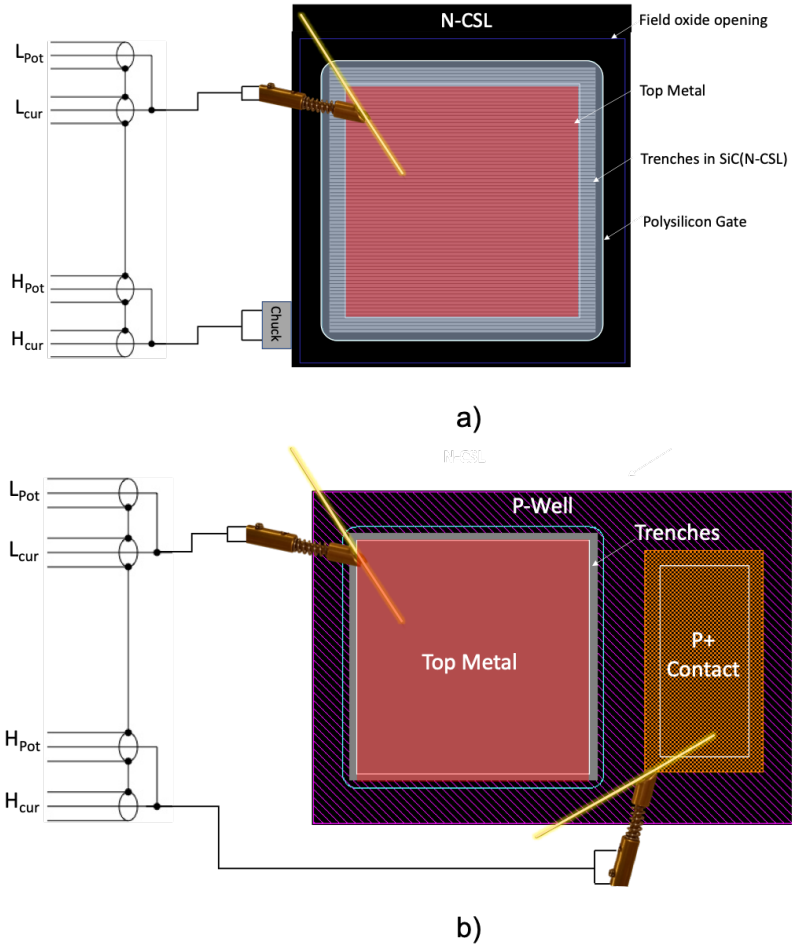


Figure 5.28.: Schematic of trench MOS capacitors on N-CSL and P-base regions with wiring configuration used to measure capacitance vs voltage.

The measured C-V characteristics of the N-CSL and p-base MOSCAPs are shown in Figure 5.29(a) and Figure 5.29(b) respectively. The oxide capacitance is determined from the accumulation capacitance as described earlier.

Equation 5.18 suggests that the oxide capacitance is directly proportional to the total area under the gate. In the case of the trench MOS capacitor, the trench width and fin width are kept constant at 0.5 µm and the trench depth is ∼1 µm, therefore total area is determined by the number of trench stripes under the gate electrode. The total area can also be expressed as the summation of the trench top, bottom and

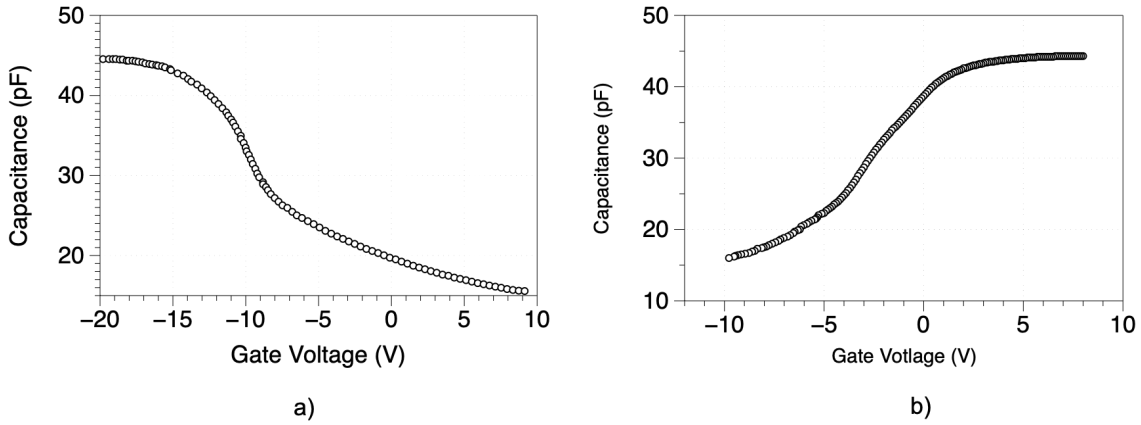


Figure 5.29.: Measured capacitance vs. voltage of planar and trenched MOS capacitors at frequency of 100 kHz and a small signal voltage of 20 mV. Dual sweep in gate voltage is done from accumulation to depletion and vice-versa at a sweep rate of 0.1 V/s. a)Trench P-base MOSCAP, b)Trench N-CSL MOSCAP.

sidewall area, and the capacitance of each of these three components are in parallel. Therefore, as seen from (5.18), any gross variation in the oxide thickness on either the top, sidewall or bottom would lead to a non-linear scaling of the oxide capacitance with respect to the total area. To determine the uniformity of the gate oxide thickness, the accumulation capacitance as a function of total gate area for the trench and planar MOSCAPs are plotted in Figure 5.30. The solid squares and hollow circles represent the trench and planar MOS capacitors respectively. A linear relationship between the measured oxide capacitance and area is observed as expected from (5.18), and the slope of the linear fit to these data points is used to calculate the oxide thickness to be 46.5 nm. This result is consistent with a uniform oxide thickness on all surfaces.

5.3.3 P-base doping

The doping in the P-base is calculated experimentally using the p-base MOS capacitor. The quasistatic and 100 kHz C-V response of the P-base capacitor was

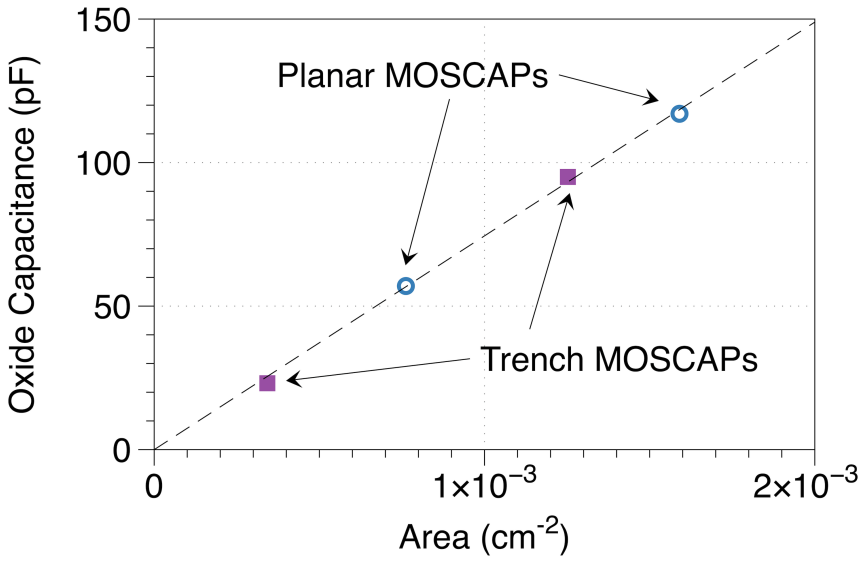


Figure 5.30.: Measured oxide capacitance for planar and trench MOS capacitors with different total area under the gate electrode. Linear scaling is indicative of the uniformity of the gate oxide on both the planar and sidewall surfaces of the trigate structure

measured at 100 kHz with an excitation voltage of 20 mV and is shown in Figure 5.31.

The doping concentration, corrected for screening by charge from oxide and interface traps, is then extracted a using the method suggested from Brews *et al.* [125] and found to be 1.5 $\times 10^{17}$ cm^{-3} as seen in Figure 5.32. This is consistent with the expected doping of the channel from the implant design of the trigate devices discussed in Section 4.1.1.1.

5.3.4 Effective and Field-Effect Mobility

The inversion channel in the trigate device is formed on the top, sidewall and bottom surfaces as described in Section 3.2. The inversion channel mobility on each of these surfaces may not be equal, and the peak value of which depends primarily on

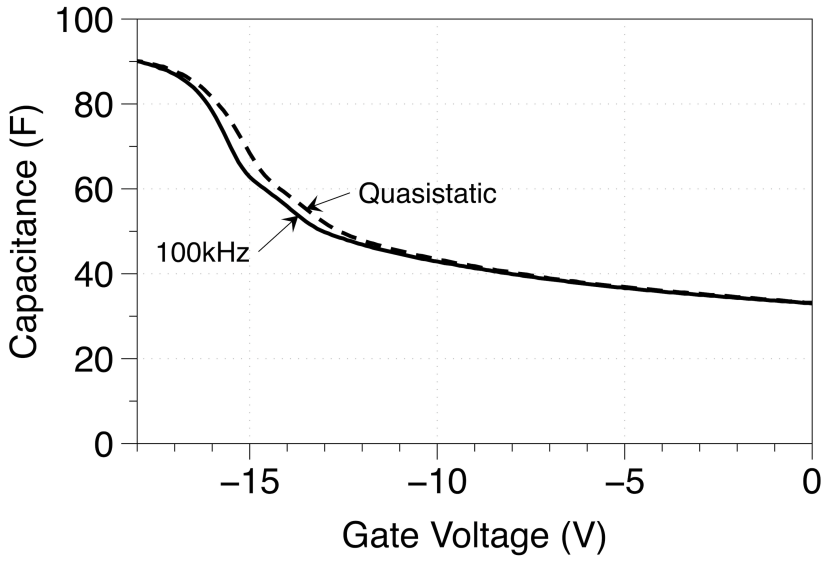


Figure 5.31.: Measured gate capacitance vs. voltage for a P-base capacitor at 100 kHz and a small signal voltage of 20 mV. Quasistatic C-V was also measured with a step voltage of 0.1 V and time delay of 0.07 sec

the interface trap density [30]. To measure these quantities accurately, lateral long channel MOSFETs are included as part of the PCM test structures. The mobility on the top and bottom surfaces are on planar surfaces and therefore expressed as one entity μ_{planar}. The mobility of the sidewall is expressed as $\mu_{sidewall}$. The determination of these two mobilities is described below.

Planar Lateral MOSFETs

The layout schematic of the planar long channel lateral MOSFET test structure with channel lengths of 50 µm, 80 µm, 110 µm and 140 µm is shown in Figure 5.33. To obtain the mobility, the schematic for the lateral MOSFET with series resistances at the source and drain terminals is shown in Figure 5.33. When the device is operated in the linear regime, the drain current can be expressed as,

$$I_D = \frac{W}{L_{CH}} \mu_{eff}\, C_{OX}\, (V_G - V_T)\, V_{DS} \tag{5.19}$$

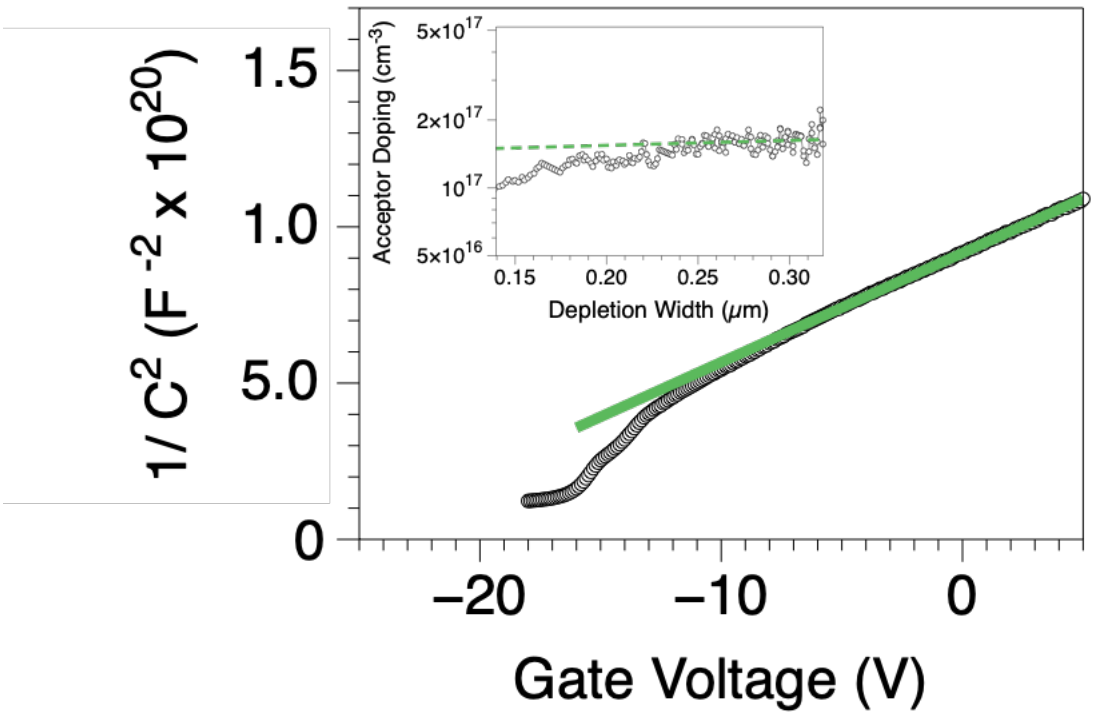


Figure 5.32.: Doping of the p-base is calculated from the slope of the $1/C^2$ curve using the procedure in [125].

The series resistance is determined using the channel resistance technique [117]. First, the total resistance $^{V_{ds}}/_{I_D}$ is plotted as a function of gate voltage for MOSFETs with different channel length as shown in Figure 5.34(a). Now at a particular gate voltage, the resistance is plotted as a function of channel length as shown in Figure 5.34(b). The resistance scales linearly with channel length, and the y-intercept in this plot represents the remaining resistance component as the channel length tends to zero. This resistance corresponds to the ungated series resistance in the device, which includes the source and drain resistance. The x-intercept represents the deviation between the physical gate length and metallurgical channel length where the metallurgical channel length is defined as the effective distance between source and drain [117]. This procedure is repeated for a number of gate voltages, and as the series resistances are independent of gate voltage in the lateral MOSFETs, the curves converge at a single

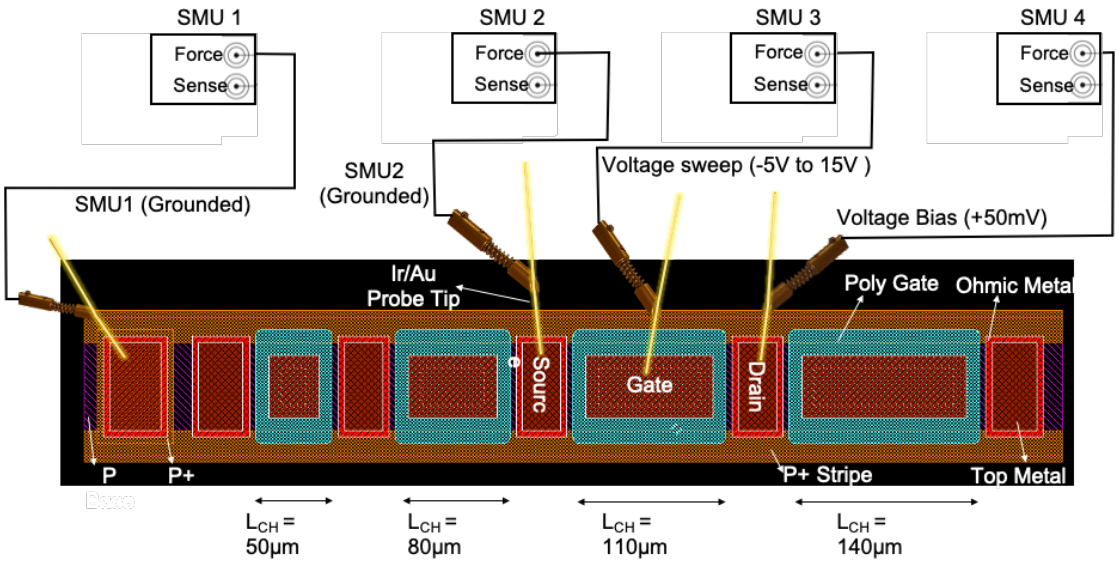


Figure 5.33.: Schematic of planar LMOSFET with different channel lengths as indicated in te figure. A separate LMOSFET test structure with a channel length of 200 µm is included in the mask set.

point as seen in Figure 5.34(b). The series resistance is found to be very small (3.8 Ω) and therefore its contribution to the total resistance of these MOSFETs can be ignored. This is consistent with the low source contact resistivity of ($\sim 1\times10^{-5}\ \Omega\,\mathrm{cm}^2$) measured using TLM patterns as discussed in Section 5.3.1.

As the source is grounded, the drain-source voltage(V_{DS}) drops entirely across the inversion channel and the effective mobility is determined by (5.19). The drain conductance g_d [117] at a specific gate voltage is given by (5.20), and the effective mobility as a function of gate voltage is calculated using (5.19) at a drain voltage of 30 mV is shown in Figure 5.35,

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \tag{5.20}$$

The effective mobility decreases with increased gate voltage, which is usually attributed to scattering due to increased confinement of electrons in the inversion

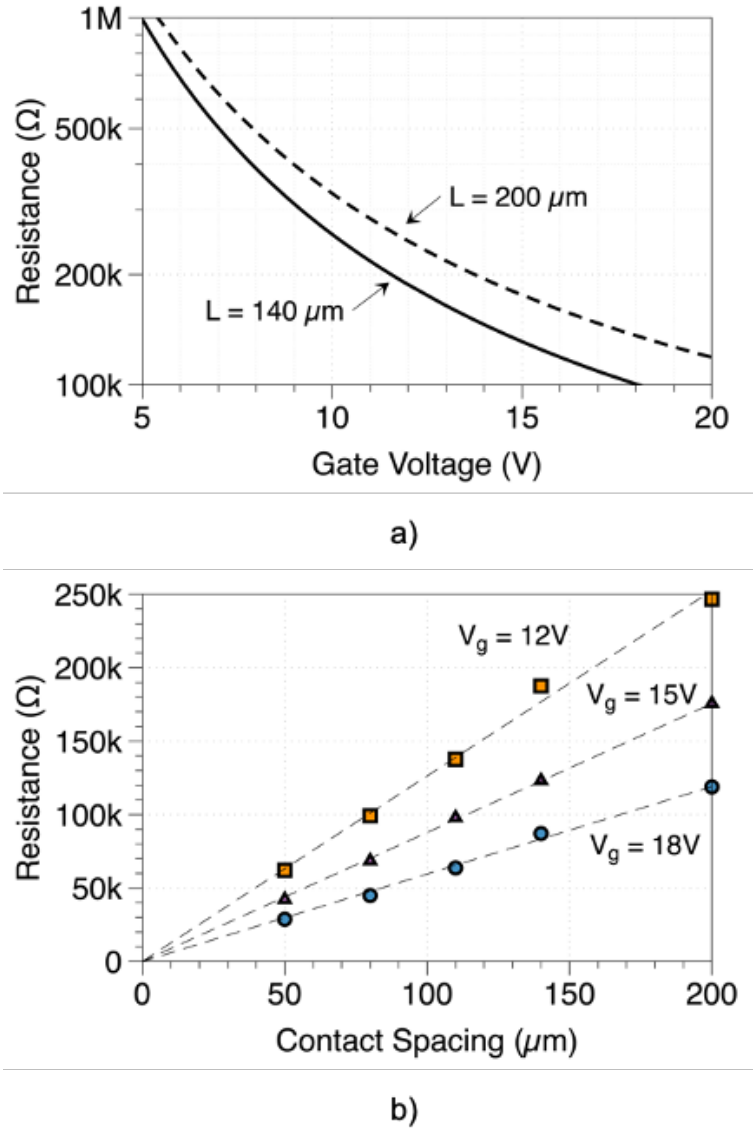


Figure 5.34.: Resistance as a function of gate voltage and contact spacing for lateral MOSFETs: a) Total resistance as function of applied gate voltage, b) Total resistance for various contact spacing(channel length). The y-intercept corresponding to intersection of different gate voltage lines is the series resistance component.

layer [116]. At high gate voltages, this effect is commonly modelled by an empirical expression given by,

$$\mu_{eff} = \frac{\mu_0}{1 + \theta\,(V_G - V_T)}$$

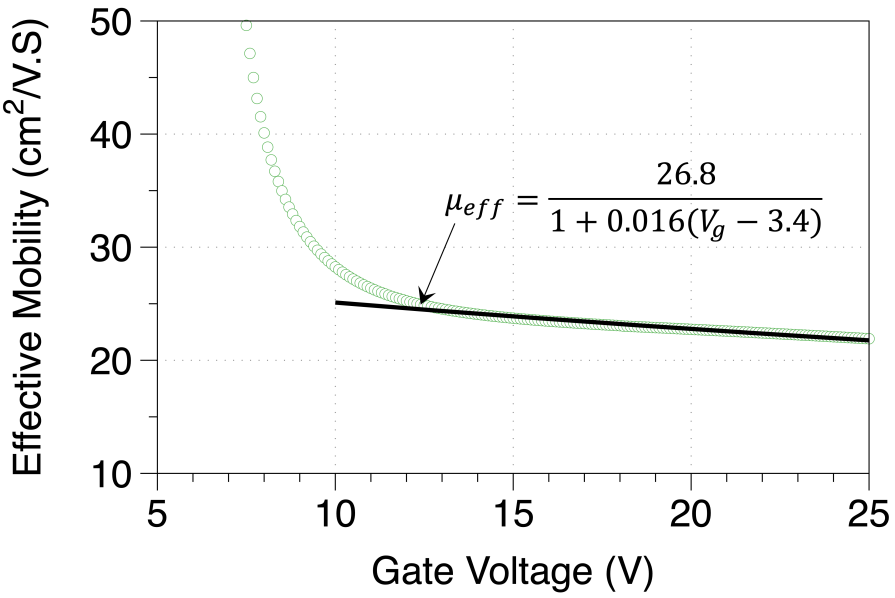


Figure 5.35.: Effective mobility of planar lateral MOSFET calculated a drain voltage of 30 mV.

Where μ_0 is the peak mobility at threshold and θ is the mobility degradation factor. The measured effective mobility at high voltages is fit with the above equation as seen in Figure 5.35. The transconductance is defined as the derivative of the drain current with respect to gate voltage at a constant drain voltage and is given by,

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{5.21}$$

Applying this definition of transconductance to expression for drain current (Equation 5.19), the field-effect mobility is defined as,

$$\mu_{FE} = \frac{L_{CH} g_m}{W C_{OX} V_{DS}} \tag{5.22}$$

The field-effect mobility as a function of gate voltage is plotted in Figure 5.36(a) for multiple devices with different channel length. The effective and field-effect mobilities as a function of gate voltage are plotted in Figure 5.36(b). These values of

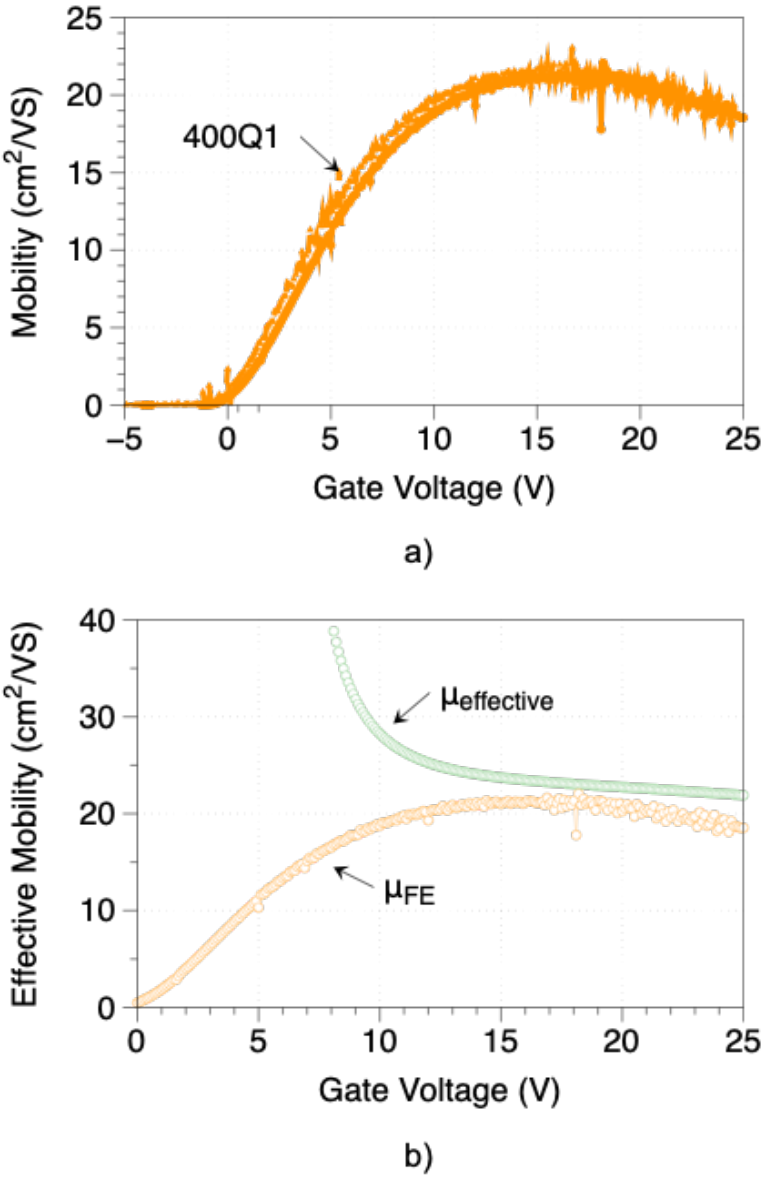


Figure 5.36.: Field-effect and effective mobilities of a planar lateral MOSFETs. a) Field-effect mobility calculated using (5.22) with a drain voltage of 30 mV as a function of gate voltage for two lateral trench MOSFETs on sample 400Q1 with a channel length of 140 µm, b)Comparison of field-effect and effective mobility of one of the two samples from (a). The field effect mobility is lower than effective mobility.

peak mobility are comparable to the carrier mobilties reported in literature for SiC DMOSFETs with NO annealed SiO_2 gate oxide on a P-base with similar doping density as the trigate devices [30]. The determination of the carrier mobility on the trench sidewall and trench bottom is discussed in the next section.

Trench Lateral MOSFETs

Trench lateral MOSFETs are also included in the PCMs, and a schematic of such a device is shown in Figure 5.37.

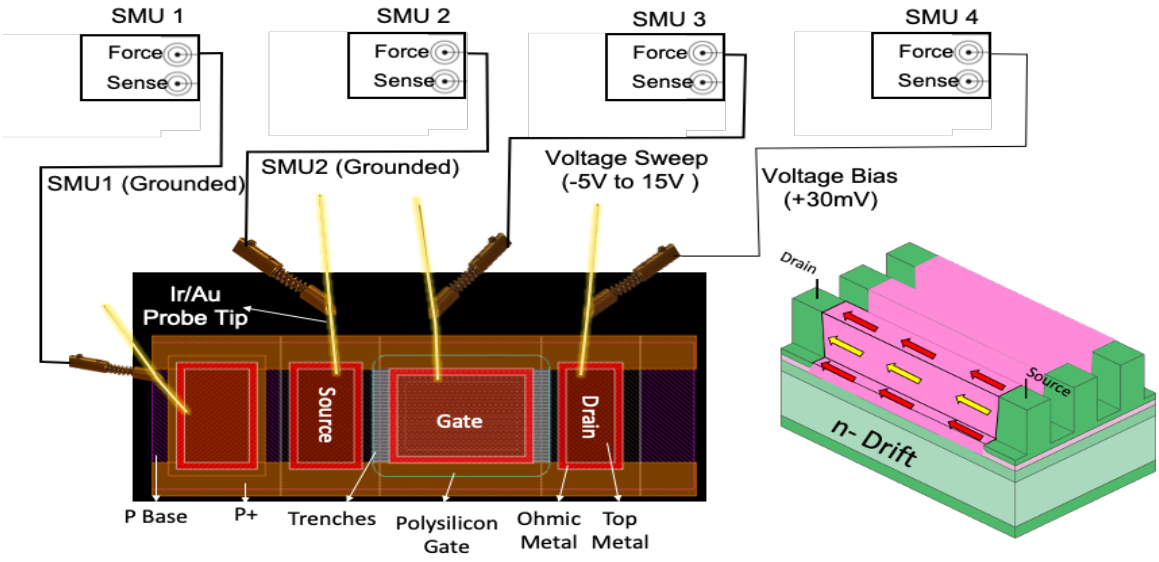


Figure 5.37.: Schematic and current path from source to drain of trench LMOSFET test structure.

The measured drain current in a lateral trench MOSFET would be the sum of the current components from the planar and sidewall channels, and thus is given by (5.23).

$$I_D = \frac{C_{OX} V_{DS}}{L_{CH}} \left[W_{Top} \left(V_G - V_{T1} \right) \mu_{Top} + W_{Bottom} \left(V_G - V_{T2} \right) \mu_{Bottom} + W_{Sidewall} \left(V_G - V_{T3} \right) \mu_{Sidewall} \right] \tag{5.23}$$

where I_D is the measured drain current at a constant drain voltage V_D. μ_{Top}, μ_{Bottom}, $\mu_{Sidewall}$ and V_{T1}, V_{T2} and V_{T3} are the carrier mobilities and threshold voltage of the top, bottom and sidewalls of the trenches in the trigate device. The channel length, L_{CH}, is assumed to be equal on all sides and it has already been established that the oxide thickness is equal on all the faces and therefore C_{OX} which is the oxide capacitance per unit area is also a constant. Lumping the top and bottom surfaces as planar surfaces, (5.23) can be written as

$$I_D = \frac{C_{OX}V_{DS}}{L_{CH}}\left[W_{Planar}\mu_{Planar}\left(V_G - V_{T,Planar}\right) + W_{Sidewall}\mu_{Sidewall}\left(V_G - V_{T,Sidewall}\right)\right] \tag{5.24}$$

Here, μ_{Planar}, $\mu_{Sidewall}$ and $V_{T,Planar}$, $V_{T,Sidewall}$ are the effective mobilities and threshold voltage on the planar and sidewall inversion channels, W_{Planar} is the total planar width and $W_{Sidewall}$ is the total sidewall width. The transconductance is obtained using Equation 5.24 and differentiating the drain current with respect to the gate voltage (V_g).

$$g_m = g_{m,Planar} + g_{m,Sidewall} \tag{5.25}$$

where $g_{m,Planar}$ and $g_{m,Sidewall}$ are the transconductance components of the planar and sidewall respectively which is given by.

$$g_{m,Planar} = \mu_{Planar}\left[C_{OX}\frac{W_{Planar}}{L_{CH}}V_{DS}\right] = \frac{1}{A}\mu_{Planar} \tag{5.26}$$

$$g_{m,Sidewall} = \mu_{Sidewall}\left[C_{OX}\frac{W_{Sidewall}}{L_{CH}}V_{DS}\right] = \frac{1}{B}\mu_{Sidewall}$$

where

$$A = \frac{L_{CH}}{C_{OX}V_{DS}W_{Planar}} \tag{5.27}$$

$$B = \frac{L_{CH}}{C_{OX} V_{DS} W_{sidewall}}$$

Substituting (5.26) into (5.23),

$$g_m = \frac{1}{A}\mu_{Planar} + \frac{1}{B}\mu_{Sidewall} \tag{5.28}$$

Now, multiplying both sides of (5.26) with B and using (5.28),

$$B * g_m = \mu_{Sidewall} + \mu_{Planar}\left(\frac{W_{Planar}}{W_{Sidewall}}\right) \tag{5.29}$$

The units of the left hand side of (5.29) are the same as that of mobility, and therefore if this factor is plotted as a function of various planar to sidewall width ratios $W_{Planar}/W_{Sidewall}$, the y-intercept would be equal to the sidewall mobility, and the slope equal to the planar mobility. As the transconductance was used in the extraction technique, the above mobility values correspond to the field-effect mobility.

Our PCM test structures contain a series of devices with various planar to sidewall width ratios, and can be used to extract the individual mobility components. The total planar width includes the top and bottom widths defined in Figure 5.37, and is given by (5.30). In the mask design, modulation of the planar width is implemented by varying W_{Top} while keeping W_{Bottom} fixed at 0.5 µm. This is done to keep the trench etch depth consistent between the active trigate and the trench lateral MOSFET test devices as the etch rate of the SiC trench etch is width dependent.

$$W_{Planar} = W_{Top} + W_{Bottom} \tag{5.30}$$

Lateral trench MOSFETs with W_{Top} of 0.5 µm, 1 µm, 2 µm, 3 µm and 4 µm are used to modulate the planar to sidewall width ratio, and the analysis is carried out using the procedure described above as seen in Figure 5.38.

The mobility on trench sidewall is found to be ~10 cm^2/Vs, while the planar mobility is found to be 17 cm^2/Vs. In the analysis above, the mobility on the top and bottom surfaces are assumed to be equal and is denoted by μ_{Planar}. However,

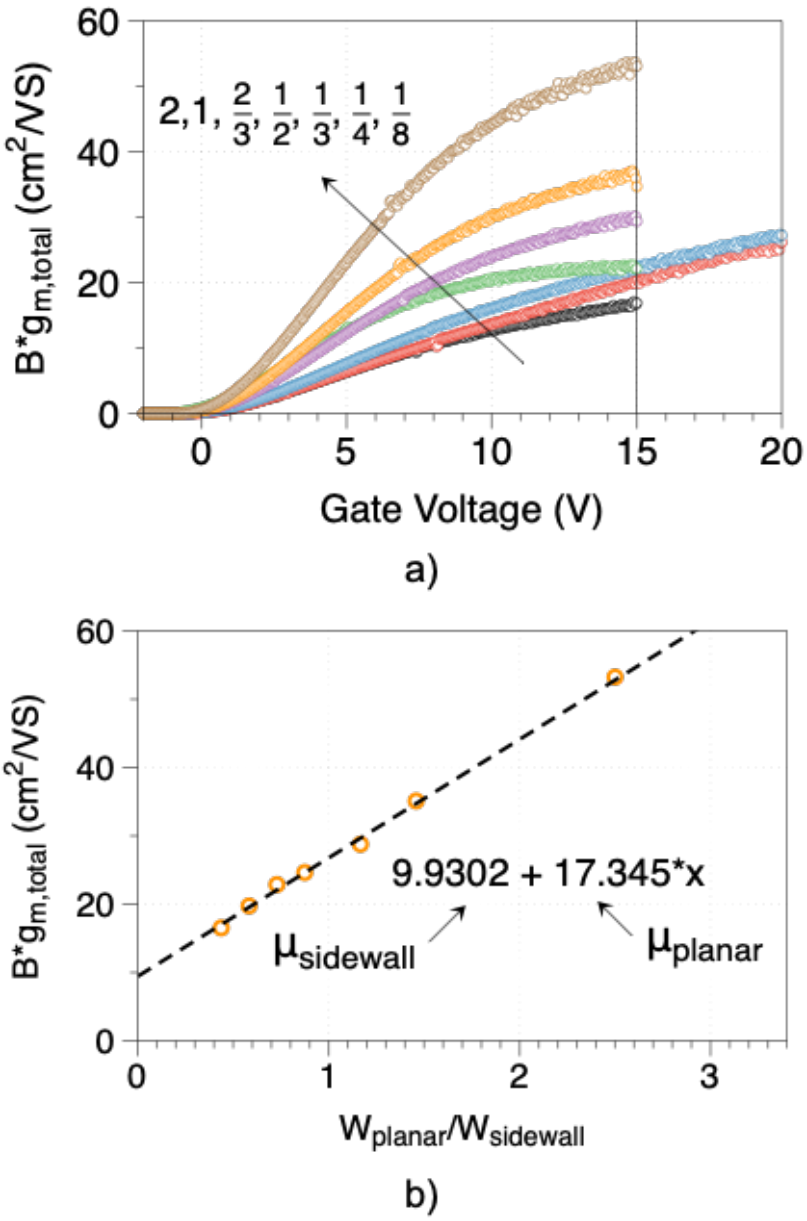


Figure 5.38.: Extraction of sidewall and planar mobilities from various long channel trench MOSFETs. a) The factor $B \times g_m$ (5.29) vs. gate voltage for trench LMOSFETs with different planar to sidewall width ratios, b) Value of $B \times g_m$ corresponding to a gate voltage of 15 V plotted as a function of planar to sidewall width ratio for trench LMOSFETs.

the channel mobility of the bottom surface is likely to be lower than the top surface in the trigate devices as the bottom surface is exposed to the RIE etch process while the top surface is not. Further analysis using a test structure with different trench bottom widths is required to separate out the bottom and top mobility. This study is not included in this thesis. However, an estimate can be obtained by assuming the planar mobility to be the average of the top and bottom surfaces. The mobility on the top surface is independently measured using planar LMOSFET test devices as shown in Figure 5.36(a) to be 21 cm^2/Vs. Now, using the lumped planar mobility is equal to 17 cm^2/Vs as found from the analysis above, the bottom channel mobility is found to be 13 cm^2/Vs.

5.3.5 Interface Trap Density

MOS capacitors on planar and trenched n-CSL and p-base areas are included in the PCM test structures, and can be used to measure interface trap density. Trenches in the MOSCAPs and MOSFETs are formed by an RIE etch, where the sidewall and bottom surfaces of the trench are exposed to the etch while the top surface is protected by a nickel mask. Therefore, the number of electronic defects and their energy distribution is likely different on the planar and sidewall surfaces. This complicates the analysis and determination of the interface trap density using the widely used methods such as high-low, $C - \psi$ or the conductance technique [126].

The measurement of the total number of interface traps across the bandgap (N_{it}) is difficult in SiC from conventional C-V measurements because of the extremely low thermal generation rate of minority carriers. In addition, interface traps deep in the bandgap are not in equilibrium with the applied DC voltage on the gate, and therefore cannot be detected by the C-V measurements. Therefore, an alternate source of minority carriers is required to measure N_{it}, and this can be done by using the room temperature photo C-V technique or the gate-controlled diode test structure. In the photo C-V technique, minority carriers are photo-generated by ultra-violet light.

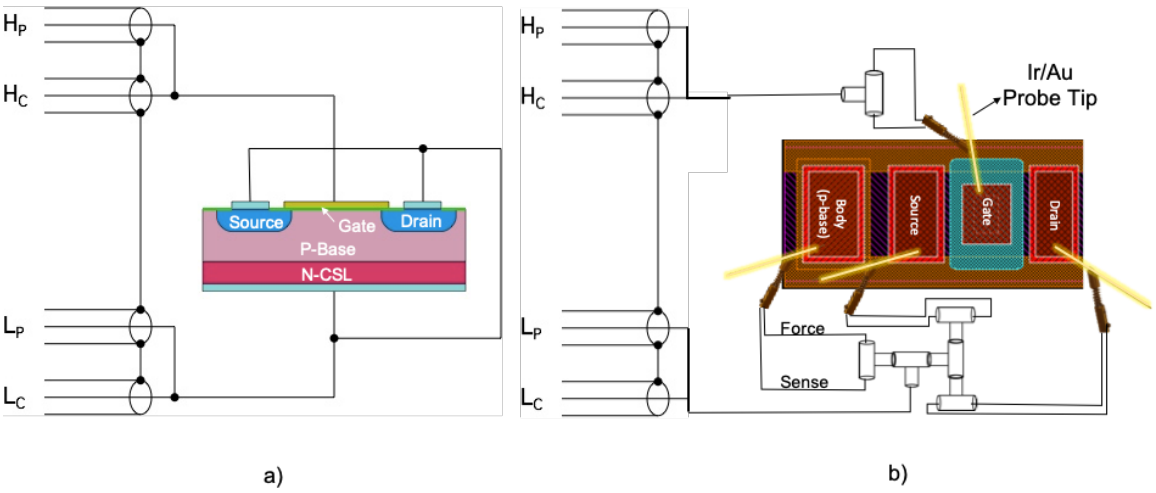


Figure 5.39.: Measurement of interface trap using gate-controlled diode (GCD). a) Terminal connections for a lateral planar MOSFET used as a GCD for C-V measurements. b) Layout schematic and wiring diagram for GCD C-V measurments.

However, it is difficult to introduce light onto the SiC substrate below the thick opaque top metal, and therefore the gate-controlled diode (GCD) technique is used to measure the N_{it}. Another advantage of using this method is that interface trap density, oxide capacitance and channel mobility measurements can all be done on the same device.

The GCD measurement is done using both planar and trench lateral MOSFETs where the source and drain are connected to the grounded substrate, and the gate voltage is swept. The wiring configuration for the GCD measurement on a planar lateral MOSFET is shown in Figure 5.39. When the gate voltage is sufficiently high, electrons are injected across the N+ source/drain and P-substrate junctions, and an inversion layer is formed underneath the gate oxide.

The gate capacitance vs. gate voltage (C-V) characteristic from the GCD measurement of the above MOSFET is shown in Figure 5.40. The gate voltage is swept from negative -18 V (accumulation) to +5 V (inversion) with a small signal voltage

of 20 mV and frequency of 1 kHz. First, the gate voltage is held at -18V in accumulation at point A for 5 seconds, and it is assumed that all the interface states below the Fermi level are filled with electrons, the traps above are empty, and the device is in equilibrium. Now the gate voltage is swept positive towards point C and the characteristics are similar to a conventional low frequency C-V measurement in SiC as will be explained below. The interface states that are now pushed below the Fermi level remain empty as there are no thermally generated electrons to capture during the duration of the sweep.

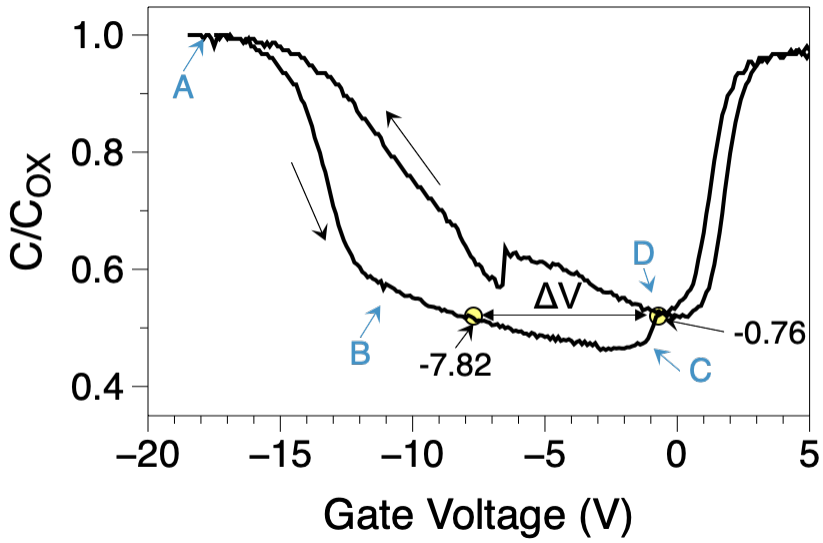


Figure 5.40.: Gate capacitance vs gate voltage charectaristics for a GCD connected planar lateral MOSFET using the schematic shown in Figure.5.39. The measurement is done at 1 kHz with a small signal voltage of 20 mV and the sweep direction is indicated in the figure by the black arrows.

Though the surface potential under the gate at point B ($2\psi_B$) is sufficient to allow electron injection from the overlapping n+ source/drain regions, the low frequency inversion characteristics do not appear. This is due to interface trapping that inhibits the inflow of minority carriers from the n+ regions to the surface under the gate. The electrons coming in from the adjacent n+ region are trapped in surface states at

the edge of the gate, and the corresponding negative charge in the interface states prevents the surface potential from rising above $2\psi_B$. These traps act like a barrier to electrons between the center of the gate and the n+ region. Therefore, without available minority carriers, the depletion region under the gate continues to increase to support the gate voltage between points B and C in Figure 5.40, and the device is in deep depletion. Now at point C, all the interface states at the gate edge and energetically below the Fermi level are filled, and the gate voltage is sufficient to lower the local potential barrier. Minority electrons from the n+ region now flood the surface under the gate driving the device into inversion. This causes the capacitance to increase from point C to the equilibrium value at point D, and the characteristic 'hook' is seen. This was first observed and explained by Goetzberger *et al.* [127].

As described above, additional gate voltage from point B to point D in Figure 5.40 is required to fill all the interface states and form a stable inversion layer at the gate edge. Therefore, the consequent change in voltage from point B to C, and then finally to point D is directly proportional to the total interface state density given by Equation 5.31 below.

$$N_{IT} = (\Delta V \times C_{OX})/q \tag{5.31}$$

Here, N_{IT} referes to interface states located energetically between $\psi_s \sim 0$ (flat-band) and $\psi_s = 2\psi_B$. Some of the interface states very close to the valence band edge are able come into equilibrium by hole emission, and cannot be accounted for in this measurement.

For the planar MOSFET shown in Figure 5.40, N_{IT} is calculated to be 2.3×10^{12} cm^{-2}. The C-V measurement was repeated on trench lateral MOSFETs with different sidewall areas as shown in Figure 5.41. The voltage shift, minimum capacitance and N_{IT} are calculated for the different trench MOSFETs from Figure 5.41. The calculated total interface trap density N_{IT} of the trench MOSFETs is plotted as a function of sidewall area in Figure 5.42, and a linear increase in interface trap density with sidewall area is observed. A higher density of interface traps on the sidewalls could be due to defects introduced during the RIE etch process.

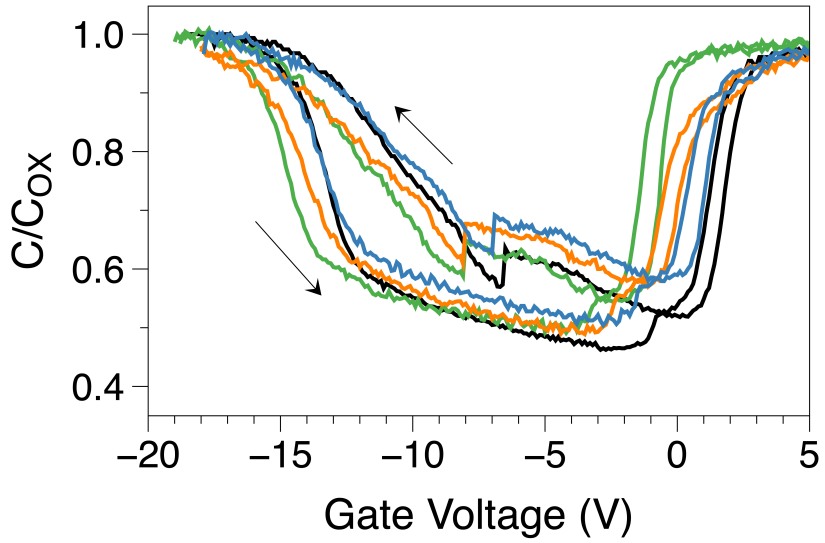


Figure 5.41.: Gate capacitance vs. gate voltage characteristics for GCD connected planar trench MOSFETs with different sidewall areas. The measurement is done at 1 kHz with a small signal voltage of 20 mV and the sweep direction is indicated in the figure by the black arrows.

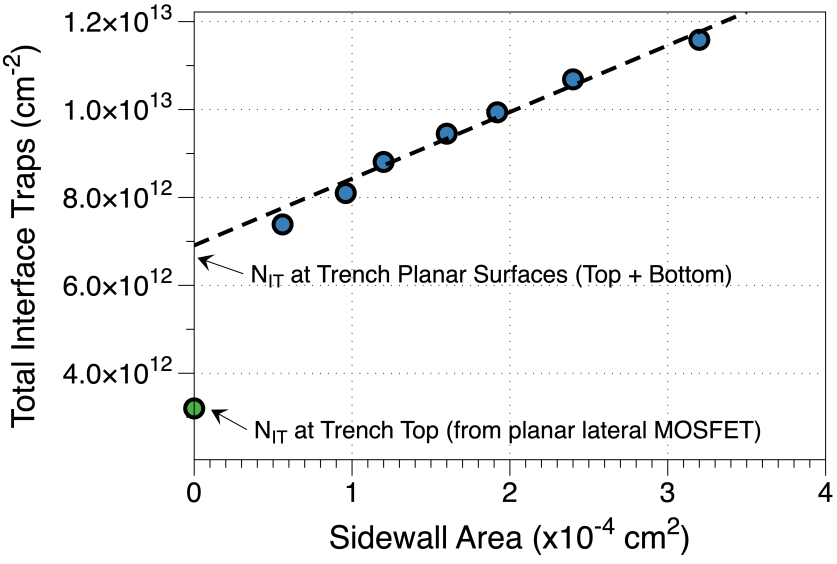


Figure 5.42.: Measured total interface trap density for trench MOSFETs with different sidewall areas. The total area of the planar surfaces (trench top + bottom) is kept constant in all the devices.

6. FUTURE WORK

Process development, integration and evaluation of the vertical trigate DMOSFET has been described in this thesis. While the results from the initial demonstration run presented here show tremendous potential for the trigate DMOSFET, further optimization and development is required for wide scale adoption and manufacturability of this device. Recommendations for future work derived from the learning from the completed trigate process runs are presented in this chapter and organized as follows:

1. Performance Improvement
    (a) Design Modification: Increase in channel length
    (b) Process Modification
        i. Waffle substrate integration
        ii. Alternate gate oxide
2. Yield Improvement
    (a) Design Modifications
        i. Elimination of polysilicon posts in implant masks
        ii. Additional edge termination testers
        iii. Reduced-area devices
    (b) Process Modification
        i. Field Oxide
        ii. Conversion from metal to oxide mask
        iii. Deposited sidewall spacer as an alternative to oxidized polysilicon in the self-aligned channel process

6.0.1 Increase in channel length

The trigate devices in Gen-1 and Gen-2 have a nominal channel length of 0.5 µm that is defined by the sidewall oxidation of the polysilicon base implant mask prior to the source implantation, and is therefore self-aligned to the base. However, a significant deviation from the drawn or expected dimensions has been noticed in the samples from the initial trigate run. As described in Section 4.1.1.1, the trigate device requires high energy ion implants and therefore it necessitates a thick film polysilicon implant mask with a high aspect ratio. Therefore, the shape and distribution of the ensuing base and source implants is very sensitive to variability in the ion implantation process parameters. A slight deviation from normal incidence in the ion beam could lead to a significant shadowing effect. Numerical simulation of the implant using the Monte Carlo method was done using Sentaurus Process to study the effect of tilt variability in the incidence angle of the ion implantation beam to the subsequent p-base and source regions in the sample. A detailed description and discussion of the results is presented in my colleague Naeem Islam's thesis [101]. Significant implantation shadowing due to the high aspect ratio mask is observed with the incident angle of the aluminum beam normal to the SiC surface during the p-base implantation and a tilt of between 2° and 5° from the normal in the nitrogen ion beam during the source implantation.

The secondary electron potential contrast technique described earlier in Section 4.2.3 was used to visualize the channel region. A cross-section SEM image perpendicular to the gate stripe for Gen-1 sample 2Q4 is shown in Figure 6.1(a) where the P-type areas appear as bright regions, while N-type areas appear as darker gray. The left-side channel appears shorter than the right-side channel, which could result from shadowing of a tilted source implant ion beam with the same conditions used above. Another feature of the implant visible in the figure is the variation of channel length with depth. It appears that the channel length at the top is lower than the bottom. This was anticipated even in our simple analytical model of the implant discussed in

Section 4.1.1.1. The straggle of N increases slower with energy, so the channel length was expected to increase with depth.

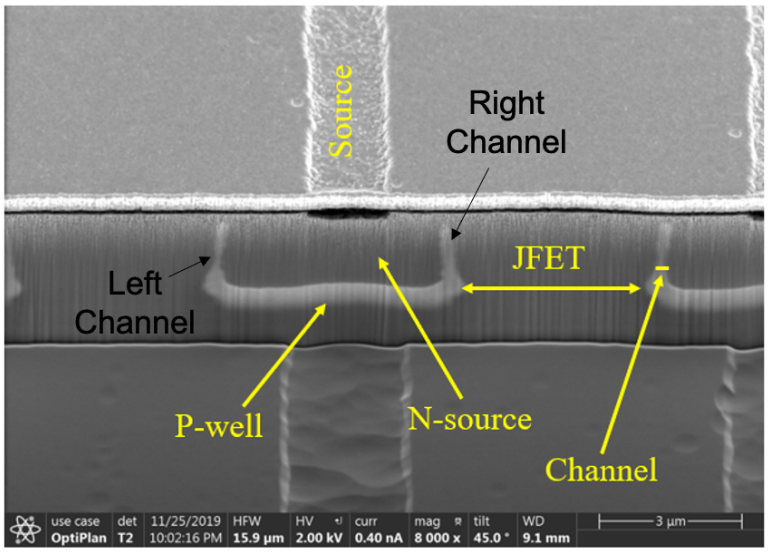


Figure 6.1.: Channel length visualization using cross-section secondary electron potential contrast images obtained using the SEM under the gate electrode. The P-type areas appear bright and the N-type areas appear dark. The P-type area until the depth of the trench (2 µm) is the channel in the trigate device.The channel at the surface cannot be visualized accurately by this technique due to surface depletion and other effects.

Further evidence of a short channel was observed in the output characteristics of the fabricated devices 1Q3 and 400Q1. Effects such as enhanced drain induced barrier lowering (DIBL), degradation of the sub threshold slope and in some extreme cases a punch-through as illustrated in Figure 6.2

The channel length can be increased without any change to the current design by oxidizing for a longer time after the base implant. For example, to increase the channel length by 0.25 µm, the oxidation time is increased by about 2 hours and 13 minutes. However, the increase in channel length with the minimum required gate source overlap is accompanied by a reduction in the source contact length. The most

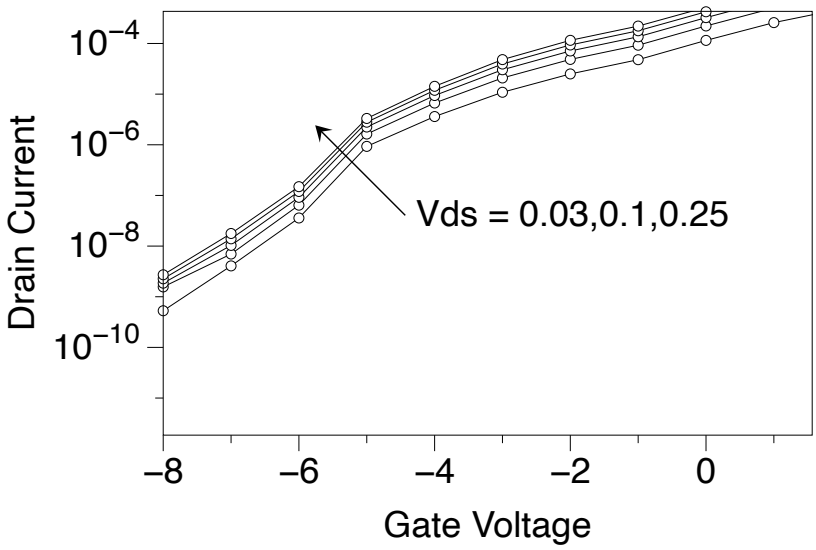


Figure 6.2.: Drain induced barrier lowering observed in trigate MOSFETs on sample 400Q1. Degradation of the subthreshold slope and increase in the subthreshold current with the increase in drain voltage is observed.

aggressive contact length in the current design is 1 µm while the measured transfer length underneath the source contact is between 0.5 µm and 0.8 µm in the current ohmic process, and further reduction in the source length is not ideal. Therefore, a design change to reduce the JFET widths by 0.25 µm on each side in all device variations is necessary to enable an increase in channel length without reducing the source contact area or increasing the cell pitch.

Numerical simulations were carried out to study the effect of JFET width reduction on the figure of merit. A reduction of JFET width increases the spreading resistance in the JFET region, and therefore could potentially lower the figure of merit (FOM) defined in Section 3.4. Figure 6.3 shows the figure of merit as a function of JFET width for a Gen-2 trigate device with a trench depth of 1 µm, CSL thickness of 1.6 µm, JFET doping of 1×10^{17} cm^{-3}, and the sidewall carrier mobility is assumed to be equal to the planar mobility. The analysis is similar to that carried out in Section 3.4 with modified JFET width. As seen in the figure, apart from a 15% reduction in

the FOM for the shortest JFET width, the FOM is largely unchanged by reducing the JFET width a total of 0.5 µm and justifies the proposed design change.

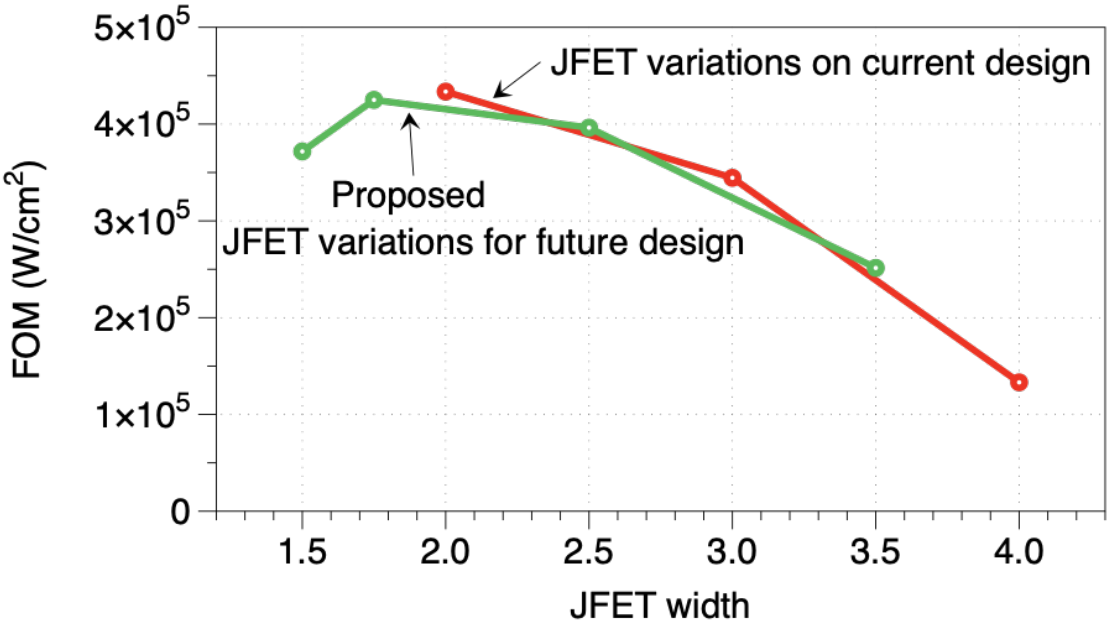


Figure 6.3.: Figure of merit comparison between the current JFET width variation and the proposed reduction in the JFET width to accommodate an increased channel length without reducing the total cell pitch.

6.0.2 Substrate resistance reduction using a waffle substrate

The primary performance advantage of the trigate DMOSFET is the reduction of the specific channel resistance as compared to the planar DMOSFET. As discussed in Section3.2.1, a reduction in channel resistance consequently reduces the total specific on-resistance, and is most effective for devices rated for blocking voltages between 400 V-900 V. However, in this regime, the substrate resistance is a major contributor to the total specific on resistance, and must be reduced to fully realize the benefit of the reduced specific channel resistance.

One way to reduce the substrate resistance is to mechanically thin the substrate, and this is currently employed in the most advanced production devices [128]. However, back-grinding can introduce surface damage such as scratches, dislocations, and cracks that reduce the mechanical strength of the wafer. In addition, wafer warp and bow may be exacerbated on thinned wafers during subsequent processing. Back-side polishing restores some of the intrinsic strength by reducing the concentration of surface defects [129], but the reduced mechanical strength can pose challenges during fabrication. Thinning is therefore carried out after most front-side processing is done, to minimize the chance of breakage.

An alternative and more effective method of reducing the substrate resistance is the adoption of a waffle substrate [130]. Here, deep depressions are etched in a repeating or "waffle" pattern on the back side of the substrate. The waffle structure provides mechanical support while reducing the effective electrical thickness of the substrate. To estimate the reduction of the substrate resistance by the waffle substrate, assume a substrate of thickness t_1 and resistivity ρ, and consider a square area having side length $d_1 \times d_1$. Now an anisotropic etch is performed in a square subsection of the area with side length $d_2 < d_1$, leaving thickness $t_2 << t_1$ remaining as shown in the inset to Figure 6.4. A conservative upper bound on the specific resistance of the $d_1 \times d_1$ region can be obtained by neglecting conduction in the unetched fins and assuming conduction only occurs through the thinned depressions [130].

This relationship is plotted in Figure 6.4, for a nominal substrate resistivity of 25 mΩ cm. The specific substrate resistance of a uniformly thinned substrate to 110 µm is also shown for comparison. For a d_2/d_1 ratio of 0.8 with the substrate etched to a final thickness t_2 of 20 µm, the resistance reduction factor with respect to the thinned wafer is 3.5×. Therefore the waffle substrate has a huge benefit when integrated with the trigate device.

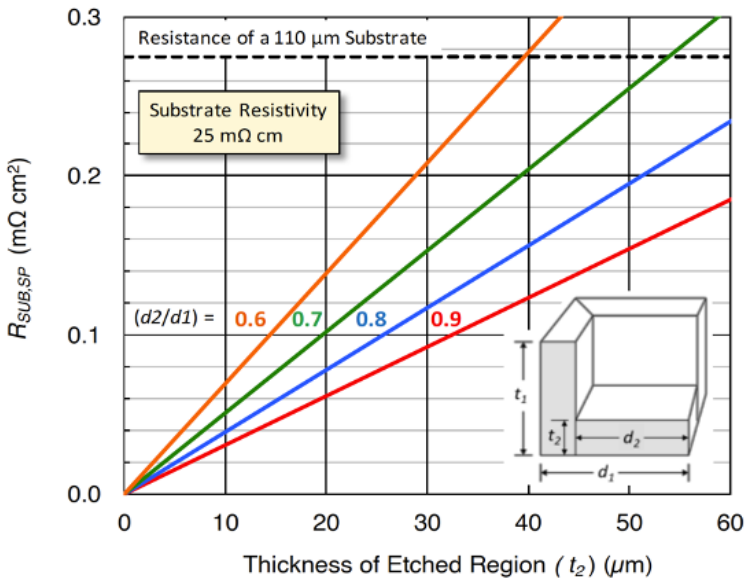


Figure 6.4.: Specific resistance of a waffle substrate assuming no conduction in the unetched fins. The specific resistance of an unetched substrate of thickness 110 µm and $t_1 = 200$ µm is shown dashed.

Waffle substrate integration plan

The waffle-etch process uses standard contact photolithography, metal mask deposition, and inductively coupled plasma (ICP) etching of the wafer backside. The trigate devices are fabricated on the front side of the wafer and once the top metal deposition is complete, the front side can be covered with photoresist to protect the devices and the waffle substrate process is applied to the backside. Figure 6.5 illustrates the integration of the waffle substrate process to the current trigate process.

Process Development

The waffle substrate process development has been carried out by Dr. Noah Opondo. The waffle pattern is formed by an anisotropic RIE process to etch the SiC substrate using a patterned Ni mask. A thick Ni mask required to block the deep

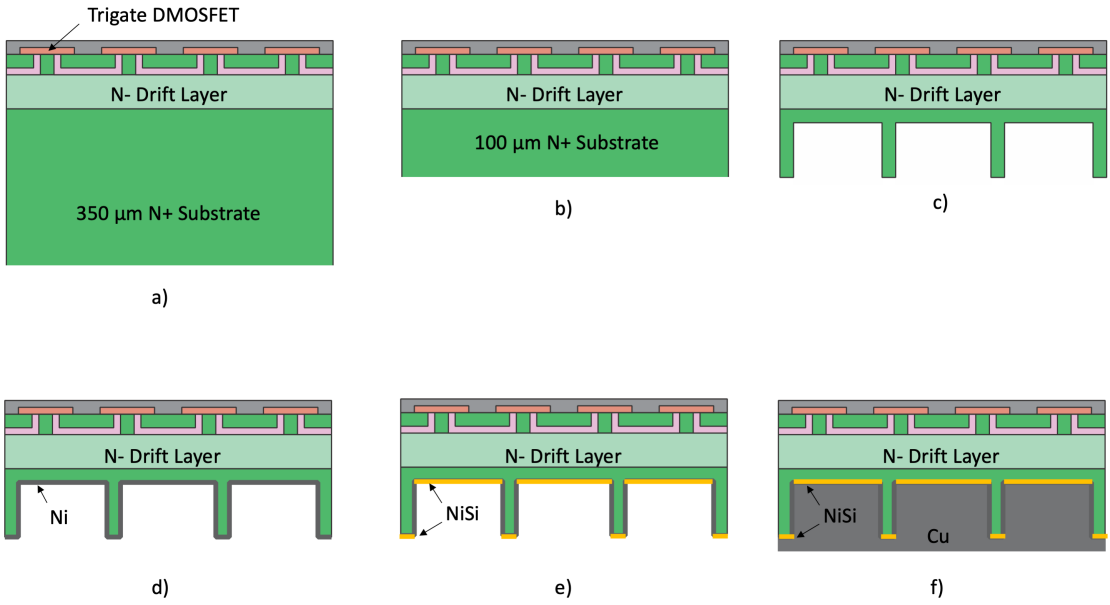


Figure 6.5.: Integration plan of the waffle substrate process to the trigate devices. a) Completion of all front side processing including top metal, b) Thinning substrate to ∼100 µm, c) Waffle pattern etch using RIE, d) Sputtered nickel on backside for ohmic contact, e) Laser anneal to form nickel-silicide for the drain contact, f) Backside planarization using electroplated copper.

SiC etch is formed by using a custom built Ni electroplating setup. Etched waffle structures with square patterns are shown in Figure 6.6.

After the waffle pattern is completed, the back of the thinned sections of the wafer will be within $20 - 30$ µm of the front surface of the wafer. In production versions of these devices, aluminum might be used for top metal, which melts at $660°C$, and polyimide or similar polymer-based encapsulants might be present. Both would preclude the $1000°C$ anneal required to create a low resistance NiSi ohmic contact. In addition, the waffle structure might not survive the mechanical stress such rapid thermal cycling would impose. Therefore, laser annealing, which is already used in industry to form backside ohmic contacts on thinned wafers, is an ideal candidate for performing the required waffle substrate contact anneal.

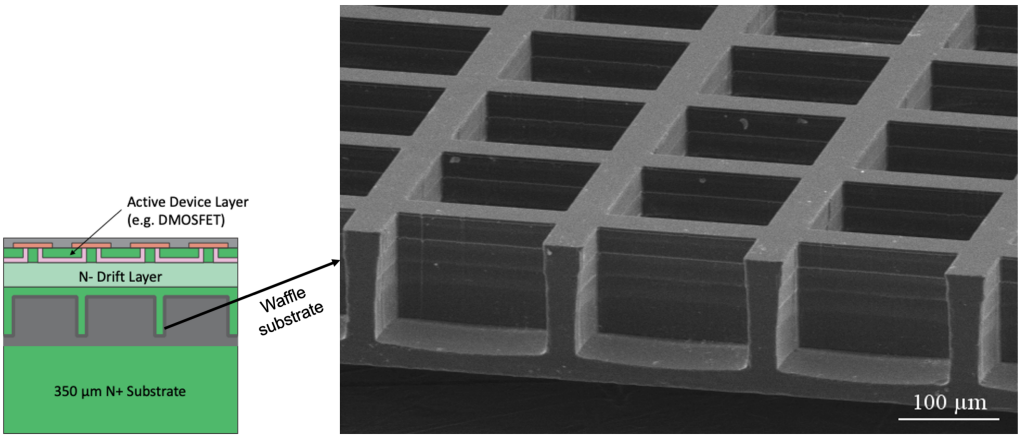
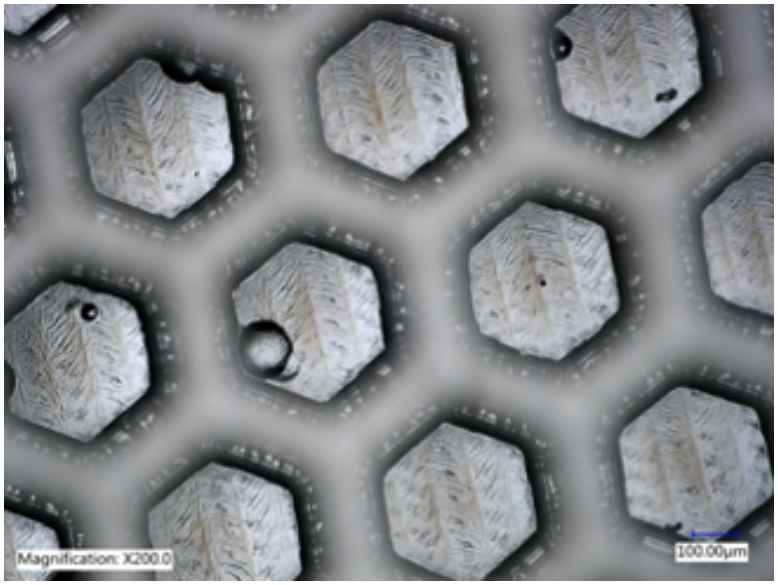
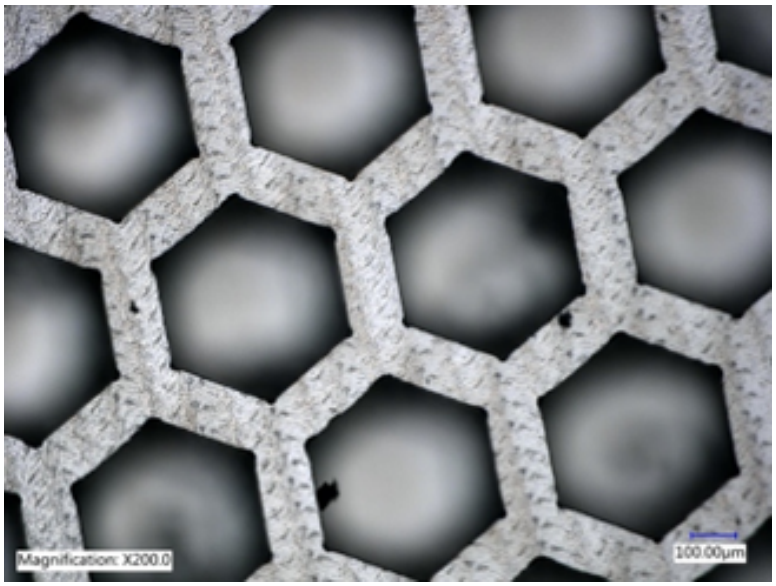


Figure 6.6.: 180 µm waffle pattern etched in a 4 inch SiC wafer with active devices(schotkey diodes) in the front side.

An initial experiment to develop and verify the ohmic anneal with the waffle pattern and laser anneal has been done in collaboration with Fraunhofer Institute in Erlangen, Germany. Two samples were prepared at Purdue University. One sample was waffle-etched and nickel sputtered over the etched surface. The second had nickel deposited on the front surface in a TLM test structure pattern. These samples were laser anneal together at Fraunhofer Institute and optical images of the results, focused both on the bottom and top surfaces of the waffle etched side of the wafer are shown in Figures 6.7(a) and 6.7(b). These images were taken after a piranha (H_2SO_4 : H_2O_2) etch, which would have removed any remaining elemental nickel. The laser raster paths are clearly visible on both surfaces. Electrical measurements were the performed at Purdue University and the result from the TLM structure is shown in Figure 6.8. A low specific contact resistance of $3.5 \times 10^{-6}\ \Omega cm^2$ is obtained from the laser anneal nickel silicide process and is comparable to the standard thermal RTA anneal process discussed in Section 4.2.3.



(a)



(b)

Figure 6.7.: Optical microscope images of a laser-annealed, nickel-coated waffle substrate: (a) Bottom focused (b) Top focused

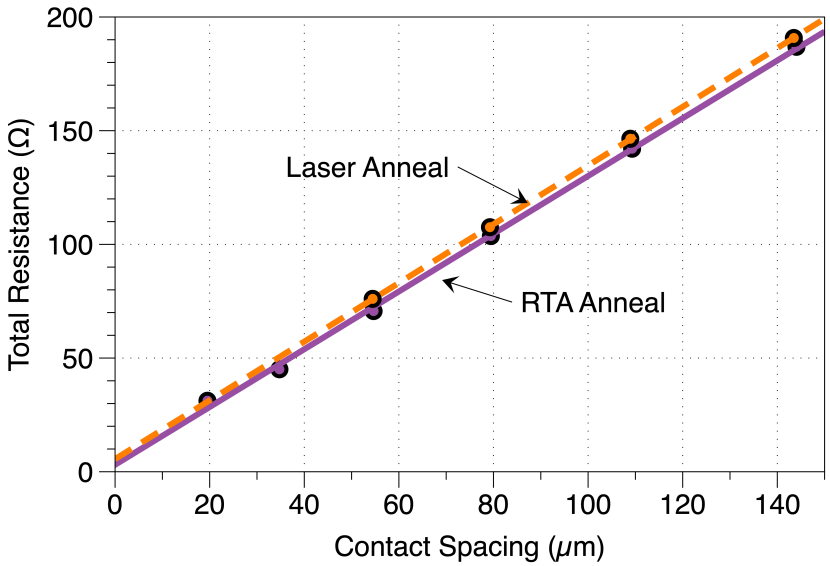


Figure 6.8.: TLM data – laser annealed vs. RTA annealed nickel silicide ohmic contacts

The expected improvement in the on-resistance of the trigate DMOSFETs on sample 400Q1 with the waffle substrate is shown in Figure 6.9. Clearly a significant improvement is possible. The waffle etch process has been developed and the laser anneal process has also been tested on a waffle etched sample. Therefore, the next step is to apply the waffle substrate structure to the trigate devices.

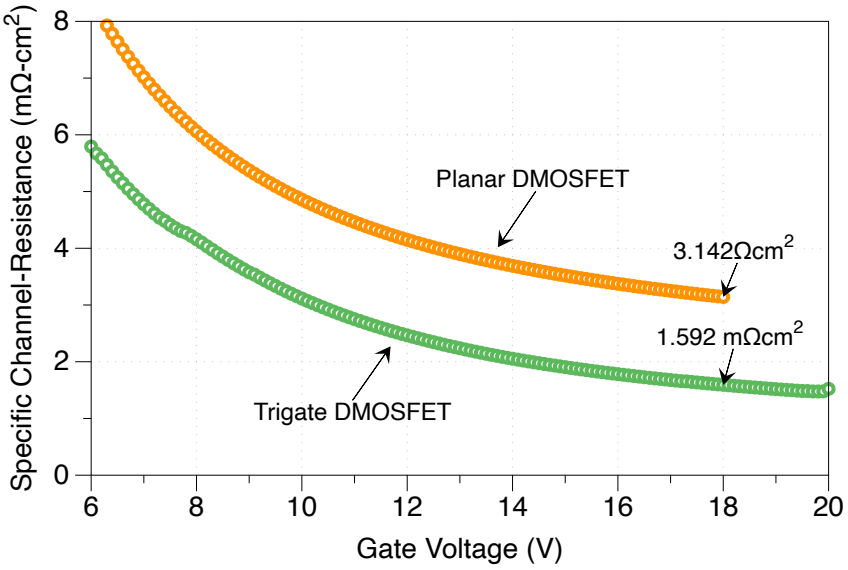


Figure 6.9.: Expected specific on resistance of sample Gen-2 400Q1 after integrating the waffle substrate with $t_2 = 20$ µm and $d_2/d_1 = 0.2$.

6.1 Yield Improvement

A number of problems pertaining to yield were encountered in the demonstration run of the trigate MOSFET. The sample with the highest number of working devices is the Gen-2 sample 400Q1, where the yield was about 50%. A number of changes to the design and process to improve the yield of trigate devices in the next run by improving the design, as well as process changes are described below.

6.1.1 Elimination of p+ contact polysilicon post

As described in Section 4.2.3, an unexpected failure mode in the fabrication process was identified that significantly impacted the yield due to a source-drain short. In the current mask design, the p+ contact to the source is made in the active area by blocking all the high energy implants prior to the p+ implant using a post of polysilicon. The layout of these posts is shown in yellow in Figure **6.10**. These polysilicon posts are apparently mechanically unstable, as they are high aspect ratio, unsup-

ported features and are susceptible to being uprooted in the consequent processing steps. This problem can be solved in the new mask set by a modification of the p-well implant mask as shown in Figure 6.10. The posts can be replaced by an interconnected cross-hatch pattern, providing the mechanical integrity lacking in the current design.

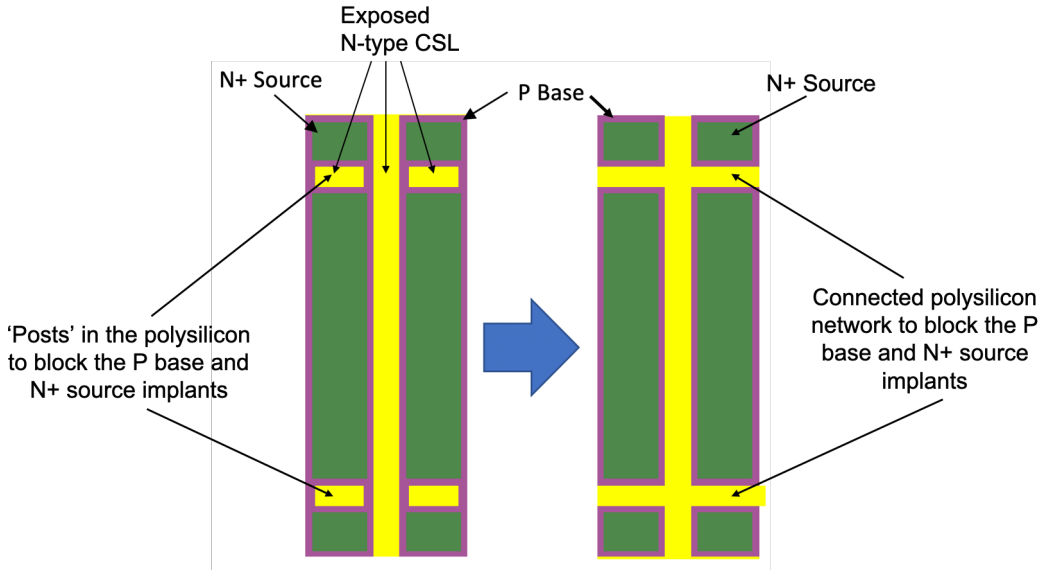


Figure 6.10.: Proposed mask change to eliminate the "missing post" defect in future devices.

Figure 6.11(a) shows an overview of the current mask set for a single device, without the edge termination rings and top metal layer. The implementation of the proposed design change in the area highlighted in Figure 6.11(b) is expanded in Figure 6.11(c). The white regions in the figure are where the polysilicon implant mask blocks both the p-well and n+ source implants. The channel regions where the p-well implant is not blocked but the n+ source implant is blocked, are shown in pink. The p+ implant regions are shown overlaid in orange. In the original design in Figure 6.11(c), polysilicon posts (white features) located at the intersections of the source and p+ implant stripes exposed a p-well region at the surface that would receive the p+ implant to form p-well contacts.

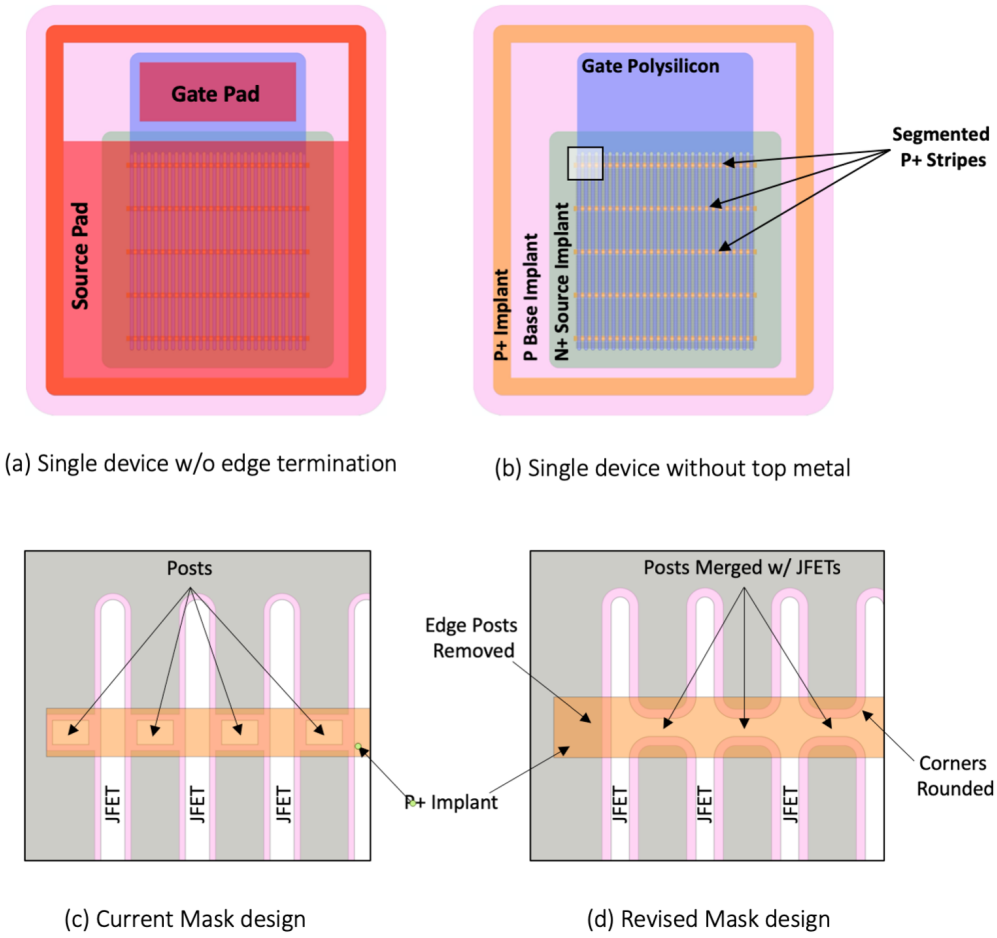


Figure 6.11.: Proposed mask change to eliminate the "missing post" defect in future devices. a) Current design on the trigate mask layout, b) Proposed layout change in the P-base implant mask.

The problem arose when some of these posts broke off between the p-well and n+ source implants, allowing an n+ implant in this area that formed a direct short between the source metal and the underlying n- drift region, creating a source-drain short. The solution is illustrated in Figure 6.11(d), where the posts are replaced by continuous horizontal stripes that merge with the vertical JFET stripes. This should provide the mechanical support to eliminate the missing post problem. To further increase the mechanical robustness of the structure, the corners where these stripes

intersect have been rounded. To accommodate the space required by the rounded corners, the p+ stripes have been widened, and one trench on either side of these stripes has been removed. This reduces a total of 10 trenches which only reduces the total area by 6%.

6.1.2 Addition of edge-termination testers

In the original mask design, the only structures with edge termination were planar and trigate MOSFETs. To measure the blocking voltage independently, simple edge termination test diodes can be added to the mask design. This test device can also be used to compare leakage characteristics of trigate MOSFETs to diodes that lack trench corners in the active area, since these could lead to field crowding and enhanced leakage. The proposed diode structure is illustrated in Figure 6.12, and consists of a simple p-well implant and a floating-field ring edge-termination structure identical to the trigate device. A p+ implant and ohmic contact form the anode, while the substrate forms the cathode. The active area is approximately $1.5 \times 10^{-3}\ cm^2$.

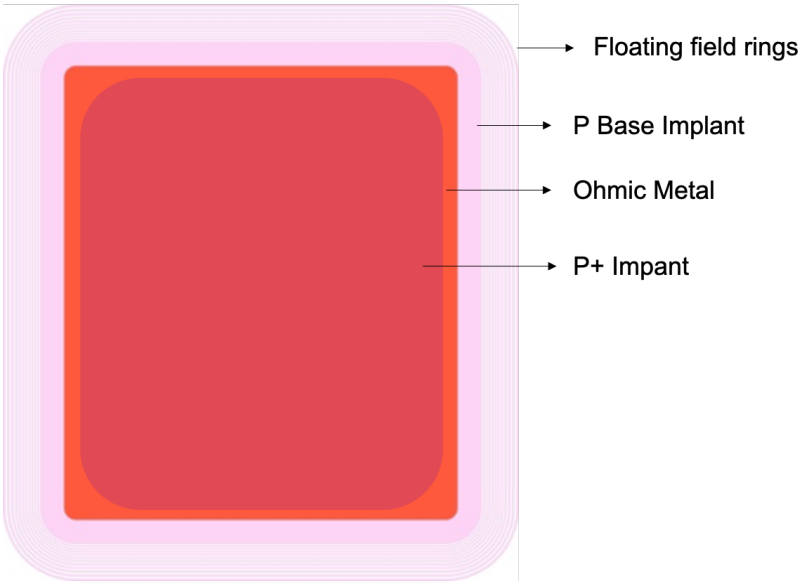


Figure 6.12.: Edge termination test device

6.1.3 Reduced area devices

To increase the likelihood of finding functional devices, two additional designs can be added to the mask set. These devices are illustrated in Figure 6.13. The devices are trigate MOSFETs with a conservative design, reduced area and have features that are intended to only check the functionality of the MOSFET in the on and off-state. The devices are not optimized nor intended to have the best performance. For example, neither of the designs include internal p+ contacts as an added precaution to eliminate any probability of source to drain short through the body contact in the active area. This would compromise the dynamic performance of the device, such as switching speed, but would not have any effect on basic functionality and have negligible impact on the static characteristics of the device. In addition, the source contact area is increased by removing every other trench. For comparison, the standard-size devices that comprise the majority of the mask set have an active area of approximately 180 µm × 200 µm, while the proposed reduced area devices have an area of 70 µm × 70 µm.

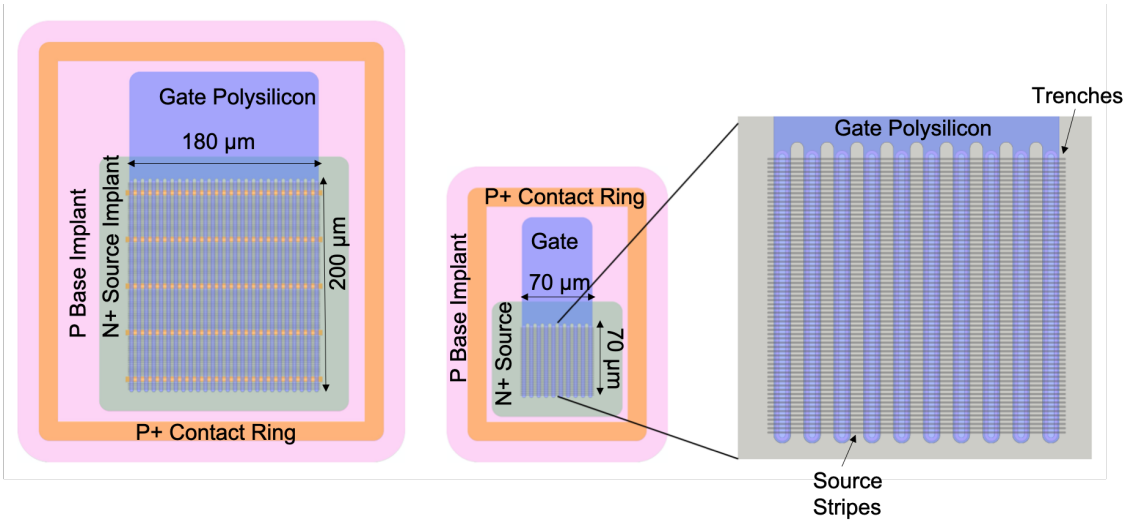


Figure 6.13.: Layout of reduced area devices.

6.1.4 Field Oxide

The wafer on which the devices were fabricated can be broadly classified into two categories i) active area, and ii) field area. The location on the sample where trigate devices and accompanying test structures such as planar MOSFETs, diodes, MOS capacitors are fabricated is termed as active area while the remaining area on the sample is the field area. For example, space between adjacent devices or die, and area allocated for alignment marks lie within the field area.

It is important to protect the field area from contamination or moisture that could potentially be sources of charge on the semiconductor surface. Such a surface charge is undesirable as it could significantly influence the electrical properties of the underlying material.For instance, positive surface charge could be present over the floating field rings, either on top of a thin native oxide or the SiC surface itself. As there is no metal or field plate over the field area, these charges are forced to image onto negative charges in the underlying SiC layer which in this case is the depletion region of the p-region or accumulated electrons in the n-epilayer that are part of the floating field ring. This could impact the electric field distribution under the floating field rings in reverse bias and cause premature breakdown of the device.

Another effect of surface charges is the possibility of surface inversion where a sheet charge at the SiC surface could be induced in the entire field area up to the edge of the wafer. This could cause an electrical short between the source and drain of the MOSFETs through the edge of the wafer.

To mitigate some of the problems mentioned above, the field area in the sample is generally protected by a thick field oxide. Typical thickness of a field oxide employed in SiC MOSFETs is $\sim$1 µm [58,108]. However, the field oxide thickness in the current devices is equal to the gate oxide thickness as it is formed during the same step in the process. This is due to a fabrication complexity caused by the presence of the deep trenches as described below.

Current Process

In the current process, the field oxide is grown using the poly-ox process. To achieve a thick film of oxide, multiple cycles of polysilicon deposition and oxidation is carried out. First, a 75 nm thick film of polysilicon is grown using LPCVD. The deposited film does not seal the trenches which are 0.5 um wide. The polysilicon film is then oxidized at 1100°C in a wet pyrogenic chamber to get a 150 nm oxide film and is followed by a NO anneal for 2 hours at 1175°C to passivate the oxide-SiC interface. This oxide growth process is then repeated twice in order to get a $\sim$ 1 µm thick oxide layer. The NO anneal is only performed after the first oxidation step. Though the above procedure can be used to achieve a high quality field oxide, there are two problems in its application. The problems encountered and the proposed solution to each of the problem is described below.

Problem 1: Difficulty in removing the oxide from the active area

Once the thick oxide is formed, it needs to be selectively removed from the active area. Photoresist is usually used as a mask to protect the oxide over the field area and then a wet etch is used to etch the oxide. This process is not trivial, as a much thicker field oxide is formed over the high aspect ratio trench feature. For example, an oxide thickness of 1 µm over the field area forms a 3 µm thick oxide layer on the 2 µm deep trench pattern as shown in Figure 6.14. To wet etch the oxide, a 40 min soak in a BOE solution is required at the nominal etch rate of $\sim$ 80 nm/min. Though the photoresist has a high selectivity during this, we observed a serious problem of poor adhesion to the surface. This allows the etchant to enter underneath the resist and causes significant undercut. The photoresist mask eventually peels off as illustrated in Figure 6.14. The problem of adhesion can be mitigated by using an adhesion promoter such as HMDS which is evaporated onto the film using a desiccator. However, the long wet etch causes significant undercut of the oxide film itself and leads to problems of mask adhesion.

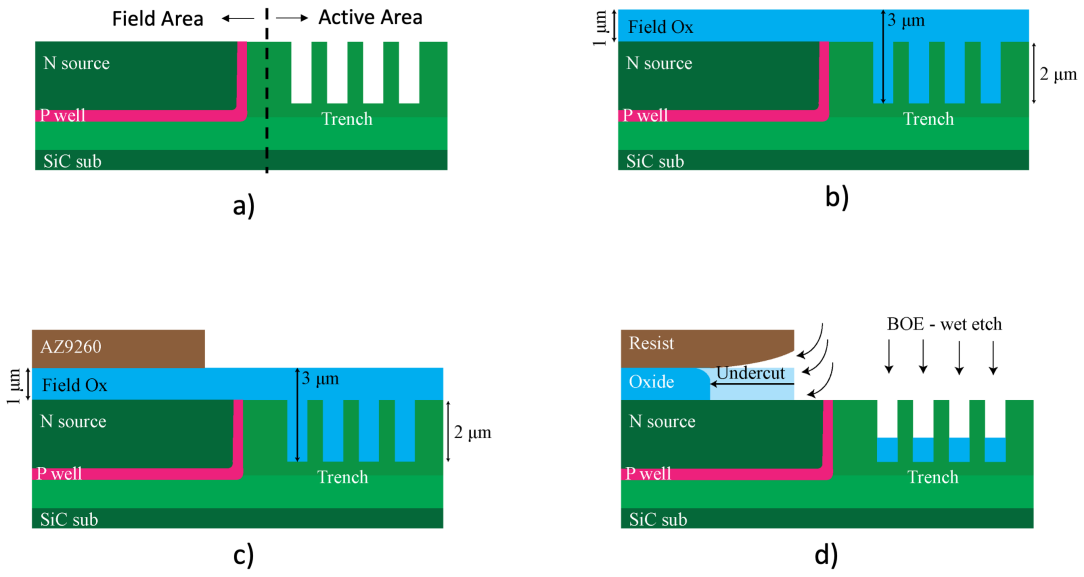


Figure 6.14.: Field oxide in the current process flow. a) Trenches etched in active area either with or without H_2 etch., b) Field oxide formed on both the active and field areas using a process similar to polyox process discussed in Section 4.1.3. Thicker oxide formed in the active area due to the high aspect ratio trenches, c) Photoresist mask patterened over the field area and open windows over the active area, d) Delamination of etch mask and underlying oxide during wet chemical etch of field oxide in active area.

Proposed Solution to Problem 1

In the current process, the field oxide is formed only after the trench etch and the added high aspect ratio of the trenches necessitates a long wet etch. The wet etch cannot be completely replaced with RIE, but a combination of RIE and wet etch is possible. The long oxide etch can be eliminated by swapping the field oxide and trench etch processes as illustrated in Figure 6.15. The trench etch lithography with the added topology of field oxide has been tested to be successful on a test sample. This solution however cannot be implemented when the H_2 etch is used in the trigate

process flow. The H_2 etch needs to be performed once the trench etch is completed and therefore the suggested process swap cannot be done.

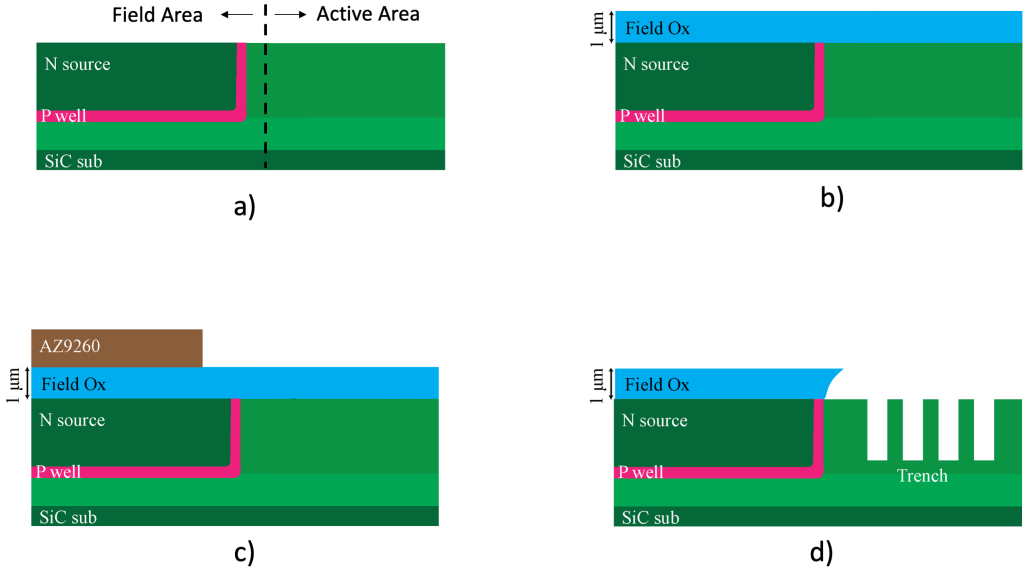


Figure 6.15.: Proposed solution and process implementation of field oxide in the trigate device process flow. a) Cross-section view of trigate sample after implant anneal, b) Field oxide deposition done before trench etch. This however does not allow the use of H_2 etch in the process flow. c) Pattern photoresist mask over field areas and open windows over active areas, d) Trench etch in active area after wet chemical etch to remove field oxide. Delamination is avoided due to shorted etch time and lower undercut.

Problem 2: Unoxidized polysilicon fillets

The poly-ox process relies on the complete oxidation of the polysilicon film as described above. However, there is a possibility of a small amount of polysilicon which remains unoxidized at the bottom of the trench in the active area as illustrated in Figure 6.16. When the field oxide is cleared in the active area using a HF or BOE etch, this polysilicon fillet remains unetched and is found to 'fall-back' or become

redeposited at the bottom of the trench. The only way to remove this polysilicon is to carry out a highly selective polysilicon dry etch, as a wet etch is aggressive and causes non-uniform etch of the oxide in the field area leading to further complications. Polysilicon dry etch using XeF_2 can be used but is generally avoided to ensure no contaminants get into the exposed gate oxide.

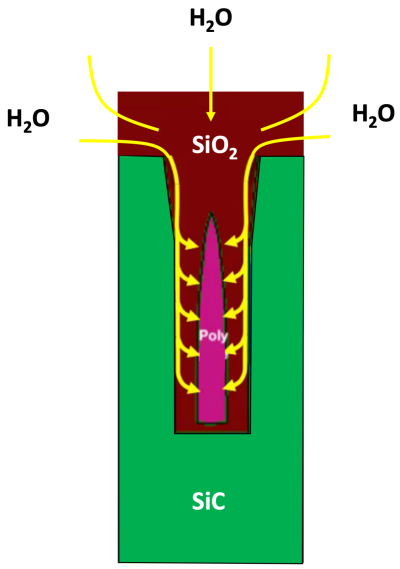


Figure 6.16.: Illustration of polysilicon fillets in SiC trenches in the current field oxide process.

Proposed Solution to Problem 2

As we do not require the field oxide to be the same quality as the gate oxide, the poly-ox process can be replaced with deposited SiO_2 process. This eliminates the polysilicon fillets and the resulting oxide film can be patterned using either a wet etch or a combination of wet etch and BOE etch. Two deposited oxides have been tested: LPCVD TEOS SiO_2 and the HDPECVD (high density plasma enhanced chemical vapor deposition) SiO_2. Planar and trenched MOS capacitors on N-type SiC samples were fabricated and the gate oxide was formed using the two deposition techniques

mentioned above with a metal gate electrode. The measured capacitance-gate voltage curves are shown in Figure 6.17 below. Bias stress measurements and capacitance hysteresis showed no evidence of mobile ion contamination in either of these methods. As seen in the figure, there is a clockwise hysteresis between the forward and backward sweep which is characteristic to interface trapping [116]. However, quantitative interface trap density measurement and analysis such as high-low technique [30] was not carried out as these samples were not NO annealed. Cross section images of oxide deposited on trench structures using both these techniques are shown in Figure 6.18. Both films have a conformal oxide topology, and are able to fill and planarize the trench. Both these oxide deposition techniques show great promise but further experiments and electrical analyses is required before applying to real devices.

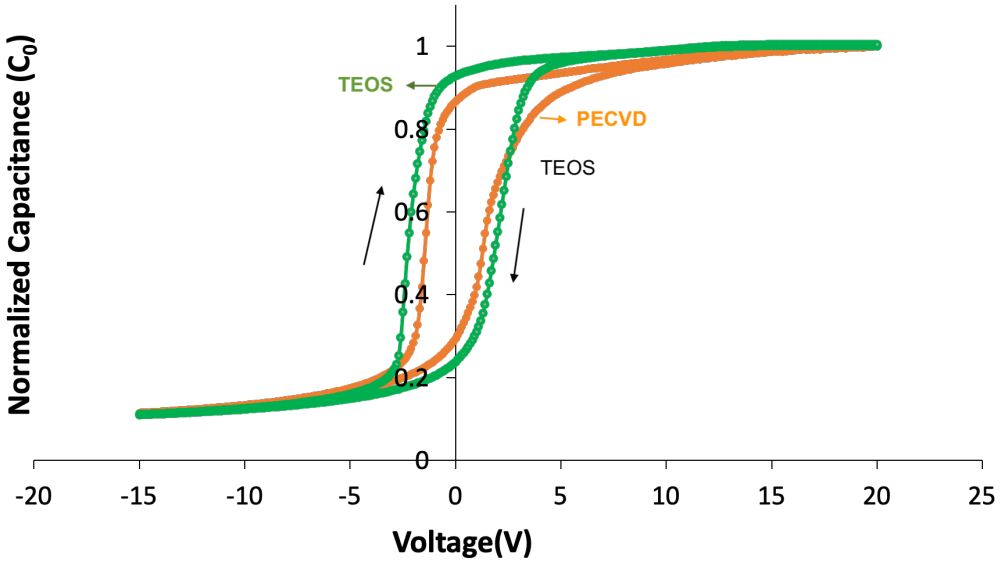


Figure 6.17.: Capacitance-Voltage characteristics MOS capacitors PECVD and TEOS SiO_2 without NO anneal. Measurement is done at 100kHz and the sweep direction is shown using black arrows.

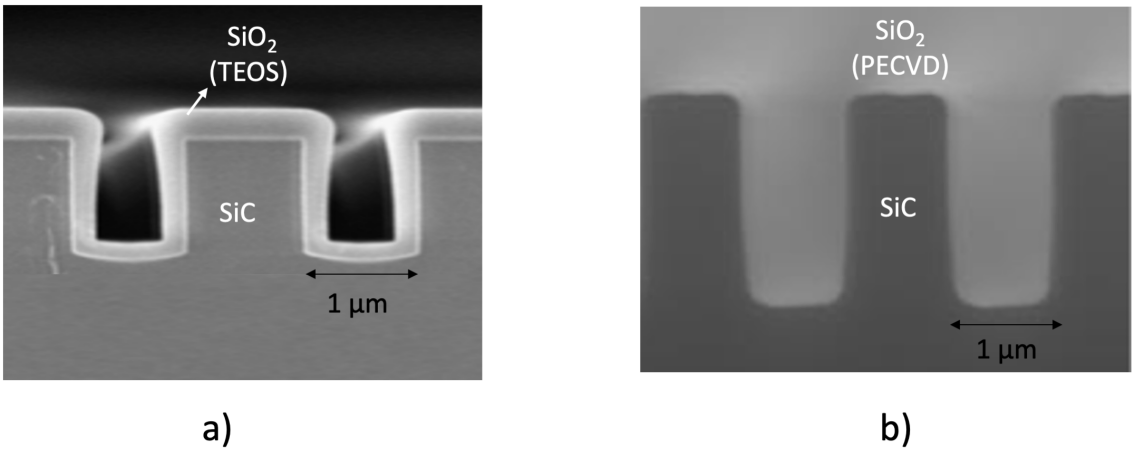


Figure 6.18.: Cross-section SEM images of a) TEOS and b) PECVD and oxide over SiC trenches.

APPENDICES

A. TRIGATE GEN-1 RUN SHEET

The procedures outlined in this run sheet are specific to the Scrifes cleanroom at the Birck Nanotechnology Center and the equipment available at the time the trigate Gen-1 were processed. The list of some of the commonly used chemicals and their vendors is provided in Table.A.1 at the end of the run sheet below. The run sheet below describes the process flow of the successfully fabricated Gen-1 samples 3Q2 and 1Q3.

1. Initial Wafer Clean

   (i) Solvent Clean

      (a) Soak in toluene: 5 minutes (do not let toluene dry on sample).

      (b) Soak in acetone: 5 minutes (do not let acetone dry on sample).

      (c) Soak in methanol: 5 minutes.

      (d) Soak in IPA: 5 minutes (end the solvent clean in IPA and use DI water to rinse only if necessary).

      (e) Blow dry using a N_2 gun.

      Blow the N_2 from sample to tweezers. It helps to place one edge of the sample on a cleanroom wipe and blow the solvent on the sample onto the wipe.

   (ii) Acid Clean

      (a) Acqua regia (3:1 - HCl : HNO_3) : 30 minutes

      let the solution rest for 5-8 minutes before dipping sample.

      (b) DI water rinse: 5 times. (never let acid dry on sample).

      (c) Piranha (1:1 - H_2O_2 : H_2SO_4) : 15 minutes

Solution needs to be used within 5 minutes of preparation. Volumetric proportion of H_2O_2 should not exceed that of H_2SO_4.

(d) DI water rinse: 5 times.

(e) BOE (buffered oxide etch) : 5 minutes.

(f) DI water rinse: 5 times.

(iii) Dehydrate sample on hot plate at 110°C for 5 minutes.

2. CSL Etch

3. P-well Implant Mask

(i) Sacrificial Oxide. (45-50nm)

(a) Solvent clean sample. (refer step.1i).

(b) RCA clean.

(c) Wet oxidation

- Equipment: Protemp tube# 4.
- Oxidation temperature: 1100°C
- Oxidation time(@ 1100°C): 5 hours
- Ambient: pyrogenic

(ii) Polysilicon Deposition(LPCVD) - target 5.25µm

Description: Polysilicon film to be used as an implant mask for the P-base and n-source implants

- Equipment: Protemp tube# 6.
- Deposition temperature: 630°C

Deposition at 630°C is used at this step in order to get reasonable depostion rate as a thick film of polysilicon needs to be deposited. Ploysilicon is deposited at 580°C as part of the poly-ox process for the gate oxide and is discussed in Section 4.1.3

- Deposition Rate(@630°C): 12.3 nm/min.

Test run carried out just before the actual run with trigate samples to determine/calibrate the deposition rate.

- Deposition time(@630°C): 425 minutes.
- Measured thickness of polysilicon film: 5.32µm

(iii) Thermal Oxidation (100 nm)

Description: Thermal oxide required for polysilicon etch mask described in Section 4.1.1.2

- Equipment: Protemp tube# 4.
- Oxidation temperature: 1100°C
- Oxidation time(@ 1100°C): 5 minutes
- Ambient: pyrogenic

(iv) Optical Lithography

Polysilicon mask pattern for P-base implant in PCM and test structures

(a) Mask#1:'P-well optical'.

(b) Dehydrate bake: 100°C, 5 minutes,

(c) Cool on heat sink.

(d) Resist: AZ1518 - spin coat: 4000 rpm for 60 seconds.

(e) Soft bake: 105°C for 3 minutes.

(f) Dose: 200 $mJcm^{-2}$ at 23 $mWcm^{-2}$ for 8.5 seconds in the MJB3-2 mask aligner.

(g) Develop: MF26A for 35 seconds.

(h) Rinse in DI water, 5 times.

(i) Dry with N_2 gun.

(j) Hardbake: 120°C for 5 min on hotplate.

(v) Buffered Oxide Etch(BOE), 2 minutes.

(vi) Remove photoresist

(a) PG remover at 80°C for 4 hours.

(b) Solvent Clean (refer step#1i).

(vii) Electron Beam Lithography

Polysilicon mask pattern for P-base implant in the active area

(a) Mask#2: 'P-well e-beam'.

(b) Dehydrate bake: 100°C, 5 minutes.

(c) Cool on heat sink.

(d) Resist: FOX-16 (HSQ) - spin coat: 2000 rpm for 60 seconds.

(e) Soft bake: 120°C for 3 minutes.

(f) Dose: $1050\mu Ccm^{-2}$ at 100kV and 100nA in the Vistec VB6.

The above parameters are specific to the Vistec electron beam(e-beam) system and has to be modified for other equipment. For example, the lithography at this step has been done using the JEOL JBX-8100FS e-beam system for the trigate Gen-2 samples and the corresponding parameters are listed in Appendix.B. At this step, a dose test run is carried out with dose in the window of $900 - 1100\mu Ccm^{-2}$ *just before the actual run with trigate samples.*

(g) Develop: 25% TMAH for 120 seconds.

(viii) Polysilicon Etch.

(a) Loading

- Carrier wafer: Clean 6-inch Si carrier wafer specifically procured and stored for the STS ASE etch. Carrier wafer must be flat without any residue in the areas that are exposed during the etch.
- Sample mounting: Good thermal contact is important for a uniform and consistent etch. Crystal bond worked well when applied uniformly to cover the entire sample from the back. Crystal bond should not be exposed to the etch.

(b) Etch Step

- Process gas: SF_6/O_2 : (130 sccm / 13 sccm).
- ICP power: 500W.
- Bias power: 20W
- Pressure: 18mT
- Cyle time: 5 seconds

(c) Deposit Step

- Process gas: C_4F_8(100 sccm)
- ICP power: 600W.
- Bias power: 0W
- Pressure: 18mT
- Cyle time: 5 seconds

There are two ways to know when all the polysilicon has been etched. First and the most obvious change is the noticeable reduction of surface roughness when the polyislicon is etched and SiC/SiO_2 surface is exposed. The SiC/SiO_2 has a smooth and uniform texture when seen in the microscope as compared to the rough polysilicon. A slight overetch is needed at this stage to ensure complete removal of polysilicon. Secondly, the color of thin polysilicon film when viewed in the microscope changes from dark grey at the beginning to light blue when only a thin layer of polysilicon is left towards the end of the etch.

(ix) High Energy Aluminum Implant

The complete implant schedule and profile for the P-base implant is listed in table.4.1. Mount samples on a 5-inch Si carrier using carbon tape. The tape should be under the sample and not exposed.

4. N-source Implant Mask.

Thermal oxidation of existing patterned polysilicon mask is used to self align the P-well and n-source implants in the active area, and electroplated Ni mask is used in the test structure areas as described in Section 4.76

(i) Solvent Clean. (refer to step.1i).

(ii) Measure Width(SEM) and Height(Stylus Profilometer) of Polysilicon Mask.

(iii) Piranha Clean, 5 minutes.

(iv) Thermal Oxidation.

  (a) Equipment: Protemp tube# 7.

  (b) Oxidation temperature: 1100°C

  (c) Oxidation time(@ 1100°C): 4 hours and 50 minutes.

  (d) Ambient: pyrogenic

(v) Measure Width(SEM) and Height(Stylus Profilometer) of Polysilicon Mask to Ensure 0.5µm Expansion.

  N+ Block Mask

(vi) Solvent Clean.

(vii) Blanket Evaporate Titanium(Ti) 20nm and Gold(Au) 500nm on sample.

(viii) Optical Lithography

  Photoresist acts as a mask during the electrodeposition process to prevent electroplating Ni in the active area.

  (a) Mask#3:'N+ block'.

  (b) Dehydrate bake: 100°C, 5 minutes.

  (c) Cool on heat sink.

  (d) Resist: AZ9260 - spin coat: 3000 rpm for 60 minutes.

  (e) Soft bake: 113°C for 6 minutes.

  (f) Dose: 510 $mJcm^{-2}$ in the Hidelberg maskless aligner.

  (g) Develop: AZ400K:DI water (1:3) for 3minutes and 20 seconds.

(h) Rinse in DI water, 5 times.

(i) Dry with N_2 gun.

(j) De-scum using Branson O_2 asher.

- Atmosphere: 1 Torr, Ar/O_2.
- Time: 2 minutes. Power: 100W.

(k) Postbake the samples in the oven for 30 minutes at 90°C to harden the photoresist.

Remove photoresist from the region of the sample on which the electroplating electrode will be attached using Q-tips and acetone.

(l) *Cover the front side of the wafers with a clear adhesive tape to protect it from getting electroplated and to protect devices from getting into contact with the electroplating solution. Do not use blue dicing tape as it reacts with the electrolyte.*

(ix) Electrodeposition of Ni - target: 3 µm

(a) Electrolyte Preparation

- Dissolve 350 g/liter of nickel sulfamate solution in water stirred at 40°C. Add 30 g/liter of boric acid and stir until it dissolves. Then add 30 g/liter of nickel carbonate and stir for 1 hour. Switch off the heat and let the solution settle down for 24 hours.
- Mix the solution continuously and let it settle for around 2 hours.
- Filter the solution by using Whatman's filter papers to filter out large particles that might still be in solution.
- Measure the pH and ensure that it is between $4-5$. If the pH is too high, lower it by adding 10 ml of sulfamic acid and re-measure after $3-5$ minutes. Repeat until the PH is within the accepted range. If it is too low, add 5 grams of sodium carbonate and stir well. However, this might introduce particles that have to be filtered out once the pH is stabilized. Measure to check the pH just before use as it might drift with time.

Electroplating Procedure

- Set the bath at 40°C and stir continuously. Ensure stirring does not cause bubbles.
- A bar of 99.9% purity Ni is used as the anode. This is cleaned using DI water, inserted into the electrolyte and connected to the positive terminal of a function generator such as Keithley 6221.
- The sample is now wet with DI water and then clipped to the negative terminal of the function generator using 'crocodile clips' and aluminum foil. The sample is then inserted into the electrolyte solution.
- Current is set at 15 mA and the deposition rate of Ni is $\sim 1.2\mu m/hr$.

Removal of Seed Layer

- Strip photoresist once the deposition is complete using PRS 2000 solution for 5 hours at 90°C.
- The gold layer is wet etched using Transense GE-8148 Au etchant solution. A test sample is used to calibrate the etch rate as this was found to be different than the once quoted by the manufacturer.
- The titanium film is left unetched on the surface due to risk of etching silicon dioxide during this step.

(x) High Energy Nitrogen Implantation.

The complete implant schedule and profile for the P-base implant is listed in Table 4.2. Mount samples on a 5-inch Si carrier using carbon tape. The tape should be under the sample and not exposed. For high temperature implantation, the sample is de-mounted from the carrier wafer and solvent cleaned. The samples are then packed in separate boxes and shipped for high temperature, high dose implant described in Section 4.55.

5. P+ Implant Mask

Metal mask is used and is patterned by e-beam lithography in the active area and optical lithography in field and tester area.

(i) Strip the Ni mask using piranha solution, 10 minutes.

(ii) DI water rinse, 5 times.

(iii) Strip the polysilicon mask using $DI + \mathrm{HF} + \mathrm{HNO_3}$ (1:1:4) for 5 minutes.

(iv) DI water rinse, 5 times.

(v) Solvent Clean. (refer to step.1i).

(vi) Electron Beam Lithography

(a) Dehydrate bake, 110°C for 5 minutes.

(b) Cool on heat sink.

(c) Spin coat EL11 co-polymer at 2000 rpm(thickness:800nm) for 60 seconds.

(d) Soft bake at 180°C for 3 minutes.

(e) Cool on heat sink.

(f) Spin coat PMMA A4 at 3000 rpm(thickness: 200 nm) for 45 seconds.

(g) Soft bake at 180°C for 3 minutes.

(h) Exposure: Dose of 700 μCcm^{-2} at 100 kV and 122 nA is used in the Vistec VB6. (refer to step 3vii)

(i) Develop: Soak in MIBK:IPA(1:3) for 1 minute. Rinse in IPA is used to stop the development.

(j) De-scum in Branson O_2 Etcher.

- Power: 100W
- Gas: Ar/O_2 (140 sccm/80 sccm).
- Time: 60 seconds.

(k) Evaporate Ti/Ni (10 nm/ 500 nm).

(l) Lift-Off

- PG remover solution, 4 hours.

(vii) Optical Lithography

(a) Mask#5: 'P-plus-optical'

(b) Dehydrate bake, 110°C for 5 minutes.

(c) Cool on heat sink.

(d) Spin coat LOR3B at 2000 rpm (thickness:400 nm) for 60 seconds.

(e) Soft bake on a hot plate 195°C for 3 minutes.

(f) Cool on heat sink.

(g) Spin coat LOR3B a second time at 2000 rpm(total thickness:800nm) for 60 seconds.

(h) Soft bake on a hot plate 195°C for 3 minutes.

(i) Cool on heat sink.

(j) Spin coat AZ1518 at 4000 rpm (thickness:1800 nm) for 45 seconds.

(k) Soft bake on a hot plate 105°C for 1 minutes.

(l) Exposure: Dose of $230\mu Ccm^{-2}$ using a 405 nm laser.

(m) Develop: Soak in AZ400K:DI water (80 ml:300 ml) for 30 seconds. Rinse in DI water immediately to stop the development.

Usually MF26A is used to develop after exposure of AZ1518 resist. However, sharper features were acheived using the AZ400K developer when dimensions of the pattern are lower than 3µm. *Here it is important to get the ratio of the developer to DI water exact and also to immediately rinse in DI water using the 'water gun' to stop the development.*

(n) De-scum in Branson O_2 Etcher.

- Power: 100 watts.
- Gas: Ar/O2(140 sccm/80 sccm).
- Time: 60 seconds.

(o) Evaporate Ti/Ni ($10nm/500nm$).

(p) Lift-Off

- PG remover solution, 4 hours

6. Implant Anneal

(i) Piranha Clean, 5 minutes (removes Ni Mask).

(ii) BOE Etch,2 minutes (removes oxide).

(iii) Acqua Regia, 5 minutes.

(iv) Piranha Clean, 15 minutes.

(v) Solvent Clean.

(vi) Carbon Cap Formation.

(a) Precondition a quartz tube ('blue-m') to a temperature of 250°C and flow nitrogen through the tube at maximum flow. This is done at least 1 hour prior to the next steps.

(b) Spin Coat AZ 1518 at 3000 rpm for 45 seconds.

Ensure no edge beads or gaps of photoresist at the corners and edges.

(c) Soft bake: 105°C for 3 minutes on hot plate.

(d) Switch the gas from argon to nitrogen in the 'blue-m' chamber.

(e) Increase temperature slowly from 105°C to 150°C at a ramp rate of 5°C per minute.

(f) Transfer to the 'blue-m' quartz tube in argon ambient.

(g) Ramp up temperature of the tube from 250°C to 650°C.

(h) Anneal for 30 minutes at 650°C.

(i) Cool down tube to $\sim$ 200°C and unload tha sample.

If the process is done right, the surface of the sample is black with a mirror-like finish.

(vii) Implant Anneal

(a) Load samples into Epigress CVD chamber.(follow tool specific SOP).

(b) Anneal Tempearature: 1700°C.

(c) Anneal Time: 20 minutes.

(d) Ambient: Argon at 400 mbar and flow rate of 4 slm.

(viii) Carbon Cap Removal

Oxidation is done to 'burn-off' the carbon. This is done in blue-m chamber.

i. Oxidation Temperature: 900°C.

ii. Oxidation Time: 1 hour.

iii. Ambient: Dry O_2.

(ix) Piranha Clean, 15 minutes.

7. Trench Etch

Trigate Gen-1 samples have a trench depth of 2µm. *Multiple test samples are loaded along with the trigate samples during the trench etch to measure etch rates and also spatial variation of the etch depth across the carrier wafer.*

(i) Solvent Clean.

(ii) Sacrificial Oxide - Target: 30nm (refer step.3i)

(iii) Electron Beam Lithography

(a) Mask#6: 'trench e-beam'.

(b) Dehydrate bake: 100°C, 5 minutes

(c) Cool on heat sink

(d) Resist: PMMA A6 - spin coat: 4000rpm (400nm) for 60 seconds.

(e) Soft bake: 180°C for 3 minutes.

(f) Dose: $1300\mu Ccm^{-2}$ at 100kV and 30nA in the JOEL JBX 8100FS (dose test run carried out with dose in the window of $1200-1400\mu Ccm^{-2}$ just before the actual run with trigate samples)

Proximity correction is applied during the e-beam write. Also lowest possible beam current is used to reduce line edge roughness. Any roughness in the pattern gets transferred to the Ni mask and eventually to the trench shape and sidewall roughness.

(g) Develop: MIBK:IPA(1:3) for 60 seconds. IPA rinse is used to stop the developement.

(iv) De-scum using O_2 barrel etch.

(a) Power: 100 W

(b) Gas: O_2/Ar : $140sccm/12sccm$

(c) Pressure: 1 Torr.

(d) Time: 30 seconds.

(v) Evaporate Ti/Ni (15 nm/200 nm).

(vi) Lift-off (refer to step.5(vi)l).

(vii) Optical Lithography

(a) Mask#7:'Trench Optical'.

(b) Dehydrate bake: 100°C, 5 minutes.

(c) Cool on heat sink.

(d) Resist: AZ9260 - spin coat: 3000rpm for 60 seconds.

(e) Soft bake: 113°C for 6 minutes.

(f) Dose: $510mJcm^{-2}$ in the Hidelberg maskless aligner.

(g) Develop: AZ400K:DI water (1:3) for 3minutes and 20 seconds.

(h) Rinse in DI water, 5 times.

(i) Dry with N_2 gun.

(j) De-sum using Branson O_2 asher.

- Atmosphere: 1 Torr, Ar/O_2.

- Time: 2 minutes. Power: 100 watts.

(viii) Trench RIE Etch

i. Sample Loading

(a) Sample is mounted onto 4-inch silicon carrier wafer with Santovac at 70°C on a hot plate.

The viscosity of Santovac is very low, so a few drops of Santovac is sufficient to cover all over the backside. Santovac is a good thermal conductor and helps in uniform thermal distribution and heat removal form the sample during the RIE etch. The trench etch is aggressive and therefore temperature during the etch is an important factor that could cause large variation.

(b) Test samples are loaded along with trigate samples to measure etch rate and trench depth.

ii. Trench Etch

*Test samples with fin-spacing (*5 µm*) are processed just prior to the trigate samples. The trench depth is measured and the etch rate is calibrated. The trench depth varies with fin-spacing and therefore and a factor of 0.73 correction to the trench depth of the test samples is applied to obtain the trench depth of the denser (*0.5µm*) pattern in the trigate samples.*

(a) Oxford Plasmapro 100 ICP-RIE at the University of Norte Dame is used for the etch.

(b) Trench etch is done in multiple steps of short duration each.

(c) Gas: SF_6

(d) ICP Power: 2800 Watts

(e) Bias Power: 200

(f) Pressure: 5 mtorr

(g) DC Voltage: 255 V

(h) Temperature: 10°C

8. Solvent Clean.

9. RCA Clean

10. Sacrificial Oxide - Target: 30nm (refer step.3i)

11. H_2 Etch

    One of the four Gen-1 samples(1Q3) described in this report undergoes the H_2 etch with the intention of smoothing SiC trench sidewalls.

    (i) Solvent Clean.

    This step is done immediately prior to loading into the Epigress CVD tool for the H_2 etch to ensure no particulates are present on the sample during the etch.

    (ii) Load samples into Epigress CVD tool.

    (iii) H_2 etch parameters

    Detailed process development and parameter discussion is discussed in Section 4.1.3.

    (a) Gas : Pure hydrogen.

    (b) Pressure: 150 mTorr.

    (c) Time: 3 minutes. (refer to 4.25 for process flow.)

12. Gate Oxide

    Poly-ox is used as the gate oxide and a detailed discussion of the process development is available in Section 4.1.3

    (i) Sample Clean

    Cleaning of the sample is done immediately prior to the poly-ox process. Unreliable and below optimal results have been observed without this step.

    (a) Solvent Clean.

(b) Piranha Clean, 15 minutes.

(c) Acqua Regia, 15 minutes.

(d) RCA Clean.

(e) BOE+HCl(1:1), 5 minutes.

(f) Solvent Clean.

(g) RCA Clean.

(h) Soak samples in IPA.

(ii) Polysilicon Deposition.

(a) LPCVD Protemp tube# 6 is used.

(b) Run the recipe: 'Poly-Polyox' and wait until tube completely purges.

(c) Once purged, remove samples from IPA and blow dry with N_2.

(d) Immediately load the samples into the polysilicon deposition tube and pump down.

o *Use clean tweezers that are dedicated for gate oxide only. Twezeers should not have carbon, plastic or teflon tip.*

(e) Deposition Parameters:

- Gas: SiH_4
- Pressure: 150mTorr
- Temperature: 580°C.
- Time: 80 seconds

(f) Keep samples inside with the tube pumped down until the oxidation tube is ready to be loaded.

(iii) Thermal Oxidation

(a) Pyrogenic oxidation tube# 1 is used for gate oxides only.

(b) Vent the polysilicon tube.

(c) Once the polysilicon tube is compeltely vented, extract the loading arm from the tube and at the same time run recipe 'Oxi-Polyox' on the oxidation tube.

(d) Unload the samples from the polysilicon tube.

Similar procedure as in step.12(ii)d is followed..

(e) Samples are immediately loaded into the oxidation tube.

(f) Thermal oxidation parameters.

- Temperature: 1000°C.
- Ambient: Wet oxidation - pyrogenic.
- Time: 7 minutes

(g) High temperature anneal.

- Temperature: 1100°C.
- Ambient: Argon
- Time: 60 minutes

(h) Re-oxidation

- Temperature: 900°C.
- Ambient: Wet oxidation - pyrogenic.
- Time: 120 minutes

(i) Cool down tube to 400°C.

(j) Let the samples stay in the oxidation tube until the NO anneal tube is ready to be loaded.

(iv) NO Anneal

- Set temperature of tube to 150°C and purge with argon for 2 hours before loading samples.
- Load samples directly from oxidation tube.
- Anneal temperature: 1175°C
- Anneal time: 2 hours.

13. Polysilicon Gate

Samples are unloaded from the NO anneal tube and immediately loaded into the polysilicon LPCVD tube. Test samples are prepared by solvent, piranha and BOE etch to go along with the trigate samples in the LPCVD tube.

(i) Purge LPCVD polysilicon deposition tube.(Protemp tube# 6).

(ii) Once completely purged, extract the loading arm and now unload samples from the NO anneal tube and load them to the LPCVD tube immediately.

Follow the loading procedure described in step.12(ii)d.

(iii) Polysilicon Deposition (LPCVD) - Target:1µm

(a) Equipment: Protemp tube# 6.

(b) Deposition Temperature: 630°C

(c) Deposition Rate(@630°C): 12.3 nm/min. (test run carried out just before the actual run with trigate samples to determine/calibrate the depostion rate.)

(d) Deposition time(@630°C): 82 minutes.

(e) Measured thickness of polysilicon film: 1.1µm

(iv) Polysilicon Doping.

Phosphorous is used to dope the polysilicon gate and the dopant is spin coated onto the sample. To increase the shelf life, the spin-on dopant solution is stored in the refrigerator using small 5ml plastic bottles.

(a) Place the spin-on bottle(PG-509) in a solvent hood for 3 hours prior to spin coating.

High sheet resistances have been observed if the dopant is not at room temperature while spin coating. This could be due to condensation on the surface that degrades the active dopant concentration. Also, black particulates are observed in film if the dopant is not at room temperature. These particulates do not seem to affect the sheet resistance but

they do not get etched away during the polysilicon RIE etch. Do not leave the solution outside the refrigerator for more than 24 *hours.*

(b) Start recipe 'polygate-dope-trigate' in protemp tube#8. It takes about 1 hour to ramp up to 800°C.

(c) Now unload the sample from the LPCVD polysilcon deposition tube.

(d) Solvent clean.(refer step.1i)

(e) BOE etch, 2 minutes

(f) Piranha soak,2 minutes.

Piranha clean is done just before spin coating the dopant to ensure the surface of the sample is hydrophilic.

(g) Dehydrade bake, 5 minutes on hot plate. Now set the hotplate to 200°C.

(h) Spin coat dopant

- Step 1: Spin at 500 rpm for 2 seconds.
- Step 2: Spin at 3000 rpm for 17 seconds.

Dopant is applied using a clean and dry plastic pipette. Inconsistent results have been onserved using the glass pipette and therefore not recommended. If glass pipette has to be used, dehydrate bake the pipette at 110°C *and cool down by continuously blowing* N_2 *before use. During spinning, every surface of the spinner tool is covered by aluminum foil to prevent any toxic SOD exposure to the tool.*

(i) Bake sample at 200°C for 20 minutes.

Immediate transfer between spin coat chamber and hot plate is important. Some vapours are usually generated when placed on the hot plate and therefore a fair distance of personnel from the hot plate is recommended.

(j) Load samples into the 'drive-in' tube#8 that was heated to 800°C in *step.*13$(iv)b$ using special heat resistant gloves.

(k) Drive in at 950°C for 2 hours in argon(80%) and oxygen(20%) ambient.

(l) BOE Etch, 5 minutes.

(m) Measure Sheet Resistance.

When measured using the 4-point probe, the sheet resistance is usually between 50Ω - 100Ω *per square.*

(n) Repeat Polysilicon Doping (step.13iv).

(o) BOE Etch, 5 minutes.

Polysilicon gate is now doped two times.

When measured using the 4-point probe, the sheet resistance is usually between 10Ω - 40Ω *per square.*

(v) Polysilicon Gate Pattern.

(a) Electron Beam Lithography.

- Mask#8 - 'gate-ebeam' for active area only.
- Solvent clean.
- Dehydrate bake, 120°C for 3 minutes.
- Cool down on heat sink.
- Spin coat CSAR resist at 4000 rpm for 60 seconds.(thickness: 400nm)
- Soft bake at 150°C for 3 minutes.
- E-beam lithography is done using JEOL 8100FSX with a dose of $300\mu C/cm^2$ and a beam current of 30nA.

  Alignment of the feature to the P-base is very important at this step and therefore higher beam currents are not used. Alignment is a challenging at this step due to the roughness of the polysilicon. Increase the width of scan and smoothing of the alignment edge calculation to get good alignment.
- De-scum in Branson O_2 etcher.(refer to step.4(viii)j)
- Polysilicon etch, total time: 2 minutes and 10 seconds. (refer to step.3iv).

A total of 1.4µm *is etched, recessing* $\sim 400nm$ *of polysilicon inside the trenches.*

- Soak in PG Remover, 80°C for 5 hours(strip CSAR resist).

(b) Optical Lithography.

- Mask#9 - 'gate-optical' for field and tester areas.
- Solvent clean.
- Dehydrate bake, 110°C,3 minutes.
- Cool on heat sink.
- Spin coat AZ9260 at 4000 rpm for 60 seconds.
- Soft bake at 110°C for 5 minutes.
- Expose with dose of $510mJ/cm^2$ using 405nm laser in the Hidelberg MLA writer.
- Develop using AZ400K:DI water(80ml : 300 ml) for 3.5 minutes.
- De-scum using Branson O_2 asher.(refer to step.4(viii)j).
- Polysilicon etch, $2minutes, 10seconds$.(refer to step.3iv)

14. Thermal Oxidation for Inter Layer Dielectric.

(i) Solvent Clean.

(ii) RCA Clean

The BOE etch is not done as part of this RCA clean.

(iii) Thermal Oxidation - target:1µm

(a) Protemp Tube# 4.

(b) Temperature: 1100°C.

(c) Ambient: Wet-Pyrogenic.

(d) Time: 205 minutes.

15. Source/Drain Ohmic Contacts

(i) Front Side Nickel Deposition and Anneal

(a) Mask#10: 'ohmic'

(b) Solvent clean.

(c) Dehydrate bake,110°C, 3 minutes.

(d) Spin coat LOR3B at 2000 rpm,45seconds.

(e) Soft bake at 190°C,5 minutes

(f) Spin coat AZ1518 at 4000 rpm, 60 seconds.

(g) Soft bake at 105°C,2 minutes.

(h) Exposure dose of $230 mJ/cm^2$ with the 405nm laser in the Hidelberg MLA.

(i) Develop in MF26A for 30 seconds.

(j) De-scum in brasnson O_2.(refer to step number.4(viii)j)

This step is to remove photoresist residue from the developed windows.

(k) BOE etch, 50 seconds.

- *This wet etch removes the* $\sim$ *45nm thick gate oxide over the source regions to be silicided. A careful calibration of the etch rate using a test sample is necessary to ensure the oxide is completely removed while the ILD oxide and undercut are kept at a minimum.*
- *The source pads can be electrically probed at this point and checked for electrical continuity to ensure all the oxide is etched. A slight overetch of* $\sim$ 10 *seconds after this point can be done to ensure all oxide is removed.*

(l) SiC RIE

This step is intended to increase the surface roughness and thereby surface area of the exposed SiC surface that could lead to lower contact resistivity.

- Equipment: Jupiter RIE

- Gas: SF_6/Ar:(20 sccm/10 sccm).
- Power: 100 Watts.
- Pressure: 195 mTorr.
- Time: 20 seconds.

Expect to etch around 10nm of SiC.

(m) De-scum in brasnson O_2.(refer to step#.4(viii)j)

This step is to removes any polymers that may have formed during the RIE etch.

(n) BOE etch, 20 seconds.

(o) Evaporate 50nm of nickel at 1.5 $\text{Å}\,\text{s}^{-1}$ec with the chamber pressure at 2.2×10^{-7} torr.

(p) Lift-off metal in PG remover at 60°C for $4 - 5$ hours.

(ii) Ohmic Anneal at 750°C - Step 1

The following procedure is specific to the Jiplec Jetfirst 2100 RTA

(a) Turn on the Jiplec and let it warm and stabilize for 15 minutes.

This step avoids the 'water cooling station error'

(b) Clean 6-inch silicon 'carrier' wafer and a quarter of 4-inch 'base' sample.

'Base' sample is a $Si - SiO_2$ sample that is preferably prepared by thermal oxidation of a clean silicon sample. The size of the 'base' sample must be larger than the sample to be annealed.

- Solvent clean.
- Piranha soak, 15 minutes.
- Acqua regia, 15 minutes.

(c) Load the 6-inch silicon carrier wafer wih the polished side facing up.

(d) Run 'recipe-1' to purge the chamber with N_2 for 30 minutes.

recipe path- C:ProgramFiles/Jetfirst/recipe/studentspecial/rahul/ohmic

(e) Cool down and do not open the chamber.

(f) Run 'recipe-2' to bake out the chamber at 250°C.

(g) Open chamber and place the 'base' sample with the polished side facing up. the Ti pellets are also loaded as shown in Figure 4.47.

(h) Run 'recipe-3' to pump and purge the chamber multiple times at 250°C.

(i) Run 'recipe-4' to pump and purge the chamber multiple times at 500°C.

(j) Cool down and do not open the chamber.

(k) Run 'ohmic-750°C' to mimic the ohmic anneal without the real samples loaded. Ensure good PID control and temperature stabilization.

(l) Now load the samples to be annealed face-down onto the 'base' sample.

(m) Run 'recipe-2'.

(n) Cool down and do not open the chamber.

(o) Run 'ohmic-750°C'. Ohmic anneal at 750°C for 3 minutes in argon ambient.

(p) Piranha soak, 7 minutes to remove non-silicided nickel over ILD.

(iii) Back Side Nickel Deposition and Anneal

(a) Solvent clean.

(b) Spin coat AZ9260 on the front surface at 2000 rpm for 60 seconds

(c) Soft bake at 110°C for 6 minutes on hot plate

(d) Hard bake at 155°C for 10 minutes.

(e) BOE dip,3 minutes.

(f) Polysilicon etch, 2.5 minute.(refer to step#3iv).

(g) De-scum in Branson O_2 asher. (refer to step#4(viii)j).

(h) BOE etch, 5 minutes.

(i) Polysilicon etch,1 minute.

(j) BOE etch, 1 minute.

(k) Evaporate 100nm of Ni on the back surface at a rate of $1.5\text{Å}\,\text{s}^{-1}$ and a pressure of 1×10^{-7} torr.

(l) Strip off the resist from the front surface using a PG remover soak for 5 hours.

(iv) Ohmic anneal at $1000°\text{C} - Step2$

This anneal is done to obtain low contact resistivity.

(a) High temperature anneal is done at 1000°C following the procedure outlined in step.15ii.

(b) Load the sample with the backside facing up.

Ensure to check the PID control multiple times because temperature overshoot could cause the carrier sample to crack and disrupt the temperature reading.

(v) Post Anneal Treatment.

i. Solvent Clean.

ii. O_2 RIE using Jupiter III.

(a) Gas O_2 at 50 sccm.

(b) Pressure 300 mTorr

(c) Power 200 Watts

(d) Time $2 - 3$ minutes

16. Gate Contact

(a) Optical Lithography

- Mask#11 'ILD opening'.
- Solvent clean.
- De-hydrade bake at 110°C for 1 minute.
- Cool down on heat sink.

- Spin coat AZ9260 at 4000 rpm for 60 seconds.
- Soft bake ar 110°C for 6 minutes.
- Expose with dose of $503 mJ/cm^2$ using the 405nm laser in the Hidelberg MLA writer.
- Develop using AZ400K:DI water(80ml:300ml) for 3 minutes and 15 seconds.
- De-scum using Branson O_2 asher.(refer step#4(viii)j)

(b) ILD Opening - SiO_2 etch

- Load sample onto 6-inch Si carier wafer using crystal bond. The Si carrier wafer is specific to the Panasonic RIE etch tool as it has a 'jeida' flat instead of the usual 'primary' and 'seconday' flat.
- Gas: $CF_4 : CHF_3$ - 10 sccm/40 sccm.
- ICP power: 650 watts
- Bias power: 50 watts
- Pressure: 1 pascal.
- Time: 5 minutes, 20 seconds. (450nm of SiO_2 etched)
- Unload sample from carrier wafer.
- DI water rinse.
- BOE etch, 1 minute.
- PG remover soak,6 hours.

17. Top Metal

(i) Solvent clean.

(ii) Sputter 50 nm of titanium at 1.5 nm/min using 150 watts and chamber pressure of 7×10^{-7} torr.

(iii) Cool down and do not break vacuum.

(iv) Sputter 1µm of gold at 7.2 nm/min using 75 watts and chamber pressure of 1×10^{-6} torr.

(v) Optical lithography using mask#12 and procedure in step#16i.

(vi) Wet etch the gold film in the resist windows using GE-8148 from Transene.

- *Etch rate is $\sim$ 7 nm/min at room temperature.*
- *The chemical does not yield a uniform etch if expired. Use test samples to verify etch rate.*
- *A number of particulates are found to deposit on the surface at the end of the etch. This can be minimized by soaking the sample either face down or sideways in the solution and performing a thorough DI water rinse immediately after the acid soak.*

(vii) Wet etch titanium using TFTN from Transene at 70°C for 6 minutes.

A teflon coated thermocouple is used to accurately measure the temperature of the etchant as the etch rate becomes erratic at temperature greater than 80°C.

18. Measure Devices!!

Table A.1.: Commonly used chemicals in the trigate fabrication process and their vendors.

Name of Chemical/Solution	**Vendor**	**Application**
AZXX Photoresist	MicroChem	Optical Lithography
PMMA	Kayakli	Electron Beam Lithograpy
FOX-16 (HSQ)	DOW Chemicals	Electron Beam Lithograpy
CSAR	Allresist	Electron Beam Lithograpy
LOR3B	MicroChem	Optical Lithography (undercut for lift-off)
EL11 Co-polymer	MicroChem	Electron Beam Lithograpy (undercut for lift-off)
MF 26A	DOW Chemicals	Developer for AZ1518 Resist
MIBK Developer	MicroChem	Developer for PMMA Resist
Xylene Developer	DOW Chemicals	Developer for CSAR Resist
TMAH 25%	MicroChem	Developer for FOX-16 Resist
PG Remover	MicroChem	Dissolve Photo and Electron Beam Resists
PRS 2000	J.T. Baker	Dissolve Photo and Electron Beam Resists
GE-8148	Transene	Gold Etchant
TFTN	Transene	Titanium Etchant
P-509	Filmtronics	Phosphorous Spin On Dopant

B. TRIGATE GEN-2 RUN SHEET

The procedures outlined in this run sheet are specific to the Scrifes cleanroom at the Birck Nanotechnology Centre and the equipment available at the time the trigate Gen-2 were processed. The run sheet below describes the process flow of the successfully fabricated Gen-2 samples 400Q1 and 400Q4.

1. Initial Wafer Clean

   (i) Solvent Clean

      (a) Soak in toluene: 5 mins (do not let toulene dry on sample).

      (b) Soak in acetone: 5 mins (do not let acetone dry on sample).

      (c) Soak in methanol: 5 mins

      (d) Soak in IPA: 5 mins (end the solvent clean in IPA and use DI water to rinse only if necessary)

      (e) Blow dry using a N_2 gun. (blow the N_2 from sample to tweezer. It helps to place one edge of the sample on a cleanroom wipe and blow the solvent on the sample onto the wipe).

   (ii) Acid Clean

      (a) Acqua regia ($3:1-HCl:HNO_3$) : 30 mins (let the solution rest for 5-8 mins before dipping sample).

      (b) DI water rinse: 5 times. (never let acid dry on sample).

      (c) Piranha ($1:1-H_2O_2:H_2SO_4$) : 15 mins (solution used within 5 minutes of preparation. Volumetric proportion of H_2O_2 should not exceed that of H_2SO_4).

      (d) DI water rinse: 5 times

(e) BOE (buffered oxide etch) : 5 mins

(f) DI water rinse: 5 times

(iii) Dehydrate sample on hot plate at 110°C for 5 minutes.

2. CSL etch

3. P-well implant mask lithography

(i) Sacrificial Oxide. (45-50nm)

(a) Solvent clean sample. (refer step.1i).

(b) RCA clean

(c) Wet oxidation

- Equipment: Protemp tube# 4.
- Oxidation temperature: 1100°C
- Oxidation time(@ 1100°C): 5 hours
- Ambient: pyrogenic

(ii) Polysilicon deposition(LPCVD) - target 4.8µm

Description: Polysilicon film to be used as an implant mask for the p-base and n-source implants

(a) Equipment: Protemp tube# 6.

(b) Deposition temperature: 630°C

Deposition at 630°C is used at this step in order to get reasonable depostion rate as a thick film of polysilicon needs to be deposited. Ploysilicon is deposited at 580°C as part of the poly-ox process for the gate oxide and is discussed in Section 4.1.3

(c) Deposition Rate(@630°C): 12.3 nm/min. (test run carried out just before the actual run with trigate samples to determine/calibrate the depostion rate.)

(d) Deposition time(@630°C): 369 minutes.

(e) Measured thickness of polysilicon film: 5.00µm

(iii) Electron Beam Lithography

Polysilicon mask pattern for p-base implant in the active area and test strutures using the process flow described in Section 4.13

(a) Mask#I: 'p-well e-beam'.

(b) Dehydrate bake: 100°C, 5mins

(c) Cool on heat sink

(d) Resist: AR-P 6200 CSAR- spin coat: 4000rpm for 60sec. (film thickness:$\sim$ 400 nm)

(e) Soft bake: 150°C for 3 mins.

(f) Dose: $290\mu Ccm^{-2}$ at 100kV and 100nA in the JOEL JBX-8100 FS. (dose test run carried out with dose in the window of $250-340\mu Ccm^{-2}$ just before the actual run with trigate samples)

(g) Develop: Xylene for 70 seconds followed by rinse in IPA to stop development.

(iv) Polysilicon Etch.

Loading

(a) Carrier wafer: Clean 6-inch Si carrier wafer specifically procured and stored for the STS ASE etch. Carrier wafer much be flat without any residue in the areas that are exposed during the etch.

(b) Sample mounting: Good thermal contact is important for a uniform and consistent etch. Crystal bond worked well when applied uniformly to cover the entire sample from the back. Crystal bond should not be exposed to the etch.

Etch Step

(c) Process gas: SF_6/O_2 : (130 sccm / 13 sccm).

(d) ICP power: 500W.

(e) Bias power: 20W

(f) Pressure: 18mT

(g) Cyle time: 5 seconds

Deposit Step

(h) Process gas: C_4F_8(100 sccm)

(i) ICP power: 600W.

(j) Bias power: 0W

(k) Pressure: 18mT

(l) Cyle time: 5 seconds

There are two ways to know when all the polysilicon has been etched. First and the most obvious change is the noticeable reduction of surface roughness when the polyislicon is etched and SiC/SiO_2 surface is exposed. The SiC/SiO_2 has a smooth and uniform texture when seen in the microscope as compared to the rough polysilicon. A slight overetch is needed at this stage to ensure complete removal of polysilicon. Secondly, the color of thin polysilicon film when viewed in the microscope changes from dark grey at the beginning to light blue when only a thin layer of polysilicon is left towards the end of the etch.

4. N-source Implant Mask.

Thermal oxidation of existing patterned polysilicon mask is used to self align the p-well and n-source implants in the active area and electroplated Ni mask is used in the test structure areas as described in Section 4.76

(i) Solvent Clean. (refer to step.1i)

(ii) Measure Width(SEM) and Height(Stylus Profilometer) of Polysilicon Mask.

(iii) Piranha clean, 5 minutes.

(iv) Thermal Oxidation.

(a) Equipment: Protemp tube# 7.

(b) Oxidation temperature: 1100°C

(c) Oxidation time(@ 1100°C): 4 hours and 50 minutes.

(d) Ambient: pyrogenic

(v) Measure Width(SEM) and Height(Stylus Profilometer) of Polysilicon Mask to Ensure 0.5µm Expansion of the Mask.

N+ Block Mask

(vi) Solvent Clean.

(vii) Blanket Evaporate Titanium(Ti) 20nm and Gold(Au) 500nm on sample.

(viii) Optical Lithography

Photoresist acts as a mask during the electrodeposition process to prevent electroplating Ni in the active area.

(a) Mask#II:'n+ block'.

(b) Dehydrate bake: 100°C, 5mins

(c) Cool on heat sink

(d) Resist: AZ9260 - spin coat: 3000rpm for 60sec

(e) Soft bake: 113°C for 6 mins.

(f) Dose: $510 mJcm^{-2}$ in the Hiderberg maskless aligner.

(g) Develop: AZ400K:DI water (1:3) for 3minutes and 20 seconds.

(h) Rinse in DI water, 5 times.

(i) Dry with N_2 gun.

(j) De-sum using Branson O_2 asher.

- Atmosphere: 1 Torr, Ar/O_2.

- Time: 2 minutes. Power: 100W.

(k) Postbake the samples in the oven for 30 minutes at 90°C to harden the photoresist.

(l) Remove photoresist from the region of the sample on which the electroplating electrode will be attached using Q-tips and acetone.

(m) Cover the front side of the wafers with a clear adhesive tape to protect it from getting electroplated and to protect devices from getting into contact with the electroplating solution. Do not use blue dicing tape as it reacts with the electrolyte.

(ix) Electrodeposition of Ni - target: 3 µm

Electrolyte Preparation

(a) Dissolve 350 g/liter of nickel sulfamate solution in water stirred at 40°C. Add 30 g/liter of boric acid and stir until it dissolves. Then add 30 g/liter of nickel carbonate and stir for 1 hour. Switch off the heat and let the solution settle down for 24 hours.

(b) Mix the solution continuously and let it settle for around 2 hours.

(c) Filter the solution by using Whatman's filter papers to filter out large particles still in the solution.

(d) Measure the pH and ensure that it is between $4-5$. If the pH is too high, lower it by adding 10 ml of sulfamic acid and re-measure after $3-5$ minutes. Repeat until the PH is within the accepted range. If it is too low, add 5 grams of sodium carbonate and stir well. However, this might introduce particles that have to be filtered out once the pH is stabilized. Measure to check the pH just before use as it might drift with time.

Electroplating Procedure

(e) Set the bath at 40°C and stir continuously. Ensure stirring does not cause bubbles.

(f) A bar of 99.9% purity Ni is used as the anode. This is cleaned using DI water, inseted into the electrolyte and connected to the positive terminal of a function generator such as Keithley 6221.

(g) The sample is now wet with DI water and then clipped to the negative terminal of the function generator using 'crocodile clips' and aluminum foil. The sample is then inserted into the electrolyte solution.

(h) Current is set at 15 mA and the deposition rate of Ni is $\sim 1.2\mu m/hr$.

Removal of Seed Layer

(i) Strip photoresist once the deposition is complete using PRS 2000 solution for 5 hours at 90°C.

(j) The gold layer is wet etched using Transense GE-8148 Au etchtant solution. A test sample is used to calibrate the etch rate as this was found to be different than the once quoted by the manufacturer.

(k) The titanium film is left unetched on the surface due to risk of etching silicon dioxide during this step.

(x) High Energy Nitrogen Implantation.

The complete implant schedule and profile for the p-base implant is listed Table 4.2. Mount samples on a 5-inch Si carrier using carbon tape. The tape should be under the sample and not exposed. For high temperature implantation, the samples are de-mounted from the carrier wafer and solvent cleaned. The samples are then packed in separate boxes and shipped high temperature, high dose implant shown in Figure 4.55.

5. P+ Implant

Metal mask is used and is patterned by optical lithography using a laser beam write(Hiderberg ML150) in both active and tester areas.

(i) Strip the Ni mask using piranha solution, 10 minutes.

(ii) DI water rinse, 5 times.

(iii) Strip the polysilicon mask using $DI + HF + HNO_3$(1:1:4) for 5 minutes,

(iv) DI water rinse, 5 times.

(v) Solvent Clean. (refer to step.1i).

(vi) Optical Lithography

(a) Mask#III: 'p-plus-optical'

(b) Dehydrate bake, 110°C for 5 mins.

(c) Cool on heat sink.

(d) Spin coat LOR3B at 2000 rpm(thickness:400nm) for 60 seconds.

(e) Soft bake on a hot plate 195°C for 3 minutes.

(f) Cool on heat sink.

(g) Spin coat LOR3B a second time at 2000 rpm (total thickness:800nm) for 60 seconds.

(h) Soft bake on a hot plate 195°C for 3 minutes.

(i) Cool on heat sink.

(j) Spin coat AZ1518 at 4000 rpm (thickness:1800nm) for 45 seconds.

(k) Soft bake on a hot plate 105°C for 1 minutes.

(l) Exposure: Dose of $230\mu Ccm^{-2}$ using a $405nm$ laser.

(m) Develop: Soak in AZ400K:DI water (80ml:300ml) for 30 seconds. Rinse in DI water immediately to stop the development.

MF26A is usually used to develop after exposure of AZ1518. However,sharper features were acheived using the AZ400K developer when the feature dimensions are lower than 3µm *. Here it is important to get the ratio of the developer to DI water exact and also to immediately rinse in DI water using the 'water gun' to stop the development.*

(n) De-scum in Branson O_2 Etcher.

- Power: 100W
- Gas: Ar/O2 ($140sccm/80sccm$).
- Time: 60 seconds.

(o) Evaporate Ti/Ni ($10nm/500nm$).

(p) Lift-Off

- PG remover solution, 4 hours

6. Implant Anneal

(i) Piranha Clean, 5 mins (removes Ni Mask).

(ii) BOE Etch, 2 mins (removes oxide)

(iii) Acqua Regia, 5 mins.

(iv) Piranha Clean, 15 minutes.

(v) Solvent Clean

(vi) Carbon Cap Formation

(a) Precondition a quartz tube ('blue-m') to a temperature of 250°C and flow nitrogen through the tube at maximum flow. This is done at least 1 hour prior to the next steps.

(b) Spin Coat AZ 1518 at 3000 rpm for 45 seconds.

Ensure no edge beads or gaps of photoresist at the corners and edges.

(c) Soft bake: 105°C for 3 minutes on hot plate.

(d) Switch the gas from argon to nitrogen in the 'blue-m' chamber.

(e) Increase temperature slowly from 105°C to 150°C at a ramp rate of 5°C per minute.

(f) Transfer to the 'blue-m' quartz tube in argon ambient.

(g) Ramp up temperature of the tube from 250°C to 650°C.

(h) Anneal for 30 minutes at 650°C.

(i) Cool down tube to $\sim$ 200°C and unload tha sample.

If the process is done right, the surface of the sample is black with a mirror-like finish.

(vii) Implant Anneal

(a) Load samples into Epigress CVD chamber (follow tool specific SOP).

(b) Anneal Tempearature: 1700°C

(c) Anneal Time: 20 minutes.

(d) Ambient: Argon at 400 mbar and flow rate of 4 slm.

(viii) Carbon Cap Removal

Oxidation is done to 'burn-off' the carbon. This is done in blue-m chamber.

(a) Oxidation Temperature: 900°C.

(b) Oxidation Time: 1 hour.

(c) Ambient: Dry O_2.

(ix) Piranha Clean, 15 minutes

7. Trench Etch

Trigate Gen-1 samples have a trench depth of 2µm. *Multiple test samples are loaded along with the trigate samples during the trench etch to measure etch rates and also spatial variation of the etch depth across the carrier wafer.*

(i) Solvent Clean.

(ii) Sacrificial Oxide - Target: 30nm (refer step.3i)

(iii) Electron Beam Lithography

(a) Mask#IV: 'trench e-beam'.

(b) Dehydrate bake: 100°C, 5mins

(c) Cool on heat sink

(d) Resist: PMMA A6 - spin coat: 4000rpm (400nm) for 60sec.

(e) Soft bake: 180°C for 3 mins.

(f) Dose: $1300\mu Ccm^{-2}$ at 100kV and 30nA in the JOEL JBX 8100FS (dose test run carried out with dose in the window of $1200-1400\mu Ccm^{-2}$ just before the actual run with trigate samples)

Proximity correction is applied during the e-beam write. Also lowest possible beam current is used to reduce line edge roughness. Any roughness in the pattern gets transferred to the Ni mask and eventually to the trench shape and sidewall roughness.

(g) Develop: MIBK:IPA (1:3) for 60 seconds. IPA rinse is used to stop the developement.

(iv) Barrel Etch.

(a) Power: 100 W

(b) Gas: O_2/Ar : $140sccm/12sccm$

(c) Pressure: 1 Torr.

(d) Time: 30 seconds.

(v) Evaporate Ti/Ni (15 nm/200 nm).

(vi) Lift-off (refer to step.5(vi)o).

(vii) Optical Lithography

(a) Mask#V:'Trench Optical'.

(b) Dehydrate bake: 100°C, 5mins

(c) Cool on heat sink

(d) Resist: AZ9260 - spin coat: 3000rpm for 60sec

(e) Soft bake: 113°C for 6 mins.

(f) Dose: $510mJcm^{-2}$ in the Hiderberg maskless aligner.

(g) Develop: AZ400K:DI water (1:3) for 3minutes and 20 seconds.

(h) Rinse in DI water, 5 times.

(i) Dry with N_2 gun.

(j) De-scum using Branson O_2 asher.

- Atmosphere: 1 Torr, Ar/O_2.

- Time: 2 minutes. Power: 100W.

(viii) Trench RIE Etch

i. Sample Loading

- Sample is mounted onto 4-inch silicon carrier wafer with Santovac at 70°C on a hot plate.

  The viscosity of Santovac is very low, so a few drops of Santovac is sufficient to cover all over the backside. Santovac is a good thermal conductor and helps in uniform thermal distribution and heat removal form the sample during the RIE etch. The trench etch is aggressive and therefore temperature during the etch is an important factor that could cause large variation.

- Test samples are loaded along with trigate samples to measure etch rate and trench depth.

ii. Trench Etch

*Test samples with fin-spacing (*5µm*) are processed just prior to the trigate samples. The trench depth is measured and the etch rate is calibrated. The trench depth varies with fin-spacing and therefore and a factor of 0.64 correction to the trench depth of the test samples is applied to obtain the trench depth of the denser (*0.5µm*) pattern in the trigate samples.*

(a) STS-AOE ICP-RIE.

(b) Trench etch is done in multiple steps of short duration each.

(c) Gas: SF_6/Ar - 20 sccm / 10 sccm

(d) ICP Power: 2800 Watts

(e) Bias Power: 100 Watts

(f) Pressure: 2 mtorr

(g) Time: 6.5 minutes

8. Solvent Clean.

9. RCA Clean

10. Sacrificial Oxide - Target: 30nm (refer step.3i)

11. H_2 Etch

    One of the two Gen-2 samples described in this report undergoes the H_2 etch with the intention of smoothing SiC trench sidewalls.

    (i) Solvent Clean.

    This step is done immediately prior to loading into the Epigress CVD tool for the H_2 etch to ensure no particulates are present on the sample during the etch.

    (ii) Load samples into Epigress CVD tool.

    (iii) H_2 etch parameters

    Detailed process development and parameter discussion is discussed in Section 4.1.3.

    (a) Gas : Pure hydrogen.

    (b) Pressure: 150 mTorr.

    (c) Time: 3 minutes. (refer to 4.25 for process flow.)

12. Gate Oxide

    Poly-ox is used as the gate oxide and a detailed discussion of the process development is available in Section 4.1.3

    (i) Sample Clean

    Cleaning of the sample is done immediately prior to the poly-ox process. Unreliable and below optimal results have been observed without this step.

    (a) Solvent Clean.

    (b) Piranha Clean, 15mins.

(c) Acqua Regia, 15 mins.

(d) RCA Clean.

(e) BOE+HCl(1:1), 5 minutes.

(f) Solvent Clean.

(g) RCA Clean.

(h) Rinse thoroughly in DI water, 10 times.

(i) Soak samples in IPA.

(ii) Polysilicon Deposition.

(a) LPCVD Protemp tube# 6 is used.

(b) Run the recipe: 'Poly-Polyox' and wait until tube completely purges.

(c) Once purged, remove samples from IPA and blow dry with N_2.

(d) Immediately load the samples into the polysilicon deposition tube and pump down.

- *Use clean tweezers that are dedicated for gate oxide only. Tweezers should not have carbon, plastic or teflon tip.*
- *Use a clean solvent glove and pull up the glove above the arm-sleeve of cleanroom gown.*
- *Make sure not to extend arm over and across the quartz boat. Load the samples by extending the tweezers out front. This reduces risk of sodium contamination.*
- *Loading the large wafers such that they lay flat on the boat with the Si-face facing up gives higher spatial uniformity as compared to loading the conventional vertical direction.*

(e) Deposition Parameters:

- Gas: SiH_4
- Pressure: 150mTorr
- Temperature: 580°C.

- Time: 72 seconds

(f) Keep samples inside with the tube pumped down until the oxidation tube is ready to be loaded.

(iii) Thermal Oxidation

(a) Pyrogenic oxidation tube# 1 is used for gate oxides only.

(b) Vent the polysilicon tube.

(c) Once the polysilicon tube is compeltely vented, extract the loading arm from the tube and at the same time run recipe 'Oxi-Polyox' on the oxidation tube.

(d) Unload the samples from the polysilicon tube.

Similar procedure as in step.12(ii)d is followed..

(e) Samples are immediately loaded into the oxidation tube.

(f) Thermal oxidation parameters.

- Temperature: 1000°C.
- Ambient: Wet oxidation - pyrogenic.
- Time: 7 minutes

(g) High temperature anneal.

> Temperature: 1100°C.

> Ambient: Argon

> Time: 60 minutes

(h) Re-oxidation

- Temperature: 900°C.
- Ambient: Wet oxidation - pyrogenic.
- Time: 120 minutes

(i) Cool down tube to 400°C.

(j) Let the samples stay in the oxidation tube until the NO anneal tube is ready to be loaded.

(iv) NO Anneal

(a) Set temperature of tube to 150°C and purge with argon for 2 hours before loading samples.

(b) Load samples directly from oxidation tube.

(c) Anneal temperature: 1175°C

(d) Anneal time: 2 hours.

13. Polysilicon Gate

Samples are unloaded from the NO anneal tube and immediately loaded into the polysilicon LPCVD tube. Test samples are prepared by solvent, piranha and BOE etch to go along with the trigate samples in the LPCVD tube.

(i) Purge LPCVD polysilicon deposition tube.(Protemp tube# 6).

(ii) Once completely purged, extract the loading arm and now unload samples from the NO anneal tube and load them to the LPCVD tube immediately.

Follow the loading procedure described in step.12(ii)d.

(iii) Polysilicon Deposition (LPCVD) - Target:1µm

(a) Equipment: Protemp tube# 6.

(b) Deposition Temperature: 630°C

(c) Deposition Rate(@630°C): 12.3 nm/min. (test run carried out just before the actual run with trigate samples to determine/calibrate the depostion rate.)

(d) Deposition time(@630°C): 82 minutes.

(e) Measured thickness of polysilicon film: 1.1µm

(iv) Polysilicon Doping.

Phosphorous is used to dope the polysilicon gate and the dopant is spin coated onto the sample. To increase the shelf life, the spin-on dopant solution is stored in the refrigerator using small 5ml plastic bottles.

(a) Place the spin-on bottle in a solvent hood for 3 hours prior to spin coating.

High sheet resistances have been observed if the dopant is not at room temperature while spin coating. This could be due to condensation on the surface that degrades the active dopant concentration. Also, black particulates are observed in film if the dopant is not at room temperature. These particulates do not seem to affect the sheet resistance but they do not get etched away during the polysilicon RIE etch. Do not leave the solution outside the refrigerator for more than 24 *hours.*

(b) Start recipe 'polygate-dope-trigate' in protemp tube#8. It takes about 1 hour to ramp up to 800°C.

(c) Now unload the sample from the LPCVD polysilcon deposition tube.

(d) Solvent clean.(refer step.1i)

(e) BOE etch, 2 mins

(f) Piranha soak,2 mins.

Piranha clean is done just before spin coating the dopant to ensure the surface of the sample is hydrophilic.

(g) Dehydrade bake, 5 minutes on hot plate. Now set the hotplate to 200°C.

(h) Spin coat dopant

> Step 1: Spin at 500 rpm for 2 seconds.

> Step 2: Spin at 3000 rpm for 17 seconds.

Dopant is applied using a clean and dry plastic pipette. Inconsistent results have been onserved using the glass pipette and therefore not recommended. If glass pipette has to be used, dehydrate bake the pipette at 110°C *and cool down by continuously blowing* N_2 *before use. During spinning, every surface of the spinner tool is covered by aluminum foil to prevent any toxic SOD exposure to the tool.*

(i) Bake sample at 200°C for 20 minutes.

Immediate transfer between spin coat chamber and hot plate is important. Some vapours are usually generated when placed on the hot plate and therefore fair distance of personnel from the hot plate is recommended.

(j) Load samples into the 'drive-in' tube#8 that was heated to 800°C in *step*.13(*iv*)*b* using special heat resistant gloves.

(k) Drive in at 950°C for 2 hours in argon(80%) and oxygen(20%) ambient.

(l) BOE Etch, 5 minutes.

(m) Measure Sheet Resistance.

When measured using the 4-point probe, the sheet resistance is usually between 50Ω - 100Ω *per square.*

(n) Repeat Polysilicon Doping(step.13iv).

(o) BOE Etch, 5 minutes.

Polysilicon gate is now doped two times.

When measured using the 4-point probe, the sheet resistance is usually between 10Ω - 40Ω *per square.*

(v) Polysilicon Gate Pattern.

(a) Electron Beam Lithography.

(b) Mask#VI - 'gate-ebeam' for active area only.

(c) Solvent clean.

(d) Dehydrate bake, 120°C for 3 minutes.

(e) Cool down on heat sink.

(f) Spin coat CSAR resist at 4000 rpm for 60 seconds.(thickness: 400nm)

(g) Soft bake at 150°C for 3 minutes.

(h) E-beam lithography is done using JEOL 8100FSX with a dose of $300\mu C/cm^2$ and a beam current of 30nA.

Alignment of the feature to the p-base is very important at this step and therefore higher beam currents are not used. Alignment is a challenging at this step due to the roughness of the polysilicon. Increase the width of scan and smoothing of the alignment edge calculation to get good alignment.

(i) De-scum in Branson O_2 etcher.(refer to step.5(vi)n)

(j) Polysilicon etch, total time: 2 minutes and 10 seconds. (refer to step.3iv).

A total of 1.4µm *is etched, recessing* $\sim 400nm$ *of polysilicon inside the trenches.*

(k) Soak in PG Remover, 80°C for 5 hours(strip CSAR resist).

(l) Optical Lithography.

(m) Mask#VII - 'gate-optical' for field and tester areas.

(n) Solvent clean.

(o) Dehydrate bake, 110°C,3 minutes.

(p) Cool on heat sink.

(q) Spin coat AZ9260 at 4000 rpm for 60 seconds.

(r) Soft bake at 110°C for 5 minutes.

(s) Expose with dose of $510mJ/cm^2$ using 405nm laser in the Hiderberg MLA writer.

(t) Develop using AZ400K:DI water(80ml : 300 ml) for 3.5 minutes.

(u) De-scum using Branson O_2 asher.(refer to step.5(vi)n).

(v) Polysilicon etch, $2mins, 10seconds$.(refer to step.3iv)

14. Thermal Oxidation for Inter Layer Di-electric.

(i) Solvent Clean.

(ii) RCA Clean

The BOE etch is not done as part of the this RCA clean.

(iii) Thermal Oxidation - target:1µm

- Protemp Tube# 4.
- Temperature: 1100°C
- Ambient: Wet-Pyrogenic
- Time: 205 minutes

15. Source/Drain Ohmic Contacts

(i) Front Side Nickel Deposition and Anneal

(a) Mask#VIII: 'ohmic'

(b) Solvent clean.

(c) Dehydrate bake,110°C, 3 minutes.

(d) Spin coat LOR3B at 2000 rpm,45seconds.

(e) Soft bake at 190°C,5 minutes

(f) Spin coat AZ1518 at 4000 rpm, 60 seconds.

(g) Soft bake at 105°C,2 minutes.

(h) Exposure dose of $230mJ/cm^2$ with the 405nm laser in the Hiderberg MLA.

(i) Develop in MF26A for 30 seconds.

(j) De-scum in brasnson O_2.(refer to step number.5(vi)n)

This step is to remove photoresist residue from the developed windows.

(k) BOE etch,50 seconds.

o *This wet etch removes the* $\sim 45nm$ *thick gate oxide over the source regions to be silicided. A careful calibration of the etch rate using a test sample is necessary to ensure the oxide is completely removed while the ILD oxide and undercut are kept at a minimum.*

- o *The source pads can be electrically probed at this point and checked for electrical continuity to ensure all the oxide is etched. A slight overetch of* $\sim$ 10 *seconds after this point can be done to ensure all oxide is removed.*

(l) SiC RIE

This step is intended to increase the surface roughness and thereby surface area of the exposed SiC surface that could lead to lower contact resistivity.

- Equipment: Jupiter RIE
- Gas: SF_6/Ar:(20 sccm/10 sccm).
- Power: 100 Watts.
- Pressure: 195 mTorr.
- Time: 20 seconds.

Expect to etch around 10nm of SiC.

(m) De-scum in brasnson O_2.(refer to step number.5(vi)n)

This step is to removes any polymers that may have formed during the RIE etch.

(n) BOE etch, 20 seconds.

(o) Evaporate 50nm of nickel at 1.5 $\text{Å}\,\text{s}^{-1}$ with the chamber pressure at 2.2×10^{-7} torr.

(p) Lift-off metal in PG remover at 60°C for $4 - 5$ hours.

(ii) Ohmic Anneal at 750°C - Step 1

The following procedure is specific to the Jiplec Jetfirst 2100 RTA

(a) Turn on the Jiplec and let it warm and stabilize for 15 minutes.

This step avoids the 'water cooling station error'

(b) Clean 6-inch silicon 'carrier' wafer and a quarter of 4-inch 'base' sample.

'Base' sample is a $Si - SiO_2$ sample that is preferably prepared by thermal oxidation of a clean silicon sample. The size of the 'base' sample must be larger than the sample to be annealed.

> Solvent clean.

> Piranha soak, 15 minutes.

> Acqua regia, 15 minutes.

(c) Load the 6-inch silicon carrier wafer.

(d) Run 'recipe-1' to purge the chamber with N_2 for 30 mins.

recipe path- C:ProgramFiles/Jetfirst/recipe/studentspecial/rahul/ohmic

(e) Cool down and do not open the chamber.

(f) Run 'recipe-2' to bake out the chamber at 250°C.

(g) Open chamber and place the 'base' sample with Ti pellets as shown in Figure 4.47.

(h) Run 'recipe-3' to pump and purge the chamber multiple times at 250°C.

(i) Run 'recipe-4' to pump and purge the chamber multiple times at 500°C.

(j) Cool down and do not open the chamber.

(k) Run 'ohmic-750°C' to mimic the ohmic anneal without the real samples loaded. Ensure good PID control and temperature stabilization.

(l) Now load the samples to be annealed face-down onto the 'base sample'.

(m) Run 'recipe-2'.

(n) Cool down and do not open the chamber.

(o) Run 'ohmic-750°C'. Ohmic anneal at 750°C for 3 minutes in argon ambient.

(p) Piranha soak, 7 minutes to remove non-silicided nickel over ILD.

(iii) Back Side Nickel Deposition and Anneal

(a) Solvent clean.

(b) Spin coat AZ9260 on the front surface at 2000 rpm for 60 seconds

(c) Soft bake at 110°C for 6 minutes on hot plate

(d) Hard bake at 155°C for 10 minutes.

(e) BOE dip,3 minutes.

(f) Polysilicon etch,2.5 minutes.(refer to step#3iv).

(g) De-scum in Branson O_2 asher. (refer to step#5(vi)n).

(h) BOE etch, 5 minutes.

(i) Polysilicon etch,1 minute.

(j) BOE etch, 1 minute.

(k) Evaporate 100nm of Ni on the back surface at a rate of $1.5 \text{Å}\,\text{s}^{-1}$ and a pressure of $1 \times 10^{-7} torr$.

(l) Strip off the resist from the front surface using a PG remover soak for 5 hours.

(iv) Ohmic anneal at 1000°C – $Step2$

This anneal is done to obtain low contact resistivity.

(a) High temperature anneal is done at 1000°C following the procedure outlined in step.15ii.

(b) Load the sample with the backside facing up.

Ensure to check the PID control multiple times because temperature overshoot could cause the carrier sample to crack and disrupt the temperature reading.

(v) Post Anneal Treatment.

i. Solvent Clean.

ii. O_2 RIE using Jupiter III.

(i) Gas O_2 at 50 sccm.

(ii) Pressure 300 mTorr

(iii) Power 200 Watts

(iv) Time $2-3$ minutes

16. Gate Contact

(i) Optical Lithography

(a) Mask#IX 'ILD opening'.

(b) Solvent clean.

(c) De-hydrade bake at 110°C for 1 minute.

(d) Cool down on heat sink.

(e) Spin coat AZ9260 at 4000 rpm for 60 seconds.

(f) Soft bake at 110°C for 6 minutes.

(g) Expose with dose of $503mJ/cm^2$ using the 405nm laser in the Hiderberg MLA writer.

(h) Develop using AZ400K:DI water(80ml:300ml) for 3 minutes and 15 seconds.

(ii) De-scum using Branson O_2 asher.(refer step#4(viii)j)

(iii) ILD Opening - SiO_2 etch

(a) Load sample onto 6-inch Si carrier wafer using crystal bond.

(b) Gas: $CF_4 : CHF_3$ - 10 sccm/40 sccm.

(c) ICP power: 650 watts

(d) Bias power: 50 watts

(e) Pressure: 1 pascal.

(f) Time: 5 minutes, 20 seconds. (450nm of SiO_2 etched)

(g) Unload sample from carrier wafer.

(iv) DI water rinse.

(v) BOE etch, 1 minute.

(vi) PG remover soak, 6 hours.

17. Top Metal

(i) Solvent clean.

(ii) Sputter 50 nm of titanium at 1.5 nm/min using 150 watts and chamber pressure of 7×10^{-7} torr.

(iii) Cool down and do not break vacuum.

(iv) Sputter 1µm of gold at 7.2 nm/min using 75 watts and chamber pressure of 1×10^{-6} torr.

(v) Optical lithography using mask#X and procedure in step#16i.

(vi) Wet etch the gold film in the resist windows using GE-8148 from Transene.

- *Etch rate is $\sim$ 7 nm/min at room temperature.*
- *The chemical does not yield a uniform etch if expired. Use test samples to verify etch rate.*
- *A number of particulates are found to deposit on the surface at the end of the etch. This can be minimized by soaking the sample either face down or sideways in the solution and performing a thorough DI water rinse immediately after the acid soak.*

(vii) Wet etch titanium using TFTN from Transene at 70°C for 6 minutes.

A teflon coated thermocouple is used to accurately measure the temperature of the etchant as the etch rate becomes erratic at temperature greater than 80°C.

18. Measure Devices!!

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