

INFLUENCE OF SIZE AND INTERFACE EFFECTS OF SILICON NANOWIRE
AND NANOSHEET FOR ULTRA-SCALED NEXT GENERATION
TRANSISTORS

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To my family.

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SYMBOLS

m	mass
v	velocity
Ψ	wave function
h	Plank's constant
q	charge
e	charge of electron
\hbar	reduced Plank's constant
Z	atomic number
E	energy
V	Coulomb potential
λ	eigen value
ν	vibrational frequency
\hat{H}	Hamiltonian
\hat{T}	kinetic energy
E_g	bandgap energy

ABBREVIATIONS

FET	field effect transistor
DFT	density functional theory
NBTI	negative bias temperature instability
GAA	gate all around
MBC	multi bridge channel
NW	nanowire
NS	nanosheet
DOS	density of states
QC	quantum conductance
MOS	metal oxide semiconductor

ABSTRACT

Sikder, Orthi. M.S.E.C.E., Purdue University, August 2020. Influence of Size and Interface Effects of Silicon Nanowire and Nanosheet for Ultra-Scaled Next Generation Transistors. Major Professor: Dr. Peter J. Schubert.

In this work, we investigate the trade-off between scalability and reliability for next generation logic-transistors i.e. Gate-All-Around (GAA)-FET, Multi-Bridge-Channel (MBC)-FET. First, we analyze the electronic properties (i.e. bandgap and quantum conductance) of ultra-thin silicon (Si) channel i.e. nano-wire and nano-sheet based on first principle simulation. In addition, we study the influence of interface states (or dangling bonds) at Si-SiO₂ interface. Second, we investigate the impact of bandgap change and interface states on GAA-FETs and MBC-FETs characteristics by employing Non-equilibrium Green's Function based device simulation. In addition to that we calculate the activation energy of Si-H bond dissociation at Si-SiO₂ interface for different Si nano-wire/sheet thickness and different oxide electric-field. Utilizing these thickness dependent activation energies for corresponding oxide electric-field, in conjunction with reaction-diffusion model, we compute the characteristics shift and analyze the negative bias temperature instability in GAA-FET and MBC-FET. Based on our analysis, we estimate the operational voltage of these transistors for a life-time of 10 years and the ON current of the device at iso-OFF-current condition. For example, for channel length of 5 nm and thickness <5 nm the safe operating voltage needs to be <0.55V. Furthermore, our analysis suggests that the benefit of Si thickness scaling can potentially be suppressed for obtaining a desired life-time of GAA-FET and MBC-FET.

1. INTRODUCTION

Over the last few decades, nanotechnology has considerably improved and revolutionized almost every technology and industrial sectors including electronics, information technology, medical and healthcare, energy, environmental remediation, transportation and so on. In modern world, every technology giant is making use of big data technology for gaining insight and making strategic decision to any problem. In order to keep these progresses going and to unveil the actual power of data, we are compelled to look for the appropriate hardware level technology that can handle the heavier computation at higher speed. The electronic transistor and the microchip are the very basic tools, which make all modern electronics possible.

1.1 Evolution of Transistor Structures

The ideal characteristic of a transistor starts with high ON/OFF current ratio and low leakage. High ON current ensures high speed operation, low OFF current ensures low leakage and thus both of them contribute to a high ON/OFF ratio. To ensure these features while keeping the power consumption low, shrinking down the size of transistor is required. The size of a transistor is determined by its gate length or the distance between source and drain. We now know that for attaining the best performance from FETs, we need to adhere to the devices of smaller size. Not only that, the cost of manufacturing for a given process is also dependent on the size as the cost of manufacturing is determined by the required area of Silicon. Either way, a smaller sized device makes the most of gain. With that in mind, various transistor structures have been explored over the decades to get the best out of this device. The initial and most widely accepted structure is Planar FET. As already mentioned, by reducing the gate length, down scaling is achieved, but with this, some issues like:

short channel effect, drain induced barrier lowering (DIBL) starts to appear. Such concerns dim the difference of OFF state and ON state current. In addition, the scalability of Planar structure is limited by 25 nm as reported by TSMC Deputy Director Jin Cai [1].

To keep the Moore's law going [2], other structures like Double gate FETs and FinFETs have been being explored. While eventually by down sizing, double gate FET is hindered by similar challenges like Planar FETs, FinFETS demonstrate a reasonable performance with respect to scaling. The FIN provides gate contact over three surfaces ensuring better electrostatic, also by reducing the width the device size gets smaller without much short channel effect or DIBL concern. However, as the device size gets shrunked another concern that comes into play is interface scattering. With the fin width decreasing, the carrier mobility in the device is worsened due to interface scattering and quantum confinement. In addition, the FinFET is challenged by quantization limit since fractional fins are not possible. Hindered with all these challenges, newer device configurations are intensively explored with the target of harnessing the utmost benefits from nanostructures (i.e. wire, sheet, slabs) with newer designs [3], [4]. Gate-all-around-FET and multi-bridge-channel-FET are two of the few designs proposed by implementing nanowire and nanosheet as channels as ultra-scaled next generation transistors. Our focus in this work is based on investigating these two transistors, which are subjected to introduce ultra-scaling era in the next phase of transistor technology.

1.2 Silicon Nanowire/Nanosheet Next Generation FETs

GAA-FET and MBC-FET both are gate all around transistors based on nanowire and nanosheet, respectively. As the transistor size continues to shrink, nanowires and nanosheets contain the advantage of having smaller channel and high surface to volume ratio. Besides, these transistors have several benefit over the current leading FinFET technology. The gate-all-around architecture shows some similarities with the

FinFET architecture. In GAA-FET, the nanowire channel is surrounded with gate in all direction. As a result, it provides a great electrostatic gate control. Thus, GAA-FET is a perfect candidate to push the scalability flow to the sub 7nm node regime introducing an era of ultra-scaled transistor. IBM has successfully demonstrated 5nm process technology using GAA-FET [int-ref]. A Multi Bridge Channel Field Effect Transistor (MBC-FET) is nanosheet based GAA-FET. They are architecturally similar except the fact that MBC-FET uses nanosheets as channel instead of nanowires. It is registered under Samsung Electronics in the US where they have announced MBC GAA-FET under 3nm process technology. For design and structural reason MBC-FETs associate with several advantages. First, the nanosheets can be stacked vertically which improves speed without additional area footprint. Second, they are really compatible to the current technology (FinFET) as they share the same manufacturing process. For the same reason, in the existing designs MBC-FETs can replace FinFETs making the transition smooth.

1.3 Challenges due to Scaling and Motivation

The transistor dimensions have already touched a number of physical limits due to the extreme down-scaling. As a result, both the manufacturing process and the transistor designs are facing challenges to keep up with the scaling while maintaining a reasonable performance. In this section, we overview the technical challenges caused by the excessive down-scaling of transistors. Hence, we describe our key motivation to address those questions through our research effort.

Generally, geometrical scaling of transistor refers to the scaling of area (width, length). However, since oxide capacitance is proportional to the ratio of area and oxide thickness, if the oxide thickness is not scaled along with area, then the capacitance would increase. An increased capacitance will impact transistors threshold voltage and ON/OFF aspects. As a result, oxide thickness is required to be scaled. Nevertheless, due to quantum effect like tunneling, oxide thickness scaling is restricted by

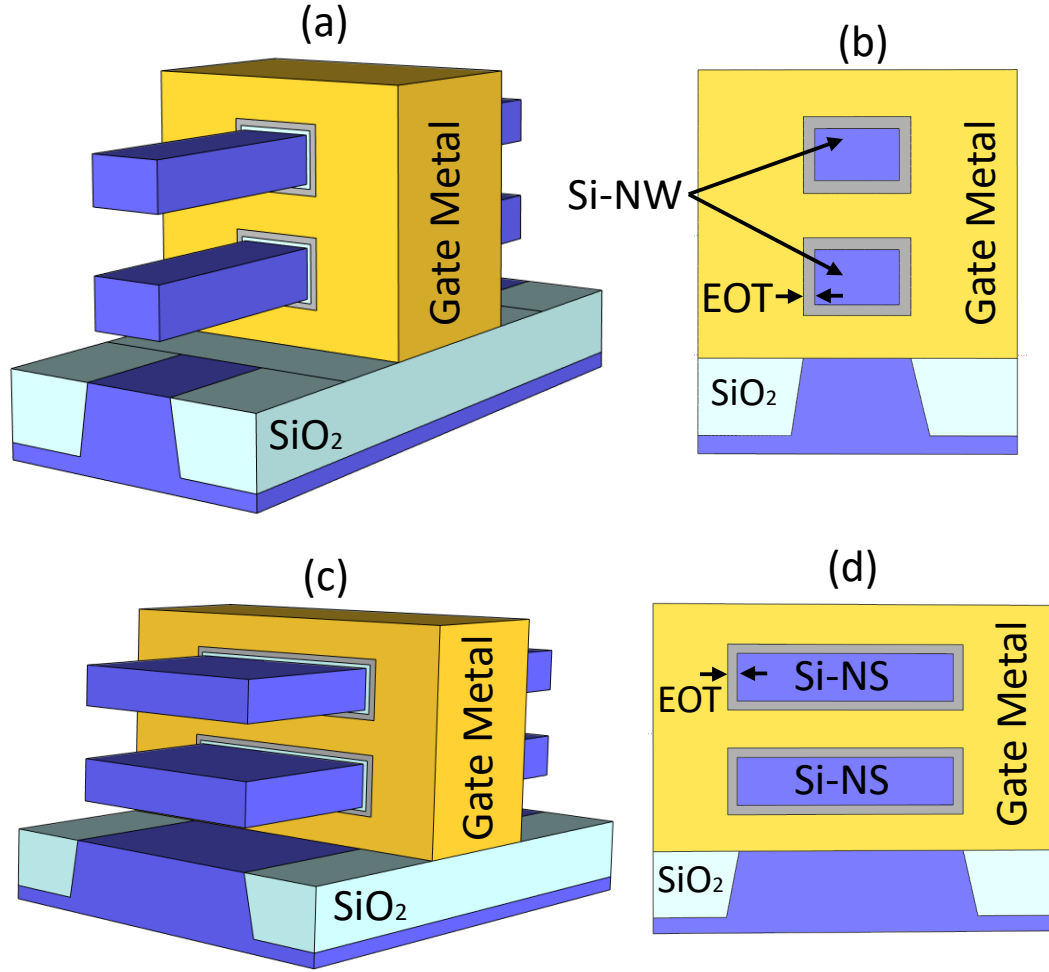


Fig. 1.1. GAA-FET (a) structure and (b) cross sectional view with Si-Nanowire (NW) channel. MBC-FET (c) structure and (d) cross sectional view with Si-Nanosheet (NS) channel.

certain value so that it does not lead to abrupt increase in leakage current. In addition, the gate voltage cannot be down-scaled at the same manner. Since oxide electric field is the ratio of supply voltage and oxide thickness, a scaled thickness with similar supply voltage will lead to large oxide electric field leading to degradation processes like bias temperature instability and so on. The earlier devices with thicker oxide thickness used to be less impacted by these kind of degradation processes. These as a whole generate a reliability concern.

These geometrical scaling give rise to various fabrication challenges like short channel effects, drain induced barrier lowering etc. Also, channel leakage current increases considerably.

Another concerning issue due to scaling is the variance of factors between a batch of device. Although variance has always been a process and fabrication consequence for transistor, but in case of ultra-scaled transistor even a small difference has a larger percentile change value. For example, in comparison with the larger devices, ultra-scaled transistors include very few numbers of Si-H bonds and Si-O bonds. The slightest deviation in this number/type of bonds will result in overall difference in charge density and current flow. In addition, due to the fabrication difficulty for scaling, the variability in device dimensions increases. Thus, even with the same process technology the transistors show major variance in their characteristics while operating in circuits.

In short, the problems due to scaling of challenges can be summarized as following:

- Due to scaling band gap increases which leads to decrease in mobile carrier concentration and potentially decrease in device current drive.
- We speculate that, due to the ultra scale size of the device, the defect state formation and its influence becomes so significant that it may require particular attention.
- Scaling becomes challenging due to interface randomness induced variability.
- Due to the defect states presence, the reliable operation of device can be challenging. Therefore, we expect a trade-off between scalability and device reliability.

1.4 Contribution

Unlike Planar FETs, in nanowire and nanosheet transistors, channels obtain finite size effect. Hence, their behavior and characteristic need to be explored extensively

while utilizing them as transistor channel in the current technology. The prior works only investigated the bandgap structures of Si systems. But for exploring finite size effects on channels and insights to transistor characteristics, considering Si/SiO₂ interfaces will be more relevant. In addition, being ultra scaled in size, the role of interface states interference becomes significant while evaluating device operation and reliability. Hence, investigating the band structures and quantum of conductance are required along with density of states. Also, prior works assume the defect formation energies as constant while we speculate these energies being dependent on channels size and oxide electric field.

Therefore, to validate our argument and scientifically verify our speculation, we have performed the following analysis:

- First Principle (DFT) Simulation
 - Si-NW and Si-NS properties
 - Defect state formation
- Self-consistent Device Simulation
 - Effect of scaling on GAA-FET and MBC-FET
 - Effect of defects in OFF state current

- Reliability Analysis
 - Optimal operational voltage
 - Lifetime prediction.

Our contribution of this work can be briefly described as below:

- We have explored the electronic bandgap structures of $\text{SiO}_2\text{-Si-SiO}_2$ systems (for both nanowire and nanosheet) along with H-passivated Si systems.
- We have investigated the influence of interface defect states through density of states, band structure, quantum of conductance despite utilizing only density of states as shown in the previous works.
- We have computed the influence of defects in ballistic current using Landauer-Buttiker formalism and discussed the effect of defects in OFF state current.
- We have studied device properties through self-consistent Schrodinger-Poisson simulator considering the band gaps found from our study to see the scaling effect (nanowire/nanosheet thickness downsizing) on device performance.
- We have evaluated the activation energy barriers for formation of interface defects for nanowire/ nanosheets of different thicknesses and explored its relation to oxide electric field.
- We have considered the electric field and thickness dependent activation energy in the reaction-diffusion model, despite using previously used constant activation energy. This provides more accurate calculation of density of defects and shift in threshold voltage.
- Finally, by considering a failure criteria on the threshold voltage shift with respect to oxide electric field, we find a predicted lifetime and optimum operating voltage to reach the targeted lifetime.

1.5 Thesis Outline

This thesis is divided into the following chapters:

- Chapter 1 discusses the evolution of fundamental block-unit of semiconductor industry: field effect transistors. Section 1.1 shows how the continued scaling growth has led the integrated circuit industry to explore various structures of FETs. Section 1.2 briefly introduces the newly launched next generations ultra-scaled transistors like GAA-FETs, MBC-FETs and so on. Section 1.3 discusses the potential challenges due to scaling and interface defects. Section 1.4 briefly describes the motivation and contribution of the work. Section 1.5 outlines the chapters in the thesis.
- Chapter 2 discusses the fundamentals of density functional theory (DFT) which is used for atomistic simulation of transistors channel materials and interface properties in the later chapters. Section 2.1 revisits the approximations and theories that eventually lead to the development of the ab-initio first principle study. Section 2.2 discusses the required key concepts of plane wave DFT computation used in this work. Section 2.3 analyzes the use of maximally localized Wannier functions (MLWF) highlighting the Wannier transformation and maximal localization. The MLWFs are implemented through the Wannier90 code in conjunction to DFT package to produce the transport properties along with the computation of electronic structures of practical size devices.
- Chapter 3 describes our work to investigate the materials electronic structure. We use DFT for the purpose. Section 3.1 explains the computational set up used for DFT simulations. Next, it describes the structural optimization of nanowire and nanosheet structures and their band structures without defects. Section 3.1 shows the results of intensive study on the NWs and NSs of various thickness through the energy dispersion relation and shows the comparison of bandgap while showing the effect of scaling of the channels thickness. Section 3.2

shows the interface defects in nanowire and nanosheet through band structure and quantum conductance and evaluate Ballistic current with the presence of interface defects.

- Chapter 4 explores the influence of quantum confinement due to scaling and interface trap due to defect states in the operation of ultra-scaled transistors character. Section 4.1 describes the device simulation methodology through non-equilibrium Greens function (NEGF) formalism in conjunction with solving Poisson's equation. Section 4.2 investigates the impact of Si bandgap in the characteristic of GAA-FET and MBC-FET and by comparing between their performance for different thickness of nanowire and nanosheet FETs explore the effect of scaling.
- In Chapter 5, the activation energy of Si-H bond has been explored. Section 5.1 describes the physical process of Si-H bond dissociation. Section 5.2 shows the computation of activation energy associated with Si-H bond dissociation. Finally, Section 5.3 analyze the correlation of the activation energy and the electric field in the SiO₂ layer.
- Chapter 6 focuses on time-dependent generation of defect states and evaluate transistor performance under that circumstance. Section 6.1 discusses the generation of defect states and analyze it in the context of scaling. Section 6.2 discusses the reliability concern NBTI and its mechanism. Section 6.3 shows a physical model for defect generation.
- Chapter 7 summarizes the thesis and offers attainable direction for future research work.

2. THEORETICAL BACKGROUND OF FIRST PRINCIPLE STUDY

For any atomic system, the Hamiltonian at equilibrium electron-electron and electron-ion interactions can be computed by DFT. We have opted for an hybrid scheme that relies on plane-wave DFT and a transformation of the output into a localized Hamiltonian to use as a key ingredient for solving NEGF equation. In this chapter the foundations of the DFT theory will be briefly revised.

In this chapter the theory for first principle simulation has been revised as well as the procedure for density functional theory (DFT) simulation for transistors made with homogeneous channel material Silicon has been discussed. The chapter is divided into the following sections: Section 2.1 describes the approximation and theoretical foundation for DFT, Section 2.2 describes the concepts for plane wave DFT calculation, Section 2.3 describes computation of Maximally Localized Wannier Functions for calculation of quantum conductance.

2.1 Density Functional Theory

Density functional theory (DFT) has been a popular form of computation used in last few decades, to investigate the electronic structure of solid state systems including bulk materials as well as atoms, molecules, interfaces, surfaces and nanostructures. The concept is to define a many body system not through many body wave function but through its particles density. The trick that is utilized in DFT is that the particle density in a N body system the degrees of freedom is reduced to spatial (three) coordinates from $3N$ degrees. As a result, the cost of computation becomes comparatively low than the conventional ways like Hartree-Fock approach, which is based on many-electron wave function. Although there has been a lot of progress in DFT,

there are still complications while using DFT in investigating some correlated systems and in calculations of the band gap of some semiconductors. For this reason, many new DFT methods are developed and designed by alterations to the functional or by the inclusion of additive terms.

2.1.1 The Many Body System & Born-Oppenheimer Approximation

A many body systems Hamiltonian consisting of nuclei and electrons can be expressed as [5]:

$$H_{tot} = -\sum \frac{\hbar^2 \nabla_{R_P}^2}{2M_P} - \sum \frac{\hbar^2 \nabla_{r_p}^2}{2m_e} + \sum_{P \neq Q} \frac{Z_P Z_Q e^2}{2|R_P - R_Q|} + \sum_{p \neq q} \frac{e^2}{2|r_p - r_q|} - \sum_{P,p} \frac{Z_P e^2}{|R_P - r_p|} \quad (2.1)$$

Here, p, q are indexes that operate on electrons and P, Q are indexes that operate on nuclei, r_p and R_P are positions for electron and nuclei respectively and m_e and M_P are masses of electrons and nuclei respectively. Z_P is the atomic number of nucleus P. The first two terms define kinetic energies of the nuclei and electrons, the next two terms describe potential energies for of nucleus-nucleus Coulomb Interaction and electron-electron Coulomb interaction and the last term in the equation describe the potential energy of nucleus-electron Coulomb interaction.

According to time-independent Schrodinger Equation:

$$H_{tot} \Psi(R_P, r_p) = E \Psi(R_P, r_p) \quad (2.2)$$

$$\hat{H} = \hat{T} + \hat{V} \quad (2.3)$$

Here, the energy operator \hat{H} is divided into the kinetic energy operator \hat{T} and coulomb potential operator \hat{V} respectively. This shows it is difficult to solve Schrodinger equation when there are bunches of electrons and nuclei that interact with each other. That is when in 1927 Born-Oppenheimer (BO) approximation was made by Born and Oppenheimer. The mass of nuclei is much larger than the mass of electrons (1836 times). So the moving speed of nuclei is much lower than the speed of electrons

(almost 2 order lower in magnitude). Since we can separate the movement of nuclei and electrons, we will consider the positions of nuclei are fixed while considering the movement of electrons. Thus, according to the Born-Oppenheimer approximation, the dynamics of atomic nuclei and electrons can be separated to write the total wave function as follow:

$$\Psi(R_P, r_p) = \Psi_N(R_P) * \Psi_e(r_p) \quad (2.4)$$

Our focus will be to solve the ground state of electrons for a fixed set of nuclei. As a result, the number of variables in the Schrodinger equation is reduced and it looks like the following:

$$\hat{H}\Psi(r_1, r_2, r_3, \dots, r_N) = E\Psi(r_1, r_2, r_3, \dots, r_N) \quad (2.5)$$

The importance of the BO approximation is that it separates the movement of electrons and nuclei. We can assume that the electrons are moving in a static external potential $V_{\text{ext}(r)}$ formed by the nuclei, which is the starting point of DFT.

2.1.2 The Kohn-Sham Equation

The significance of the Kohn-Sham Equation for DFT is immense. It is the contribution of this equation that made DFT calculation possible with even a single computer and became the most widely used tool for electronic structure calculation. In 1998, Kohn was honored with Nobel Prize in chemistry as a recognition of this contribution.

If we apply the BO approximation in the time independent Schrodinger equation, the Hamiltonian \hat{H} of the electronic wave function can be expressed in the following way [5]:

$$\hat{H} = \sum_p^N \underbrace{-\frac{1}{2}\nabla^2}_{\hat{T}} + \underbrace{\sum_p^N V(r_p)}_{\hat{V}} + \underbrace{\sum_{p<q}^N U(r_p, r_q)}_{\hat{U}} \quad (2.6)$$

Where N is the number of electrons, V is the external potential field generated by the fixed nuclei, \hat{T} , \hat{U} , \hat{V} denote kinetic energy, electron-electron interactions and

external potential respectively. If we are considering a fixed number of particles than the potential term \hat{V} is only system dependent.

The KS equation redefines an original many-body system by an auxiliary independent-particle system where it assumes two systems with same ground state density. It maps the original interacting system with real potential onto a fictitious non-interacting system whereby the electrons move within an effective Kohn-Sham single-particle potential $V_{KS}(r)$. The Hamiltonian for the auxiliary independent-particle can be written as [5]:

$$\hat{H}_{KS} = -\frac{1}{2}\nabla^2 + V_{KS}(r) \quad (2.7)$$

For a system with N independent electrons, the ground state is obtained by solving the N one-electron Schrodinger equations,

$$\left(\frac{1}{2}\nabla^2 + V_{KS}(r)\right)\Psi_p(r) = \varepsilon_p\Psi(r) \quad (2.8)$$

$$n(r) = \sum_p |\Psi_p(r)|^2 \quad (2.9)$$

where,

$$\int n(r)dr = N \quad (2.10)$$

there is one electron in each of the N orbitals $\psi_i(r)$ with the lowest eigenvalues ε_i .

2.1.3 The Exchange Correlation Functional

The Kohn-Sham ansatz does not consider any approximation, but in practice it is not possible to know the exact form of the exchange-correlation functional unless in the case of slowly varying densities or high densities. Again, it is important to have an accurate XC energy functional $E_{XC}[n(r)]$ or potential $V_{XC}(r)$ in order to describe a practical condensed-matter system. The most popular form of XC potential approximation is the local density approximation (LDA). Although LDA has been widely used to solve many quantum chemistry problems, it underestimates the band gap of most semiconductors to some extent. That makes the physical meaning of the

Kohn-Sham equations questionable. For improving the accuracy of the method, the gradient of the electron density is also taken into account along with the local density itself. In the generalized gradient approximation (GGA) the exchange-correlation functional is defined as the spatial integral of a function that depends both on the density and on the gradient of the density at a given point.

2.2 Plane Wave DFT

In our work, by DFT study we investigate the electronic properties of Si nanowire and Si nanosheet. Therefore, our study is performed over a set of atoms within a crystal which are periodic in one direction (nanowire) or two directions (nanosheet). This is the reason plane wave DFT is utilized for the materials study. The Bloch waves for a free electron in a periodic crystal is expressed as:

Where $U_k(r)$ is the positively charged nuclei periodic potential and $e^{ik}(r)$ is electrons plane wave in a crystal. The major concepts which are used in plane wave DFT calculation in general are discussed below.

2.2.1 Pseudo-potentials

The outer shell electrons of an atom are known as valence electrons. The characteristics and chemical interaction of materials are determined by the valence electrons. In order to avoid heavy computation, an approximation called frozen core is adopted. According to this approximation, the core electrons of an atom, which are regarded as less crucial for the calculation, can be substituted by a smoothed density. The pseudo-potentials for different elements can be found from the library built by DFT packages based on the exchange correlations.

2.2.2 Periodic Boundary Condition and Supercell

With DFT, it is easy to represent a crystal or lattice since unit cell defined in DFT computation repeats periodically in all the specified directions based on the boundary condition. Such unit cells are called supercell. Usually it can be a single atom or a set of atoms or molecule. When unit cell is defined using the minimum number of atoms, it is called primitive cell. Depending on how the periodic boundaries are set, there will be interaction between two periodic images in a direction. Therefore, in order to restrict the crystal in a dimension a vacuum region is usually inserted so that the interaction between periodic images can be avoided in that case. The volume of the cell and the atom coordinates are specified.

2.2.3 Cutoff Energy

When the periodic function in equation [5] is expanded by Fourier series, we get the reciprocal lattice vector.

$$\Psi_{nk}(r) = e^{ik \cdot r} u_{nk}(r) = e^{ik \cdot r} \sum_G C_k e^{iG \cdot r} \quad (2.11)$$

The equation above shows that the sum of plane waves results in Bloch wave. The kinetic energy of plane wave is expressed as:

$$E = \frac{\hbar^2}{2m} |k + G|^2 \quad (2.12)$$

The finite lattice vectors defined in real space turn into infinite reciprocal space lattice vectors. This means we will need to evaluate the sum of plane waves over reciprocal lattice vectors. The concept of cutoff energy becomes important in this regard. Since the plane waves obtain higher kinetic energy for increased reciprocal vectors size, the plane waves having kinetic energy larger than the cutoff energy will be disregarded for computing the sum of plane waves.

2.2.4 k points

In the reciprocal space, the primitive cell is known as first Brillouin Zone (BZ). The plane waves extend over the reciprocal space as wave vectors, k . The wave vectors which shifts from BZ can be expressed as: $k_0 = k + G$, where G is the shifted lattice vector in reciprocal space. As the wave vectors outside the BZ are expressed through the actual wave vector k inside BZ, we will need sufficiently large k points number inside to properly capture the actual form. By taking summation over the k points integrals are evaluated. Hence, a proper sampling of k points is required to get better approximation of energies.

2.3 Maximally Localized Wannier Functions

In almost all the DFT packages, plane waves are used to develop the KS wavefunctions. While that enables high accuracy computation of electronic structures, it does not support transport simulation. Because in the transport simulations, the localized basis functions are required. In 1930, Wannier introduced real-space representation of localized Bloch states [6]. In recent years, with the criteria of maximal localization, a computational method has been developed to develop those Wannier Functions (WFs) [7]. The method has been implemented as a code [eth-88] which is known as the Wannier90 code. By the maximally localized Wannier functions (MLWFs) the Bloch Hamiltonian is transformed into the basis for producing a maximally sparse block-tridiagonal matrix which is crucial for the atomic level simulations of devices with realistic physical sizes. In our work, we have utilized the MLWFs for computing quantum conductance of Si/SiO₂ systems of different thicknesses.

3. ELECTRONIC PROPERTIES OF SILICON NANOWIRE NANOSHEET

This chapter describes our work to investigate the materials electronic structure. We use DFT for the purpose. Section 3.1 explains the computational set up used for DFT simulations. Next, it describes the structural optimization of nanowire and nanosheet structures and their band structures without defects. Section 3.1 shows the results of intensive study on the NWs and NSs of various thickness through the energy dispersion relation and shows the comparison of bandgaps while showing the effect of scaling of the channels thickness. Section 3.2 shows the interface defects in nanowire and nanosheet through band structure and quantum conductance and evaluate ballistic current with the presence of interface defects.

3.1 First-principle Simulation of Si Nano-Wire and Nano-Sheet

We study the materials structural characteristic and electronic properties through Density Functional Theory (DFT) study. The DFT calculations given in this work have been done using ABINIT [8], Quantum Espresso [9] and Wannier90 [10] packages. We have used ultra-soft pseudopotentials [11] and bases of numerical atomic orbitals for the DFT simulations. The pseudopotentials were supplied with the ABINIT and Quantum Espresso packages. The exchange-correlation has been considered as the GGA-PBE (Generalized Gradient Approximation Perdew–Burke–Ernzerhof) functional. The Silicon basis has been built in a way so that we get the correct electronic properties of a Silicon nanowire. The performed convergence tests have the dependency of total energy on supercell size and k point sampling. In accordance with the convergence tests and considering the computational loads, the final simulations have been conducted using 1x1x2 supercells. The lattice parameter for Silicon is the value

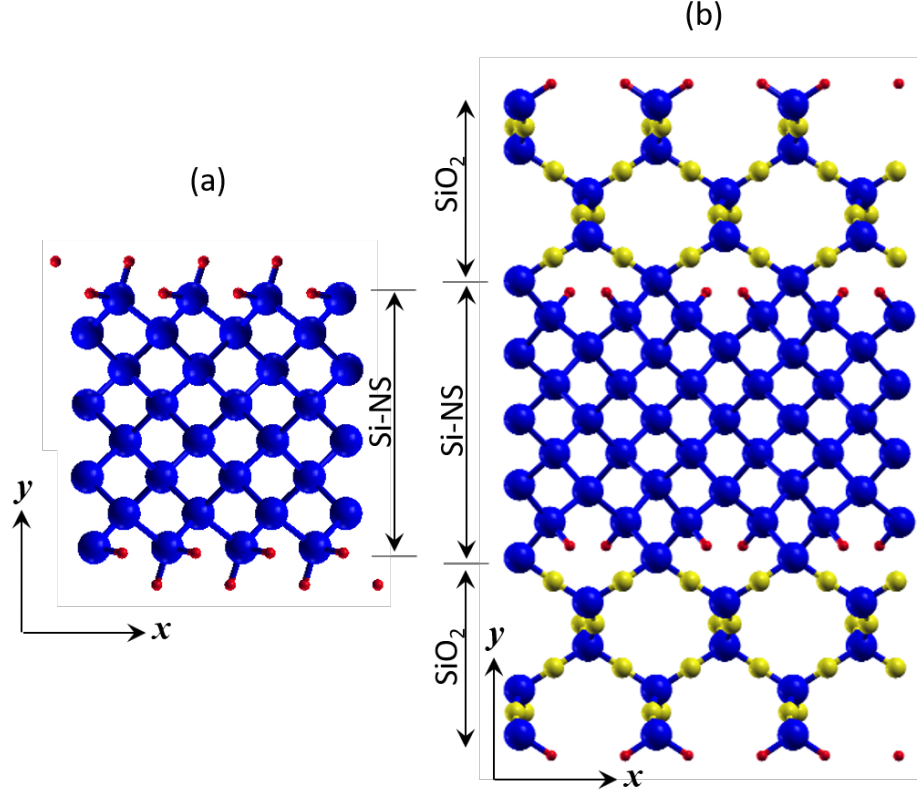


Fig. 3.1. (a) H-passivated Si-Nanosheet (NS) and (b) H-passivated SiO₂-Si-NS-SiO₂. Here, blue atoms are Si; red atoms are H, and yellow atoms are oxygen (O).

identical to the experimental value 5.431 Å. The k-space is sampled by 20 points. In a Monkhorst-Pack scheme, this is a 20x1x1 grid. The kinetic energy cut-off used for wavefunctions is 30 Ry. The kinetic energy cut-off for charge density and potential is 240 Ry. The convergence criteria is set to less than $10.0e^{-8}$ eV total energy difference between two subsequent iterations. All the calculations are conducted after allowing the supercell volume and shape relaxation, the maximum force being required to be less than $10.0e^{-3}$ eV/Å.

As Si-NW and Si-NS, we have considered two different systems for each of them. In the first system, we consider that the all dangling bonds at the open Si surfaces are passivated by Hydrogen (H) atoms. In the second system, we consider a SiO₂ layer

on top of the all open Si surfaces and the dangling bonds at the Si-SiO₂ interfaces are H-passivated. We call such system as SiO₂-Si-SiO₂. Considering Si-NS, a fully H-compensated system and H-compensated SiO₂-Si-SiO₂ system are shown in Figure 3.1(a-b), respectively. Here, the structures are optimized for the minimum energy of the system, which we discuss in the next subsection.

3.1.1 Structural Optimization of Si-Nanowire and Si-Nanosheet

In this section we demonstrate the physical configurations of Silicon nanowire (NW) and nanosheet (NS) used for the atomistic simulations in DFT. We first show the generic physical realization of Hydrogen (H) passivated Si structure and H passivated SiO₂-Si-SiO₂ structures, which are subjected to relaxation and cell optimization later one so that the minimum ground state energy is attained for each of the configurations.

Here, the configuration setups for the very initial structures are described on which we operate further by changing thickness and interface bonds status. The initial structure is built up using the measured bulk lattice parameters without geometry relaxation. Thus, to build the supercell for Si nanowire and nanosheet, $a = 5.431$ Å as the lattice parameter is used. The distance between the periodic images along y and z axis are set as $b = 15$ Å and $c = 25$ Å respectively for nanowire and only $c = 30$ Å for nanosheet. In such a structure, there are dangling bonds associated with all surface silicon atoms. We have used hydrogen atoms to fill those dangling bonds on surfaces. The bond length considered for Si-H bonds is 1.5 Å, which is similar as experimental value. The bond length value for Si-O bond and Si-Si bonds are 1.64 Å and 2.3 Å. The supercell for DFT calculations is employed in a way that for nanowire it gets infinite length in x direction, 1 Si unit cell (5.431 Å) width in y direction, 2 Si unitcell (10.862 Å) thickness in z direction. For Silicon nanosheet it becomes infinite in x direction and y direction and 2 Si unitcell or 10.862 Å thickness in z direction.

As the periodic images appear, for having a distance more than 10 Å they do not have interactions along y and z directions.

Atom/Ion relaxation

Unlike bulk crystal for a nanowire and nanosheet two dimensional (2-D) or one dimensional (1-D) confinement and surface are created. When the bulk symmetry is broken, there exist additional forces on the atoms especially on the atoms on or around surface. Hence, after determining the initial structures, at this stage we performed relaxation on the structure to reduce these forces. The relaxed structure for H passivated Si-NW is shown in Figure 3.2(b).

Cell Optimization

After reducing the additional forces upon atoms, now we considered relaxing the geometry and determine the optimized lattice parameter of the structures. We performed vc-relax simulation through Quantum Espresso package. The term vc-relax refers to variable cell relaxation. While it minimizes the inter-atomic forces, it simultaneously optimizes the lattice geometry using the components of stress tensor. The optimized cell has lattice vector of 5.54 rÅ and 5.68 Å for H passivated Si systems and SiO₂-Si-SiO₂ systems respectively. The finalized structures after these steps for H passivated Si-NW is shown in Figure 3.2(c), which is used towards further studies.

So the relaxation and optimization can be summarized in 3 steps:

- Relax all atoms in the structure keeping the cell parameter fixed.
- Optimize the cell along x axis using the relaxed structure from previous step.
- Using optimized cell parameter performed another relaxation study to investigate final positions for surface atoms.

During relaxation and cell optimization study the two factors taken into considerations are: the force on the atoms in supercell and the total energies for each of

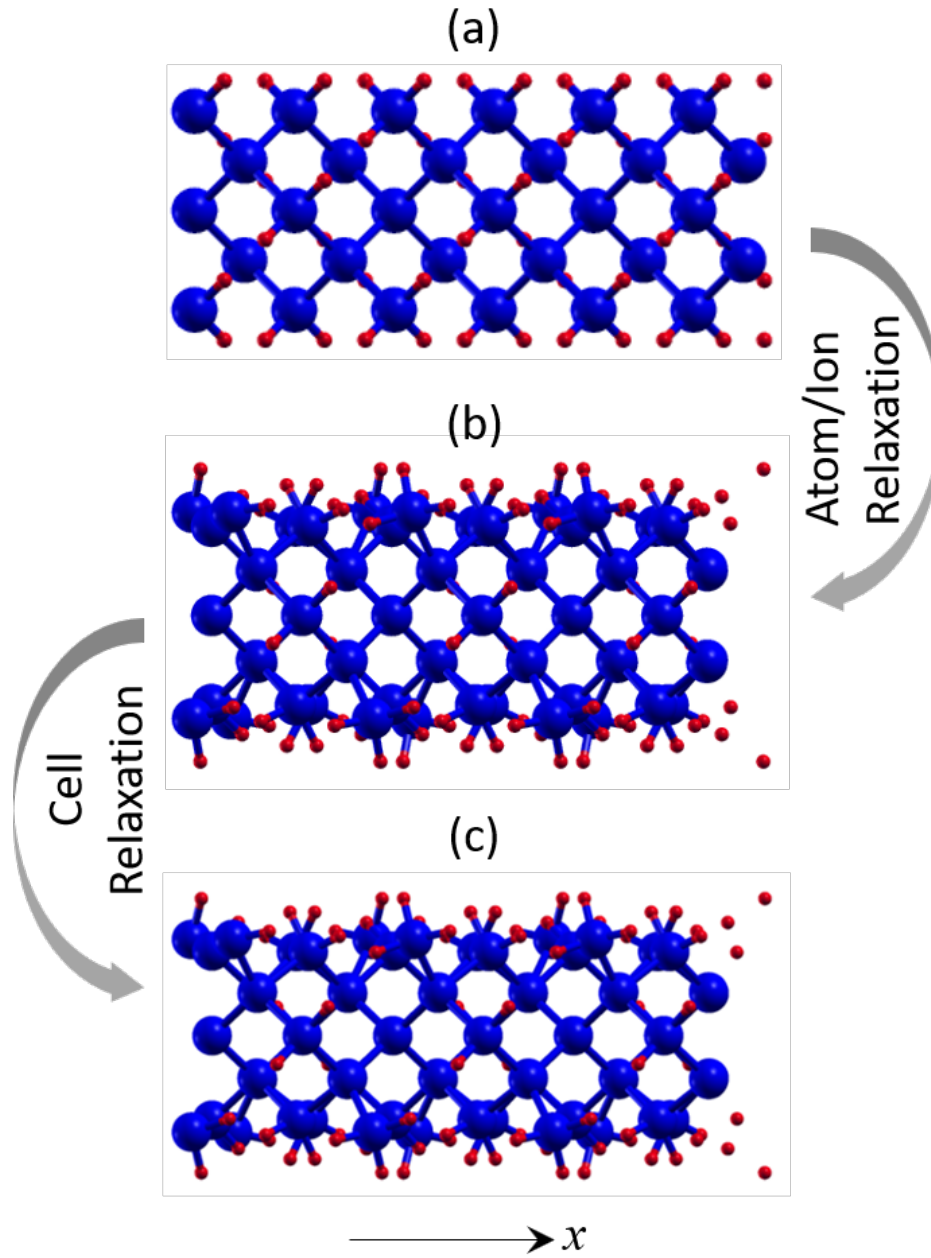


Fig. 3.2. Structural relaxation of H-passivated Si-nanowire (NW) showing atomic configuration as (a) input, (b) after atom/ion relaxation, and (c) after cell optimization. Here, the super-cell is periodic along the x direction; blue atoms are Si and red atoms are H.

the structure. Convergence threshold on total energy for ionic minimization is set as $5.0\text{E-}5$ eV/atom and convergence threshold on force for ionic minimization is set as $5.0\text{E-}4$ hartree/bohr while relaxing through the self-consistent field steps. All relaxation calculation is done using BFGS quasi-newton algorithm, based on the trust radius procedure. With the final set of relaxed atom a cell optimization study is conducted which gives us new lattice parameter 5.54 \AA and 5.68 \AA for H passivated Si structures and $\text{SiO}_2\text{-Si-SiO}_2$ structures respectively. We used this value for a in all the subsequent calculations.

3.1.2 Band Structure of Si Nanowire and Nanosheet without Defects

Unlike bulk Si crystal, the Si-NW and Si-NS exhibit finite dimension along certain directions. For example, Si-NS is confined along the z axis due its finite thickness and Si-NW is confined along the y and z directions due to its finite diameter. As a result, two-dimensional (2-D) and one-dimensional (1-D) quantum confinement effect arises in the electronic properties of Si-NW and Si-NS. In order to navigate such characteristics, we compute the band structures of Si-NW and Si-NS by performing DFT simulation on the relaxed structures.

So far, there are many approaches used for the purpose such as tight binding method, density functional theory, non-empirical self-consistent approaches and so on. We have utilized DFT by combining the most-widely exchange-correlation GGA-PBE (Generalized Gradient Approximation, Perdew–Burke–Ernzerhof) functionals. Figure 3.4 and 3.3 shows the energy-dispersion relation of the H passivated Si-NW and Si-NS structures.

However, due to the lack of correctness in the energy states of the excites electrons, bandgap calculated from GGA-PBE is underestimated by 30-40% than the experimental value [12]. The source of this inconsistency is the semi-local approximation in portraying exchange-correlation, which results in underestimation of bandgaps of semiconductors and insulators.

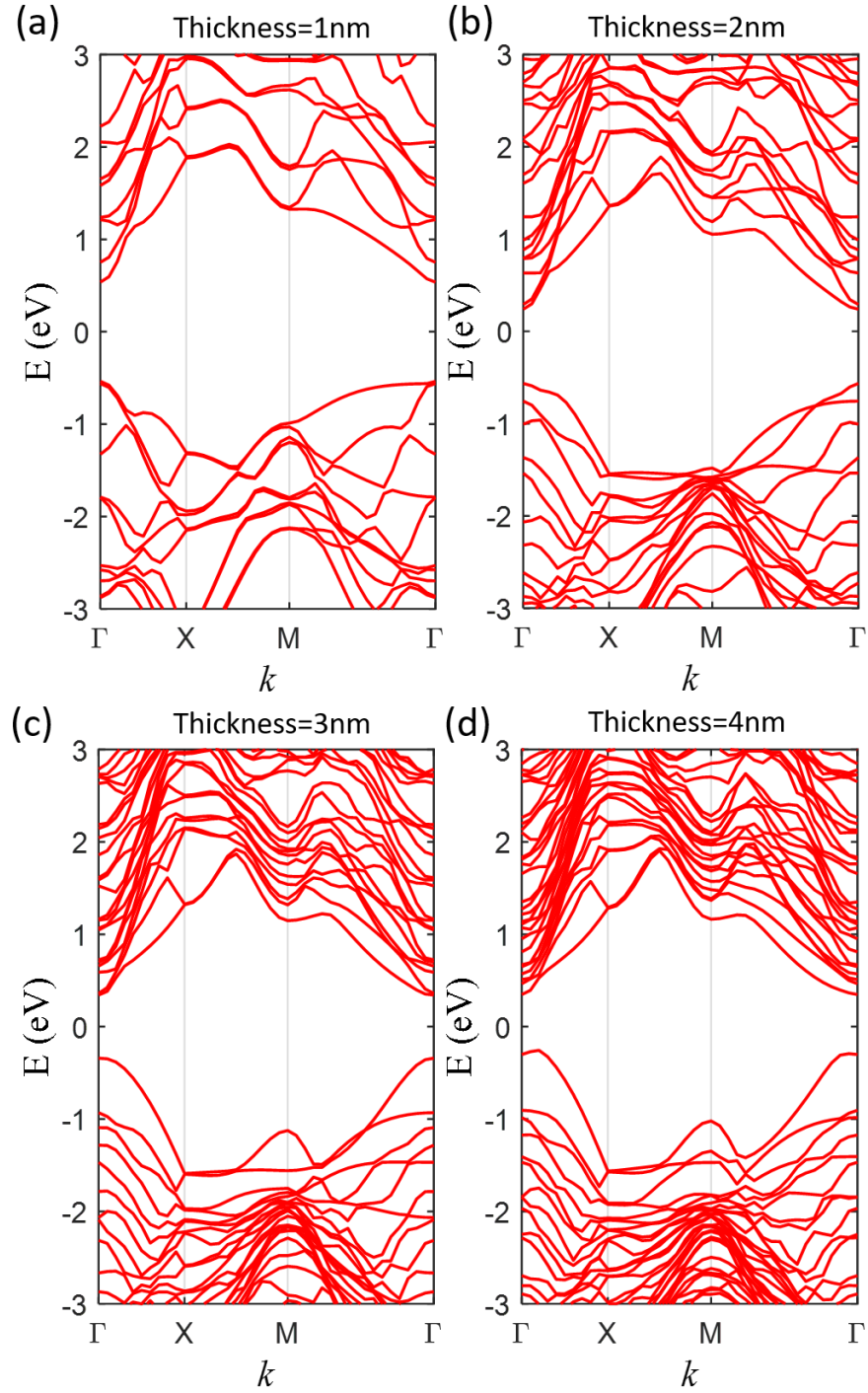


Fig. 3.3. Energy-Dispersion ($E-k$) characteristics of Si nanosheet obtained from DFT simulation for the thickness of (a) 1nm, (b) 2nm, (c) 3nm, and (d) 4nm. Here, the nanosheet is periodic along the x and y directions, therefore, $k \equiv (k_x, k_y)$.

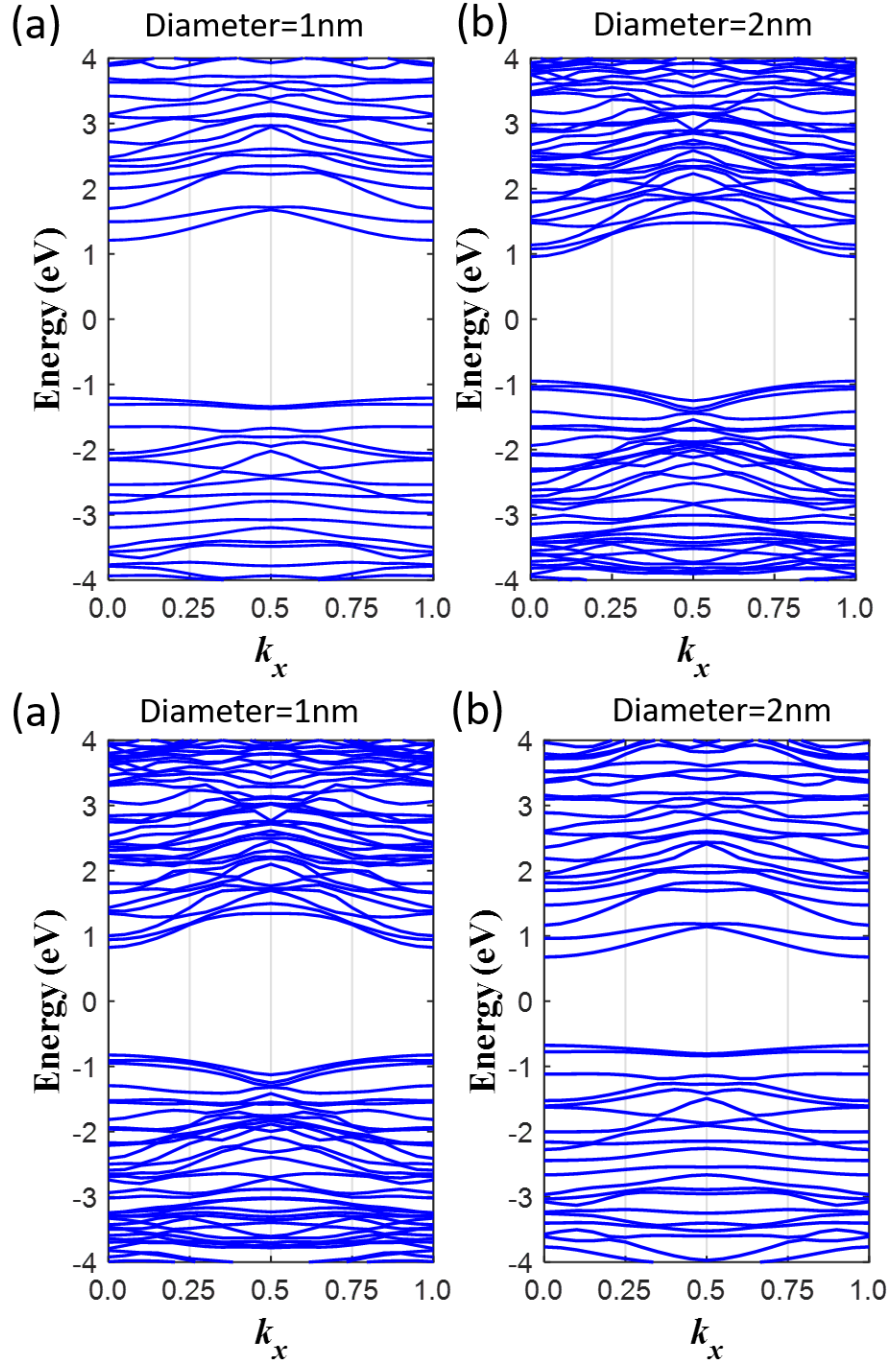


Fig. 3.4. Energy-Dispersion ($E-k$) characteristics of Si nanowire obtained from DFT simulation for the diameter of (a) 1nm, (b) 2nm, (c) 3nm, and (d) 4nm. Here, the nanowire is periodic along the x direction, therefore, $k \equiv k_x$.

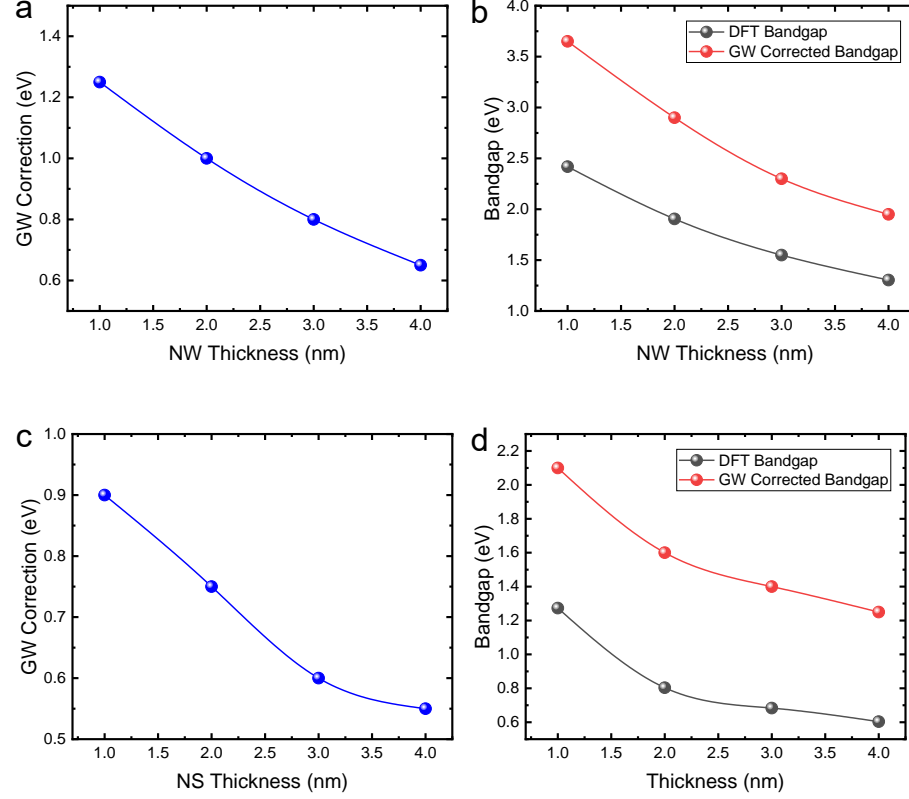


Fig. 3.5. (a) GW correction of Bandgap and (b) comparison of DFT Bandgap and GW corrected Bandgap (DFT+GW) for Si nanowire. (c) GW correction of Bandgap and (d) comparison of DFT Bandgap and GW corrected Bandgap (DFT+GW) for Si nanosheet.

While such limitation of GGA-PBE based DFT calculation is well known, the mitigation of this issue needs to undertake a hybrid orbital correction to enhance the GGA-PBE bandgap. In this case, we use the GW approximation in QE to calculate the required correction in bandgap.

Figure 3.5(a) shows the GW correction for different Si-NW thickness and 3.5(b) signifies the comparison of DFT calculated and DFT+GW corrected band gap for different Si-NW diameter. The similar characteristics for Si-NS are shown in 3.5(a-b). Here, we consider the Si-NW and Si-NS with fully H-passivated interface. The bandgaps found from our study suggest excellent agreement with the experimentally measured bandgaps [13], [14], [15] as depicted in Figure 3.7.

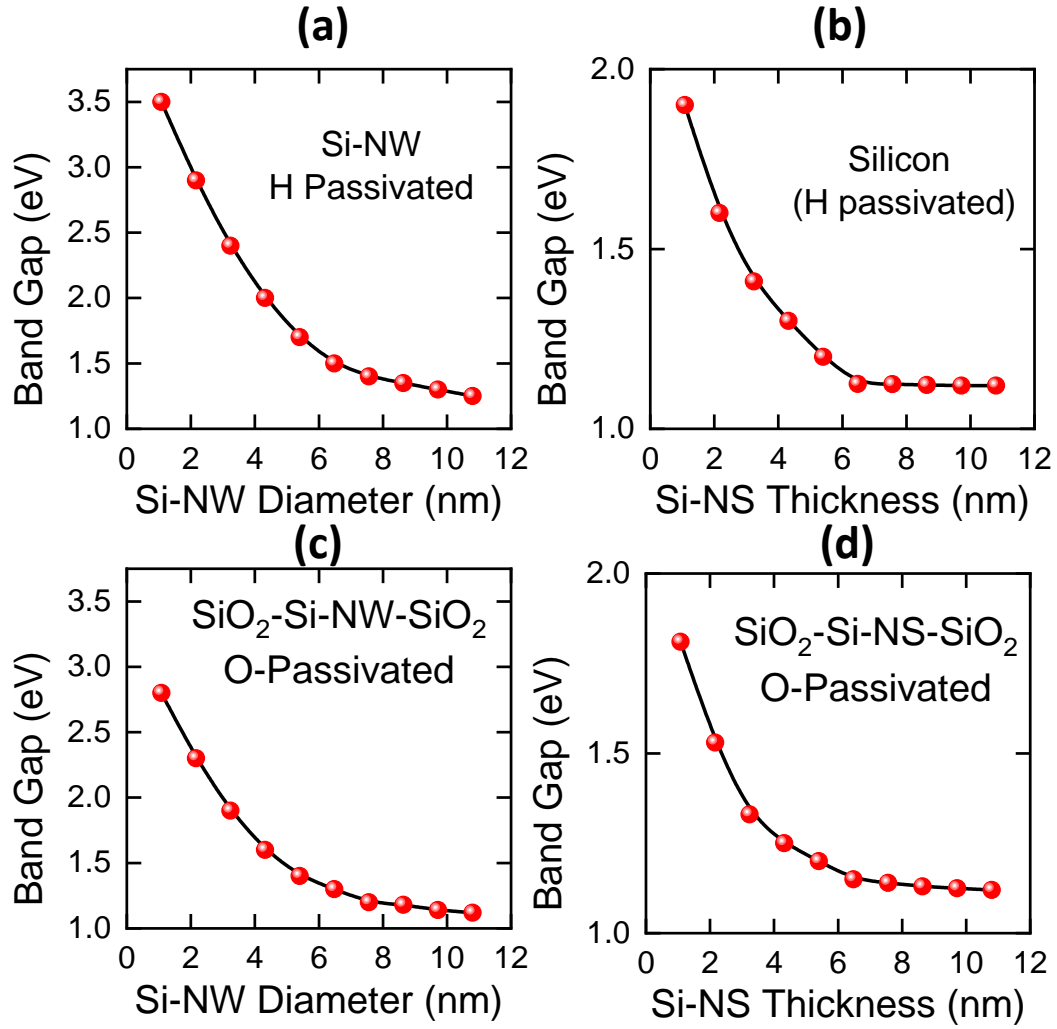


Fig. 3.6. Bandgap of Si (a) nanowire and (b) nanosheet with hydrogen passivated surface. Bandgap of Si (c) nanowire and (d) nanosheet with Hydrogen passivated SiO₂-Si-SiO₂ system.

Similarly, the bandgap of Si-NW and Si-NS for a larger range of thickness and diameter are shown in Figure 3.6(a) and Figure 3.6(b), respectively. Further, we consider the SiO₂-Si-NW-SiO₂ and SiO₂-Si-NS-SiO₂ systems, and their respective bandgaps with different diameter/thickness are shown in Figure 3.6(c) and Figure 3.6(d).

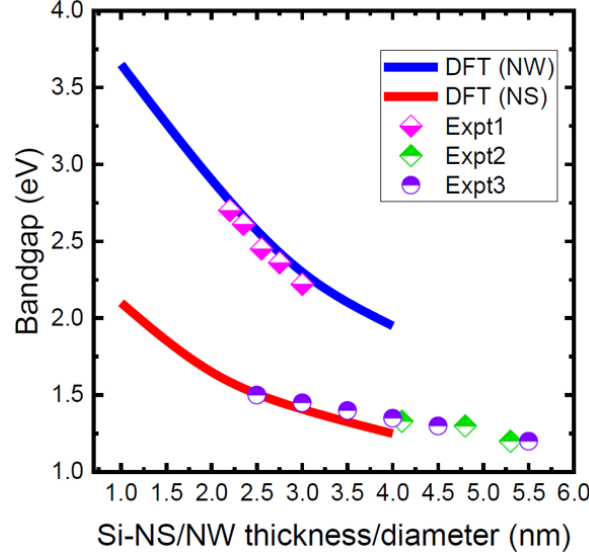


Fig. 3.7. DFT+GW computed bandgap compared to the experimental bandgap [13], [14], [15] of Si-NW and Si-NS

3.2 Interface Defects in Si Nanowire and Nanosheet

So far, we have considered Si-NW and Si-NS with no dangling bonds and that implies, all the Si surfaces or Si-SiO₂ interfaces are fully H-passivated. However, in different scenarios, such Si-H bonds can break and that can lead to the appearance of dangling bonds. Such dangling bonds in Si surface is known as Pb center and/or interface defects. Formation of such interface defects can be triggered depending on various factors. Among them, the dissociation of Hydrogen atom from a Si site is most prominent, which we discuss in Chapter 5. Most importantly, such interface defects are of significant importance from the perspective of the use of Si-NW/NS in a transistor channel. In particular, as transistors continue to shrink, interface defects and its adverse effects can become crucially significant in the ultra-scaled transistors compared to the transistors of earlier technology nodes, which we analyze in chapter 6 in great details.

To enable such discussion, in this subsection we show that, how the interface defects affect the electronic properties of Si-NW and Si-NS. To that effect, we compute

$E - k$ relations, density of states (DOS) and quantum conductance ($G(E)$) of Si-NW and Si-NS by considering different combinations of interface defects.

3.2.1 Band Structure of Si Nano-wire and Nano-sheet with Defects

So far, we have considered ideal surface or interface with no presence of defect. Now we will consider defects at Si and oxide interface. We vary the number of defects at the surface and explore its effect through the density of states (DOS) and quantum conductance. In absence of any defects, the density of states should not have any electronic states within the bandgap region as shown in Figure 3.8(a). However, in presence of defects, electronic states appear within the bandgap region as shown in Figure 3.8(b-c). The energy-dispersion ($E-k$) relation for different Si-NW and Si-NS thickness are shown in Figure 3.9(a-c) and Figure 3.10(a-c). Both the results suggest that the electronic states appear in bandgap region with presence of interface defect.

3.2.2 Effects of Defects in Quantum Conductance

Now we analyze the influence of theses defect states in the quantum conductance characteristics. The quantum conductance (QC) is calculated using DFT code coupled to Wannier90 [[10]] code. First, using self-consistent field (scf) calculation the ground states eigen functions are computed. Then they are transformed to Maximally Localized Wannier Function (MLWF) basis. The Hamiltonian in MLWF basis is used to calculate the quantum conductance ($G(E)$) in one-dimensional direction (along the x direction).

The effects of defects in the $G(E)$ characteristics are shown for Si-NW and Si-NS in Figure 3.9(d-f) and Figure 3.10(d-f) that suggest the formation of finite conductance states within the bandgap energy window in presence of defects. At the same time, the defect induced conductance increases with the increase in the number of defects.

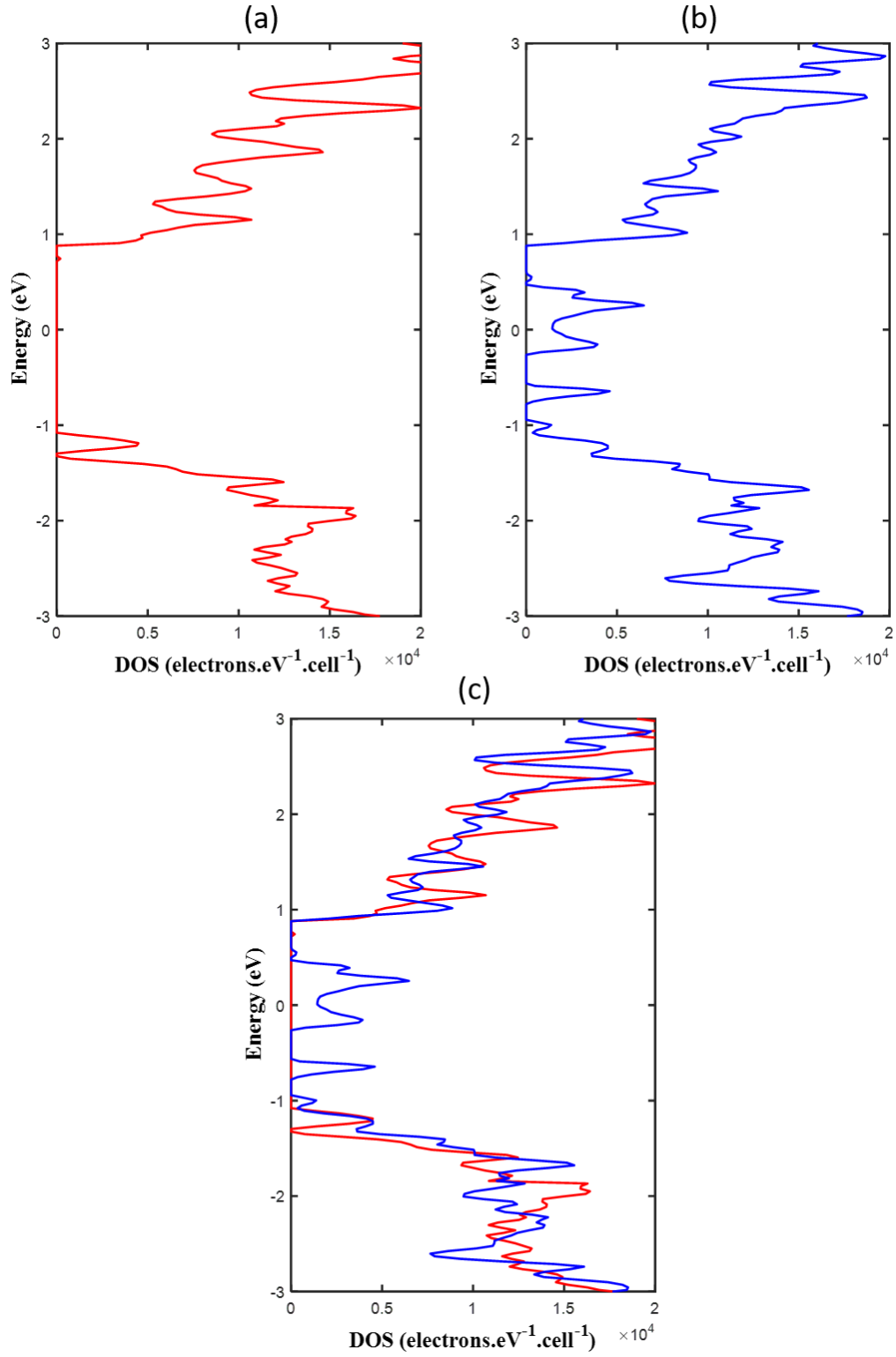


Fig. 3.8. Density of states (DOS) of Si-NW (a) with no-defect, (b) with defects, and (c) their comparison. Here, the Si-NW thickness is 3.5nm.

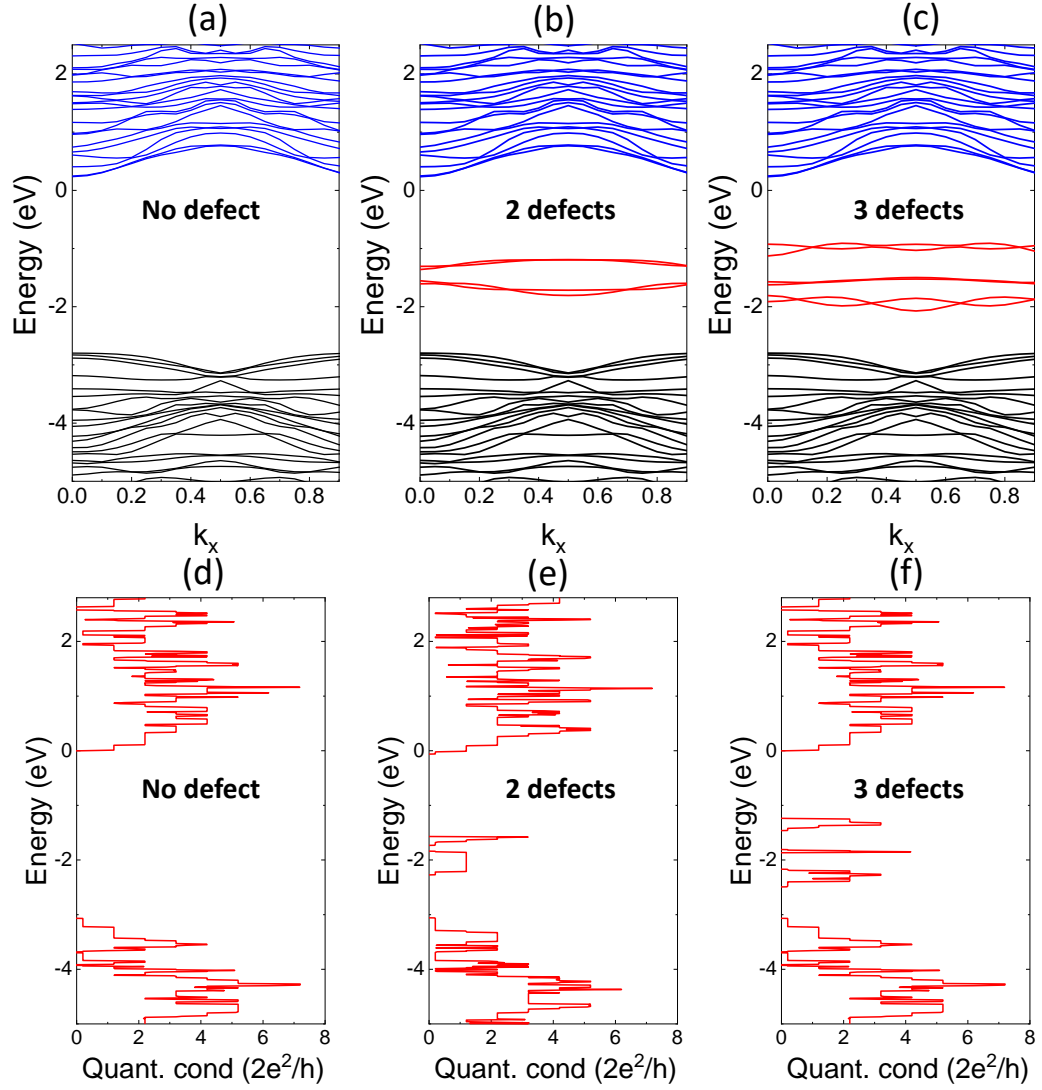


Fig. 3.9. (a-c) Energy-dispersion ($E-k$) characteristics and (d-f) corresponding quantum conductance ($G-E$) of Si-NW for 0, 2, and 3 defect states (dangling bonds), respectively.

Note that, in case of no defect scenario, there is no conductance within the bandgap energy region. Such defect induced conductance influence the current-voltage characteristics of the Si-NW and Si-NS, which we analyze next.

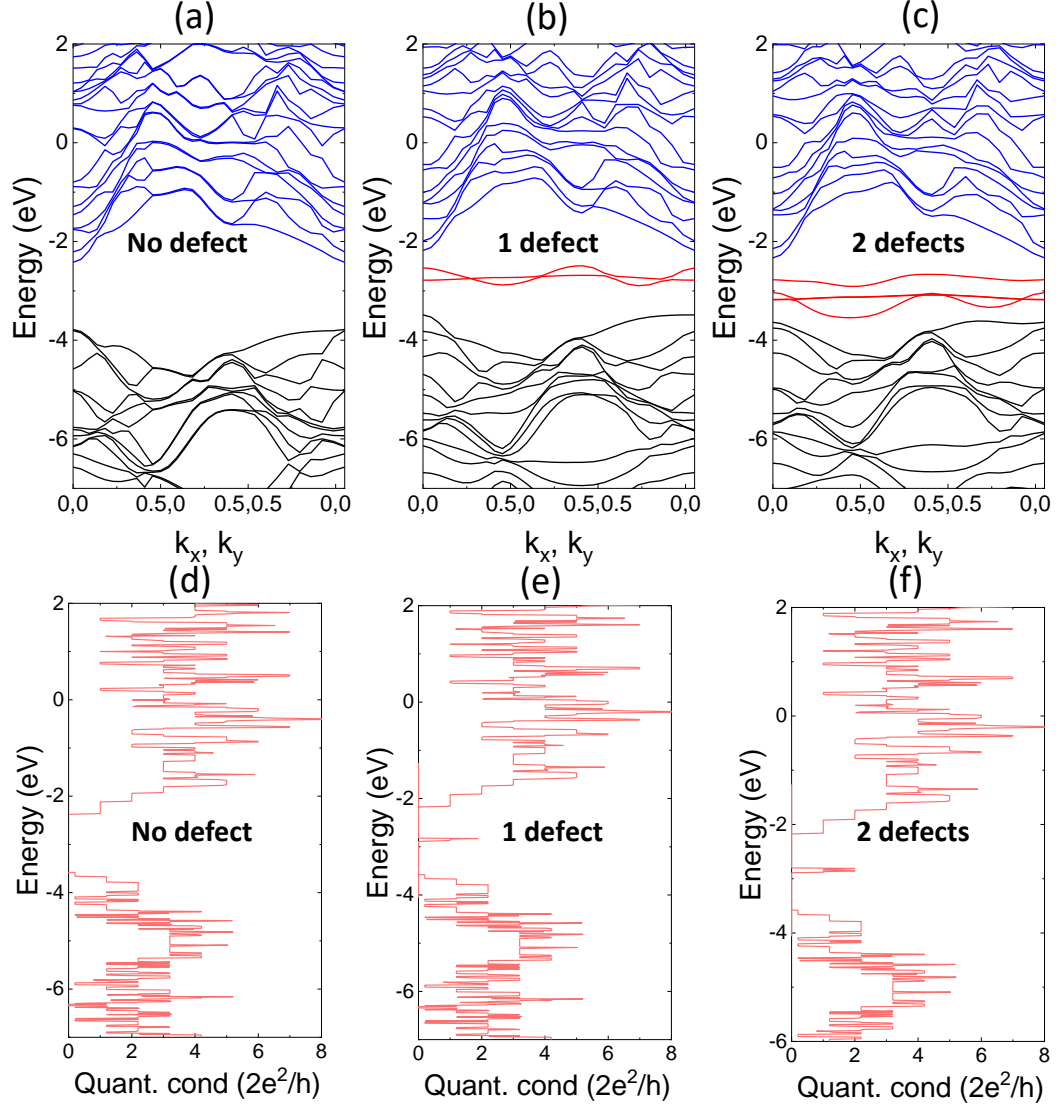


Fig. 3.10. (a-c) Energy-dispersion ($E-k$) characteristics and (d-f) corresponding quantum conductance ($G-E$) of Si-NW for 0, 2, and 3 defect states (dangling bonds), respectively.

3.2.3 Influence of Defects in Ballistic Current

The term ‘ballistic-current’ implies that an electron flowing through the Si-NW and Si-NS does not change its energy, which is analogous to say that the electron-phonon interaction is negligible. Such an assumption is valid considering the very small dimension of our systems along the x -axis. This is because the mean free path

for the electron to scatter and its changes in energy is larger than the dimension of the system. Now, let us consider that the left side and right side of the system are contacted through metals. Such a system is analogous to a transistor without having a gate control. The current-voltage ($I - V$) characteristics of this Si-NW/NS system can be calculated based on Landauer formalism by employing the following equation. Such observation implies that the threshold voltage of the transistor decreases with the increase in interface states.

$$I = \int G(E)[f_2(E - qV/2) - f_1(E + qV/2)]dE \quad (3.1)$$

Here, $f_{1(2)}(E)$ is the fermi function of the left (right) electrode, $G(E)$ is the quantum conductance and V is the applied voltage. In the above equation, the term $[f_1(E - qV/2) - f_2(E + qV/2)]$ can be denoted as the fermi window for an applied voltage V as shown in Figure 3.11(a). The Landauer equation suggests that, only the conductance state, $G(E)$ within this fermi window takes part in conduction. Now, let us first consider the scenario where there is no defect states (Figure 3.11(b)). In this case, there is no $G(E)$ within the fermi window and the resultant current remains zero upto a certain V . In contrary, the presence of defect states leads to a finite $G(E)$ within the bandgap region and also within the fermi window. As a result, finite current is observed in the $I - V$ characteristics as shown in Figure 3.11(d). Note that the current increases with the increase in the number of defects due to the increase in defect induced $G(E)$. It is important to note that the $I - V$ characteristics presented in Figure 3.11(d) is analogous to the drain-current versus drain-voltage ($I_D - V_{DS}$) characteristics of a transistors. Based on this analogy, we can state that off-state resistance or off-current of a scaled transistor is highly dependent on the interface states and such current increases with the increase in trap state density.

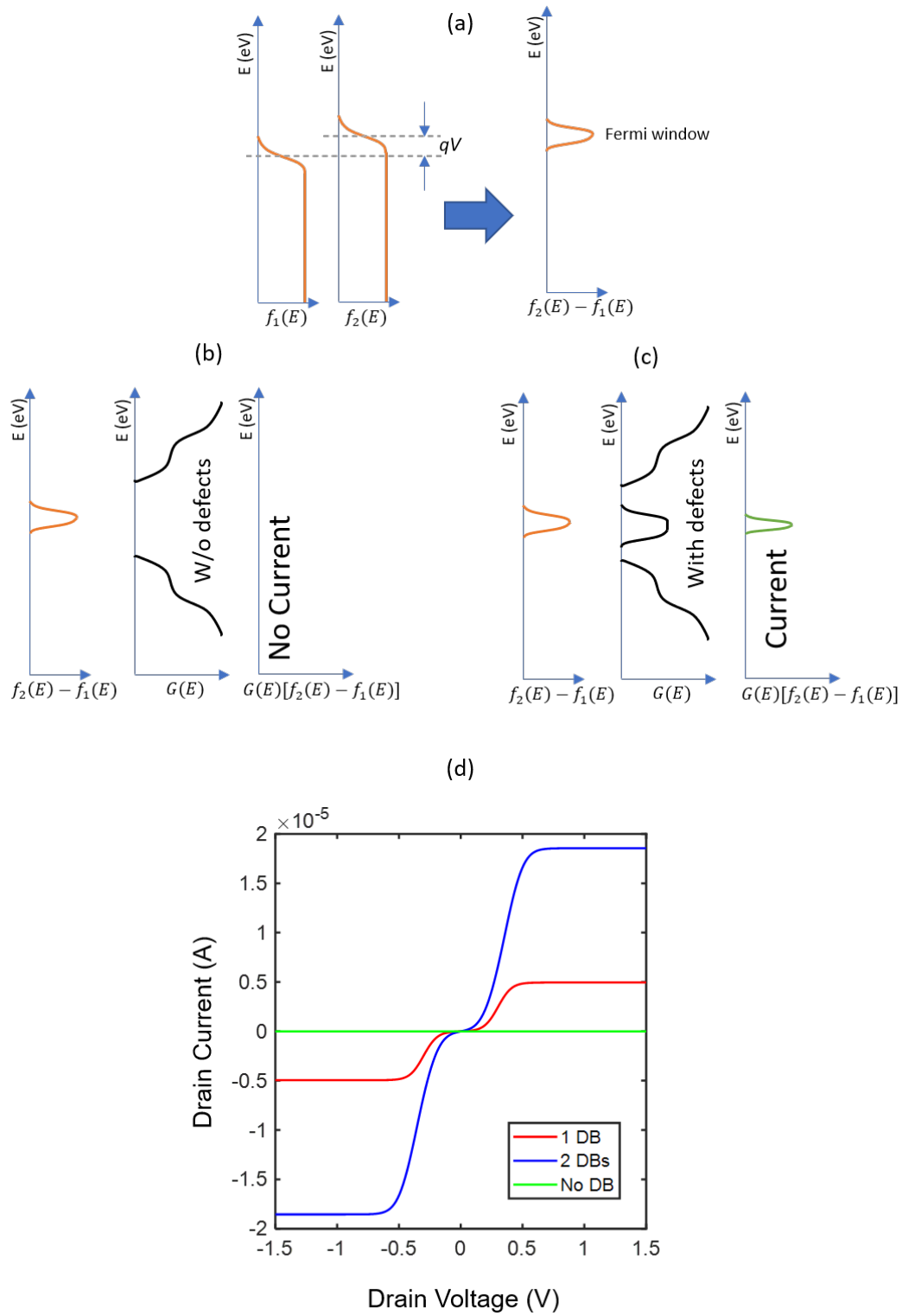


Fig. 3.11. (a-c) Energy-dispersion ($E-k$) characteristics and (d-f) corresponding quantum conductance ($G-E$) of Si-NW for 0, 2, and 3 defect states (dangling bonds), respectively.

4. INFLUENCE OF SCALING IN GAA-FET AND MBC-FET CHARACTERISTICS

In this chapter, we analyze the effect of scaling on the Gate-all-around (GAA)-FET and Multi-bridge-channel (MBT)-FET characteristics. In Section 4.1, we briefly discuss the simulation framework for device simulation. In Section 4.2, we analyze the bandgap effect of GAA-FET and MBC-FET characteristics.

4.1 Self-consistent Device Simulation Framework

A self-consistent simulation technique among electrostatic potential and charge distribution is required to simulate any electronic device. When a device channel is linked with the source and drain contacts, there will be charge flow into or out of the device respectively. Similarly, when the device channel is linked with gate contact, the electric field-lines will insert into or out of the device. This process develops a resulting self-consistent potential ($U_{SC}(r)$). Any change in $U_{SC}(r)$ changes the charge density in the device $\rho(r)$ and it continues until they achieve consistent values. This process is modeled using two key equations: the Poisson equation [10.1.1..36] and the Schrodinger equation. For self-consistent solution of potential and charge, we utilize non-equilibrium Green's function (NEGF) formalism that solves the Poisson's equation and Schrodinger's equation in an iterative scheme until the self-consistency is achieved.

The Poisson's equation describes the interrelation between the charge density profile ($\rho(r)$) and potential profile ($U_{SC}(r)$) based on the following equation.

$$\nabla(\varepsilon(r)\nabla U_{SC}(r)) = -\rho(r) \quad (4.1)$$

Here, $U_{SC}(r)$ is the self-consistent potential, $\rho(r)$ is the charge density. The dielectric constant $\varepsilon(r)$ is position dependent because of the transition in material from Silicon layers to oxide layers.

Now, under NEGF formalism, the Schrodinger equation of an open system (due to the presence of contacts) can be written in the following forms.

$$G(E) = [EI - (H + U_{SC}) - \Sigma_S - \Sigma_R]^{-1} \quad (4.2)$$

Here, $G(E)$ is the Green's function; H is the device Hamiltonian matrix; E is the energy; I is the identity matrix; and $\Sigma_{S(D)}$ is the self-energy matrix for source (drain) contacts. From the above equation, the spectral charge density can be calculated from the following equations.

$$n(r) = \int_{-\infty}^{\infty} \frac{dE}{2\pi} [(G\Gamma_S G^\dagger) f_S(E) + (G\Gamma_D G^\dagger) f_D(E)] \quad (4.3)$$

$$p(r) = \int_{-\infty}^{\infty} \frac{dE}{2\pi} [(G\Gamma_S G^\dagger)(1 - f_S(E)) + (G\Gamma_D G^\dagger)(1 - f_D(E))] \quad (4.4)$$

$$\Gamma_S(D) = i[\Sigma_{S(D)} - \Sigma_{S(D)}^\dagger] \quad (4.5)$$

$$\rho(r) = -q[n(r) - p(r) - N_D^+(r) + N_A^-(r)] \quad (4.6)$$

Here, $f_{S(D)}$ is the source (drain) fermi function; N_A^- and N_D^+ is the ionized acceptor and donor concentration, respectively. The self-consistent loop of the quantum mechanical simulation in NEGF framework can be described with the following steps:

- Obtain an approximate value for $U_{SC}(r)$ from semi classical simulation or assume any small value.
- For a given $U_{SC}(r)$ device, Hamiltonian and self-energy matrices are constructed.
- Charge density ($\rho(r)$) is computed from NEGF equation.
- Utilizing the $\rho(r)$, Poissons equation is solved for the $U_{SC}(r)$.
- The above three steps are repeated until the convergence of $\rho(r)$ and $U_{SC}(r)$.

- Using converged value of density matrix and self-consistent potential, drain current (I_D) is calculated under Ballistic transport approximation based on the following equation.

$$I_D = \frac{2\pi q}{h} \int_{-\infty}^{\infty} dE [(G\Gamma_S G^\dagger \Gamma_D)(f_S(E) - f_D(E))] \quad (4.7)$$

To get the GAA-FET and MBC-FET characteristics, we have performed the NEGF simulation in Nano-hub tool [16]. Next, we discuss different simulated characteristics of GAA-FET and MBC-FET, which we obtained from device simulations.

4.2 GAA-FET and MBC-FET Characteristics

The GAA-FET and MBC-FET utilizes the Si-NW and Si-NS as the channel material, respectively. The side-view of the GAA/MBC-FET is shown in Figure 4.1(a). Similarly, the cross-sectional view of the GAA-FET is shown in Figure 4.1 (b) and of the MBC-FET is shown in Figure 4.1 (c). Corresponding parameters we have used in the simulation are provided in the Figure caption. Next, we analyze their simulated characteristics. For GAA-FET, we consider $W_{Si}=t_{Si}$ and for MBC-FET we fixed the W_{Si} as 9nm.

The simulated drain-current (I_D) versus gate-voltage (V_{GS}) characteristics of GAA-FET for different Si-NW thickness is shown in Figure 4.2(a). We plot these I_D - V_{GS} characteristics at iso-OFF current condition and that suggest an increase in ON current with the decrease in Si-NW thickness. It is trivial to understand that, with the decrease in Si-NW thickness, the electrostatic control of gate voltage over the channel carrier increases. As a result, the ON current should increase. However, in chapter 3, we discussed that the bandgap of Si-NW increases with the decrease in Si-NW thickness. As a consequence, the channel carrier concentration should decrease. Between these, two opposite effects (improvement in electrostatic control and increase in bandgap), the improvement in electrostatic control dominates. Hence, the drain-current improves with scaling.

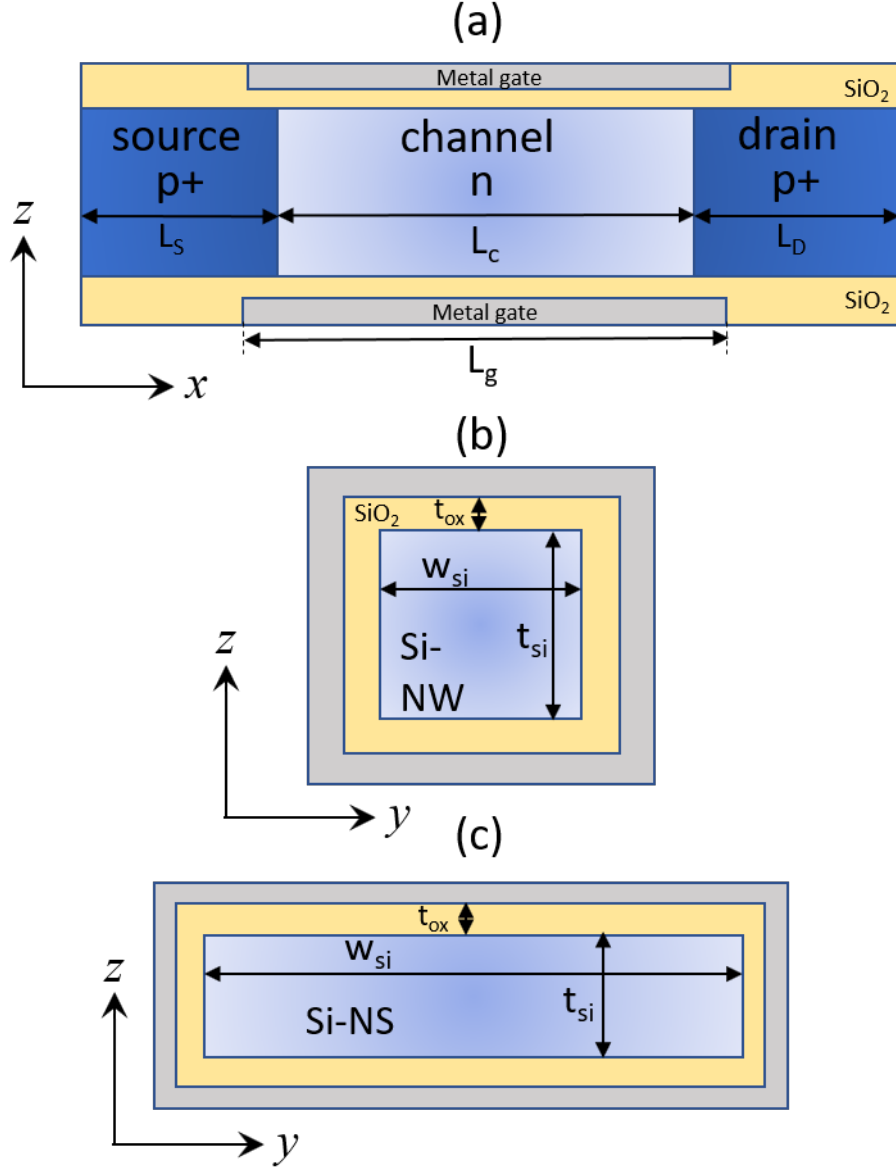


Fig. 4.1. GAA-FET (a) structure and (b) cross sectional view with Si-Nanowire (NW) channel. MBC-FET (c) structure and (d) cross sectional view with Si-Nanosheet (NS) channel. In our simulation, we assume $EOT=0.75\text{nm}$; gate length, $L_g=10\text{nm}$; channel length, $L_c=5\text{nm}$; source (drain) extension, $L_{S(D)}=5\text{nm}$; gate-source (drain) overlap, $L_{ov,S(D)}=2.5\text{nm}$; channel doping, $N_D=10^{15}\text{cm}^{-3}$; source (drain) doping, $N_A=10^{20}\text{cm}^{-3}$

Similarly, we plot the simulated I_D versus drain-voltage (V_{DS}) characteristics in Figure 4.2(b-d) of GAA-FET for different Si-NW thickness that confirms an increase in drain-current with thickness scaling.

Similar to the GAA-FET, the simulated I_D - V_{GS} characteristics and I_D - V_{DS} characteristics for MBC-FET are shown in Figure 4.3(a) and Figure 4.3(b-d) for different Si-NS thickness. Here, the trends are similar to GAA-FET with respect to thickness scaling. However, our simulation suggest a higher ON current for MBC-FET compared to the GAA-FET due to the higher width of GAA-FET. At the same time, the quantum confinement effect on bandgap is less for Si-NS (that corresponds to MBC-FET) compared to Si-NW (that corresponds to GAA-FET). As the bandgap is low, the carrier concentration increase and that leads to higher current in MBC-FET compared to GAA-FET.

Based on our findings, we can summarize that, for the similar Si-NW/NS thickness, the MBC-FET performance can be higher compared to the GAA-FET performance in terms of the ON state current of the device (for an iso-OFF state current condition).

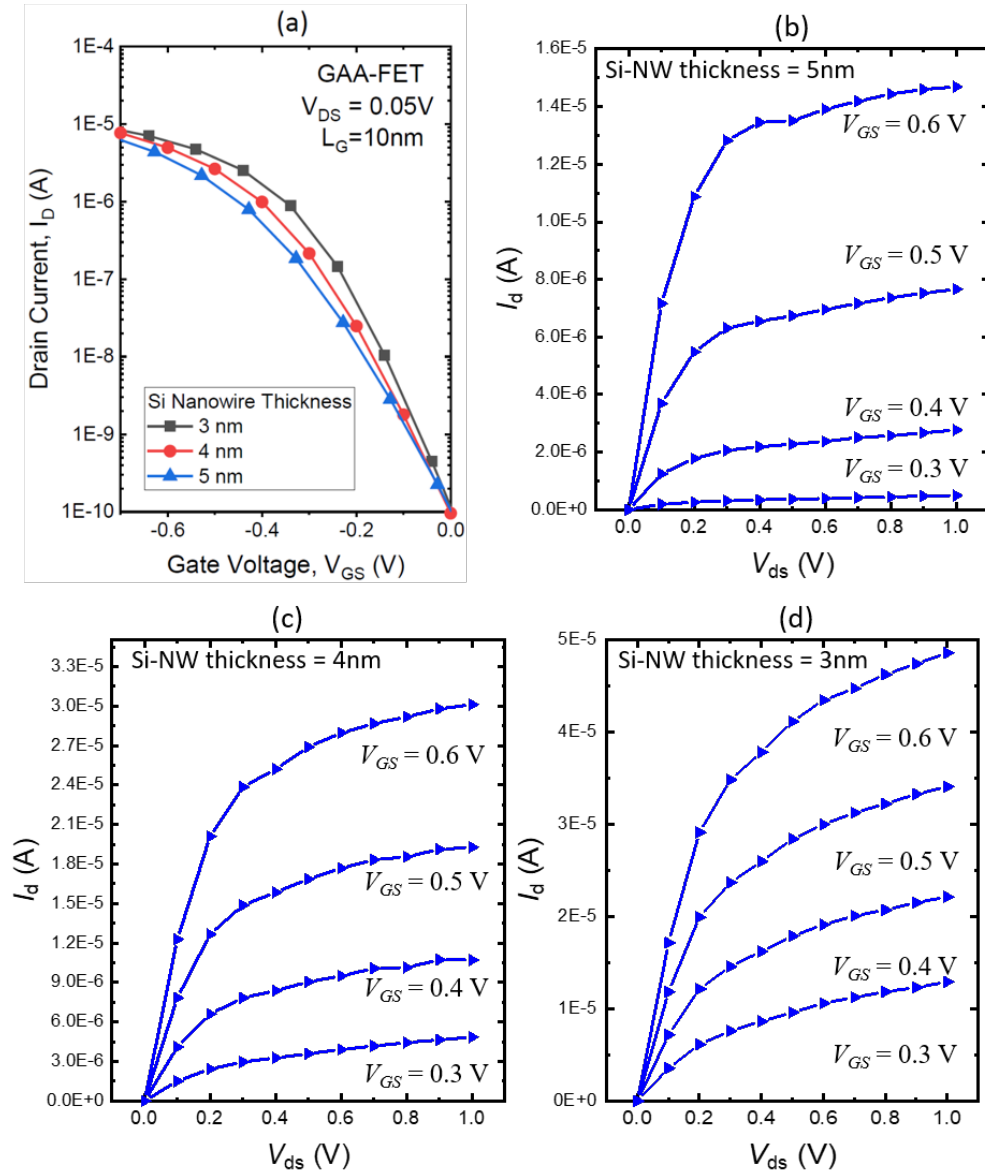


Fig. 4.2. (a) I_D - V_{GS} characteristics and (b-d) I_D - V_{DS} characteristics of GAA-FET for different Si-NW thickness.

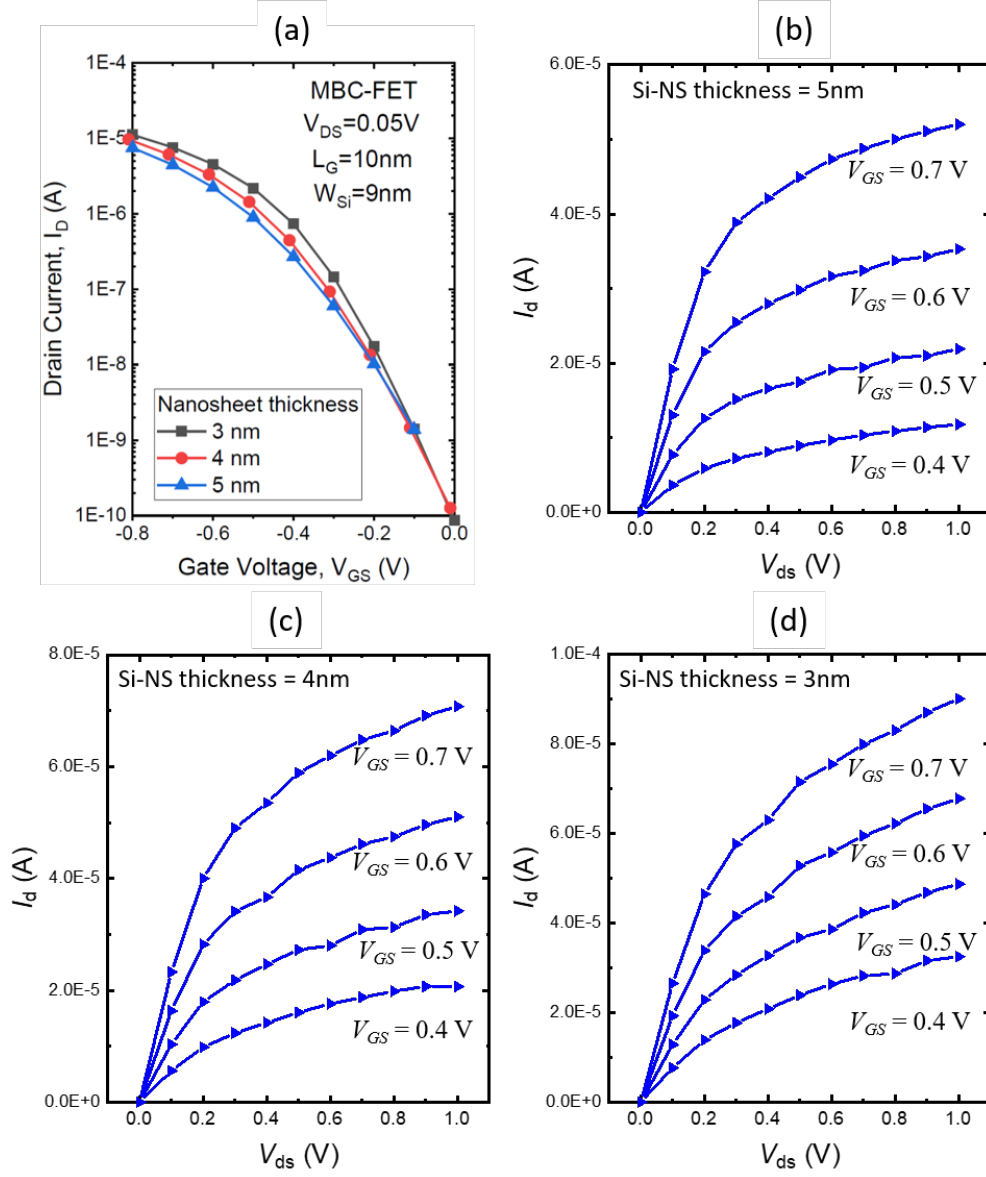


Fig. 4.3. (a) I_D - V_{GS} characteristics and (b-d) I_D - V_{DS} characteristics of MBC-FET for different Si-NS thickness.

5. ACTIVATION ENERGY OF SI-H BOND DISSOCIATION

In this chapter, we focus on analyzing the process for interface defect state generation at the Si-SiO₂ interfaces. In Section 5.1, we discuss the physical process of Si-H bond dissociation. In Section 5.2, we compute the activation energy associated with the Si-H bond dissociation and in Section 5.3, we analyze the correlation of the activation energy and the electric-field in the SiO₂ layer.

5.1 Formation of Defects at Si-SiO₂ Interface

While the formation of interface defects can occur in a diverse set of scenarios, the most frequent and plausible mechanism is the dissociation of a Si-H bonds. In Si-SiO₂ interface, the dissociation of a Si-H bonds typically takes place based on the following reaction.



The above reaction suggest that the presence of H⁺ ion is localized near the Si-SiO₂ interface. Then it leads to the dissociation of Si-H bonds by forming a H₂ molecule and a dangling bond (D). Once the H₂ molecule is formed, it diffuses and moves away from the interface. Such a process has been depicted in Figure 5.1 (a). It is important to note that the dissociation of such Si-H bonds exhibits an energy barrier needs to be overcome for the occurrence of this process as shown in Figure 5.1 (b). The height of this energy barrier is known as the activation energy (E_A) of the Si-H bond dissociation.

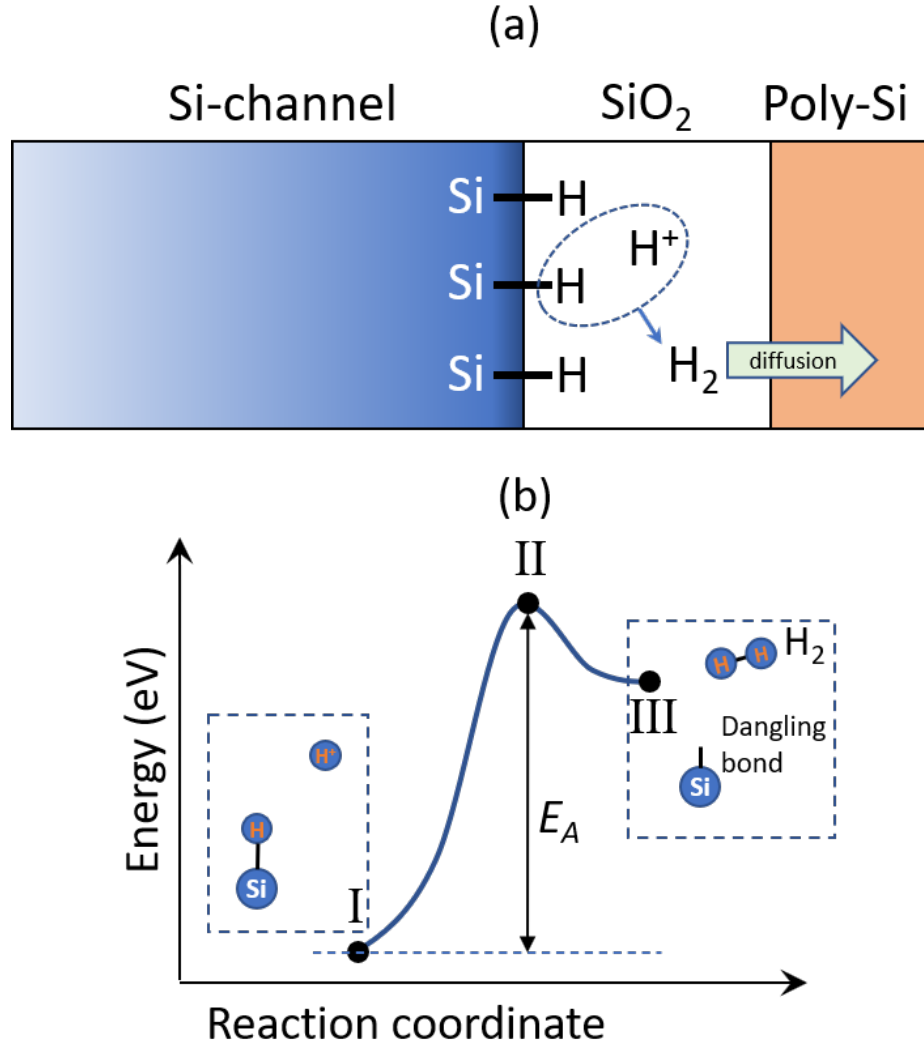


Fig. 5.1. (a) Process of Si-H bond dissociation in Si-SiO₂ interface. (b) Energy landscape of Si-H bond dissociation signifying the presence of an activation barrier (E_A).

5.2 Activation Energy of Si-H Bond Dissociation

To calculate the activation energy (E_A) for dissociation of Si-H bonds, we have used Nudged Elastic Band (NEB) method in conjunction with DFT simulation in ABINIT. In NEB method, we need to provide the configurations that corresponds to the initial structure (no defects + H⁺ at a certain distance) and final structure

(dangling bond + H₂ molecule). The initial and final configurations for a SiO₂-Si-NS-SiO₂ system are shown in Figure 5.2(a-b), which we obtained from the complete structural relaxation. The NEB simulation compute an atomic trajectory for H atom (which was initially bonded with Si) that corresponds to the minimum energy path (MEP) for the desired reaction. We compute the system energy for this MEP and obtained E_A as the difference between the maximum and minimum energy of the reaction path. The E_A for different Si-NS thickness are plotted in Figure 5.2(c) signifying an decrease in E_A with the decrease in thickness. Similarly, we compute the E_A for Si-NW with different diameter showing the similar dependency with its dimension (5.2(c)).

In both of the cases (Si-NW and Si-NS) the activation energy (E_A) decreases with the decrease in thickness/dimension. While such insights are completely new, an easy understanding may not be trivial. It is possible that, in the case of lower thickness/diameter, the long range interactions are more confined and therefore, when the H displacement takes place the corresponding change in atomic positions of Si are less. As a result, the change in energy is less for lower dimension. Due the similar effects, we observe that the E_A is lower in Si-NW compared to Si-NS due to the more size confinement in the former case. Nevertheless, this observation suggests that the formation of dangling bond demands less energy with the scaling of Si-NW and Si-NS.

5.3 Effects of Oxide Electric Field on E_A

So far, we have investigated the activation energy for the Si-H bond dissociation at Si-SiO₂ interface. Now, we will turn our focus into its dependency with applied voltage or electric-field. First, we will briefly explain the physics behind such dependency. In ideal condition and in absence of an electric-field, Si-H bonds do not carry any net charge. However, the Si and H have different electro-negativities. As a result, in presence of an electric field, they attract their bonding electrons with different forces and that gives rise to a dipole. Most importantly, the applied electric field

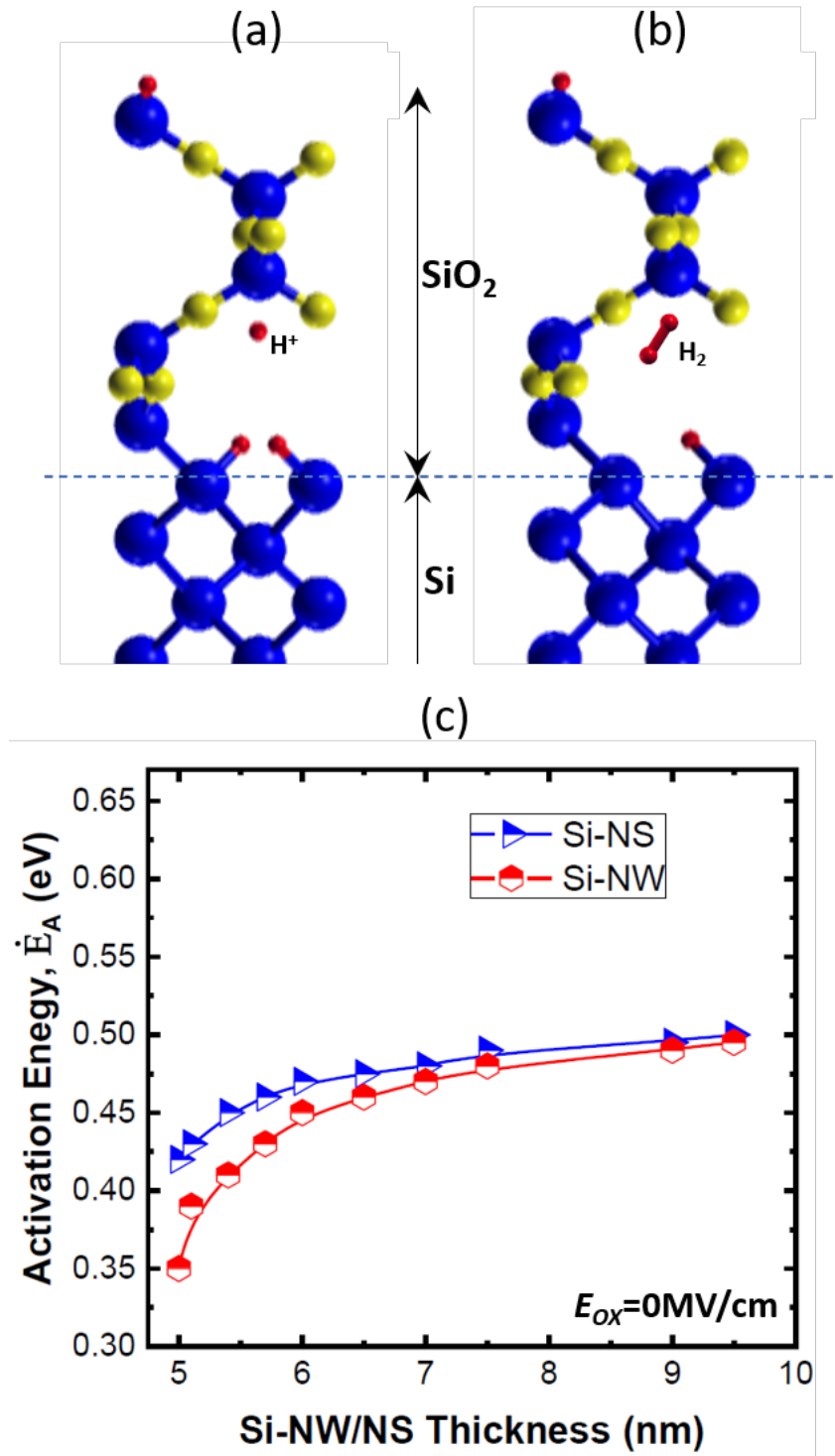


Fig. 5.2. (a) Process of Si-H bond dissociation in Si-SiO₂ interface. (b) Energy landscape of Si-H bond dissociation signifying the presence of an activation barrier (E_A). (c) activation energy E_A for Si-NS and Si-NW with different thickness and diameter, respectively.

exert a force on this dipole, which is proportional to the electric-field. Due to this additional force, that stretches the Si-H bonds, the activation energy for the Si-H bond dissociation decreases with the increase in electric-field. This phenomena has been investigated in the work by J. W. McPherson et al. [17], where they developed a thermo-chemical model to include the dipole effect showing how that lowers thermal barrier justifying through experimental results. However, an animistic calculation of such barrier lowering is never being attempted, which can potentially be important for scaled Si-NW and Si-NS channel.

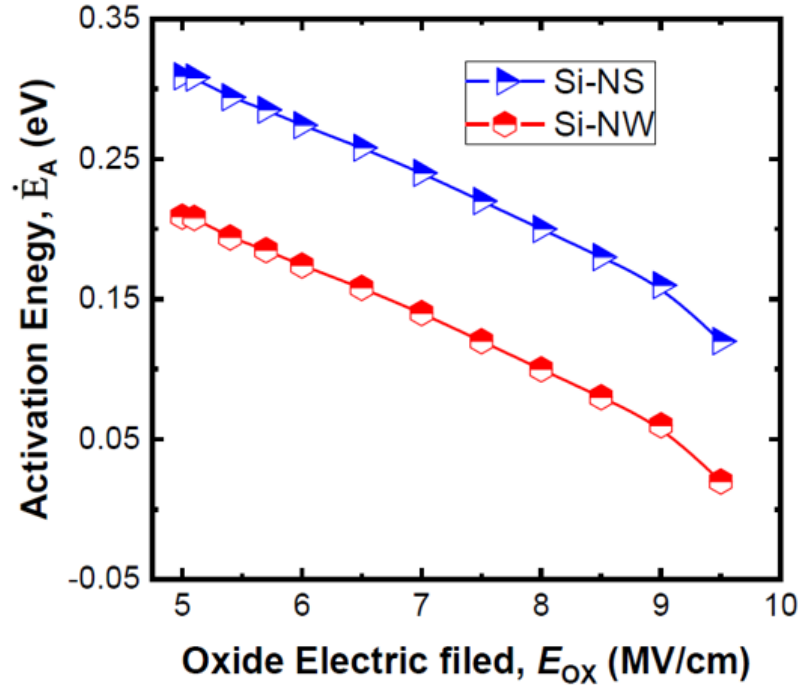


Fig. 5.3. Activation energy E_A for Si-NS and Si-NW with different oxide electric-field (E_{OX}). Here, we consider the Si-NS (NW) with a thickness (diameter) of 5nm.

To that effect, we have computed the E_A for a Si-H bond dissociation considering different electric-field in the SiO_2 layer based on DFT+NEB simulation. Our simulation results suggest that the E_A decreases with the increase in oxide electric-field (E_{OX}) as shown in Figure 5.3. This is due to the formation of electric dipoles in

the presence of electric-field and therefore, the Si-H bonds become more prone to dissociate.

6. DEFECT INDUCED RELIABILITY IN GAA-FET AND MBC-FET

In this chapter, we focus on analyzing the time-dependent generation of defect states at the Si-SiO₂ interfaces in transistors and evaluating device performance under that circumstance from the long-term reliability aspect. Section 6.1 discusses the generation of defect states and analyze it in the context of scaling. Section 6.2 discusses the reliability concern NBTI and its mechanism. Section 6.3 shows a physical model for defect generation.

6.1 Negative Bias Temperature Instability (NBTI)

The most common reliability issues for logic transistors are Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB). Among the, NBTI appears to be the most dominant component in scaled transistors. Hence, in this chapter, we focus on NBTI induced reliability issues in GAA-FET and MBC-FET.

NBTI is a temperature-accelerated degradation phenomenon experienced by p-type MOSFET. It was first recognized in the 1960s as a device reliability issue. At that time, it was not regarded as a very serious problem. But now-a-days it is considered as one of the common reliability concerns. Since the transistor technology trend is experiencing rapid down-scaling, the oxide layers have also been scaled below 2nm in the current technology nodes. However, the supply voltage did not undergo such a significant scaling. As a result, the corresponding oxide electric field increases. Hence, the NBTI has become a common degradation process faced by current transistors.

In p-type transistors, NBTI leads to defects at the Si-SiO₂ interface. In general, the main two reasons that causes the bias temperature instability are (i) the trapping of positively charged holes and (ii) that supplies the required energy for Si-H bond dissociation at the Si-SiO₂ interface. Such phenomena leads to a defect states with positive charge at the interface. As a result, the threshold voltage of the device changes with the increase in defect charge at the interface. The dynamic change in threshold voltage, $V_T(t)$ with respect to the interface defect density can be written as the following equation.

$$V_T(t) = V_{T0} + \Delta V_T(t) = V_T + \frac{qN_{it}(t)}{C_{OX}} \quad (6.1)$$

Here, V_{T0} is the threshold voltage without any defects; V_T is the threshold voltage with defects; N_{it} is the interface defect density; C_{OX} is the capacitance of the gate oxide; and q is the electron charge. As N_{it} increases over time, the threshold voltages also deviates. Such a dynamic change in threshold voltage leads to a shift in device characteristics and if the change is significant, the device may fail to operate the way it was supposed to be. Such a scenario is called breakdown. Now, to analyze the NBTI induced reliability issues in GAA-FET and MBC-FET, we utilize a well-established model, which we discuss next.

6.2 Reaction-Diffusion Model for NBTI

According to the R-D model, when a gate voltage is applied, it initiates an electric-field dependent reaction at the Si/SiO₂ interface that generates interface traps by breaking the passivated Si-H bonds. Further, some H converts to H₂ and as the H diffusion is a slower process, H removal is mostly happened by H₂ diffusion. Within the R-D framework, the trap density (N_{IT}) and the corresponding change in threshold voltage (ΔV_T) with respect to time (t) can be calculated from the following equations [18], [19]:

$$\frac{N_{IT}}{t} - \frac{\delta k_H}{k_r^2 N_{IT}^2} (k_f N_0 - \frac{N_{IT}}{t})^2 + \frac{\delta k_{H_2} N_{IT}}{\sqrt{6D_{H_2}t}} = 0 \quad (6.2)$$

$$\Delta V_T = \alpha \frac{qN_{IT}}{C_{OX}} \quad (6.3)$$

Here, k_f , k_r , and N_0 are defined as Si-H bond dissociation rate, Si-H bond reformation rate and the initial density of Si-H bonds before applying any gate voltage. k_H and k_{H_2} are the generation rate of H and H₂; D_H and D_{H_2} is the diffusion coefficient of H and H₂, and δ is the interfacial thickness (considered as $\sim 1.5\text{\AA}$ in this work). Now, the dependence of N_{IT} generation on the activation energy of Si-H bond dissociation (E_A) and the oxide electric-field (E_{OX}) is captured in k_f through the following equation [18], [19]:

$$k_f = A \times EOT \times E_{OX} \times \exp(-\hat{E}_A/k_B T) \quad (6.4)$$

Here, \hat{E}_A is the effective activation energy that depends on E_{OX} , which we have calculated from DFT simulation (shown in Figure 5.3), A is a fitting parameter, k_B is the Boltzmann constant, EOT is the effect oxide thickness which is considered 0.7 nm here, and T is the temperature. Now we utilize eqn. (6.2)-(6.4) to compute the shift in threshold voltage by including the electric field dependency and corresponding effective activation energy.

Figure 6.1 (a) shows the shift in threshold voltage (ΔV_T) with respect to time. The different lines here signify ΔV_T shifts for oxide electric field ranging from 5-10 MV/cm. Here we have considered the operating temperature $T=125^\circ\text{C}$ (398K). Our result implies that the degradation is faster for higher electric field. According to the general convention, when a transistor attains a threshold voltage shift of 50 mV or greater, the transistor will fail to operate and face breakdown. This failure criterion is shown with red dotted line in Figure 6.1 (a). We also see that each different oxide electric field requires different time period to reach the particular ΔV_T . These are shown with black dots Figure 6.1 (a). We extract the time period values to explore the relation between oxide electric field and time until device failure (device lifetime). Figure 6.1 (b) shows the relation between oxide electric field and device lifetime.

Our result suggests for a lifetime of 10 years the oxide electric field is 7.4 MV/cm. Figure 6.2 shows the relation between oxide electric field E_{OX} and gate voltage V_{GS}

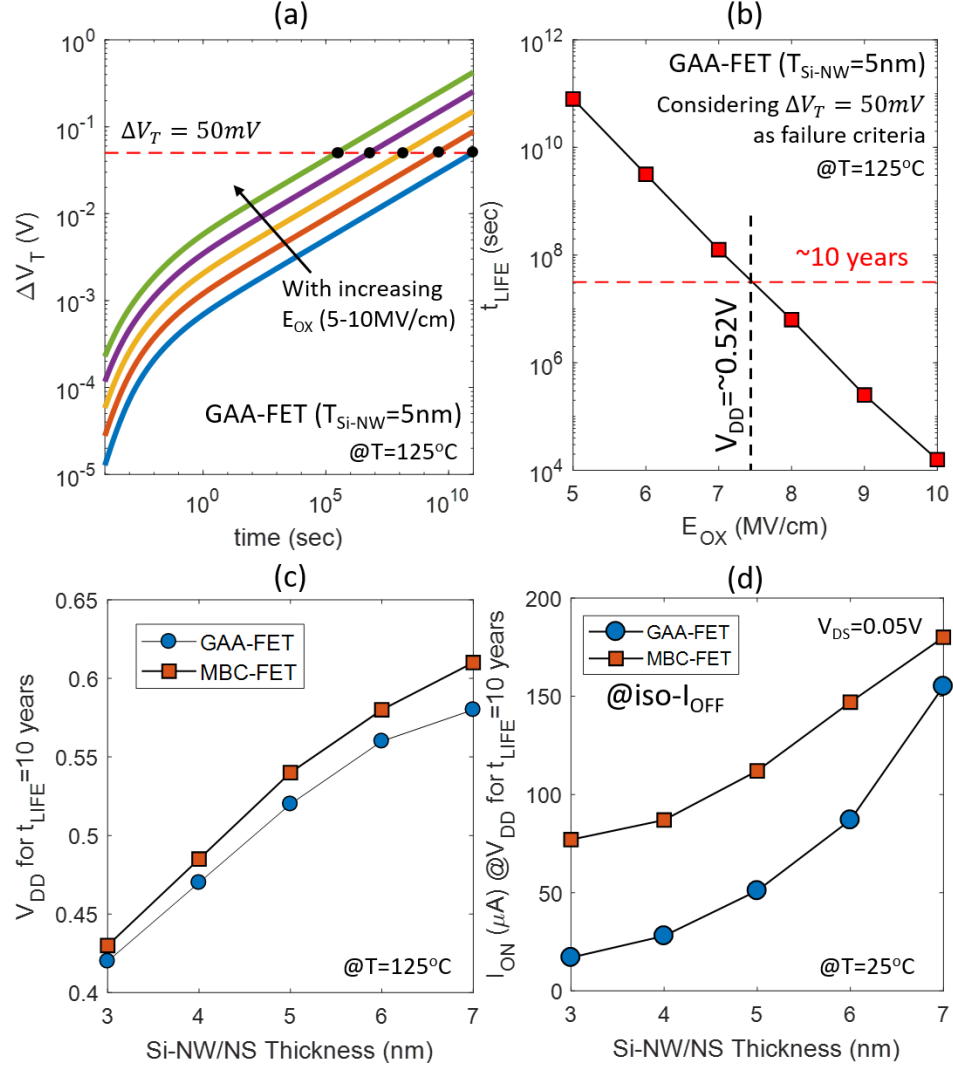


Fig. 6.1. (a) Shift in threshold voltage (ΔV_T) with different oxide electric-field (E_{OX}) for GAA-FET with $T_{Si-NW}=5nm$. (b) Corresponding device life-time (t_{LIFE}) prediction versus E_{OX} based on failure criteria of $\Delta V_T=50mV$ [19]. (c) Optimum operating voltage (V_{DD}) of GAA-FET and MBC-FET for 10 year life-time. (d) I_{ON} of GAA-FET and MBC-FET at optimum V_{DD} for 10 year life-time.

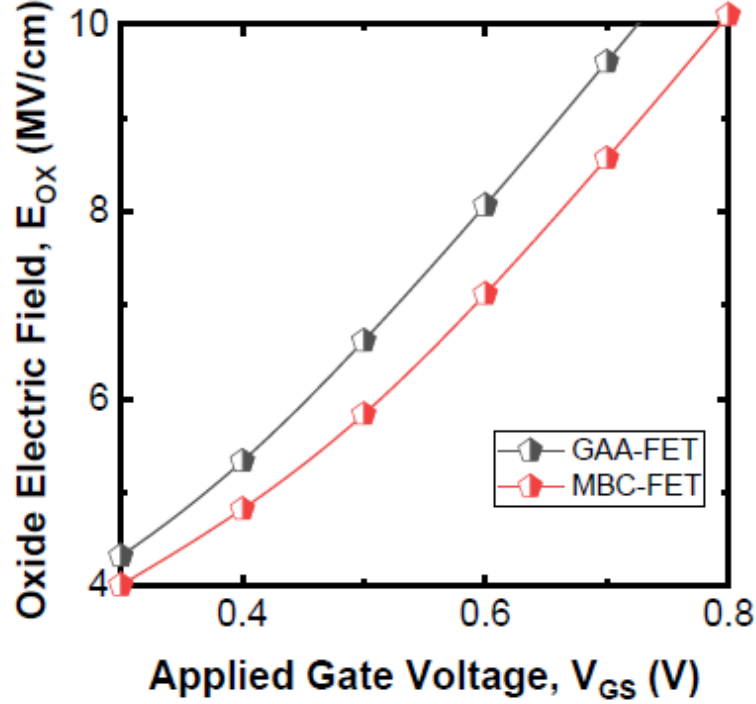


Fig. 6.2. E_{OX} versus gate voltage, V_{GS} for GAA-FET and MBC-FET obtained from device simulation.

obtained from device simulation. Using that we extract the corresponding gate voltage to 7.4 MV/cm is 0.52 V. Thus, we determine the safe operating voltage as 0.52V for this particular device.

We employ the same approach to compute the safe operating voltage for $t_{LIFE}=10$ years for GAA-FET and MBC-FETs. The results are described through Figure 6.1(c). Our results suggest that with scaling (i.e. decrease in thickness of NW/NS) the safe operating voltage for device also lowers. Using the calculated safe operating V_{DD} as the V_{GS} we now compute the device ON current which is the safe I_{ON} at iso-OFF-current (iso- $I_{OFF} \sim 0.1nA$) condition for the GAA-FETs and MBC-FETs. These results are shown in Figure 6.1 (d). The results suggest we get a decrease in I_{ON} due to scaling i.e. decrease in NW/NS thickness.

Our calculations suggest, while decrease in channel thickness gives better electrostatic control but that benefit comes with a cost of lower I_{ON} and lower V_{GS} for a targeted device lifetime. Whereas the alternate approach (higher electric field) will provide higher V_{GS} and higher I_{ON} , but at the cost compromised device lifetime.

7. SUMMARY AND OUTLOOK

7.1 Conclusion

In summary, by considering the $\text{SiO}_2\text{-Si-SiO}_2$ systems, we have analyzed the quantum confinement effects in on its bandgap for nanowire and nanosheet. We have evaluated the influence of thickness scaling on GAA-FET and MBC-FET based on first-principle DFT simulation and NEGF based device simulation. In addition, we have studied the effects of Si-H bond disassociation on Si-NW/NS characteristics in terms of quantum conductance and defect mediated trap-state generation. Further, we have established a relation between the Si-H bond dissociation energy and finite-size effect of Si-NW/NS, as well as its electric-field dependency. Our analysis suggests a decrease in the activation energy with the decrease in Si-NW/NS thickness and with the increase in oxide electric-field. Moreover, by employing R-D model of trap-state generation and utilizing the electric field and thickness dependent activation energies, we have analyzed the change in threshold voltage of GAA-FET and MBC-FET and determined the safe operating voltage for a life-time of 10 years. Our analysis signifies that - while scaling of Si-NW/NS thickness should provide better short-channel effect, at the same time, the trap state mediated conductance increases and the safe operating voltage decreases for a certain life-time of the device. As a consequence, the desired benefit of thickness scaling of Si-NW/NS based GAA/MBC-FET can potentially be suppressed. Therefore, it is suggested to investigate the possible mechanisms to increase the device reliability along with the thickness scaling of transistor channel.

7.2 Future Work

Our work suggests that, to mitigate the adverse effect of scaling on defect formation in ultra-scaled devices, some form of extensive engineering is required. To that effect, we envision the following tasks as the future work, which can possibly lead to the solution of these scaling problem:

- Investigating the effects of reverse bias voltage on the activation energy and recovery of defect states.
- Use of new oxide materials and that disfavours the Si-H bond dissociation.
- Use of other materials in place of H that makes stronger bonds with Si and hence, are less prone to defect generation.
- Investigating presence of catalyst as single atom or clusters around the interface to find out its effect on Si-H bond recovery after dissociation and before diffusion.

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