LITHIUM NIOBATE ACOUSTOELECTRIC PLATFORMS FOR INTEGRATED NON-RECIPROCAL RF MEMS DEVICES

by

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To my friends and family,
for their love and encouragement

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A_{in}	peak amplitude at the input probe point
A_{out}	peak amplitude at the output probe point
C_{s}	finger stack capacitance
E_{D}	applied drift electric field
F	fitness function for a constant forward amplitude
G_{s}	finger stack conductance
H	diffusion term
L_{f}	metal free length
L_{m}	metalized length
N	free carrier concentration
N_{elem}	number of mesh elements
N_{df}	evaluation point division factor
P	penalty function
Q	quality factor of the mode
R	space-charge reduction factor
R_{c}	metal IDT finger conductive losses
R_{elem}	element ratio
$\mathbf{S} = \{S_x, S_y, S_z\}$	material strain
T	temperature
V_1	drain voltage controlling a drift field in the forward direction
V_2	drain voltage controlling a drift field in the backward direction
V_{DC}	DC bias voltage
Z_{a}	interaction impedance
Z_{f}	metal free acoustic impedance
Z_{m}	metalized acoustic impedance
Δv_{a}	acoustic velocity shift
α^{AE}	acoustoelectric attenuation
α_{prop}	propagation attenuation

β_{a}	unperturbed acoustic propagation constant
β_{RD}	Rayleigh damping beta term
γ	dimensionless velocity
η_{RD}	loss factor for the Rayleigh damping beta term
λ	acoustic wavelength
μ	free carrier mobility
ω	acoustic wave frequency
ω_{D}	diffusion frequency
ω_{c}	dielectric relaxation frequency
ϕ	free region acoustic phase
ψ	metalized region acoustic phase
ε	material permittivity
φ	potential
ξ	penalty weight
b	dimensionless frequency term
d	semiconductor film thickness
d_{prop}	propagation distance between points
f_{free}	eigenfrequency with a free electric boundary condition
f_{ground}	eigenfrequency with a grounded electric boundary condition
h_{max}	maximum mesh size
k^2	piezoelectric coupling coefficient
k_{B}	Boltzmann constant
n	electron free carrier concentration
$n^{\mathrm{L}} = \ln(n)$	logarithmic electron free carrier concentration
p	hole free carrier concentration
$p^{\mathrm{L}} = \ln(p)$	logarithmic hole free carrier concentration
q	elementary charge
r_{T}	piezoelectric transformer ratio
$t_{\mathrm{step}}^{\mathrm{max}}$	maximum time step chosen for acoustoelectric simulation

t_{layer}	layer thickness
v_0	acoustic wave velocity without the presence of free carriers
v_{a}	acoustic wave velocity
v_{free}	SAW mode acoustic velocity with a free electric boundary condition
v_{ground}	SAW mode acoustic velocity with a grounded electric boundary condition
v_{f}	metal free acoustic velocity
v_{m}	metalized acoustic velocity

ABBREVIATIONS

ABR	acoustic Bragg reflector
ADS	Advanced Design System
AE	acoustoelectric
Al	Aluminium
Au	Gold
BAW	bulk acoustic wave
BOE	buffered oxide etch
BOX	buried oxide
BW	bandwidth
CFL	Courant–Friedrichs–Lewy
CMP	chemical-mechanical polishing
CV	capacitance-voltage
CW	continuous wave
DART	distributed acoustic reflection transducer
DOF	degrees of freedom
EWC	electrode width control
FEA	finite element analysis
GSG	ground signal ground
HEMT	high-electron-mobility transistor
HR	high resistivity
IC	integrated circuit
IDT	interdigital transducer
IFBW	intermediate frequency bandwidth
IL	insertion loss
IV	current-voltage
InGaAs	Indium Gallium Arsenide
InGaAs-LN	Indium Gallium Arsenide on Lithium Niobate
LN	Lithium Niobate

LNOSOI	Lithium Niobate on SOI
LNOSi	Lithium Niobate on Silicon
LSAW	leaky surface acoustic wave
MBVD	modified Butterworth-Van Dyke
MEMS	microelectromechanical systems
MIS	metal–insulator–semiconductor
MSC	multistrip coupler
NID	non-intentionally doped
PAE	power added efficiency
PDE	partial differential equations
PMMA	poly(methyl methacrylate)
RF	radio frequency
RIE	reactive-ion etching
RMS	root mean square
RMSC	reversing multistrip coupler
SAW	surface acoustic wave
SEM	scanning electron microscope
SH_0	shear horizontal Lamb mode
SiO_2	Silicon Dioxide
SMU	source measure unit
SOI	silicon on insulator
SOLT	short open load through
STAR	simultaneous transmit and receive
S_0	symmetric Lamb mode
Si	Silicon
Tx/Rx	transmit/receive

ABSTRACT

Some of the biggest challenges with analog signal processing at radio frequencies (RF) are: RF loss at the frequency of interest, large enough fractional bandwidth, and sufficient delay. It is difficult to achieve enough delay in radio front ends using a purely electromagnetic approach since it is limited to a fraction of the speed of light. A solution has been the use of acoustic RF devices, such as surface acoustic wave (SAW) delaylines and MEMS filters. For some acoustic RF devices, like high performance Transmit and Receive SAW correlators, the long delays introduce significant propagation losses. These propagation losses can be compensated within the device by integrating a low noise amplifier into the acoustic correlator architecture. This can be accomplished by designing the SAW correlator on a high performance acoustoelectric (AE) platform. The AE effect is a phenomenon where nearby free carriers can interact with a travelling acoustic wave. Free carriers in close proximity to a piezoelectric material can interact with a travelling acoustic wave through its periodic potential. When a drift field is applied, depending on the relative velocity difference between the free carriers and acoustic wave, energy can either be transferred into (amplification) or out of (attenuation) the acoustic wave.

This thesis investigates the design and feasibility of AE MEMS devices on several Lithium Niobate (LN) platforms. First, the key acoustic and free carrier parameters are discussed and optimized for an ideal high performance AE material stack. In order to debug and analyze the performance of intermediate steps in the process of making high performance AE MEMS devices, three LN-based platforms are used throughout this work. These platforms help further examine some of the key challenges associated with making a high performance AE platform, like wafer bonding, fabrication, device design, and device operating conditions. These material stacks consist of: thin film LN bonded to a silicon wafer (LNOSi), thin film LN bonded to a silicon on insulator wafer (LNOSOI), and epitaxial indium gallium arsenide bonded to a LN wafer (InGaAs-LN).

The acoustic and piezoelectric performance of SAW devices on the LNOSi and LNOSOI platforms are modeled using COMSOL Multiphysics. A full study is performed to determine the piezoelectric coupling coefficient variation vs. device wavelength, propagation angle,

transducer metal, and acoustic mode. A lumped element cross-field Mason model is modified to include substrate conductivity and simulated in Advanced Design System (ADS) software. SAW delaylines are then fabricated with both aluminum (Al) and gold (Au) Interdigital Transducers (IDT) and measured to compare to the simulated results. The analytical AE theory is then presented and calculations are performed to determine the desired (optimum) carrier concentration for AE devices. In addition to the 1D analytical AE model, initial work is done on developing a generalized 2D Finite Element Analysis (FEA) AE modeling scheme in COMSOL. The results for a piezoelectric semiconductor bulk acoustic wave (BAW) resonator and SAW delayline amplifier are presented.

On the LNOSi platform, gate controlled passive AE delaylines are fabricated and measured to examine the effects of LN bonding on Silicon free carrier concentrations and interface charges. Then, the fabrication and initial measurement results for doped Silicon AE delayline amplifiers are outlined. Based on the device design, the non-reciprocal nature of the AE effect can be used for more than just amplification and loss compensation. Using the InGaAs-LN platform, several classes of AE devices are designed and tested in pulsed mode operation. First, a series of segmented AE delayline amplifiers are measured to look at how the relative AE gain performance and input DC power scale with acoustic frequency, segment unit length, and number of segments. By taking advantage of the non-reciprocal shift in acoustic velocity, a dual-voltage AE delayline phase shifter is designed and tested. Routing of the acoustic waves between parallel delaylines can be accomplished through multistrip couplers (MSC) and can increase the library of possible AE device designs. The simplest example is a 3-port AE switch, which is designed and tested. The demonstration of these AE MEMS devices opens the door to a larger library of non-reciprocal acoustic devices utilizing the AE effect in high performance integrated material platforms.

1. INTRODUCTION

1.1 Motivation

The field of microelectromechanical systems (MEMS) has expanded over the years to reach more disciplines and make its way into our every day lives. Surface acoustic wave (SAW) devices in particular have found many applications, ranging from chemical and biological sensors to inertial sensors, oscillators, and filters. These SAW devices typically use a piezoelectric material to convert electromagnetic energy into a mechanical wave. This transduction from radio frequencies (RF) to the acoustic domain is accomplished through an interdigital transducer (IDT). The addition of a semiconductor layer to these piezoelectric SAW platforms opened up new avenues for acoustic RF devices, like acoustic charge transport delaylines [1] and electro-acoustic convolvers or correlators [2, 3]. Specifically, SAW correlators have been of interest for RF correlation using a Simultaneous Transmit and Receive (STAR) radio architecture. The challenge with these analog correlators in a Transmit and Receive (Tx/Rx) radio is illustrated in Figure 1.1.

After the desired signal is encoded at the transmitter, it experiences an in-band jammer signal that significantly reduces the signal to noise ratio. If the receiver has the encoding

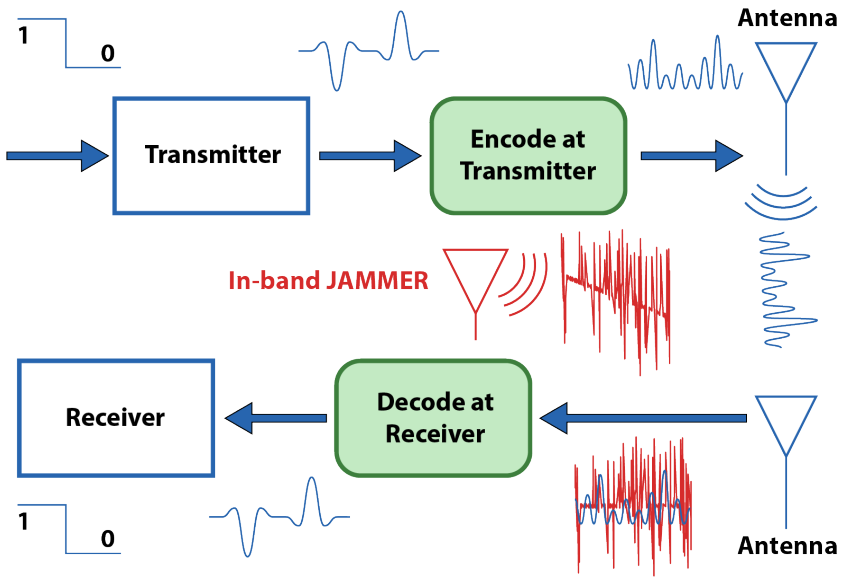

Figure 1.1. Illustration of a Tx/Rx radio in the presence of an in-band jammer signal.

scheme, the signal can be decoded and the original signal recovered given a sufficient amount of processing gain. The major challenge with an analog correlator implementation is the excessive attenuation of the desired RF signal. In order to achieve the necessary processing gain and data rate to recover the signal from an in-band jammer signal, a very long delay with hundreds of segments is required. SAW delaylines with long delays have large propagation losses, which results in significant insertion loss (> 20 dB). These losses also reduce the signal level at each tap, which will degrade the signal to a point where the weighted coding scheme can no longer recover the desired signal.

These propagation losses can be compensated for within the device by integrating a low noise amplifier into the acoustic correlator architecture. This can be accomplished by designing the SAW correlator on a high performance acoustoelectric (AE) platform. Within each segment of the correlator, a small AE amplifier will be implemented before each tap, compensating for the propagation loss and scattering loss within each segment. Additionally, there will be an AE amplifier before the first chip to compensate for the insertion loss of the input IDT. The AE effect has also been shown to have a low noise figure [4], which will contribute minimally to the total noise figure of the system. An initial demonstration of this SAW AE correlator architecture has been shown on a Gallium Nitride (GaN) material platform [5]. This platform, however, is not ideal for developing AE devices due to the low piezoelectric coupling coefficient and high carrier concentration. In this thesis, several material platforms will be investigated for the design of high performance AE RF MEMS devices.

1.2 Acoustoelectric Effect

The AE effect is a result of the interaction between free charge carriers and the electrical deformation potential produced by a propagating elastic wave in the piezoelectric material. When an external DC electric field is applied across the semiconductor in the direction of the propagating wave, a drift velocity is imparted to the free carriers. If the drift velocity is slower than (or opposite to) the acoustic wave velocity, the electrical deformation potential lags behind the strain field of the travelling acoustic wave. This phase lag not only decreases

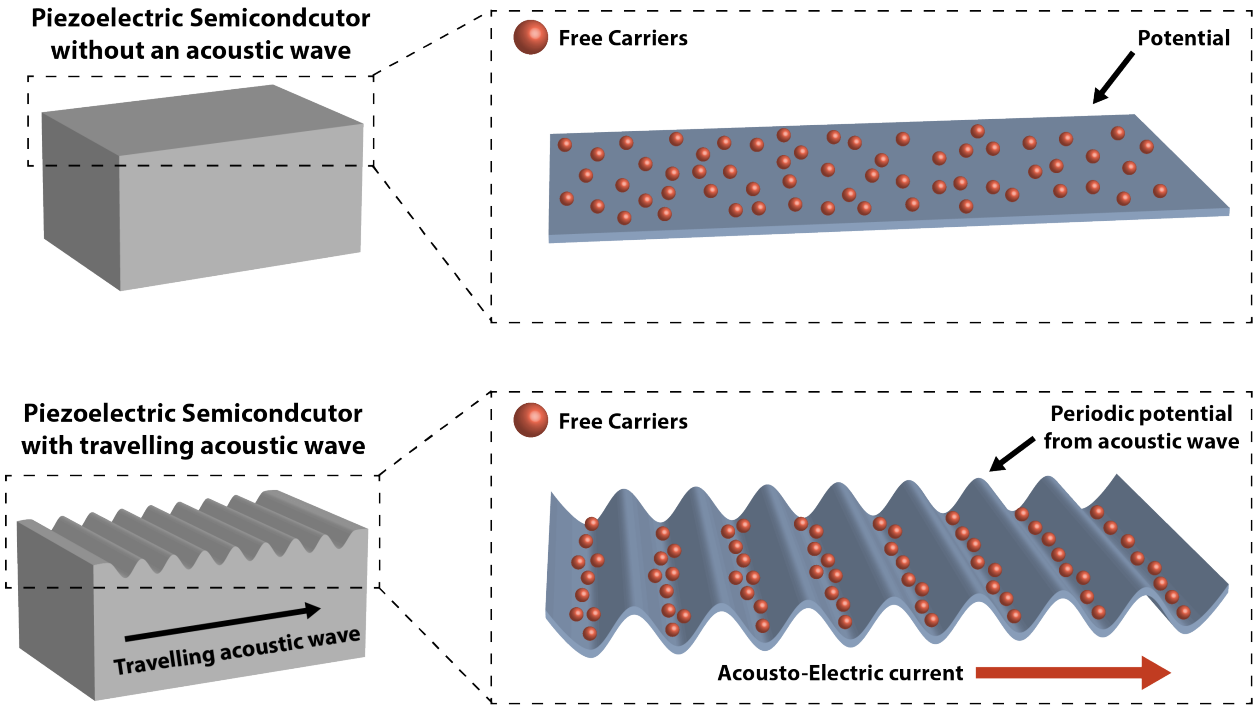

Figure 1.2. Illustration of the AE effect and how it relates the potential, acoustic wave, and free carriers.

the acoustic wave velocity, but also transfers energy from the acoustic wave to the electrons, increasing the acoustic losses. When a sufficient DC field is applied to cause the drift velocity to exceed the acoustic wave velocity, the electrical deformation potential now leads the strain field. This transfers energy from the electrons to the acoustic wave, resulting in an increased acoustic velocity and net acoustic gain [6].

Figure 1.2 shows an illustration of the AE effect in a piezoelectric semiconductor material. Without the presence of an acoustic wave, the free carriers are uniformly distributed within the material with an unperturbed potential. The strain field from the travelling acoustic wave creates a periodic potential in the material and the free carriers bunch in the potential wells generating an AE current. There was a lot of initial research done on the AE effect in piezoelectric semiconductors [7–12] and later extended to piezoelectric semiconductor thin film heterostructures.

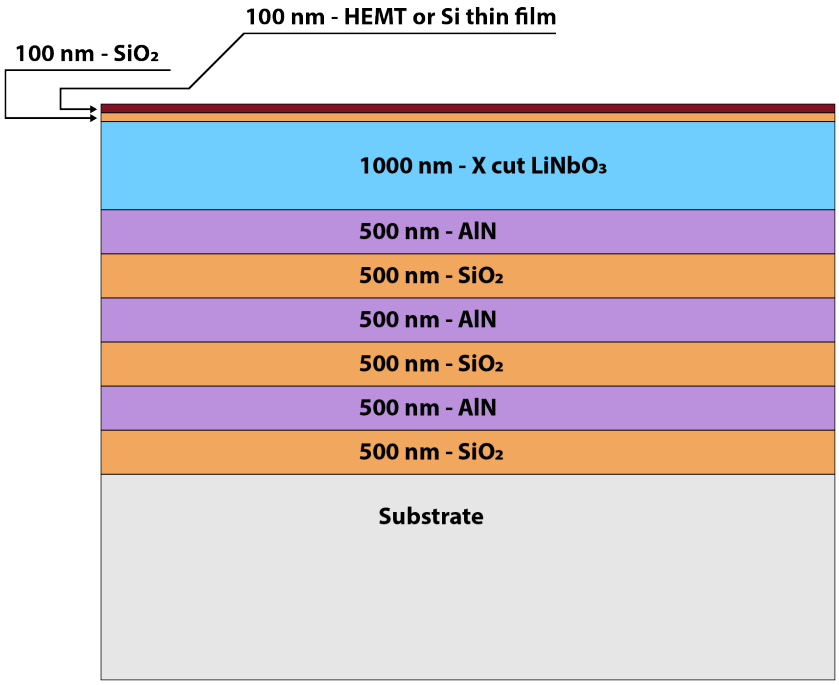

Figure 1.3. Illustration of a designed high performance AE platform.

1.3 High Performance Acoustoelectric Material Platforms

Lithium Niobate (LN) has been used extensively for acoustic RF devices in the MHz – GHz regime because of the material's high piezoelectric coupling coefficient, which allows for efficient conversion between electrical and mechanical energy. Typical cuts of LN for acoustic devices are either the 128° Y or Y-cut, which have high coupling coefficients for the Rayleigh SAW mode of 5.5% and 4.5%, respectively [13]. There has recently been interest in the X-cut of LN for Lamb mode devices because of the much higher coupling coefficient of both the Symmetric (S_0) and Shear Horizontal (SH_0) modes. Experimentally, these modes have been shown to have coupling coefficients in excess of 30% [14, 15]. The key challenge with scaling acoustic devices that use the S_0 or SH_0 mode is the release process. It would be difficult, for example, to reliably release either a long AE amplifier design [16], or a long acoustic correlator which requires hundreds of chips. One solution is to bond a thin film of LN to an Acoustic Bragg Reflector (ABR) substrate [17–19].

Figure 1.3 shows an example high performance AE platform utilizing a solidly mounted LN thin film. Alternating layers of AlN and SiO_2 act as an ABR for the SH_0 mode of

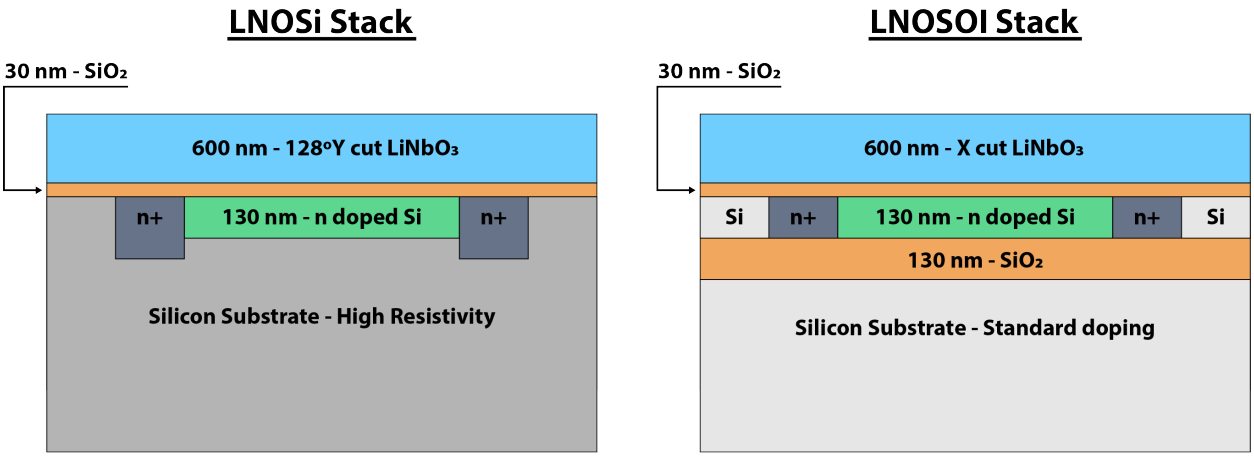

Figure 1.4. Illustration of the LN on Si (LNOSi) and LN on SOI (LNOSOI) platforms used in this work.

the LN thin film. This allows for an entirely unreleased device platform without the need to etch through the LN. Another important component is the semiconductor layer. FD-SOI wafers are already used for RF CMOS processing, so by bonding an FD-SOI wafer to the LN ABR stack [20], the AE platform can take advantage of the established silicon processing for controlling the free carriers through implantation. Also, the CMOS circuitry can be integrated on the bonded wafer stack. Most importantly, the direct bonding of the SOI wafer and LN ABR wafer allows for close proximity between the acoustic wave and free carriers. This will allow for the maximum AE interaction and ultimately very high performance AE devices.

1.3.1 Thin Film Lithium Niobate on Silicon/SOI

Since the development of the ideal LN ABR bonded to FD-SOI material stack will be very time consuming, two material stacks with shorter development times will be investigated in this thesis. These two material stacks will help test and debug different steps of the bonding and fabrication process as well as test initial concepts of non-reciprocal AE devices. The first stack shown in Figure 1.4 is a 128° Y-cut LN thin film bonded to a High Resistivity (HR) Silicon wafer (LNOSi). The 128° Y-cut was chosen because it has the highest coupling coefficient for Rayleigh SAW modes. The LNOSi material stack was chosen to test unreleased

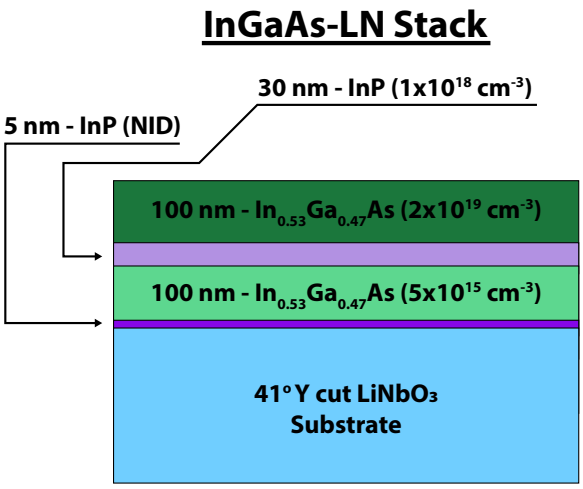

Figure 1.5. Illustration of the InGaAs-LN material platform fabricated at Sandia National Labs.

AE devices using the Rayleigh SAW mode. The HR Silicon wafer allows for a low enough carrier concentration where there will be no significant AE effect. Previous work in our group on the LNOSi platform used a top gate metal to control the carrier concentration [21], but selective implanted regions are presented here to allow for precise patterned control of the free carriers used for the AE effect.

The second material stack in Figure 1.4 is an X-cut LN thin film bonded to an implanted PD-SOI wafer (LNOSOI). By etching the Silicon substrate, released X-cut LN films with the bonded Si device layer attached can be used to investigate high performance AE devices using the S_0 or SH_0 mode of LN [22–24]. Also, by starting with known substrate and implanted free carrier concentrations, the effects of the bonding process can be investigated through any measured differences in expected AE performance.

1.3.2 InGaAs on Lithium Niobate

So far, all of the high performance AE material platforms presented use a LN thin film to make use of the high k^2 S_0 and SH_0 modes. There are some cuts of bulk LN that have high k^2 SAW modes as well. In particular, the 41° Y-cut, X-propagating LN Leaky SAW (LSAW) mode has low propagation loss and $k^2 = 17\%$ [25]. Sandia National Labs has

developed a high performance AE platform using this 41° Y-cut LN bonded to an InGaAs thin film [26]. Figure 1.5 shows an illustration of this material platform. Before the bonding process, the InGaAs heterostructure is epitaxially grown on an InP wafer. The top InGaAs (2 x 10^{19} cm^{-3}) and InP (1 x 10^{18} cm^{-3}) layers are needed to make Ohmic contact to the InGaAs (5 x 10^{15} cm^{-3}) layer used for AE interactions. The thin 5 nm InP capping layer is intended to protect the InGaAs layer during the bonding process and maintain the desired carrier concentration for the AE effect. In this thesis, several AE SAW device designs were fabricated at Sandia on this material stack and proof of concepts were demonstrated on this high performance AE platform.

1.4 Thesis Outline

There has been increasing interest in developing a platform that can integrate all acoustic RF devices needed in the radio front end. This integration requires compact non-reciprocal elements and acoustic signal routing elements in order to achieve all the desired acoustic RF devices. The non-reciprocal AE effect has been investigated in various material platforms for use as RF amplifiers and charge transport devices. Recently, there has been work on the AE effect in high coupling coefficient integrated piezoelectric material platforms. These material platforms can also leverage multistrip couplers for acoustic signal routing between SAW delaylines. This thesis looks to investigate the feasibility of developing a high performance AE material platform for a library of integrated acoustic RF devices.

Chapter 1 gives an introduction to piezoelectric acoustic RF devices as well as an introduction to the acoustoelectric effect. Then, some key parameters for designing a high performance AE platform are discussed along with a brief introduction to the material platforms used in this thesis.

Chapter 2 covers the analytical and FEA modeling of the piezoelectric coupling coefficient for the acoustic SAW modes on the LNOSi and LNOSOI platforms. The FEA simulation setup in COMSOL is detailed and the results are presented. Then, a lumped element cross-field Mason model with added substrate conductivity is presented and used to fit to measured SAW delaylines on the LNOSOI platform. The extracted piezoelectric coupling coefficients

from COMSOL and ADS are then compared. Finally, the trade off between piezoelectric coupling coefficient and quality factor in these SAW modes is discussed.

Chapter 3 starts with an introduction to the analytical AE theory for piezoelectric semiconductors. Then, the Rayleigh wave amplifier model for thin film piezoelectric semiconductor heterostructures is presented and used in the remainder of the thesis. The optimal carrier concentration is determined to maximize both the absolute AE interaction strength and the relative strength between the forward and backward propagating acoustic waves. The second section of this chapter covers the AE FEA modeling development. An overview of the COMSOL implementation is followed by two example AE FEA simulations: a piezoelectric semiconductor BAW resonator and a piezoelectric semiconductor SAW delayline.

Chapter 4 covers the AE devices on the LNOSi platform. It starts with the theory, fabrication, and measurement of a gate controlled passive AE delayline. The results show an increase in the interface trap charge density and negative fixed charge density after the LN bonding process. The second section covers the work on active AE delaylines on the doped Silicon LNOSi platform. The full wafer and chip level fabrication process is detailed, followed by the non-reciprocal S-parameter results. The trapped charges from LN bonding and substrate current effects limited the possible non-reciprocity observed.

Chapter 5 contains all the AE work done on the InGaAs-LN platform. The fabrication was performed at Sandia National Labs and the fabrication process flow is briefly outlined in the first section. Then, the segmented AE amplifier performance is evaluated over a range of parameters, including the trade-off between AE gain and input DC power. The dual-voltage AE amplifier makes use of two independent drain voltages to leverage varying AE performance between the forward and backward propagating waves. A fitness function is developed for a fixed forward gain with variable backward isolation and variable forward phase. The device is then measured and compared to the fitness function theory. Finally, signal routing is incorporated in a 3-Port AE switch through multistrip couplers and the relative insertion loss is compared for all switch paths.

Chapter 6 concludes the results of the thesis and discusses the future work on these AE platforms, which includes expanding the library of AE devices on both the InGaAs-LN and LNOSOI platforms.

2. PIEZOELECTRIC SAW DELAYLINE MODELING

For the AE material platforms investigated in this thesis, understanding the acoustic and piezoelectric behavior of the mechanical modes is a crucial step in the design of high performance AE RF MEMS devices. This chapter will cover the COMSOL modeling, ADS simulations, and fitting methodology for the piezoelectric coupling coefficient (k^2) for various SAW modes used throughout this thesis. The chapter will start with detailing the k^2 simulation setup using COMSOL Multiphysics, including setting up the COMSOL-MATLAB LiveLink workflow on Purdue's Rice compute cluster. Then, Rayleigh SAW mode k^2 simulations are performed and discussed for the LNOSi platform. The simulations for the LNOSOI platform are expanded to include various propagation angles, mode shapes, and metal loading effects. The second section covers the development of a lumped element cross-field Mason model implemented in Advanced Design System (ADS) software to model the SAW delaylines. In the final part of this chapter, SAW delaylines on LNOSOI are fabricated and used in ADS to fit key acoustic and piezoelectric parameters to compare with the corresponding COMSOL simulations.

2.1 COMSOL Simulations

Due to the anisotropic nature of LN, the piezoelectric coupling coefficient on a thin film LN material platform can vary depending on the penetration depth and propagation angle of the SAW wave. A modeling scheme in COMSOL was used to simulate Rayleigh modes in LNOSi and additionally Shear Horizontal (SH) SAW modes in LNOSOI. This section will start with an outline of the simulation process flow on the Rice compute cluster at Purdue. Then, the metalized and unmetalized Rayleigh SAW mode simulations as a function of acoustic wavelength on LNOSi are presented. For the LNOSOI platform, the simulation parameter space is expanded to include propagation angle, IDT metal type, and SAW mode type. The simulation results are displayed as surface plots as a function of wavelength and propagation angle for both the Rayleigh and SH SAW modes. Finally, fabrication variability studies are performed for a few key propagation angles of interest and presented.

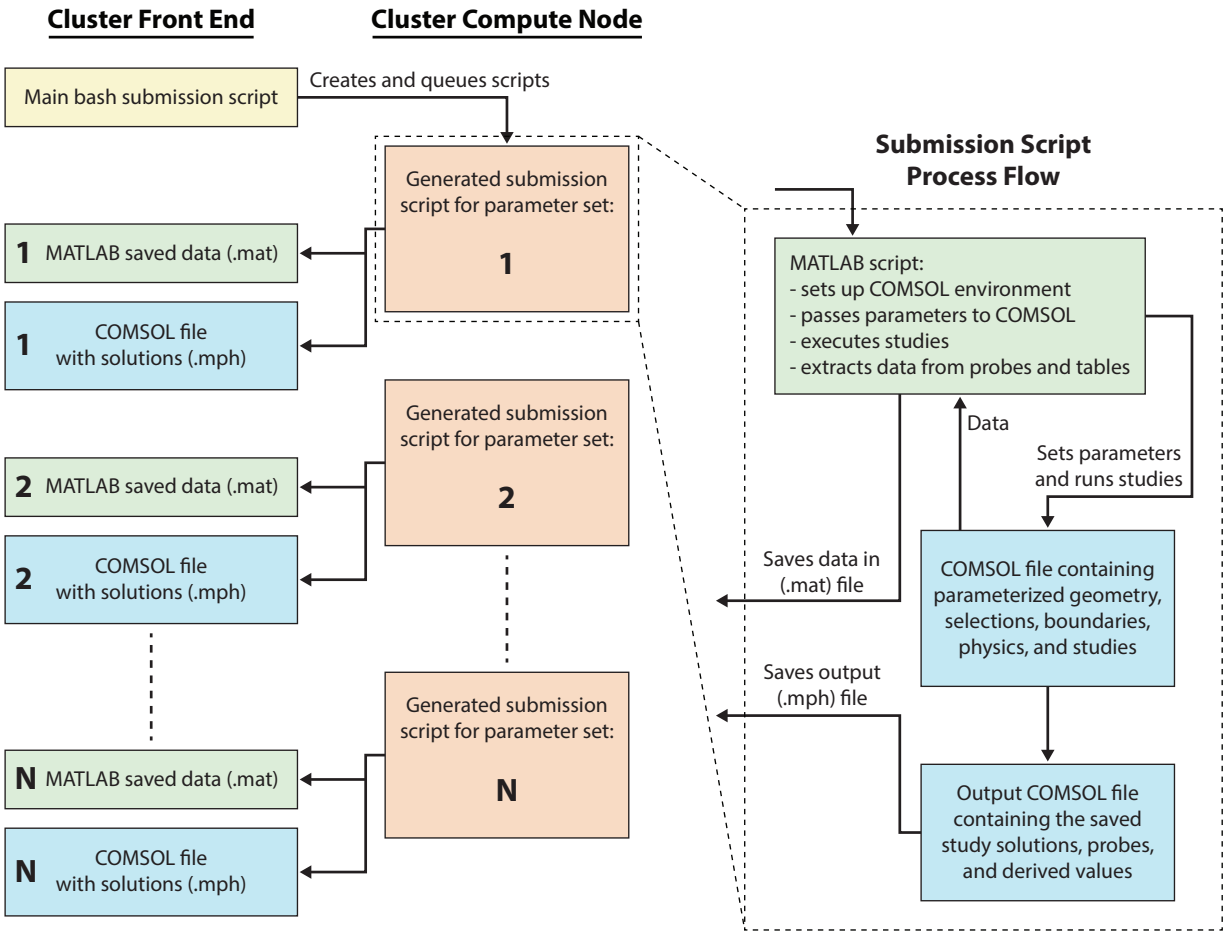

Figure 2.1. Flowchart showing the workflow for the COMSOL-MATLAB LiveLink setup on the Purdue Rice cluster.

2.1.1 LiveLink Setup and Meshing Algorithm

In order to help facilitate the process of simulating a large number of parameterized COMSOL simulations and to take advantage of the computational resources available at Purdue, a COMSOL-MATLAB LiveLink workflow was established to run on the Rice computational cluster. The Rice cluster consists of 4 front end nodes and 576 compute nodes. Each node contains 20 processor cores, 64 GB of RAM, and 56 Gbps Infiniband interconnects. Figure 2.1 shows the workflow for running simulations on the cluster using the Linux bash shell. There are four main file types used in this workflow: a main bash submission script (yellow), PBS submission scripts (orange), MATLAB related file types (green), and COMSOL related file types (blue).

The bash submission script contains all of the parameters used to setup the PBS scheduler for placing the jobs in the queue, and all the parameters that need to be passed to COMSOL and MATLAB based on the job specific simulations desired. When the submission script is executed, it writes and automatically submits all of the submission scripts to the PBS scheduler on Rice. Once a job moves from the queue to a compute node, it passes all parameters to a MATLAB function and runs MATLAB. The MATLAB script opens and sets up the environment for a COMSOL server and COMSOL simulation file, sets the parameters in the COMSOL file, executes the studies, and extracts probes and derived values from tables in the COMSOL file. At this time, a secondary COMSOL (.mph) file is saved containing all of the simulation results and solutions states. The MATLAB script finishes by saving all of the extract data in a (.mat) file. The submission script closes COMSOL and MATLAB and then copies the (.mat) data file and secondary (.mph) COMSOL file back to the front end working directory.

One challenge to simulating these SAW modes over a range of wavelengths is automatically maintaining a smooth mesh transition between material layers over several length scales. By taking advantage of the workflow already established, a meshing algorithm was implemented in MATLAB to generate meshing parameters for each material layer based on the acoustic wavelength simulated. Using the arithmetic series mesh distribution option in COMSOL, each material layer thickness (t_{layer}) needs two inputs: an element ratio (R_{elem})

and number of mesh elements (N_{elem}). In order to find the relation between these parameters, first consider an arithmetic series

$$e_1 + e_2 + e_3 + \ldots e_{N_{\text{elem}}} = e_1 + [e_1 + \delta] + [e_1 + 2\delta] + \ldots [e_1 + (N_{\text{elem}} - 1)\,\delta]\,, \tag{2.1}$$

where δ is a constant value added to each successive element in the series. Since the first and last elements in the series are related by the element ratio ($R_{\text{elem}} e_1 = e_{N_{\text{elem}}}$), this additive term can be expressed as

$$\delta = e_1 \frac{R_{\text{elem}} - 1}{N_{\text{elem}} - 1}. \tag{2.2}$$

Additionally, the sum of the elements in the series is equal to the thickness of the material layer

$$t_{\text{layer}} = \frac{N_{\text{elem}}}{2} \left[2e_1 + (N_{\text{elem}} - 1)\,\delta\right]. \tag{2.3}$$

Equations (2.2) and (2.3) can be solved for the first and last elements in the series as a function of the layer thickness, element ratio, and number of elements in the series

$$e_1 = \frac{2\,t_{\text{layer}}}{N_{\text{elem}}\,(R_{\text{elem}} + 1)}, \qquad e_{N_{\text{elem}}} = \frac{2\,R_{\text{elem}}\,t_{\text{layer}}}{N_{\text{elem}}\,(R_{\text{elem}} + 1)}. \tag{2.4}$$

For each layer in the material stack, the elements touching every material interface are set equal. This creates a system of equations to solve for each material's number of elements and element ratio. For the thinnest material in the stack, a minimum of 3 mesh elements is forced if the layer thickness is thinner than the desired minimum mesh size.

Figure 2.2 shows three example meshes generated from this algorithm. The thinnest material layer was 30 nm, which is drastically alters the mesh distribution when scaling the acoustic wavelength over an order of magnitude from 1 μm to 12 μm. The next step is to perform a mesh convergence study using this meshing algorithm over a range of acoustic wavelengths. For each wavelength, a total of three propagation angles were simulated. The global error for k^2 is the sum of squares for all propagation angles when comparing mesh number i and $i+1$

$$\varepsilon^i_{k^2} = \sqrt{\sum_{\theta=1}^{3} \left(\frac{\left| k_\theta^{2\,(i)} - k_\theta^{2\,(i+1)} \right|}{k_\theta^{2\,(i)}} \right)^2}. \tag{2.5}$$

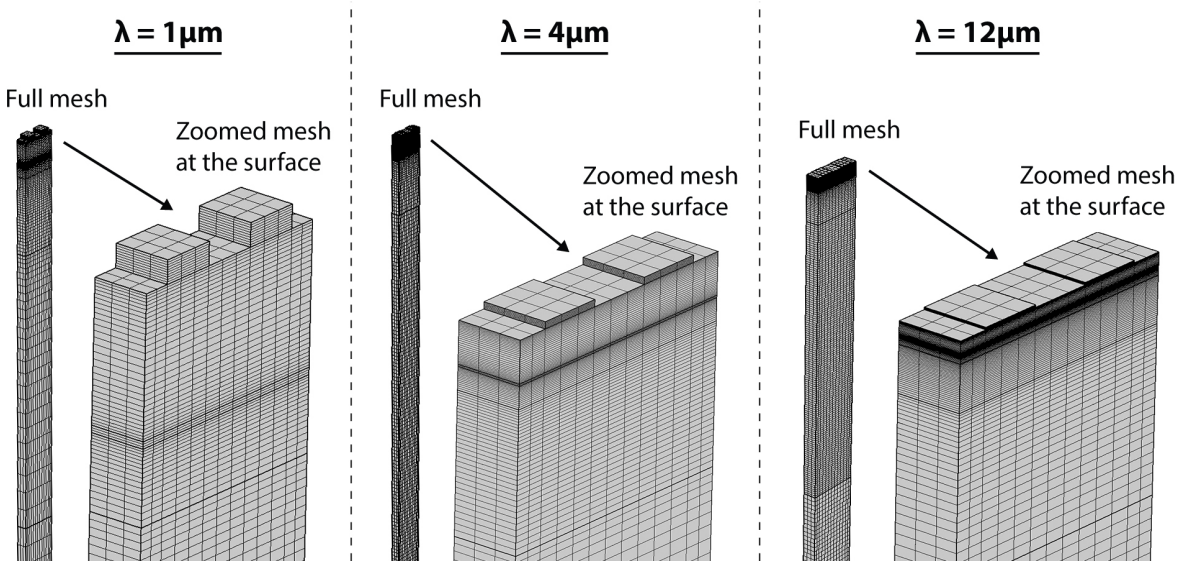

Figure 2.2. Example COMSOL generated meshes for three different acoustic wavelengths using the described meshing algorithm.

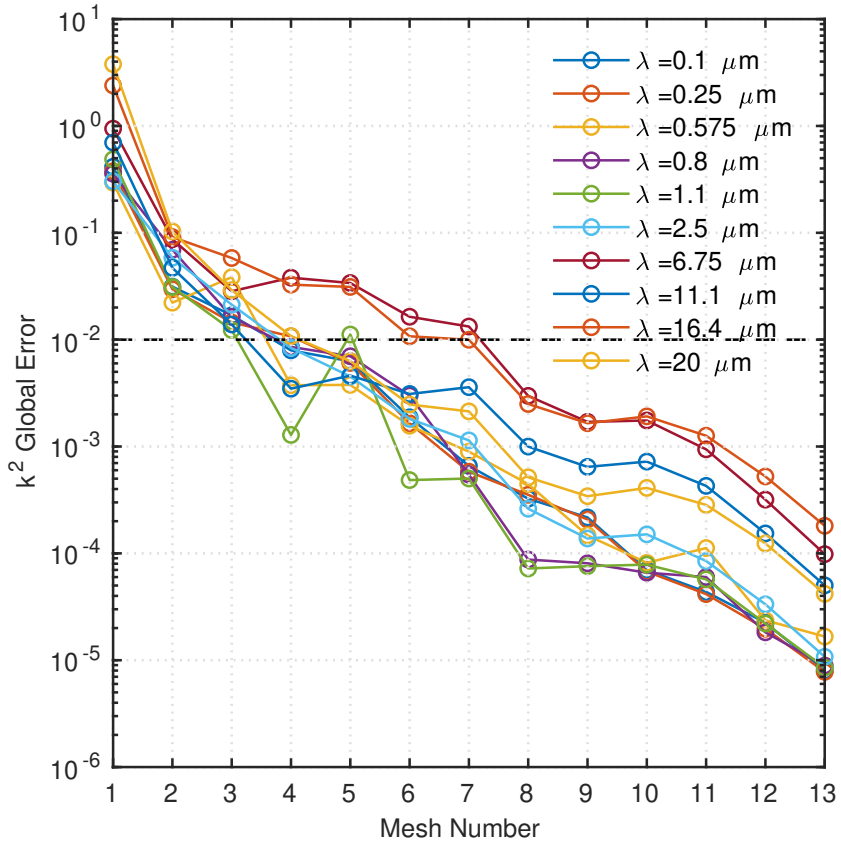

Figure 2.3. Global error for k^2 as a function of mesh number in the mesh convergence study. As the mesh number increases, the overall mesh gets finer and increases the DOF solved for.

The meshing algorithm generated a total of 14 meshes, where each successive mesh had more elements and Degrees of Freedom (DOF) to solve for. The maximum mesh size ranges from 1/2 of a wavelength for the coarsest mesh to 1/22 of a wavelength for the finest mesh. This leads to 13 k^2 global errors, which are plotted as a function of mesh number in Figure 2.3. As the number of mesh elements increase, the relative difference in k^2 solutions decreases. The global error is different depending on the acoustic wavelength solved for, so if a certain error tolerance is desired the mesh number chosen needs to have a global error below that threshold for all wavelengths simulated. For example, if a error tolerance of 0.01 is needed (dashed black line) then mesh number 8 would be the coarsest mesh that could be used.

2.1.2 LNOSi Simulations

The setup for COMSOL simulations of the Rayleigh SAW mode in the LNOSi stack is shown in Figure 2.4. The material thickness dimensions are all listed, as well as the definition of the acoustic wavelength (λ) and boundary conditions. The eigenvalues were simulated over one wavelength of the acoustic mode using periodic boundary conditions in the direction of propagation. A low reflecting boundary condition was also placed at the bottom of the Si substrate. The model was solved first with a free electrical boundary condition at the top of the LN thin film and again with a grounded electrical boundary condition. The shift in frequency is proportional to the coupling coefficient and can be calculated as

$$k^2 = \frac{\left|v_{\text{free}}^2 - v_{\text{ground}}^2\right|}{v_{\text{free}}^2} = \frac{\left|f_{\text{free}}^2 - f_{\text{ground}}^2\right|}{f_{\text{free}}^2}, \tag{2.6}$$

where v_{free} and v_{ground} are the SAW mode's acoustic velocity with a free and grounded electrical boundary condition at the LN surface, respectively. Since the acoustic wavelength is the same for both simulations, the k^2 can be calculated using the eigenfrequency of the free (f_{free}) and grounded (f_{ground}) simulations as shown in Equation (2.6).

The simulation results of the Rayleigh SAW k^2 vs. acoustic wavelength are shown in Figure 2.5. The coupling coefficient reduces as wavelength increases because of the SAW mode's penetration depth into the LNOSi stack. The Rayleigh SAW mode has most of its

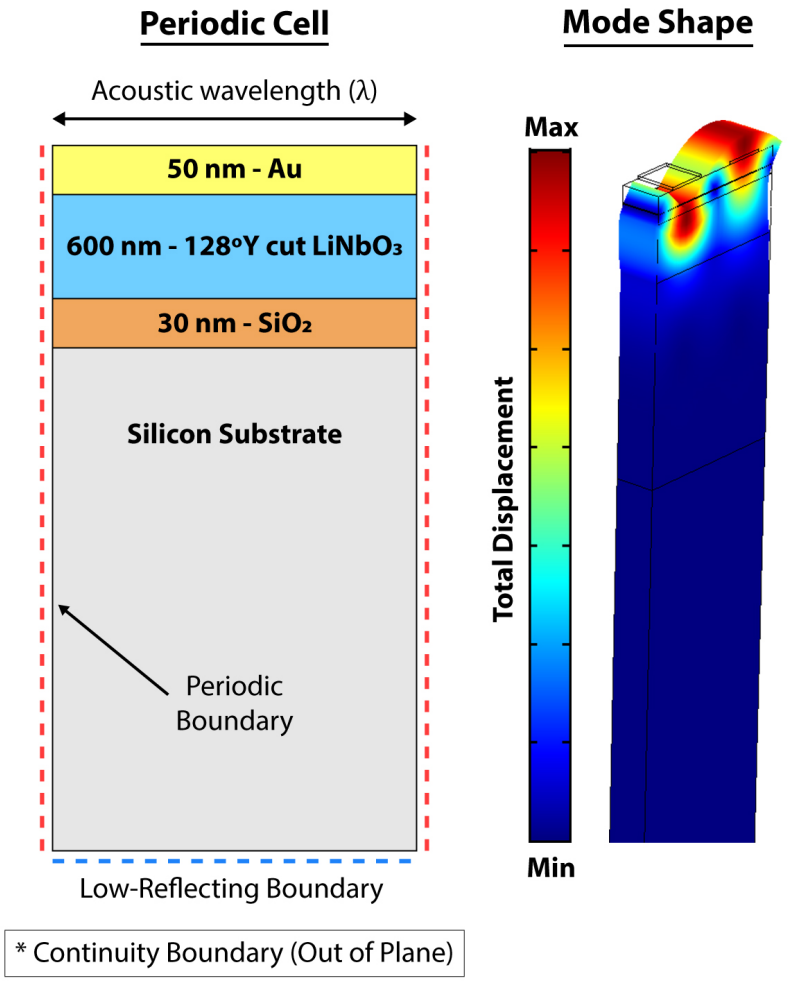

Figure 2.4. Periodic cell used for simulating the k^2 on the 128° Y-cut LNOSi platform with Au metal loading on top and an example mode shape for the Rayleigh SAW mode.

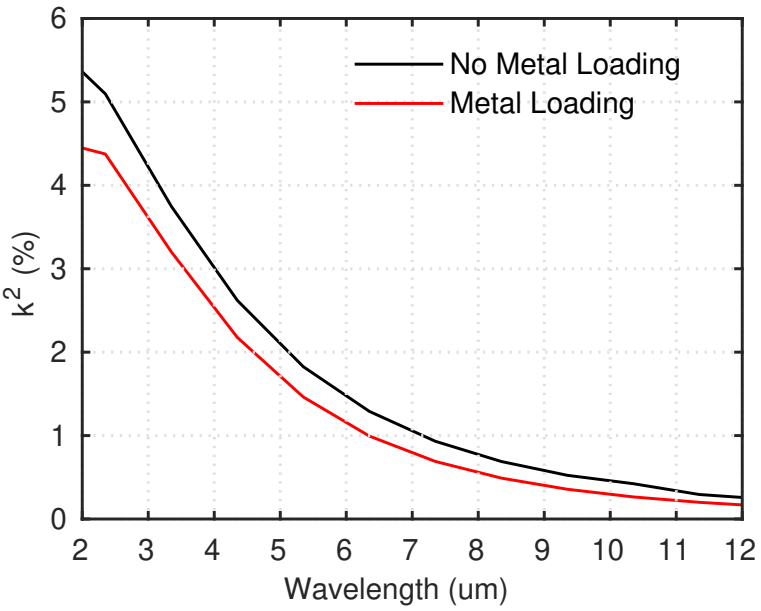

Figure 2.5. COMSOL simulated k^2 for the Rayleigh SAW mode on the 128° Y-cut LNOSi stack with and without Au metal on top.

energy within one acoustic wavelength of the surface. As the acoustic wavelength increases, more of the SAW mode energy sits in the Silicon substrate, which reduces the effectiveness of the LN to actuate the SAW mode. Since the target application for this work is RF (specifically 1 GHz), that corresponds to an acoustic wavelength of 4 μm in LN. Due to limitations in LN thin film bonding through Partow Technologies [27], the thickest LN thin film possible was 600 nm. From the simulations, at a 4 μm wavelength this corresponds to a k^2 of 2.5 – 3%, which is about half the coupling coefficient of a bulk 128° Y-cut LN wafer. This reduction in k^2 would decrease the performance of all the AE device designs. In order to achieve a k^2 comparable to bulk 128° Y-cut LN, the acoustic wavelength would have to be reduced to below 2 μm (above 2 GHz).

As will be discussed in Chapter 4, there is uncertainty about how the LN bonding process will affect the free carrier concentration and mobility, so it is important to have a gate metal to control the carrier levels. Using the thin film LN as an insulating layer, a MIS capacitor can be used in the LNOSi stack to control the carrier level. This gate metal will cause mass loading of the acoustic mode and degrade the electromechanical coupling efficiency, which is acceptable considering how important it is to control the carrier concentration.

2.1.3 LNOSOI Simulations

Since the LNOSi stack's high k^2 is limited to devices operating at GHz frequencies, the COMSOL SAW simulations were expanded in the LNOSOI stack to see if there was any advantage to using an X-cut LN thin film for SAW mode devices. X-cut LN was chosen for its high k^2 acoustic modes both released and unreleased. Bulk X-cut LN has a Rayleigh SAW mode with a k^2 of 4.5% [28]. Released thin film X-cut LN has S_0 Lamb modes with reported k^2 of 30% [14, 29, 30] and SH_0 Lamb modes with reported k^2 of 40% [31]. The S_0 mode's k^2 is highest at -30° relative to the +Y-axis and the SH_0 mode's k^2 is highest at +10° [32]. There has been work looking into these LN plate waves solidly mounted on either a Si or SiO_2 substrate, especially the Shear Horizontal (SH) SAW mode, which propagates in the same direction as the SH_0 plate wave [33]. Therefore, a simulation was performed for

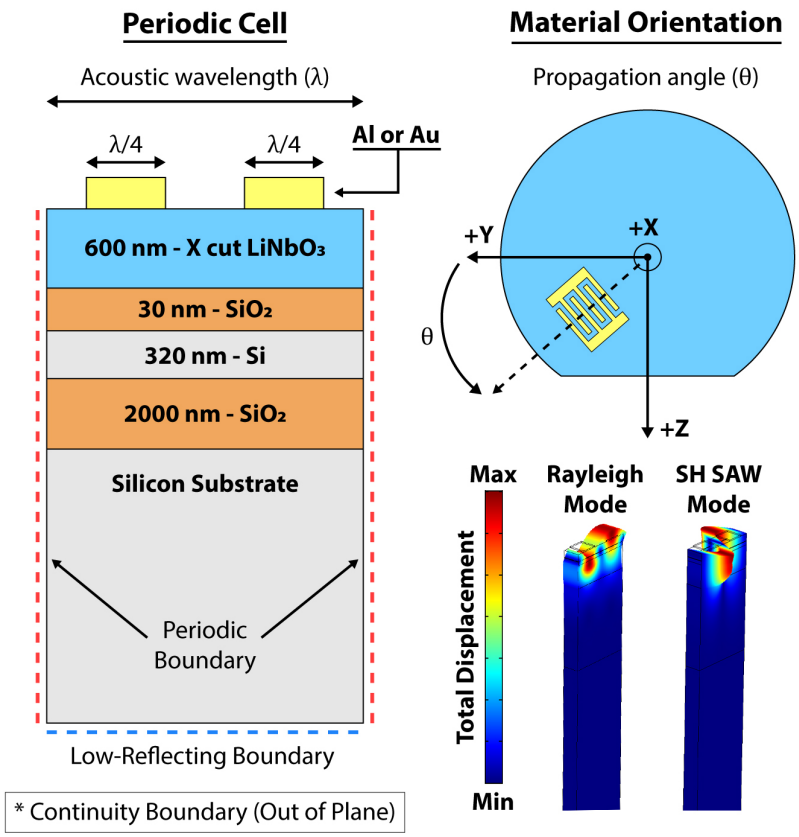

Figure 2.6. Periodic cell used for simulating the k^2 on the LNOSOI platform with the acoustic wavelength and propagation angle defined. Mode shapes are shown for both the Rayleigh and SH SAW modes.

the LNOSOI stack to study both the Rayleigh and SH SAW mode's k^2 as a function of both acoustic wavelength and propagation angle.

Figure 2.6 illustrates the COMSOL geometry and variable definitions. The boundary conditions are set up the same as in the LNOSi simulation and the k^2 is again calculated using Equation (2.6). The two sweep variables are the acoustic wavelength and propagation angle. The acoustic wavelength is defined the same as in the LNOSi simulation and the propagation angle is defined as a material rotation in COMSOL. The propagation angle is referenced to the +Y-axis towards the +Z-axis (as shown in Figure 2.6). This translates to propagation angles for the X-cut Rayleigh SAW, S_0, and SH_0 as +90°, -30°, and +10° respectively.

The results of the Rayleigh SAW mode's simulation are shown in Figure 2.7. To get a clearer picture of the trends in k^2, the results are plotted as a function of normalized

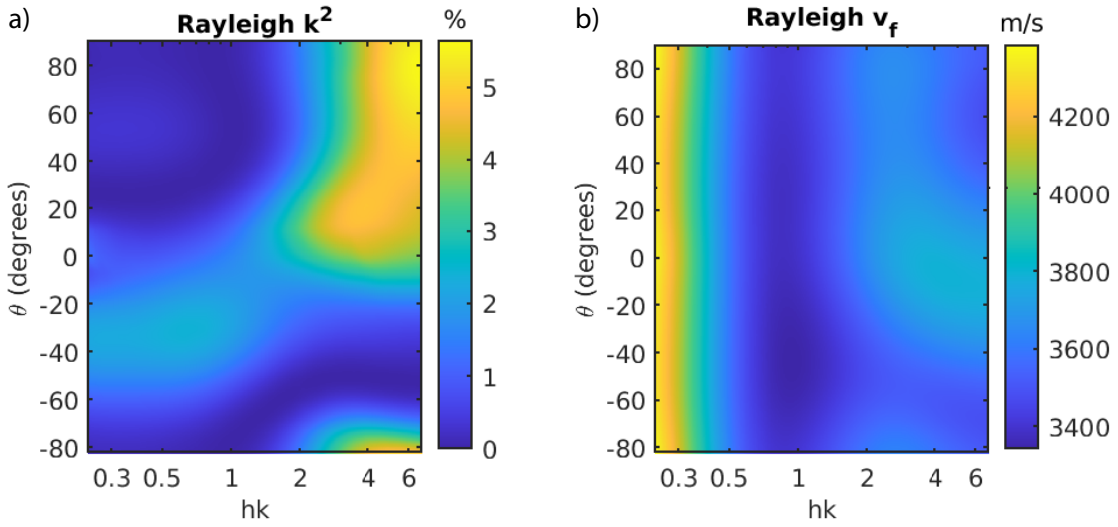

Figure 2.7. Simulated surface plot of the (a) k^2 and (b) acoustic velocity of the Rayleigh SAW Mode as a function of normalized wavelength and propagation angle.

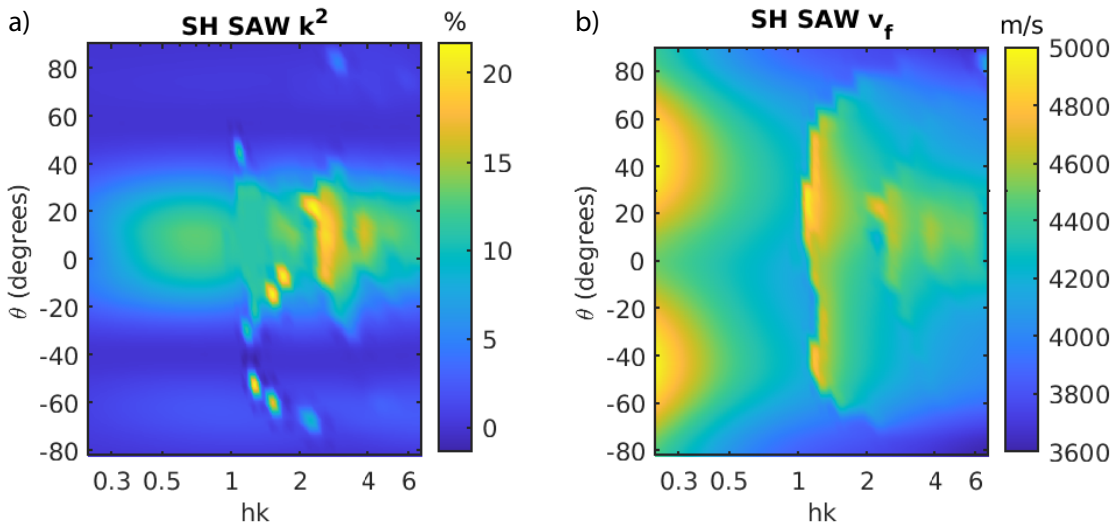

Figure 2.8. Simulated surface plot of the (a) k^2 and (b) acoustic velocity of the SH SAW Mode as a function of normalized wavelength and propagation angle.

wavelength (hK), where h is the LN thin film thickness and K is the acoustic wave number ($2\pi/\lambda$). At large normalized wavelengths hK $>$ 4 ($\lambda < 1$ μm), the majority of the SAW mode's energy is in the X-cut LN thin film and behaves similar to a bulk X-cut LN wafer. The optimal k^2 in this case is around 5% in the +90° propagation direction as expected. Between the normalized wavelengths of 4 and 1 (1 μm and 5 μm), the optimal propagation angle shifts from +90° to -30°, which is the angle for the plate wave S_0 mode. At normalized wavelengths hK $<$ 1 ($\lambda > 5$ μm), the optimal propagation angle is -30° with a k^2 of 2.5% that slowly decreases as wavelength increases. This material stack can be useful in designing unreleased AE devices utilizing the Rayleigh SAW mode in the MHz frequency range.

Figure 2.8 shows the result of the SH SAW simulation. The propagation angle with the highest k^2 for the SH SAW mode is always at +10°, independent of the normalized wavelength. Between the normalized wavelengths of 1 and 4, there are several sporadic jumps in the k^2. This is due to the presence of guided acoustic modes in the SiO_2 layer. Unlike other SH SAW material platforms, mounting a thin film of LN on a SOI wafer with a thick buried oxide (BOX) layer creates an acoustic waveguide in the BOX between the Si device layer and Si substrate. The higher order modes of this guided BOX mode have

frequency crossings with the SH SAW mode in the dispersion curve for this specific material stack. This could be resolved by using a thinner BOX layer to push the guided modes to higher frequencies above the desired operating range. This distortion in the SH SAW mode crossing with guided BOX modes can also be seen in the simulated acoustic velocity in Figure 2.8 (b). There are clear distortions in the acoustic velocity occurring at normalized wavelengths of 1.5, 3, and 4. The possibility of a high k^2 SH SAW mode spanning over a large range of wavelengths is attractive for unreleased AE devices on the LNOSOI platform. SAW delaylines will be fabricated for both the Rayleigh and SH SAW to compare not only the k^2 performance, but also the propagation losses associated with these modes and if there is any trade off between high coupling coefficient and high propagation losses in this LNOSOI platform.

2.1.4 Fabrication Variability Simulations

All of the simulations performed up to this point on the LNOSOI material platform did not take into account the loading effects of metal fingers used in the IDTs for the transduction of the SAW modes. For the three angles of interest (+90°, +10°, and -30°), k^2 simulations were performed with the addition of metal IDT fingers in the periodic cell (positioning shown in Figure 2.6). During the fabrication process, some variation in the film thicknesses or propagation angle can be introduced. For each variation, the COMSOL simulations were performed again for the three angles fabricated over the fabricated wavelength range. The largest variation at each wavelength is recorded and plotted against the ideal metal loaded SAW simulation.

Figure 2.9 shows an example fabrication variability k^2 simulation for the Rayleigh SAW mode with Al IDT fingers. The solid lines for each propagation angle represent the ideal designed material stack with no variation in the material thicknesses. The shaded color regions show the maximum deviation in k^2 at each wavelength given variability in deposited Al thicknesses and propagation angle misalignment. Given an Al metal thickness of 100 nm, simulations were performed with a 25 nm variability in thickness. Also, a misalignment of 5° was simulated for each propagation angle. From Figure 2.9, the Rayleigh SAW mode

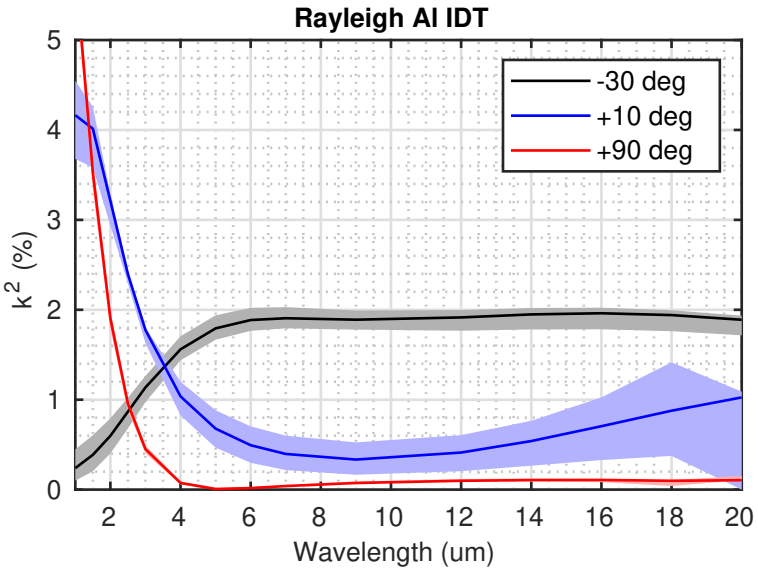

Figure 2.9. Rayleigh Mode COMSOL k^2 simulations with Al IDT fingers. The solid line is the ideal metal loaded curve and the shaded color regions for each of the three propagation angles is the maximum k^2 deviation based on fabrication variability.

at +90° is not sensitive to fabrication variations and has the same k^2 value as the ideal metalized case. The k^2 variation along the -30° angle is due to the Al thickness variation. The Rayleigh mode at this angle seems to be most sensitive to the metal loading effects. Finally, the variation found in the +10° angle is due in large part to the propagation angle misalignment.

2.2 ADS Simulation and Measurement Fitting

This section covers the modified cross-field Mason model implemented in ADS software, which includes adding a substrate conductivity term. Then, the design of IDTs are covered including the importance of a symmetric grounding scheme and shielding. The full design of experiment is outlined for single finger delaylines at different propagation angles and wavelengths with normalized geometric dimensions for easier comparisons. After detailing the design, the fabrication process for these delaylines is covered along with the experimental setup for measuring the 2-Port S-parameters. These measured data sets are imported

into ADS and fit to extract several key acoustic and piezoelectric device parameters. The extracted parameters are compared to COMSOL simulations and the results are discussed.

2.2.1 Modified Cross-Field Mason Model

The key to designing SAW devices is the accurate modeling and extraction of acoustic and piezoelectric properties. For traditional SAW delayline devices, there are several well known modeling methods including coupled mode theory [34, 35], impulse response [36, 37], and Mason circuit model [38]. These methods are great at predicting the behavior of SAW delaylines for simple material stacks on insulating substrates. With the desire to integrate SAW devices with Integrated Circuit (IC) platforms and other technologies built on Silicon platforms, the substrate conductivity's effect on the SAW performance can't be overlooked [39–42]. Since the LNOSOI platform also has issues with substrate conductivity, the lumped element Mason equivalent circuit model was chosen to model the SAW delaylines on this platform. This is due to its flexibility to be adjusted and generalized to include second order effects [43–45]. Another benefit is the ability to implement the model in a circuit simulation software [46, 47] to build and simulate extremely complex structures and interaction mechanisms. For SAW devices, the Mason model uses an idealized field distribution across the piezoelectric material that is either perpendicular to the propagation direction (cross-field), parallel to the propagation direction (in-line), or a weighted mix of both [48]. Experimentally, in almost all cases the cross-field model is a more accurate representation of the device performance and characteristics [49], so this model was chosen as a starting point for the modeling of LNOSOI SAW delaylines.

The cross-field Mason model was initially developed for insulating substrates, so substrate conductivity still needed to be incorporated in to the lumped element model. The work done including substrate conductivity in the equivalent circuit cross-field Mason model [50–52] was used as a starting point to include this term in the lumped element cross-field Mason model. Based on the model presented here [53], substrate conductance was added and Figure 2.10 shows the illustration of this modified model for a single metalized finger. The top of the figure shows the geometric layout of a single metalized finger. Within each unit

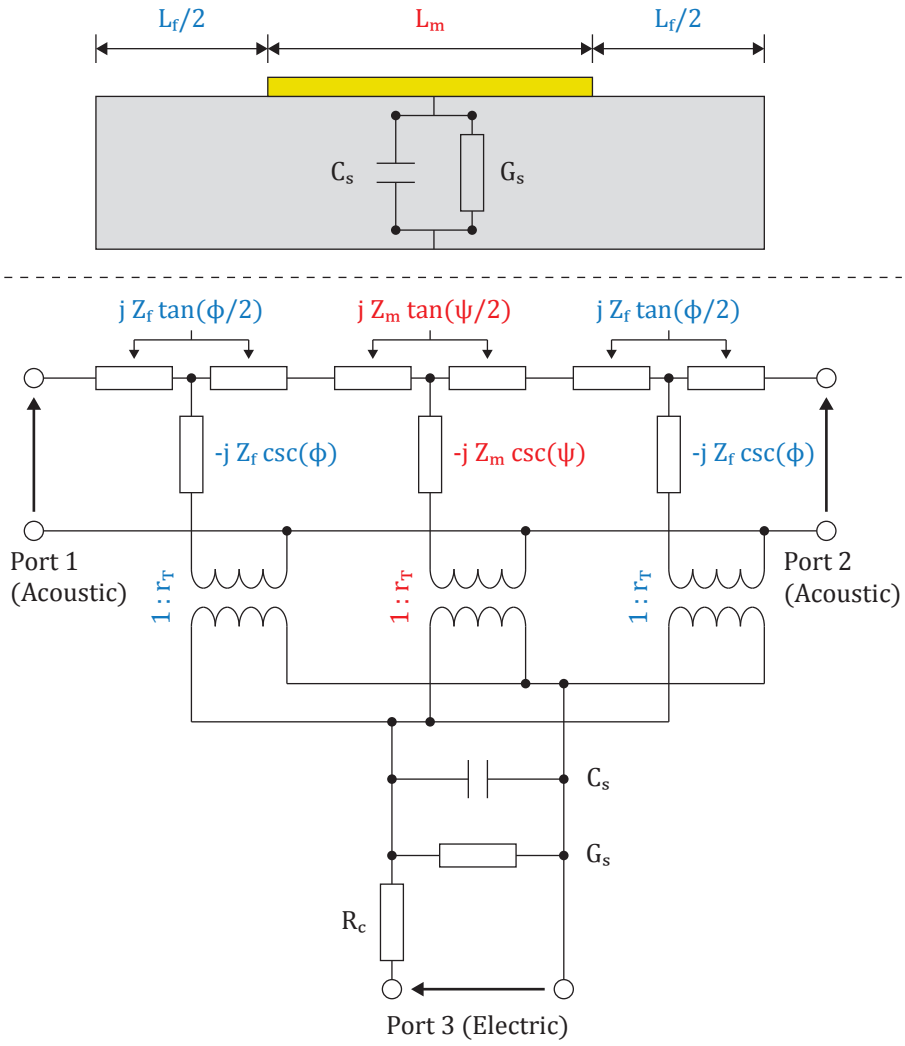

Figure 2.10. Illustration of the cross-field Mason model with added substrate conductance.

cell, there is a length of device that is metalized (L_m) and a length that is free of metal (L_f). Electrically, each section of substrate between the metal and ground is some capacitance (C_s) and conductance (G_s). The bottom of Figure 2.10 shows the geometry represented as the lumped element cross-field Mason model. The model consists of two acoustic ports and one electrical port. Each free and metalized propagation region is represented by a transmission line in the acoustic domain with a free (Z_f) and metalized (Z_m) acoustic impedance. The propagation of an acoustic wave through each region also picks up some phase in the free (ϕ) and metalized (ψ) regions. The acoustic impedance can be transformed into an effective electrical impedance seen at the electrical port through a transformer with a turn ratio r_T. In the electrical domain, the conductive losses associated with the metal finger can be represented as R_c. These lumped elements are related to the SAW mode characteristics and IDT geometry by (see [53])

$$f_0 = \left[m\frac{\lambda}{v_\mathrm{m}} + (1-m)\frac{\lambda}{v_\mathrm{f}} \right]^{-1}, \tag{2.7}$$

$$\phi = (1-m)\,\frac{f_0 \lambda \pi}{2\,v_\mathrm{f}}, \qquad \psi = m\,\frac{f_0 \lambda \pi}{v_\mathrm{m}}, \qquad \frac{Z_\mathrm{f}}{Z_\mathrm{m}} = \frac{v_\mathrm{f}}{v_\mathrm{m}}, \tag{2.8}$$

where m is the finger metalization ratio, λ is the acoustic wavelength, v_f is the free acoustic velocity, v_m is the metalized acoustic velocity, and f_0 is the synchronous frequency. The transformer ratio for metal finger i is then defined as

$$r_\mathrm{T} = (-1)^i \sqrt{2 f_0 C_\mathrm{s} k^2 Z_\mathrm{f}} \left[\frac{K\left(2^{-1/2}\right)}{K\left(q\right)} \right], \qquad q = \sin\left(m\frac{\pi}{2} \right). \tag{2.9}$$

Figure 2.11 shows how this single finger lumped element model can be connected together to model a full 2-Port delayline. Within each IDT, the single finger lumped element models are connected acoustically in series and electrically in parallel. Also, the transformer ratio alternates in polarity to model the signal and ground connections on alternating fingers. Each IDT block is then connected acoustically in series with a lossy transmission line (to

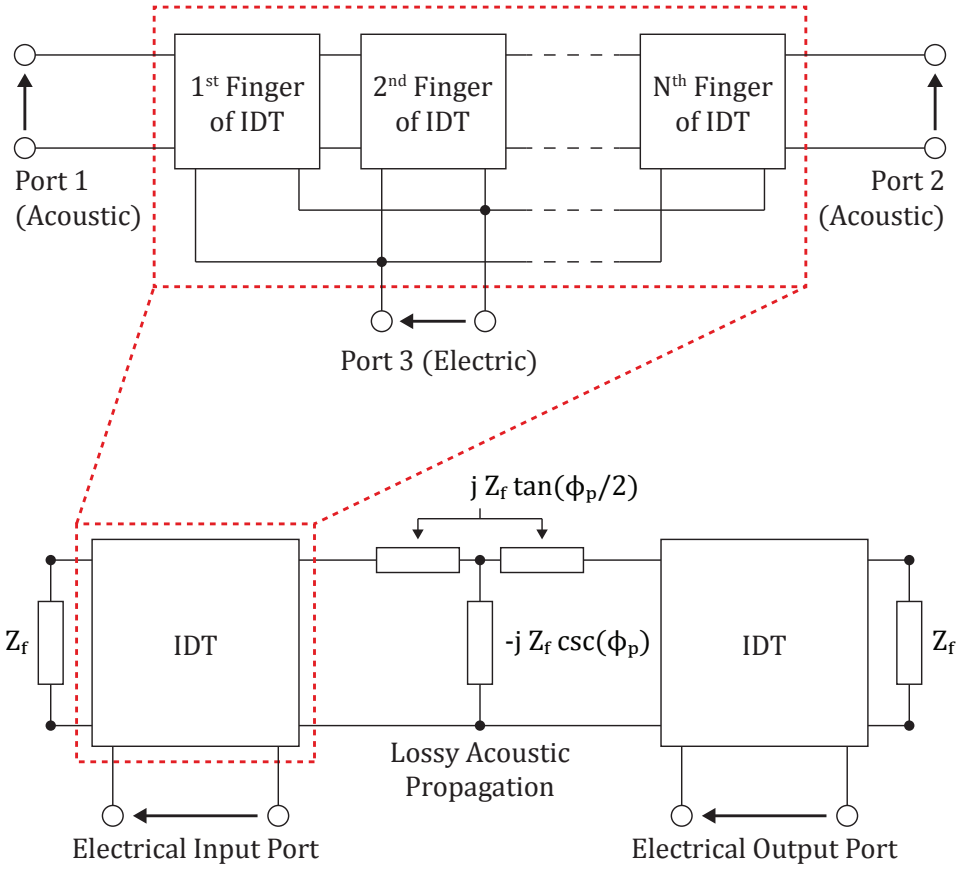

Figure 2.11. Full Block Diagram of the single finger delayline. (top) Each finger model is connected acoustically in series and electrically in parallel to form an IDT. (bottom) Higher level block diagram showing the two IDTs with a lossy acoustic transmission line connected in series.

capture the propagation losses). Later in this chapter, the full model will be implemented in ADS and used to simulate the performance of SAW delaylines on the LNOSOI platform.

2.2.2 SAW Delayline Design

When designing the IDT for the SAW delayline, several weighting schemes of the finger periodicity and metal width were considered, like double electrode [54], slanted finger [55, 56], electrode width control (EWC) [57, 58], and distributed acoustic reflection transducer (DART) [59, 60] designs. These designs require knowledge of the velocity shift and reflection coefficient for each finger width and metalization thickness [61], which vary based

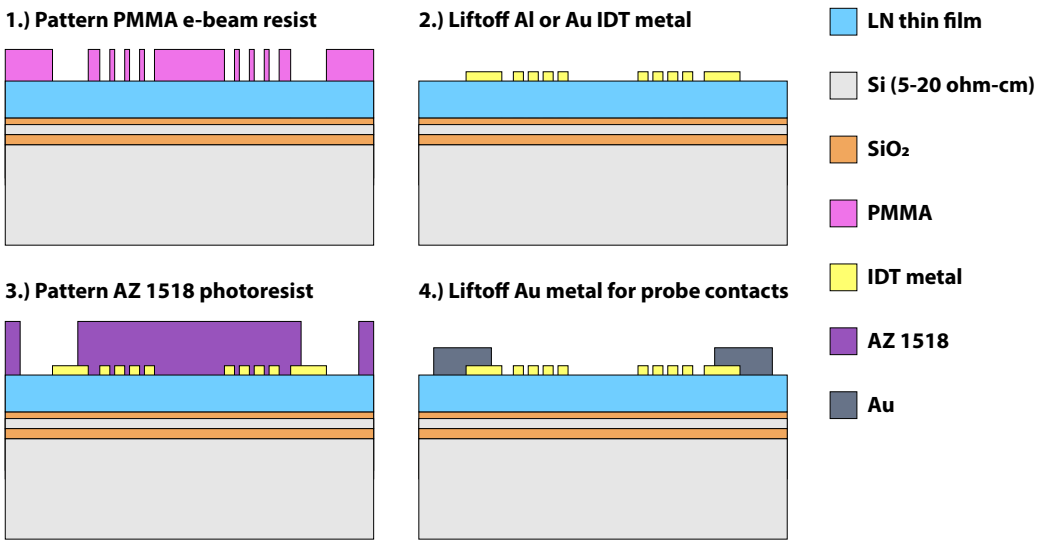

Figure 2.12. Illustration of the SAW fabrication process on the LNOSOI stack.

on the material platform and SAW mode used. Therefore, a simple single finger IDT design was chosen for this experiment to focus on the development of the ADS model and fitting procedure. Another IDT design consideration is the routing of the ground bus bar. There have been several examples of incorporating grounded shielding lines in between the IDTs [62, 63]. These shielding lines can act as a shorter path to ground to reduce feed through capacitance between transmit and receive IDTs. When designing SAW devices at high RF frequencies in the GHz range, the capacitive effects of the ground lines for Ground Signal Ground (GSG) RF probes must also be taken into consideration. Using a symmetric and angled ground bus bar [64] has two advantages. First, the symmetric ground termination on the GSG probes ensures there are no unbalanced capacitive effects, especially at higher frequencies (GHz). Additionally, the angled shielding lines help divert acoustic reflections from the propagating acoustic wave away from the IDTs. The full set of fabricated SAW delaylines on LNOSOI will look at a range of IDT wavelengths (1 μm to 16 μm), propagation angles (-30°, +10°, and +90°), and finger metals (Al & Au). Then, both the Rayleigh and SH SAW modes will be measured in the S-parameter frequency response. To try and keep diffraction and second order propagation effects the same for all devices, the IDT geometric dimensions were designed as a function of wavelength instead of absolute dimension.

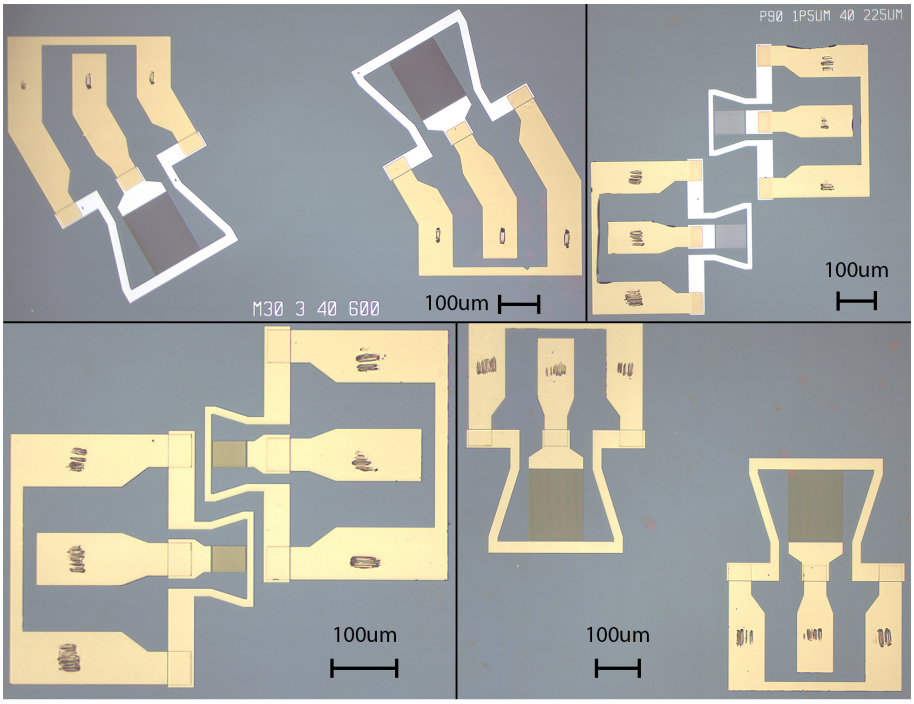

Figure 2.13. Optical images of four example SAW delaylines fabricated on the LNOSOI platform. These images show examples of the different IDT finger metals, propagation angles, and acoustic wavelengths with scaled IDT dimensions.

2.2.3 SAW Delayline Fabrication and Measurement

Figure 2.12 shows the fabrication process for SAW delaylines on LNOSOI. First, the sample is coated in PMMA e-beam resist and patterned using e-beam lithography. Step 2 is to lift off either 90 nm of Al or 50 nm of Au metal to define the IDT fingers and bus bars. The third step is to coat the sample in AZ 1518 photoresist and pattern using photolithography. Finally, a 250 nm thick Au layer is deposited using lift off to define the GSG pad lines.

Optical images showing examples of four fabricated delaylines are shown in Figure 2.13. These images show examples of the different propagation angles, wavelengths, and finger metals used in this experiment. Showing the images side by side highlights the normalization of the IDT geometric dimensions. The IDT aperture and delay lengths were scaled as a function of wavelength to keep the resistance per finger equal for every device. Also, this was done so that the diffraction effects and relative delay lengths were similar as well.

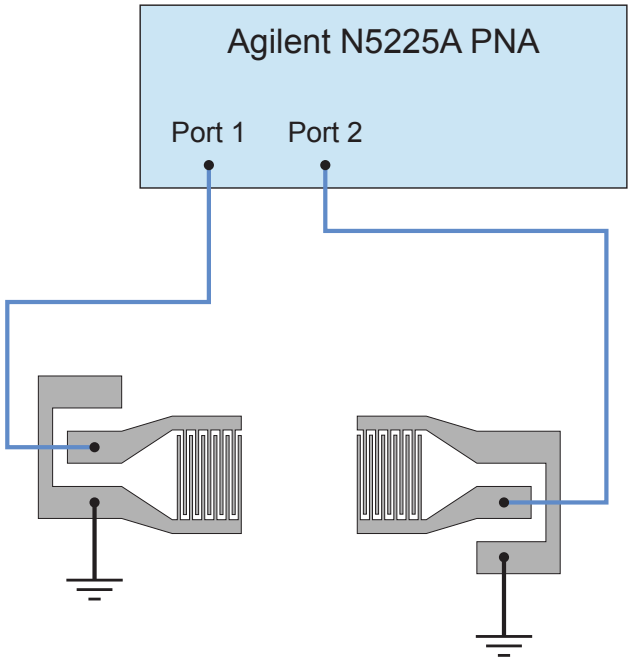

Figure 2.14. Illustration of the experimental setup for measuring the SAW delayline 2-Port S-parameters.

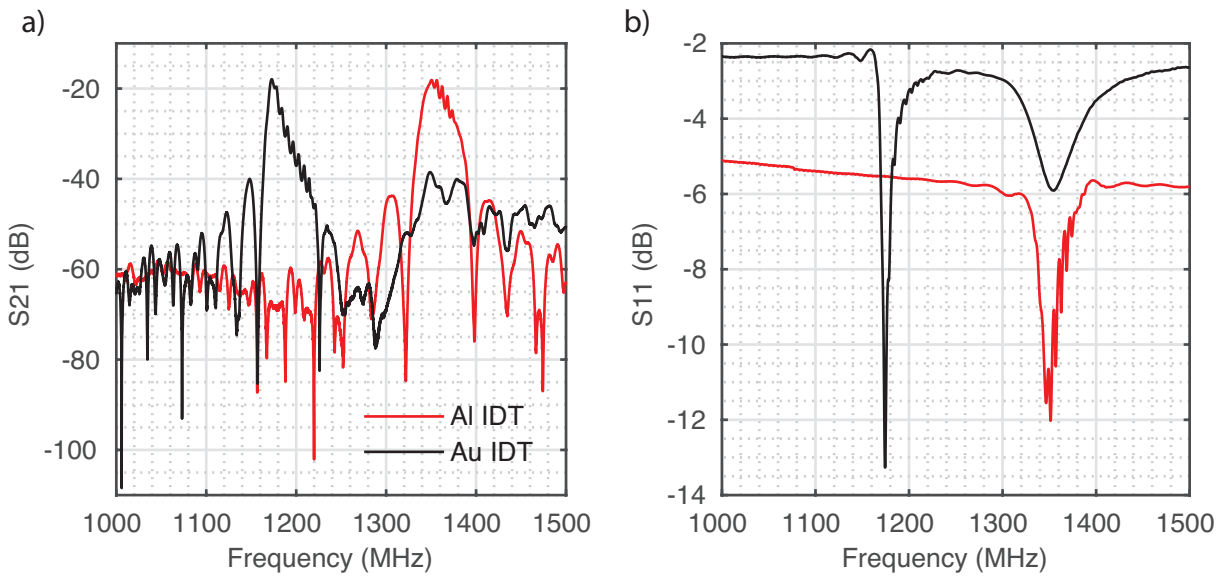

Figure 2.15. Measured S-parameters on a -30° delayline with $\lambda = 2.5$ μm for the Rayleigh SAW mode.

Figure 2.14 shows the experimental setup for measuring the S-parameters of each SAW delayline. Using two GSG probes connected to each port of the PNA network analyzer, an RF signal generated at Port 1 is applied to the transmit IDT on the left. The IDT generates an acoustic wave that travels to the receive IDT connected to Port 2 of the PNA. The full set of 2-Port S-parameters measured contain the transmitted signal levels between ports (S_{21} & S_{12}) and the reflected signal level off of each port (S_{11} & S_{22}).

Figure 2.15 shows a set of S-parameter measurements with both Al and Au metal IDT fingers. One noticeable difference between Al and Au electrodes is the frequency shift as a result of the metal mass loading. Since Al has a similar acoustic impedance to LN [65], there is only a small frequency shift observed in the Al IDTs compared to the large shift with Au IDTs. In general, the most prominent second order effect observed is the reflection of the acoustic wave at the electrode edges from acoustic mismatch [66, 67]. These ripples at the S_{21} resonance peak can be seen in both structures, but larger in magnitude with Au electrodes. Also, the metal loading effects cause a distortion in the S_{21} frequency response because the metalized regions have a lower acoustic velocity when compared to the free surface [68]. Since Au has a larger mass loading effect, the asymmetry observed in the frequency response

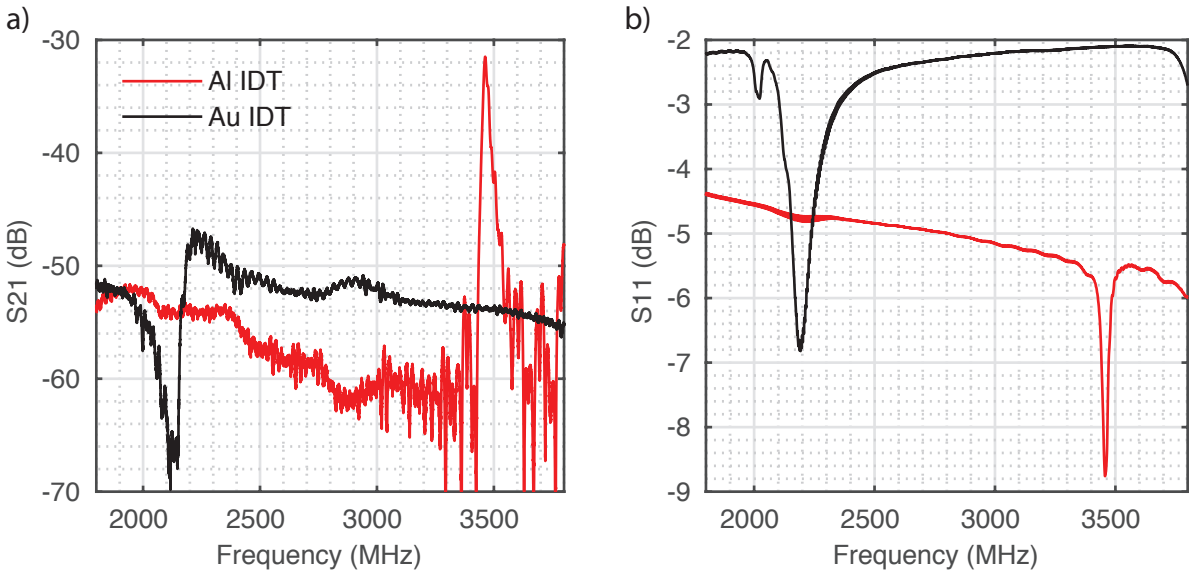

Figure 2.16. Measured S-parameters on a -30° delayline with $\lambda = 1$ μm for the Rayleigh SAW mode.

is larger when compared to Al. Au, however, is more conductive than Al, which means a thicker layer of Al is needed to achieve the same conductive losses in the electrodes. For these Al devices, the thickness wasn't enough to have the same conductive losses, which can be seen by the lower S_{11} response.

As the wavelength decreases, so does the SAW mode's penetration depth into the substrate. This effectively increases the metal thickness at these small wavelengths. At this point, the mass loading effects and acoustic impedance mismatch alter the dispersion of the mode under the metalized surface enough where it can no longer be transduced by the IDT [69]. Figure 2.16 shows the measurement of a 1 μm wavelength delayline with both Au and Al electrodes. At this wavelength, the Al IDTs can still transduce the Rayleigh SAW mode at 3.5 GHz, but the Au IDTs show no response above the measurement noise floor.

2.2.4 Fitting Methodology

When trying to extract acoustic and piezoelectric SAW device characteristics, like the piezoelectric coupling coefficient (k^2) and quality factor (Q), the most common practice is to fabricate a SAW resonator and fit the experimental frequency response to a modified Butterworth-Van Dyke (MBVD) model [33, 70]. In this work, the lumped element cross-field Mason model will be fit to a travelling wave SAW delayline using the optimization component in ADS. Figure 2.17 shows the full setup in ADS for fitting the cross-field Mason model to experimental delayline measurements. First, the experimental S-parameter data set is imported into ADS through the DAC component. Then, initial guesses and optimization ranges for each acoustic and piezoelectric parameter is input. These parameters are: wavelength, IDT separation distance, IDT aperture, metalization ratio, free acoustic velocity, metalized acoustic velocity, attenuation coefficient, finger capacitance, substrate conductance, electrode resistance, and piezoelectric transformer ratio. The next step is to set up the optimization goals, which are minimization goals set as the difference between the simulated and experimental frequency response. For this model, the goals were defined as minimizing the difference in the S_{11} magnitude, S_{11} phase, and S_{21} magnitude.

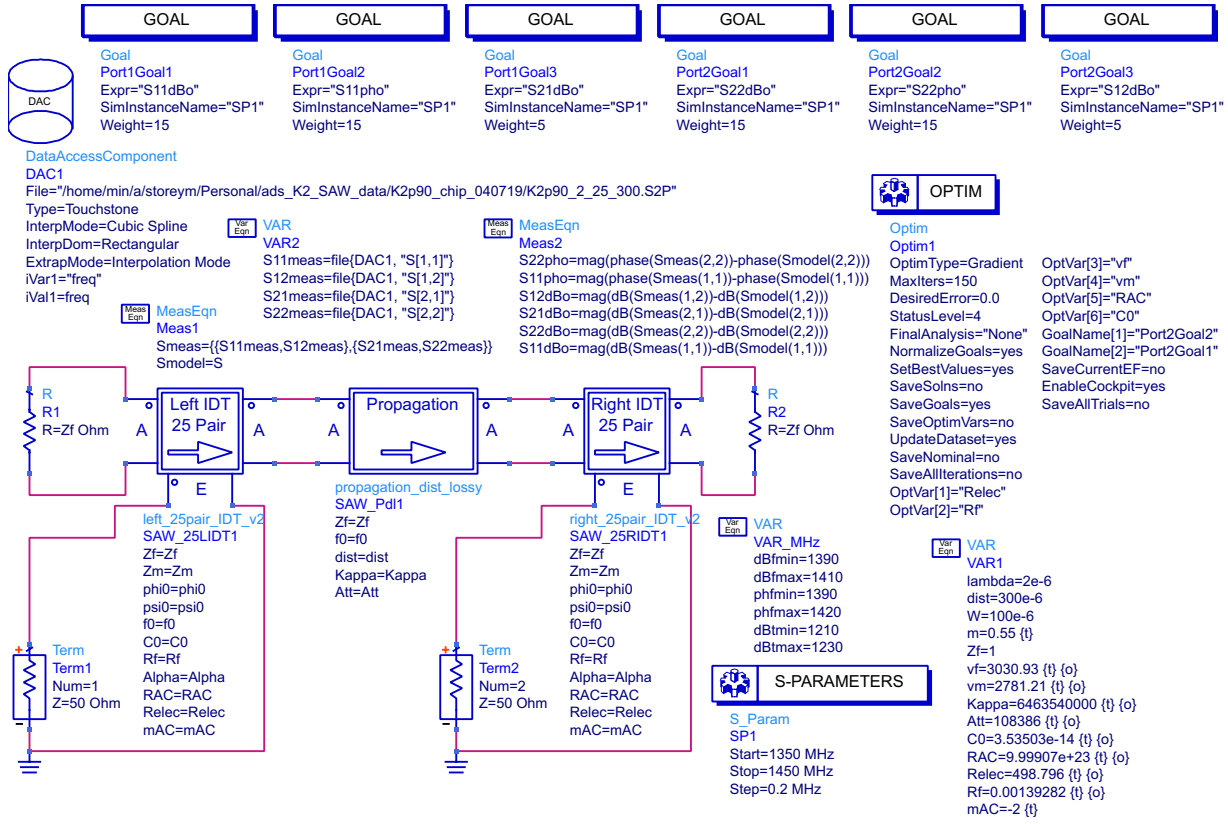

Figure 2.17. ADS setup of the lumped element cross-field Mason model, S-parameter data import component, S-parameter simulation component, and optimization component.

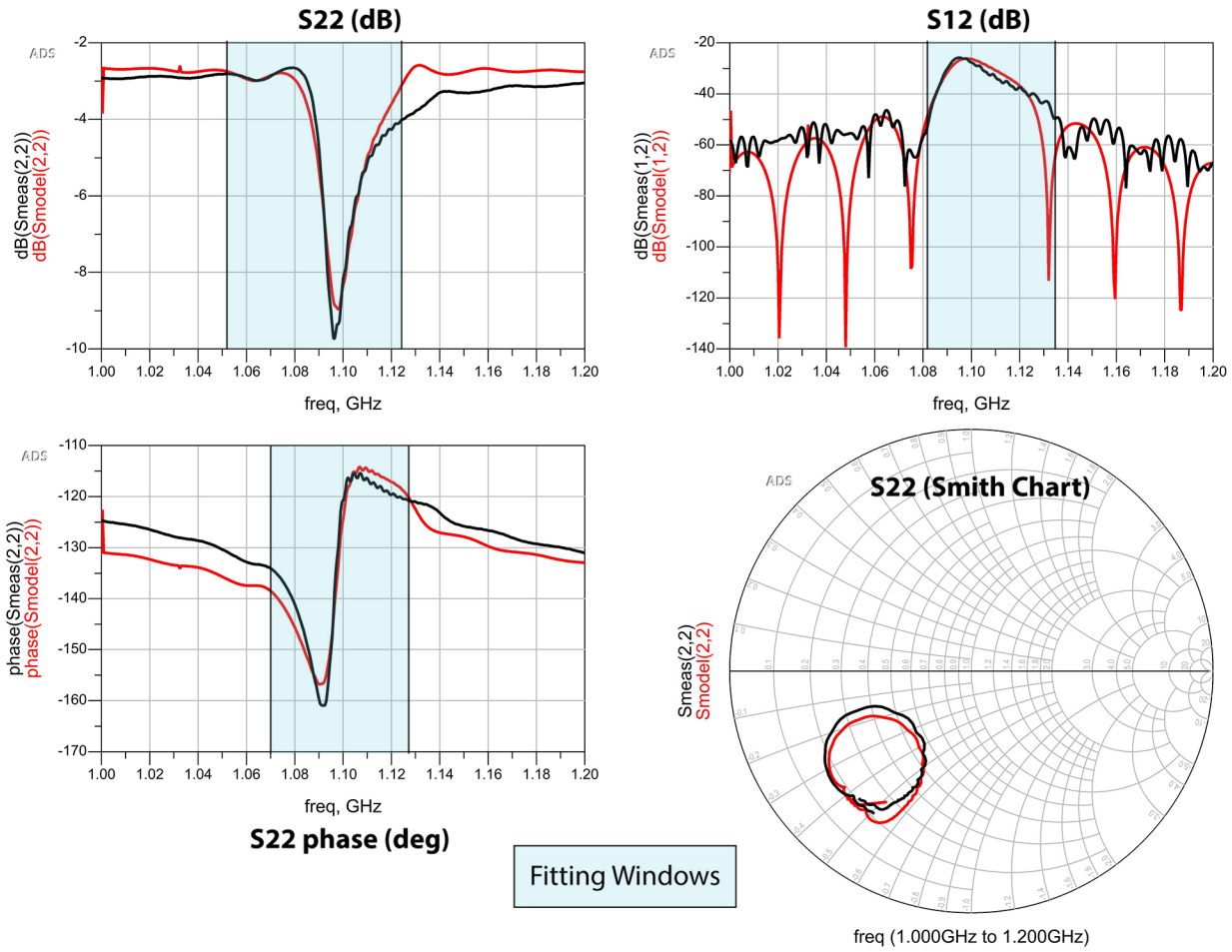

Figure 2.18. ADS readout screen comparing measured S-parameters with the fitted lumped element circuit model. The frequency ranges used for fitting are highlighted in blue.

Figure 2.18 shows an example ADS output screen after optimization. The ADS model is setup to optimize for both Port 1 excitations (S_{11} & S_{21}) and Port 2 excitations (S_{22} & S_{12}). For each of the three S-parameter plots, the set fitting frequency window is highlighted in blue. This frequency window should include the key characteristics of the resonance and may need to be slightly adjusted in order to find the local minimum. The full frequency response for all three goals in addition to a Smith chart representation of the reflection are then plotted.

2.2.5 Fitting Comparison and Results

Once the experimental data is fit to a curve generated by the Mason model, the acoustic and piezoelectric properties of the SAW delayline can be extracted directly from the lumped element circuit parameters or by solving Equations (2.7-2.9). For example, the k^2 can be extracted directly from Equation (2.9) since r_{T}, f_0, C_{s}, and Z_{f} are parameters solved for in the lumped element circuit.

Figure 2.19 shows examples of four measured SAW delaylines and their lumped element circuit models fit using ADS. As discussed previously, the Rayleigh mode with Au IDTs has more interference in the S_{21} peak and more asymmetry in the frequency response when compared to measured Rayleigh modes with Al IDTs. The lumped element circuit model is able to capture these interference patterns from internal reflections in the IDT as well as the asymmetry in the frequency response. The lumped element circuit model is able to capture these first and second order effects because each parameter in the model affects certain aspects of the frequency response. The geometrically defined IDT parameters, λ and m, set the location of the synchronous frequency. The propagation distance between IDTs (d_{prop}) and propagation attenuation (α_{prop}) set the S_{21} insertion loss. The relative difference in the free and metalized acoustic velocities (v_{f} & v_{m}) determine the amount of asymmetry in the frequency response. In the electrical domain, the admittance parameters (R_{c}, C_{s}, and G_{s}) determine the off resonance signal levels and phase in the S_{11} response. Finally, the transformer ratio r_{T} scales the overall magnitude of the response in both the S_{11} and S_{21} S-parameters.

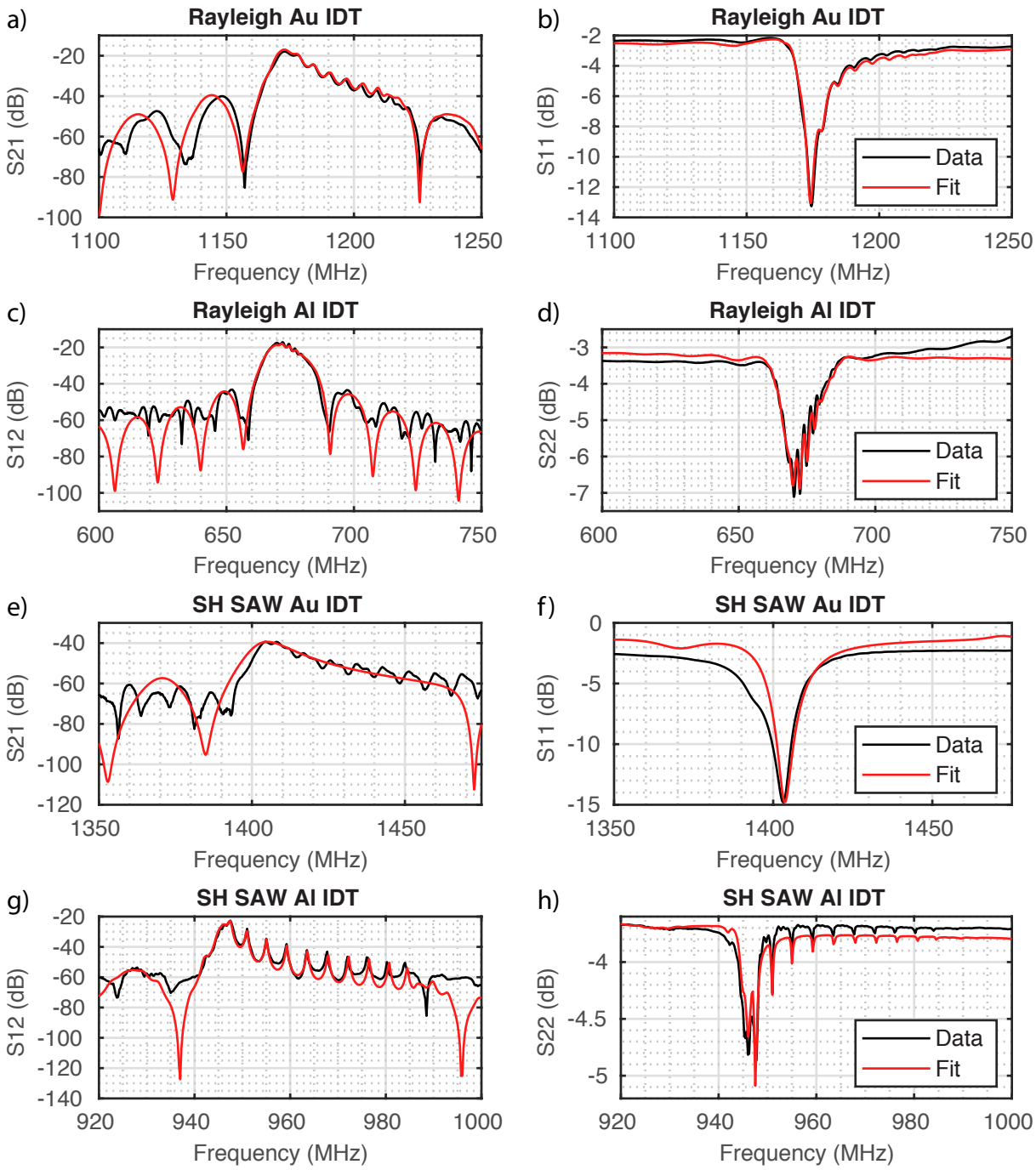

Figure 2.19. Comparison of ADS fit lumped element circuit models to measured SAW delayline S-parameters.

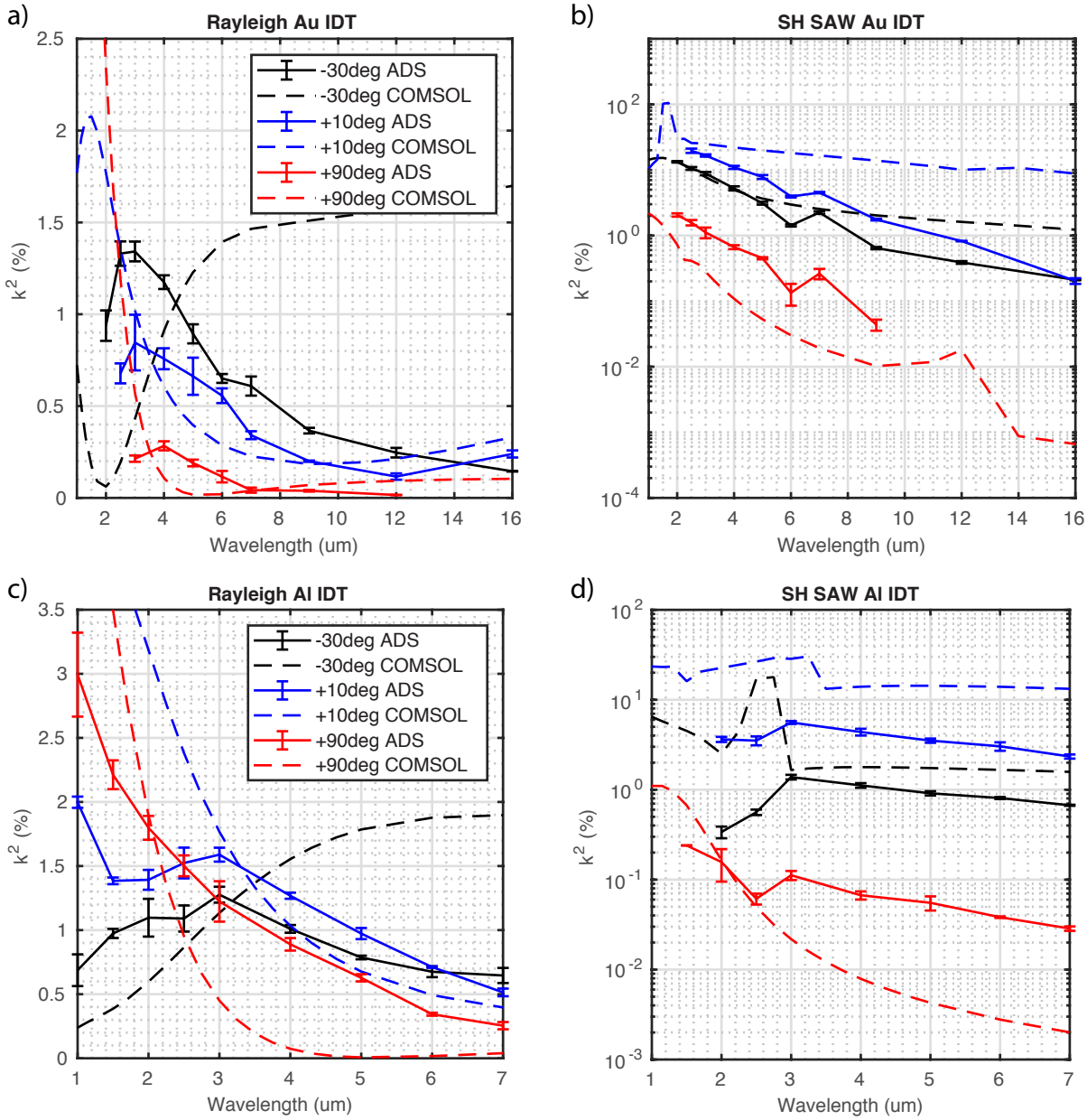

Figure 2.20. k^2 vs. wavelength plots for both the Rayleigh and SH SAW modes with Au and Al IDTs. The ADS extracted k^2 values (solid lines) are compared to the metal loaded COMSOL k^2 simulations (dashed lines).

Figure 2.20 shows a comparison of ADS extracted k^2 with the metal loaded COMSOL k^2 simulations. For the Rayleigh SAW with Au IDTs, there is reasonable agreement between the fit and simulation for the +10° and +90° propagation angles, but the -30° angle shows a significant drop off in k^2 when compared to simulation. Similarly for the SH SAW mode with Au IDTs, there is good agreement with simulation for the -30° and +90° propagation angles, but a significant drop off in the predominant angle of +10°. There are several possible explanations for these large discrepancies. There has been other work describing variations of 20% in the reported k^2 compared to theory [71]. Also, a similar study was performed with Al and Au mass loaded LN delaylines, which showed good agreement on predicting the resonant frequency, but only qualitatively predicted the trends in the admittance [72]. A similar result is seen here, especially for the SH SAW modes with Al IDTs. Qualitatively, the fitting captured the trends in the large k^2 angles (-30° & +10°). The coupling coefficient increased as wavelength decreased until a point where it starts to decrease. A second possible explanation is related to the conductivity of the substrate. It has been shown that SAW transduction on a conductive substrate reduces the k^2 based on the conductivity [50]. As the wavelength increases, more of the mode sits in the conductive substrate and has a larger interaction region with the carriers, which could further reduce the k^2. Control of the substrate conductivity under the IDTs could be achieved by applying a DC voltage between the fingers and bottom of the substrate [73]. This could reduce the conductivity under the IDTs enough to determine if substrate conductivity is the explanation for this discrepancy in k^2.

When considering an acoustic mode and material platform to use, it is important to consider other factors in addition to the k^2. Another important factor in SAW device performance is the propagation loss. Depending on the device application, it might be more advantageous to use a SAW mode with a lower propagation loss at the expense of a smaller k^2 [74]. This propagation loss can also be expressed as a quality factor [75]

$$Q = \frac{\pi f_0}{v_\mathrm{f}\, \alpha_\mathrm{prop}}, \tag{2.10}$$

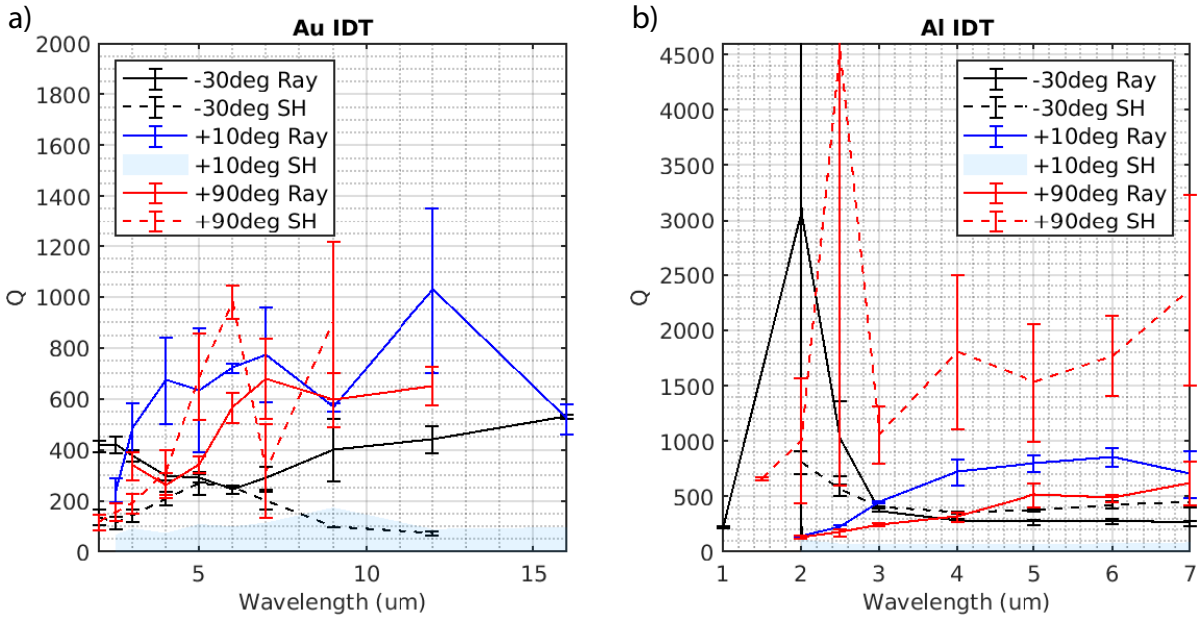

Figure 2.21. Extracted Q vs. wavelength for both the Rayleigh and SH SAW modes with Au and Al IDTs. The +10° SH SAW modes were below the measurement noise floor, so the shaded regions represents the area where the unmeasured Q could exist.

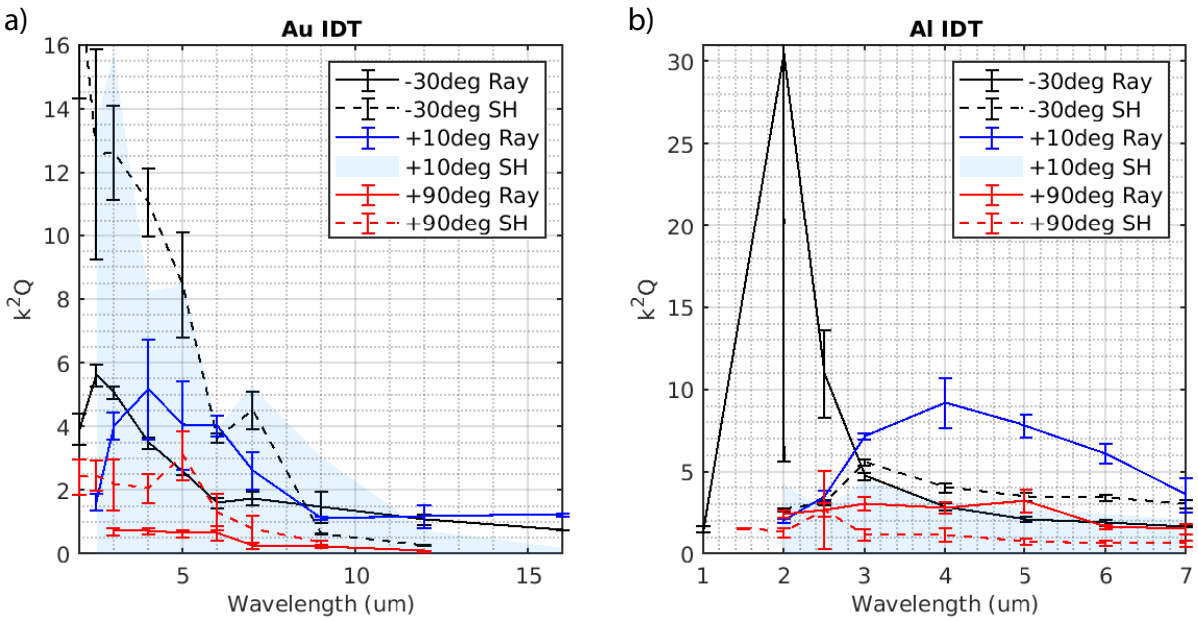

Figure 2.22. Extracted k^2Q vs. wavelength for both the Rayleigh and SH SAW modes with Au and Al IDTs. The +10° SH SAW modes were below the measurement noise floor, so the shaded regions represents the area where the unmeasured k^2Q could exist.

where f_0, v_f, and α_{prop} are all parameters extracted from the ADS fitting. Figure 2.21 shows the Q fit from ADS vs. wavelength for both Rayleigh and SH SAW modes with Au and Al IDTs. For the Au electrodes, the +10° Rayleigh mode had the largest Q across almost all of the wavelengths. With Al electrodes, however, the highest Q mode was the +90° SH SAW mode. In both metalizations, the -30° Rayleigh mode had one of the lowest Q values across all of the wavelengths. The highest k^2 mode (+10° SH SAW) had the lowest Q out of any mode because it was not measurable above the measurement noise floor. While this SH SAW mode is appealing for its high k^2 value, its high propagation losses could make it undesirable for certain applications.

Finally, the k^2Q figure of merit is calculated and shown in Figure 2.22. For Au IDTs, the -30° SH SAW mode has a very high k^2Q at lower wavelengths. This suggests that the Au metal loading helps concentrate the SH SAW mode near the surface, increasing its k^2 while not introducing significant propagation losses. Al metal loading, however, does not concentrate the SH SAW modes near the surface as much as Au, so the SH SAW modes have

a smaller k^2Q with Al IDTs. It is the $+10°$ Rayleigh mode that has the highest k^2Q with Al electrodes. Therefore, when considering the trade off between k^2 and Q, it is important to not only look at the SAW mode and material platform, but also the choice of IDT metal.

3. ACOUSTOELECTRIC THEORY AND MODELING

There are several key parameters to consider when designing a high performance AE material platform. These include: the piezoelectric coupling coefficient (k^2), acoustic mode shape, acoustic velocity, free carrier concentration, mobility, and metal loading effects on the transduction and IL of the device. All of these need to be designed for and accurately characterized in order to get an accurate picture of the AE performance. Chapter 2 covered the measurement and fitting procedure for determining the acoustic mode's characteristics. This chapter will discuss the semiconductor material parameters and how each of those play an important part in maximizing the AE performance. The semiconductor film thickness, mobility, and carrier concentration are all interconnected when describing the AE interaction and need to be optimized to a certain value in order match with the acoustic mode and acoustic frequency chosen. This chapter will begin with an overview of the volumetric AE analytical model and discuss broadly how the effect behaves as a function of applied drift field. Then, the Rayleigh wave amplifier analytical model will be discussed and applied to designing the semiconductor properties for the three material stacks used in this thesis. Finally, initial development of a generalized 2D FEA AE scheme is presented.

3.1 Acoustoelectric Analytical Modeling Overview

Piezoelectric semiconductor materials were one of the first demonstrated with the AE effect. Initial investigations looked at this possibility by investigating the piezoelectric strength and conductivity in both ZnO and CdS bulk materials [76]. Piezoelectric semiconductor materials like CdS are homogeneous and allow for full volumetric overlap between the piezoelectric mode shape and the free carriers. Early demonstrations of the AE effect and AE amplification in CdS were done with bulk acoustic waves [11, 12]. Later, surface elastic wave propagation and AE amplification was also demonstrated in CdS [9]. In these piezoelectric semiconductor

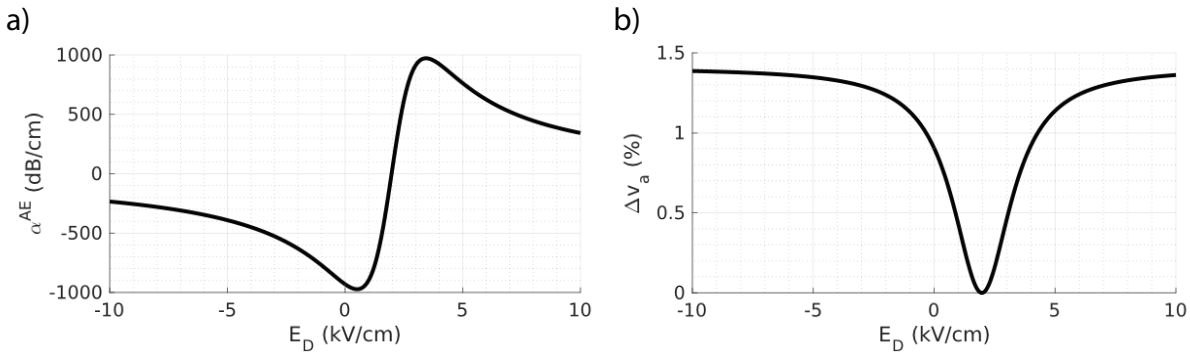

Figure 3.1. (a) Theoretical AE attenuation and (b) AE velocity shift curves for a piezoelectric semiconductor as a function of applied drift electric field.

materials, the equations for AE attenuation (α^{AE}) and acoustic velocity shift (Δv_{a}) are (see [6])

$$\alpha^{\mathrm{AE}} = \frac{k^2}{2}\frac{\omega_{\mathrm{c}}}{v_{\mathrm{a}}}\,\frac{\gamma}{\gamma^2+b^2}, \tag{3.1}$$

$$\Delta v_{\mathrm{a}} = v_0\frac{k^2}{2}\left[\frac{\gamma^2+\dfrac{\omega_{\mathrm{c}}}{\omega_{\mathrm{D}}}+\dfrac{\omega^2}{\omega_{\mathrm{D}}^2}}{\gamma^2+b^2}\right], \tag{3.2}$$

$$\gamma = 1-\left|\frac{\mu E_{\mathrm{D}}}{v_{\mathrm{a}}}\right|, \quad b=\frac{\omega_{\mathrm{c}}}{\omega}+\frac{\omega}{\omega_{\mathrm{D}}}, \quad \omega_{\mathrm{c}}=\frac{q\mu N}{\varepsilon}, \quad \omega_{\mathrm{D}}=\frac{v_{\mathrm{a}}^2 q}{\mu k_{\mathrm{B}} T}.$$

Here, γ and b are dimensionless velocity and frequency terms, respectively. The other parameters are the electromechanical coupling coefficient k^2, acoustic wave velocity v_{a}, acoustic wave velocity without the presence of free carriers v_0, free carrier mobility μ, applied drift electric field E_{D}, acoustic wave frequency ω, elementary charge q, material permittivity ε, free carrier concentration N, Boltzmann constant k_{B}, temperature T, dielectric relaxation frequency ω_{c}, and diffusion frequency ω_{D}.

Example theoretical plots for the AE attenuation and acoustic velocity shift as a function of applied drift field are plotted in Figure 3.1. The AE attenuation is anti-symmetric about the equal velocity point, whereas the acoustic velocity shift is symmetric. This equal velocity point is when the dimensionless velocity $\gamma = 0$. If Figure 3.1 was plotted instead as a function of γ, one would see the AE curves perfectly anti-symmetric and symmetric about the y-axis.

Since devices operate with reference to an applied drift field, then the curves are shifted in the x-axis when plotted as a function of E_{D}. In this example case, the equal velocity condition occurs at an applied drift field of 2 kV/cm. In practical AE device implementation, the forward and backward propagating waves will experience the same drift field, but with opposite polarity. This means the forward and backward propagating acoustic waves will experience not only different polarity of the AE attenuation, but also a relative difference in magnitude. This fact can be taken advantage of when designing variable isolation devices (described later in Chapter 5). Similarly, the acoustic velocity shift due to the AE effect will now be different in magnitude between the forward and backward propagation waves. This unequal shift in acoustic velocity can be taken advantage of when designing an AE-based phase shifter (described later in Chapter 5).

When designing a material stack to optimize the performance of AE devices, there are a few key material parameters to consider. First, both the AE attenuation and velocity shift are directly proportional to the coupling coefficient (k^2). Therefore, a piezoelectric material with the highest possible coupling coefficient is desired for AE devices. The mobility of the free carriers is critical for reducing the power needed for AE devices. Using a semiconductor with a high mobility allows for smaller drift fields to be applied to achieve the same relative carrier drift velocity. Given the same carrier density, applying a smaller drift field will result in a lower applied voltage with the same current, therefore reducing the total input DC power to the system. This can also be beneficial to AE devices that are prone to overheating. With less power heating up the semiconductor, the overall power handling and linearity could be improved by using a semiconductor with a very high mobility. Manipulation of the dimensionless velocity γ shows that lowering the acoustic velocity can have a similar effect. A lower acoustic velocity means a smaller drift field can be applied to achieve the same AE biasing condition. Overall, a combination of high mobility and low acoustic velocity are most desirable for a high performance AE platform.

Finally, the free carrier concentration is critical in determining the optimal performance of the AE device. The diffusion frequency ω_{D} and operating acoustic frequency ω are set based on the acoustic mode chosen for the AE device. In order to maximize the AE effect, the dimensionless frequency term b must be optimized, which means the only remaining term to

analyze is the dielectric relaxation frequency ω_c. This term can be tuned through the choice of a semiconductor carrier concentration N. Effectively, the optimum choice of a carrier concentration is when the acoustic wave is impedance matched to the carriers [77]. Therefore, it is important to develop a material platform that can tune the free carrier concentration to impedance match to the desired acoustic waves at different acoustic frequencies.

This work on analytical AE modeling for piezoelectric semiconductor materials was extended to a piezoelectric acoustic plane wave incident on an infinitely thin 2D semiconductor sheet [78]. This theory for 2D semiconductor thin films could be applicable to many desirable material systems, like AlGaN/GaN heterostructures [79–81] or conductive thin films like graphene [82]. This concentration of interaction area to a 2D film increases the strength of the AE interaction considerably. An analytical comparison of the volumetric and 2D equations for a GaN and AlGaN/GaN material system is presented in [83]. While the 2D analytical equations predict a strong AE interaction, there has not been substantial experimental verification of these equations in 2D semiconducting material systems.

3.1.1 Rayleigh Wave Amplifier Model

The previous AE analytical models considered incident acoustic plane waves interacting either uniformly over a volume or passing through a 2D semiconductor. Since the acoustic wave and free carriers interact through the electrical deformation potential, it is important to consider the spatial overlap of these waves. Since LN itself is not a piezoelectric semiconductor, it requires a semiconductor thin film to be placed in its proximity either above or below. An AE theory was developed by Kino and Reeder for an AE amplifier using a Rayleigh SAW mode in a piezoelectric semiconductor thin film heterostructure [84]. The AE attenuation coefficient and acoustic wave propagation constant perturbation are (see [84])

$$\alpha^{\mathrm{AE}} = \frac{1}{2}\frac{\left(v_s/v_a - 1\right)\omega_c \varepsilon Z_a' \beta_a \tanh\left(\beta_a d\right)}{\left(v_s/v_a - 1\right)^2 + \left(R\omega_c/\omega + H\right)^2}, \tag{3.3}$$

$$\beta^{\mathrm{AE}} = \frac{1}{2}\frac{\left(R\omega_c/\omega + H\right)\omega_c \varepsilon Z_a' \beta_a \tanh\left(\beta_a d\right)}{\left(v_s/v_a - 1\right)^2 + \left(R\omega_c/\omega + H\right)^2}, \tag{3.4}$$

where Z_a is the interaction impedance, β_a is the unperturbed acoustic propagation constant, d is the semiconductor film thickness, R is the space-charge reduction factor, and H is the diffusion term. More details on the interaction impedance, space-charge reduction factor, and diffusion term can be found in [84]. It is also important to note that the form of Equations (3.3) and (3.4) are very similar to those in the volumetric AE analytical Equations (3.1) and (3.2). This AE analytical model was chosen for use in this thesis because the material platforms used are all heterostructures comprised of a piezoelectric (LN) and semiconductor thin film (either Si or InGaAs). This model will also be used later in the thesis for predicting and fitting to the performance of the fabricated AE devices on the InGaAs-LN platform.

3.1.2 Optimal Free Carrier Concentration Determination

As previously discussed, once the acoustic mode and material platform thicknesses are determined, the appropriate carrier concentration needs to be calculated for the AE devices of interest. It was briefly touched upon earlier when introducing the AE effect, but the maximum AE interaction occurs when the carriers are impedance matched to the acoustic mode. Equations (3.1) and (3.2) show that this is related to the dielectric relaxation frequency and diffusion frequency. This means for a desired operating drift electric field, the maximum AE interaction can be obtained by tuning the acoustic frequency, acoustic velocity, semiconductor permittivity, carrier mobility, and carrier concentration. When a piezoelectric layer and acoustic mode is chosen, it sets the acoustic velocity, coupling coefficient, and piezoelectric permittivity. When the semiconductor film is chosen, it sets the mobility that is possible and the semiconductor permittivity. This leaves the carrier concentration (N) and operating acoustic frequency (ω) to tune for maximizing the AE interaction.

Figure 3.2 shows for the InGaAs-LN platform the calculated maximum AE gain as a function of both the carrier concentration and operating acoustic frequency. For each acoustic frequency and carrier concentration value, the drift field is swept until the maximum possible AE gain is found and then plotted. This plot shows that as the desired acoustic frequency is increased, the carrier concentration must also increase in order to stay impedance matched and achieve the optimal AE interaction. An interesting observation is the appearance of

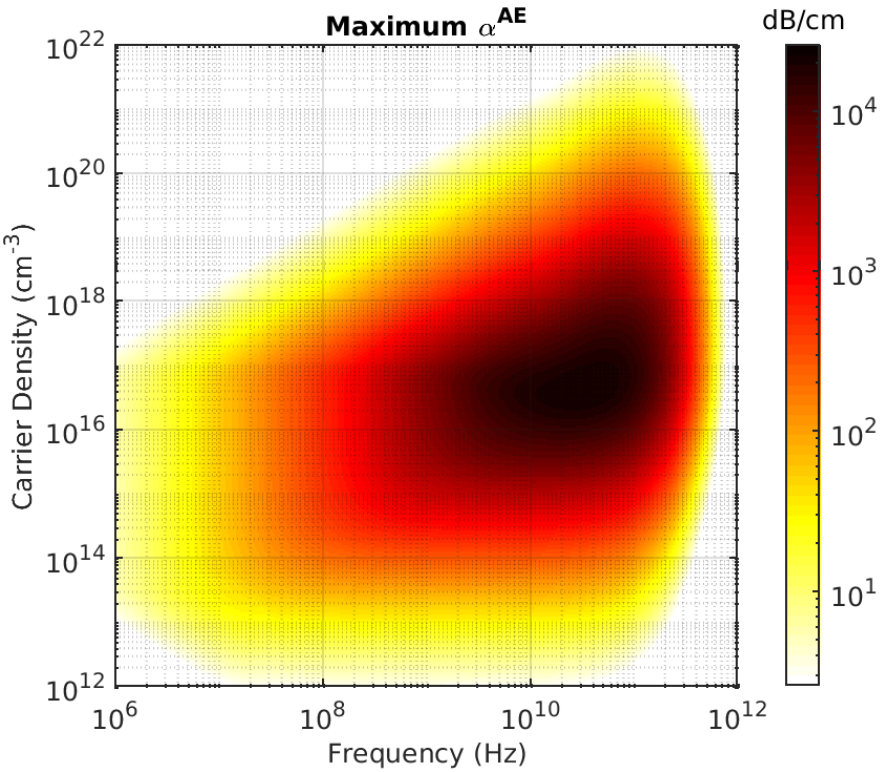

Figure 3.2. Calculated surface plot showing the trends of the maximum AE gain as a function of carrier concentration and acoustic frequency for the InGaAs-LN platform.

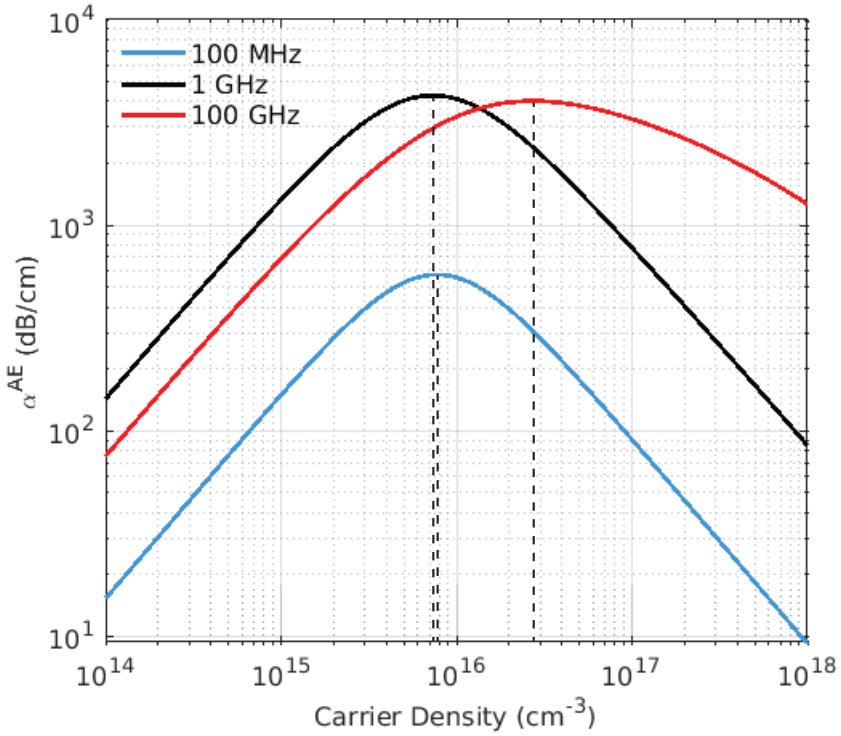

Figure 3.3. Calculated AE gain vs. free carrier concentration at select acoustic frequencies for a given drift electric field operating point (2 kV/cm) on the InGaAs-LN platform.

an absolute maximum interaction, where the effect falls off even at higher carrier concentrations and acoustic frequencies. This is due to the interconnected relationship between the mobility, semiconductor thickness, and acoustic velocity. The acoustic mode chosen sets the acoustic velocity and the ratio between acoustic velocity and mobility determines the diffusion frequency. So given a fixed diffusion frequency for the material platform, there will exist an absolute AE interaction point over the entire carrier concentration and acoustic frequency parameter space. It can be seen in Figure 3.2 that the optimal acoustic frequency range is around 10–40 GHz with a carrier concentration between 10^{16}–10^{17} cm^{-3}.

For the InGaAs-LN platform, which operates in the range of MHz to GHz, slices of the parameter space from Figure 3.2 are plotted for key acoustic frequencies as a function of carrier concentration in Figure 3.3. There are two key takeaways from Figure 3.3. Based on photolithography and e-beam lithography limitations, the fundamental SAW modes on

a LN platform range from MHz to a couple of GHz. As shown in the blue and black curves in Figure 3.3, scaling of the acoustic devices from the MHz range to GHz roughly requires the same optimal carrier concentration, but significantly increases the maximum AE gain achievable. This means that for the InGaAs-LN platform designed for LSAW modes operating around 270 MHz, the devices can be scaled up using e-beam lithography into the GHz range and see over an order of magnitude improvement in the AE performance while still being near the optimal carrier concentration. The second item to consider is the broadening of the AE gain curve as a function of carrier concentration for very high acoustic frequencies (100 GHz). Even though the optimal carrier concentration has shifted, the AE gain drop off at higher carrier concentrations is less than at lower acoustic frequencies. Ultimately, this means at very high frequencies the AE performance is less sensitive to fabrication variations in the carrier concentration levels.

While the AE region definition in the InGaAs-LN platform is straightforward, the design of the AE regions in the LNOSi and LNOSOI platforms are a little more challenging. A similar analysis as detailed above is also done for the LNOSi and LNOSOI platforms. For RF applications in the range of 100 MHz — 10 GHz, the ideal carrier concentrations range is from $5\text{x}10^{14}$ cm^{-3} to $8\text{x}10^{15}$ cm^{-3}. This carrier concentration range, however, is around the standard doping of silicon wafers. This makes it challenging to create Ohmic contacts with the silicon and control where the current flows. A solution to these problems is to do two implantation steps in the silicon wafers before bonding. The first implantation step is to define the AE regions by applying a dose slightly higher than the standard doping of silicon. An implantation of $1\text{x}10^{16}$ cm^{-3} was chosen for these stacks, which is close to the optimal carrier concentration for GHz acoustic devices. The second implantation step is to define regions for Ohmic contacts to the AE regions. This implantation step was chosen to be $1\text{x}10^{19}$ cm^{-3}. Specifically for the LNOSi stack, a high resistivity (HR) silicon wafer was chosen for two reasons. First, this ensures current isolation between AE devices by having a much lower carrier concentration in the non-implanted regions. Second, this allows for the design of AE devices utilizing a gated MIS structure instead of implantation. By applying a gate voltage on top of the LN thin film, an inversion layer of carriers can be formed and used in AE devices.

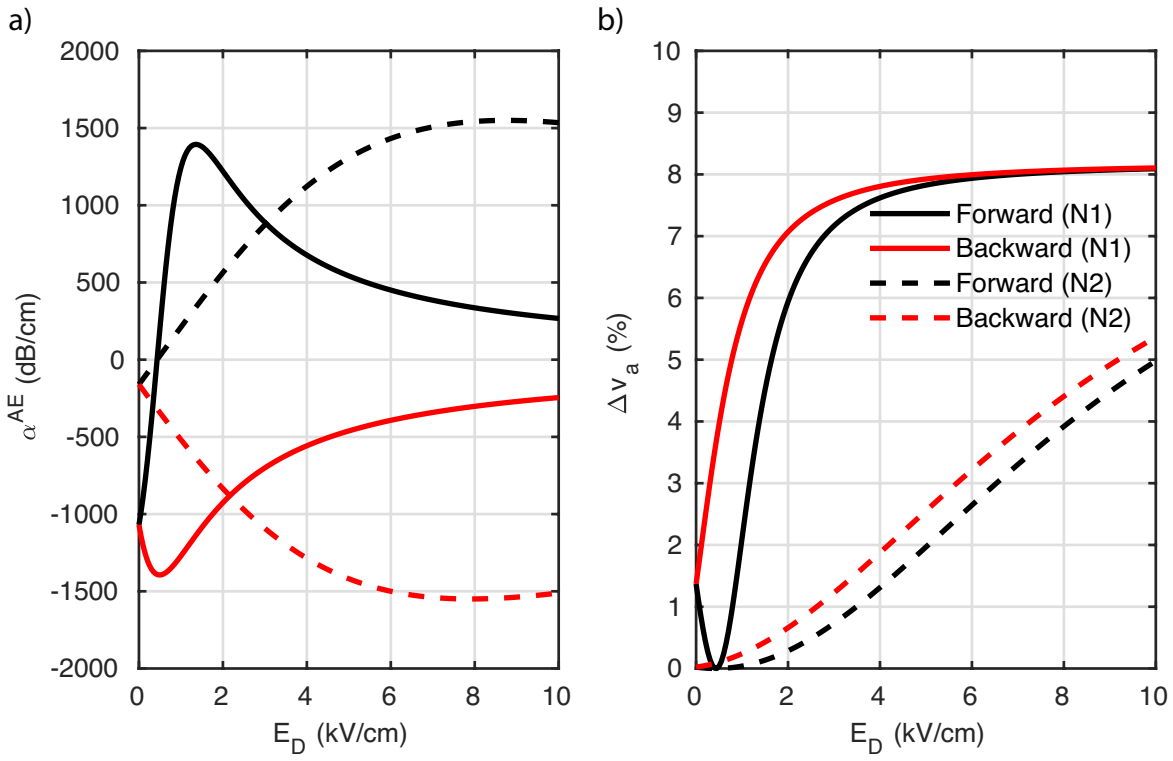

Figure 3.4. Theoretical AE gain and velocity shift as a function of applied drift field for two carrier concentrations: N1 = 5x10^{15} cm^{-3}, N2 = 2x10^{16} cm^{-3}.

The last consideration when designing the AE platform and its carrier density is the relative AE performance between the forward and backward propagating acoustic waves. The carrier concentration affects not only the maximum possible AE gain (or interaction strength), but also the relative gain difference and relative velocity shift between the forward and backward propagating acoustic waves in the device. Figure 3.4 shows the theoretical AE gain and acoustic velocity shift as a function of drift field for two carrier concentrations on the InGaAs-LN platform. For an AE device under an operating drift field, the forward wave will see a positive drift field whereas the backward wave will effectively see the negative drift field applied. To make the comparison clearer, the plotting style (as seen in Figure 3.1) was altered to fold the negative drift field values over and color it red to signify the backward travelling acoustic wave. As an example, if a drift field of +2 kV/cm was applied across the AE device, then the forward wave (in black) would see a +2 kV/cm field, but the backward wave (in red) would effectively see a -2 kV/cm field. The two carrier concentrations chosen

(N1 = $5x10^{15}$ cm^{-3}, N2 = $2x10^{16}$ cm^{-3}) are both near the optimal value, but show very different behavior as a function of applied drift field. The maximum AE gain in Figure 3.4 (a) is almost the same for both N1 and N2 (1500 dB/cm), but the drift field required to reach this value is much larger for N2. This means a much larger input power is required for a device with N2 carrier concentration. Also, the more compressed nature of the N1 curve leads to a larger relative difference in the magnitude of the AE effect between the forward and backward wave. This large difference in relative AE effect magnitude is important for designing a variable isolation AE device (discussed in Chapter 5). A similar effect is seen for the acoustic velocity shift shown in Figure 3.4 (b). For low drift fields applied, AE devices with N1 carrier concentration can have 2-4% relative difference between the velocity shifts, whereas devices with N2 carrier concentration will have a relative velocity difference <1% for any applied drift field value. This large relative velocity shift between forward and backward propagating acoustic waves is key for designing an AE phase shifter discussed later in Chapter 5. Overall, it is important to have the ability to tune the carrier concentration during the fabrication process of the material platforms not only to optimize for the overall maximum AE interaction, but also for the relative AE interaction magnitude between the forward and backward propagating acoustic waves.

3.2 Generalized 2D Acoustoelectric COMSOL Modeling

Currently, the analytical modeling of the AE effect is limited to ideal mode shapes and simple device structures. In order to model the AE effect with arbitrary acoustic modes or resonator shapes in various material stacks, like either the LNOSi or LNOSOI platforms, a numerical model needs to be developed. There has been some work on using Finite Element Analysis (FEA) or Boundary Element Method (BEM) to accurately model the performance of SAW delaylines [85]. For the AE effect, this numerical analysis needs to be extended to couple both the piezoelectric and free carrier governing equations and solve them at the same time. Since COMSOL has been used extensively to model the acoustic behavior of piezoelectric devices, that software platform was chosen to develop the AE FEA modeling. The AE effect uses both piezoelectric and semiconductor carrier physics. Since COMSOL does not have built-in

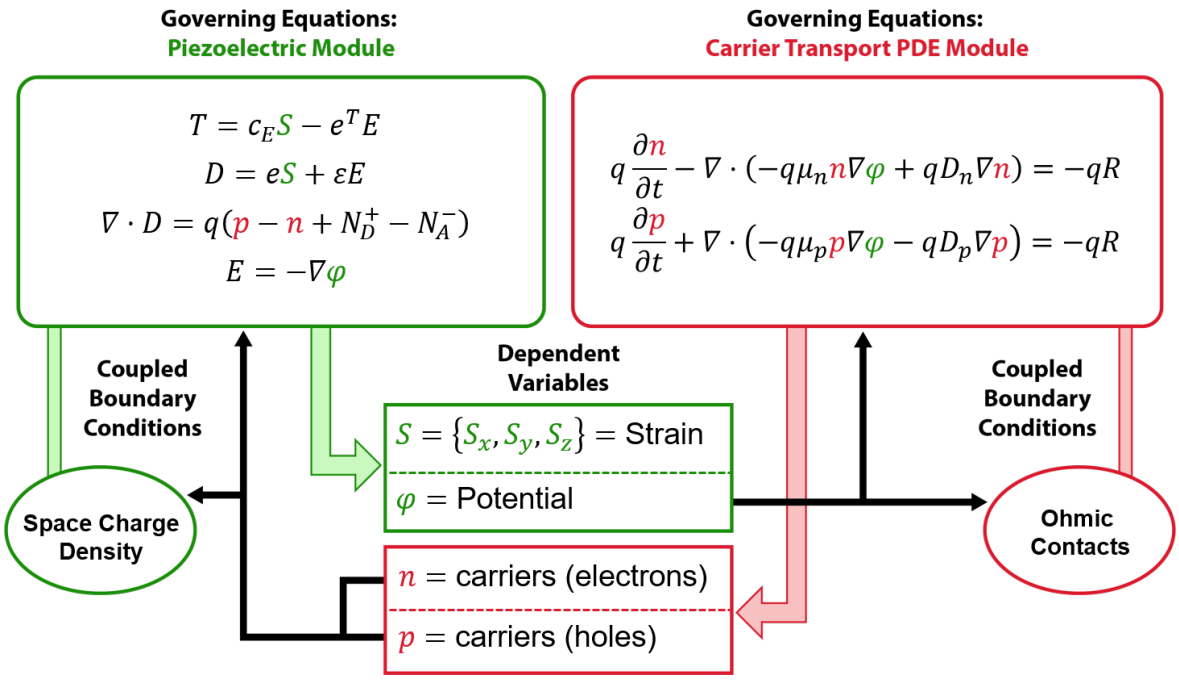

Figure 3.5. Illustration showing the governing equations for the piezoelectric effect and the drift diffusion of the free carriers. The equations are color coded and the inter-relation between the independent variables are shown.

support for coupling these two physics modules, a set of partial differential equations (PDE) for the semiconductor carrier physics will have to be manually coupled to the piezoelectric module. This coupling option allows the user to take advantage of COMSOL's built-in piezoelectric physics module that is optimized for the software's solver engines.

The proposed coupling scheme for numerical AE simulations in COMSOL is shown in Figure 3.5. COMSOL already has a built-in piezoelectric physics module with the dependent variables being the material strain ($\mathbf{S} = \{S_x, S_y, S_z\}$) and potential ($\varphi$). The only other dependent variables needed are the electron and hole free carrier concentrations (n and p). These can be introduced by adding a partial differential equation (PDE) math module in COMSOL for the drift-diffusion carrier transport equations [86–88]. In total, there are 4 dependent variables: two solved by the piezoelectric module (S and φ) and two solved by the carrier transport PDE (n and p). The only modification to the piezoelectric physics module was the addition of a space change density volumetric boundary as a function of the net carrier concentration present in the material. The semiconductor carrier physics

were captured in a set of equation-based PDEs. The potential (φ) dependent variable was implemented in the equation-based PDEs and also in the Ohmic boundary conditions, which are implemented as a Dirichlet boundary condition. The initial model development used a homogeneous piezoelectric semiconductor material with simple actuation methods, such as a BAW mode and Rayleigh SAW mode in time domain COMSOL simulations. The following subsections will cover how the model was setup and equations implemented in the COMSOL software, how the COMSOL values and analytical expressions are computed and related to each other, and finally the initial results and future work discussion.

3.2.1 COMSOL Coupled Physics Implementation

For practical implementation of these governing equations, several steps need to be taken to couple these two modules in COMSOL and to avoid any numerical or convergence errors. Since the major and minor carrier concentrations sometimes vary by 30 orders of magnitude or more, the dependent n and p variables were transformed into the log scale. COMSOL then solves for these exponent values, named n^{L} and p^{L} and are related to the original dependent variables as

$$n = \mathrm{e}^{n^{\mathrm{L}}},$$
$$p = \mathrm{e}^{p^{\mathrm{L}}}.$$

Another thing to help avoid numerical displacement errors, especially near 0 V biasing conditions, was to implement a small built-in DC voltage that is always on. During these initial development stages, a built-in DC voltage of 1 μV was used.

In terms of the time domain simulation parameters, the maximum time step size was carefully chosen to provide numerical stability. Within each time step, the displacement of any free carriers or piezoelectric acoustic wave should not exceed the distance between mesh elements. The maximum time step chosen for these AE simulations is defined as

$$t_{\mathrm{step}}^{\mathrm{max}} = \frac{\mathrm{CFL}\, h_{\mathrm{max}}}{v_{\mathrm{a}} N_{\mathrm{df}}},$$

where CFL is the Courant-Friedrichs-Lewy number, $h_{\max}$ is the maximum mesh size, and N_{df} is the evaluation point division factor. For the FEA simulations in this chapter, a CFL number of 0.2 was chosen. The maximum mesh size was set to be $\lambda/5$, where λ is the acoustic wavelength. The acoustic velocity is set by the Bulk Acoustic Wave and Rayleigh SAW modes used. Finally, the division factor was set to 2. When starting the time domain simulation, an initial stationary step was implemented to slowly ramp up the DC bias voltage from 0 to the desired $\mathrm{V_{DC}}$. The default solver configuration was changed from fully coupled to a segregated solver. This change was necessary because a lower limit to the dependent variables n^{L} and p^{L} needed to be applied. The lower limit of -150 was set for both variables so that the solver converges and doesn't look for a 0 carrier density by searching for a $-\infty$ carrier density in the log scale. The following sections outline the two devices simulated in FEA using these implementation methods.

3.2.2 Piezoelectric Semiconductor BAW Resonator Model Setup

The simulation of an ideal BAW resonator is a first attempt at validating the coupling between the piezoelectric and carrier PDEs in the FEA modeling. Figure 3.6 is a diagram of the modeled ideal BAW resonator in a piezoelectric semiconductor material. The BAW resonator in Figure 3.6 is made of bulk GaN with full length aluminum electrodes on top and bottom. Symmetric boundary conditions were applied on the sides to simulate an ideal (infinite) BAW resonator. The ideal mode shape is shown in the bottom right and has a resonant frequency of 778 MHz. Most of the AE theory is described in terms of the mode's attenuation coefficient. Therefore, the goal was to simulate the attenuation coefficient of the BAW resonator. Initial attempts were poor at fitting to the rise constant of the displacement's time evolution. The time evolution was not entirely exponential, which led to inaccurate attenuation coefficients while fitting. One solution is to allow the signal to reach steady state and then switch off the AC driving voltage. Then, extend the simulation time to allow the displacement to decay back down to 0. The decay envelope could be more accurate, but this was an impractical solution because the simulations would take too long to run.

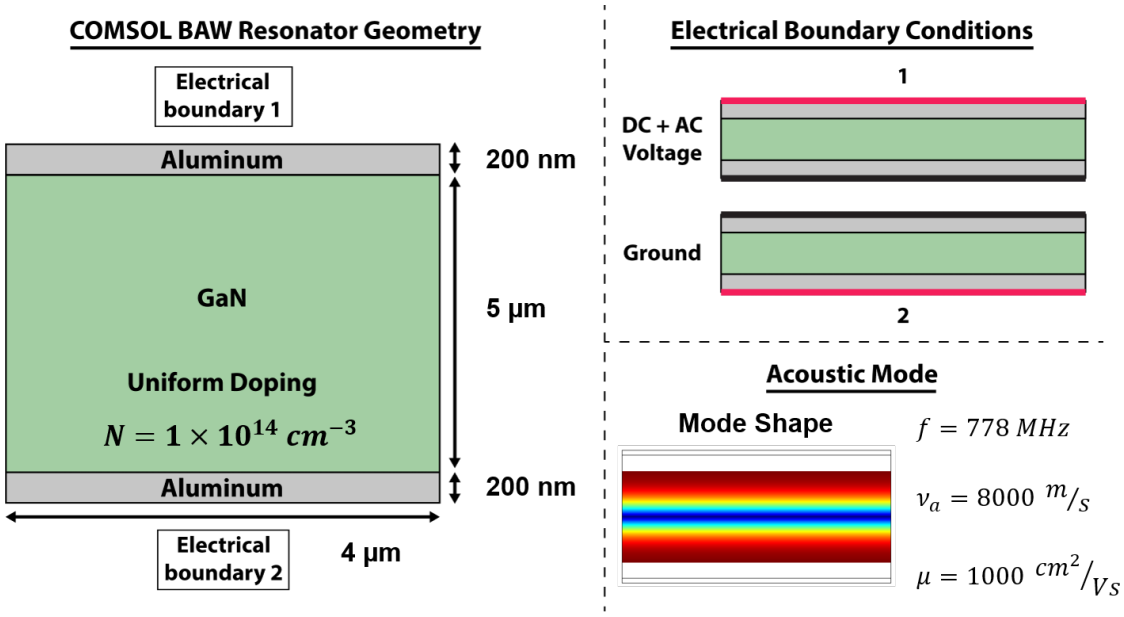

Figure 3.6. Illustration of the BAW geometry and boundary setup in COMSOL for AE FEA.

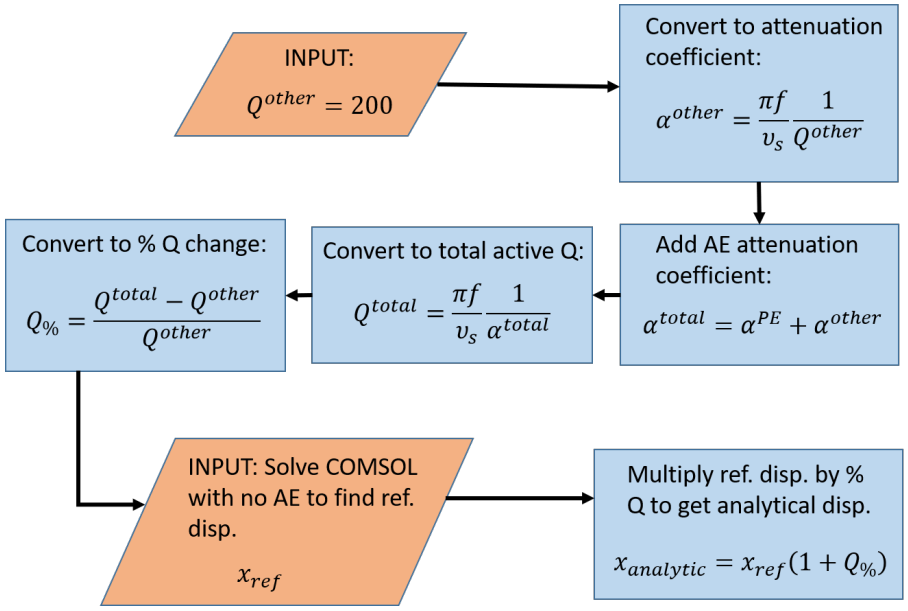

Figure 3.7. Flowchart showing how the BAW COMSOL Q is computed, converted to an attenuation value, and then compared to the analytical theory.

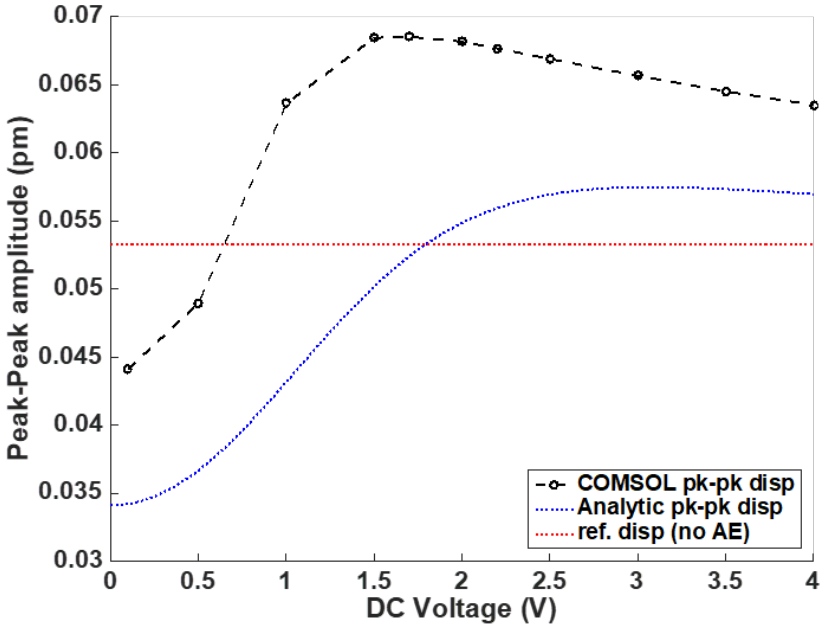

Figure 3.8. Plot of the COMSOL simulated AE attenuation vs. analytical AE theory for a volumetric piezoelectric semiconductor BAW resonator.

Instead, the theoretical AE attenuation coefficient was converted into a theoretical steady state displacement. Figure 3.7 shows a flow chart for converting the theoretical attenuation coefficient into a theoretical displacement. The first step was converting the unbiased resonator's losses (quality factor) into an attenuation coefficient. Then, the theoretical AE attenuation coefficient is added to give the total theoretical attenuation coefficient. This is again converted back into an effective quality factor and expressed as a percent change relative to the unbiased condition. The unbiased displacement was simulated in COMSOL with no coupling to the carriers. Finally, the expected displacement is found by multiplying the reference displacement with the analytical percent change curve.

3.2.3 BAW Analysis and Initial Results

Figure 3.8 shows the comparison between the simulated BAW displacement and expected displacement. The large discrepancy in the graphs can be attributed to the comparison method. The expected (analytical) displacement is not purely analytical and requires a

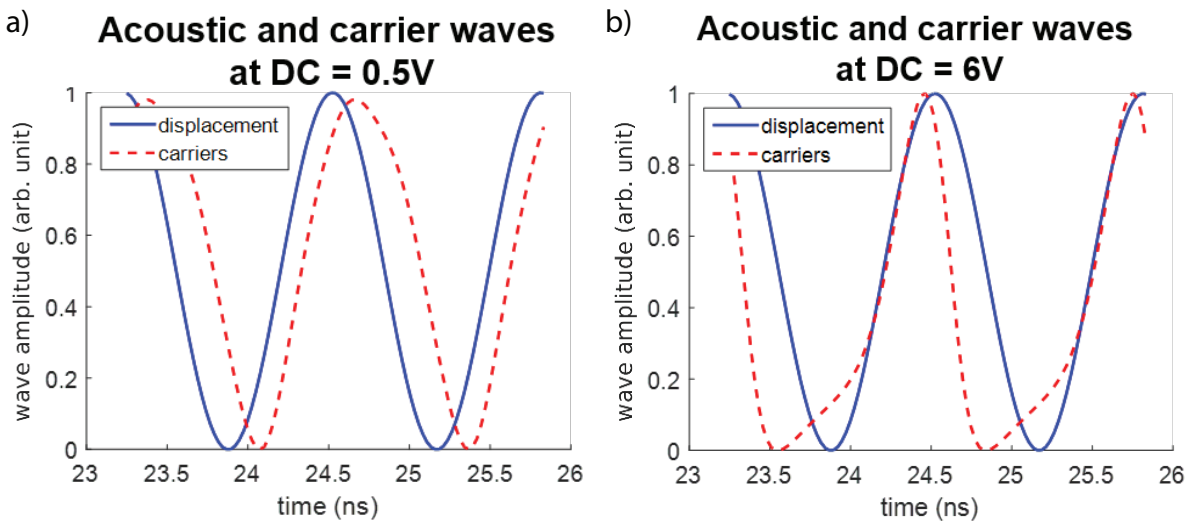

Figure 3.9. Plot of the simulated acoustic and carrier waves in time for small and large DC voltages applied. As the DC voltage is increased, bunching of the carriers is observed.

simulated reference displacement. Therefore, if the reference displacement is not accurate, the entire analytical displacement curve will be shifted. A more accurate comparison would involve the attenuation coefficients directly, but this is difficult to extract from COMSOL transient simulations. While the absolute numbers don't show good agreement, the trend in the simulated displacements does show coupling between the piezoelectric and carrier PDEs. More evidence of coupling is shown in Figure 3.9. When the drift voltage applied is low (0.5 V), the carriers move out of phase with the acoustic wave, either leading or lagging the displacement wave. When the drift voltage is increased high enough (6 V), the carriers experience bunching within the potential field and travel in phase with most of the displacement wave.

3.2.4 Piezoelectric Semiconductor SAW Delayline Model Setup

The second test device for this AE coupling scheme in COMSOL is a simple travelling SAW delayline amplifier made using a homogeneous piezoelectric semiconductor material. The geometry and boundary conditions for this SAW delayline are shown in Figure 3.10. GaN was chosen as the piezoelectric semiconductor material with a uniform fixed charge density

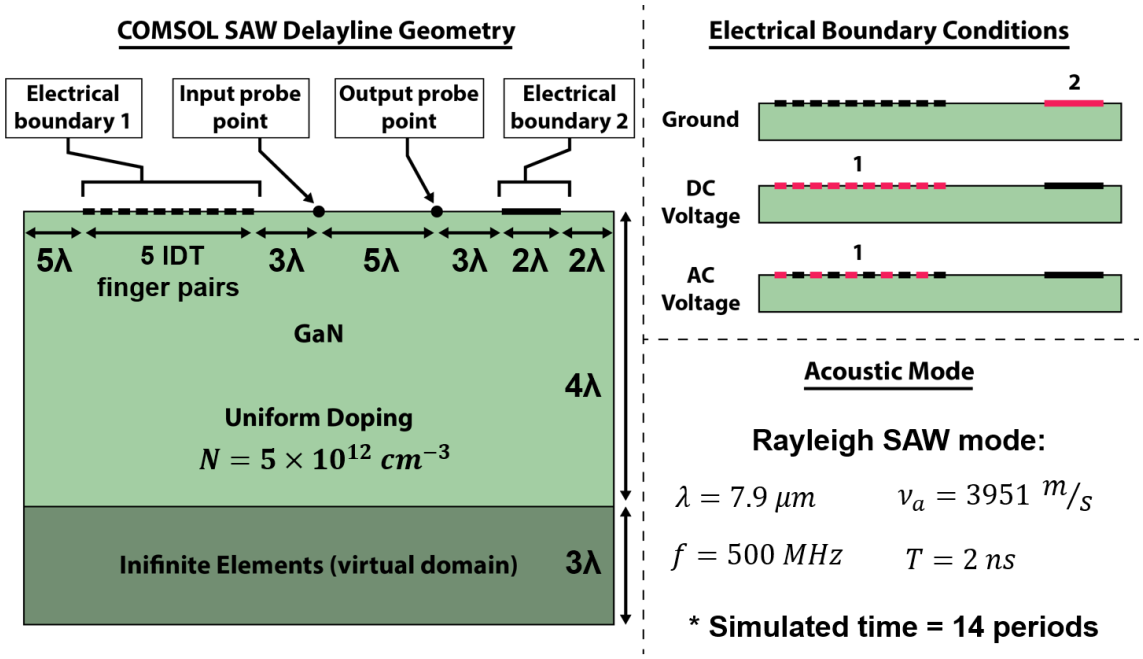

Figure 3.10. Illustration of the SAW delayline setup, including the geometric parameters, boundary conditions, and probe points.

of 5x10^{12} cm^{-3} and mobility of 1000 cm^2/Vs. The GaN material was made 4 wavelengths thick so that all of the SAW mode energy was contained in the simulation domain. The infinite elements underneath the GaN are to stretch the coordinate system to resemble a full substrate thickness. A total of 5 IDT finger pairs were used to launch the SAW wave in a time domain simulation. Since the delayline is propagating to the right, 5 wavelengths were added to the left so that the reflected SAW wave off the left domain will have sufficient delay to not interfere with the pick off times on the right side of the domain. A cushion of 3 wavelengths between the input/output amplitude probe points and the applied DC voltages are necessary to remove electric field discontinuity effects at the applied voltage boundaries. Therefore, the simulated attenuation coefficient is calculated from a 5 wavelength propagation region in the middle of the simulation region. In order to create a drift field for the carriers, a DC voltage was placed under all of the IDT fingers and a ground bus 2 wavelengths wide was placed after the input and output probe points. The AC voltage is then applied to alternating IDT fingers to generate the travelling SAW wave. Finally, artificial mechanical damping was added to stabilize the time stepping. Rayleigh damping was implemented with only the stiffness matrix (beta damping) term. This damping is directly proportional to the strain rate and acts similar to viscous damping. This provides damping that is larger at higher simulated frequencies, which can help suppress high frequency spurious modes. The beta damping term (β_{RD}) was set with a desired loss factor ($\eta_{\mathrm{RD}} = 10^{-3}$) at the SAW resonant frequency (f) as $\beta_{\mathrm{RD}} = \eta_{\mathrm{RD}}/2\pi f$.

3.2.5 SAW Analysis and Initial Results

In order to accurately compare the COMSOL time domain AE simulation with the theory presented in Equation (3.1), the total attenuation coefficient will be considered. The total attenuation is

$$\alpha^{\mathrm{total}} = \alpha^{\mathrm{AE}} + \alpha^{\mathrm{other}}, \tag{3.5}$$

where α^{other} is the attenuation encompassing all other loss mechanisms besides the AE effect. For computing the analytical AE attenuation, all of the same parameters from COMSOL were used in the calculation of the attenuation coefficient (mobility, acoustic velocity, fre-

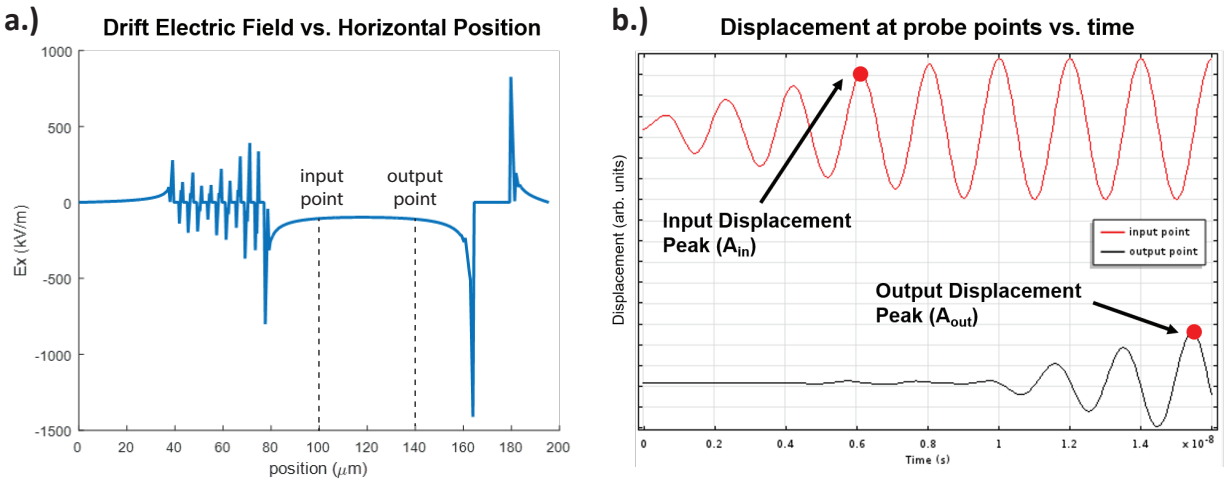

Figure 3.11. Example (a) drift electric field and (b) input/output probes extracted from a COMSOL time domain AE SAW simulation.

quency, doping, etc.) except for the piezoelectric coupling coefficient of the SAW mode. This is very difficult to compute in COMSOL (for a traveling wave mode) so a value of $k^2 = 0.8$ % is used in calculations. Experimentally, GaN has shown $k^2 = 0.08$ %, so this discrepancy of an order of magnitude needs to be investigated further. The Rayleigh beta damping term modifies the stiffness matrix, which could affect the coupling coefficient. For future work, a more extensive study would need to be performed to investigate the interplay between the Rayleigh damping magnitude and the piezoelectric coupling coefficient scaling.

When calculating the AE attenuation from Equation (3.1), a couple adjustments need to be made to match the non-ideal conditions in the COMSOL file. Since the DC field is not uniform over the propagation region in the COMSOL simulation, the DC field profile within the propagation region is extracted from COMSOL. Figure 3.11 (a) shows the extracted drift field profile as a function of horizontal position along the SAW delayline. The dashed vertical lines show the horizontal position of the input and output probe points. At every point within the propagation region between the input and output points, the analytical attenuation coefficient is computed with the specific DC field value extracted from COMSOL. The other attenuation (α^{other}) also needs to be extracted from the COMSOL simulation, which is achieved by running the simulation with the fixed and free carriers set to 0. The average analytical attenuation coefficient is then computed by adding α^{other} and integrating

over the entire propagation region. The equation for the average analytical attenuation coefficient is

$$\alpha_{\text{avg}}^{\text{analytical}} = \frac{1}{d_{\text{prop}}} \int_{\text{input pt}}^{\text{output pt}} \left(\alpha^{\text{AE}}(x) + \alpha^{\text{other}} \right) \mathrm{d}x, \tag{3.6}$$

where d_{prop} is the propagation distance between the input and output probe points.

For the numerical attenuation calculation, the displacement amplitude at both the input and output probe points are monitored in the time domain. The peak amplitude at the input probe point (A_{in}) is tracked by adding the expected delay time and finding the corresponding peak amplitude at the output probe point (A_{out}). The attenuation exponent is then found by taking the ratio of these amplitudes and dividing by the propagation distance. The expression for the numerical average attenuation coefficient is

$$\alpha_{\text{avg}}^{\text{numerical}} = \frac{1}{d_{\text{prop}}} \ln \left(\frac{A_{\text{in}}}{A_{\text{out}}} \right). \tag{3.7}$$

Figure 3.11 (b) shows an example probe output from COMSOL as a function of simulation time. The input and output displacement curves are offset in the vertical axis for clarity. The input displacement peak is tracked over 5 cycles and then found at the output probe for computing the numerical average attenuation coefficient.

The comparison between the analytical and numerical attenuation coefficient are shown in Figure 3.12. There is good agreement between the simulation and theory as well as showing a trend in the attenuation coefficient consistent with the AE effect. Further analysis is necessary to determine if the discrepancy between the analytical and COMSOL attenuation coefficients is a result of the piezoelectric coupling coefficient scaling or because of the temporal resolution in the COMSOL simulation. Since the attenuation simulated is so small, then the difference between the input and output amplitudes is also small. The current temporal resolution only had a couple simulated points in the displacement peaks. Increasing the temporal and spatial resolution of this simulation could help reduce the discrepancies with the analytical attenuation coefficient.

At low voltages (< 6 V), the total attenuation coefficient is larger than the reference attenuation (α^{other}). Since the free carriers are moving slower than the acoustic wave, energy is

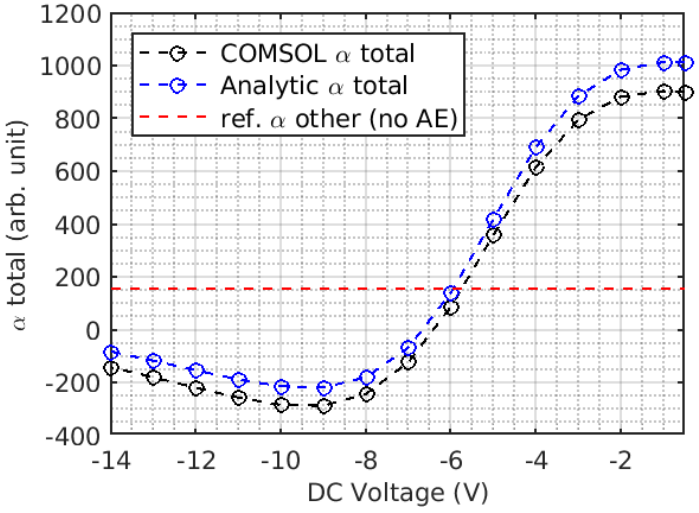

Figure 3.12. Comparison between the COMSOL simulated AE attenuation and analytical theory.

being transferred from the acoustic mode and therefore increasing its attenuation coefficient. Above 6 V, the free carriers are travelling faster than the acoustic mode and energy is being transferred to the acoustic mode, reducing the attenuation coefficient. The attenuation coefficient becomes negative above 8 V, which means enough energy is being transferred to the acoustic mode to compensate for the other losses and achieve amplification.

The next step in simulating the AE effect is to expand the physics to handle heterostructures, which would be useful in designing AE devices in more complicated material platforms, like all three of the platforms used in this thesis. The first heterostructure to simulate would be an extension of the GaN SAW device. Using an AlGaN/GaN heterostructure, the SAW mode can interact with the 2DEG formed at the interface. There are a couple challenges in implementing these simulations because they require adjustments to the current COMSOL code. Currently, the carrier physics is described with simple homogeneous drift-diffusion relationships. When heterostructures are implemented, the carrier physics need to capture the proper energy band profiles and continuities. There has been some work on modeling AlGaAs/GaS heterostructures with thermionic-field emission boundary conditions [89]. There has also been some work in modeling the AlGaN/GaN heterostructure by solving the Poisson and Schrodinger equations [90, 91] or even using a δ-doping model [92]. The biggest challenge in implementing heterostructures for simulating the AE effect is getting the FEA solvers to converge. For homogeneous materials, the basic direct FEA solvers were sufficient. In order to get these heterostructure devices to converge, more advanced settings in both direct and iterative FEA solvers need to be explored.

4. LITHIUM NIOBATE ON SILICON ACOUSTOELECTRICS

This chapter covers all of the work on the LNOSi platform for AE devices. The First section covers the passive AE device. This includes the device design of a capacitor in the propagation path of the delayline, the fabrication process, and testing results and conclusions. The second section covers the active AE segmented delayline on the doped LNOSi platform. For active devices, doping is required to define the AE regions where current will flow. The full device fabrication will be outlined along with some of the fabrication challenges. Some preliminary non-reciprocal insertion loss is presented between the S_{21} and S_{12} S-parameters.

4.1 Gate Controlled Passive Acoustoelectric Devices

For the LNOSi and LNOSOI material platforms, there is a lot unknown about the effects of bonding a LN thin film to an oxidized Silicon wafer. This bonding process could introduce more interface trap charges or generate fixed charges in the oxide. When designing for a certain carrier concentration, the interface and trapped charge effects from the bonding process need to be known so that these effects can be compensated. In a metal-insulator-semiconductor (MIS) structure, the desired carrier concentration can be obtained by either implantation of the semiconductor layer or a gate metal bias to create an inversion later. There has been similar work on controlling the carrier concentration with a gate voltage to tune the AE effect on ZnO/GaN [93], MoS_2/LN [94], and InGaAs quantum well on LN [95]. The work presented in this section [96] will cover the design, fabrication, measurement, and analysis of the gated results on the LNOSi platform.

4.1.1 Gate Control Theory

Figure 4.1 shows an inset of the MIS capacitor structure in the delayline propagation path and a plot of maximum AE gain as a function of sheet conductance. The LNOSi material stack consists of a top gold metal layer, 600 nm thin film of 128° Y-cut LN (k^2 = 5 %), and a 15 nm thermal SiO_2 layer on a standard doped Silicon wafer (N = 1x10^{16} cm^{-3}). The application of a gate voltage creates an inversion layer at the LN/Si interface. By changing

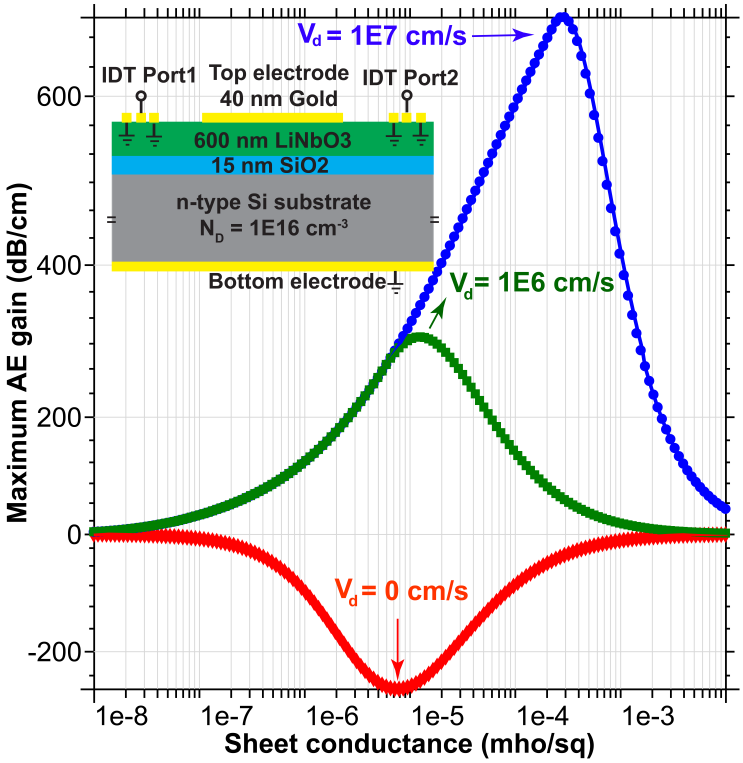

Figure 4.1. Analytical calculations of the maximum AE gain from the sheet conductance at the LN/Si interface for various carrier drift velocities.

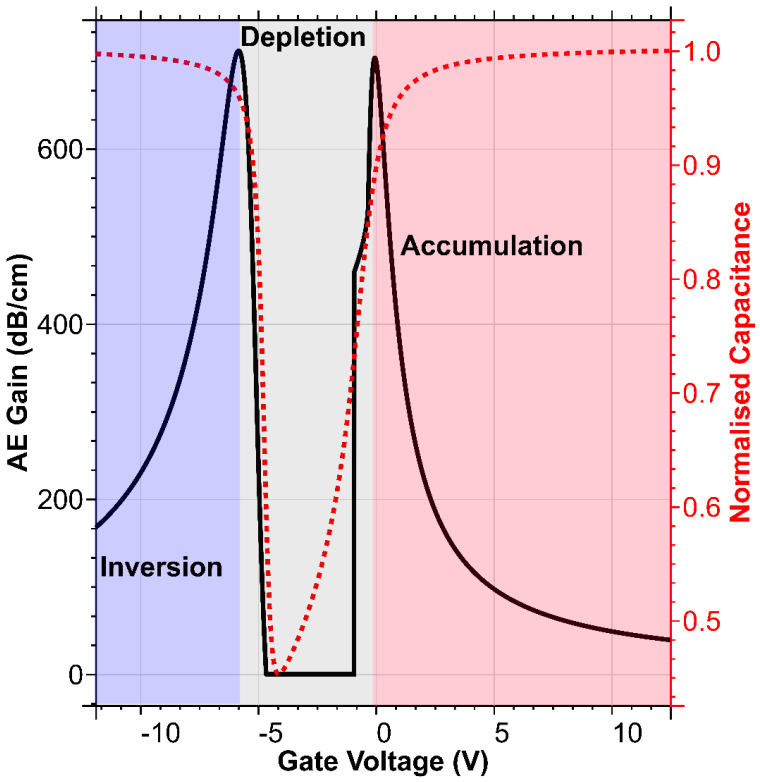

Figure 4.2. Analytical calculation of AE gain for the gated LNOSi delayline assuming a carrier drift velocity of 10^7 cm/s.

the gate voltage, the sheet conductance can change depending on operating region of the device (inversion, depletion, accumulation). With no drift field applied, the free carriers have a drift velocity of 0, which leads to AE attenuation for all possible sheet conductance values (no AE gain). This is illustrated by the red curve in Figure 4.1. There is an optimal sheet conductance value where the maximum AE interaction takes place, resulting in a maximum AE attenuation value. As a drift velocity is imparted, the carriers begin to move faster than the acoustic wave and results in AE gain. The optimal sheet conductance increases with increasing carrier drift velocities, which means gated control of the carrier concentration is key in the LNOSi platform in order to operate at the optimal interaction sheet conductance.

The gate voltage applied to the surface of the LN thin film changes the surface potential of the Si substrate, which alters the carrier density distribution within the Si. Figure 4.2 shows the AE gain as a function of applied gate voltage assuming a carrier drift velocity of 10^7 cm/s. To better illustrate the effect of gate voltage on the AE interaction strength,

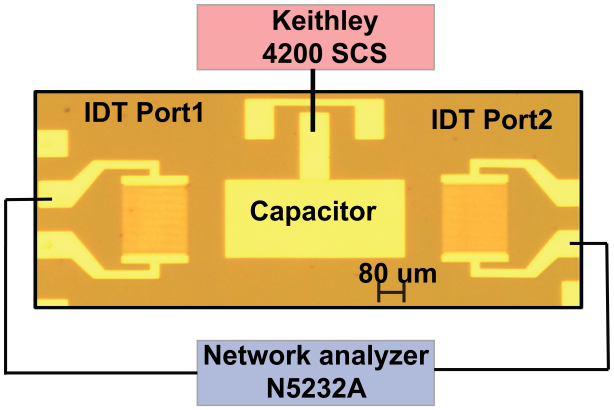

Figure 4.3. Optical image of the fabricated MIS AE delayline and schematic of the measurement setup.

the normalized capacitance of the MIS structure is also plotted. The two peaks in the AE gain correspond to inflection points in normalized capacitance curve. These inflection points between accumulation-depletion and depletion-inversion regions indicate flat-band and weak inversion conditions, respectively. The AE strength decreases as the device enters accumulation because the majority carriers screen the interaction. Then, as the device enters depletion the space charge region effectively increases the dielectric spacing between the acoustic wave and free carriers. Finally, in the strong inversion regime a similar screening occurs and reduces the AE interaction strength. The peaks in the AE gain near the flat-band and weak inversion regions indicate impedance matching conditions between the acoustic wave and semiconductor.

4.1.2 Fabrication and Measurement

Figure 4.3 shows the fabricated basic delayline and experimental setup for passive AE measurements. The device design, fabrication, and measurement was done by Umesh Bhaskar and more details on the experiment can be found in [96]. The fabrication starts with a 15 nm layer of thermally grown SiO_2 on a Silicon substrate. This thin layer of oxide is meant to act as a dielectric buffer between the bonded LN and the n-type Silicon substrate in an attempt to reduce the effects of interface traps. A 128° Y-cut LN thin film is then bonded to the n-type Silicon substrate through "ion-slicing" [97]. Then liftoff is performed to place gold

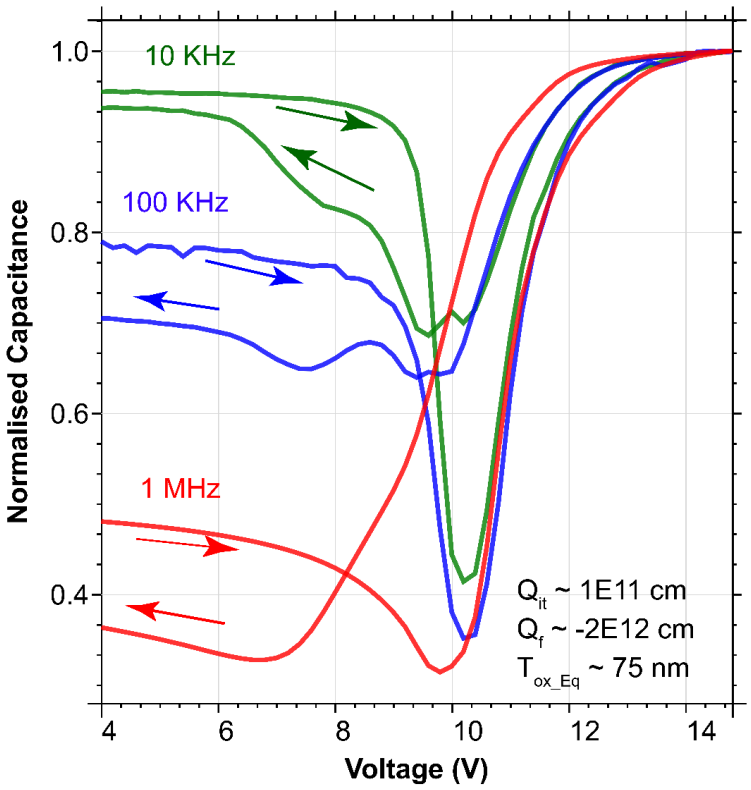

Figure 4.4. CV measurement of the MIS capacitor.

IDTs and a gold top gate metal to form the delaylines. These MIS delaylines were fabricated with the same number of IDT finger pairs and aperture, but with varied acoustic wavelengths ranging from 4.5 μm to 10 μm. The range of acoustic wavelengths is used to determine the dispersion of the acoustic velocity and k^2 as a function of frequency. The MIS capacitor shown in Figure 4.3 is used to tune the surface conductivity electrostatically, which in turn will change the AE attenuation strength.

4.1.3 Results and Discussion

The first experiment looked at the effect of the LN bonding process on the interface trap density (Q_{it}) and fixed charge density (Q_{f}). CV measurements were performed and are shown in Figure 4.4. The CV measurements were performed at three different RF frequencies to get the varied response rates of the trapped and fixed charges in order to calculate the density of each. Based on the gate voltages required to transition from accumulation to depletion, there

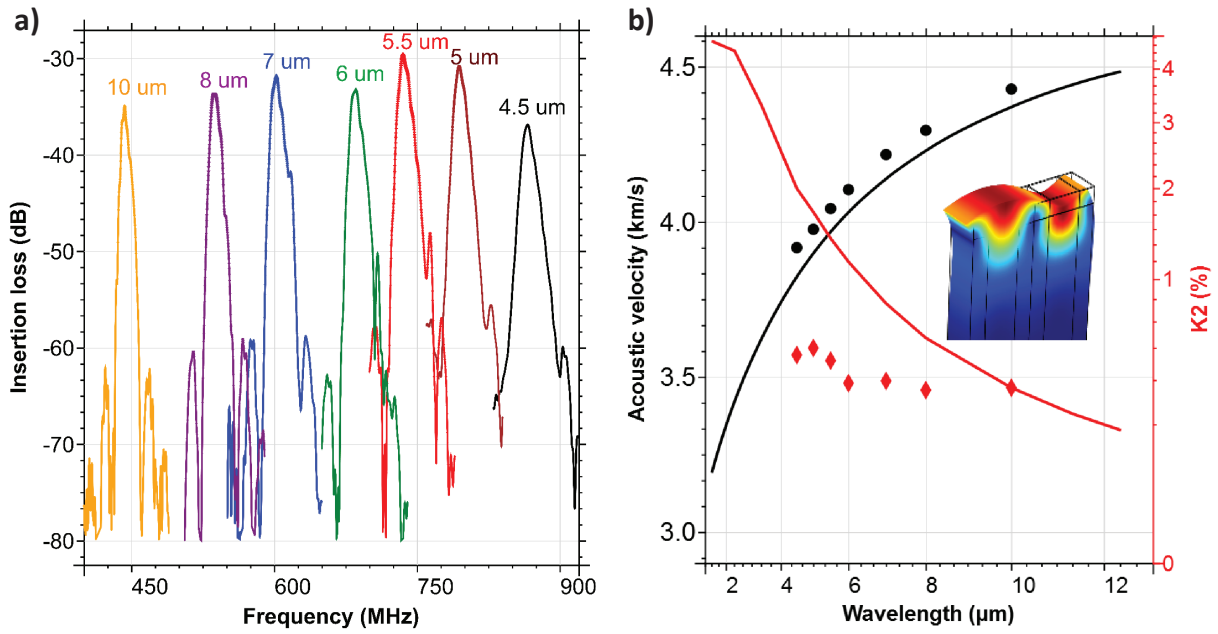

Figure 4.5. (a) Insertion loss of the measured delaylines (time-gated) for acoustic wavelengths ranging from 4.5 μm to 10 μm. (b) Measured dispersion of the acoustic velocity and coupling coefficient (symbols) compared to COMSOL simulation (solid lines). The figure inset shows the Rayleigh SAW mode shape.

is a positive shift in the effective flat-band voltage (instead of at the designed gate voltage of 0 V). This positive voltage shift in the flat-band leads to the presence of a negative fixed charge density as a result of the bonding process. One possible source of this increase in fixed charges is the out-diffusion of some oxygen ions from the LN thin film during the 500° C, 24 hour long post-bond anneal in ambient air. The moderate level of interface traps could be a result of the quality of the thermally grown oxide. This trap density could be lowered through the growth of a MOS-quality thermal oxide instead.

The next set of experiments examine the effect bonding had on the acoustic performance of the SAW mode. The experimentally fitted k^2 was compared to COMSOL simulations and showed a large deviation at smaller wavelengths. For example, the 5 μm wavelength delayline had an experimental k^2 of 0.5% compared to a COMSOL simulated k^2 of 2%. This degradation of the coupling could be a result of damage to the LN crystal during the thinning process. Subsequent samples had a better bond quality and polished LN surfaces to remove crystal damage. The passive AE measurement was performed using a network analyzer and

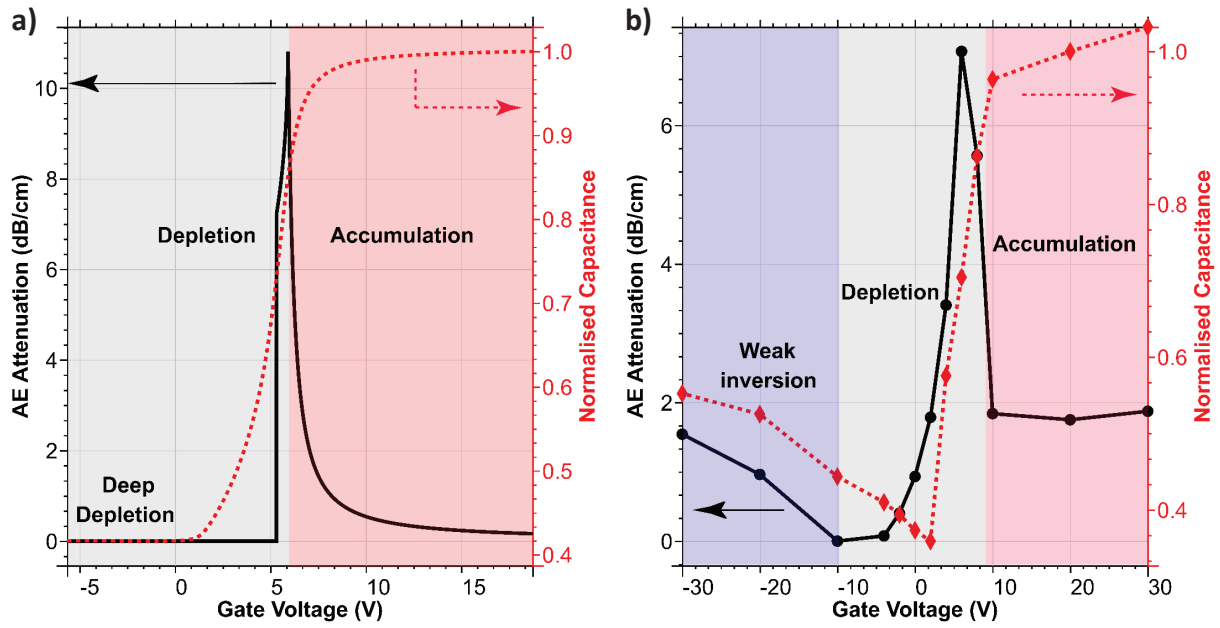

Figure 4.6. (a) Analytical and (b) experimental AE attenuation as a function of the applied gate voltage for a MIS delayline with a 795 MHz acoustic frequency.

Keithley SCS. Two port S-parameter measurement were taken as the gate voltage on the delayline was varied. At each gate voltage, the peak of the S21 data was found and its attenuation was recorded. The analytical and experimental passive AE results for the 5 μm delayline are shown in Figure 4.6. Since the silicon wafer in this LNOSi chip is standard doped, at 0 V gate voltage the carriers should be impedance matched to the acoustic wave. While the doping of the silicon wafer is ideal to maximize the AE interaction strength, it is also very susceptible to the electrostatic potential from surface states [98]. When the carriers and acoustic wave are impedance matched, there should be a peak in the AE attenuation. As the gate voltage is made positive, it should enter accumulation and the AE effect should be screened, resulting in a smaller AE attenuation. As a negative gate voltage is applied, it enters depletion and the reduction in free carriers at the surface would result in a smaller AE attenuation. The experimental results in Figure 4.6 (b) show the flat-band is shifted to a gate voltage of 6 V due to a large number of negative fixed charges (Q_f = -2x10^{12} cm^{-2}) at the LN/Si interface. Therefore, it would be very difficult for ungated devices to work on the

LNOSi stack because the large negative fixed charge density shifts the carriers to depletion at 0 V gate voltage. This means being able to control (and reduce) the interface trap density (Q_{it}) and fixed charge density (Q_{f}) during the fabrication process is essential to achieving a maximum AE interaction. If p-type Silicon doped regions are used instead, the negative fixed charge density could create an inversion layer for use in AE devices. This induced weak inversion layer could be impedance matched with the acoustic wave, as shown in the first AE gain peak in Figure 4.2.

4.2 Acoustoelectric Effect in Doped Silicon Devices

In order to make active AE devices on the LNOSi platform, additional doping steps were implemented before the LN bonding process in order to define impedance matched AE regions and DC Ohmic contact regions. With highly doped Ohmic contact regions, there are two ways to achieve a desired carrier density on the LNOSi platform. The first method is to use a MIS (as in the last section) structure in the delayline propagation path while also supplying a drift field in the propagation direction. Experimentally, an active AE device has been demonstrated on the LNOSi stack using this gated approach. The gates were segmented and connected in parallel to allow for smaller voltages to be applied to achieve large drift fields for AE gain. For this device, there was only an Ohmic contact implantation ($1\text{x}10^{19}$ cm^{-3}) and the segmented gates were used to tune the carrier concentration in the High Resistivity (HR) silicon wafer. These devices were designed, fabricated, and measured by Umesh Bhaskar [21]. The limiting factor in these devices, however, was the applied drift field. Larger drift fields could not be applied because this device is limited by substrate currents. At large drift fields, the substrate current becomes larger than the surface current. This can be improved by designing a device with an inversion channel or incorporating the AE implantation regions.

Figure 4.7 shows an illustration of a segmented AE delayline on the doped LNOSi platform. In addition to the Ohmic doping, a second AE region doping ($1\text{x}10^{16}$ cm^{-3}) is performed before the bonding process. Since this is on a HR Si wafer, no current should flow between

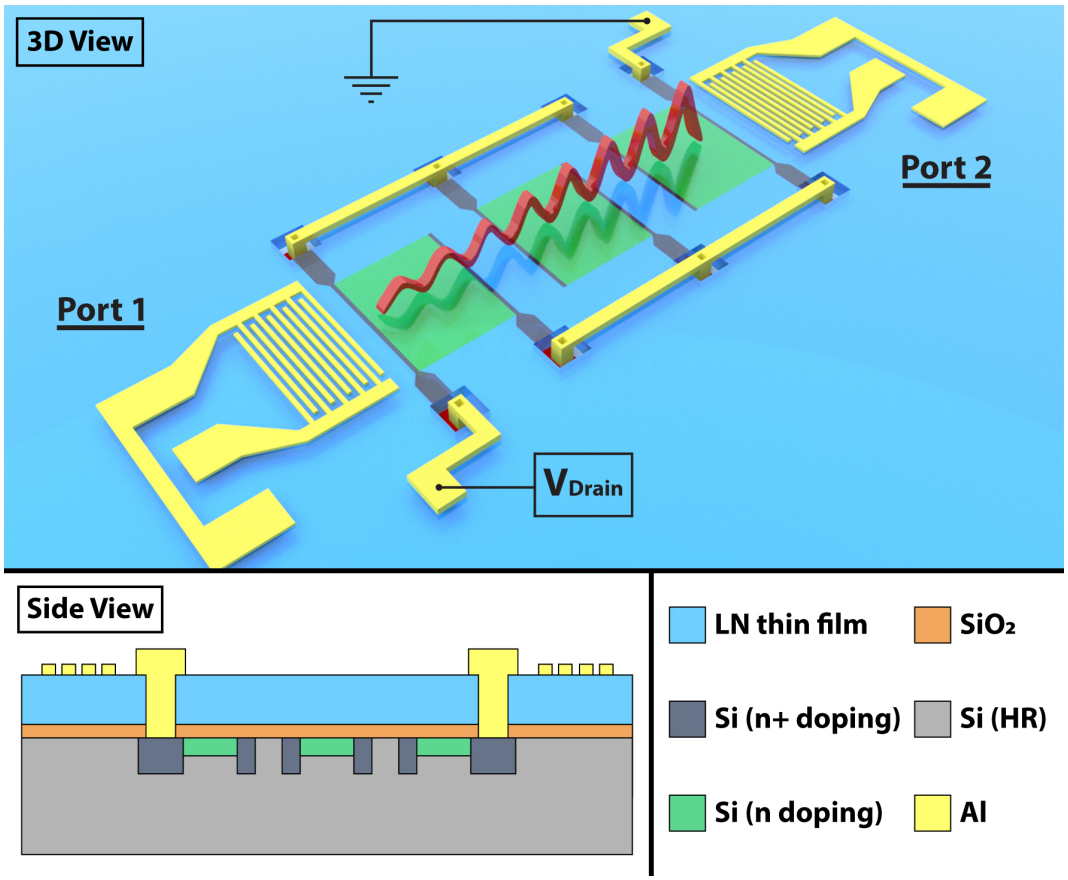

Figure 4.7. Illustration of an AE delayline amplifier on a doped LNOSi platform. A drift field is applied through the doped Si channel in the propagation path of the delayline, causing amplification of the acoustic wave (red curve).

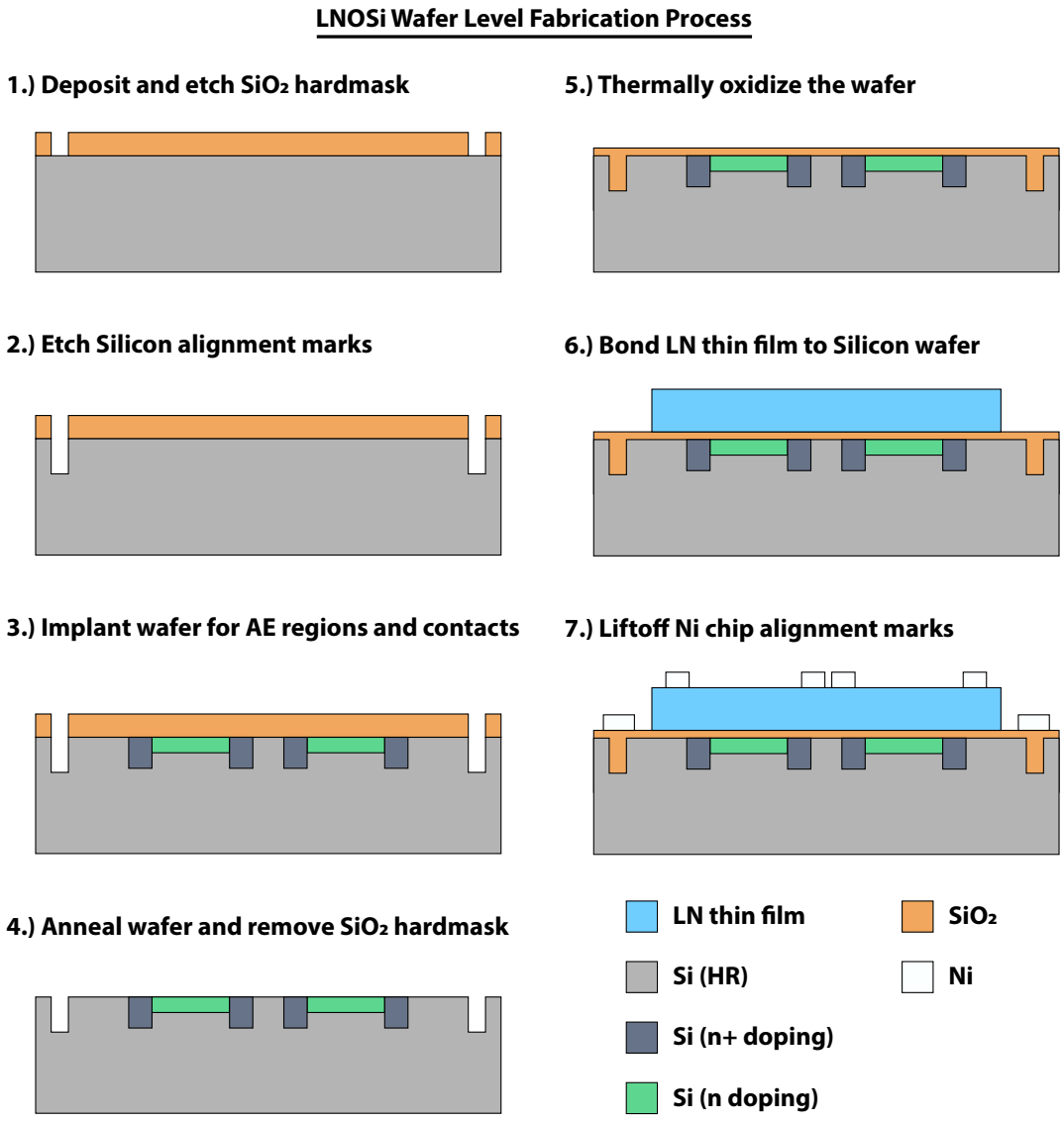

Figure 4.8. Wafer level fabrication process flow for the doped LNOSi AE devices.

doped regions, allowing for selective patterning of the AE regions. This section will detail the full fabrication process and initial measurements and results.

4.2.1 Fabrication and Measurement

The fabrication process is broken up into two sections: wafer level and chip level fabrication. Figure 4.8 outlines the wafer level fabrication process. The first step is to etch wafer alignment marks into the HR Silicon wafer with Reactive Ion Etching (RIE). Then, a 10-20 nm

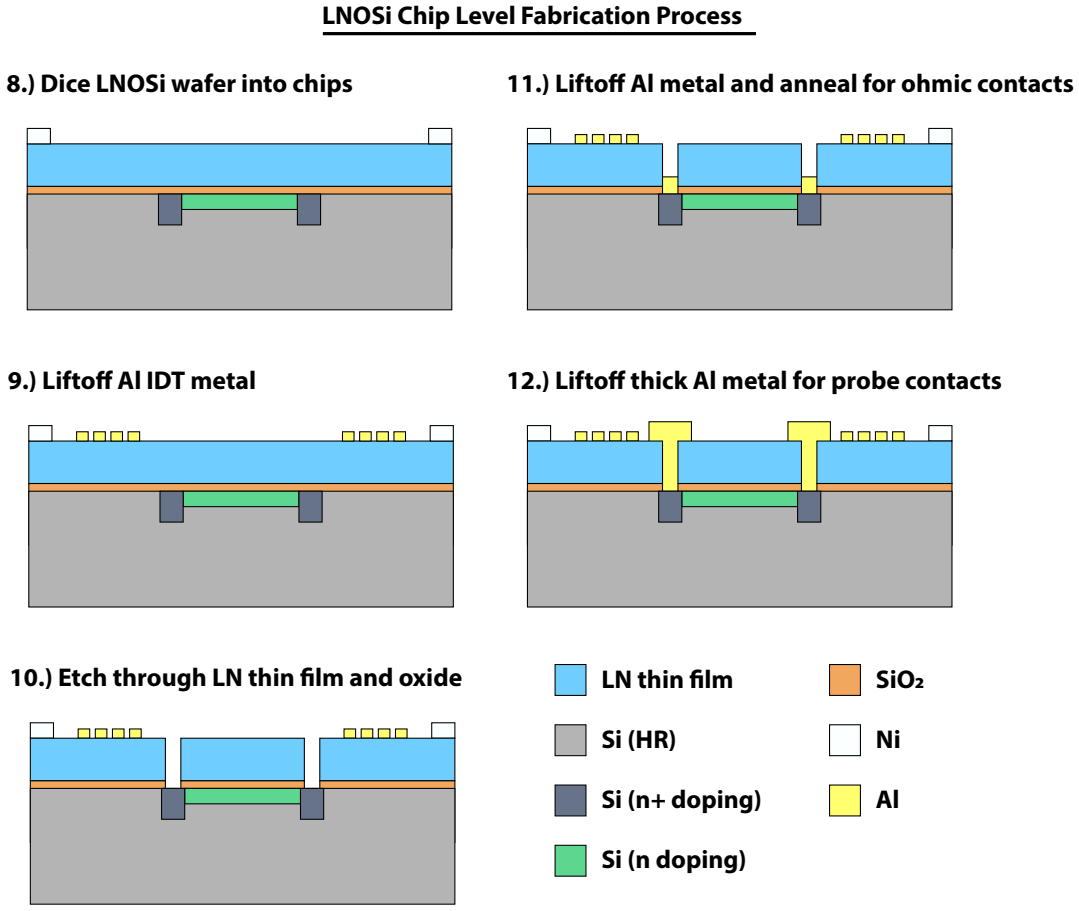

Figure 4.9. Chip level fabrication process flow for the doped LNOSi AE devices.

SiO_2 hardmask is deposited to protect the substrate from implantation damage during the two implantation steps. The third step is to implant the Ohmic contact and AE regions with Phosphorus ions, followed by an anneal at 800° C for 30 min. The fourth step is to remove the oxide hardmask with RIE. The fifth step is to thermally oxidize the wafer (15 nm) to create a buffer for the LN bonding process. Step 6 is to bond the 128° Y-cut LN thin film with the doped HR Silicon wafer. This bonding process was performed by Partow Technologies, LLC [27]. Finally, step 7 is to lift off Nickel (Ni) chip level alignment marks so further processing can be performed after dicing the wafer. Ni was chosen as the alignment mark metal because it was the heaviest metal (by atomic number) that could be detected in the e-beam lithography tool and allowed in the etching tools at the Scifres Nanofabrication Lab.

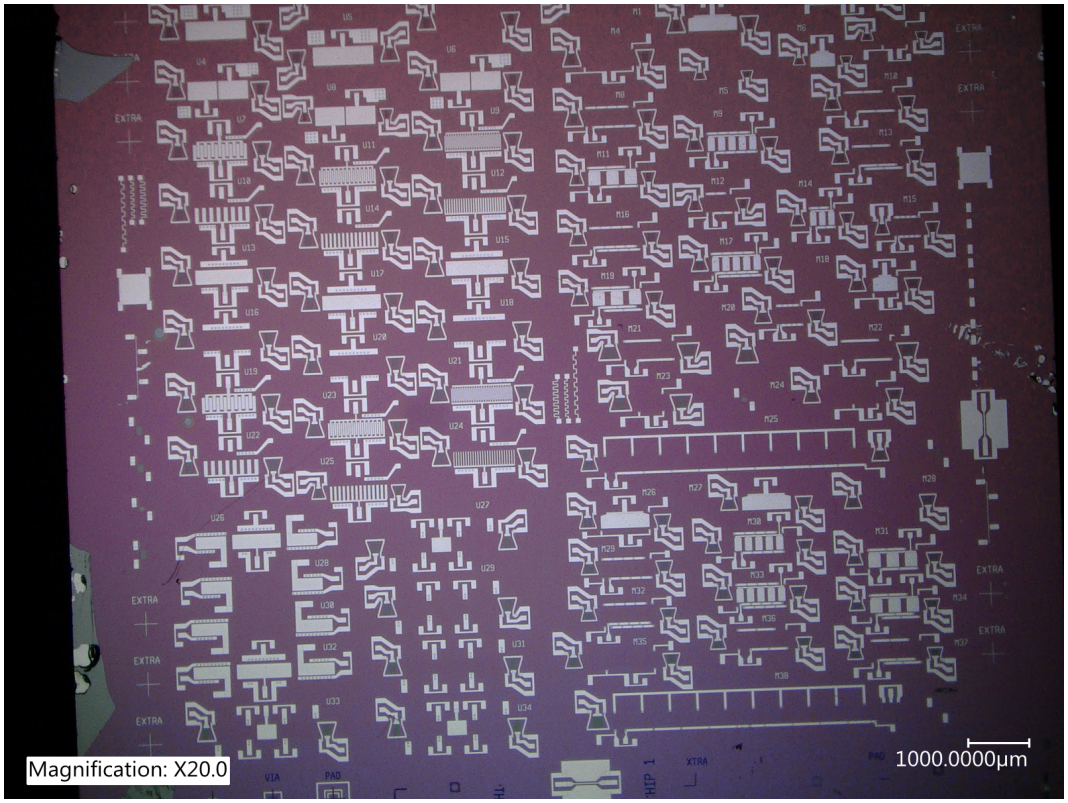

Figure 4.10. Optical image of the fully fabricated doped LNOSi AE chip.

Figure 4.9 details the chip level fabrication process for the doped LNOSi AE delaylines. Step 8 is to dice the wafer into chips for further processing. Step 9 uses PMMA A6 resist to define the IDTs using e-beam lithography. Aluminum (Al) metal was deposited (100 nm) and patterned using liftoff. The next step used the ion mill to etch vias for the highly doped Ohmic contact regions in the Silicon underneath the LN thin film. Since all of the device metal is Al in this process (IDTs, Ohmic contacts, and prove pad metal), the entire chip needs to be protected by photoresist during the Buffered Oxide Etch (BOE) to strip the native oxide off of the Silicon in the vias. Therefore, an intermediate Ohmic contact Al deposition step is added before the thick pad metal. During step 11, everything is protected by photoresist except for the etched vias. A quick BOE dip is performed followed by liftoff of Al metal and anneal in forming gas to create Ohmic contact to the doped silicon regions. The final step is to pattern and liftoff the Al pad metal for DC and RF probes.

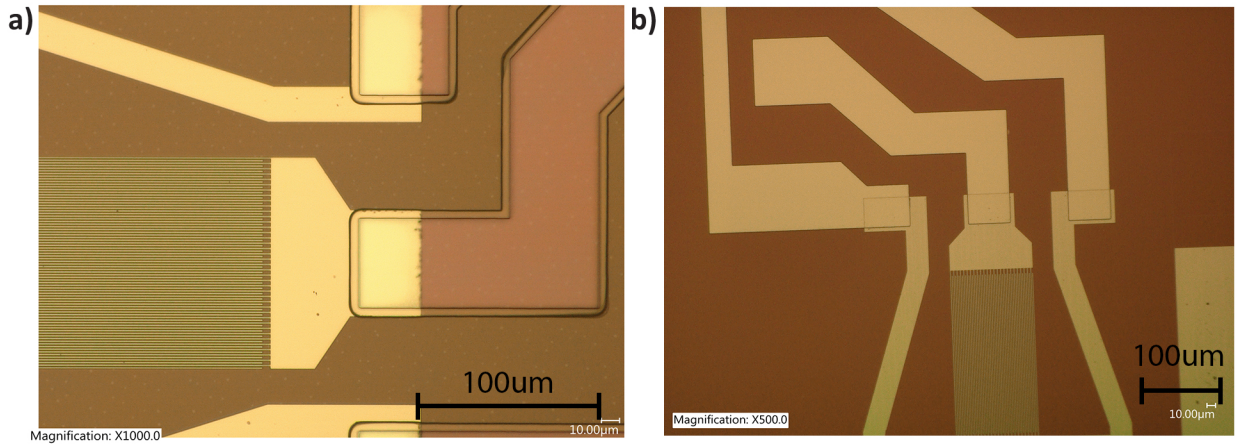

Figure 4.11. Optical images of the thick Al metal liftoff process using a LOR 30B and AZ 1518 bi-layer. Image (a) is of bi-layer resist after development and (b) is after 750 nm of Al deposited and resist removal.

Figure 4.10 is an optical image of the completed doped Silicon AE chip. One of the challenging aspects in the fabrication was the development of the Al Ohmic and pad metal liftoff steps. Since the ion mill etch for silicon vias was 700 nm deep, a very thick Al metal deposition and liftoff was needed to have sufficient sidewall coverage and uniformity over the large LN etch step height. A thick bi-layer liftoff process was chosen using a combination of LOR 30B and AZ 1518 photoresists. Figure 4.11 (a) is an optical image of the bi-layer process after development. It shows a uniform 5 μm undercut in the LOR 30B layer to allow for a clean liftoff of 750 nm of Al. Figure 4.11 (b) shows the resulting thick Al pad metal pattern after a clean liftoff with the bi-layer process.

A large part of the fabrication development was in the ion mill etch step to form the vias to the highly doped Silicon regions underneath the LN thin film. While LN has been dry etched using RIE with SF_6 gas [99], the most widely used dry chemical etching process is RIE using a BCl_3/Cl_2 gas mixture [100]. Variations of this RIE recipe have been used to make not only released LN Lamb mode resonators [101], but also Lamb mode delaylines [102, 103] and even optical ring resonators [104]. Ion milling with Ar gas is a purely physical etching process and has shown very promising results for making high quality factor resonators [105, 106] and delaylines [107] on suspended LN thin films. Since a similar etch is needed

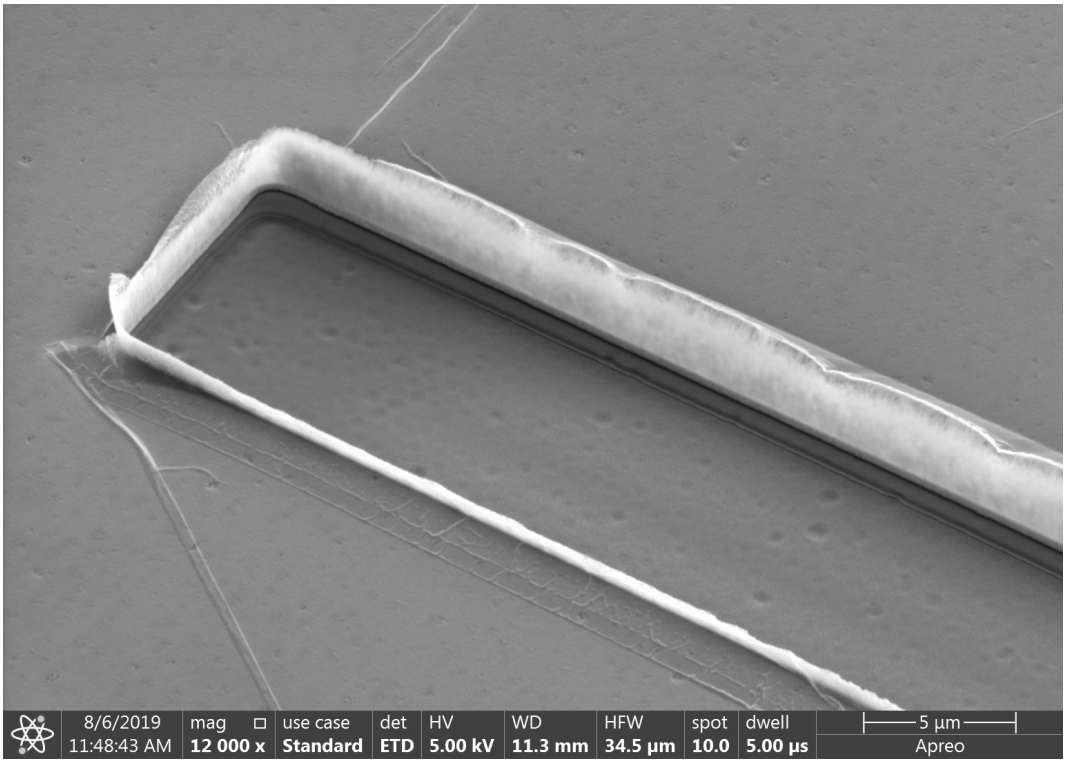

Figure 4.12. SEM of an ion mill vias etch without a sufficient cleaning step or UV curing, resulting in large sidewall accumulation still present after resist removal.

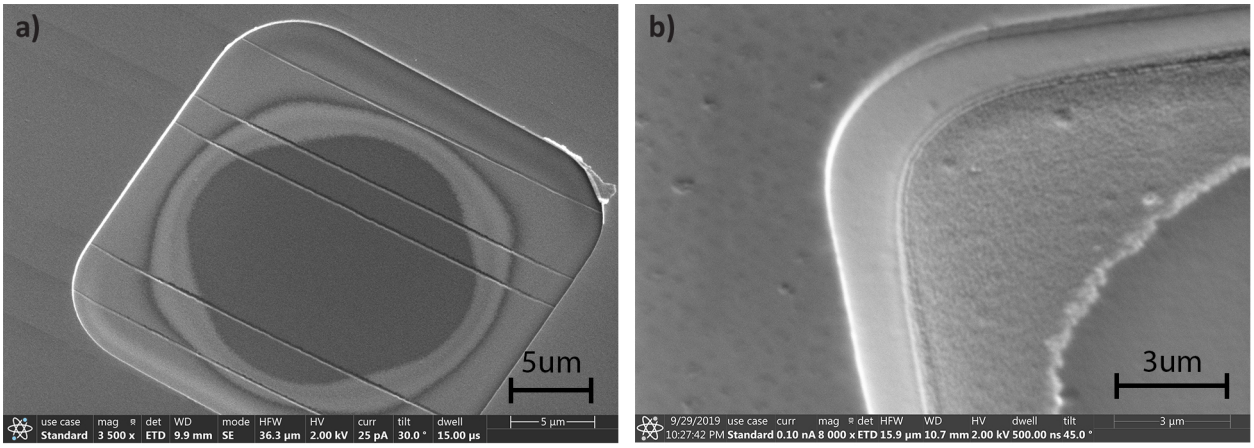

Figure 4.13. SEM (a) of the final via etch profile and (b) shows an zoomed SEM of the corner of the via. The light grey is the LN thin film while the dark grey circle in the middle of the via is the underlying highly doped Silicon layer.

for producing released AE delaylines and AE resonators on the LNOSOI platform in the future, the LNOSOI through etch and LNOSi vias etch using the ion mill were developed concurrently. Figure 4.12 shows an SEM of an initial attempt at the vias etch using a similar milling recipe as [32]. This recipe used a -14° etch angle and had only 25% of the total etch time at -70° etch angle for cleaning the sidewalls of resputtered LN and resist. There was still significant resputtered material left on the sidewalls even after resist removal and sonication. Also, Figure 4.12 shows a thin layer of burnt resist on the surface. LN requires very high accelerating voltages to physically etch, so with 600 V the photoresist is prone to burning from the heat generated during milling. There is an additional problem of trenching present near the edges of the vias etch window. Trenching occurs when a steep enough ion mill etch angle is used and the accelerated ion reflect off of the sidewall and etch additional material near the edges of the pattern [108]. This is a serious problem for a Silicon via because the trenches will penetrate deeper than the doping and make electrical contact to the Silicon substrate. The final via etch profile was achieved by implementing a UV curing step after the photoresist development, increasing the ion mill etch angle to -22°, and increasing the cleaning angle step to 33% of the total etch time. Figure 4.13 shows an SEM of the via etch profile. The change to a -22° etch angle resulted in a rounding of the etch profile (with no trenching). Due to this rounding, the underlying Silicon was not exposed over the entire

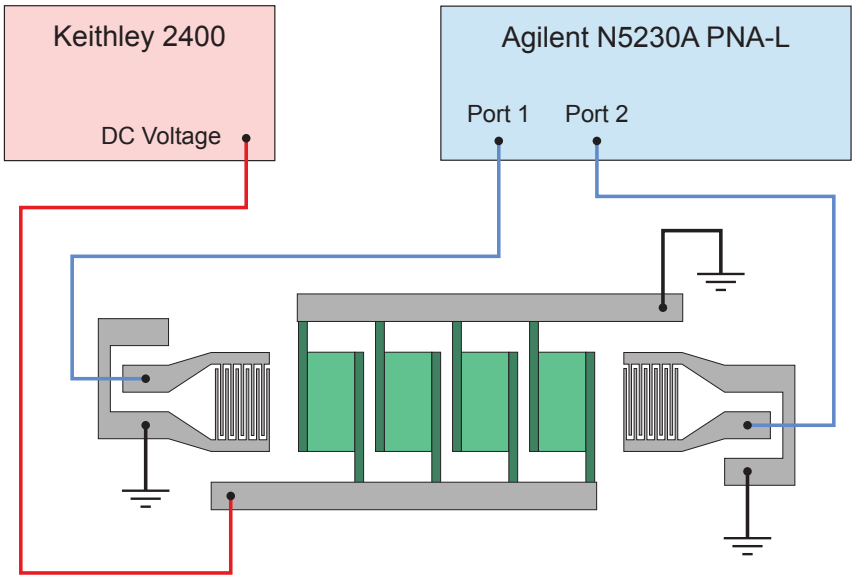

Figure 4.14. Illustration of the experimental setup for measuring AE delay-lines on the doped LNOSi platform.

patterend via. The via is a 25 μm x 25 μm square, but the exposed Silicon (dark grey color in Figure 4.13) is only the middle 17 μm diameter circle. Also, the addition of the UV curing step before ion milling and sonication during resist removal got rid of all the burnt photoresist on the LN surface.

Figure 4.14 shows an illustration of the experimental setup used to measure the S-parameters of the AE delaylines with the application of a drift field. A network analyzer is used to measure the S-parameters of the 2-Port A delayline. One DC bus bar is connected to ground while the other bus bar is connected to a Source Measure Unit (SMU) and a DC voltage is applied during the network analyzer frequency sweep. The following subsection will discuss the initial results of the fabricated AE delayline and some of the major challenges with the current fabrication process.

4.2.2 Results and Discussion

Figure 4.15 shows an optical image of the measured segmented AE delayline on the doped LNOSi platform. The performance of this AE amplifier was limited by several issues during

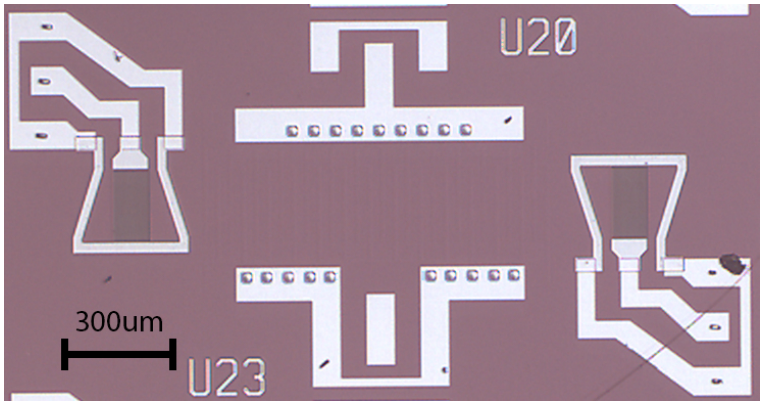

Figure 4.15. Optical image of the measured doped LNOSi segmented AE amplifier.

the fabrication process. The first challenge in the fabrication is developing a doping profile and making good contact to the highly doped Silicon regions without generating significant substrate current. The ion mill vias etch went 130 nm into the doped Silicon substrate, leading to enough contact with the underlying HR substrate to have significant substrate current. Initial current-voltage (IV) measurements were performed with a grounded and floating chuck on the measurement setup. There was the same order of magnitude current in both cases, meaning the substrate current path is just as favored as the doped Si regions. This large current path through the substrate increases the distance between drifting free carriers and the SAW mode, resulting in a lower spatial overlap and lower AE interaction strength. This contact issue can be resolved through further optimization of the implantation doping profile and ion mill etching recipe.

The second major challenge is the successful bonding of the 128° Y-cut LN thin film to the doped Silicon HR wafer. The alignment mark etch, implantation process, anneal, and thermal oxidation of the HR Silicon wafer all contributed to additional stress and roughness that can cause problems during the bonding process. As a result, the wafer shattered after the bonding process. The wafer pieces were then Chemical-Mechanical Polished (CMP), but periodic cracks in the surface of the LN thin film were present upon receiving the polished pieces. Figure 4.16 shows an SEM of a cleaved LNOSi piece, revealing the side profile and cracking present at the surface. These cracks have a periodicity of about 4 μm and the cracking is present throughout the LN thin film as seen in the via etch profile in Figure 4.13 (a).

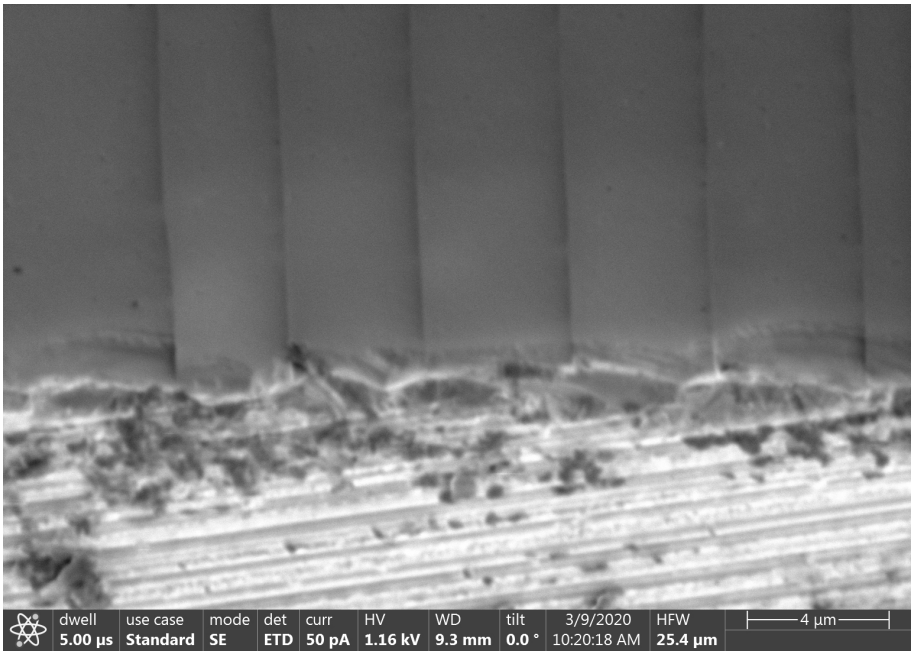

Figure 4.16. SEM of the LNOSi surface showing the periodic cracks in the LN thin film.

A periodic cracked piezoelectric thin film perpendicular to the propagation direction of the acoustic wave will severely degrade the mechanical response of the device. The cracks in the film will create strong reflection points along the propagation path, significantly increase the propagation losses (IL), and reduce the effective k^2 of the SAW mode. The measured S-parameters under no DC biasing are shown in Figure 4.17. The S_{11} response shows the presence of two acoustic modes close to one another at 1.035 GHz and 1.050 GHz. The first mode is the Rayleigh SAW mode, which should have a high piezoelectric coupling coefficient ($k^2 = 5\%$) and the second mode is a shearing SAW mode with a very small k^2. Figure 4.17 (a) shows the S_{21} response of the delayline and the Rayleigh SAW mode has significant IL (-55 dB) compared to the shearing SAW mode (-40 dB). This large insertion loss and roughening of the Rayleigh SAW mode's transmission peak is a direct result from the cracking at the surface. This large loss coupled with a reduced k^2 makes it difficult to detect a small non-reciprocal change in the insertion loss with an applied DC bias across the device.

In order to measure a change in the peak amplitude of the Rayleigh SAW mode, time gating is needed to filter out all of the acoustic reflections from triple transit and reflections

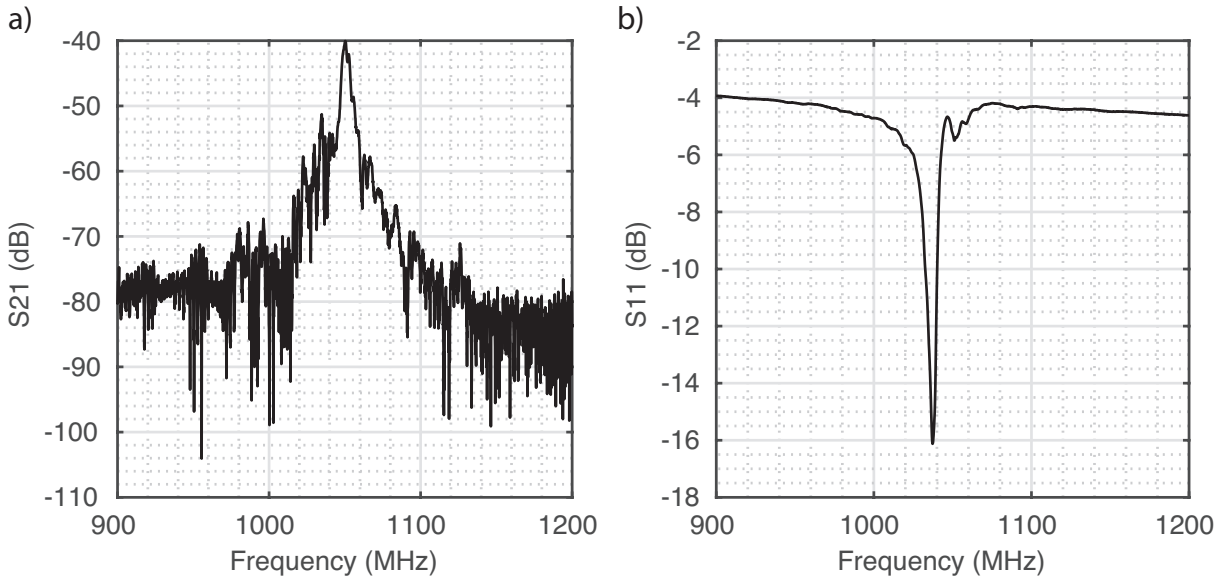

Figure 4.17. Measured (a) S_{21} and (b) S_{11} response of the doped LNOSi delayline with no DC bias.

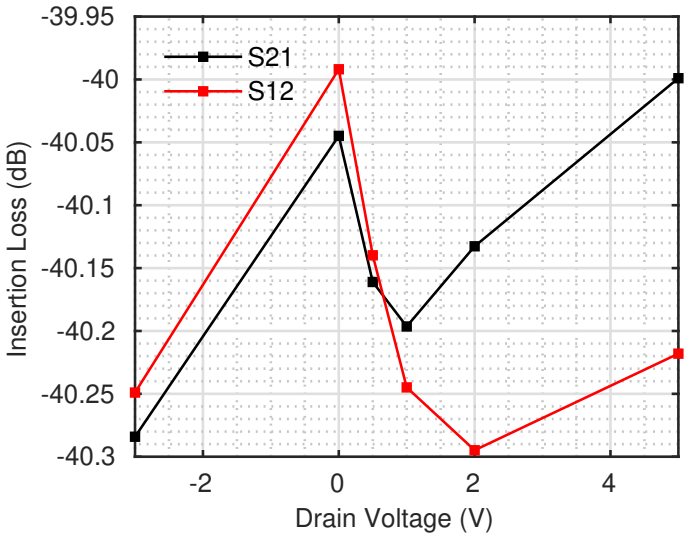

Figure 4.18. Measured non-reciprocal change in the insertion loss as a function of applied drain voltage for a segmented doped LNOSi AE delayline.

off of each crack in the LN during wave propagation. For each DC voltage applied, the S_{21} response is time gated and the Rayleigh SAW mode's peak value is recorded. Figure 4.18 shows the measured insertion loss of both the forward (S_{21}) and backward (S_{12}) acoustic Rayleigh waves as a function of drain voltage applied. There is a potential non-reciprocity of 0.2 dB observed between the forward and backward waves, but no amplification was achieved. This possible non-reciprocity was limited by trapped charges from bonding, substrate current effects, large reflections, and large propagation losses from cracking in the LN thin film. Recent work on a LNOSOI material platform has improved the non-reciprocal response by implementing a symmetric DC biasing scheme to compensate for trapped charge effects [24]. This biasing scheme could be implemented in this measurement setup, but the major limiting factor in Figure 4.18 is the failed bonding process and substrate current effects. The fabrication process developed for this doped LNOSi platform could be used for fabricating similar devices on a doped LNOSOI platform to take advantage of the high k^2 S_0 and SH_0 Lamb modes.

5. INDIUM GALLIUM ARSENIDE ACOUSTOELECTRICS

The 41° Y-cut LN material platform has gained a lot of interest for RF MEMS devices for its X-propagating Leaky SAW (LSAW) mode. This LSAW has an acoustic velocity (4300 m/s) larger than most Rayleigh SAW modes, a very high piezoelectric coupling coefficient ($k^2 = 17$ %), and very low propagation losses [25]. Early work in AE delayline amplifiers utilizing Indium-based semiconductor layers showed large electronic gains and even terminal gain [109]. Terminal gain was also achieved in pulsed operation with a LN LSAW mode using a Si semiconductor [13]. Sandia has published work on an epitaxial InGaAs thin semiconductor film bonded to Y-cut LN wafers for delayline amplifiers utilizing both the Rayleigh SAW and LSAW modes [110–112]. Their most recent work combines all of these efforts by achieving a large terminal gain using a InGaAs thin film bonded to a 41° Y-cut LN wafer [26], which is the same material platform (InGaAs-LN) used in this thesis. The first part of this chapter gives an overview of the fabrication process performed at Sandia, followed by the pulsed measurement setup. Then the segmented AE amplifier design and results are presented along with several other AE device designs.

5.1 Fabrication and Measurement Setup

The fabrication of the InGaAs-LN wafer was performed at Sandia National Labs. The fabrication subsection gives a brief overview of each step in the fabrication process. Then, the pulsed measurement setup is outlined. This includes the hardware setup, triggering, timing sequences, and data extraction from the raw pulse.

5.1.1 Fabrication Process

Figure 5.1 illustrates each step of the Sandia InGaAs-LN fabrication process flow. More details about the fabrication process can be found in [112]. Step 1 starts with an epitaxial growth of an InGaAs heterostructure on an InP wafer. The heterostructure on top of the InP wafer consists of a non-intentional doped (NID) InP buffer layer, (NID) InGaAs etch stop layer, (1 x 10^{18} cm^{-3}) InP etch stop layer, (2 x 10^{19} cm^{-3}) InGaAs layer, (1 x 10^{18} cm^{-3}) InP

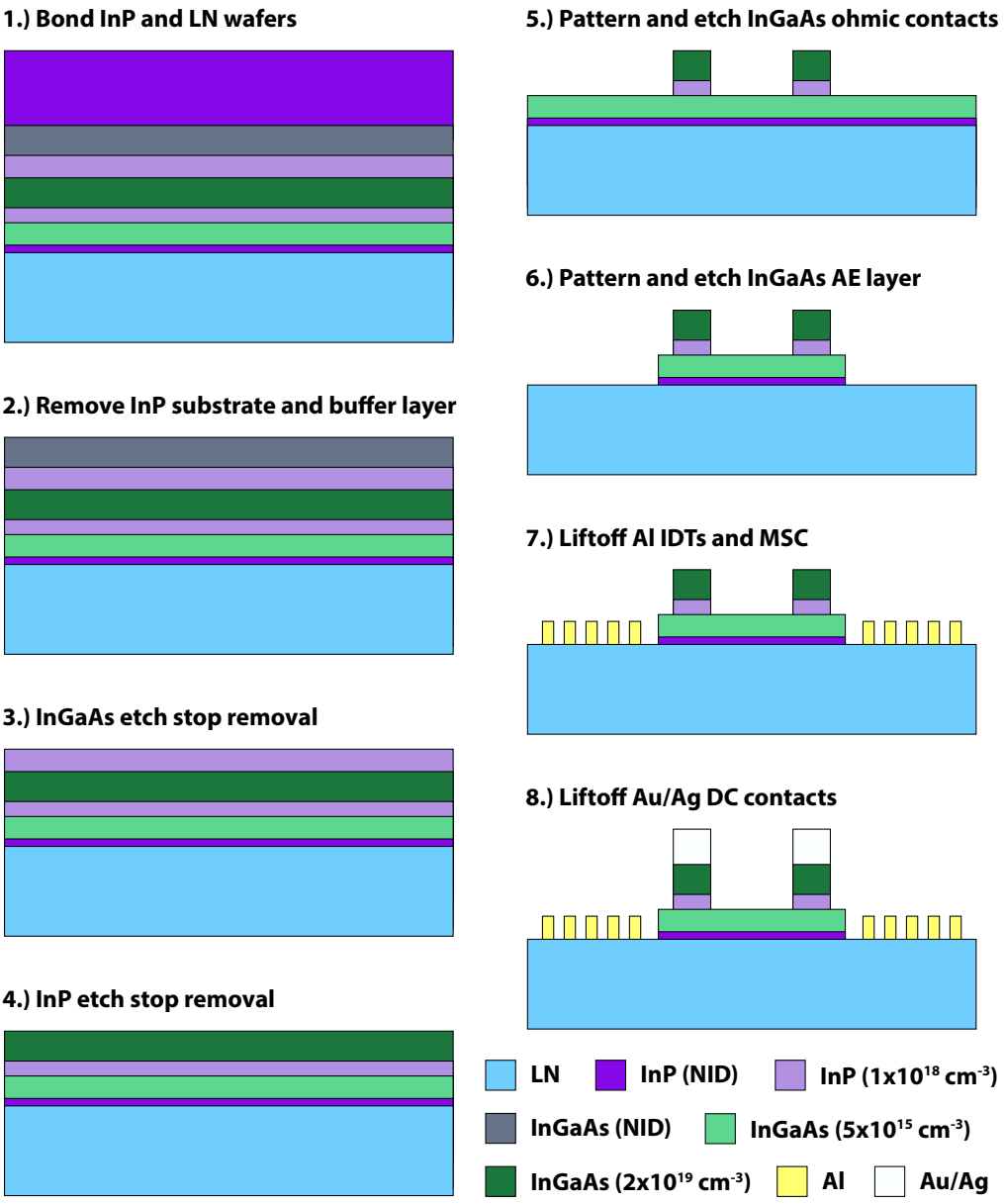

Figure 5.1. Fabrication process flow for the Sandia InGaAs-LN AE platform.

layer, (5 x 10^{15} cm^{-3}) InGaAs layer, and finally a (NID) InP capping layer. This InP wafer is then bonded to a 41° Y-cut LN wafer. The second step etches through the InP wafer handle and InP buffer layer, stopping at the first InGaAs etch stop. Step 3 then removes the first InGaAs etch stop layer. Step 4 removes the last InP etch stop layer. Step 5 lithographically patterns and etches both the InGaAs and InP contact layers. These two layers form the Ohmic contacts to the AE regions of InGaAs. Step 6 lithographically patterns and etches the remaining InGaAs layer and InP capping layer. These last two layers form the AE regions with an optimal carrier concentration for acoustic devices operating in the MHz frequency range. Step 7 uses photolithography to pattern and liftoff Aluminum (Al) IDTs. Finally, step 8 uses photolithography to pattern and liftoff a gold/silver (Au/Ag) metal stack for Ohmic contact to the (2 x 10^{19} cm^{-3}) InGaAs layer. This Au/Ag metal stack is also used to land DC probes and make contact to the source and drain of the AE devices.

5.1.2 Pulsed Voltage Measurement Setup

Due to the poor heat dissipation of the LN wafer, the heating effects under continuous operation could cause drift and damage the InGaAs carrier layer [26]. Therefore, the S-parameter and IV measurements were all taken in pulsed mode operation. Figure 5.2 shows a schematic of the pulsed measurement setup along with illustrated plots showing the triggering and timing sequences. The first step is to calibrate the PNA-L in continuous wave (CW) time mode. Instead of sweeping over a frequency range while measuring the S-parameters, CW time mode records the data at a single frequency, recording the single frequency data at the same sampling rate as in the frequency sweep mode. The sampling rate is determined by the Intermediate Frequency Band Width (IFBW). The PNA-L applies filtering at each frequency measured, and the IFBW sets both the dynamic range and settling time of the measurement. This trade-off needs to be carefully considered when choosing an IFBW. As the IFBW is increased, the settling time reduces, but the dynamic range of the measurement decreases. This decrease in dynamic range limits the possible signal level that can be measured. The voltage pulse width in these experiments is 2 ms, which means the settling time for each measurement point using the PNA-L needs to be < 0.1 ms in order to capture enough points

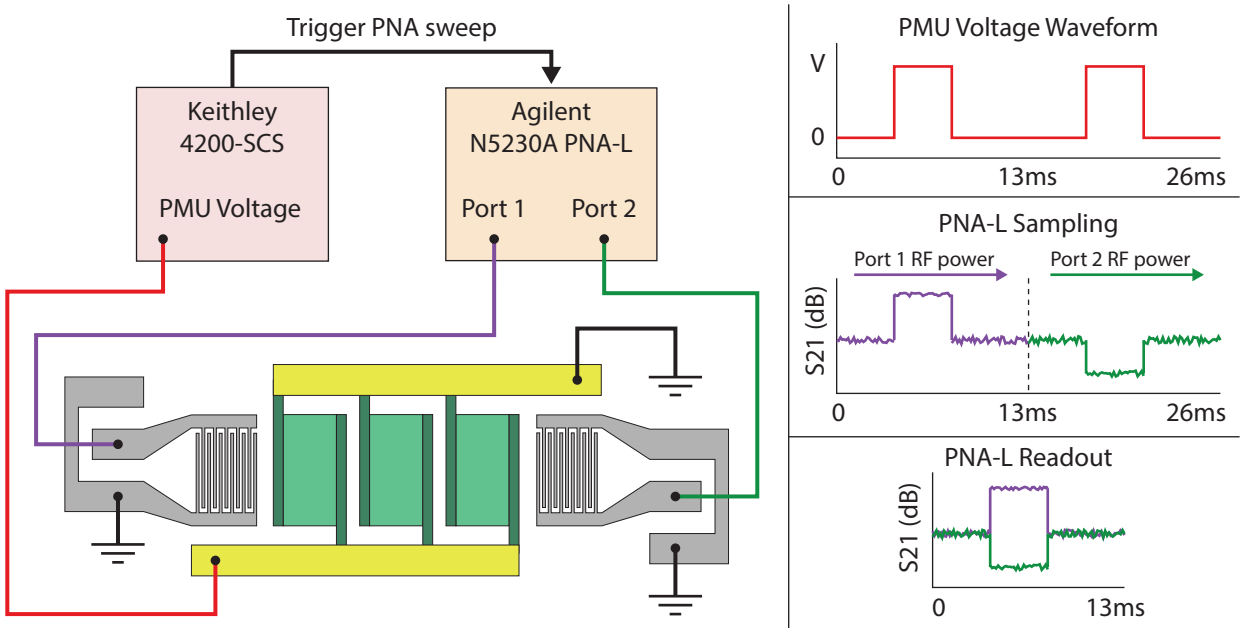

Figure 5.2. (left) Illustration of the pulse measurement setup with the PNA-L and Keithley 4200-SCS. (right) The illustrated plots show the triggering and timing sequence for measuring the S-parameters with an applied voltage pulse.

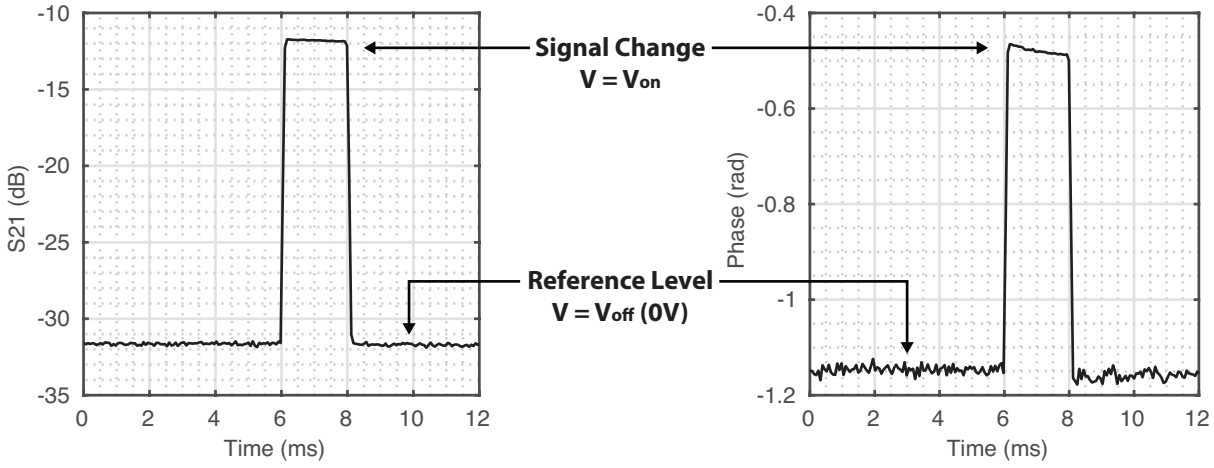

Figure 5.3. S_{21} measurement using CW Time mode displayed (a) in dB and (b) in phase with a DC voltage pulse applied. The definitions for signal change and reference level are shown.

during the pulse to extract reliable data. This leads to an IFBW of 15 kHz with the Agilent N5230A PNA-L used in these experiments. The number of points chosen for the sweep (201) is enough to capture and average the data before, during, and after the applied voltage pulse. This led to a total sweep time of 13 ms with the network analyzer in CW time mode.

Now that the sweep is set up in the PNA-L, a full 2-Port Short Open Load Thru (SOLT) calibration is performed and saved on the network analyzer. Once the calibration is completed, each calibrated measurement actually takes 26 ms instead of 13 ms. The PNA-L does a full sweep with only Port 1 RF excitation, then does a second sweep with Port 2 RF excitation and uses both sets of sweep data to compute the correction coefficients to be applied to the raw data. Since each calibrated measurement requires two sweeps, the voltage pulse waveform output from the Keithley 4200-SCS is actually a pulse train with 2 of the same voltage pulse. This voltage pulse waveform is illustrated by the red curve in Figure 5.2. The Keithley 4200-SCS also sends a trigger signal to the PNA-L when it generates the voltage waveform. This trigger starts the calibrated CW Time sweep on the PNA-L. The first half of the sweep with Port 1 excitation sees the first voltage pulse and the second half of the sweep with Port 2 excitation sees the second voltage pulse. An illustration for a PNA-L sampling waveform is shown in the second plot of Figure 5.2. The correction coefficients are

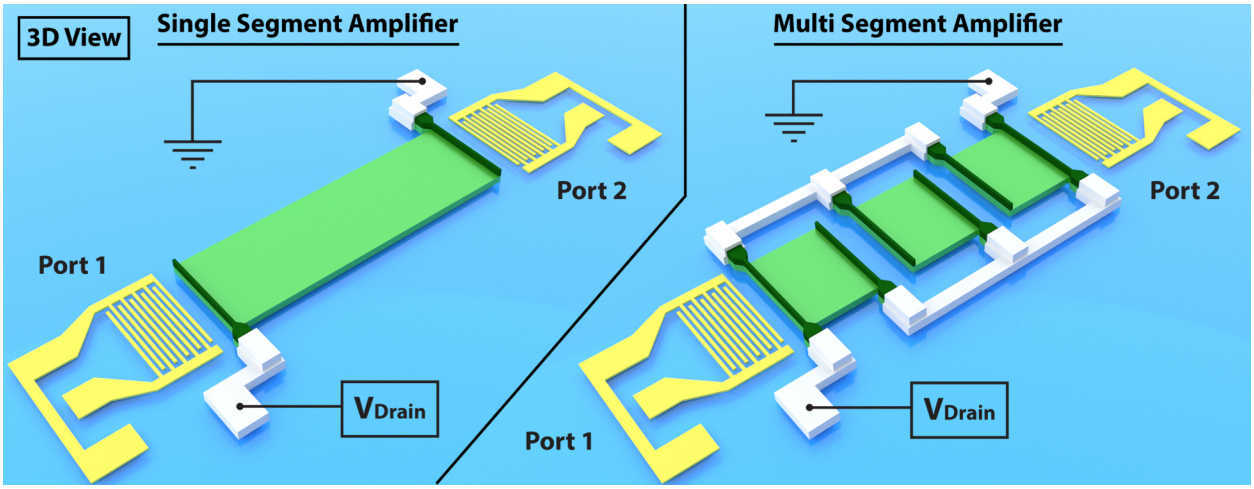

Figure 5.4. Illustration showing the single and multi segmented delayline amplifier on the InGaAs-LN platform.

then applied to both sweeps and displayed as a single sweep on the PNA-L. An illustration of this final displayed sweep is shown in the last plot of Figure 5.2.

An example calibrated S-parameter measurement is shown in Figure 5.3. For either insertion loss or phase measurements, the reference level for the measurement is defined as the signal level averaged over the entire time the voltage waveform is off (V_{off}), which is 0 V. The signal change is defined as the signal level averaged over the entire time the voltage pulse is on (V_{on}). The relative change in a signal is then defined as the signal change minus the reference level for each measured sweep.

5.2 Segmented Acoustoelectric Amplifier Design

A lot of work has been done on the SAW delayline amplifier using a single AE gain element. When that single gain element is segmented and connected in parallel, it provides a trade-off in input power consumption: decreasing the input voltage by increasing the current. By making the segments shorter, a smaller voltage is required to achieve the same drift field. All of these gain elements produce a current with the application of the drift field, and since they are all electrically connected in parallel the total current scales with the number of gain segments. Figure 5.4 shows an illustration comparing the structure of a single-segment and multi-segment delayline amplifier. Assuming the unit length of an AE gain segment

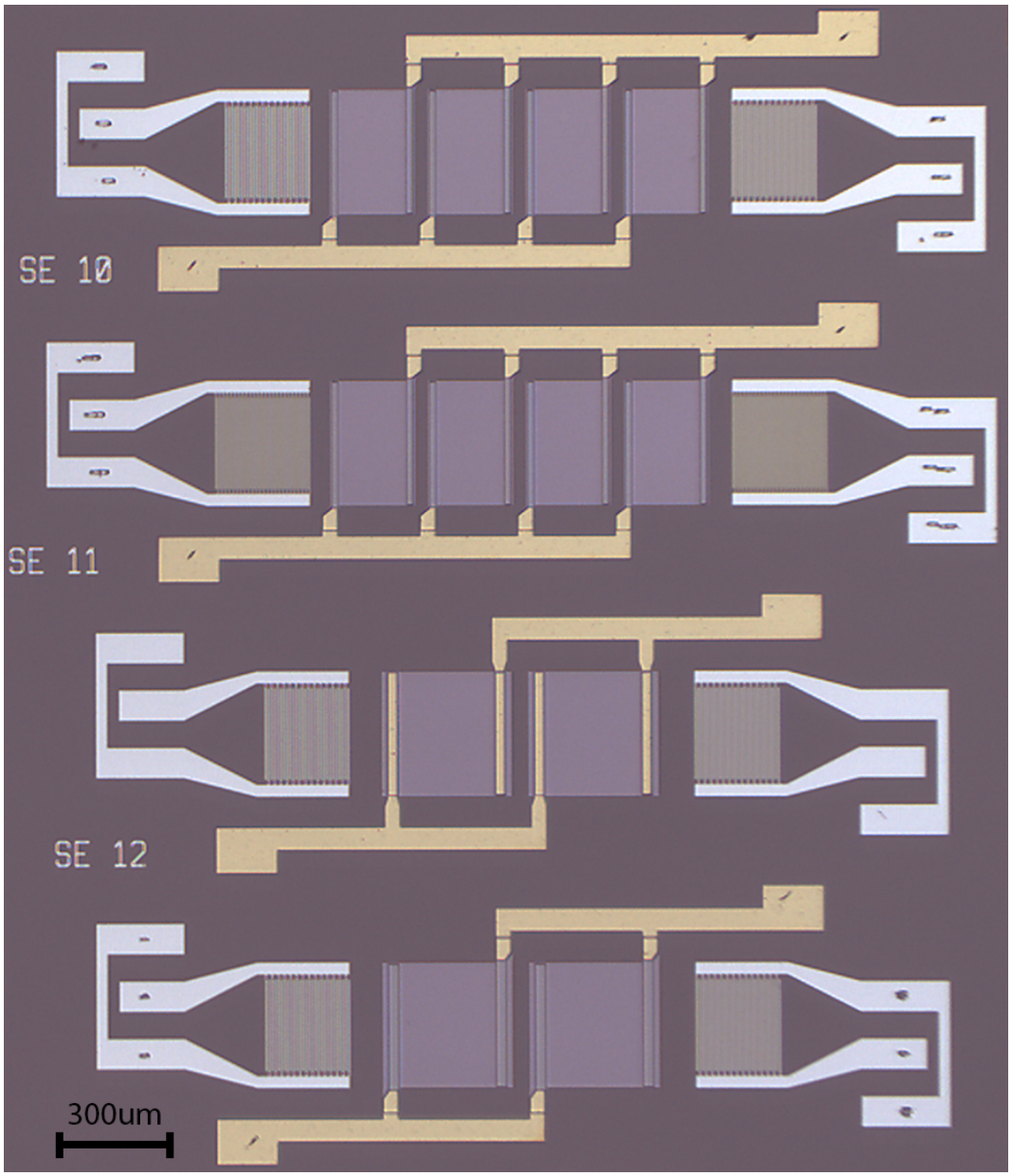

Figure 5.5. Optical microscope image showing the different parameters being investigated for segmented AE delaylines on the Sandia InGaAs-LN AE platform. This includes the AE segment unit length, number of segments, operating acoustic frequency, and type of Ohmic contact.

is fixed, one key difference between a single and multi-segment delayline amplifier is the relative operating point on the AE gain curve. In order to reach the same net gain, a much large drift field needs to be applied to the single-segment amplifier, which could have a different gain slope at that point. Some work has been done on integrated multi-segment AE delaylines [113], but it doesn't look at how the AE gain or input DC power scales with segmentation.

The operating acoustic frequency is another aspect of scaling to consider. Since the acoustic frequency of the AE delaylines are lithographically defined, A single InGaAs-LN wafer can have a range of devices with varying operating frequencies. In Chapter 3, the maximum AE gain for the InGaAs-LN platform as a function of carrier density was discussed. While the optimum carrier density was roughly the same over a range of 100 MHz to 1 GHz, the maximum possible AE gain increased with frequency [114].

The last performance comparison is specific to the InGaAs-LN platform. The Au/Ag Ohmic pad metal is acoustically very thick, which introduces large acoustic losses when the metal is lithographically defined within the propagation path. One solution is to have the Au/Ag metal stack make Ohmic contact with the heavily doped (N+) InGaAs outside of the propagation path and use the N+ InGaAs layer itself to distribute the voltage across the width of the delayline. In summation, this section will look at the performance of segmented AE delaylines as they scale with the segment unit length (100 μm, 175 μm, 250 μm), number of segments (x1, x2, x3, x4, x5), operating acoustic frequency (270 MHz, 440 MHz), and type of Ohmic contact (Au, N+).

Figure 5.5 shows four example segmented AE delaylines with different combinations of the parameters being investigated. The S-parameters of two different delaylines were measured (without any voltage bias), one with a 14 pair IDT and LSAW acoustic wavelength of 16 μm (270 MHz), and another with a 25 pair IDT and LSAW acoustic wavelength of 10 μm (440 MHz). The S-parameters of these two delaylines are shown in Figure 5.6. It is important to note that the 440 MHz LSAW mode has an additional 10 dB IL compared to the 270 MHz LSAW mode. The IDT transducer design (aperture, finger pairs, bus spacing, bus width, pad capacitance) was optimized for the 270 MHz mode at Sandia, so the additional IL found in the 440 MHz mode could be a result of impedance mismatch with the transduction of the

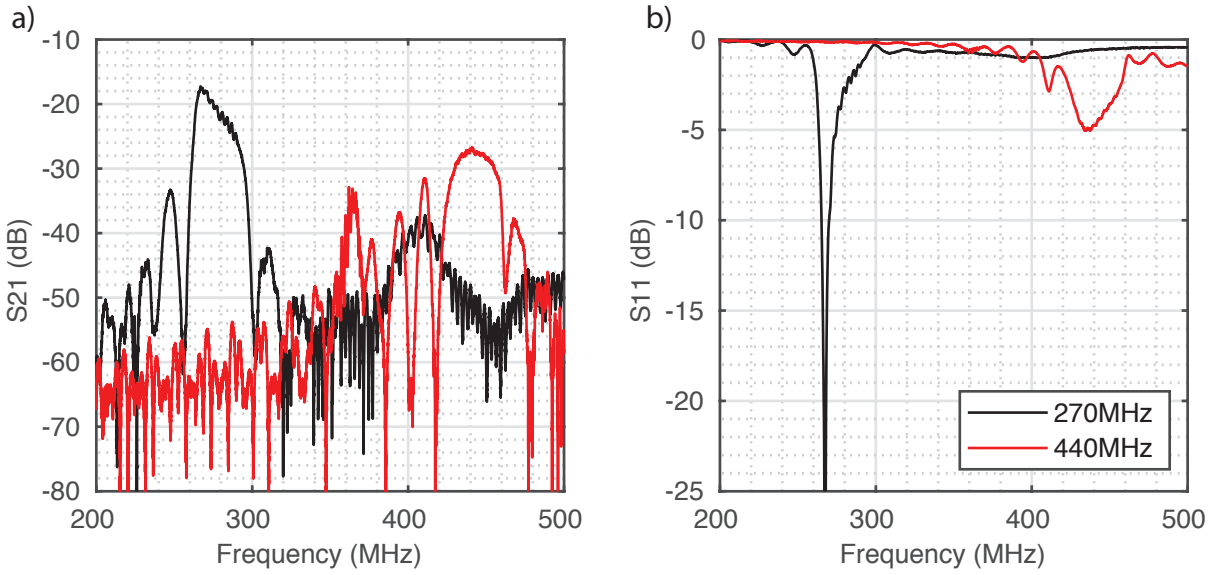

Figure 5.6. Measured S-parameters of a 270 MHz and 440 MHz acoustic delayline on the InGaAs-LN wafer with no voltage bias.

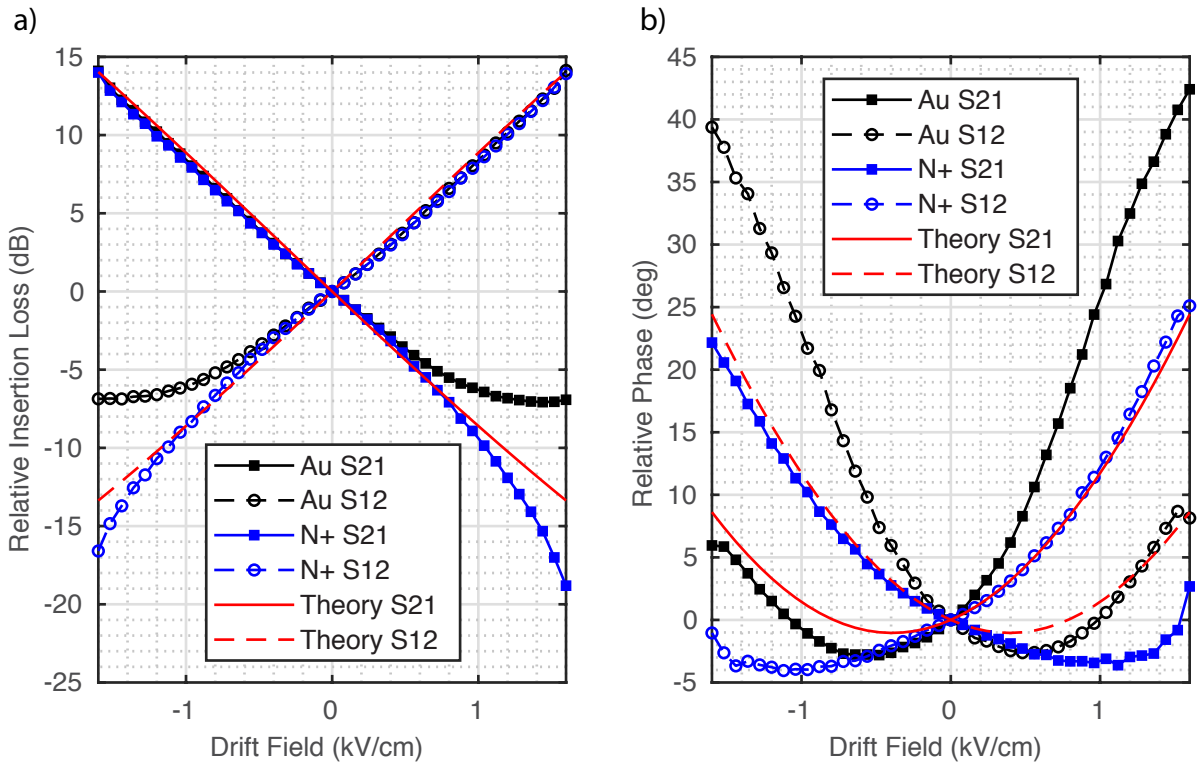

Figure 5.7. Measured relative (a) insertion loss and (b) phase comparing the AE performance of the Au and N+ contacts to fitted analytical theory.

mode. Further optimization of the IDT would have to be done for further reduction in the insertion loss. Because of this impedance mismatch in the 440 MHz mode, the rest of this section will compare the relative performance of all of these segmented AE amplifiers.

In order to compare the performance of the Ohmic contact types, single 250 μm segment AE delaylines operating at 270 MHz were measured with exactly the same geometric conditions except for having either the Au/Ag metal in the propagation path or just having the N+ InGaAs layer in the propagation path. Figure 5.7 shows the measured relative insertion loss and relative phase of the delaylines as a function of the applied voltage pulse (converted to a drift field value). There is no degradation in AE performance when opting for the N+ contacts over the Au contacts. Also both contact types show good agreement with the analytical AE theory using the normal mode theory for a Rayleigh wave amplifier discussed in Chapter 3. The theoretical curve was used to estimate the carrier concentration of the InGaAs AE regions (3.8 x 10^{16} cm^{-3}), which is higher than the carrier concentration

designed for (5 x 10^{15} cm^{-3}). This higher carrier concentration will alter the shape of the AE gain curves (as discussed in Chapter 3) and change the relative performance of the measured AE devices discussed later in this chapter. The big takeaway from the comparison in Figure 5.7 is that there is no loss in AE performance with using N+ Ohmic contacts. At no bias voltage, the delayline with Au contacts had an IL = -25.6 dB while the delayline with N+ contacts had an IL = -18.5 dB. By not using Au/Ag in the acoustic propagation path, the IL improved by 7 dB while maintaining the same level of AE performance. By using N+ contacts, a higher terminal gain can be achieved without any significant loss in AE performance. Therefore, the remainder of the AE segmented delayline comparisons will all have the N+ contacts to reduce the IL as much as possible.

5.2.1 Single vs. Segmented Gain Comparison

Figure 5.8 shows all the measured AE gain comparisons for varying AE segment unit lengths, acoustic frequencies, and number of segments. All of these measurements were taken at the same input RF power of -20 dBm. The measurements were plotted as a function of applied drift field in order to compare the relative performance between different unit lengths. The smaller unit lengths have the advantage of requiring a smaller applied voltage to reach the same drift field. As an example, if a 1 kV/cm drift field is desired, the 100 μm unit length requires 10 V, while the 175 μm and 250 μm unit lengths require 17.5 V and 25 V, respectively. When comparing the performance while holding the AE unit length constant, a couple clear trends emerge from Figure 5.8 (a-c). First, when looking at delaylines that operate at same acoustic frequency, as the number of segments is increased the gain slope increases and a larger AE gain is achievable with the same drift field applied. This scaling of adding segments to the amplifier for increased gain slope is a trade-off because of the increase the total current and therefore the total input power. The second thing to consider is the same number of segments with different acoustic frequencies. In almost all cases, the 440 MHz mode has a higher AE gain than the 270 MHz mode for all of the applied drift fields. This matches with the predicted trend in Chapter 3. For example, in the 175 μm unit length case with 2 segments at a drift field of -1 kV/cm, the relative AE gain goes from 18 dB for

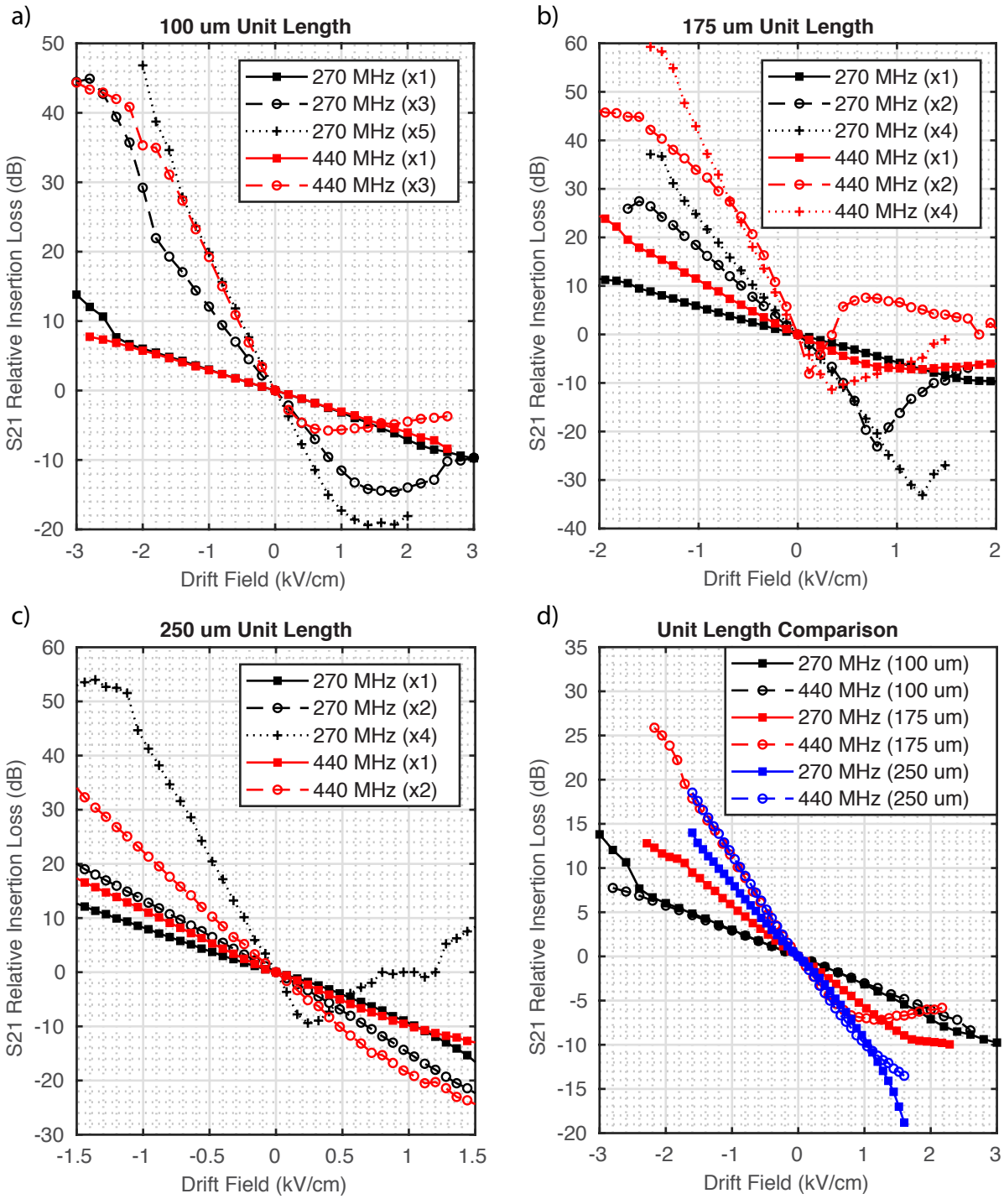

Figure 5.8. Measured S_{21} relative insertion loss as a function of drift field. (a) comparison of all AE delaylines with 100 μm unit length segments. (b) comparison of all AE delaylines with 175 μm unit length segments. (c) comparison of all AE delaylines with 250 μm unit length segments. (d) comparison of all AE delaylines with a single segment.

the 270 MHz mode to 33 dB for the 440 MHz. That is a x31 improvement just by doubling the operating acoustic frequency. The improvement is even more (x40) when looking at the delaylines with 4 segments. Finally, Figure 5.8 (d) compares the measured AE gain for single segment delaylines with varying segment unit lengths. The graph was plotted as a function of drift field instead of voltage to normalize the shape of the AE gain curve. Ideally, all three delaylines at the same acoustic frequency should have the same gain slope. None of the devices at 270 MHz (solid lines) and only two of the devices at 440 MHz (dashed lines) have the same gain slope. This discrepancy could be from slight carrier concentration variation between devices. Most of these measurements were performed in air at room temperature, so the shifts in the carrier concentration could be from adsorption of particles or moisture on the InGaAs surface. Performing future measurements in vacuum could help to reduce the variability in the carrier concentration between devices.

5.2.2 Gain vs. Input Power

With the trade off established between AE gain and input power as segments are added, this section will look into the rate of change of each to determine if either the AE gain or input power changes at a faster or slower rate. In order to make this comparison, the measured non-reciprocity for each device was plotted as relative AE gain vs. input DC power. For each voltage applied, the corresponding current was measured and that product is the input DC power. Figure 5.9 shows several different comparisons of input DC power vs. measured relative AE gain. For the case where the segment unit length is held constant, then there are two possible outcomes when adding an additional segment. If the scaling is the same, then the additional segment will increase the AE gain but also increase the input DC power to the same value as if applying a larger voltage on a single segment to achieve that gain. On the other hand, if the scaling is not the same then adding segments will either have a larger or smaller input DC power than a single segment for the same achievable AE gain.

Figure 5.9 (a-c) make this comparison for segment unit lengths of 100 μm, 175 μm, and 250 μm, respectively. For devices operating at the same acoustic frequency, adding segments actually reduces the required input DC power to achieve the same AE gain. This makes

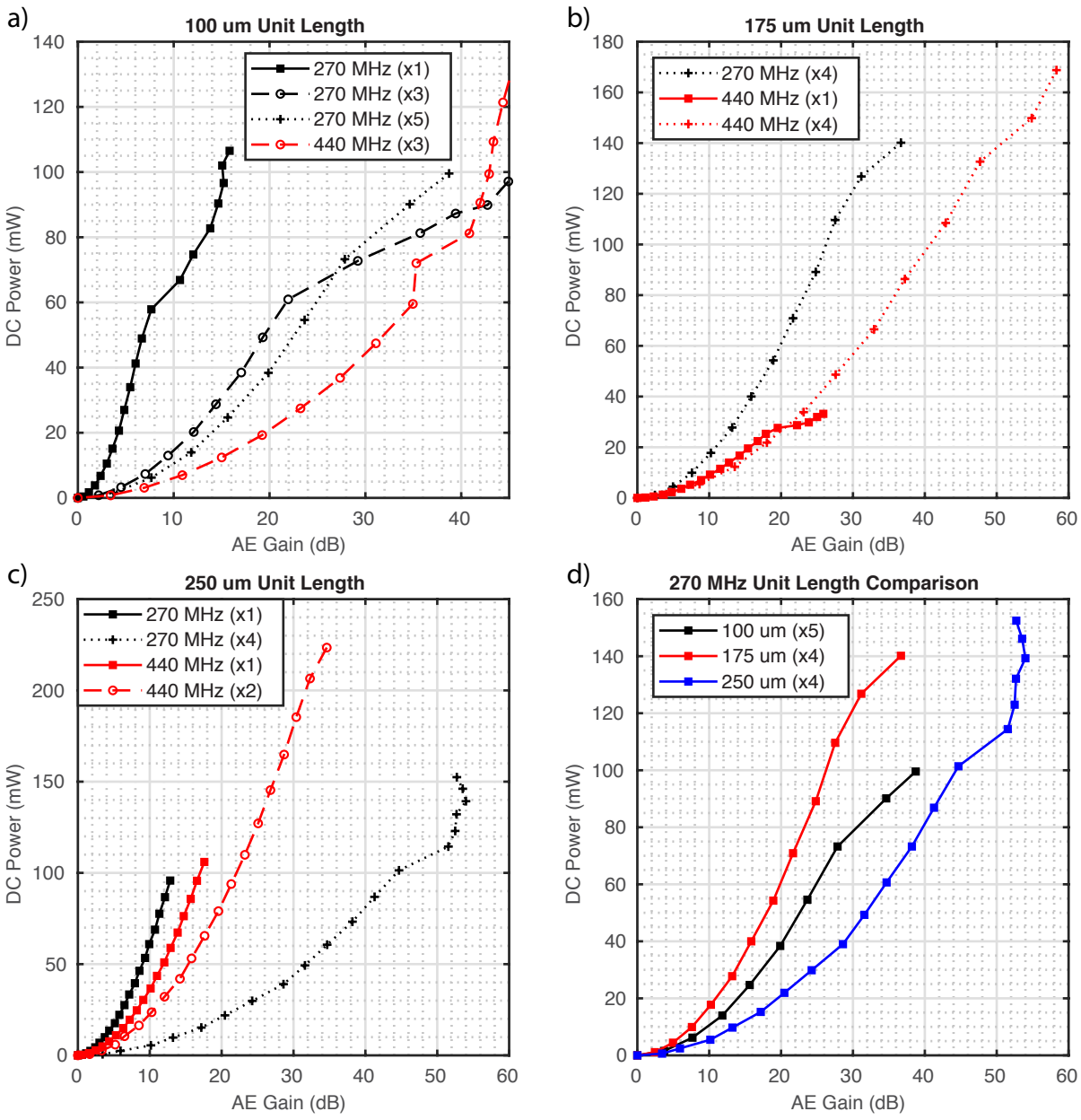

Figure 5.9. Trade-off between input DC power and measured relative AE gain performance. (a) comparison of AE delaylines with 100 μm unit length segments. (b) comparison of AE delaylines with 175 μm unit length segments. (c) comparison of AE delaylines with 250 μm unit length segments. (d) comparison of AE delaylines operating at 270 MHz.

sense in the current InGaAs-LN platform since applying a smaller drift field allows one to operate at a higher gain slope and therefore consume less input power. A similar trend is observed for the same number of segments, but operating at a higher acoustic frequency. Operating at a higher acoustic frequency increases the maximum achievable AE gain, which increases the gain slope at lower drift fields. Similar to before, the higher gain slope allows for less DC power to be consumed for the same AE gain. Take for example the 270 MHz and 440 MHz four segmented delaylines with a unit length of 175 μm. For both of them to achieve a relative AE gain of 30 dB, the 270 MHz delayline requires 120 mW of input DC power whereas the 440 MHz delayline only requires 58 mW. The final comparison is shown in Figure 5.9 (d). For an operating acoustic frequency of 270 MHz, the largest number of segments is plotted for each unit length. When comparing the 175 μm device (red) with the 250 μm device (blue), the larger unit length device used 3 times less DC power to achieve the same relative AE gain. Overall, adding segments and increasing the acoustic frequency increases the gain slope and reduces the input DC power to achieve a certain AE gain on this InGaAs-LN platform.

5.3 Dual-Voltage Acoustoelectric Amplifier Design

The device designs so far have only taken advantage of the non-reciprocal attenuation. The AE effect can also be explored to take advantage of the non-reciprocal acoustic phase shifts [115, 116]. This can be accomplished by adding another degree of freedom, a second drain voltage, to the segmented delayline design. This dual-voltage delayline is illustrated in Figure 5.10. In each segmented AE region, there are two drain voltages (V_1 & V_2) that control opposing drift fields. The V_1 controls a drift field in the same direction as the forward propagating acoustic wave (blue arrows) and V_2 controls a drift field in the direction of the backward propagating acoustic wave (red arrows). The forward acoustic wave is defined as propagating from Port 1 to Port 2 and the backward propagating wave is defined as propagating from Port 2 to Port 1. This section will cover the theory and fitness function analysis for the dual-voltage amplifier. Then, initial measurements and analysis are presented and discussed.

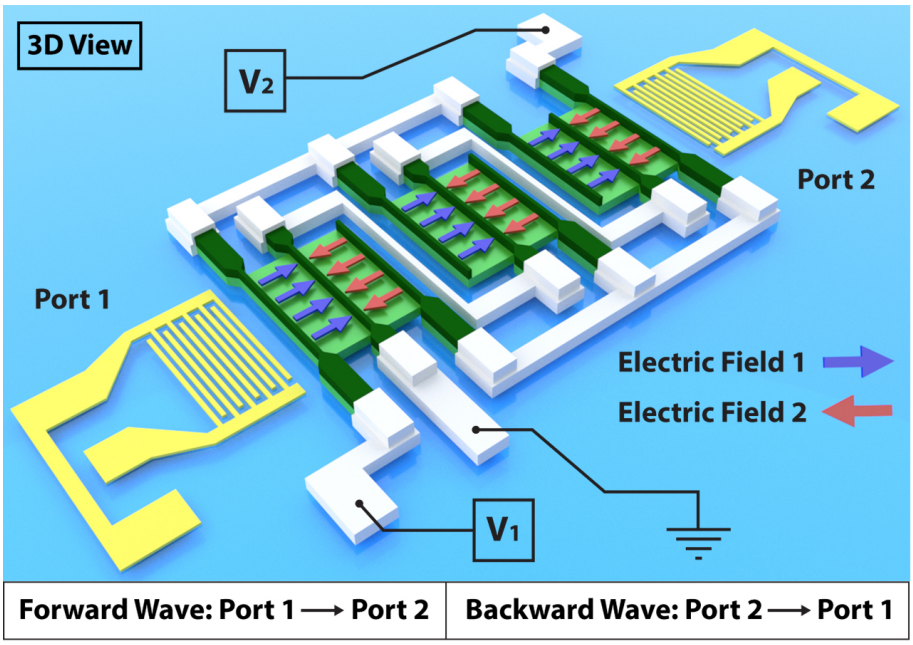

Figure 5.10. Illustration of a dual-voltage AE delayline amplifier. The blue and red arrows indicate the drift field direction for drain voltage 1 and drain voltage 2, respectively.

5.3.1 Variable Isolation and Phase Shifting Theory

The AE attenuation is antisymmetric about the equal velocity operating point, which is different than the 0 V drift field operating point. If the antisymmetric point was at 0 V drift field, then the AE attenuation from V_1 and V_2 would cancel each other out as the forward wave propagates through both regions. Since that is not the case, a fitness function was developed to find a path along the AE attenuation surface V_1 & V_2 that has a fixed forward amplitude, but variable forward phase delay and variable backward isolation. The AE attenuation for the forward and backward propagating acoustic waves can be defined as

$$\alpha^{\mathrm{AE}}_{\mathrm{forward}} = \alpha^{\mathrm{AE}}\left(\mathrm{V}_1\right) + \alpha^{\mathrm{AE}}\left(-\mathrm{V}_2\right), \tag{5.1}$$

$$\alpha^{\mathrm{AE}}_{\mathrm{backward}} = \alpha^{\mathrm{AE}}\left(-\mathrm{V}_1\right) + \alpha^{\mathrm{AE}}\left(\mathrm{V}_2\right). \tag{5.2}$$

The fitness function for a constant forward amplitude is

$$F = \alpha^{\mathrm{AE}}_{\mathrm{forward}} - P, \tag{5.3}$$

where the term P is a penalty function applied to the fitness function, given as

$$P = \xi \left| \alpha^{\mathrm{AE}}_{\mathrm{forward}} - \alpha^{\mathrm{AE}}_{\mathrm{operating}} \right|. \tag{5.4}$$

The penalty function P assigns a penalty weight (ξ) proportional to how much the fitness function deviates from the desired fixed forward AE operating gain ($\alpha^{\mathrm{AE}}_{\mathrm{operating}}$). Also, to remove duplicates in the fitness curve a conditional penalty is given as

$$\text{If} \quad \alpha^{\mathrm{AE}}_{\mathrm{backward}} > 0, \quad \text{then} \quad F = \mathrm{NaN}. \tag{5.5}$$

This removes any part of the fitness curve where there is gain in the backward direction, ensuring the fitness function is only being evaluated for backward isolation.

Figure 5.11 (a) shows an example analytical fitness function for a 250 μm unit length dual-voltage delayline in the InGaAs-LN platform. A fixed AE forward gain of 0 dB was

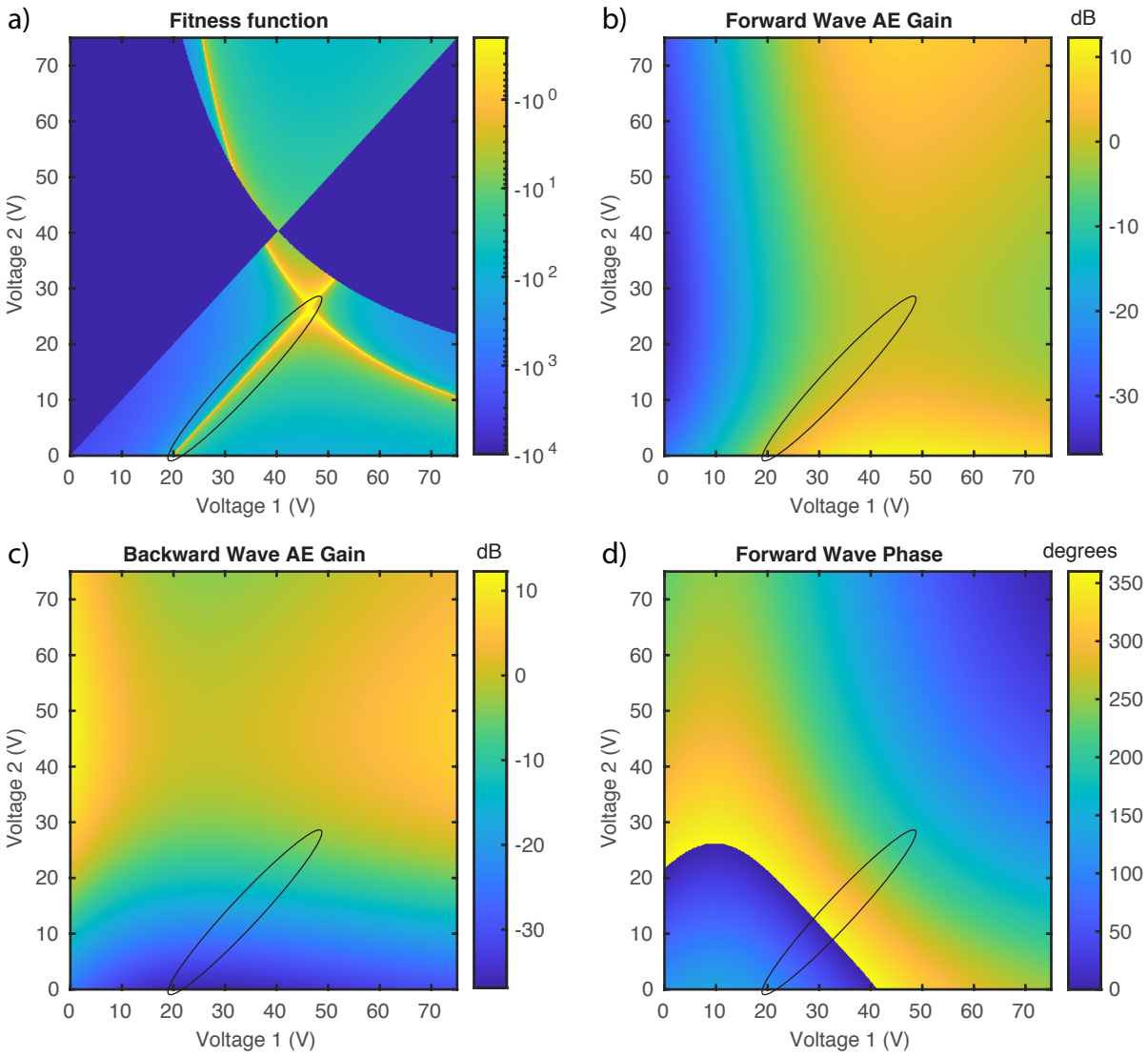

Figure 5.11. Analytical (a) fitness function for a fixed forward wave AE gain, (b) surface plot of forward wave AE gain, (c) surface plot of backward wave AE gain, (d) surface plot of forward wave phase.

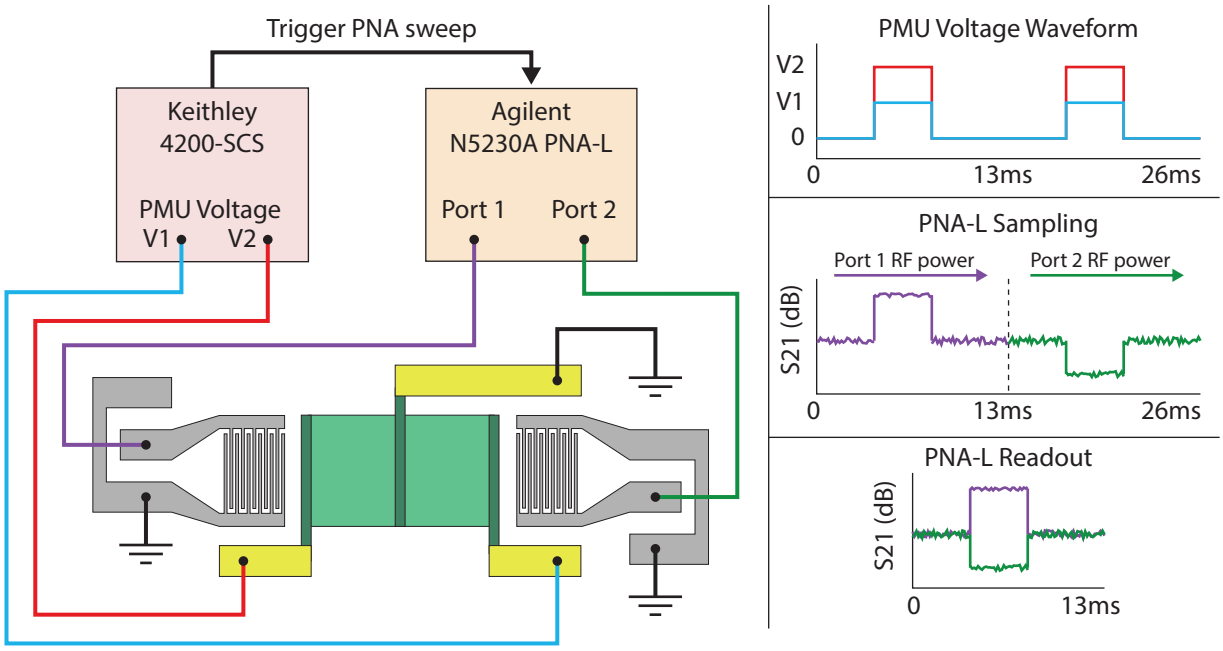

Figure 5.12. (left) Illustration of the dual-voltage pulse measurement setup with the PNA-L and Keithley 4200-SCS. (right) The illustrated plots show the triggering and timing sequence for measuring the S-parameters with applied voltage pulses.

chosen as the operating point. For illustrative purposes, an example voltage path is circled in black ranging from $[V_1,V_2] = [20\ V,\ 0\ V] \rightarrow [45\ V,\ 25\ V]$. Figure 5.11 (b-d) show the analytical surface plots of the parameters of interest along with the example voltage path circled. Within the voltage path, the forward wave AE gain is a constant 0 dB, while the backward wave AE gain varies from -35 dB to -10 dB. Also, the forward wave phase changes over 180° along this voltage path.

In order to measure a dual-voltage AE delayline, a slight modification needs to be made from the previous pulsed setup in Figure 5.2. The new measurement setup and example timing sequence is shown in Figure 5.12. An additional, independent voltage line is connected to the dual-voltage AE delayline. The triggering sequence and data acquisition method for the PNA-L remains the same, but now the voltage pulse waveform contains two voltages that are applied during the same 2 ms window. This ensures the device operates with both voltages on at the same time.

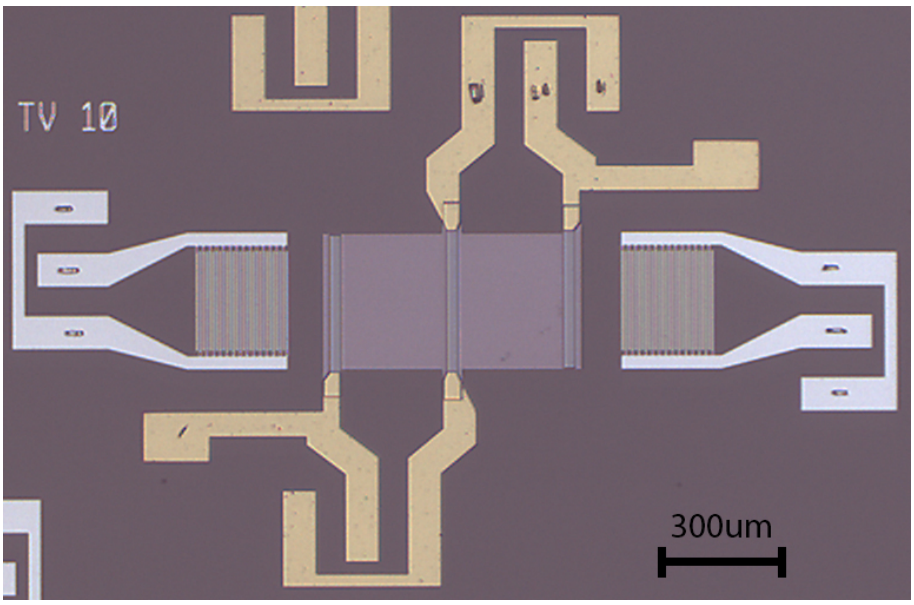

Figure 5.13. Optical image of the measured dual-voltage AE delayline.

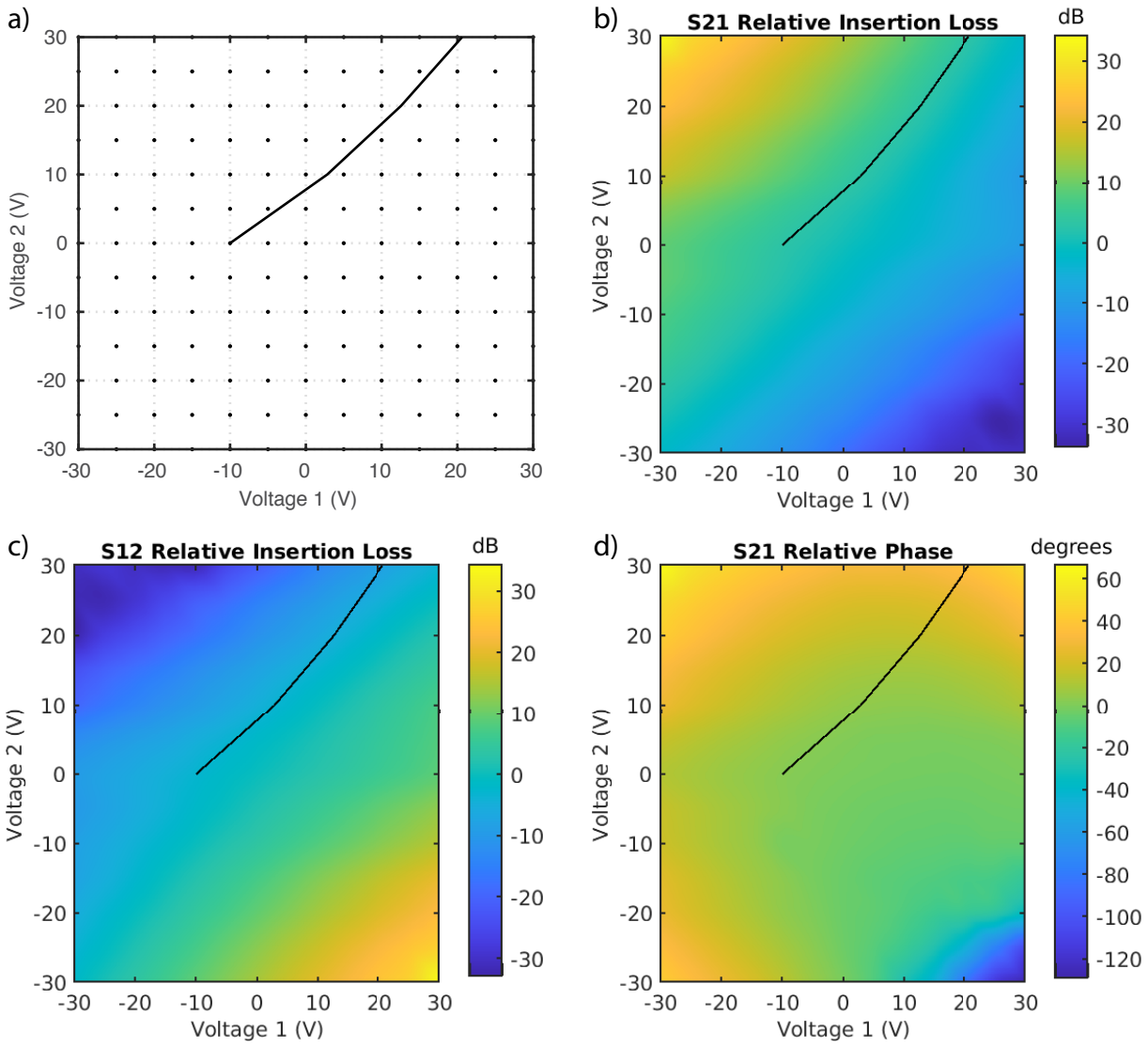

Figure 5.14. (a) Display of the measurement points in the V_1 & V_2 parameter space along with the interpolated voltage path. (b) Interpolated relative S_{21} insertion loss, (c) relative S_{12} insertion loss, and (d) relative S_{21} phase.

5.3.2 Results and Discussion

Figure 5.13 shows an optical image of the measured dual-voltage AE delayline. The AE unit lengths for both V_1 and V_2 regions are 250 μm and operates at an acoustic frequency of 270 MHz. The measurement results are shown in Figure 5.14 over a parameter space of 30 V. In order to see the trends over the full voltage range, a grid based measurement was performed [Figure 5.14 (a)]. Measurements were taken every 5 V over the entire voltage space and the

resulting data was interpolated to get the trends in relative insertion loss and phase. A fixed forward AE gain of 3 dB was chosen and the resulting interpolated voltage path is shown as a solid black line. This voltage path ranges from [-10 V, 0 V] $\rightarrow$ [20.6 V, 30 V]. Along this interpolated voltage path, the relative S_{21} insertion loss remains around the desired +3 dB. The relative S_{12} insertion loss changes from -3 dB to -8 dB along the voltage path, leading to a total change of 5 dB in isolation. Finally, the relative S_{21} phase changes from 2.7° to 37.9° along the voltage path. This results in a net change of 35.2°, which is much lower than the expected total phase shift. This large discrepancy in performance has to do with the carrier concentration on this InGaAs-LN wafer. The fitted carrier concentration is higher than expected, which results in a broadening of the AE gain and velocity curves (as discussed in Chapter 3). This broadening reduces the relative difference in AE velocity shift between the forward and backward propagating waves. In order to get a large phase shift in this dual-voltage AE delayline, there needs to be a large relative difference in AE velocity shifts. Therefore, a lower carrier concentration is desired for operation of these dual-voltage AE delaylines.

5.4 Acoustoelectric Switch Design

When designing AE RF devices, the use of AE regions in the propagation path of SAW delaylines does not need to be limited to single delaylines. For SAW delaylines, Multi-Strip Couplers (MSC) have been used extensively for signal routing applications [117, 118], removal of unwanted modes [119, 120], SAW filters [121, 122], and even recently in released Lamb wave delaylines [123]. An natural extension of the previous AE device designs on the InGaAs-LN platform is to incorporate MSC elements to create non-reciprocal acoustic signal routing. Figure 5.15 shows an illustration on a 3-Port AE switch utilizing a MSC element and two segmented AE delaylines. The two segmented delaylines are connected source-to-drain, which means the applied drain voltage will have opposite polarities in the two AE delaylines. Effectively this creates gain in one track and increased attenuation in the other track. By switching the polarity of the applied drain voltage, the output acoustic signal can switch tracks. For example, in Figure 5.15 the polarity of the applied drain voltage

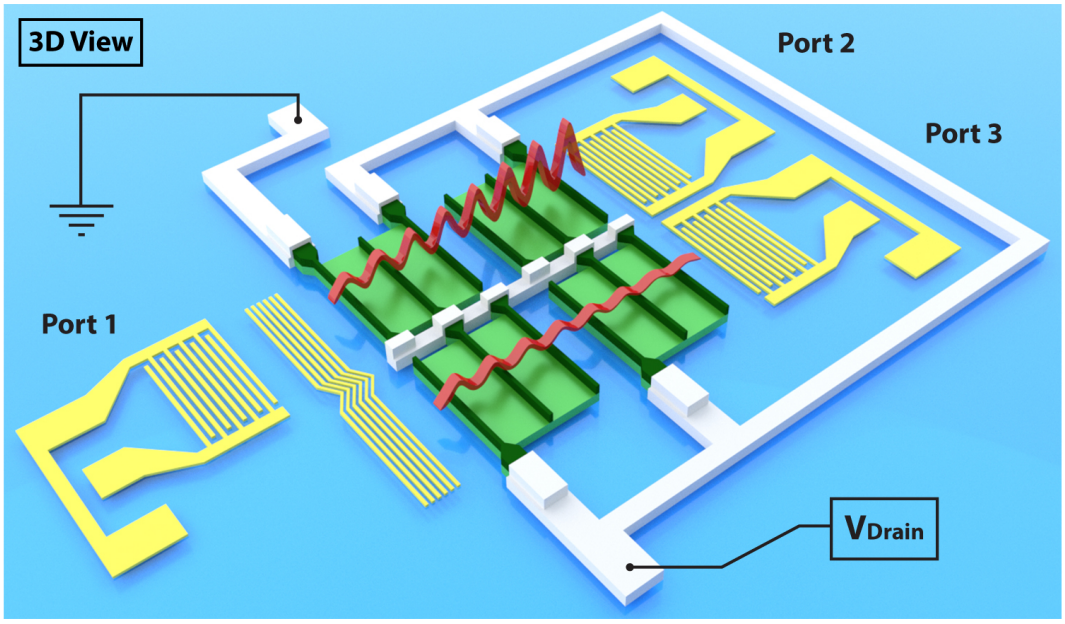

Figure 5.15. Illustration of a 3-Port AE delayline switch.

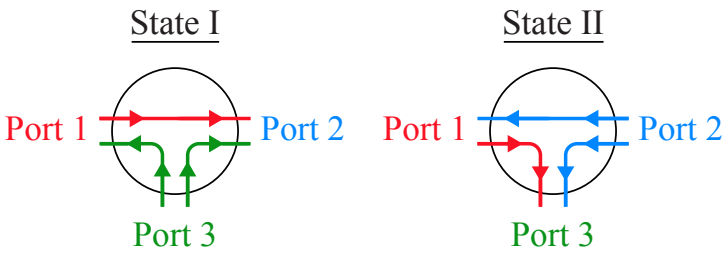

Figure 5.16. Illustration of the different switch states depending on the polarity of the voltage applied.

can switch the allowed propagation from Port 1 → Port 2 to Port 1 → Port 3. Figure 5.16 shows the full set of non-reciprocal paths for both drain voltage polarities (switch states). The main switch paths designed for are highlighted in red. Depending on the drain voltage applied, an RF signal excited from Port 1 will either be allowed to propagate to Port 2 or Port 3. Without the presence of any reflections, the path between Port 2 and Port 3 should not exist, but if any reflections are present they will be amplified by the AE regions in both delaylines. Since they will experience two segments of gain instead of one, the amplification from Port 2 → Port 3 should have a higher gain slope than the other port paths.

5.4.1 Multi-Strip Coupler Theory

These MSC are a series of open-circuit metal lines with a pitch less than the pitch of the IDTs. An illustration of how example MSC routing designs transfer energy is shown in Figure 5.17. The simplest MSC design is the half transfer MSC [124, 125]. When an acoustic wave enters the half coupler from the upper track, it generates an alternating voltage and current on the MSC metal strips. This in turn actuates an acoustic mode in the lower track. Since the voltages are the same in both the upper and lower track, but the current is equal and opposite on both track, a 90° phase shift is imparted on the track where the acoustic wave is being generated. Each MSC unit represents the amount of metal strips needed to transfer half of the acoustic energy from one track to another. The theory for determining the appropriate number of fingers for half energy transfer and the pitch needed to avoid the stop band of the MSC can be found here [126, 127]. When two of these half couplers are placed in series [Figure 5.17 (left)], it creates a full energy transfer MSC. The illustration shows at the end of the full transfer MSC, all of the energy has transferred from the upper track to the lower track with an additional 90° phase shift plus propagation phase.

When a half transfer MSC is folded in a U-shape so that the output of the half coupler goes back into the input, the result is a perfect mirror where all of the energy is reflected back. These U-shaped reflectors can be combined with a half transfer MSC to create a track change MSC [Figure 5.17 (right)]. When an acoustic wave is incident on the track change MSC from the upper track, all of the energy is transferred to the lower track but propagating

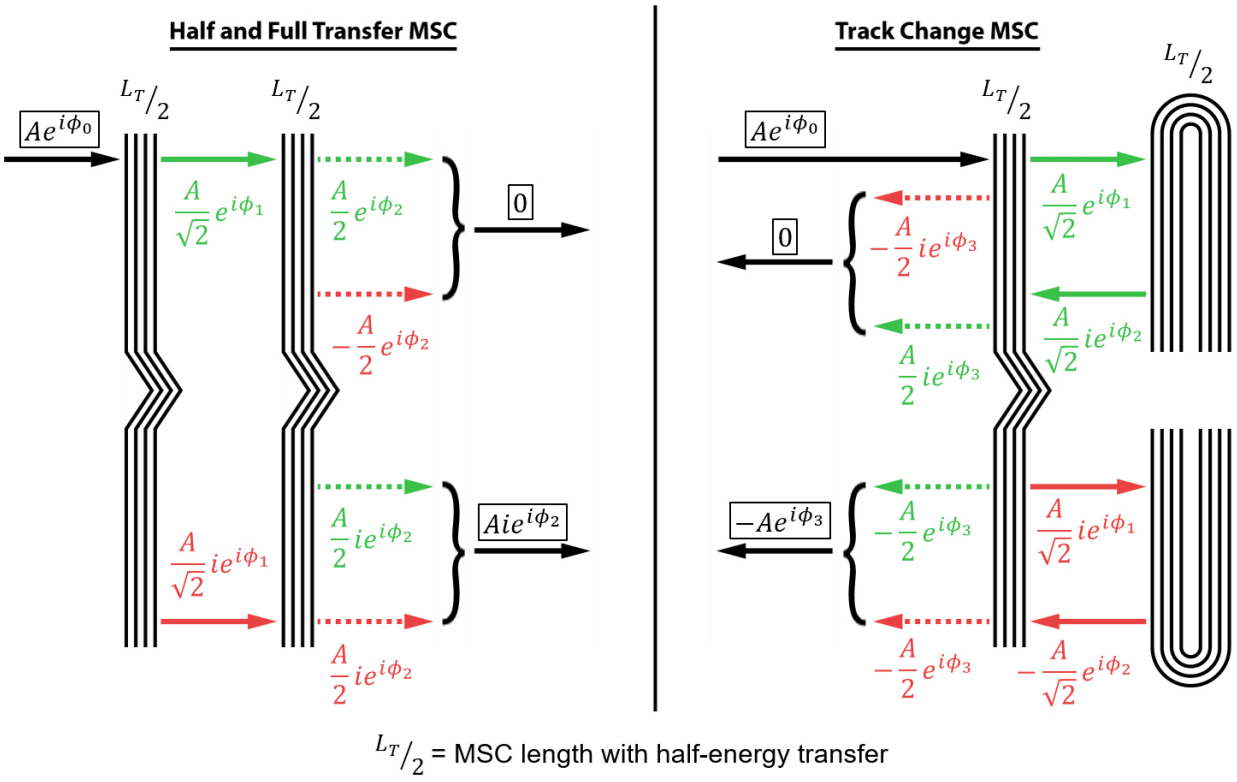

Figure 5.17. Illustration of MSC operation and example MSC devices.

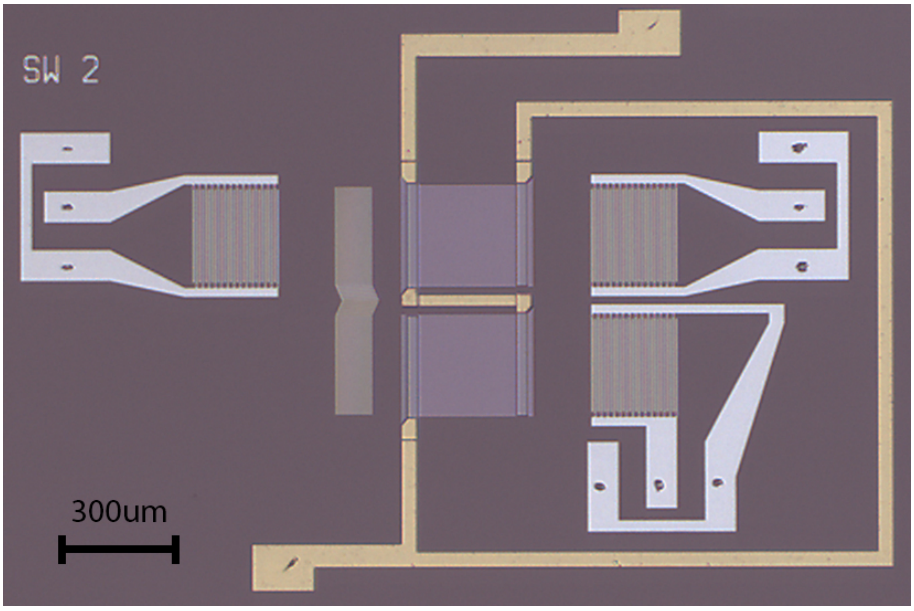

Figure 5.18. Optical image of the measured AE delayline switch.

in the opposite direction. In addition to the U-type track change MSC design [128], there is also a reversing multistrip coupler (RMSC) design [129] that is compact and more practical to implement in SAW AE devices. The half, full, and RMSC designs will be used in the subsequent AE device designs to route the non-reciprocal acoustic signals.

5.4.2 Results and Discussion

Figure 5.18 shows an optical image of the measured AE switch. Instead of taking a fully calibrated 3-Port S-parameter measurements, the experimental setup in Figure 5.2 was used with three separate calibrated 2-Port S-parameter measurements. The device consists of cross-linked single segment AE delaylines with unit lengths of 250 μm. The measured transmission and reflection characteristics of all port combinations with no applied voltage pulse is shown in Figure 5.19. The S_{21} and S_{31} insertion losses were designed to be the same with a half energy transfer MSC. The resulting insertion losses differ by about 4 dB, which means the MSC might not be exactly transferring half of the energy or there were some slight fabrication differences between the top and bottom delaylines. The transmission between

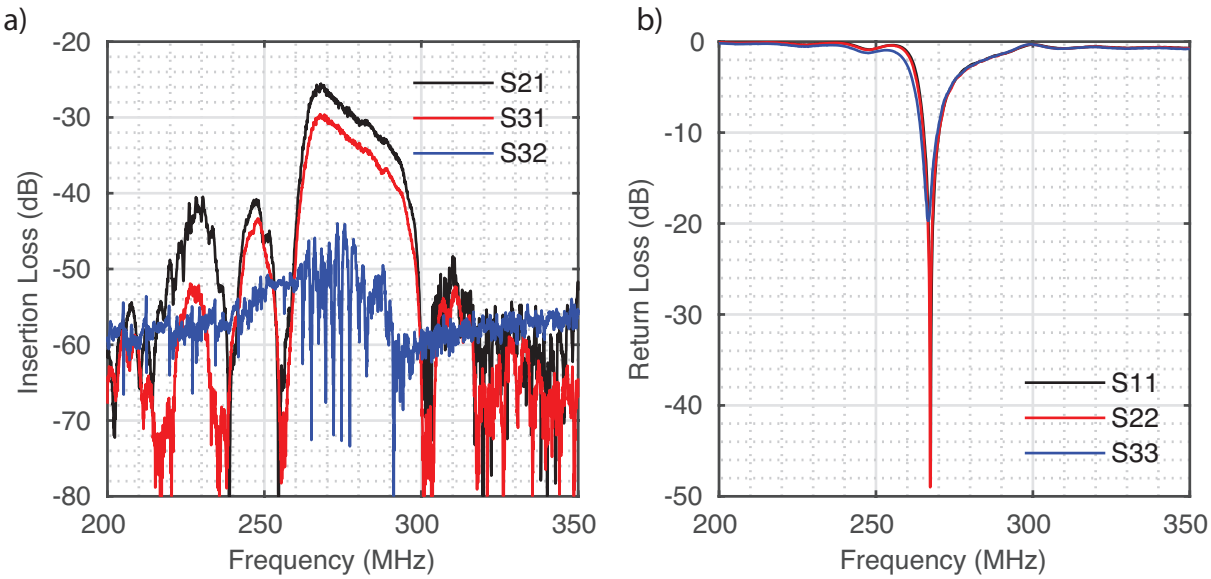

Figure 5.19. The measured (a) transmission and (b) reflection S-parameters for all of the port combinations with no voltage pulse applied.

Port 2 and Port 3 is almost 20 dB lower because only reflections off of the MSC and IDTs are transmitted along that path.

Figure 5.20 shows the measured relative insertion loss of all of the switch paths as a function of applied drift field. In this configuration, State I of the switch corresponds to a positive drift field and State II corresponds to a negative drift field. The main switch paths were intended to operate with a Port 1 excitation and to look at 3 main characteristics: signal gain (Port 1 $\rightarrow$ Port 2), backward isolation (Port 2 $\rightarrow$ Port 1), and switch isolation (Port 1 $\rightarrow$ Port 3). For example, in State I with an applied drift field of 1.5 kV/cm, the signal gain (S_{21}) is 14.5 dB, the backward isolation (S_{12}) is -17.8 dB, and the switch isolation (S_{31}) is -28 dB. This also leads to a total signal strength difference of 42.5 dB between forward and backward propagating waves between Port 1 and Port 2. There is also a 32.3 dB difference in signal strength when comparing both of the output ports of the switch (Port 2 and Port 3).

When looking at both paths with a Port 3 excitation (S_{13} & S_{23}), the application of a drift field had no change on the signal amplitude. With no voltage pulse applied, the frequency response of the IL was completely reciprocal between Port 1, Port 2, and Port 3 excitations, so the application of a drift field should produced a mirrored AE response to

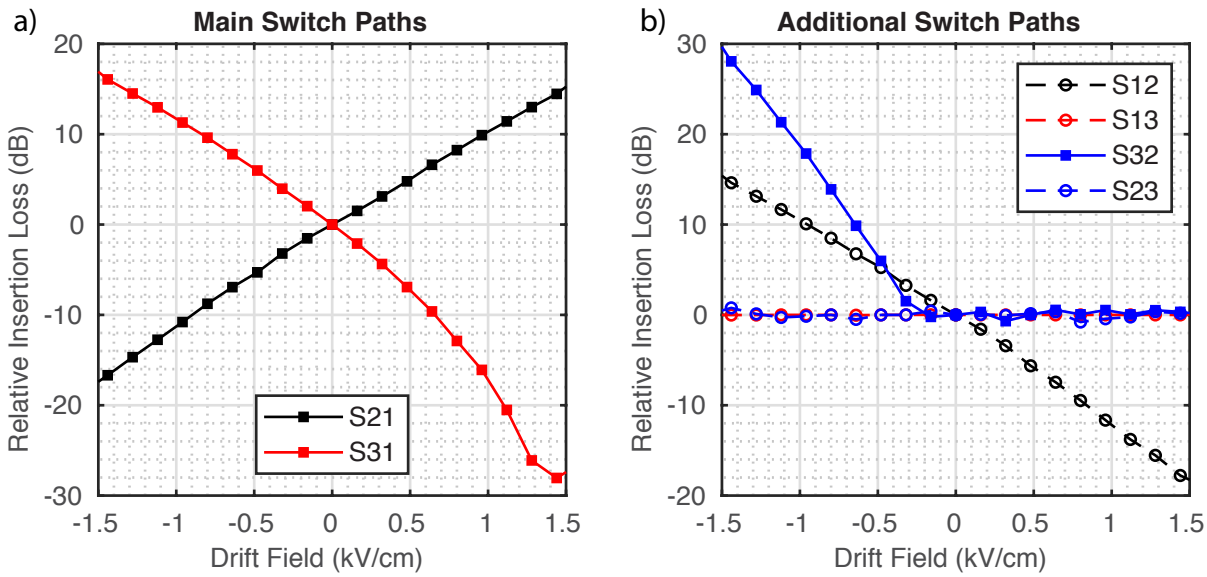

Figure 5.20. Measured relative insertion loss as a function of drift field for (a) the main switch paths and (b) all of the additional switch paths.

that seen from a Port 2 excitation (S_{12} & S_{32}). Further investigation is needed into the chevron MSC design, Port 3 IDT design, and DC routing of the cross linked AE segments to figure out this discrepancy in AE performance with a Port 3 excitation. Finally, the path between Port 2 and Port 3 is examined. The starting IL with no voltage applied is -55 dB, which is at the noise floor of this measurement setup. For both State I and State II of the switch, the S_{32} relative insertion loss as a function of applied drift field will be analyzed. In State I, the wave (Port 2 $\rightarrow$ Port 3) travels through an AE region with an opposite drift field polarity, get reflected off of the MSC, and again sees an AE region with an opposite drift field polarity. This means the reflected signal will experience AE attenuation from two AE segments. Since the S_{32} signal strength is already at the measurement floor, any additional loss won't be captured above the measurement noise which is why the relative insertion loss remains constant through State I. Similarly, in State II the reflected signal sees AE gain from two AE segments and the signal strength increases above the measurement noise. Based on the previous analysis of segmented AE delaylines, adding segments increases the gain slope and allows for a higher relative AE gain for the same drift field applied. This gain slope difference can be seen by comparing in State II a single segment propagation path (S_{12}) and the double segment reflected propagation path (S_{32}). At a -1.5 kV/cm applied drift field, the AE gain is 30 dB for S_{32}, which is 30 times higher than the AE gain (15 dB) for S_{12}.

5.5 Strip-Coupled Acoustoelectric Amplifier Design

One of the major issues with AE delaylines on bulk LN platforms is substrate heating during Continuous Wave (CW) operation. One possible solution is to engineer the stack itself to utilize a thin film of LN on Si or SiO_2 to have better heat dissipation [33, 130]. A more flexible solution, which can be lithographically defined, is the use of periodic metal strips to couple an adjacent semiconductor thin film to a travelling acoustic wave [131–133]. When the semiconductor is placed in the propagation path, the aperture of both the semiconductor and acoustic wave need to be similar in order to have maximum interaction strength. By spatially separating the semiconductor layer and acoustic mode, the relative widths no longer need to be the same. The semiconductor's aperture can be reduced and coupled to the acoustic mode

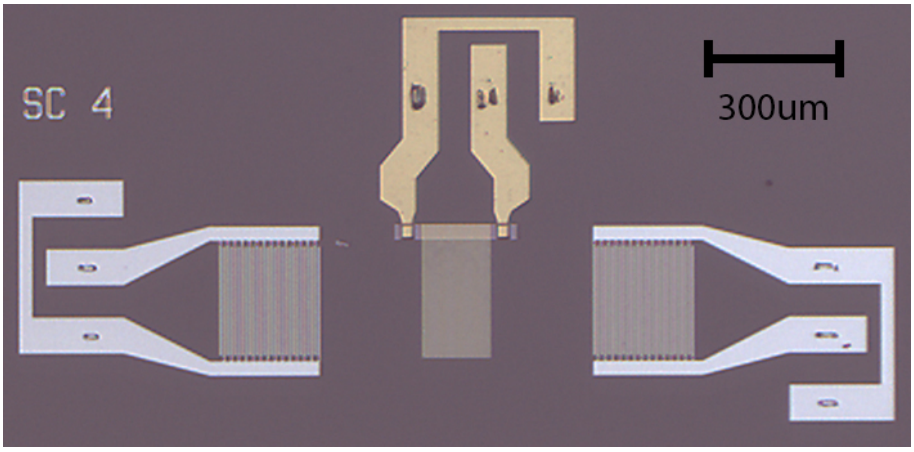

Figure 5.21. Optical image of the strip coupled AE delayline amplifier.

through strip couplers. Recently, CW operation was achieved on a bulk LN AE platform using an adjacent graphene layer strip coupled to a SAW mode [82]. Using the InGaAs-LN platform, a small aperture InGaAs segment is strip coupled to a LSAW delayline. The goal is to achieve similar AE gain performance compared to the previous segmented delaylines with the added benefit of lower heat dissipation from a smaller semiconductor area. The ultimate goal is to operate these strip coupled AE amplifiers on the InGaAs-LN platform in CW instead of pulsed mode.

Figure 5.21 shows the optical image of the measured strip coupled AE amplifier. The acoustic wavelength is 16 μm and the width of each strip coupler is 2.45 μm. As the acoustic wave is propagating, the strip coupler is sampling around 6-7 samples per wavelength. The InGaAs region is 175 μm long and two wavelengths wide. In order to compare the performance of this strip coupled (SC) amplifier to a traditionally coupled (TC) amplifier of similar length, the SC amplifier was measured in pulsed mode operation using the same setup in Figure 5.2. A comparison of measured relative AE gain as a function of drift field for pulsed mode operation is plotted in Figure 5.22. For all of the drift fields applied, the AE interaction is smaller in the SC amplifier as compared to the TC amplifier. At a drift field of -1 kV/cm, the SC amplifier shows an AE gain of 0.35 dB while the TC amplifier has an AE gain of 2.7 dB. The performance of the SC amplifier could be improved by using e-beam lithography instead of photolithography. The choice of a 2.45 μm strip width was limited

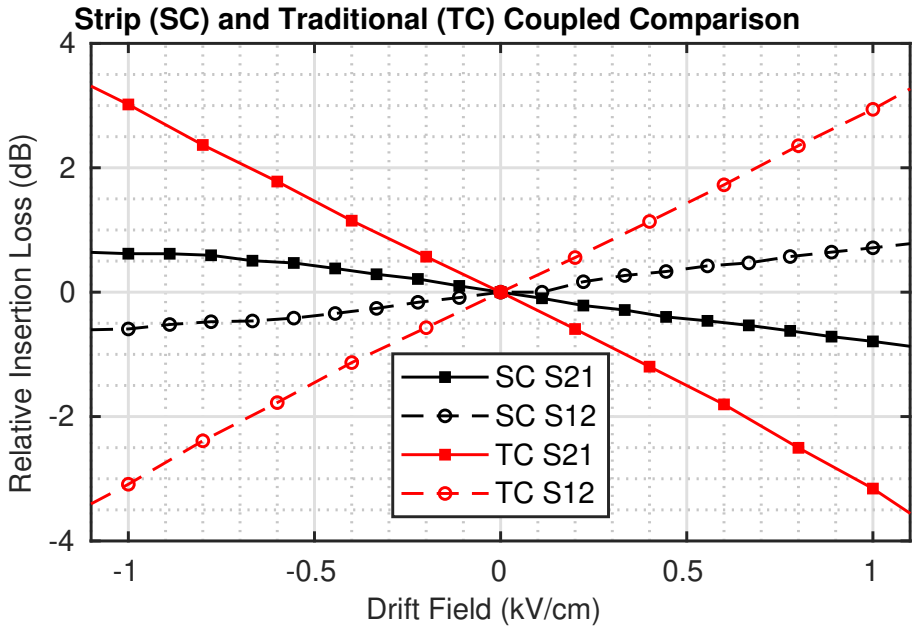

Figure 5.22. Measured relative insertion loss as a function of drift field for a SC and TC amplifier with 175 μm long gain segment.

by the lithographic resolution of the current fabrication process. The overall performance could be improved by increasing the sampling, which means making the strip widths as thin as possible relative to the acoustic wavelength. Also, in order to operate in CW a smaller aperture InGaAs layer is required. Other strip coupled amplifiers on bulk LN [82] had a semiconductor aperture smaller than 1 acoustic wavelength. An initial SC amplifier was demonstrated on the InGaAs-LN platform in pulsed mode operation. In order to further improve the performance and operate in CW, more sampling of the acoustic mode is needed as well as optimizing the InGaAs segment length and aperture.

5.6 Ultra Compact Single Wavelength Acoustoelectric Amplifier Design

This last section looks at scaling the AE delayline amplifier down to a single wavelength interaction region. There has been previous work on wavelength-scale AE interactions on an AlGaN/GaN platform using high-electron-mobility transistors (HEMT) for the generation and detection of SAW modes [134, 135] and even demonstrating AE gain [136]. On the InGaAs-LN platform, single wavelength InGaAs segments with N+ contact types were used in a delayline amplifier. The N+ contact type was chosen over the Au contact type to reduce the IL as much as possible under no biasing conditions. The first device operates at an acoustic frequency of 270 MHz, which corresponds to an acoustic wavelength of 16 μm. The second amplifier operates at 440 MHz and has an acoustic wavelength of 10 μm. Both of these fabricated devices are shown in Figure 5.23.

Since the devices have different acoustic wavelengths, the AE segments are also different lengths. Given the same voltage applied to each device, they will experience different drift fields and therefore different operating points on the AE curve. To better compare the performance of these devices, the measured relative insertion loss and relative phase are plotted as a function of applied drift field and shown in Figure 5.24. The 440 MHz device has a larger AE gain and phase shift (7 dB, 45°) than the 270 MHz device (2.8 dB, 16°) for the same drift field, which again shows that increasing the acoustic operating frequency of devices on the InGaAs-LN platform towards the GHz regime will improve the AE performance of all device designs. In terms of input power, the 440 MHz amplifier operates at 5 V and

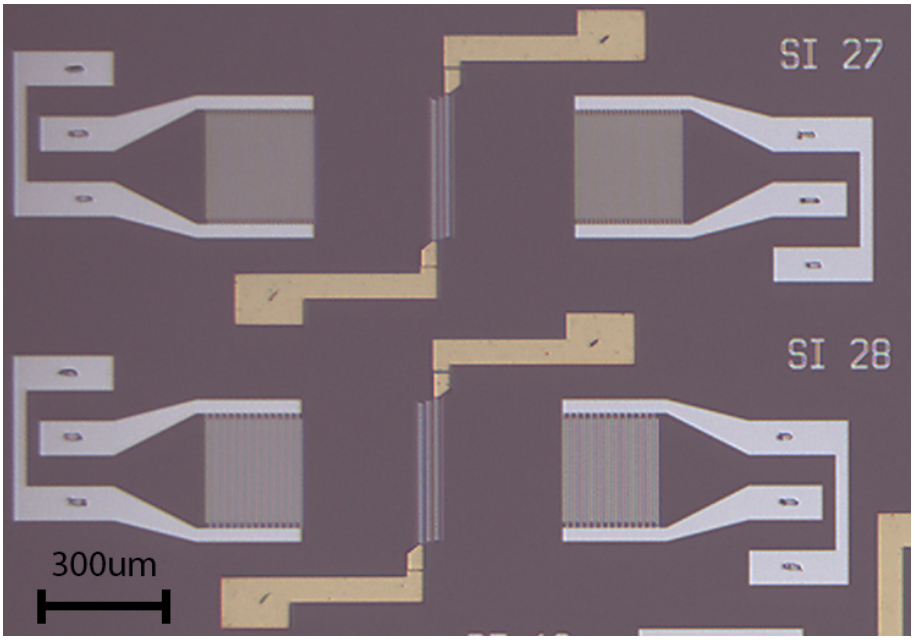

Figure 5.23. Optical image of the single wavelength AE delayline amplifiers at acoustic frequencies of (top) 440 MHz and (bottom) 270 MHz.

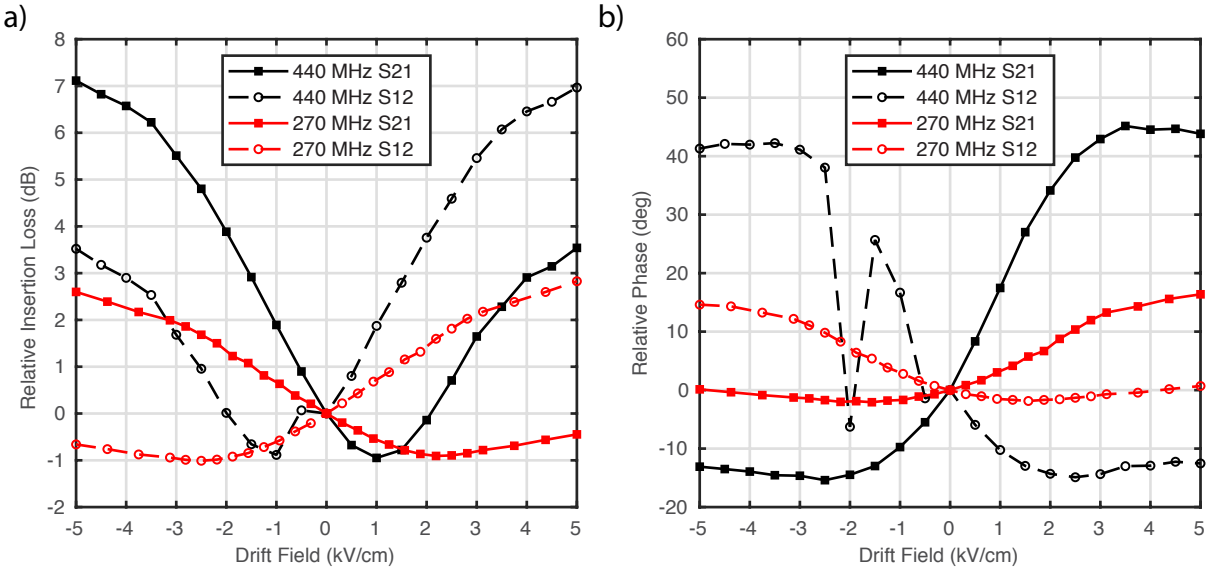

Figure 5.24. Measured (a) relative insertion loss and (b) relative phase as a function of drift field for both the 440 MHz and 270 MHz single wavelength amplifiers.

generates 1.36 mA of current, leading to a total input power of 6.8 mW. The 270 MHz amplifier required a larger voltage (10 V) and generated 1.76 mA of current, which leads to an input power of 17.6 mA. Further work can be done to investigate the wavelength and sub-wavelength AE interaction mechanics on the InGaAs-LN platform, but initial results have demonstrated an ultra compact single wavelength (10 μm) AE amplifier at 440 MHz yielding an AE gain of 7 dB consuming only 6.8 mW of power.

6. CONCLUSION AND FUTURE WORK

Several AE platforms were investigated in this thesis and a new library of AE devices were designed and demonstrated. For these new material platforms (LNOSi and LNOSOI), the acoustic and piezoelectric properties were simulated in COMSOL to explore the possible design space for making high performance AE devices. It was shown on the LNOSi platform that AE devices would need to be scaled above 2 GHz in order to take full advantage of the high k^2 Rayleigh SAW mode. On the LNOSOI platform, an extensive study was performed on the piezoelectric performance of both the Rayleigh and SH SAW modes as a function of wavelength, propagation angle, and type of IDT metal. The -30° Rayleigh SAW and +10° SH SAW showed promising results of having high k^2 values over a wide range of wavelengths, so a series of delaylines were fabricated for comparison. Due to the complexity of the LNOSOI platform, the lumped element cross-field Mason model was modified to include substrate conductivity and implemented in ADS. A fitting methodology was developed in ADS to fit lumped element circuit parameters to the measured S-parameters of SAW delaylines. The acoustic and piezoelectric properties of the SAW delayline can then be extracted from these fitted lumped element circuit parameters and compared to the COMSOL simulations. In addition, the trade offs between k^2 and Q were examined for all of the modes.

The AE analytical theory was discussed with respect to designing a high performance AE platform. Based on the semiconductor and operating acoustic mode chosen, there exists a maximum achievable AE gain for the platform at a specific carrier concentration and acoustic frequency. It is important to also consider the relative AE performance between forward and backward propagating acoustic waves when choosing an operating carrier concentration. This relative performance is critical when designing AE devices that incorporate opposing polarity AE segments. Finally, the initial development of a 2D AE FEA simulation scheme was presented with the goal of being able to simulate the AE interaction in more complex material stacks or mode shapes.

Finally, several new AE device designs were demonstrated on Sandia's InGaAs-LN platform. By moving the acoustically lossy Au/Ag Ohmic contact points outside of the delayline propagation region, the insertion loss was significantly reduced while maintaining the same

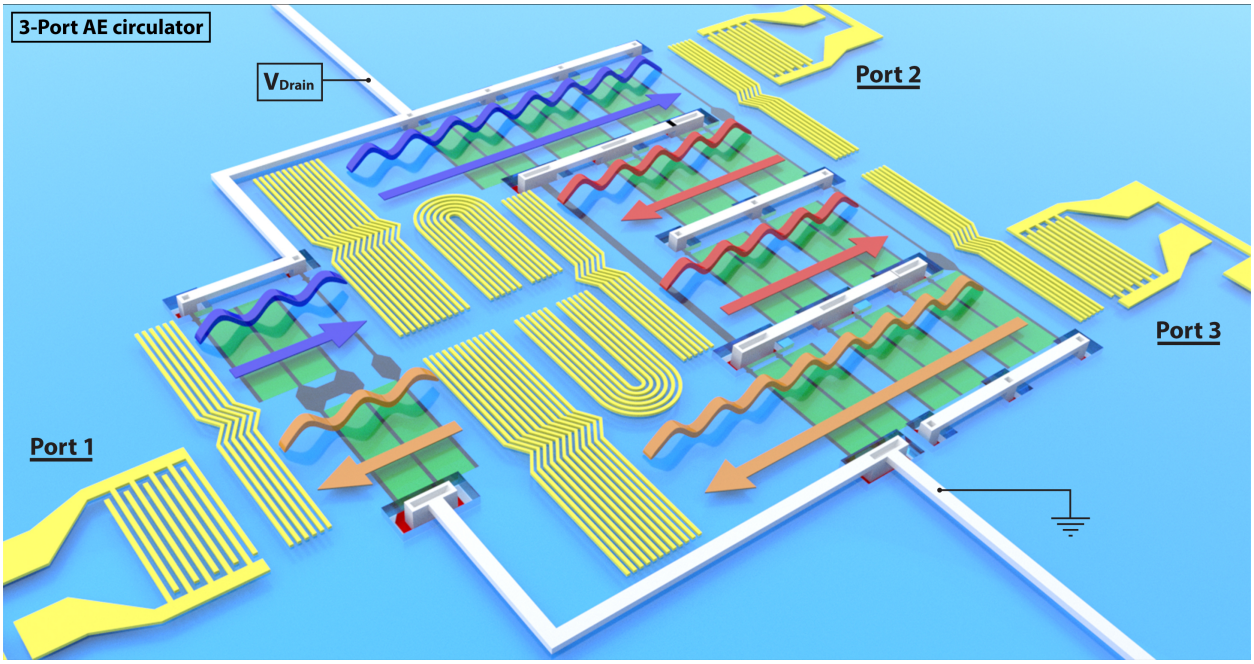

Figure 6.1. Illustration of a 3-Port AE circulator comprised of three interconnected AE switches.

AE performance. This opened up the possibility of designing multi-segmented AE delayline amplifiers. The relative AE gain and input DC power were then compared for different acoustic frequencies, segment unit lengths, and number of segments. It was concluded that for the given carrier concentration, operating at a higher acoustic frequency and having more segments will increase the AE gain slope and allow one to achieve a higher AE gain and lower input DC power. The dual-voltage AE delayline uses two segments in opposite polarity to provide independent control of a forward and backward wave. If a fixed forward gain is desired, a fitness function can be evaluated in the voltage parameter space to find such a voltage path. This in turn will also provide variable backward isolation and variable forward phase shift as a function of position along the voltage path. By incorporating MSC routing elements, AE delaylines can be combined to form more complicated signal manipulation devices. The first example of this is a 3-Port AE switch, which amplifies the Port 1 RF signal toward either Port 2 or Port 3 depending on the polarity of the applied drain voltage.

The next step for the InGaAs-LN platform is to expand the library of AE devices demonstrated. The most logical extension is to connect 3 AE switches together to form a 3 Port

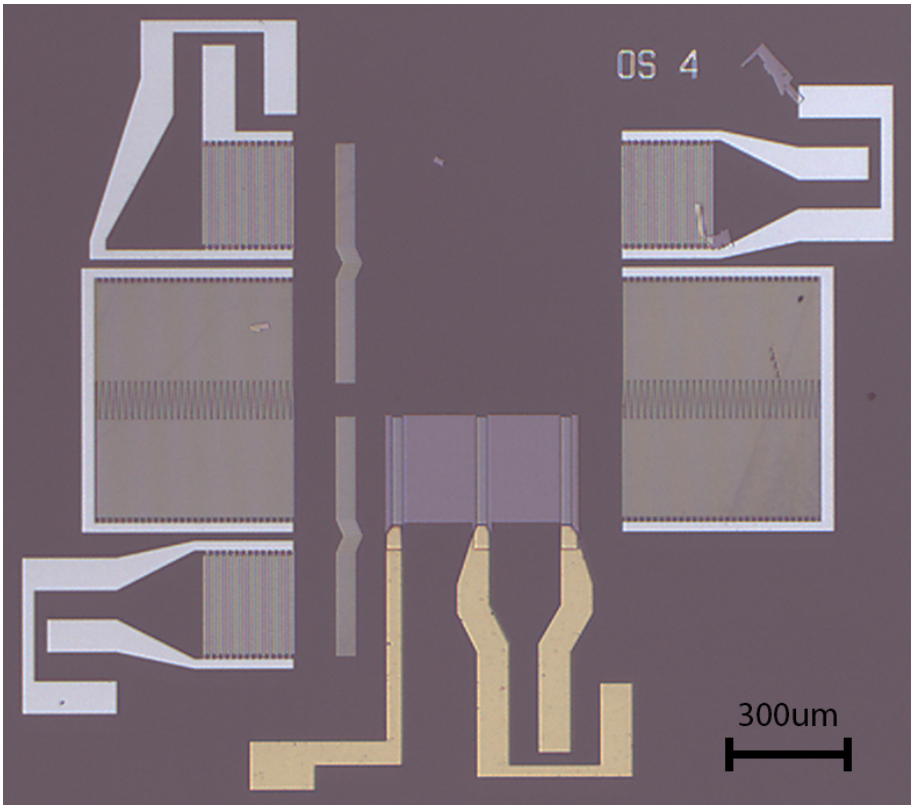

Figure 6.2. Optical image of a travelling wave AE resonator.

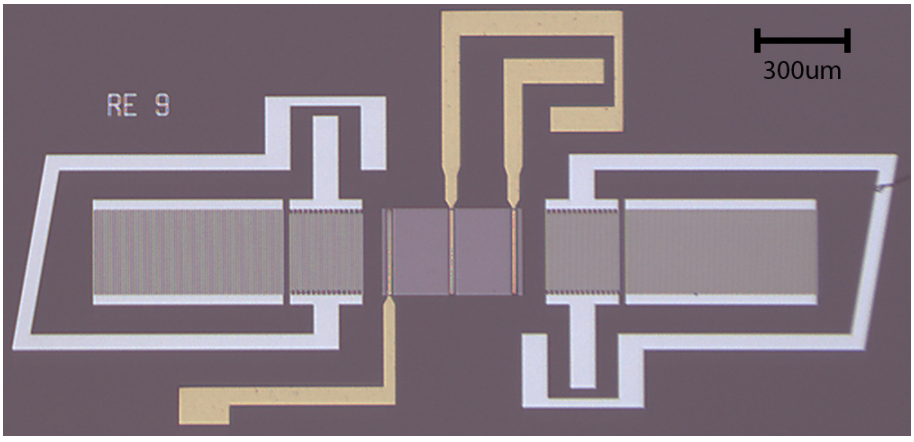

Figure 6.3. Optical image of an AE SAW resonator.

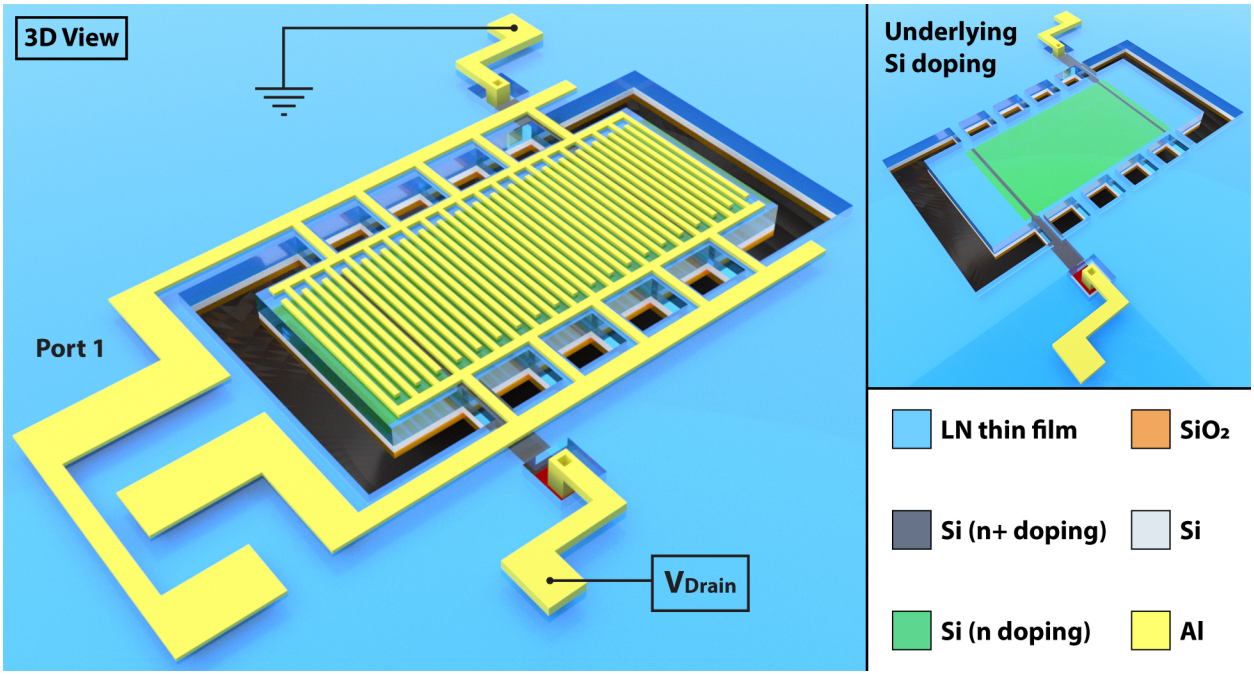

Figure 6.4. Illustration of an AE Lamb mode resonator on the LNOSOI platform.

AE circulator. Figure 6.1 shows an illustration of a 3 Port AE circulator. For a given drain voltage, each acoustic wave excited by a port is only amplified to the subsequent port (colored arrows). All other propagation paths for the acoustic wave would be attenuated. There have been recent publications on AE circulators, but one only simulated the performance [113] and the other had the IDTs within the circulation path [137]. The problem with having the IDTs in the circulation path is the gain loop formed between successive IDTs. As a wave from Port 1 is amplified to Port 2, some signal will propagate through the Port 2 IDT and continue to Port 3 and get amplified again. The circulator architecture proposed in Figure 6.1 folds all of the IDTs outside of the circulation path through the use of MSC routing.

Once the InGaAs-LN AE devices can be engineered to operate in CW mode, an interesting device to investigate is the AE travelling wave oscillator. Similar to a SAW ring waveguide resonator [138], the proposed design for an AE travelling wave oscillator is shown in Figure 6.2. Two RMSCs set up a travelling wave resonant cavity and a dual-voltage AE segment is placed inside the resonator. To achieve oscillation, the round trip gain and

phase conditions must be met. Both of these conditions can be met by finding the forward gain and forward phase shift operating point in the two voltage parameter space of the AE amplifier. Similarly, this dual-voltage AE gain segment could be placed in a standing wave SAW resonator as shown in Figure 6.3.

Finally, a high performance AE platform could be used to make AE Lamb wave resonators and oscillators. The doped LNOSOI material platform would be ideal for demonstrating this device. Figure 6.4 shows an illustration of an AE Lamb wave resonator on the LNOSOI platform. Previous work on AE resonators [75, 139] used material platforms with low k^2 and demonstrated small AE gains. Another added benefit to a doped LNOSOI platform is the ability to pattern the AE regions under the resonator (Figure 6.4 inset). This could even allow for the patterning of AE regions under resonator coupling beams, creating non-reciprocal mechanical coupling elements. These high performance AE platforms are still in their infancy, and the devices demonstrated and proposed in this thesis are just the beginning to a growing library of integrated non-reciprocal RF MEMS devices.

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