FABRICATION AND IMPLEMENTATION OF FLEXIBLE ELECTRONICS BASED ON MODERN PRINTING TECHNOLOGIES

by

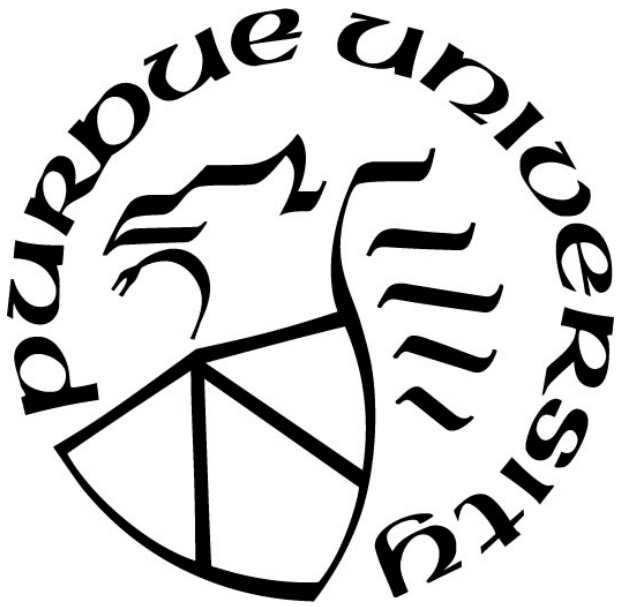
Yuhang Zhu

A Thesis

Submitted to the Faculty of Purdue University

In Partial Fulfillment of the Requirements for the degree of

Master of Science in Electrical Engineering



School of Electrical and Computer Engineering

West Lafayette, Indiana

May 2021

THE PURDUE UNIVERSITY GRADUATE SCHOOL
STATEMENT OF COMMITTEE APPROVAL

Dr. Saeed Mohammadi
School of Electrical and Computer Engineering

Dr. Sunil Bhave
School of Electrical and Computer Engineering

Dr. Ali Shakouri
School of Electrical and Computer Engineering

Approved by:
Dr. Dimitrios Peroulis

ACKNOWLEDGMENTS

First and foremost, I would like to express my sincere gratitude to my advisor, Dr. Saeed Mohammadi, who offered me the best opportunity for studying in one of the best university and doing research in my beloved area. His vision, enthusiasm, motivation have deeply inspired me.

I am extremely grateful to all my friends, for all the hard time we went through together and for all the fun we had. I could not imagine how hard the life would be if without them. I thank all my fellows teammates: Nojan Aliahmad, Shabnam Gohotbi, Nathan J. Conrad, John S. Peterson, Hengying Shan, Abdulrahman Alghamdi and other who we had worked together. Thank you for your patience and valuable guidance. I am overwhelmed in all humbleness and gratefulness to acknowledge my depth to all those who have helped me in my life.

Finally to my parents, who support me unconditionally at anytime. Although there are thousands miles between us, your love, your support gives me courage to cross through any difficulty. Love you.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

In the last decade, the information technology industry shifted its focus from personal computing devices to mobile computing devices. The benefit offered from information technologies is more accessible than ever. In recent years, mobile computing devices have been developed further due to the high-demand from the market. The trend has led to the evolution of mobile computing devices, with huge diversification towards wearable devices, implantable devices and flexible electronics. Aligned with such applications, this thesis focuses on flexible electronics and its fabrication technologies.

In this context, several implementations are demonstrated. The first is an integration technology for embedding conventional rigid components and conventional chips into flexible substrate and using modern printing technologies to integrated the circuit with other components. The prototype exhibits good performance for dc and high-speed ac signals. It also shows outstanding flexibility, good durability and reliability. The fabrication process is simple and is designed to suit large-scale manufacturing processes.

Next, a thin-film field-effect transistor technology using solution-based materials has been demonstrated. The materials used for the technology show excellent performance despite being implemented with solution-based techniques. Advantages of these materials and their potential for flexible electronic applications are explored. The materials have been process using a unique fabrication method, which may lead to low cost high performance and reliable flexible electronics.

1. INTRODUCTION

1.1 Introduction to Flexible Electronics

Conventional electronic components, such as capacitors, diodes and integrated circuits, are generally fabricated by thick rigid materials. Therefore, they are usually fragile to mechanical stress. Once the stress exceeds the limit, permanent damage will be done to the component. On the other hand, flexible electronics can be folded, twisted or rolled. Because of the nature of flexible electronics, they can be designed to be thinner, smaller, lighter and more robust against mechanical stress.

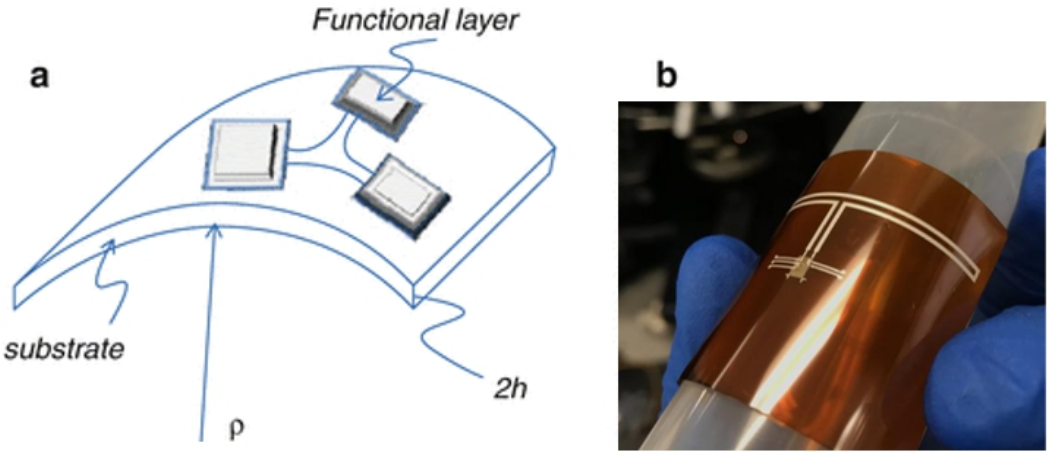


Figure 1.1. (a) A schematic of the structure of flexible electronics; (b) A printed circuitry on flexible substrate [1]

A typical flexible electronic includes three elements - a flexible substrate, one or more functional layers and the interconnection between the functional layers:

1. Substrate layer

a) Flexible substrate

b) Stretchable substrate

c) Transparent substrate

d) Textile substrate

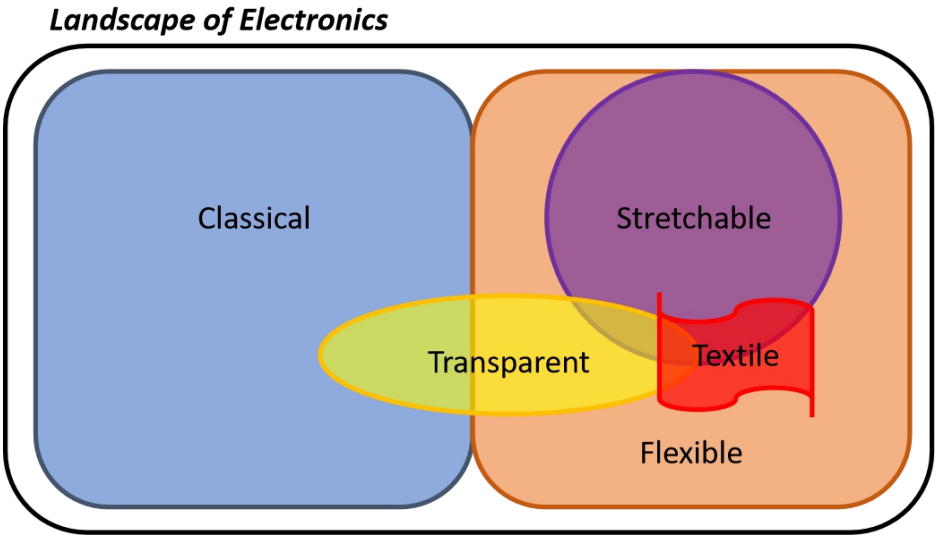


Figure 1.2. Landscape of electronics which has been invented until today. Stretchable electronics, textile electronics and transparent electronics are subset of flexible electronics.

2. Active layer

a) Classic component

b) Thin-film device

3. Interconnection

“Almost three quarters of internet users will access the web solely via their smartphone by 2025, equivalent to 3.7 billion people.” according to a report published by the World Advertising Research Center (WARC). Driven by this rapidly growing population of mobile devices and even urged by the refreshing rate of the mobile devices industry, there is a huge demand for novel technologies to push the industry forward. Flexible electronics is the supernova in this area, not only because it has large potential to break the barrier of current technologies, but also, it has a board-less range of application in the industry.

The application in the display sector is one of the most developed areas for flexible electronics. Highly demanding technologies, such as LCD, AMOLED [2], [3], [4], have been demonstrated in the

last two decades. In recent years, foldable displays have also been commercialized successfully on some mobile phones by companies like Samsung Group, Sony Corp. and LG Electronics.

In the healthcare and human-interface area, a single-pixel wireless contact lens display was demonstrated in 2011 [5] and later the concept to a glucose-sensing contact lens for the diabetic patients was developed by the same group [6]. Although the project was dropped due to insufficient consistency in the measurements of correlation between tear glucose and blood glucose, the demonstration attracted numerous attentions from researchers all over the world. Taking advantage of soft and biocompatible materials, flexible electronics show incomparable wearing/deploying comfort and excellent electrical performance. Continuous real-time healthcare monitoring can be achieved by using these wearable or implantable devices in a comfortable manner. They usually collect human-metabolic data from liquid media such as saliva [7], tears [7], [8] and sweat [9], [10], [11], [12].

Continuously evolving advances in thin-film materials and devices have given more capacity to develop much advanced flexible electronics than ever. Flexible microprocessors with two-dimensional semiconductors have drawn attention from researchers and the public. A 1-bit implementation of a microprocessor using a two-dimensional semiconductor has been demonstrated. Chemical vapor deposited (CVD) molybdenum disulfide was chosen as the semiconductor material. As a result, the group demonstrated the feasibility of using 2D semiconductor to construct complex large-scale circuits. [13]

The global market value for flexible electronics was around $5.3 Billion in 2015. Based on the statistical study, a prediction says that the market size of flexible electronics is growing at a compound annual growth rate (CAGR) of 20% from 2015 to 2024. [14] Flexible electronics which has been called as a next generation ubiquitous platform, has already attracted the attention of many researchers and it will develop faster by riding the trend of this rapidly growing mobile devices and internet of things (IoT).

Despite the achievement in research, few flexible electronics projects have been successfully commercialized. To match the performance of rigid electronics and to maintain the applicability of the flexible electronics, the use of exotic device architecture and novel material are unavoidable. According to the current manufacturing method, which is well developed for conventional electronics for over half a century, the financial benefit of electronics is buried unless the adjustment could be done by

manufacturers for fabricating flexible electronics. Secondly, mechanical stability is still the biggest concern for commercializing most of the past projects. Electrical performance degradation with bending still dominates the lifetime of these devices. Fortunately, novel integrating methods that improve the bending stability and reliability have been introduced.

In summary, financial cost, performance stability and yield coefficient are the major challenges, which impeded the progress of commercialization of the flexible electronics. However, successful commercialization of a few flexible electronic technologies are proving that the challenges are not impossible to solve. Like integrated circuits gradually took the place of discrete circuits, once the technologies are mature, the flexible electronics may bring a next revolution to the electronics industry.

1.2 Introduction to Printed Electronics

Following the booming development in flexible electronic technologies, the printing technologies also gathered attention from researchers and manufacturers. It is obvious that the development of printing technologies is closely related to the development of flexible electronics. Modern printing technologies offer the best cost and fabrication efficiency, low temperature operating process and excellent printing quality. Therefore, printing technologies are the key to the success of the mass production of flexible electronics.

Printing electronics is not a new idea, and a patent for “Printed Wires” was filed in 1903, which represents the earliest concept of printed electronics. Later on, Paul Eisler produced the first printed circuit and it was immediately adopted for large-scale radios during World War II. Since then, the printed circuit board, as on the most representative of printed electronics, has been embedded in every aspect of our daily lives.

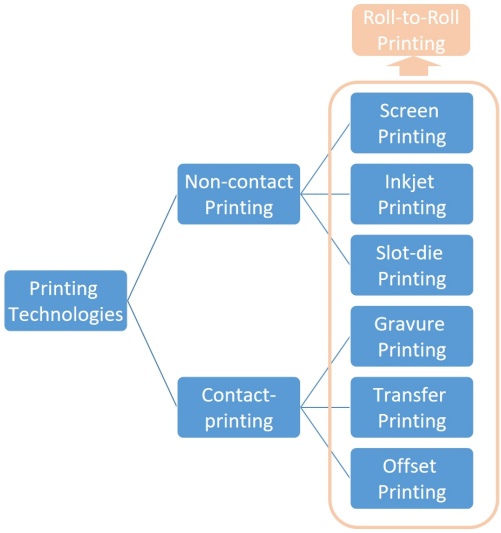


Figure 1.3. Categories of commonly used modern printing technologies [15]

Printing technologies can be roughly divided into two categories: non-contact printing and contact printing. In contact printing, a pre-patterned mold brings ink (or solution) and transfers the ink to the substrate by physical contact. The advantage of this printing approach is that the printing process completed once the mold has contacted the substrate. Aiding by the ink feeding system, the contact printing system can constantly print high quality stable features with very high fabrication efficiency. This feature makes contact printing become the best solution of large-scale production.

The approach of non-contact printing usually uses nozzles to dispense functional ink onto substrate or force the paste through the opening apertures to form the patterns. During these printing processes, there is no rubbing or pressing applied onto the substrate except for the gravity force from the dispensed ink or paste, such that the printing process does not disturb or damage the delicate material and structure that is already on the substrate. Inkjet printing and screen-printing are two typical printing technologies of non-contact printing.

a) Screen printing

Screen-printing or stencil printing is commonly used in the textile industry for printing on clothes. Due to the simple operation process of this technology, manufacturers have started to adopt this printing technology to print electronics. A conductive ink is often used for printing. There are two major components that are required to complete a print - a stencil with pre-defined configuration and a

squeegee set above the stencil. While printing, the squeegee press against the stencil and the horizontal movement of the squeegee moves the paste across the stencil. During this movement the paste is pressed through the pre-defined apertures in the stencil and transfers the paste onto the substrate.

Screen-printing is well developed in traditional industries. Screen-printing equipment usually costs less than other kinds of printing machines, due to its simple structure. The stencil can be used repeatedly. If the setting is correct, the printing quality can be guaranteed during the lifetime of the stencil. Thus, the benefits of its low initial investment, low maintenance cost, high production efficiency and high-quality stability make this technology one of the best candidates for large-scale manufacturing of printed electronics.

b) Inkjet printing

Inkjet printers are used to reproduce the digital configuration on substrates by dispensing ink droplets onto the substrate. Basically, inkjet printers can be classified into two types, namely continuous inkjet printing (CIJ) and drop-on-demand inkjet printing (DOD).

In the continuous inkjet printing as its name says, there is a stream of ink droplets recycling continuously inside the printhead. Only the particular droplets will be deflected out of the stream and printed onto the substrate. To realize this, ink is pressurized and directed to a microscopic nozzle. Controlled by a characteristic signal, a piece of piezoelectric material at the nozzle regulates the ink to form droplets when the ink is dispensed out of the nozzle. While the droplets pass through the first electrode, some of them will be charged. The charged droplets deflect at the second parallel plate electrodes due to the electric field. The deflecting angel can be controlled by the amount of charge. Depending on the design, the deflected droplets will dispense onto the substrate and the un-deflected droplets will be recycled to the ink reservoir or vice versa.

In drop-on-demand inkjet printing, the ink droplets are pressed out only when it is needed. To realize the DOD printing, the ink is transferred to a small chamber inside the printhead from the ink reservoir. By temporarily changing the pressure inside the chamber a droplet can be fired from the nozzle. There are two major methods to generate the rapid pressure change. The first one is to heat the

ink inside the small chamber. The heat causes vaporization and pushes the ink out of the nozzle. The second method is to use piezoelectric material to push out the ink from the nozzle. The piezo DOD is more popular and advanced than thermal DOD since it has less restriction for the ink.

Compared to traditional continuous inkjet printing, drop-on-demand printing provides higher printing resolution. The advantage of continuous inkjet printing is that the clogging issue happens less often than drop-on-demand technology during the printing, higher viscosity ink is allowed in continuous inkjet printing. However, new types of continuous inkjet printing have been recently introduced. Examples include aerosol inkjet printing (AIJ), and electro-hydrodynamic inkjet printing (EHD), which have further pushed the limits and resolution of continuous inkjet printing [16].

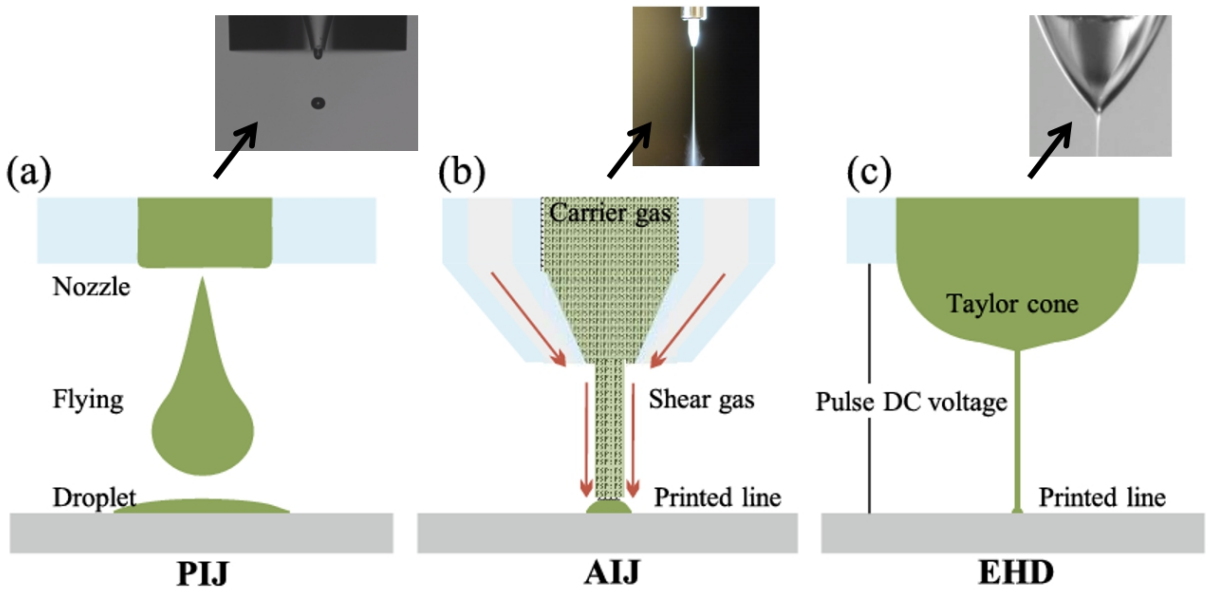


Figure 1.4. Three types of inkjet printing technologies: (a) Piezoelectric inkjet printing. (b) Aerosol inkjet printing. (c) Electro-hydrodynamic printing. [17]

Besides the evolution of printing technology, various kinds of printing inks have evolved and contributed to the growth of printed electronics. Nowadays, one can fabricate complex electronics from bottom to top only by printing (and the post-process of each layer). There ink is composed of two parts: solvent and solute (or suspension). The physical properties, such as printability and flexibility of the ink deposition are directly related to the composition of the solvent. On the other hand, the electrical performance, such as conductivity and dielectric constant, is closely related to the solute (or the suspension). However, the final result also depends on the fabrication process.

Parameters such as viscosity, volatility, material and solvent compatibility with the underlying materials need to be considered when selecting or synthesizing the proper ink for different printing technologies and particular fabrication processes. For example, DOD inkjet printing requires low viscosity ink for the proper droplet formation at the nozzle; screen-printing, on the other hand, requires high viscosity ink to achieve the desired printing uniformity. Not only the physical property of the printed material, but also the electrical performance of the finished devices can be tuned while synthesizing the ink. An example of doping the solution-based indium zinc tin oxide semiconductor with gallium (paper) shows a significant reduction in turn-on voltage. According to their functionality, the inks for printing electronics can be classified into one of these categories in general: conducting materials, semiconductor materials and dielectric materials.

The conducting material is the skeleton of the electronics device. It conducts electricity signals across the device structure. A proper printed pattern can also be used as an antenna to transmit or receive signals [6], [7], [10], [13]. Silver nanoparticle ink is one of the most popular inorganic ink for conducting material due to its high conductivity, low oxidation rate and lower cost compared to gold nanoparticle ink. Alternatively, PEDOT:PSS is an organic material that is often used as a conducting material. Although the conductivity is lower than nanoparticle inks, it has good printability due to its excellent flexibility and transparency, and is widely used in transparent flexible electronics.

The semiconductor material is the fundamental of building complex electronics devices like memories, sensors and microcontrollers. The traditional semiconductor devices are fabricated on bulk semiconductor by dedicated metallization and doping processes. Following Moore's law, the transistors (and other components) have become more and more compact on Si wafers. As of 2017, manufacturers can pack more than 100,000,000 transistors in each square millimeter of the chip [17]. No matter how compact the traditional semiconductor technology is, it only utilizes a thin layer of material on the top of the wafer to construct the devices. The rest of the material on the wafer is wasted. Instead of using a piece of bulk material, printing semiconductor material on a cheap substrate, right on the demanded area can significantly reduce the material waste. In addition, one may manage the dopant of the printable semiconductor material by simply changing the composition of the semiconductor ingredient while preparing the precursor. Compared to the doping process of traditional semiconductor fabrication (ion implantation or diffusion), tuning the dopant of printable semiconductor materials is simpler and much more affordable. Many works have proved that it is possible to achieve the printed semiconductor with

as good performance as the traditional semiconductors by a well designed and fabricated process [18], [19].

Many printable dielectric or the passivation materials have exhibited outstanding performance either for electrical or physical passivation purposes. For electrical passivation purpose, in addition to the financial and simplicity advantage of printing technology, the novel printable dielectric materials have demonstrated much higher performance than the dielectrics in traditional processes, such as silicon dioxide and silicon nitride. Sol-gel processed amorphous metal oxide materials are one category of printable dielectric materials. Many compositions have been explored by researchers, such as aluminum oxide [20], [21] zirconium dioxide, [22], [23] titanium dioxide [24], and yttrium oxide [25]. To achieve better performance from a transistor, high-$\mathcal{K}$ dielectric is more favorable for the gate dielectric. It provides higher gate capacitance without thinning the gate dielectric, higher drain current without the spiking in the gate leakage current. Printable dielectric materials have been reported having much higher dielectric constant than traditional dielectrics. Printable organic materials are also widely used as good dielectrics in printed electronics. Their good chemical resistance, high printability, excellent flexibility and low cost make them also suitable for physical passivation to protect the fragile electronics from environmental impacts.

1.3 Project Description and Thesis Outline

This research focuses on developing fabrication processes of micro-electronic systems with cutting-edge technologies and studying the performance of the integration to optimize the fabricating solution. In the dissertation, a comparison of laser cutting technologies, printing technologies, flexible substrates, amorphous metal oxide semiconductors etc. are presented. The performance of devices made with each technology are demonstrated and an optimized fabrication solution for each technology has been proposed.

The organization of the rest of the dissertation is as follows: Chapter 2 presents the method of embedding silicon die into a flexible substrate and the method of integration. Laser cutting technology is utilized to prepare the substrate and several printing technologies to make the die to substrate interconnections are proposed and compared in this chapter; Chapter 3 proposes the solution-based amorphous semiconductor and dielectric thin-film transistors. The investigation on the dielectric and

semiconductor materials by fabricating and characterizing, metal-insulator-metal structure and the thin-film transistor respectively, are presented. Finally, a summary of the research, a brief discussion on the potential of the proposed technologies and possible improvements for the future research are presented.

2. A METHOD OF INTEGRATING SILICON DIE IN FLEXIBLE SUBSTRATE

2.1 Introduction

The definition of flexible hybrid electronics is very similar to flexible electronics; it can be folded, twisted or rolled, except that some of the components are rigid or not fully flexible. The body of the flexible hybrid electronics is a combination of rigid and flexible building blocks and this is where the word “hybrid” comes from. Though the device contains rigid components, it as a whole, is flexible. The performance of a good flexible hybrid electronics device should be identical while relaxing, flexing or after flexing. In practical terms, the surface mount devices (SMD) are the most rigid components on the flexible hybrid electronics devices. These surface mount devices include packaged integrated circuits (IC), resistors, capacitors, crystal oscillators and physical connectors.

The idea of flexible hybrid electronics is very simple. It uses the same structure as the electronics devices based on the printed circuit board: The core of a PCB is a piece of non-conductive substrate. It provides mechanical support. Copper sheet is laminated on the single side or both sides (for multi-layer PCB the inner copper layers are sandwiched between the substrates). By etching or milling the copper, one can construct the conductive tracks, pads, through holes and other features to provide the electrical connections. Before the existence of the PCB, wire wrapping (Figure 2.1. (Top left)) was one of the most popular methods to make connections among different components. Though it didn’t require any layout design, wire wrapping of discrete components must be done by hand soldering. Because of the loose parts in the wire wrapping system, it was usually vulnerable to human mistakes and difficult to test. On the other hand, the components on PCB (Figure 2.1. (Top right)) are securely fastened on metal contact pads by solder so that the connections are strong and reliable. Large-scale production is much easier using PCB. Fabricating PCB, placing components and soldering, are the three major processes to complete a PCB circuit. Every step in the process can be fully automated. Thus, PCB circuits are much more practical in large-scale production. More importantly, PCB circuits are robust and reliable. They have less performance variation thanks to the fully automated fabrication process. Due to all the benefits above, PCB circuits have dominated the electronics’ packaging area since they were invented.

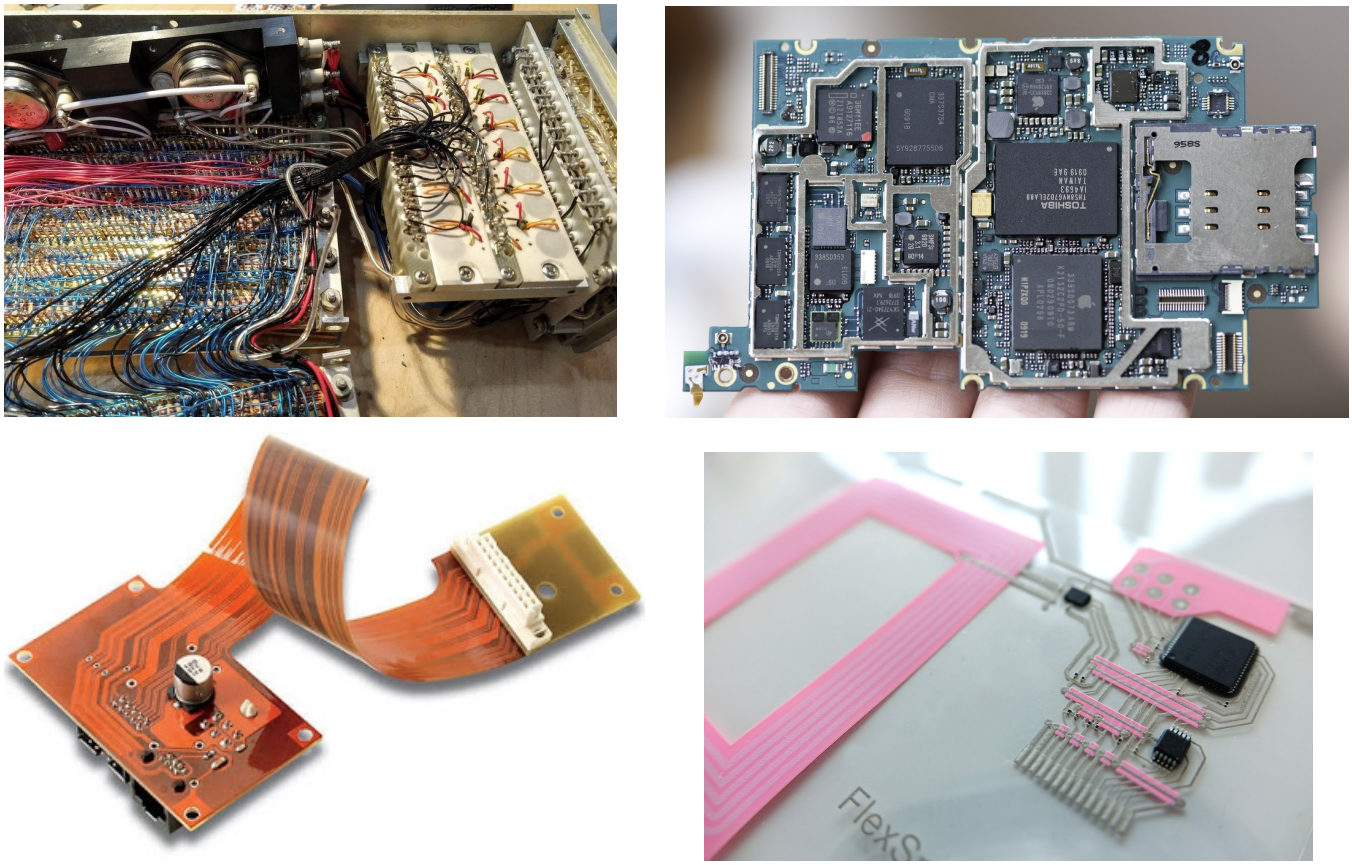


Figure 2.1. (Top left) Part of the circuitry of the Apollo Guidance Computer which helped the spacecraft navigate to the Moon and land on it. The components were connected by wire wrapping. (Top right) A motherboard PCB of a smartphone (Bottom left) A PCB with FPC ribbon cable on the right (Bottom right) A hybrid flexible circuit

Just like the PCB, the flexible printed circuit (FPC) (Figure 2.1. (Bottom left)) is made by the same fabrication process as the traditional PCB as it was described above, although it uses flexible plastic, for example polyethylene naphthalate (PEN), polyimide (PI) and Polyethylene terephthalate (PET), as the substrate instead of a rigid substrate.

Take one more step forward, the flexible hybrid electronics (FHE) (Figure 2.1. (Bottom right)) use not only flexible substrates but also utilize modern printing technology. Conductive interconnections, and as many components as possible are printed onto the flexible substrate. Any kind of non-printed components are able to be placed and mounted on the substrate after printing. This combination of flexible substrate, cutting-edge printing technology results in a lighter, more flexible and more reliable system than any form of electronic circuits which have already existed.

Because of the domination of PCB circuits, the packaging of most of electrical components is designed to assemble onto the PCB. Modern semiconductor devices are still relying on silicon wafer which is rigid and fragile. Based on these restrictions, fully flexible devices are still far from practical as consumer-level electronics. Technically speaking, flexible printed circuit (FPC) and flexible hybrid electronics (FHE) are transition forms between PCB and fully flexible electronics. Using the existing electrical components, FPC and FHE can achieve as good performance as conventional PCB devices. Although the electrical components which are attached on the circuit are rigid, the device is still flexible enough for many applications which are infeasible with PCB devices such as implantable devices, and 'plying-up' wearable devices.

2.2 Motivation

Flexible and reliable electrical circuits with as much processing capability as conventional electronic systems are very desirable, and fulfill innovative applications that were otherwise impossible. FPC and FHE are the methods to achieve flexible electronic circuits. However, the performances of these available methods are not optimized in many aspects and more optimization and innovations are needed to achieve full capabilities of fully flexible electronic systems.

FPC relies on the subtractive manufacturing process to fabricate traces and features. Large proportion of conductive material (usually copper) is wasted though part of the conductive material can be recycled by complex chemical reaction during the waste chemicals recycling process. FPC is not compatible with the R2R fabricating process, since the traces and features on either PCB or FPC are defined by photolithography, it has to be exposed sheet to sheet. Another imperfection of FPC is caused by the tensile and fatigue properties of thin metal foil. The conductive layers on FPC are two layers of thin metal films laminated on each side of the substrate. Due to tensile and fatigue characteristics of FPC, scratching or bending may cause the failure of the device.

The traces and conductive features on the FHE are defined by printing the conductive ink on the substrate. The conductive ink is designed for flexible and stretchable devices. Usually, the conductive ink is composed of conductive nanoparticle, polymer filler and solvent. After curing, the solvent evaporates and the conductive nanoparticles are evenly distributed in the cured polymer, which forms a conductive network. Unlike the metal foils, the cured ink doesn't form into crystal form, thus it doesn't

suffer from metal film tensile and fatigue issues. However, the delamination is an unsolved issue for printed electronics. It is very common for FHE that the components delaminate from the substrate while the device is flexing. The delamination will directly cause the failure to the device.

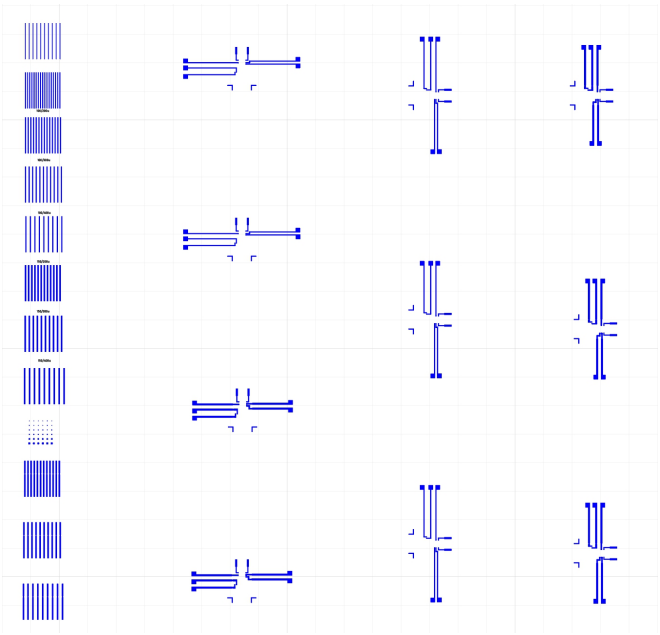
In this chapter, an innovative integration method is proposed. The method takes advantage of FPC and FHE approaches and eliminate the weaknesses of both methods. Inspired by the fabrication processes of FPC and FHE, the concept of the proposed fabrication process is similar to the existing process and all equipment used in the process is commonly adopted in industry.

Distinguishing from the FPC and FHE, this integration method: 1. Embeds components in the substrate, both FPC and FHE mounts components on the surface of the substrate instead; 2. Uses bare dies instead of packaged integrated circuits. The standard packages of ICs are bulky and rigid so they can seal the IC from the environment. To make the device more flexible, getting rid of the package is necessary 3. ICs are accessed directly by the printed traces. This innovative manufacturing process can provide a new way to fabricate electrical circuits. Our study shows that the device fabricated by this method can demonstrate similar or even better performance than current state-of-art technologies.

2.3 Fabrication

In this section, multiple approaches to fabricate flexible electronics will be presented. We will compare each approach and explain its pros and cons.

Before the fabrication, several preparations need to be done. Similar to PCB fabrication, a CAD design is required to place the components and rout the interconnections among them. This design document should content the location information of all the elements, such as traces, components, and cutting-lines. Figure 2.2 shows the CAD design of an interconnection layer. The fabrication process starts with embedding the dies into the flexible substrate. It includes the following steps: 1. Cutting the slots from the substrate for the rigid components. 2. Mounting the flexible substrate on a sacrificial layer. 3. Place the rigid components into the slots. 4. Encapsulating the device and removing the sacrificial layer (Figure 2.3). The next part of the fabrication process is to print the interconnection.



2.2. CAD design of the screen printing stencil

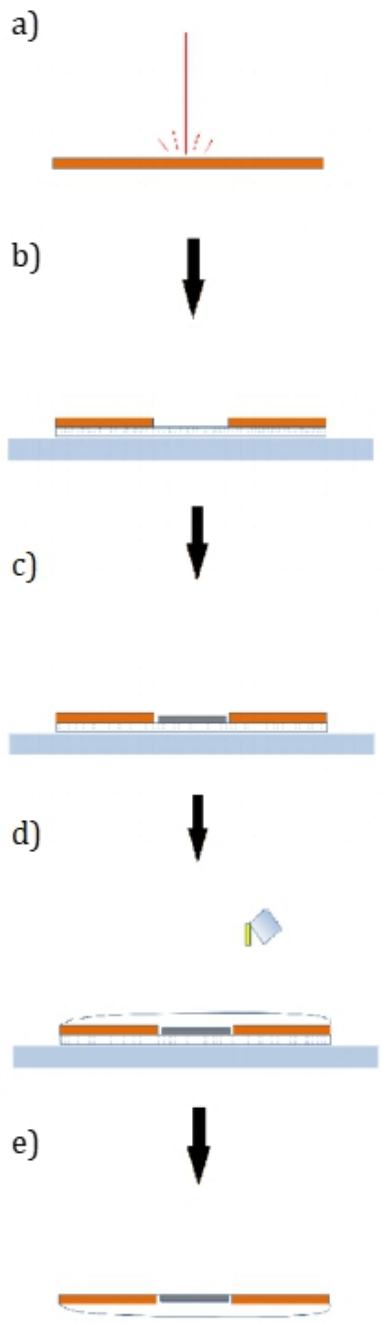


Figure 2.3. (a) Cutting Kapton by using a UV laser cutter. (b) Attaching the Kapton substrate on a carrier substrate with PDMS gel sacrificial layer. (c) Attaching the rigid components on the carrier substrate. (d) Filling the gap and encapsulating the system with PDMS elastomer. (e) Releasing the device from the carrier substrate.

2.3.1 Substrate Preparation

The substrate preparation process is the foundation of fabricating reliable and high performance devices. Figure 2.3 depicts the process flow of the preparation process. The very first step is to cut out the 'windows' from the flexible substrate for embedding the components. There are many cutting technologies. In this study, three cutting technologies were investigated: punch pressing, CO2 laser cutting and UV laser cutting.

Punch pressing was the first cutting method to be tested, it was quickly concluded that the slot cut by punch press machine did not provide flat enough cutting edges to meet the requirement for the subsequent printing step. Three phases of the punching process are shown in figure 2.4 (a) when the hydraulic punch press against the sheet, it first deforms (b) then the sheet breaks along the contour as the material under such high pressure is torn. (c&d) the punching slug is ejected from the bottom.

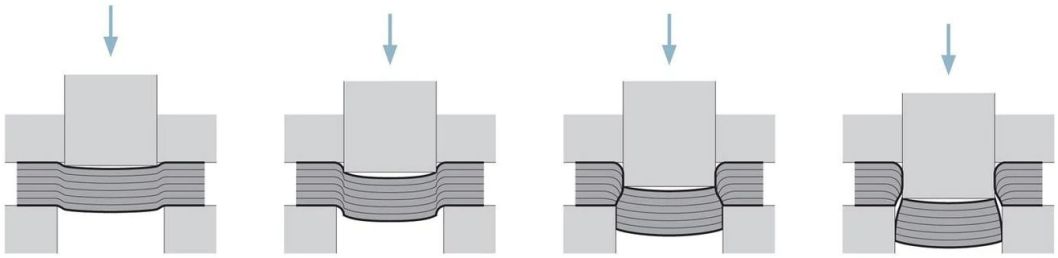


Figure 2.4. Phases of a punching process (a) Hydraulic punch push against the work-piece (b) Torn the work-piece along the contour (c&d) Eject the slug

Although the punching pressing is a convenient method to cut through the substrate, the nature of this cutting mechanism using large mechanical force to cut leaves inevitable flaws at the cutting edges. Figure 2.5 shows that the edge wraps inside the substrate after a punch press.

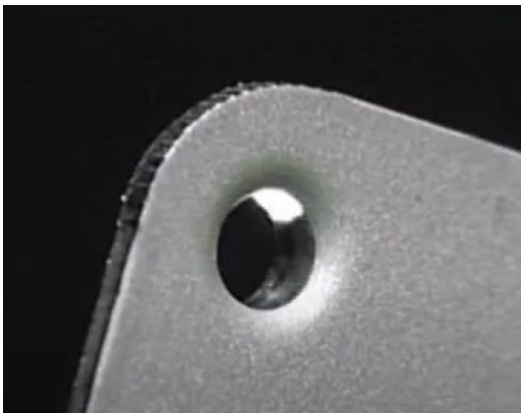


Figure 2.5. Edge-effect on a punch pressed work piece

Unlike a punch-pressing machine, a laser cutter, as known as a non-contact cutting method, does not apply any contact force for cutting the material. The wavelength of the laser affects the mechanism of the ablation. Here, two kinds of laser processing were tried and the results on Kapton substrate were compared. These two laser sources were carbon dioxide laser and ultraviolet laser.

The carbon dioxide (CO2) laser is an invisible laser with an infrared wavelength of 10,600 nm. Multiple applications of CO2 laser ablation have been reported including vitreous surgery [26], micro-structure sensor and electro-microfluidic device fabrication [27], [28], assisting drug delivery [29] and nano-scale transistor annealing applications [30]. Due to its infrared spectrum, the CO2 laser generates lots of heat on a small area of the target to cut through the materials. Theoretically, the smallest beam diameter is 10.6 μm. However, the cutting path is always wider than 10.6 μm in practical terms. Regardless of the limitation of the hardware (such as lens imperfection), the variations in the beam size and the edge roughness of the ablated area are caused by two major factors during the fabrication process. The first one is short depth of focus. One needs to accurately focus the laser beam on the surface of the material to achieve the narrowest cutting path. It is more difficult to get a clean cut if the material is transparent to IR since the light deflects from the two interfaces right after it goes into the media ((top and bottom of the flex transparent material). The deflection inside the media causes the heat generation in a larger area compared to the beam size so that the width of the cutting path is larger than the beam diameter. The second factor is that the heat may not disperse fast enough and the excess heat may melt additional material around the cutting path.

The ultraviolet (UV) laser is another invisible laser located in the ultraviolet spectrum. It provides high photon energy that can realize a wide range of applications when compared to the infrared lasers [31], [32], [33], [34], [35]. UV lasers with 266 nm and 355 nm wavelengths are the most commonly used lasers in the industry. In the cutting applications, UV laser outperforms infrared laser in general, thanks to its lower wavelength. First of all, the beam size of a UV laser is much smaller than the beam size of an infrared laser. Secondly, the UV laser offers much higher photon energy to ablate the molecular bond of the target material unlike the infrared lasers that have to rely on 'thermal processing' to do the ablation. As a result, the cut work-piece can achieve sharp edges, small heat affected zones and minimal carbonized residues.

Figure 2.6 shows the outcome of cutting a 500 um Kapton HN (DuPont) substrate by a 355 nm UV laser cutter (LPKF ProtoLaser U4) and Figure 2.7 shows the outcome of cutting the same substrate by a 10.6 um CO2 laser (Universal Laser Systems PLS6MW Multi-Wavelength Laser Cutter). The left figures are captured by a Bruker GT-K1 Optical Profilometer and the profilograms on the right are measured by KLA-Tencor Alpha-Step IQ surface profiler. It can be clearly seen from Fig. 2.6 (right) and Fig. 2.7 (right) that the CO2 laser causes a more significant heat deformation effect to the Kapton substrate. Fig. 2.6 (left) and Fig. 2.7 (left) also demonstrate the minimum beam size and cutting diameter of each laser. In this comparison, the UV laser demonstrated better cutting performance than the CO2 Laser on Kapton substrate.

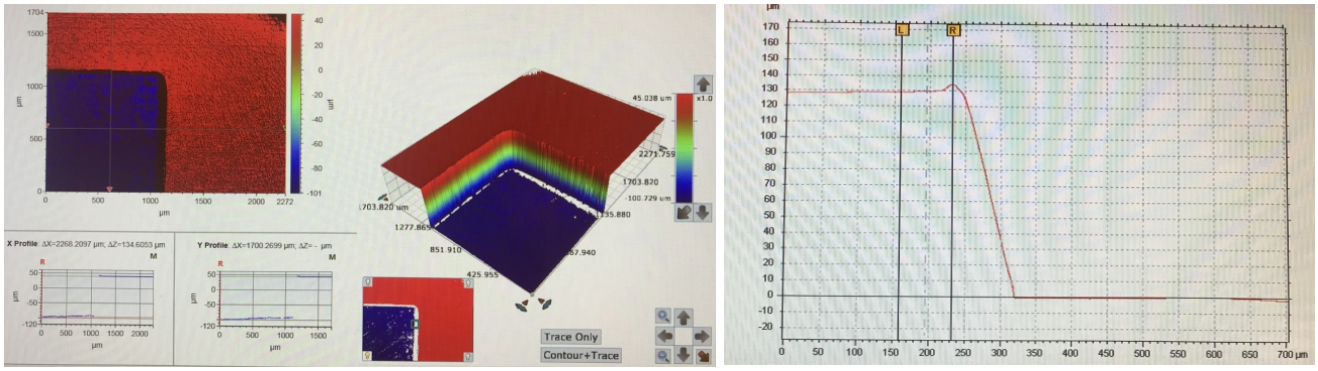


Figure 2.6. Height-profile analysis of a UV laser cutted Kapton sheet

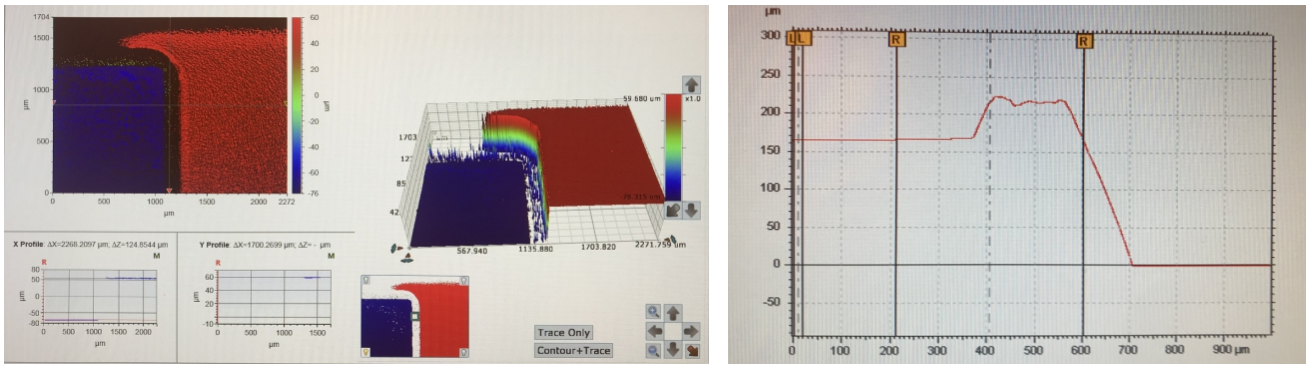


Figure 2.7. Height-profile analysis of a CO2 laser cutted Kapton sheet

The heat-treated the ablated flexible substrate is placed in an oven for 1 hour at 200-250 degrees Celsius. This process relaxed the flexible substrate, releases the stress, and heals the crinkles of the sheet and tilt at the cutting edges To securely integrate the electrical components, such as a silicon die, into the flexible substrate, both cut substrate and components need to be mounted on a flat carrier (Figure 2.3 (b)&(c)). A thin layer of adhesive layer (Dow Corning Sylgard 527 A&B Silicone Dielectric Gel) has been spun (2000rpm for 45 seconds) on the carrier. The process is followed by placing the carrier in the oven for 3 hours at 120 degrees Celsius to fully cure the silicone dielectric gel. During the curing, the flexible substrate is sandwiched between two rigid plates. Before placing the flexible substrate and components a thin layer of silicone releasing agent is sprayed on the top of silicone dielectric gel to help during the release stage. Finally the system is encapsulated by drop-casting PDMS (Dow Corning Sylgard 184 Silicone Elastomer) on the top (Figure 2.3 (d)) followed by curing the sample in an oven at 120 degrees Celsius for 1 hour. The cured sample is easy to be peeled off from the carrier.

2.3.2 Printing Interconnection

The printed interconnection will route the contact (the conductive contact on a die, an electrical component or a connector) to another contact according to the design. By printing the proper features, one can also fabricate electromagnetic components on the substrate such as antennas, resonators and filters. The printed interconnection has to be selected and fabricated properly to survive the continuous flexing of the flex substrate.

Several modern printing technologies were introduced in the previous chapter. However, for printing the interconnection on hybrid flexible substrate, two kinds of printing technologies have been

investigated: the inkjet printing technology and the screen printing technology. Both techniques will be discussed in this section and the reason why the screen printing is preferred for this application will be presented.

For the inkjet printing, a Fujifilm Dimatix DMP-2800 Series printer and a DMC-11600 Series Cartridge were used in this study. The conductive inkjet printing ink (ORGACON SI-J20X Nanosilver Inkjet Printing Ink) is supplied from AGFA. For the screen printing, a Micro Printing System Intl. TF-100 screen printer with DuPont PE873 Stretchable Silver Conductor Paste were used. The stencil was fabricated by NBC Meshtec Inc.

The reliability of the printed interconnection is extremely important. A single open circuit can cause large functional deficiencies. Research has shown that fatigue occurs in conventional metal films during bending process. Thankfully, the conductive traces fabricated with conductive ink or paste are usually flexible since the ink for inkjet printing or the paste for screen printing are usually the composite of solvents (to tune the fluid characteristics), polymer compounds and active particles (such as silver nanoparticle, gold nanoparticle or carbon nanoparticle). Unlike metal films, the active materials in conductive inks do not form a hard and stiff structure. Thus, the traces fabricated with conductive inks are less vulnerable to the mechanical stress.

Beside the general compatibility to bending, it is necessary to study printability and reliability of the interconnections at some particular places such as the surface of the rigid components and cross-interfaces between rigid components and the flexible substrate. Conventionally, these printing technologies have been applied to sheets of homogeneous substrates. Homogeneous substrates are flat, have constant thickness and are not composed of laminated various pieces of sheets. In this study, however, the printed trace will not only go across the surface of different materials, it also has to cover the height differences between the interface of the flexible substrate and rigid components. Figure 2.8 shows two traces printed by an inkjet printer. The traces were printed across the substrate – component interface. In this case, the traces were printed across (from left to right) polyimide – PDMS – polyimide – aluminum contact pad. It can be seen clearly that the traces are in good shape on polyimide and even on the PDMS interface material. The ink on the other hand is repelled from the metal pad. The repellence happens on the metal surface because aluminum has larger surface energy than polyimide and

PDMS (the surface energy of aluminum is about 1134-1160 $mJ \cdot m^{-2}$, the surface energy of polyimide is around 44 $mJ \cdot m^{-2}$ and the for PDMS is around 21.3
$mJ \cdot m^{-2}$) [36], [37], [38]. On the other hand, the traces printed by screen printing didn't have such issues (Figure 2.9). The silver conductive paste covered the desired area perfectly.

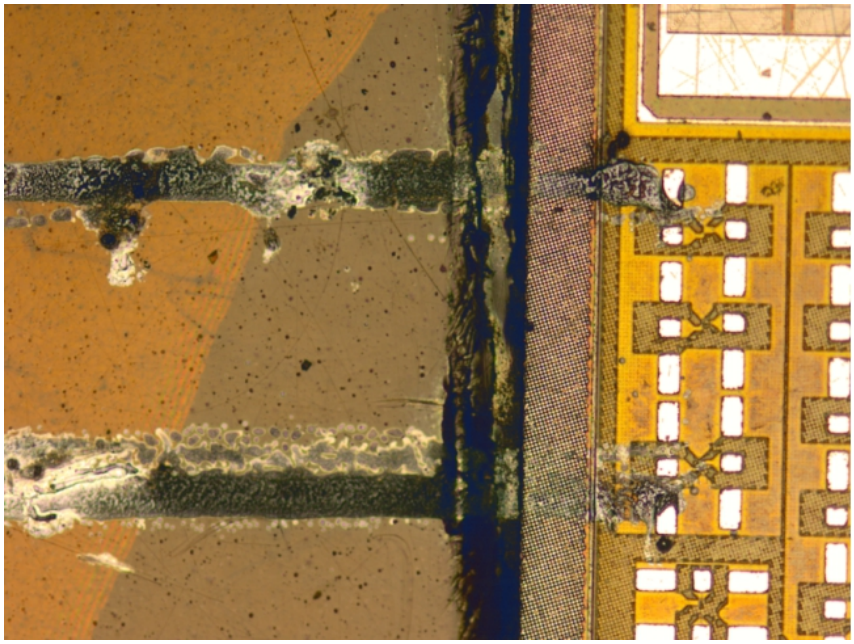


Figure 2.8. Inkjet printed traces on a die-embedded substrate

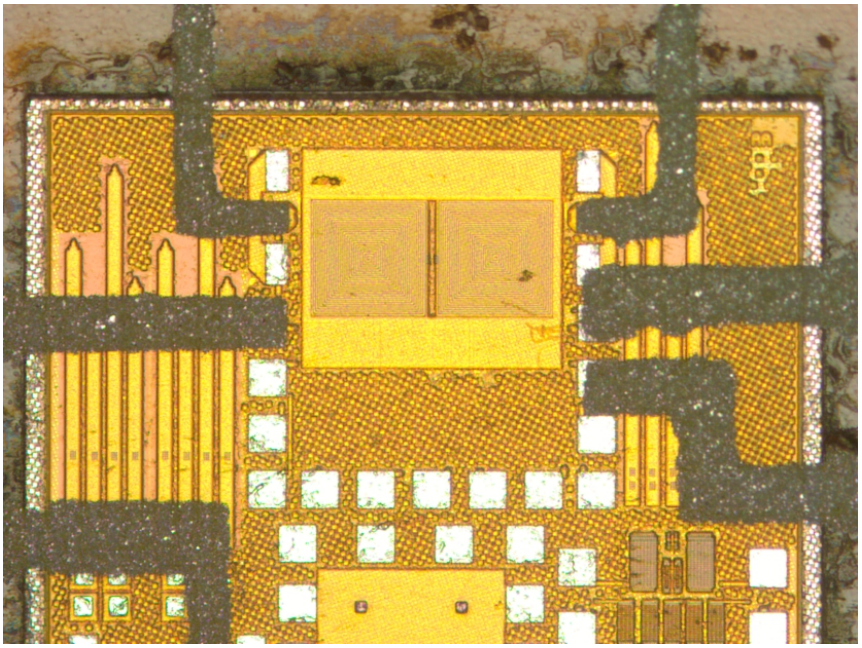


Figure 2.9. Screen printed traces on a die-embedded substrate

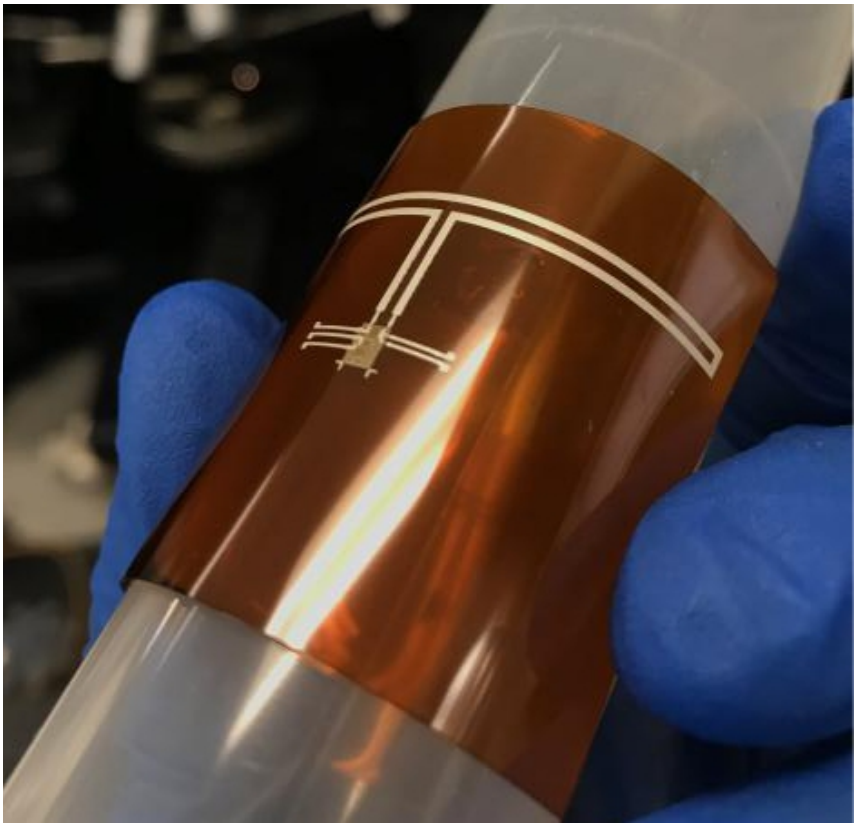


Figure 2.10. Bending the die embedded flexible system

2.4 Results

Connection between printed off-chip interconnections and a CMOS chip was fully verified by applying an external power using a source meter (Keithley 2400) and monitoring the current being sourced. The data for two different chips integrated with the flexible substrate are shown in Figure 2.11 as well as the one data point measured from the chip itself and without printed interconnects. The measurements were done by using DC probes at the appropriate pads and off-chip leads (Figure 2.12).

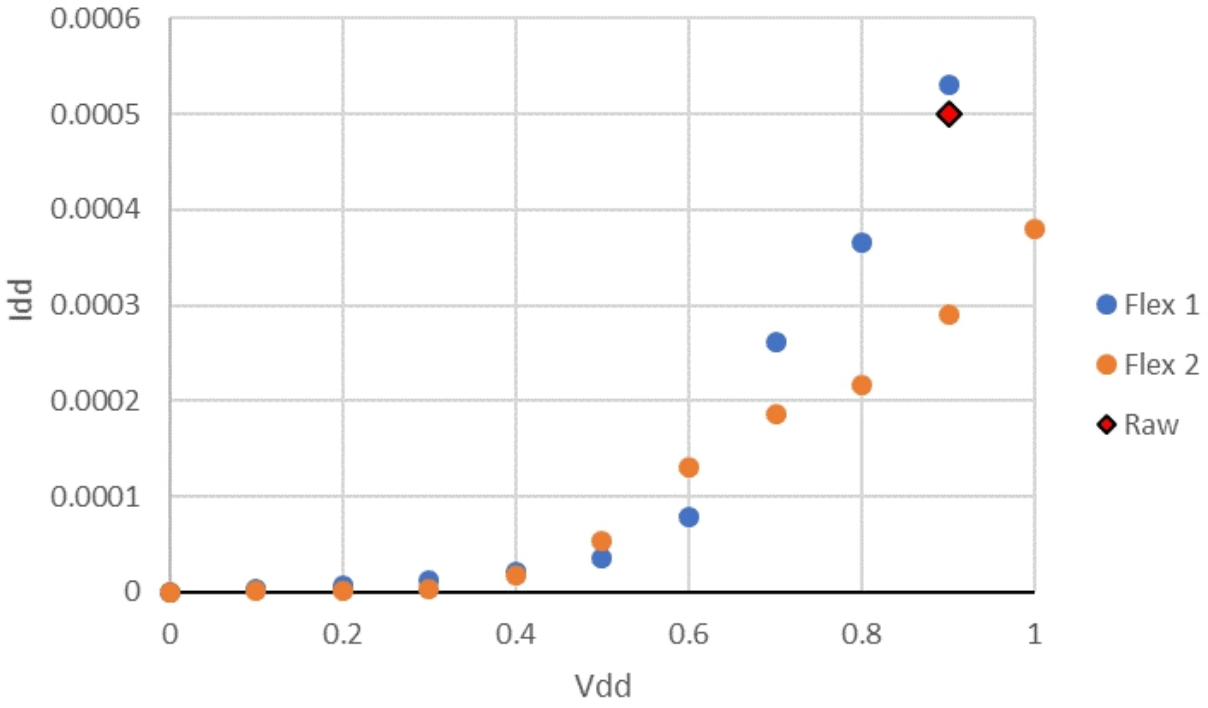


Figure 2.11. DC measurements show that the printed traces work as well as wire bond

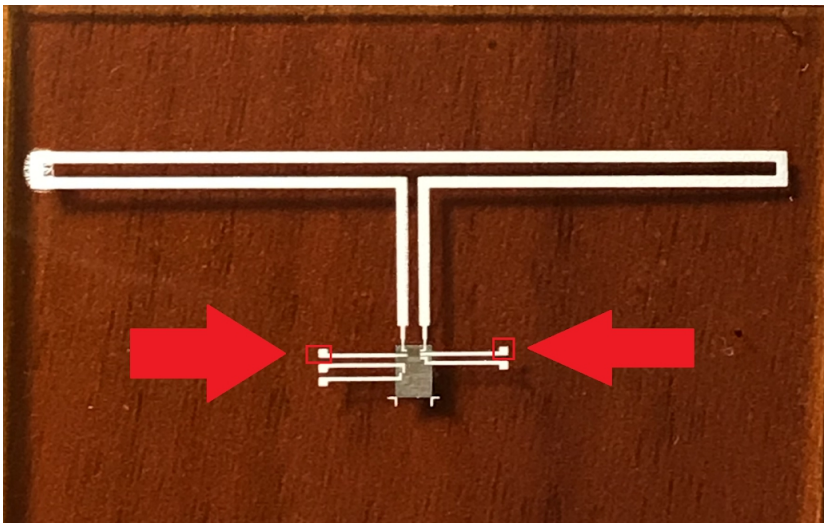


Figure 2.12. Screen printed pad extensions

Fully wireless, raw chips, no wire-bond

A fully wireless test inside a custom anechoic chamber) of both wireless chips with and without printed interconnects used as antenna were carried out. The wireless chips were designed to provide backscattering transmission when connected to an external antenna. To detect the backscattering signal, a transceiver with a cancellation chain was implemented as the Reader unit. The cancellation chain removed all leakage from the Reader transmitter to its receiver to make it easier to view the backscattered sidebands on the spectrum analyzer. Without any wiring connected to the embedded chips within the flexible substrate, the chips proved not to provide much visible backscattering. With wiring to a flexible antenna, backscattering signals with an IF measured at 7 MHz (chip clock) was measured under an external power supply of 0.9V as seen in Figure 2.13.

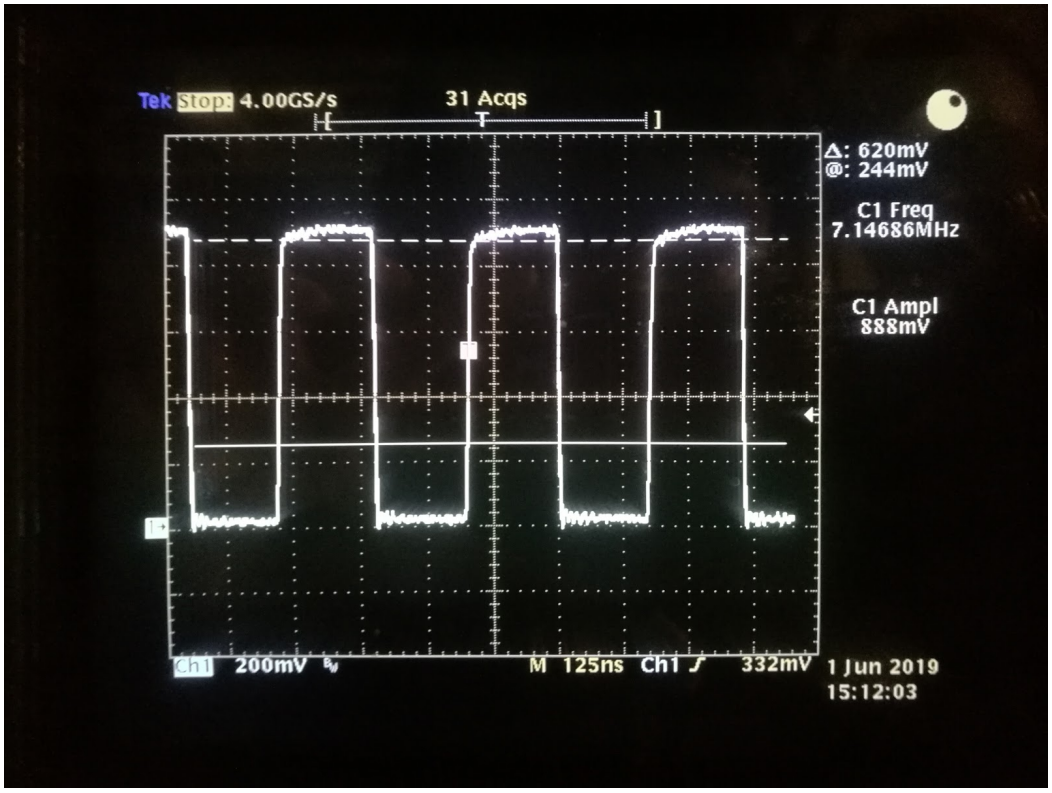


Figure 2.13. 7 MHz on chip clock signal was measured from the printed pad (CLK pad) when an external 0.9V is supplied to the chip from the printed pad (VDD pad & GND pad).

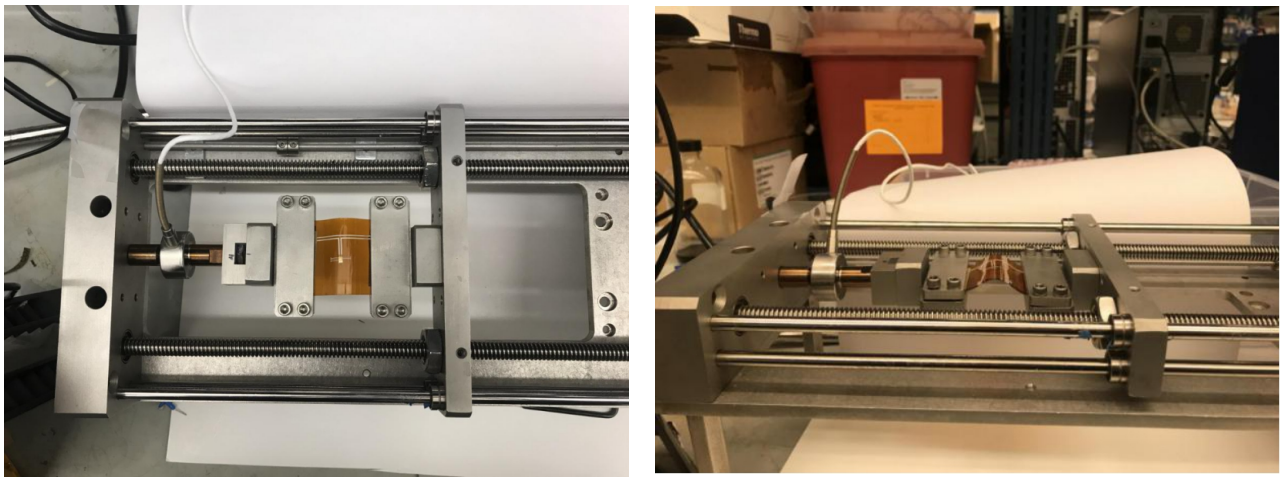


Figure 2.14. Cyclic bending setup

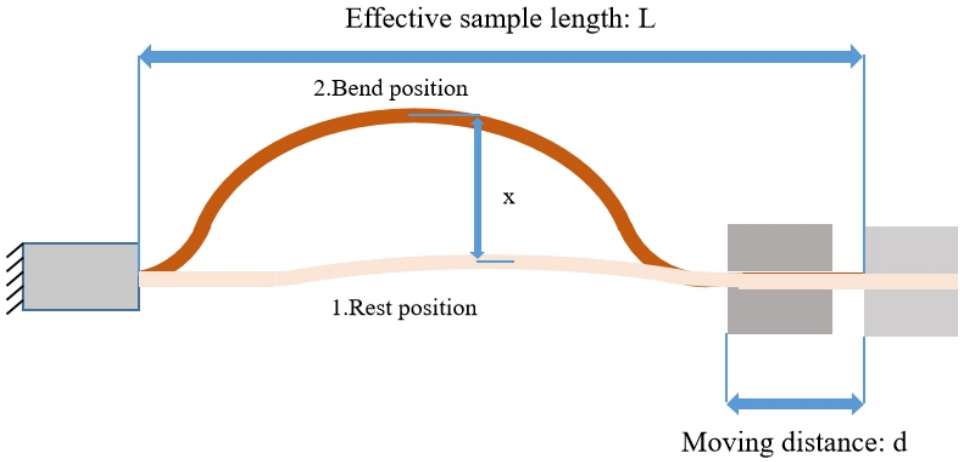


Figure 2.15. Schematic of the cyclic bending setup

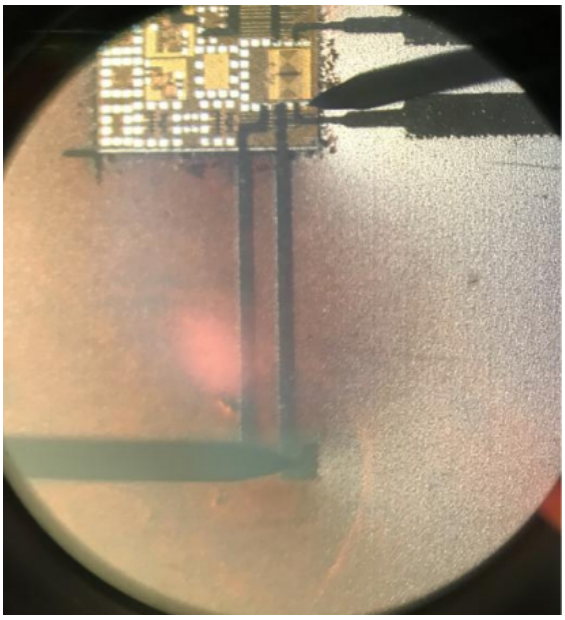


Figure 2.16. Probing the sample before and after the cyclic bending test

Table 2.1. Cyclic bending result

Cycle	Connectivity	Resistance (ohm)	Resistivity (mOhm/sq)	% of change (resistivity)	Visible damage
0	**Yes**	**0.755**	**13.48**	**0**	**No**
100	**Yes**	**0.755**	**13.48**	**0**	**No**
200	**Yes**	**0.79**	**14.11**	**25.2%**	**No**
500	**Yes**	**0.84**	**15**	**72.4%**	**No**

3. A SOLUTION-BASED AMORPHOUS OXIDE DIELECTRIC AND SEMICONUCTOR THIN-FILM TRANSISTOR

3.1 Introduction

Transistors are essential to all kinds of modern-day electronics. A transistor can amplify or switch the electrical signals. Amplifying electrical signals is one of the simplest applications of transistors in analog circuits. Providing a small signal and static power supply to a transistor, one can generate higher-power output from the transistor. In digital circuits, transistors can be used to modulate signals. Connecting transistors into a proper logic circuit, one can use the circuit to accomplish binary computations.

Before the existence of transistors, vacuum tube is the component that people used to modulate electrical signals. The vacuum tubes utilize the phenomenon called thermionic emission -thermal energy can liberate the electrons from the heated electrode; to activate an electrode (cathode), force it to emission electrons. By applying positive potential on the plate electrode (anode), electrons are attracted to the plate and current is established. Based on this design, engineers insert a control grid between the cathode and the anode so that the current flows between the cathode and anode can be controlled according to the potential on the control grid.

However, we have already known the story after. Once the transistors were out, they quickly dominated the market. The reason was very straight-forward. Transistors require much less voltage than vacuum tubes to operate, they have much lower power consumptions, they are much more durable (any air leakage in the tube will cause the failure but a transistor can easily stand for decades) and a transistor is much smaller than a vacuum tube (a modern CPU itself can easily contain over a billion transistors).

In general, there are two kinds of transistors - bipolar junction transistors (BJT) and field-effect transistors (FET). In this work, we will focus on the FETs. Similar to the vacuum tube which was mentioned above, the simplest FET also has three terminals. For FET, there is a gate terminal, a drain terminal and a source terminal. Power supply provides voltage between the drain and the source. A small signal fed to the gate modulates the current through the source and drain.

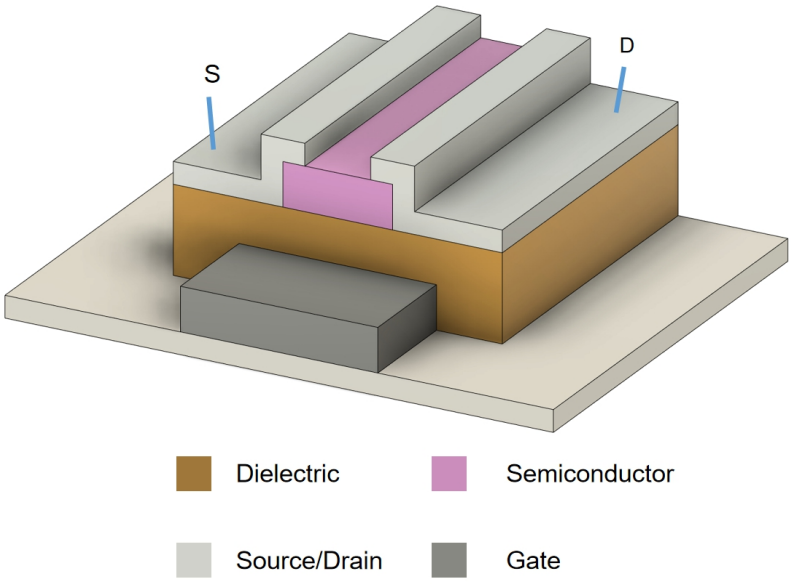


Figure 3.1. A model of a thin-film field effect transistor

Figure 3.1 shows the structure of a staggered bottom-gate thin-film transistor. It can be clearly seen that a thin-film transistor is composed by 4 components. There is a gate metal to conduct the gate control signal, a source and a drain contact to inject / draw the channel current, a piece of semiconductor and a layer of dielectric between gate and semiconductor to prevent any leakage current between them. As the main character among the components in a FET, the semiconductor determines the performance of the transistor directly. The next two sections will focus on the semiconductor. An innovative semiconductor material and its fabrication process will be demonstrated later.

3.2 Solution-Based Metal Oxide Semiconductor

3.2.1 Motivation

Undoubtedly, a good semiconductor is the fundamental of a high-performance transistor. Not any material has the semiconducting property. Besides the conventional group IV elements (Si & Ge) and III-V compounds (such as GaAs & InAs), there are also organic semiconductors (PB3T & PEDOT). Based on the morphology of the material, semiconductor material can be also classified into crystalline semiconductors, polycrystalline semiconductors and amorphous semiconductors. No matter which semiconductor is chosen, fabricating it is a complex and dedicated process. The conventional process on

a silicon wafer usually involves evaporators, sputtering machines, ion implanters and furnaces (Figure 3.2).

A convenient and economic friendly deposition method for semiconductor is always appreciated by the industry. Therefore researchers have tried different approaches and different materials associated to the fabrication method. Some notable approaches are pattern transferring [39], solution-processed amorphous semiconductor [40], inkjet-printing semiconductor [41], [42]. Solution-based method has received considerable focus. Not only because this approach is easy to accomplish. The solution-based process is highly compatible to fabricate flexible electronics and roll-to-roll fabricating process.

Figure 3.2. (top left) A Leker E-beam evaporator (top right) A Fuji200 ALD system (bottom) A PVD vacuum system

3.2.2 Indium-Zinc-Tin & Indium-Gallium-Zinc Oxide Semiconductor Fabricated by Sol-Gel Process

Apparently the conventional silicon-based electronics cannot meet the requirements of emerging technologies such as flexible displays and wearable computers. Although amorphous silicon / hydrogenated amorphous silicon (α-Si/α-Si:H) were also investigated (field effect mobility of α-Si and α-Si:H are no higher than $1\,cm^2/VS$ [43], [44], [45] and $2.7\,cm^2/VS$ [46], [47] respectively, and the carrier mobility of a solution based organic thin-film transistor (TFT) is limited to $2cm^2/VS$ [48], [49], [50], [51], [52], [53] The poor performance and insufficient reliability illustrated that they may not be capable in practical applications. On the other hand, the amorphous oxide semiconductor (AOS) has gained a lot of attention from the researchers and was expected as the best solution for the new challenges.

In this work, two novel materials are exhibited. The amorphous indium-zinc-tin oxide (α-IZTO) and amorphous indium-gallium-zinc oxide (α-IGZO) were synthetized by sol-gel process from their precursor solution. To demonstrate the performance for these innovative semiconductors, staggered style bottom-gate TFTs (Figure) with IGZO and IZTO were fabricated on silicon wafers (with 1 wet oxide) and characterized.

The fabricating process (shown in Figure 3.3) is simple and convenient due to the solution-based semiconductor fabricate process. The detail fabricating recipe is provided in Appendix A.1 and A.2.

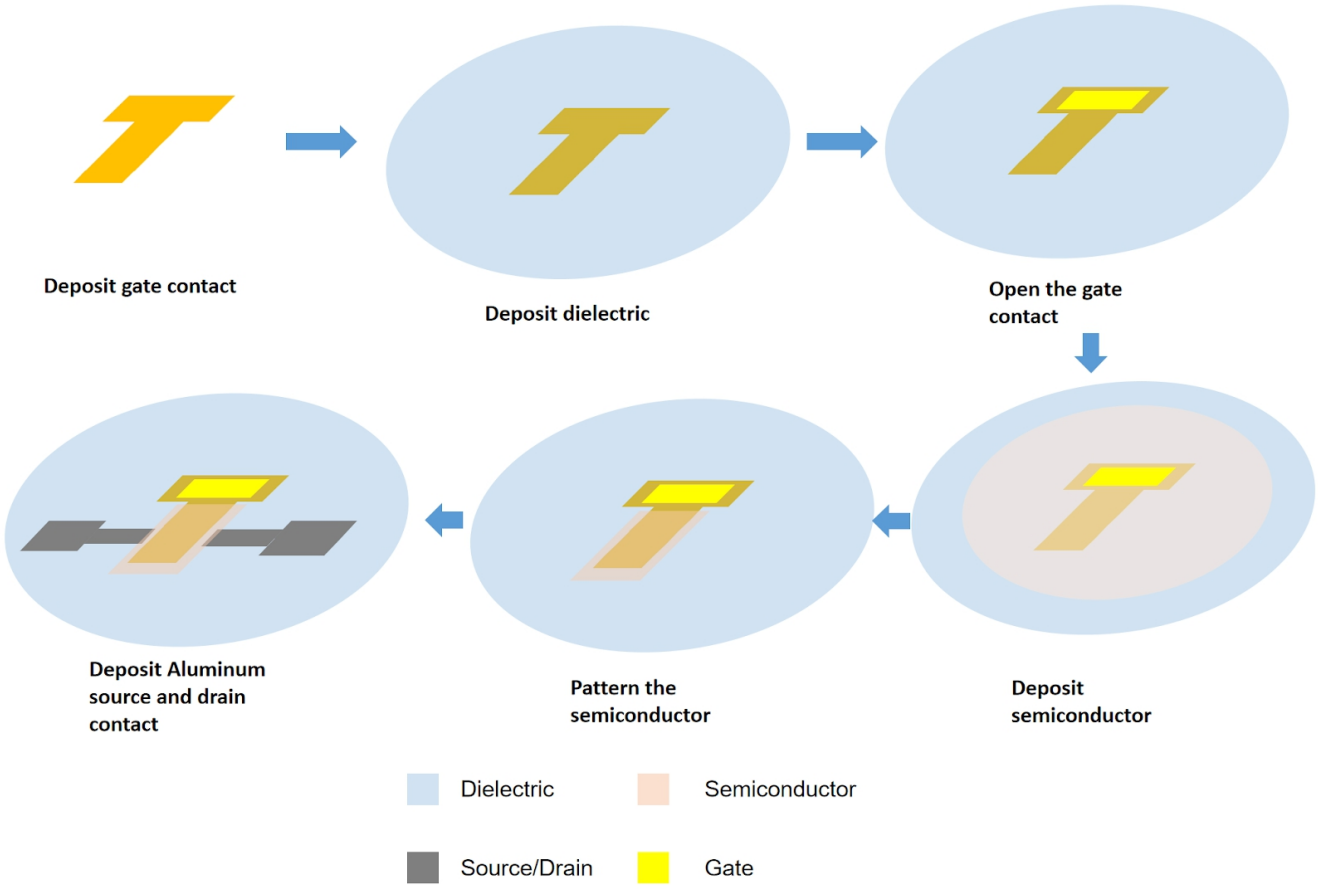


Figure 3.3. Demonstration of the fabricating process of the staggered bottom-gate TFT

In this study, heat treatment is the only external energy we had applied to accomplish the sol-gel process (synthesized the AOS from their precursor) through there are various indirect methods which can sufficiently aid the synthesis. The indirect methods include self-combustion [54], Laser locally annealing [55], [56], microwave annealing [57] and UV irradiation. In the next section, we will demonstrate the samples of UV annealed zirconium oxide and study the effect of different synthesis methods.

With various sol-gel methods that may be used to synthesize the desired film, the mechanisms to achieve semiconducting film are similar (Figure 3.4). During the annealing process, the external energy breaks the hydroxyl groups. The liberated hydroxyl groups react with each other or any released group and generate H2O, CO2, H2, and escape from the film. Concurrently, the empty bond from the metal ion catches another empty bond from its neighbor and forms into either metal-oxide-metal networks (M-O-

M), metal-oxide compounds (M-Ox) or metal-hydroxyl compounds (M-OH). Eventually, most impurities will reform into M-O-M since this form has the lowest binding energy if enough energy was supplied. [58]

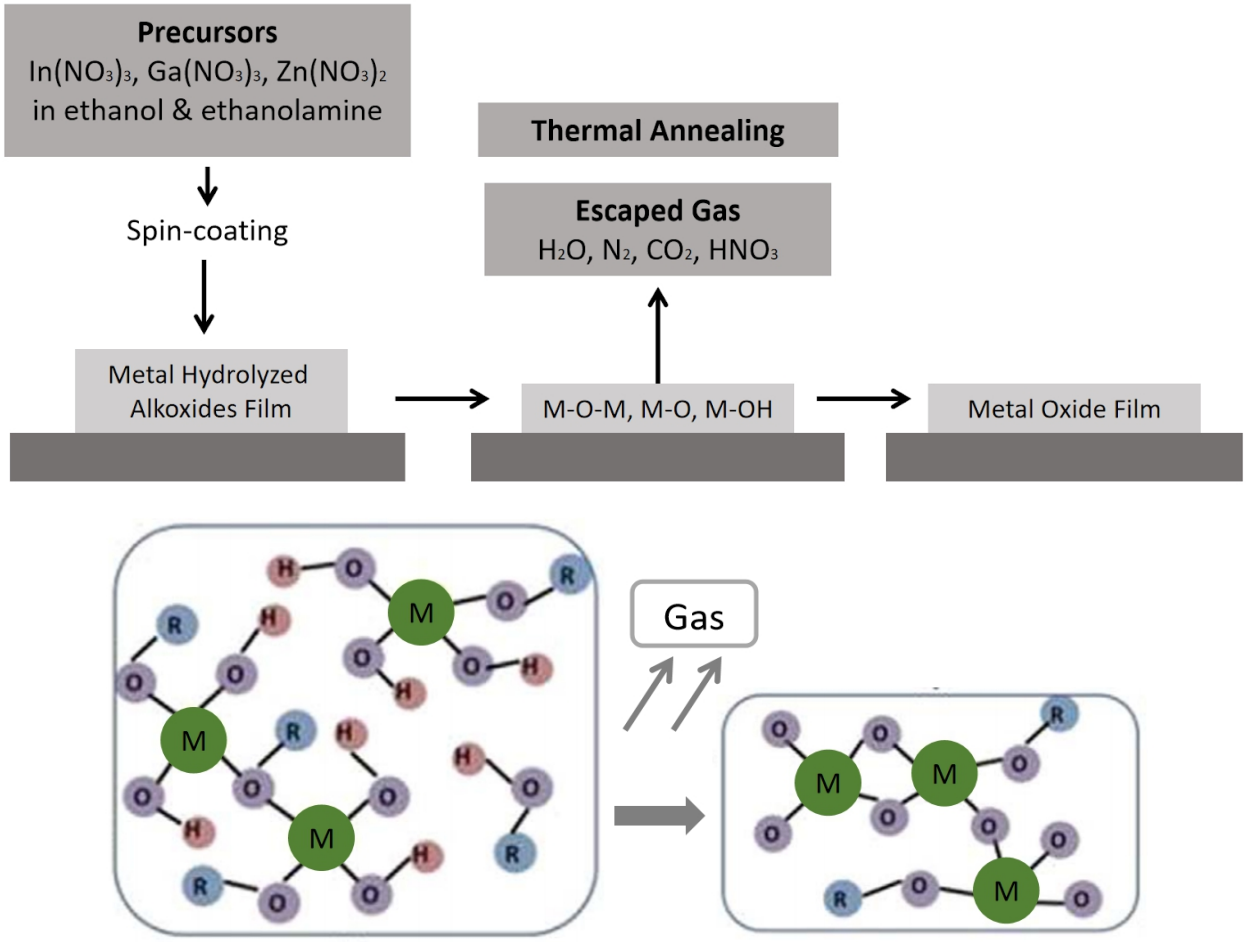


Figure 3.4. Film formation (Top) Mechanism of sol-gel α-IGZO (Bottom) Chemical reaction

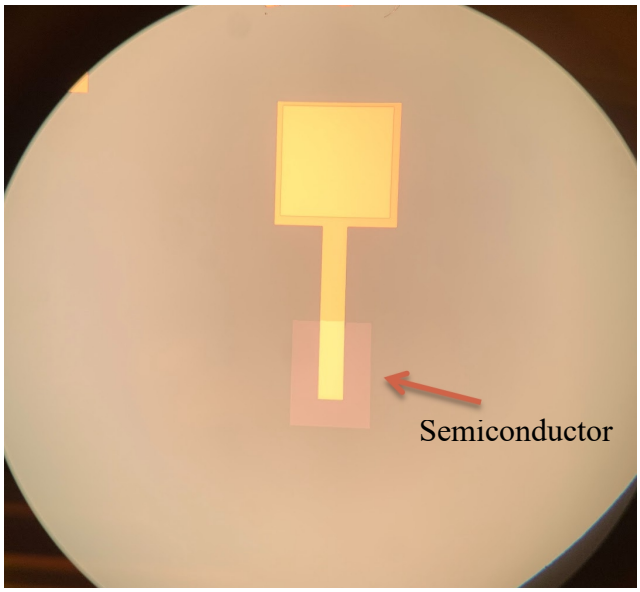


Figure 3.5. A TFT device (without source and drain) under the microscope

To directly present the performance of our solution-processed amorphous semiconductors, the TFTs were fabricated on silicon wafers. We chose e-beam evaporated SiO_2 as the gate insulator. The thickness of the insulator was highly controlled so that there should be less error and external influence involved into the final calculated result. The IV characteristics curves and the transistor parameters are shown in next 4 pages.

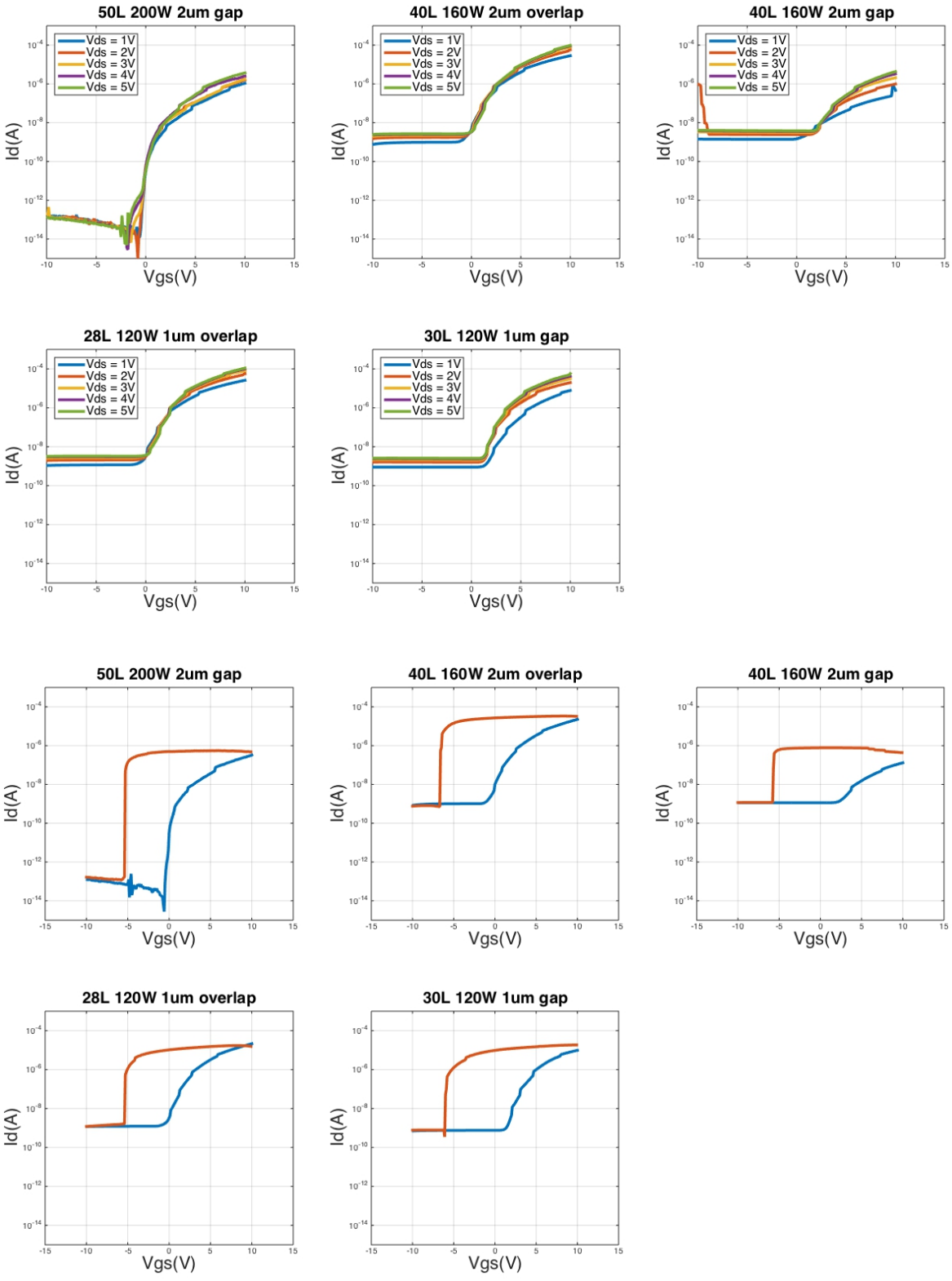


Figure 3.6. Transfer curve of α-IGZO TFTs with different size (Top left) Sample #1 (Top middle) Sample #2 (Top right) Sample #3 (Bottom left) Sample #4 (Bottom right) Sample #5

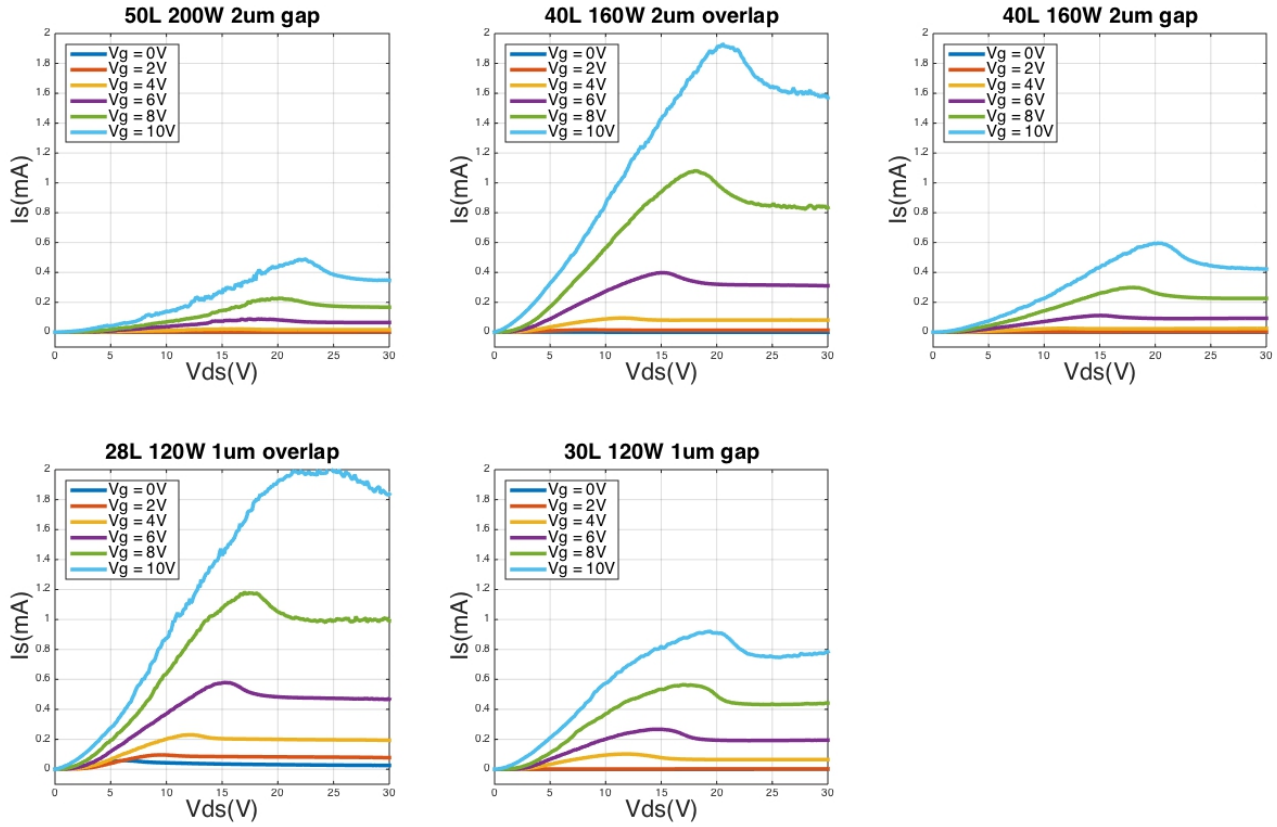


Figure 3.7. Output curve of α-IGZO TFTs with different size(Top left) Sample #1 (Top middle) Sample #2 (Top right) Sample #3 (Bottom left) Sample #4 (Bottom right) Sample #5

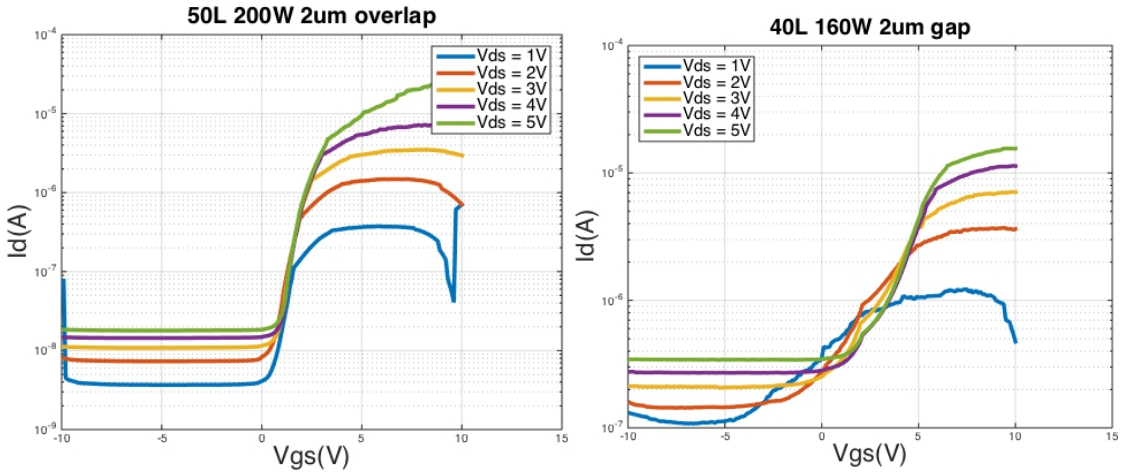


Figure 3.8. Transfer curve of α-IZTO TFTs with different size (Left) sample #1 (Right) sample #2

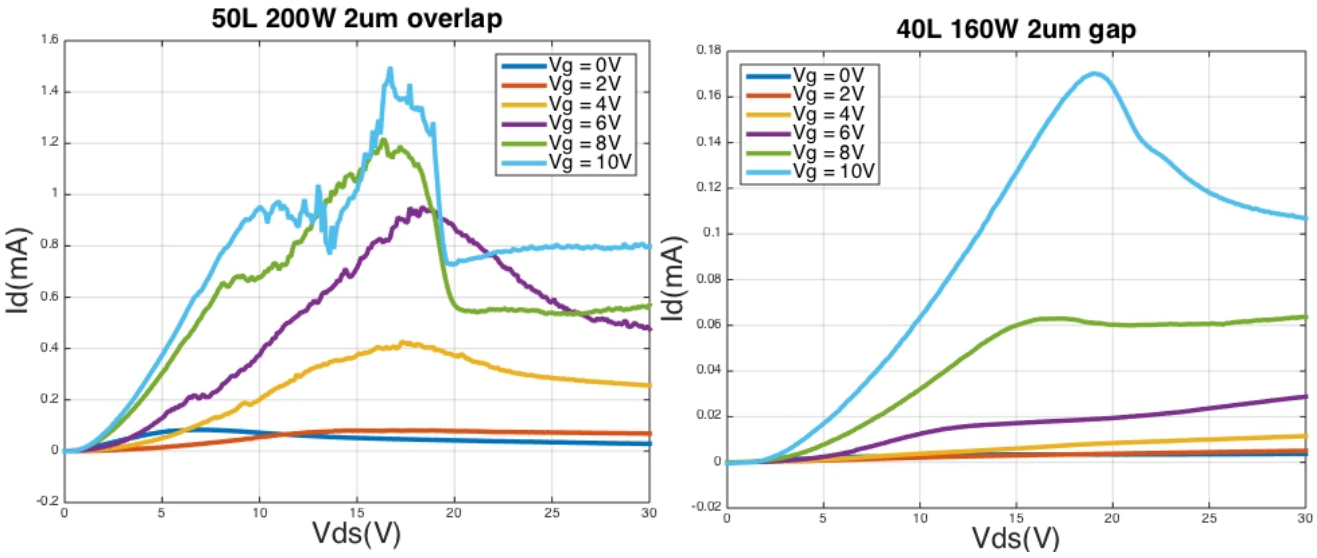


Figure 3.9. Output curve of α-IZTO TFTs with different size (Left) sample #1 (Right) sample #2

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{{V_{ds}}^2}{2} \right]$$

$$I_{D_{sat}} = \mu_{sat} C_{ox} \frac{W}{2L} (V_{gs} - V_{th})^2$$

$$SS = \frac{d\, V_{gs}}{d\, log I_{ds}}$$

With the given data, the parameter can be calculated from the equations above. The thickness of the dielectric is ~60nm and according to the report the dielectric constant of e-beam evaporated SiO_2 is ~3.9. C_{ox} is around 5.75 F/cm^2. The calculated result is shown in the table below.

Table 3.1. Calculated results for the AOS and compare to the performance to other's work

Ref	Device	Mobility ($cm^2V^{-1}S^{-1}$)	V_{th} (V)	SS (mV/dec)	I_{on}/I_{off}	Hysteresis (V)
	α-IGZO SiO_2 400°C #1	10.49	-0.6	200	~10^7	-5
	α-IGZO SiO_2 400°C #2	65.12	-0.9	1000	~10^4	-5
	α-IGZO SiO_2 400°C #3	33.76	2.1	1800	~10^3	-8
	α-IGZO SiO_2 400°C #4	71.54	-0.3	1050	~10^4	-5
	α-IGZO SiO_2 400°C #5	67.53	1.3	1350	~10^3	-7
	α-IZTO SiO_2 400°C #1	77.89	0.1	800	~10^3	/
	α-IZTO SiO_2 400°C #2	8.115	1.6	2800	~0.35 x 10^3	/
[59]	α-IZTO ZrO_2 300°C	0.91	0.28	199	10^7	0.32
[62]	α-IZTO ZrO_2 300°C UV	2.65	0.44	133	10^8	0.01
[60]	α-IGZO HfO_2 300°C	25.8	0.67	90	1.1 x 10^7	/
[61]	α-ZTO AlO_x 300°C #2	24	1.2	96	10^8	/

3.3 High-Performance Dielectrics for Thin-Film Transistor

3.3.1 Motivation

If the semiconductors are the fundamental of FETs, the dielectrics in FETs are the bricks. Thermal-grown silicon dioxide [62], [63] and vacuum-processed oxide dielectrics [64], [65] are the typical gate insulator choices for conventional FETs. However, researchers are always exploring a substitute with larger dielectric constant to enhance the overall performance of FETs, besides improving the performance of semiconductors themselves. Moreover, the lower leakage current and better chemical, mechanical and thermal stability are also desirable for advanced FETs.

To respond the demand of the fast-growing flexible and printable electronics industry, researchers have put more efforts on solution-based amorphous oxide dielectrics than ever. Zirconium dioxide, as one of the representative materials for the amorphous dielectrics, has been proved that it has outstanding chemical, mechanical and thermal resistivity, relatively high dielectric constant (~25 [66]) and high breakdown potential.

In this study, we have investigated this novel dielectric material. Instead of fabricating with the conventional high-temperature sol-gel process, we have applied an innovative low-temperature process so that it could be more compatible with flexible polymer substrates and micro-scale roll-to-roll printing technologies.

3.3.2 Low-Temperature UV Annealed Zirconium Oxide

During the sol-gel synthesizing process, there is a trade-off between the final performance and the treating temperature, treating duration. In general, applying higher temperature and treating with longer duration will result a film with high dielectric constant and higher breakdown potential. This phenomenon can be explained by the mechanism of the formation of amorphous oxide – External energy is required to break the high-energy (less stable) bonds (hydroxyl groups) and force the element form low-energy (more stable) bonds (M-O-M networks). The amorphous oxide may contain less active compound because of the lower temperature or shorter duration during the annealing. The sufficient annealing temperature and treating duration can be extracted from the thermogravimetric analysis (TGA). According to the past reports, annealing the precursor at 400°C for 1 hour is sufficient for most of hydrolyzed-alkoxide-based precursors [69], [67], [68], [69].

Despite the outstanding chemical stability, flexible, as well as the economic efficiency, the flexible polymer substrate cannot withstand the high temperature during the traditional fabrication. Due to the temperature limitation of flexible polymer substrate, it was nearly impossible to synthesize amorphous oxide by solution-based method.

To overcome the challenge, several low-temperature approaches were employed to accomplish the sol-gel process and showed promising results. UV annealing is one of the low-temperature methods. Instead of applying thermal energy to break the chemical bonds, UV light source emits high-energy photon to the target. The photon kicks out the hydroxyl group, simultaneously M-O-M structure form on the film. The method avoids inefficient heat conducting to the substrate but successfully catalyze the decomposition of the precursor. The UV sensitivity of the precursor can be checked from uv-vis spectroscopy. Figure 3.9. proves that a low pressure mercury light can cover the absorption spectrum of ZrAcAc in ethanol and ethanolamine and sufficiently deposes the precursor into the desired film.

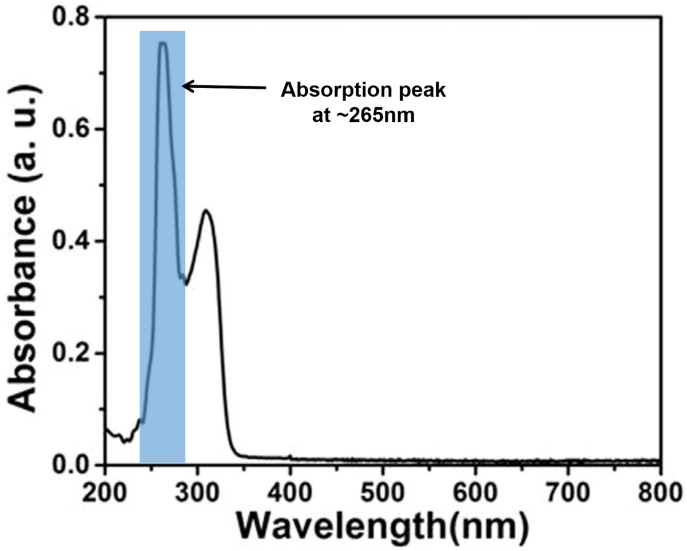


Figure 3.10. UV absorption of ZrAcAc in ethanol and ethanolamine [69]

To testify the performance of UV annealed amorphus oxide, we used metal-insulator-metal parallel plates capacity (Figure 3.10.) on silicon wafers (with 1 μm default wet oxide) and characterized the devices on probe station with Keithley 4200A-SCS Parameter Analyzer. We fabricated a test group with UV annealing process and a reference group annealed with 400 °C and 300 °C for 1 hour. The fabrication details are given in the Appendix B.1.

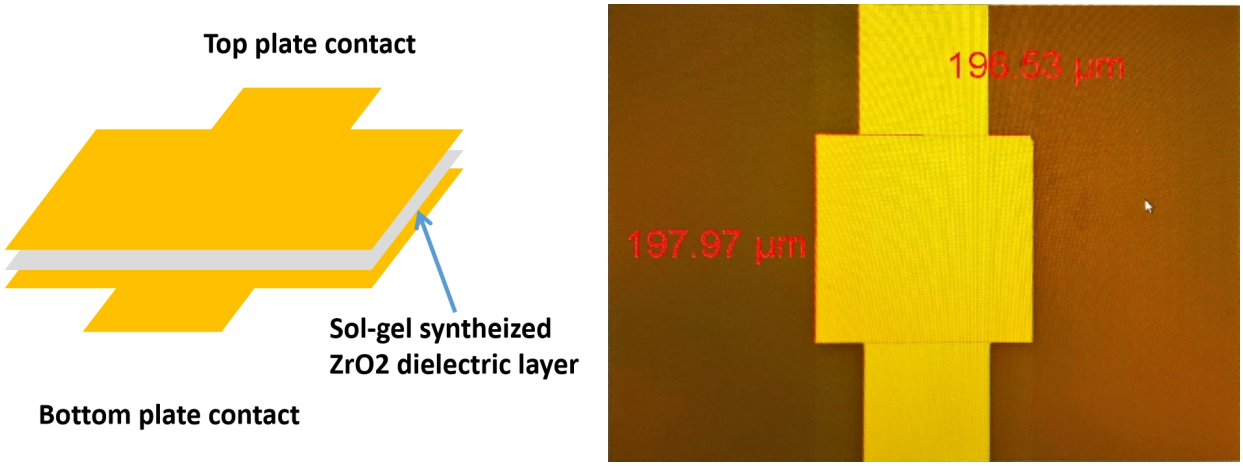


Figure 3.11. (Left) Schematic of a MIM structure (Right) MIM sample on silicon wafer

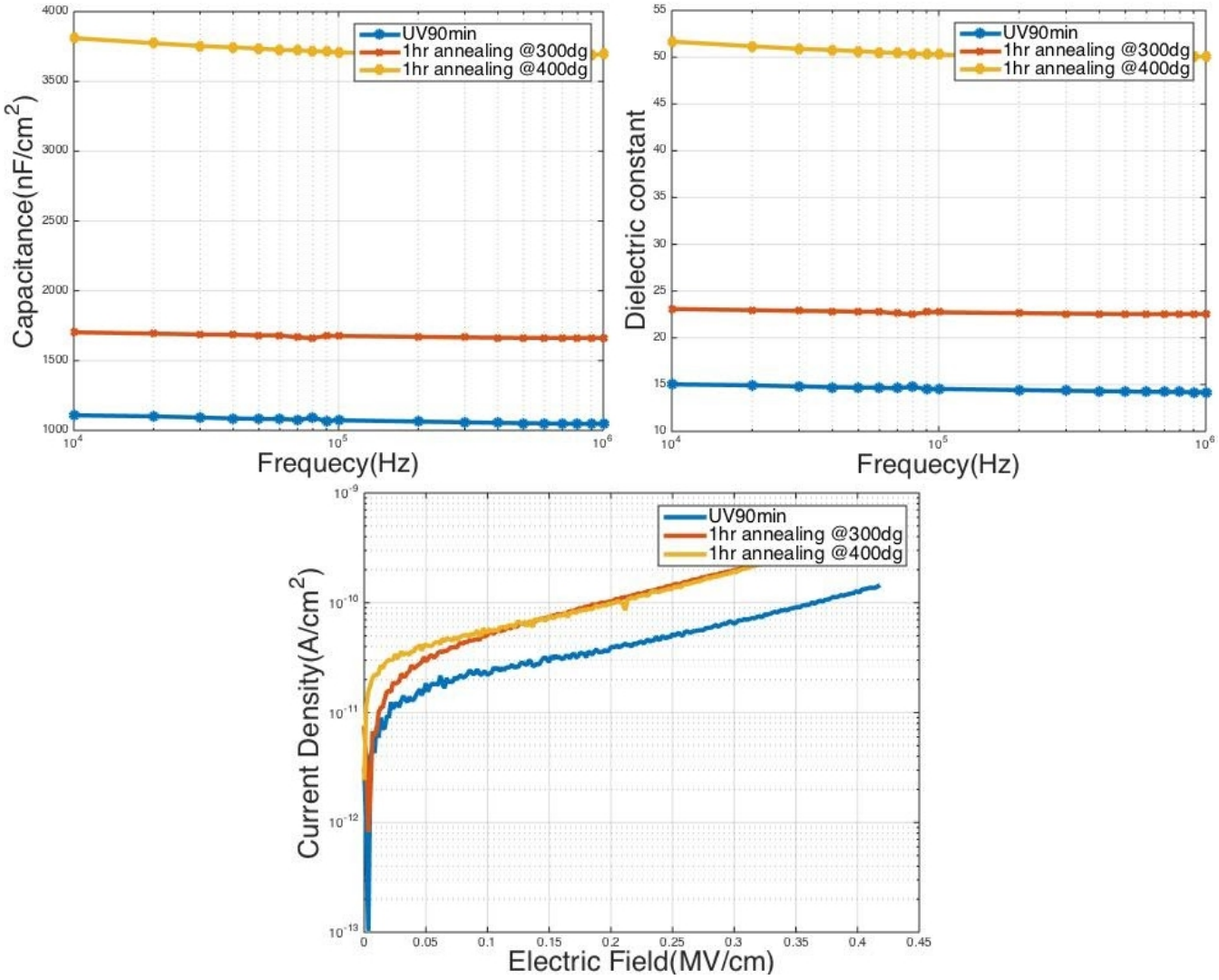


Figure 3.12. (Top left) Areal capacitance (Top right) Dielectric constant (Bottom) Leakage current of the capacitors based on ZrOx

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

Substitute the measured capacitance (C), effective area (A), and dielectric thickness (d) into the equation above, one can obtain the dielectric constant (ε_r - relative permittivity). The raw data and the measuring methods for the dielectric thickness are provided in Appendix B.2. The results (Figure 3.11) show the trend that the dielectric constant was improved when annealing temperature was increased. In the meanwhile, the UV annealing process sufficiently converted the precursor to amorphous zirconium oxide and exhibited good performance.

Table 3.2. Calculated results for the dielectrics and compare to the performance to others work

Ref	Precursors/Material	Treatment	Treatment duration	Dielectric Thickness	Dielectric constant	Leakage Current
	ZrAcAc in Ethanol & Ethanolamine	**UV**	**90 mins**	**120 nm ± 10%**	**15 ± 10% @100kHz**	**$9x10^{-11}$A/cm^2**
	ZrAcAc in Ethanol & Ethanolamine	**400°C**	**1 hour**	**120 nm ± 10%**	**51.6 ± 10% @100kHz**	**$2x10^{-10}$A/cm^2**
	ZrAcAc in Ethanol & Ethanolamine	**300°C**	**1 hour**	**120 nm ± 10%**	**22.5 ± 10% @100kHz**	**$2x10^{-10}$A/cm^2**
[70]	**AlOx**	**Mist CVD**	**/**	**/**	**6**	**/**
[64]	**AlCl3 in acetonitrile & ethylene glycol**	**300°C**	**1 hour**	**110nm**	**6.3**	**/**
[71]	**ZrAcAc in 2-ME & ethanolamine**	**400-700°C**	**1 hour**	**13nm**	**25.7-26.5**	**/**
[74]	**ZrAcAc in 2-ME & ethanolamine**	**400-700°C**	**1 hour**	**7nm**	**13.1-18.2**	**/**
[72]	**RF Sputtering HfO2**	**Thermal annealing**	**Annealing in H2, vacuum, O2**	**80nm**	**21/21.1/19.8**	**/**

4. SUMMARY AND FUTURE WORK

4.1 Summary

There is overwhelming demand for flexible electronics in the current market. Flexible electronics have shown adaptability, reliability and affordability and offer advantages in a wide-range of applications. Despite all these benefits, the development of flexible electronics is still in its infancy. In this thesis; (i) An innovative integrating method was demonstrated in Chapter 2. The method has successfully embedded the conventional semiconductor chips into flexible substrates without any modification. The integrated system exhibits good flexibility and reliability. It has also replicated the functionality without compromises (ii) In chapter 3, amorphous oxide semiconductor TFTs fabricated in our lab were demonstrated. The solution-processed AOS TFTs exhibited considerable high mobility of > 8 $cm^2V^{-1}S^{-1}$. However, large hysteresis, series resistance measured from IV characteristics point to the need for further development. The phenomenon might be caused by sub-optimum alignments and poor insulator quality: (iii) Gate insulators of TFTs have also been investigated. A novel low-temperature fabrication method for solution-based amorphous oxide has been demonstrated and the dielectrics fabricated by this method has exhibited characteristics in par with conventional materials. This demonstration has also proved the feasibility of fabricating amorphous oxide materials on flexible substrates by solution-based methods.

4.2 Future Work

The future work for the embedded flexible system is to demonstrate the applications of complex and larger scale circuits and systems. It can be achieved by integrating flexible batteries, on-board printed antennas, printed sensors and electronics. In the fabrication aspect, refining the fabrication process to be suitable for the roll-to-roll process is also an essential goal for the next phase of investigation.

For solution-based amorphous oxide thin-film transistors, the next phase of research is to determine the cause of the large output resistance, and large hysteresis in the output characteristics. In addition, improving the performance of amorphous oxide TFTs and obtaining reliable devices by fine-tuning the precursor will be important. Based on the current experiments, a systematic procedure (Figure

4.1) was established for tuning the materials to get better performance. The metallization process in the current phase is still based on the vacuum deposition systems. In the next phase, printed electrodes should substitute the current electrodes fabricated by the vacuum-based processes.

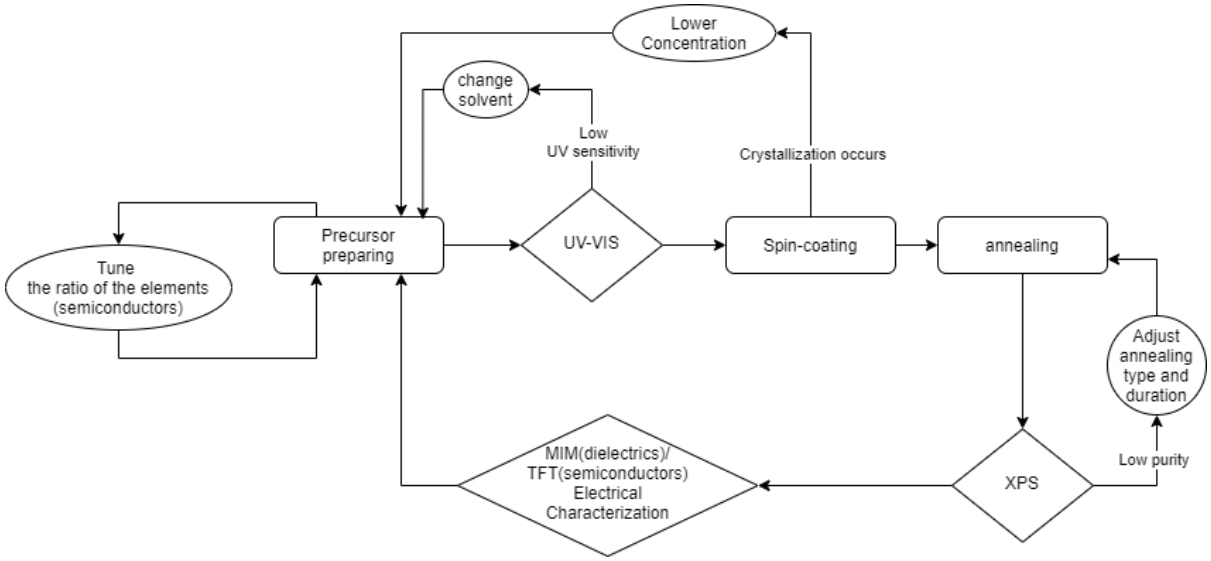


Figure 4.1. Flowchart of investigating the amorphous oxide materials

APPENDIX A. TFT FABRICATION PROCESS

A.1. Fabrication process of IZTO thin-film transistors

- **Preparing the Precursor Solution**
  - Dissolving 0.5 m mol indium acetylacetonate ($C_{15}H_{21}InO_6$, Alfa Aesar *98%*), 0.125m mol zinc acetylacetonate ($C_{10}H_{14}O_4Zn•H_2O$, Alfa Aesar) and 0.5m mol tin bis(acetylacetonate) chloride ($SnCl_2(C_5H_7O_2)_2$, Alfa Aesar, 95%) in 15mL ethanol.
  - Adding 0.75m mol of ethanolamine into the precursor solution.
  - Vigorous stirring the solution on a hot plate at 60 °C
- **Fabricating the Back-Plate**
  - Preparing a clean silicon wafer with 1 μm default oxide.
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 5 nm Ti and 60nm Au with Lesker E-beam evaporator.
  - Lift-off
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 60nm SiO_2 with Lesker E-beam evaporator.
  - Lift-off
- **Depositing the Semiconductor film**
  - Spin-coating the precursor on the back-plate with 3000 rpm for 30 seconds.
  - Immediately annealing the sample on a hot plate at 400 °C for 1 hour.
- **Depositing the Source and Drain Contact**
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 5 nm Ti and 60nm Au and follow with 20nm Al with Lesker E-beam evaporator.
  - Lift-off

A.2. Fabrication process of IGZO thin-film transistors

- **Preparing the Precursor Solution**
  - Dissolving 0.2 m mol indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$, Sigma-Aldrich, 99.9%), 0.2 m mol gallium nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$, Sigma Aldrich, 99.9%) and 0.2m mol zinc nitrate hydrate ($Zn(NO_3)_2 \cdot 6H_2O$, Sigma Aldrich, 98%) in 10mL 35% acetonitrile and 65% ethylene glycol .
  - Vigorous stirring the solution on a hot plate at 60 °C
- **Fabricating the Back-Plate**
  - Preparing a clean silicon wafer with 1 μm default oxide.
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 5 nm Ti and 60 nm Au with Lesker E-beam evaporator.
  - Lift-off
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 60 nm SiO_2 with Lesker E-beam evaporator.
  - Lift-off
- **Depositing the Semiconductor Film**
  - Spin-coating the precursor on the back-plate with 3000 rpm for 30 seconds.
  - Immediately annealing the sample on a hot plate at 400 °C for 1 hour.
- **Depositing the Source and Drain Contact**
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 5 nm Ti and 60nm Au and follow with 20nm Al with Lesker E-beam evaporator.
  - Lift-off

APPENDIX B. FABRICATION PROCESS OF LOW TEMPERATURE GATE INSULATORS

B.1. Fabrication process of ZrO_2 Metal-Insulator-Metal Capacitors

- **Preparing the Precursor Solution**
  - Dissolving 0.2 m mol zirconium acetylacetonate ($Zr(C_5H_7O_2)_4$, Sigma-Aldrich, 97%) in 10mL ethanol.
  - Adding 0.75m mol of ethanolamine into the precursor solution.
  - Vigorous stirring the solution on a hot plate at 60 °C
- **Fabricating the Back-Plate**
  - Preparing a clean silicon wafer with 1 μm default oxide.
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 5nm Ti and 60nm Au with Lesker E-beam evaporator.
  - Lift-off
- **Depositing the Dielectric Film**
  - Spin-coating the precursor on the back-plate with 3000 rpm for 30 seconds.
  - Immediately annealing the sample in a UV cleaner (Jetlight uvo clear model 42) for 90 min / on a hot plate at 300 / 400 °C for 1 hour.
- **Depositing the Top Metal Contact**
  - Depositing and Patterning the Photoresist on the wafer.
  - Depositing 5 nm Ti and 100nm Au with Lesker E-beam evaporator.
  - Lift-off

B.2. The method of measuring the thickness

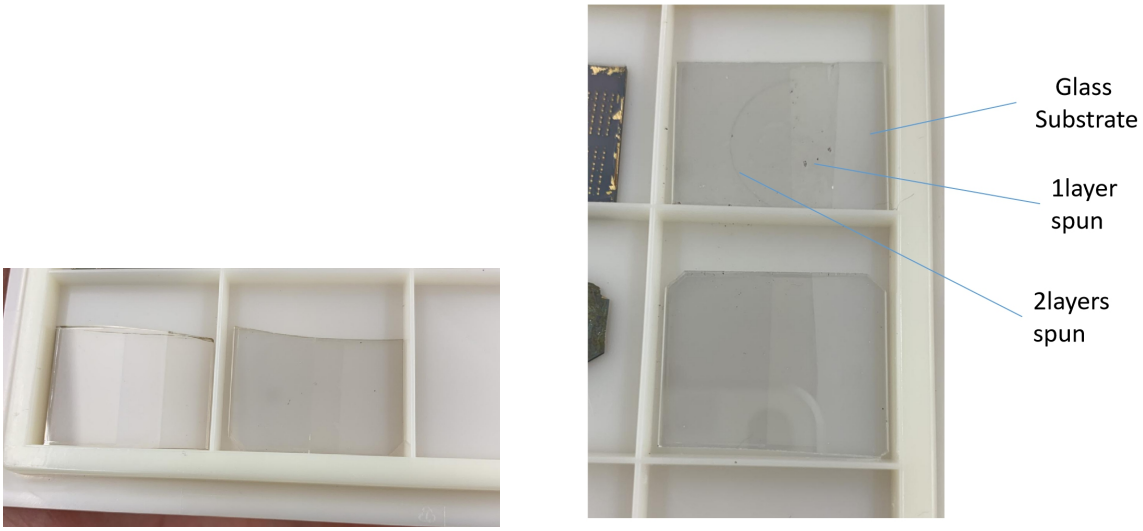


Figure B.2. Verifying the thickness of the dielectric film (Left) UV annealed samples (Right) High temperature annealed samples

To verify the thickness of the dielectric film and give the thickness reference to calculate the characteristics of under testing dielectrics film. The precursor was spun on a wafer half covered with tape. The tape was removed right after the spin coating. Then sample was treated with the proper annealing process. The process was repeated again. Measured from the alpha-step IQ surface profiler. The thickness of two layers of ZrO_2 film was 110 – 125 nm.

REFERENCES

[1] A. Nathan *et al*., "Flexible Electronics: The Next Ubiquitous Platform," in *Proceedings of the IEEE*, vol. 100, no. Special Centennial Issue, pp. 1486-1517, 13 May 2012, doi: 10.1109/JPROC.2012.2190168.

[2] Alam M.A., Kumar S. (2012) Flexible Electronics. In: Bhushan B. (eds) Encyclopedia of Nanotechnology. Springer, Dordrecht. https://doi.org/10.1007/978-90-481-9751-4_147

[3] Cheng IC., Wagner S. (2009) Overview of Flexible Electronics Technology. In: Wong W.S., Salleo A. (eds) Flexible Electronics. Electronic Materials: Science & Technology, vol 11. Springer, Boston, MA. https://doi.org/10.1007/978-0-387-74363-9_1

[4] M. Mizukami et al., "Flexible AM OLED panel driven by bottom-contact OTFTs," in IEEE Electron Device Letters, vol. 27, no. 4, pp. 249-251, April 2006, doi: 10.1109/LED.2006.870413.

[5] D.H. Cho, O.E. Kwon, Y.S. Park, B.G. Yu, J. Lee, J. Moon, H. Cho, H. Lee, N.S. Cho, Flexible integrated OLED substrates prepared by printing and plating process, Org. Electron. 50 (2017) 170\u2013176.

[6] Lingley, A. R., Ali, M., Liao, Y., Mirjalili, R., Klonner, M., Sopanen, M., . . . Parviz, B. A. (2011). A single-pixel wireless contact lens display. *Journal of Micromechanics and Microengineering, 21*(12), 125014. doi:10.1088/0960-1317/21/12/125014

[7] Yao, H., Liao, Y., Lingley, A. R., Afanasiev, A., Lähdesmäki, I., Otis, B. P., & Parviz, B. A. (2012). A contact lens with integrated telecommunication circuit and sensors for wireless and continuous tear glucose monitoring. *Journal of Micromechanics and Microengineering, 22*(7), 075007. doi:10.1088/0960-1317/22/7/075007

[8] Liao, C., Mak, C., Zhang, M., Chan, H. L., & Yan, F. (2014). Flexible Organic Electrochemical Transistors for Highly Selective Enzyme Biosensors and Used for Saliva Testing. *Advanced Materials, 27*(4), 676-681. doi:10.1002/adma.201404378

[9] Romeo, A., Moya, A., Leung, T. S., Gabriel, G., Villa, R., & Sánchez, S. (2018). Inkjet printed flexible non-enzymatic glucose sensor for tear fluid analysis. *Applied Materials Today, 10*, 133-141. doi:10.1016/j.apmt.2017.12.016

[10] Yang, Y., & Gao, W. (2019). Wearable and flexible electronics for continuous molecular monitoring. *Chemical Society Reviews, 48*(6), 1465-1491. doi:10.1039/c7cs00730b

[11] Wang, Y., Qiu, Y., Ameri, S. K., Jang, H., Dai, Z., Huang, Y., & Lu, N. (2018). Low-cost, μm-thick, tape-free electronic tattoo sensors with minimized motion and sweat artifacts. *Npj Flexible Electronics, 2*(1). doi:10.1038/s41528-017-0019-4

[12] Koh, A., Kang, D., Xue, Y., Lee, S., Pielak, R. M., Kim, J., . . . Rogers, J. A. (2016). A soft, wearable microfluidic device for the capture, storage, and colorimetric sensing of sweat. *Science Translational Medicine, 8*(366). doi:10.1126/scitranslmed.aaf2593

[13] Nakata, S., Arie, T., Akita, S., & Takei, K. (2017). Wearable, Flexible, and Multifunctional Healthcare Device with an ISFET Chemical Sensor for Simultaneous Sweat pH and Skin Temperature Monitoring. *ACS Sensors, 2*(3), 443-448. doi:10.1021/acssensors.7b00047

[14] Wachter, S., Polyushkin, D. K., Bethge, O., & Mueller, T. (2017). A microprocessor based on a two-dimensional semiconductor. *Nature Communications, 8*(1). doi:10.1038/ncomms14948

[15] Flexible Electronics Market Size, Analysis: Industry Report 2024. (n.d.). Retrieved November 02, 2020, from https://www.ameriresearch.com/product/flexible-electronics-market/

[16] S. Khan, L. Lorenzelli and R. S. Dahiya, "Technologies for Printing Sensors and Electronics Over Large Flexible Substrates: A Review," in *IEEE Sensors Journal*, vol. 15, no. 6, pp. 3164-3185, June 2015, doi: 10.1109/JSEN.2014.2375203.

[17] Tao, R., Peng, J., Ning, H., Chen, J., Zou, J., Fang, Z., . . . Yao, R. (2018). Inkjet Printed Electrodes in Thin Film Transistors. *IEEE Journal of the Electron Devices Society, 6*, 774-790. doi:10.1109/jeds.2018.2852288

[18] Courtland, R. (2017, March 30). Ntel Now Packs 100 Million Transistors in Each Square Millimeter. Retrieved November 03, 2020, from https://spectrum.ieee.org/nanoclast/semiconductors/processors/intel-now-packs-100-million-transistors-in-each-square-millimeter

[19] Chung, S., Cho, K., & Lee, T. (2019). Recent Progress in Inkjet-Printed Thin-Film Transistors. *Advanced Science, 6*(6), 1801445. doi:10.1002/advs.201801445

[20] Garlapati, S. K., Divya, M., Breitung, B., Kruk, R., Hahn, H., & Dasgupta, S. (2018). Printed Electronics Based on Inorganic Semiconductors: From Processes and Materials to Devices. *Advanced Materials, 30*(40), 1707600. doi:10.1002/adma.201707600

[21] Bolat, S., Sevilla, G. T., Mancinelli, A., Gilshtein, E., Sastre, J., Vidani, A. C., . . . Romanyuk, Y. E. (2020). Synaptic transistors with aluminum oxide dielectrics enabling full audio frequency range signal processing. *Scientific Reports, 10*(1). doi:10.1038/s41598-020-73705-w

[22] Carlos, E., Leppäniemi, J., Sneck, A., Alastalo, A., Deuermeier, J., Branquinho, R., . . . Fortunato, E. (2020). Printed, Highly Stable Metal Oxide Thin-Film Transistors with Ultra-Thin High-κ Oxide Dielectric. *Advanced Electronic Materials, 6*(3), 1901071. doi:10.1002/aelm.201901071

[23] Park, Y. M., Desai, A., Salleo, A., & Jimison, L. (2013). Solution-Processable Zirconium Oxide Gate Dielectrics for Flexible Organic Field Effect Transistors Operated at Low Voltages. *Chemistry of Materials, 25*(13), 2571-2579. doi:10.1021/cm303547a

[24] Dong, X., Xia, G., Zhang, Q., Li, L., Gong, H., Bi, J., & Wang, S. (2017). Room-temperature UV-ozone assisted solution process for zirconium oxide films with high dielectric properties. *Ceramics International, 43*(17), 15205-15213. doi:10.1016/j.ceramint.2017.08.055

[25] Jeong, J., Hwang, H., Choi, D., Ma, B., Jung, J., & Chang, M. (2020). Hybrid Polymer/Metal Oxide Thin Films for High Performance, Flexible Transistors. *Micromachines, 11*(3), 264. doi:10.3390/mi11030264

[26] Zharkova, G. M., & Streltsov, S. A. (2020). Effect of yttrium oxide nanoparticles on the dielectric properties and dynamics of the formation of holographic polymer–liquid-crystal composites. *Journal of Optical Technology, 87*(1), 23. doi:10.1364/jot.87.000023

[27] Dyson, D. (2020, May 06). Flexible Hybrid Electronics: Future of Flexible Printed Circuit Boards. Retrieved November 04, 2020, from https://www.idtechex.com/en/research-article/flexible-hybrid-electronics-future-of-flexible-printed-circuit-boards/20603

[28] Susan, Donald Francis, Beck, David F., Sorensen, Neil R, & Thayer, Gayle Echo. *Fatigue Behavior of Thin Cu Foils and Cu/Kapton Flexible Circuits.*. United States.

[29] Wolbarsht, M. (1984). Laser surgery: CO2or HF. *IEEE Journal of Quantum Electronics, 20*(12), 1427-1432. doi:10.1109/jqe.1984.1072328

[30] Palaniappan, V., Masihi, S., Panahi, M., Maddipatla, D., Bose, A. K., Zhang, X., . . . Atashbar, M. Z. (2019). Laser-Assisted Fabrication of Flexible Micro-Structured Pressure Sensor for Low Pressure Applications. *2019 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*. doi:10.1109/fleps.2019.8792235

[31] Kothuru, A., Amreen, K., & Goel, S. (2020). Electromicrofluidic Device on Multilayered Laser-Induced Polyamide Substrate for Diverse Electrochemical Applications. *IEEE Transactions on Electron Devices*, *67*(11), 5097–5103. https://doi.org/10.1109/ted.2020.3022346

[32] Haedersdal, M., Sakamoto, F. H., Farinelli, W. A., Doukas, A. G., Tam, J., & Anderson, R. R. (2010). Fractional CO2 laser-assisted drug delivery. *Lasers in Surgery and Medicine, 42*(2), 113-122. doi:10.1002/lsm.20860

[33] Lee, Y., Cho, T., Sung, P., Kao, K., Hsueh, F., Hou, F., . . . Yeh, W. (2015). High performance poly Si junctionless transistors with sub-5nm conformally doped layers by molecular monolayer doping and microwave incorporating CO2 laser annealing for 3D stacked ICs applications. *2015 IEEE International Electron Devices Meeting (IEDM)*. doi:10.1109/iedm.2015.7409638

[34] Kurimoto, M., Yamashita, Y., Ozaki, H., Kato, T., Funabashi, T., & Suzuoki, Y. (2015). 3D printing of conical insulating spacer using alumina /UV-cured-resin composite. *2015 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. doi:10.1109/ceidp.2015.7352047

[35] Zhang, W., Yao, Y., & Chen, K. (2001). Modelling and Analysis of UV Laser Micromachining of Copper. *The International Journal of Advanced Manufacturing Technology, 18*(5), 323-331. doi:10.1007/s001700170056

[36] Kitai, M., Popkov, V., Semchischen, V., & Kharizov, A. (1991). The physics of UV laser cornea ablation. *IEEE Journal of Quantum Electronics, 27*(2), 302-307. doi:10.1109/3.78235

[37] Leest, R. V. (1995). UV photo-annealing of thin sol-gel films. *Applied Surface Science, 86*(1-4), 278-285. doi:10.1016/0169-4332(94)00398-x

[38] F. Liu *et al*., "Innovative Sub-5- μ m Microvias by Picosecond UV Laser for Post-Moore Packaging Interconnects," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 10, pp. 2016-2023, Oct. 2019, doi: 10.1109/TCPMT.2019.2941866

[39] Vitos, L., Ruban, A., Skriver, H., & Kollár, J. (1998). The surface energy of metals. *Surface Science, 411*(1-2), 186-202. doi:10.1016/s0039-6028(98)00363-x

[40] Salma Habib, Marian Lehocky, Daniela Vesela, Petr Humpolíček, Igor Krupa, Anton Popelka, Preparation of Progressive Antibacterial LDPE Surface via Active Biomolecule Deposition Approach, Polymers, 10.3390/polym11101704, 11, 10, (1704), (2019)

[41] Mark, J. .. (2007). *Physical properties of polymers handbook*. New York: Springer.

[42] Guilhabert, B., Hurtado, A., Jevtics, D., Gao, Q., Tan, H. H., Jagadish, C., & Dawson, M. D. (2016). Transfer Printing of Semiconductor Nanowires with Lasing Emission for Controllable Nanophotonic Device Fabrication. *ACS Nano, 10*(4), 3951-3958. doi:10.1021/acsnano.5b07752

[43] Jeong, S., Jeong, Y., & Moon, J. (2008). Solution-Processed Zinc Tin Oxide Semiconductor for Thin-Film Transistors. *The Journal of Physical Chemistry C, 112*(30), 11082-11085. doi:10.1021/jp803475g

[44] Lee, D., Han, S., Herman, G. S., & Chang, C. (2009). Inkjet printed high-mobility indium zinc tin oxide thin film transistors. *Journal of Materials Chemistry, 19*(20), 3135. doi:10.1039/b822893k

[45] Ko, S.H., Pan, H., Grigoropoulos, C.P. *et al.* Lithography-free high-resolution organic transistor arrays on polymer substrate by low energy selective laser ablation of inkjet-printed nanoparticle film. *Appl. Phys. A* 92, 579–587 (2008). https://doi.org/10.1007/s00339-008-4597-9

[46] Powell, M. J. (1983). Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors. *Applied Physics Letters*, *43*(6), 597–599. https://doi.org/10.1063/1.94399

[47] Libsch, F. R., & Kanicki, J. (1993). Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors. *Applied Physics Letters*, *62*(11), 1286–1288. https://doi.org/10.1063/1.108709

[48] Chabinyc, M. L., Street, R. A., & Northrup, J. E. (2007). Effects of molecular oxygen and ozone on polythiophene-based thin-film transistors. *Applied Physics Letters*, *90*(12), 123508. https://doi.org/10.1063/1.2715445

[49] Chiang, H. Q., Wager, J. F., Hoffman, R. L., Jeong, J., & Keszler, D. A. (2004). High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer. *Applied Physics Letters*, *86*(1), 013503. https://doi.org/10.1063/1.1843286

[50] Chun-Ying Chen, & Kanicki, J. (1996). High field-effect-mobility a-Si:H TFT based on high deposition-rate PECVD materials. *IEEE Electron Device Letters*, *17*(9), 437–439. https://doi.org/10.1109/55.536285

[51] Arias, A. C., MacKenzie, J. D., McCulloch, I., Rivnay, J., & Salleo, A. (2010). Materials and applications for large area electronics: Solution-based approaches. *Chemical Reviews*, *110*(1), 3–24. https://doi.org/10.1021/cr900150b

[52] Yan, H., Chen, Z., Zheng, Y. *et al.* A high-mobility electron-transporting polymer for printed transistors. *Nature* 457, 679–686 (2009). https://doi.org/10.1038/nature07727

[53] Naber, R. C. G., Tanase, C., Blom, P. W. M., Gelinck, G. H., Marsman, A. W., Touwslager, F. J., Setayesh, S., & de Leeuw, D. M. (2005). High-performance solution-processed polymer ferroelectric field-effect transistors. *Nature Materials*, *4*(3), 243–248. https://doi.org/10.1038/nmat1329

[54] Faber, H., Burkhardt, M., Jedaa, A., Kälblein, D., Klauk, H., & Halik, M. (2009). Low-temperature solution-processed memory transistors based on zinc oxide nanoparticles. *Advanced Materials*, *21*(30), 3099–3104. https://doi.org/https://doi.org/10.1002/adma.200900440

[55] Rivnay, J., Jimison, L. H., Northrup, J. E., Toney, M. F., Noriega, R., Lu, S., Marks, T. J., Facchetti, A., & Salleo, A. (2009). Large modulation of carrier transport by grain-boundary molecular packing and microstructure in organic thin films. *Nature Materials*, *8*(12), 952–958. https://doi.org/10.1038/nmat2570

[56] Sakanoue, T., & Sirringhaus, H. (2010). Band-like temperature dependence of mobility in a solution-processed organic semiconductor. *Nature Materials*, *9*(9), 736–740. https://doi.org/10.1038/nmat2825

[57] Bae, E. J., Kang, Y. H., Han, M., Lee, C., & Cho, S. Y. (2014). Soluble oxide gate dielectrics prepared using the self-combustion reaction for high-performance thin-film transistors. *Journal of Materials Chemistry C*, *2*(28), 5695–5703. https://doi.org/10.1039/C4TC00874J

[58] Kim, K., Kim, S., & Lee, S. Y. (2012). Effect of excimer laser annealing on the properties of ZnO thin film prepared by sol-gel method. *Current Applied Physics*, *12*(2), 585–588. https://doi.org/10.1016/j.cap.2011.09.006

[59] Tsay, C.-Y., & Wang, M.-C. (2013). Structural and optical studies on sol–gel derived ZnO thin films by excimer laser annealing. *Ceramics International*, *39*(1), 469–474. https://doi.org/10.1016/j.ceramint.2012.06.050

[60] Song, K., Young Koo, C., Jun, T., Lee, D., Jeong, Y., & Moon, J. (2011). Low-temperature soluble InZnO thin film transistors by microwave annealing. *Journal of Crystal Growth*, *326*(1), 23–27. https://doi.org/10.1016/j.jcrysgro.2011.01.044

[61] Chae, D., Kim, J., Shin, J., Lee, W. H., & Ko, S. (2019). A low-temperature and short-annealing process for metal oxide thin film transistors using deep ultraviolet light for roll-to-roll processing. *Current Applied Physics*, *19*(8), 954–960. https://doi.org/10.1016/j.cap.2019.02.004

[62] Naik, B. R., Avis, C., Chowdhury, M. D. H., Kim, T., Lin, T., & Jang, J. (2016). Improvement in performance of solution-processed indium–zinc–tin oxide thin-film transistors by UV/O $_3$ treatment on zirconium oxide gate insulator. *Japanese Journal of Applied Physics*, *55*(3S1), 03CC02. https://doi.org/10.7567/JJAP.55.03CC02

[63] Son, D., Kim, D.-H., Sung, S.-J., Jung, E.-A., & Kang, J.-K. (2010). High performance and the low voltage operating InGaZnO thin film transistor. *Current Applied Physics*, *10*(4), e157–e160. https://doi.org/10.1016/j.cap.2010.03.012

[64] Avis, C., & Jang, J. (2011). High-performance solution processed oxide TFT with aluminum oxide gate dielectric fabricated by a sol–gel method. *Journal of Materials Chemistry*, *21*(29), 10649–10652. https://doi.org/10.1039/C1JM12227D

[65] Aubuchon, K. G. (1971). Radiation hardening of p-mos devices by optimization of the thermal si02 gate insulator. *IEEE Transactions on Nuclear Science*, *18*(6), 117–125. https://doi.org/10.1109/TNS.1971.4326422

[66] Green, M. L., Ho, M.-Y., Busch, B., Wilk, G. D., Sorsch, T., Conard, T., Brijs, B., Vandervorst, W., Räisänen, P. I., Muller, D., Bude, M., & Grazul, J. (2002). Nucleation and growth of atomic layer deposited HfO2 gate dielectric layers on chemical oxide (Si–o–h) and thermal oxide (Sio2 or si–o–n) underlayers. *Journal of Applied Physics*, *92*(12), 7168–7174. https://doi.org/10.1063/1.1522811

[67] Arulkumaran, S., Egawa, T., Ishikawa, H., Jimbo, T., & Umeno, M. (1998). Investigations of SiO2/n-GaN and Si3N4/n-GaN insulator–semiconductor interfaces with low interface state density. *Applied Physics Letters*, *73*(6), 809–811. https://doi.org/10.1063/1.122009

[68] Jun, S.-I., McKnight, T. E., Melechko, A. V., Simpson, M. L., & Rack, P. D. (2005). Characterisation of reactively sputtered silicon oxide for thin-film transistor fabrication. *Electronics Letters*, *41*(14), 822. https://doi.org/10.1049/el:20051045

[69] Dong, X., Xia, G., Zhang, Q., Li, L., Gong, H., Bi, J., & Wang, S. (2017). Room-temperature UV-ozone assisted solution process for zirconium oxide films with high dielectric properties. *Ceramics International*, *43*(17), 15205–15213. https://doi.org/10.1016/j.ceramint.2017.08.055

[70] Lee, D.-H., Han, S.-Y., Herman, G. S., & Chang, C. (2009). Inkjet printed high-mobility indium zinc tin oxide thin film transistors. *Journal of Materials Chemistry*, *19*(20), 3135. https://doi.org/10.1039/b822893k

[71] Jeong, S., Jeong, Y., & Moon, J. (2008). Solution-processed zinc tin oxide semiconductor for thin-film transistors. *The Journal of Physical Chemistry C*, *112*(30), 11082–11085. https://doi.org/10.1021/jp803475g

[72] Naik, B. R., Avis, C., Chowdhury, M. D. H., Kim, T., Lin, T., & Jang, J. (2016). Improvement in performance of solution-processed indium–zinc–tin oxide thin-film transistors by UV/O_3 treatment on zirconium oxide gate insulator. *Japanese Journal of Applied Physics*, *55*(3S1), 03CC02. https://doi.org/10.7567/JJAP.55.03CC02

[73] Growth and electrical properties of AlO_x grown by mist chemical vapor deposition. (2013). *AIP Advances*, *3*(3), 032135. https://doi.org/10.1063/1.4798303

[74] Hwang, S. M., Lee, S. M., Park, K., Lee, M. S., Joo, J., Lim, J. H., Kim, H., Yoon, J. J., & Kim, Y. D. (2011). Effect of annealing temperature on microstructural evolution and electrical properties of sol-gel processed ZrO2/Si films. *Applied Physics Letters*, *98*(2), 022903. https://doi.org/10.1063/1.3541784

[75] Son, D., Kim, D.-H., Sung, S.-J., Jung, E.-A., & Kang, J.-K. (2010). High performance and the low voltage operating InGaZnO thin film transistor. *Current Applied Physics*, *10*(4), e157–e160. https://doi.org/10.1016/j.cap.2010.03.012

VITA

Zhu, Yuhang

EDUCATION BACKGROUND

01/2018-Present Purdue University,West Lafayette

Major: Electrical Engineering

Degree: Master of Science

Advisor: Prof. Saeed Mohammadi

08/2012-12/2016 Purdue University, West Lafayette

Major: Electrical Engineering

Degree: Bachelor of Science

RESEARCH INERESTS

Flexible and Printable Electronics | RF Integrated Circuits | Flexible Sensors

ACADEMIC EMPLOYMENT

Research Assistant to Professor Saeed Mohammadi, Department of Electrical and Computer Engineering, Purdue University, Summer 2017 - present. Research activities include Solution-processed Printable Metal Oxide Thin-film Transistors, Innovative Packaging Method of a CMOS-Based Wireless Sensor System on Flexible Substrates, RFID Reader

Graduate Teaching Assistant, Department of Electrical and Computer Engineering, Purdue University, January 2019 - May 2019. Responsibilities include: assisting professors with the preparation and presentation, grading, and tutoring of the ECE senior design course.

HONORS AND AWARDS

05/2016 Eaton Design Award

- Eaton Design award is the award for individual designer who made the best design in the senior design course. Only one student can get this remarkable honor each semester.