FEEDBACK DRIVEN MATCHING NETWORKS FOR RADIO FREQUENCY POWER AMPLIFIERS

by

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I would like to dedicate this work to my wife.

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GLOSSARY, ABBREVIATIONS, AND SYMBOLS

Abbreviations

ADC: Analog to Digital Converter

BJT: Bipolar Junction Transistor

C: Capacitor

DAC: Digital to Analog Converter

dB: Decibel

DSP: Digital Signal Processor

FET: Field Effect Transistor

FPGA: Field Programmable Gate Array

G: Gain

HBT: Heterojunction Transistor

HEMT: High Electron Mobility Transistor

L: Inductor

MEMS: Micro Electro-Mechanical System

MESFET: Metal Semiconductor Field Effect Transistor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

PA: Power Amplifier

PAE: Power Added Efficiency

R: Resistor

RF: Radio Frequency

RFPA: Radio Frequency Power Amplifier

VNA: Vector Network Analyzer

VSWR: Voltage Standing Wave Ratio

V_t: Threshold Voltage

V_0^-: Reflected Wave Voltage

Γ: Reflection Coefficient

V_0^+: Incident Wave Voltage

X: Reactance

X_C: Capacitive Reactance

X_L Inductive Reactance

X_P: Parallel (Shunt) Reactance

X_S: Series Reactance

Z_L: Load (Output) Impedance

Z_S: Source (Input) Impedance

Symbols

π: standard definition of pi (3.14159)

ω: angular velocity in radian/second

Ω: resistance in Ohms

°: angle in degrees

ABSTRACT

The research presented covers the theory and design of feedback-driven matching networks for radio frequency power amplifiers. The study examines amplifier classifications, types of tunable components, feedback topologies, and control systems to achieve the desired operation. The work centers on designing and implementing a tunable matching network for an amplifier's input and output. The tunable systems provide the amplifier with a wide range of operational frequencies at reasonable power levels comparable to today's modern communication systems and produce millisecond-based tuning times. Simulated results are verified against a fabricated system prototype and tweaked to provide further insight into the design's operation.

CHAPTER 1. INTRODUCTION

The wireless communication industry is ever-expanding, driven by the need for faster speeds, more substantial data transfer, and reduced power consumption. The incorporation of these features presents an interesting problem for engineers. Engineers are turning to wideband operations as the way of the future to accomplish these goals. The concept is that each user has more stake in the Radio Frequency (RF) spectrum for their data transmission, analogous to larger pipelines for data to flow through (Rodriguez, 2008). To achieve this, high-efficiency electronic systems and devices that can handle the wide bandwidth are required.

Power amplifiers (PA) are among the most critical aspects of the Radio Frequency (RF) transmit chain. Radio Frequency Power Amplifiers (RFPAs) are typically the final stage before the antenna and thus provide the actual power for transmission. A Typical RFPA converts DC voltage into RF power employing an N channel transistor. The change of the voltage on the transistor gate and the device's constant gain amplifies the signal. RFPAs are not like other high-efficiency amplifiers, such as class D amplifiers. Device and circuit parasitics in these high-efficiency amplifiers cause problems at higher switching frequencies, unlike low-frequency audio amplifiers (Raab, et al., 2002). For these reasons, RFPAs need to be linear in design. A standard example of an RFPA topology is a Class A amplifier. Linear amplifiers are notorious for their lack of efficiency. Removal of inefficiencies in the surrounding system compensates for the RFPA's already high losses (Zannas & Vafiadis, 2016).

One of the challenges to power transmission from an RFPA is the impedance mismatch at different frequencies. An impedance mismatch can cause reflections on the input and output of the power amplifier. The system loses the reflected power instead of transmitting it and can even incur noise on the output. In traditional narrowband applications, matching the antenna and amplifier together is done using a lumped element matching network allowing optimal power transfer. RFPA's can be statically matched because over a narrow band of operation, the devices' impedance remains constant. For narrowband applications, static matching networks work well due to the design's simplicity but fall short in wideband applications (Thompson, Richardson, Davis, & White, 2005). In wideband configurations, an RFPA and antenna's impedance changes significantly enough that the static matching network no longer provides a high power

transmission level. For very wide bandwidths, this requires lots of networks and an increase in cost in printed circuit board (PCB) space and parts, which is not practical.

One technology currently being implemented around the country is 5G ultra-wideband. One of the many advances that this technology bolsters is the concept of wide bandwidths for data transfer on handheld devices. Many of the systems that will support 5G are handheld and thus run on batteries. The RF transmit chain's high efficiency is crucial to successful deployment and general adoption by the community. Since the power amplifier consumes the most energy in the RF chain for these devices, it is desirable to minimize its losses.

This thesis's research addresses the impedance mismatch that occurs as power amplifiers impedance change over the frequency spectrum and how best to control the match using feedback. Power amplifiers offer a complex impedance (resistance and reactance) on their inputs and outputs. The matching networks on the inputs and outputs of the RFPA can be adjusted to provide optimal power transmission (maximizing forward power and minimizing reflections) using tunable elements (Leuzzi & Micheli, 2003). A tuned matching network can provide a gain performance increase of 32% over untuned networks (Thompson, Richardson, Davis, & White, 2005). The increase in efficiency would allow for energy to be conserved and help prolong the system's battery life. Implementation of adaptive feedback loops to control the tunable matching network provide enhanced performance over calibrated responses. There are several methods possible, and some are faster or more power-efficient than others (Po, de Foucauld, Morche, Vincent, & Kerherve, 2011)

Based on the problem presented, the purpose of this thesis is to design and analyze a working prototype of wideband tunable matching networks with feedback control for use with a power amplifier. The outcome of this research should yield a functional system that can answer the following hypothesis. Maximum forward power transmission into and out of the RFPA, conservation of energy, and dynamic optimization of a wideband RFPA is achievable using feedback-controlled tunable matching networks.

The system should tune the matching networks based on the RF transmission chain feedback within 100 milliseconds (ms). The system should also cover a tuning range of 500 MegaHertz (MHz) to 2.5 GigaHertz (GHz). The power output of RFPA should be between 27dBm and 30dBm after the matching network. These goals will be met using standard RF

design processes and maintain a low budget and physical footprint. These, however, are not constraints of the design but considerations to keep in mind throughout the process.

The significance of this work lies in its ability to configure the system appropriately. Proper configurations save energy, keep high transmission levels, allow for reconfigurability, and provide constant updates (Po, de Foucauld, Morche, Vincent, & Kerherve, 2011) (Gu & Morris, 2013). This type of system could exist in first responder and military-grade electronics, where battery power is a limiting factor, consistent transmission power is critical, and reconfigurability provides extensive communication techniques (Nesimoglu, Aydın, Atilla, Köprü, & Yarman, 2013). Loss of communication due to battery depletion or because the transmission power levels drop drastically is at least inconvenient and even potentially life-threatening in specific applications.

There is a definitive need for controlled tunable elements in the vast RF space. Providing any efficiency upgrade and control over a system will enable future technologies to utilize the RF spectrum better.

CHAPTER 2. REVIEW OF LITERATURE

2.1 Literature Review Introduction

The following chapter provides an overview of matching networks, power amplifiers, tunable elements, RF feedback topologies, detection methodologies, and control systems. The chapter explains how each element works individually, along with potential design considerations and challenges. Along with the considerations, each section gives theoretical calculations where applicable.

2.2 System and Device Impedance

Oliver Heaviside used the term Impedance for the first time in the nineteenth century to describe the complex voltage and current ratio of alternating current (AC) circuits (Pozar, 2011). Impedance is the inherent resistance to an alternating current that consists of resistance and reactance. Impedance (Z) is a complex number with a "Real" and "Imaginary" part, denoted by (Ω). Resistance (R) is the real value and has the same effect on direct current (DC) as AC. Power loss occurs through resistance. A typical example of a resistive element is a resistor. Reactance (X) is the imaginary part of the impedance and does not contribute to power loss. Reactive components are capacitors and inductors. In a circuit implementation, inductors do have internal resistance and thus produce a signal loss even though inductors are considered purely reactive. In its Cartesian form, impedance is expressed as follows in EQN(2.1). Note that the "j" in the equation denotes the imaginary term.

$$Z = R + jX \qquad \text{EQN(2.1)}$$

Resistors, capacitors, and inductors whose units are typical Ohms, Farads, and Henry's, respectively, can be transformed into their impedance equivalent. The impedance transformation for a resistor is simple. The nature of a resistor is frequency independent, so the resistance's value is the same as the impedance. EQN(2.2) shows the impedance transformation for a resistor. For capacitors and inductors, due to their reactive nature, the impedance for these devices is frequency-dependent. The definition of the term angular velocity (ω) is double the frequency (*f*)

multiplied by pi (π) EQN(2.3). The unit for ω is radians per second. EQN(2.4) and EQN(2.5) show the impedance calculations for a capacitor and inductor, respectively.

$$Z_R = R \quad \text{EQN(2.2)}$$

$$\omega = 2\pi f \quad \text{EQN(2.3)}$$

$$Z_C = \frac{-j}{\omega C} \quad \text{EQN(2.4)}$$

$$Z_L = j\omega L \quad \text{EQN(2.5)}$$

All devices in an RF signal chain will have impedance, either purely resistive, purely reactive, or complex. Even though the term impedance existed for many years prior, it was not until the 1930's that S. A. Schelkunoff recognized that the concept of impedance could be applied in a distributed manner to describe a system characteristic (Pozar, 2011). The system will also have an overall impedance as defined by its inputs and outputs. There are several standard system impedances, including 50Ω and 75Ω. For RF applications, the preference is a purely resistive 50Ω system. The reason dates to the development of coax cables for high power systems in the 1930s. Through examination, 77Ω provided the least amount of loss while 30Ω offered the best power handling. The geometric mean between these two, 50Ω, is used to compromise between power handling and loss. From here, many devices, cables, and connectors use the standard 50Ω impedance (Why Fifty Ohms?, 2020).

2.3 Static Matching Networks

The following sections outline the purpose and design of several different matching network topologies. The structure is as follows: why is a matching network important, what is a matching network, and the different network designs.

2.3.1 Why a Matching Network

When cascading devices in an RF signal chain, the device's input impedance must match the previous device's output. A system with a perfect match will have the source and load be equal impedances. When this occurs, the maximum amount of power transfers to the load (Pozar, 2011). Take *Figure 2.1*, for example, which shows a network consisting of a source and load impedance. The load will be adjusted and show how an impedance mismatch will affect the output voltage, current, and power.

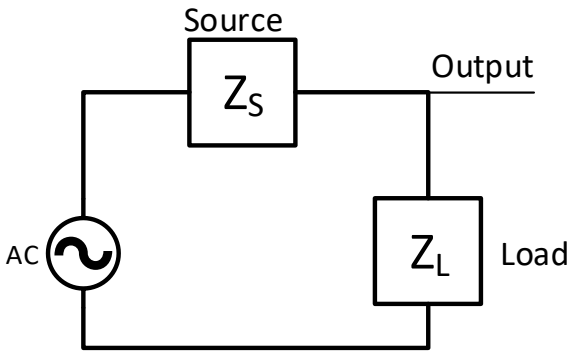


Figure 2.1: Basic Network Diagram

Normalization is a widely accepted form for generalizing impedances of an RF signal chain. In this case, the system source impedance sets the normalization. To normalize the system, divide the source and load impedances by the source impedance. Doing so means that the source's impedance will be 1, and the output will be scaled accordingly. EQN(2.6) and EQN(2.7) demonstrate this. Once the load impedance is normal, it is then used along with the input voltage to calculate the output voltage EQN(2.8), output current EQN(2.9), and output power EQN(2.10).

$$Z_{SNorm} = \frac{Z_S}{Z_S} = 1 \qquad \text{EQN(2.6)}$$

$$Z_{LNorm} = \frac{Z_L}{Z_S} \qquad \text{EQN(2.7)}$$

$$V_{out} = V_{in} * \frac{Z_{LNorm}}{Z_{LNorm} + Z_{SNorm}} \quad \text{EQN(2.8)}$$

$$I_{out} = \frac{V_{out}}{Z_{LNorm}} \quad \text{EQN(2.9)}$$

$$P_{out} = V_{out} * I_{out} \quad \text{EQN(2.10)}$$

To demonstrate how the mismatch affects the output, apply a 2 volt (V) signal onto the network's input. Adjust the load impedance from a normalized value of 0 to 100. As this change occurs, the voltage and current at the load also change. When the source and load are the same value, 1 in this case, the maximum amount of power is transferred to the load even though the current and voltage are only half their starting values. *Figure 2.2* shows the voltage, current, and power present at the load due to the change in load impedance compared to the input impedance. From the graph, the maximum power transfer of an RF system is when Z_{LNorm} is equal to Z_{SNorm} which in this case is 1. The phenomenon is the Maximum Power Transfer Theorem (Maximum Power Transfer Theorem, 2020). RF communications rely on power transfer, so having a system with matched impedances is crucial to its functionality.

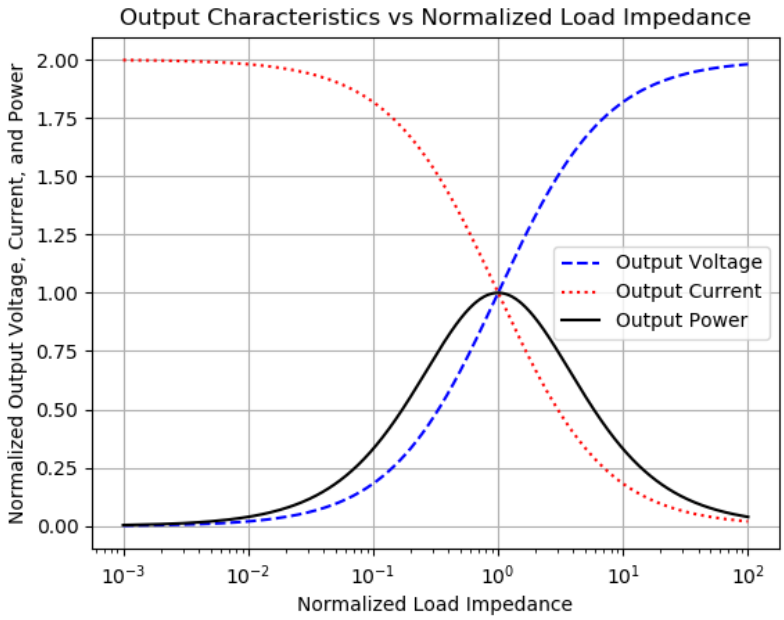


Figure 2.2: Output Characteristics vs. Normalized Load Impedance Based on EQN(2.8), EQN(2.9), and EQN(2.10)

2.3.2 What is a Matching Network

As mentioned earlier, some aspects of an RF system such as connectors, transmission lines, cables, and even individual IC's are pre-matched to a specific impedance making designs simple. When these parts are not available, the designer takes measures to fix the impedance mismatch by implementing a matching network. These are purely reactive circuits that transform one impedance into another, so all system components are matched accordingly. It is important to note that all the elements in a matching network be reactive to minimize losses. Reactive components are capacitors and inductors. These components theoretically will not dissipate power. If using a resistive element, the energy loss occurs due to the resistance.

Matching networks come in several different topologies and bandwidths. These are L, Tee, and Pi. Each of these also comes in high pass, low pass, and bandpass configurations. Tee and Pi networks also can be configured in a band stop configuration.

2.3.3 L Matching Network Topology and Analysis

L networks are the easiest to implement and get their name from the shape of the circuit. L networks are considered a narrow band matching network. As the operating frequency moves away from the design frequency, the matching network quickly begins to fail. For L networks, there is a series element and a shunt element. Proper configuration requires placing the series element between the shunt element and the lowest impedance, while the shunt element placement is adjacent to the highest impedance. *Figure 2.3* and *Figure 2.4* show the basic designs of L matching networks.

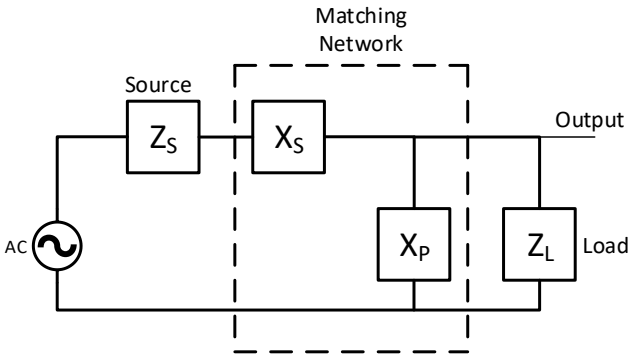


Figure 2.3: L Matching Network $Z_s < Z_L$

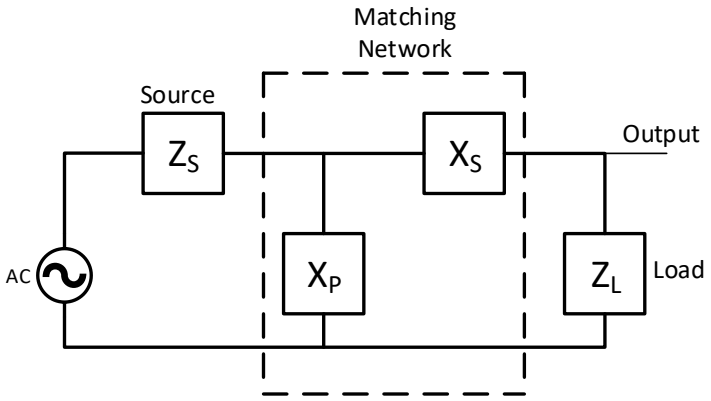
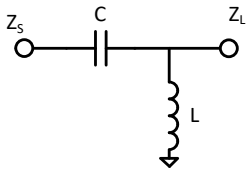
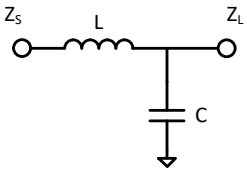
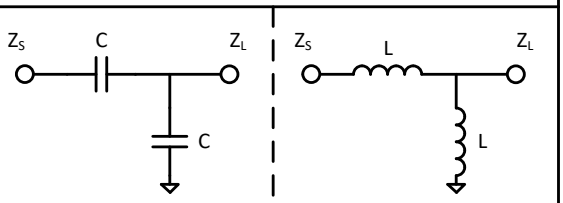
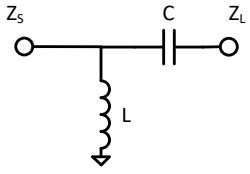
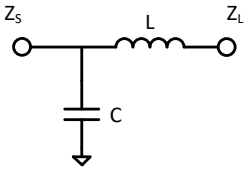
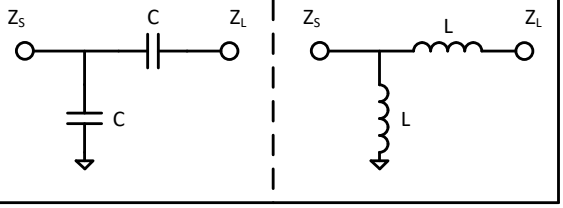


Figure 2.4: L Matching Network $Z_s > Z_L$

L Matching networks implement the two types of reactive elements, inductors and capacitors, producing eight different topologies (Bahl, 2003). *Table 2.1* shows the network configurations, their band properties, and what load to source impedance provides that topology. Note that matching networks are versions of highpass, lowpass, and bandpass LC filters.

Table 2.1: L Matching Network Options

	High Pass	Low Pass	Band Pass
$Z_L > Z_S$			
$Z_S > Z_L$			

For purely resistive sources and loads, the calculation of the components in the matching network is straightforward. The quality factor (Q) first needs to be determined. The quality factor is a unitless ratio that compares the input and output impedances. The equation for calculating Q is expressed in EQN(2.11) (Bahl, 2003).

$$if\ Z_S > Z_L\ then\ Q = \sqrt{\frac{Z_S}{Z_L} - 1} \quad \text{EQN(2.11)}$$

$$if\ Z_L > Z_S\ then\ Q = \sqrt{\frac{Z_L}{Z_S} - 1} \quad \text{EQN(2.12)}$$

After calculating Q, calculate the reactance of the series and shunt components. EQN(2.13) and EQN(2.14) show the calculations for these, respectively (Bahl, 2003), $Z_{Nearest}$ is the impedance to be matched closest to the series or shunt matching component.

$$X_s = Q * Z_{Nearest} \quad \text{EQN(2.13)}$$

$$X_P = \frac{Z_{Nearest}}{\mathrm{Q}} \quad \text{EQN(2.14)}$$

The final step for calculating the series and shunt components is taking the reactances and plugging them back into the respective components' impedance definition. The reactances derived in the previous step are those of the capacitor and the inductor chosen (Bahl, 2003).

$$L = \frac{X_L}{2\pi f} \quad \text{EQN(2.15)}$$

$$C = \frac{1}{2\pi f X_C} \quad \text{EQN(2.16)}$$

2.3.4 Cascaded L Matching Networks

One of L networks' intriguing parts is their ability to be cascaded to create different impedance matches and at much wider bandwidths. These are typically to create bandpass matching networks. A typical design of an L matching network works for only one frequency, but a bandpass network will better match a wide range of frequencies. The bandpass matching

network is just a lowpass matching network cascaded in series with a highpass network. *Figure 2.5* and *Figure 2.6* show the typical cascaded L matching network (Breed, 2008).

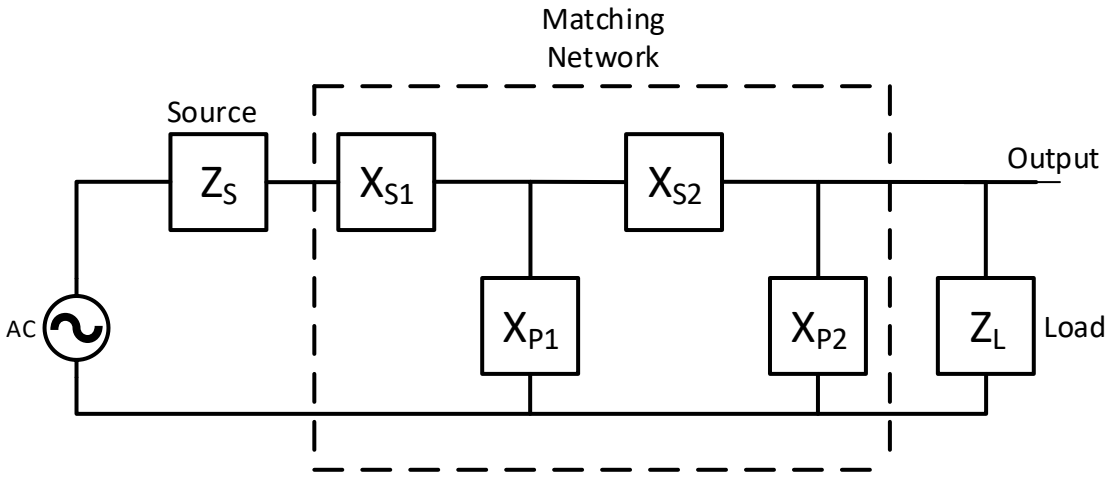


Figure 2.5: Series Shunt Cascaded L Matching Network

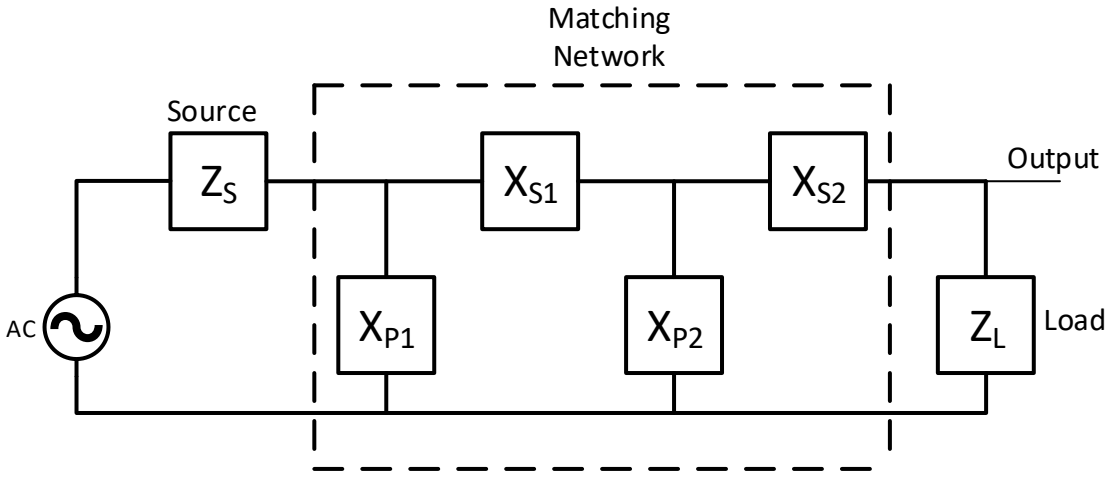


Figure 2.6: Shunt Series Cascaded L Matching Network

To calculate the network components' values, use a similar design process to simple L matching networks. First, place a theoretical resistance between the two L Networks. Note that this theoretical resistance is not in the final circuit. This resistance is simply a common point to match each half of the network too. When solving for the left L network, this resistance is the load, and when solving for the right side matching network, this is the source. The same equations for quality factor and reactance still apply to this. *Figure 2.7* shows the cascaded L

matching network with theoretical resistance. The theoretical resistance which is the geometric mean of Z_L and Z_s can be calculated, as shown in EQN(2.17).

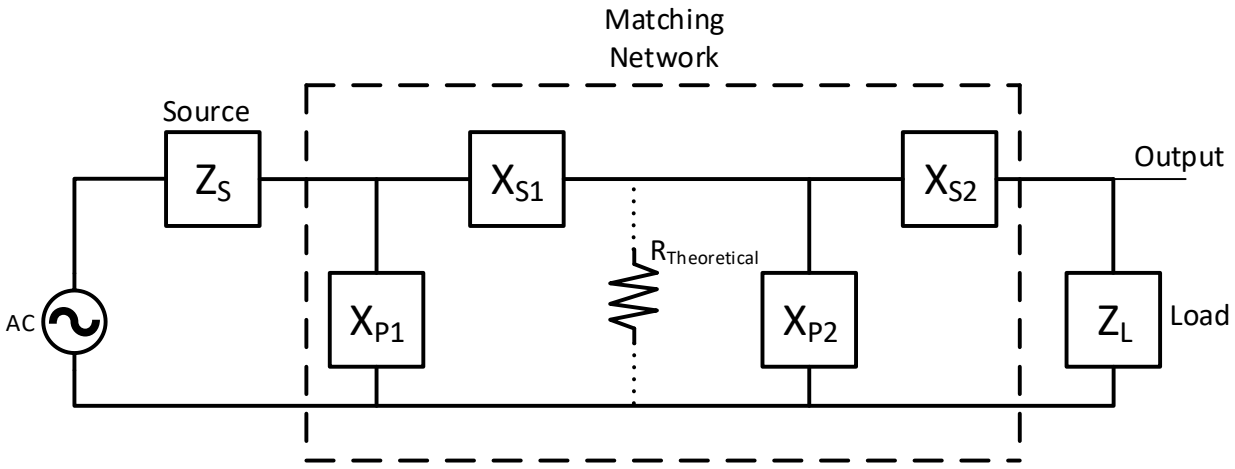


Figure 2.7: Theoretical Resistance for Cascaded L Network Design

$$R_{Theoretical} = \sqrt{Z_s * Z_L} \qquad \text{EQN(2.17)}$$

After calculating the reactance's, solve for the component values. It is at this point where the increased bandwidths come in. Bandpass matching networks have two break frequencies f_{low} and f_{high} at the band edges, which are chosen based on application. One of the L network configurations is for lowpass, and the other is for highpass. The low pass L network uses $f_{High,}$ and the high pass L network uses the f_{Low} parameter.

2.3.5 Pi and Tee Matching Networks

Pi and Tee networks are a form of three-element matching. They offer several advantages over L networks; wider bandwidth and adjustable Q. All components have a specific Q based on their physical properties, and this cannot be changed. Recalling EQN(2.11) and EQN(2.12), the required component Q of the L network is fixed based on the source and load impedances. Cascaded L networks Q is also fixed because of the intermediate impedance in EQN(2.17), based on the source and load impedances. The Q of the component must be higher than the required Q of the network, or the system will not function properly. Pi and Tee networks have an adjustable Q because the designer can pick the intermediate impedance. The only criteria for the

intermediate impedance for Pi networks are that it must be lower than both the source and load impedances. For Tee networks, the intermediate impedance must be higher than the source and load. The larger the impedance mismatch, the higher the required Q. Therefore, it will be in the best interest of the designer to pick a topology that has the smallest impedance transformation to keep the network Q sufficiently low compared to components. For these networks, it does not matter if the source or load impedance is higher like it does for L networks (Bowick, 2008).

Pi and Tee Matching networks are very similar to the cascaded L matching network design process. The networks are solved essentially the same way but account for a common part in the last step. Pi and Tee networks get their name the same way that L networks do by their shape. *Figure 2.8* and *Figure 2.9* show the Pi and Tee Network designs, respectively. Pi and Tee networks are considered a more wideband approach to matching networks (Bowick, 2008).

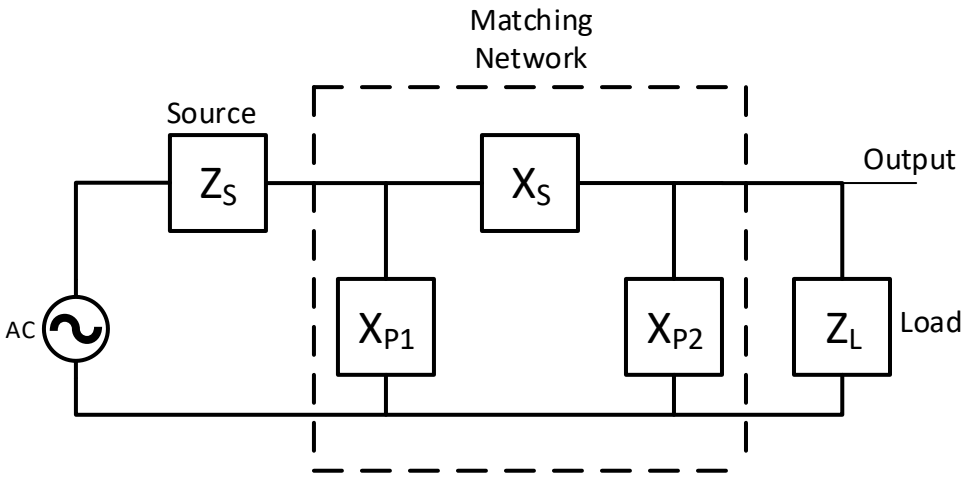


Figure 2.8: Generic Model of Pi Matching Network

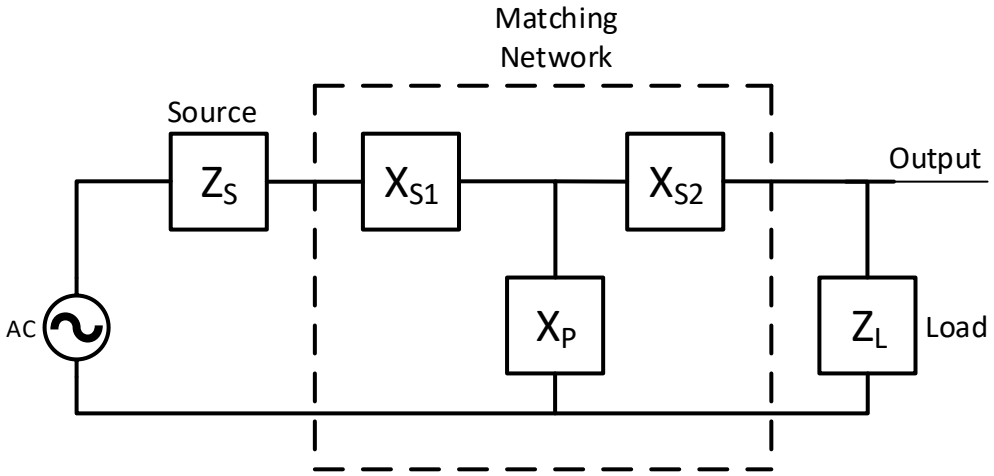


Figure 2.9: Generic Model of Tee Matching Network

When designing the networks, the first thing to do is split the network into two back-to-back L networks with a theoretical resistance in the middle. From here, solve the networks as cascaded L networks. *Figure 2.10* and *Figure 2.11* show how to split the Pi and Tee networks, respectively (Bowick, 2008).

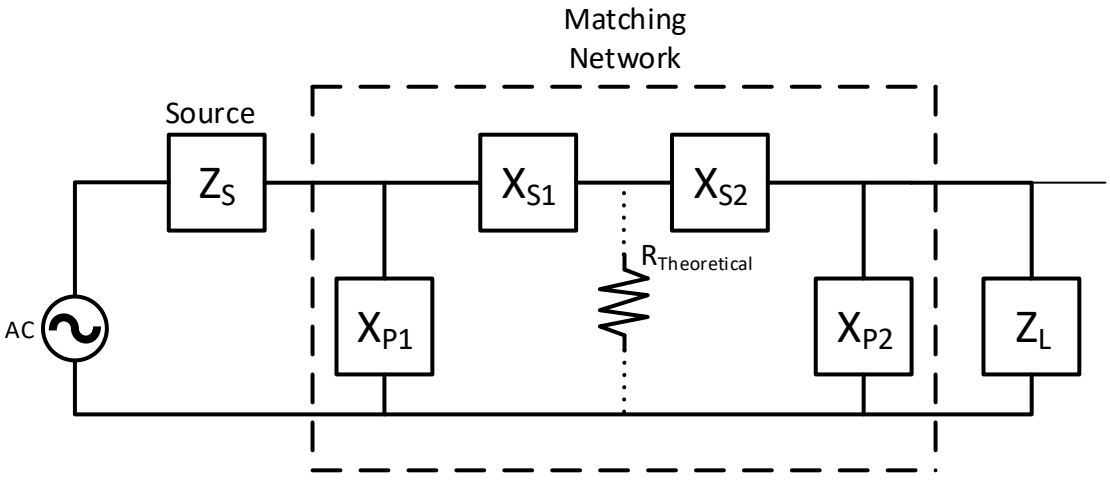


Figure 2.10: Pi Network With Theoretical Resistance

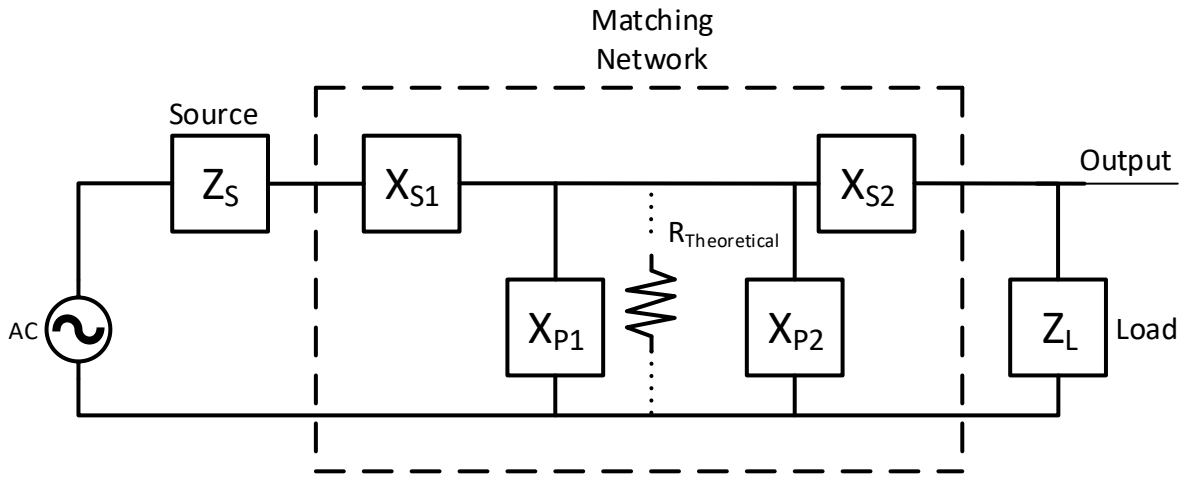


Figure 2.11: Tee Network with Theoretical Resistance

After solving the split network reactances, the center's reactances need to be combined. Combining reactances before converting to components is the easiest way to combine the components. Combining the reactances starts with one of the four topology options in *Figure 2.12* for Pi Networks or *Figure 2.13* for Tee Networks.

For Pi Networks, combine the center reactances in series by adding the two series reactances to obtain total reactance. Convert the total reactance back into an equivalent reactive component.

For Tee networks, combine the center components in parallel. Do this by using EQN(2.18) to obtain the total parallel reactance. The last step is to convert the combined reactance back into an equivalent reactive component.

One thing to note is that the individual L networks need to have one capacitor and inductor. Both components on the same half of the L network cannot be the same type. *Figure 2.12* and *Figure 2.13* show the lumped element options for Pi and Tee Networks (Bowick, 2008).

$$\frac{1}{(\frac{1}{X_{P1}} + \frac{1}{X_{P1}})} \qquad \text{EQN(2.18)}$$

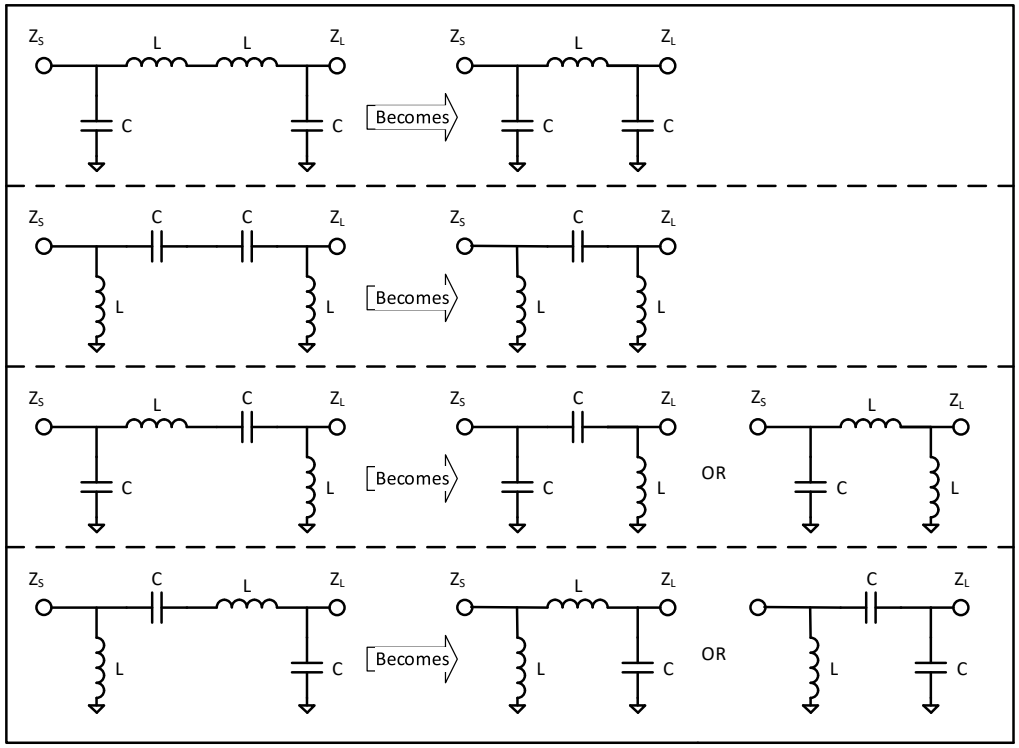


Figure 2.12: Lumped Element Pi Network Configurations

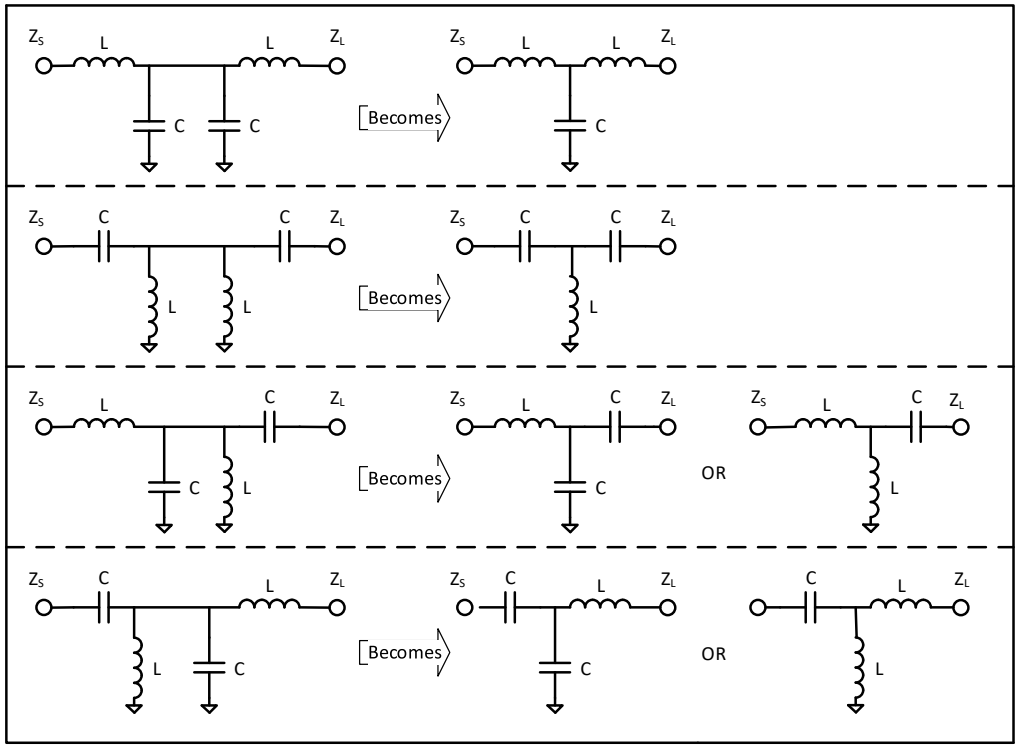


Figure 2.13: Lumped Element Tee Network Configurations

2.3.6 Correcting for Complex Loads

Up to this point, for simplicity, loads have been considered to be purely resistive to make the math simple. As load and source impedances introduce their reactive elements, the mathematics behind the matching network's development becomes increasingly involved. A simple way to solve the problem would be to place a series or shunt component with the complex impedance to achieve a purely resistive impedance (Breed, 2008). *Figure 2.14* and *Figure 2.15* show how adding a reactive element to a load can create a purely resistive load. The same principle applies to source impedances.

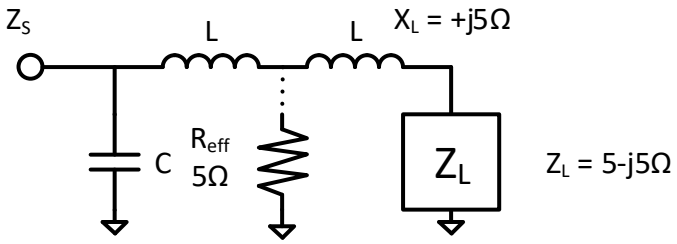


Figure 2.14: Series Circuit for Realization of Resistive Load (Breed, 2008)

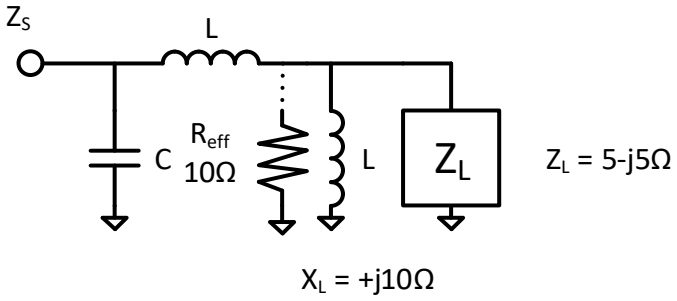


Figure 2.15: Shunt Circuit for Realization of Resistive Load (Breed, 2008)

2.3.7 Summary of Matching Networks

As can be seen, matching networks play a significant role in the RF signal chain. Ensuring a matched circuit guarantees maximum power transfer to the load and minimizes power loss from reflections. Matching Networks come in many shapes and configurations but are often straightforward to produce. Here is a quick recap of the different types of networks covered.

- L Networks:
    - Consists of two reactive elements in an "L" configuration
    - Narrow bandwidth
    - Can be cascaded easily
    - Simple to design
    - Does not handle complex source and load impedances well
- Pi Networks
    - Consist of 3 components in a "π" configuration
    - Offers wideband matching
    - Is based on back to back L networks
    - Medium complexity to design
- Tee Networks
    - Consists of 3 components in a "T" configuration
    - Offers wideband matching
    - Is based on back to back L networks
    - Medium complexity to design
- Cascaded Networks
    - Consist of back to back L networks
    - Provides the widest bandpass options compared to the rest of the networks
    - Medium to high level of complexity to design

2.4 Power Amplifier Classification and Designs

Power amplifiers are common components in RF signal chains and are extensively studied. These devices take low power signals and amplify the signal power to drive some load. The most basic options are going to be covered. Amplifiers come in different "classes" these are standard operating topologies, and each comes with benefits and challenges. Along with the different types of amplifiers, there are basic principles of amplifiers that need to be covered.

2.4.1 Parameters of a Power Amplifier

RFPA's have several characteristics that are important to understand before discussing the different classifications. These are gain, 1dB compression, efficiency, transistor type, and impedance. The following sections cover these topics before moving on to discussing the different power amplifier classes.

2.4.1.1 Gain

Power amplifiers are designed for one task, provide gain to a signal at its input. Gain is defined as the output power (P_{out}) compared to input power (P_{in}), both in Watts. Typically gain for a power amplifier is in dB, which is a logarithmic representation. Gains represented linearly, especially at high power, can be vary enough that it is easier to transform everything into a log scale for simplicity. Characterizing an amplifier gain in dB also allows it to be calculated in the system easier since log gains add. To calculate the power gain of an amplifier, use the formula shown in EQN(2.19).

$$G = \frac{P_{out}}{P_{in}} \quad , \quad G_{dB} = 10 * \log\left(\frac{P_{out}}{P_{in}}\right) \qquad \text{EQN(2.19)}$$

2.4.1.2 1dB Compression Point

Another critical characteristic of an amplifier is its 1dB compression point. Typically power amplifiers have a set gain. As the input power increases and decreases, so does the output power by the same amount. This phenomenon is known as the linear region of operation. The 1dB compression point is where the amplifier's gain has dropped by 1dB from the amplifier's expected gain. At this point, extra harmonics and unwanted noise, along with the amplifier saturation, begin to occur. When this occurs, the amplifier is in its nonlinear region of operation. RF amplifiers need to operate below the 1dB compression point. *Figure 2.16* shows the principle for the 1dB compression point (Pozar, 2011).

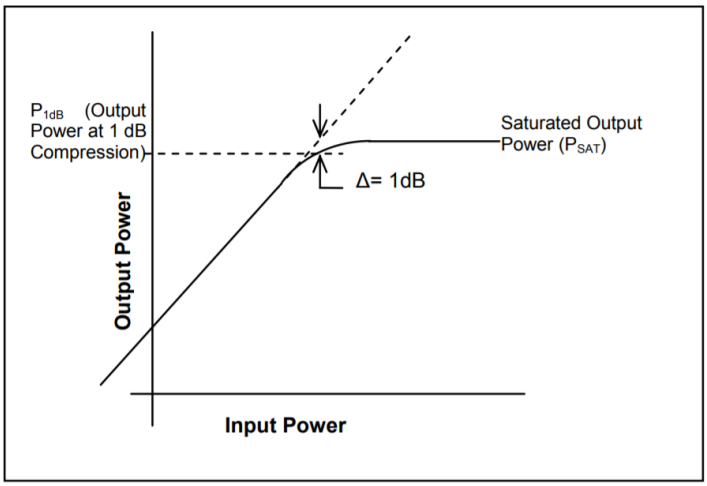


Figure 2.16: 1dB Compression Point (Mini-Circuit, 2015)

2.4.1.3 Efficiency

The power amplifier is typically the largest consumer of DC power (P_{DC}) in most handsets. When measuring the power efficiency of a device, compare the output power to the input power. For RFPA's, however, the output power is measured in relation to the DC power. This measurement does not account for any RF power on the input of the device. Instead, power added efficiency can be used instead of traditional efficiency techniques. Power added efficiency (PAE) takes into account the input power (P_{in}), output power (P_{out}), and DC power (P_{DC}) of the device, in Watts, to give a more reasonable approximation to the efficiency of the device. EQN(2.20) shows the calculations for PAE. Note that G is the gain of the amplifier from EQN(2.19) (Pozar, 2011).

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right) * \frac{P_{out}}{P_{DC}} \qquad \text{EQN(2.20)}$$

Along with the amplifier gain and its efficiency, the output type is either linear or switching. Linear amplifiers are inherently lossier than switching amplifiers but create a more accurate output waveform. Switching amplifiers are suitable for constant envelope waveforms, where high distortion is ok, but most applications require as little distortion as possible (Pozar, 2011).

*2.4.1.4 **Transistor Types***

Transistors come in various topologies, which break up into two major categories, Bipolar Junction Transistors (BJT) and Field Effect Transistors (FET). The BJT comes in two configurations, standard BJT and Heterojunction Bipolar Transistor. BJT's are among the oldest types of transistors and still find use in RF applications to this day. The device acts as a current-controlled current source. As the base current changes, the collector current changes as well. The BJT offers good operating performance in terms of its frequency range, power efficiency, cost, and ease of biasing. One drawback is a higher noise figure that exists because of the shot noise created in the transistor. *Figure 2.17* shows the equivalent circuit for a Bipolar Junction Transistor. Typically, one ignores the capacitance of C_C because it is small enough not to have significant effects. A Heterojunction Transistor (HBT) is almost identical to a BJT except in the semiconductor layer layout. The semiconducting layer of an HBT breaks into several different layers, unlike a single layer BJT's. This topology allows for high electron mobility increasing frequency range (Pozar, 2011).

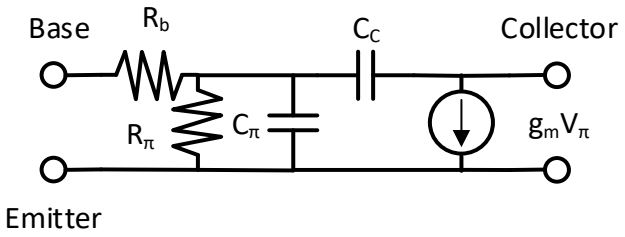


Figure 2.17: Simplified Hybrid π Equivalent Circuit of Junction Transistor in Common Emitter Configuration (Pozar, 2011)

As mentioned, the other type of transistor is the Field Effect Transistor (FET). These devices come in various device types (Metal Semiconductor FET, Metal Oxide Semiconductor FET, and High Electron Mobility Transistor). The device acts as a voltage-controlled voltage source. This principle means that as the gate's input voltage is adjusted, the device changes the source voltage. *Figure 2.18* is the equivalent circuit for a FET in a common source configuration. Metal Semiconductor FET's (MESFET's) are one of the enabling technologies for microwave applications. The GaAs topology allows for excellent electron mobility and, thus, high-frequency operation. Along with the increased frequency range, the device's high electron mobility characteristics eliminate shot noise present in BJT devices (Pozar, 2011).

The Metal Oxide Silicon FET (MOSFET) is one of the most common FET's. The MOSFET is similar to MESFET's but with an additional insulating layer between the gate and channel. This type of device does not have the same frequency range or power handling as other FET's but is simple to bias and very cost-effective for lower-powered applications. The High Electron Mobility Transistor (HEMT) is a heterojunction FET. The principle behind it is the same as an HBT. The semiconducting layer is broken up into different materials to achieve a better frequency response while also having high power handling capabilities (Pozar, 2011).

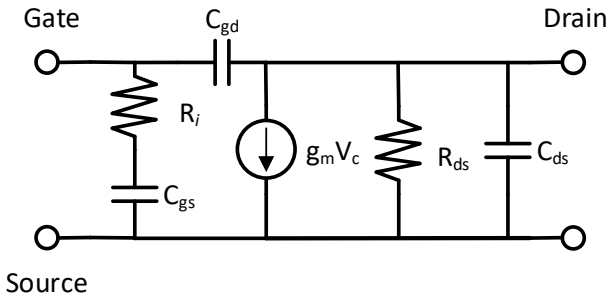


Figure 2.18: Small-signal Equivalent Circuit for FET in Common-source Configuration (Pozar, 2011)

Each transistor has its strengths and weaknesses and must be chosen carefully depending on the application. *Table 2.2* summarizes and compares all the mentioned transistor types.

Table 2.2: Performance Characteristics of Transistors (Pozar, 2011)

Device	BJT	HBT	CMOS	MESFET	HEMT	HEMT
Semiconductor	Si	SiGe	Si	GaAs	GaAs	GaN
Frequency range (GHz)	10	30	20	60	100	10
Typical gain (dB)	10–15	10–15	10–20	5–20	10–20	10–15
Noise figure (dB)	2.0	0.6	1.0	1.0	0.5	1.6
(frequency, GHz)	(2)	(8)	(4)	(10)	(12)	(6)
Power capacity	High	Medium	Low	Medium	Medium	High
Cost	Low	Medium	Low	Medium	High	Medium
Single-polarity supply	Yes	Yes	Yes	No	No	No

2.4.1.5 Transistor Impedances

One thing to note is that each transistor is different and will have different typical impedances at different frequencies. Meaning there are no general values of impedances for transistors. It is typically easier to get the scattering parameters of a particular transistor and use those to calculate the impedance than to try and model the transistor (Pozar, 2011).

2.4.2 Amplifier Classes

With all transistors used in RF applications, the amplifier must be biased to achieve the desired amplification. The different biasing techniques define the different "Classes" of amplifiers.

2.4.2.1 Class A Amplifier

Class A amplifiers are a class of linear amplifiers that runs a transistor in its linear region all the time. The transistor in this amplifier acts as a current source controlled by the gate voltage, which is biased into allowing the transistor always to be conducting. When a sine wave passes through the amplifier, the transistor will pass the entire wave out, assuming no violation of the amplifier's gain design. Another way to state this is that the transistor has a conduction angle of 360° (Kazimierczuk, 2015). Class A amplifiers are typically the least efficient amplifier with a theoretical max at 50% efficiency (Raab, et al., 2002).

On the other hand, Class A amplifiers offer high gain, good linearity, and operate up to the transistors maximum frequency (Raab, et al., 2002). *Figure 2.19* shows a standard class A amplifier. Note that there are two voltage sources in series. The DC source is used to bias the transistor into its conduction region, and the AC source is the RF input signal that will modulate the transistor. *Figure 2.20* shows the waveform of this circuit (Kazimierczuk, 2015). Here the amplifier gain was set to 2.5. The time and voltage scales are normal for generalization purposes. Assume a DC blocking section of the filter/matching network stage to remove the DC offset caused by the single-sided amplifier design.

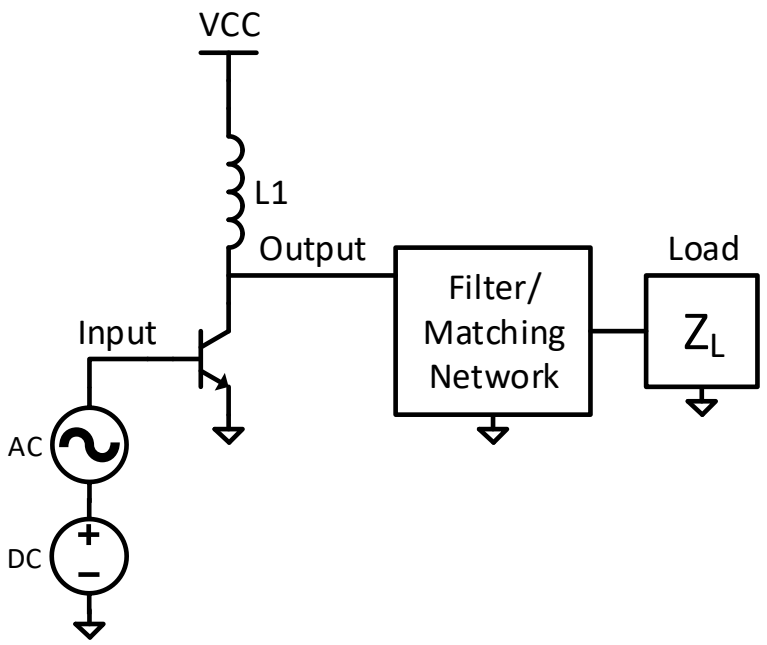


Figure 2.19: Class A Amplifier Basic Design

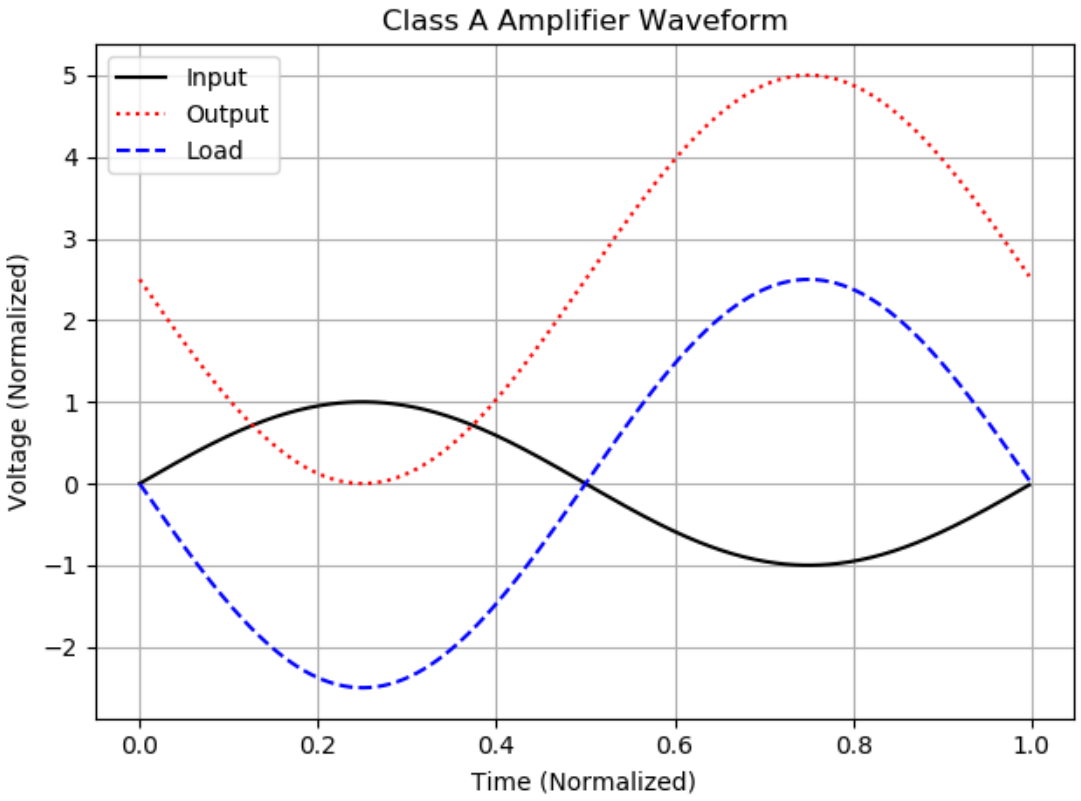


Figure 2.20: Class A Amplifier Output Waveform

2.4.2.2 Class B Amplifier

Class B amplifiers are another form of a linear amplifier, but unlike Class A, where the transistor is biased into conduction for both the positive and negative cycles of a sine wave. Class B Amplifiers are biased at its conduction threshold (V_t), so it only transmits half the wave (Kazimierczuk, 2015) to the load. Due to each transistor's conduction angle being 180°, these kinds of amplifiers have a higher efficiency than Class A amplifiers, upwards of 78%. Currently, Class B amplifiers are standard in wideband applications (Raab, et al., 2002). Two complementary transistors are required for the amplifier because each is biased to output only half of the waveform. This configuration is known as a complementary amplifier. This topology allows for the recreation of most of the entire waveform. One issue with this amplifier is that both transistors are off at the zero-crossing, causing a small amount of distortion (Kazimierczuk, 2015). *Figure 2.21* shows the basic circuit design for a complimentary Class B amplifier. The boxes that state "Bias = V_t" are placeholders for circuits that would be used to bias that transistor to its threshold voltage. *Figure 2.22* shows the common voltage waveforms of a Class B Amplifier (Kazimierczuk, 2015). Note for the waveforms that state either "NPN Transistor Conduction Waveform" or "PNP Transistor Conduction Waveform"; the flat line is when the transistor is no longer conducting. One sees that each waveform for each transistor starts and stops conducting at exactly the zero crossing.

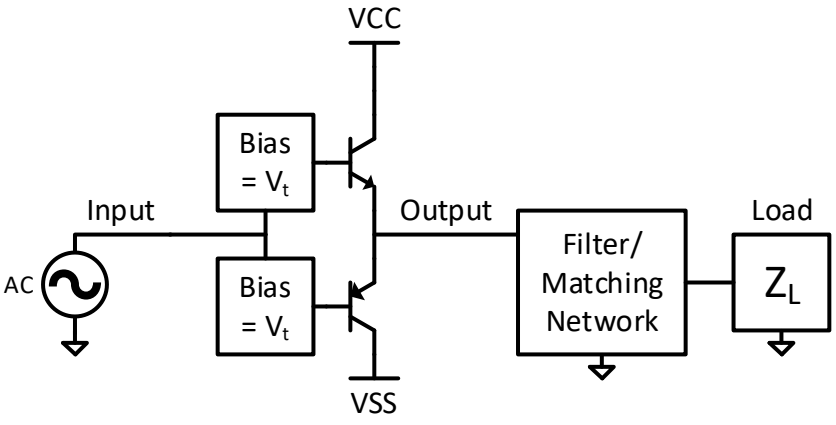


Figure 2.21: Class B Complementary Amplifier Basic Design

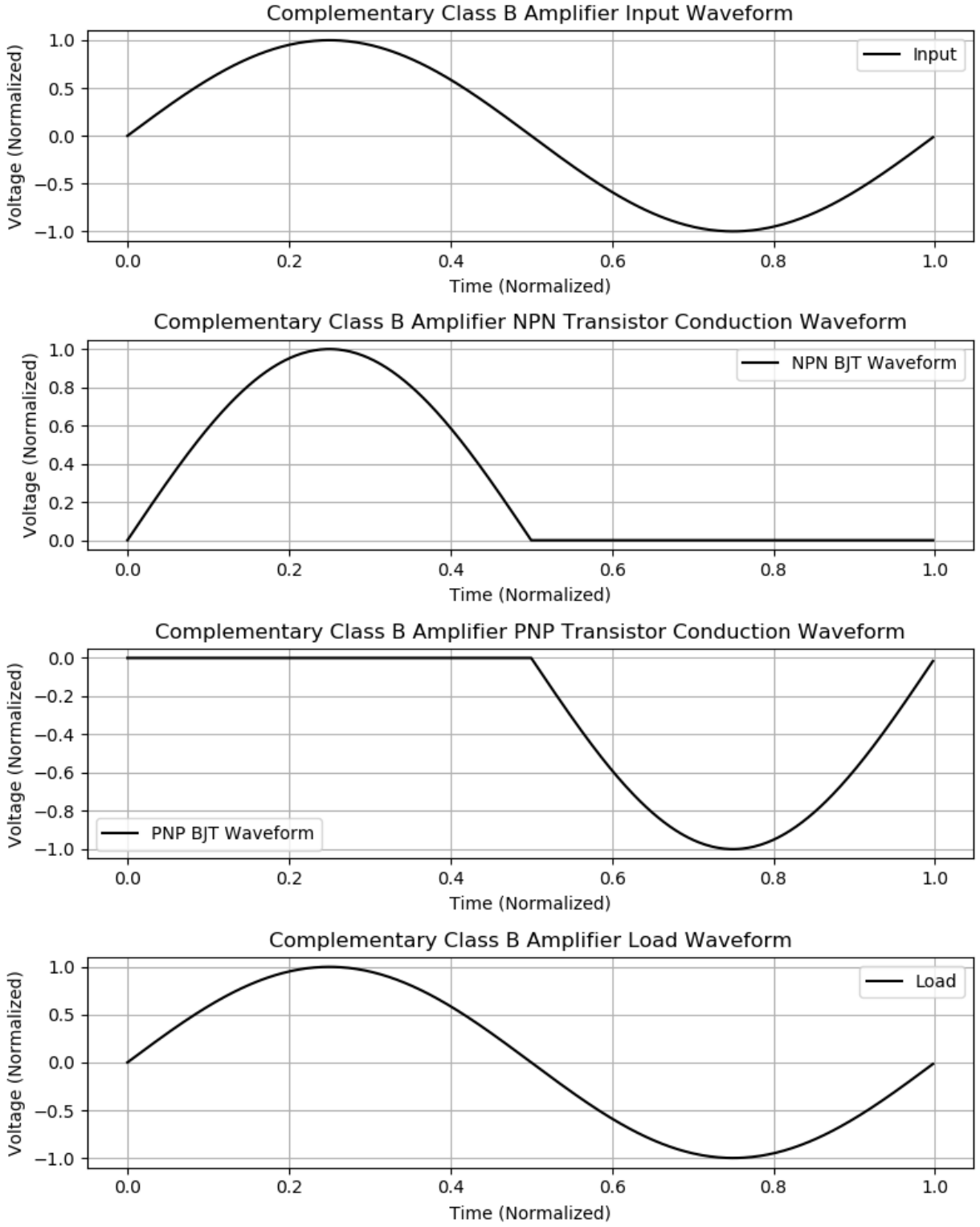


Figure 2.22: Class B Amplifier Waveforms

2.4.2.3 Class AB amplifier

Class AB amplifiers are a combination of Class A and Class B Amplifiers. This classification is similar to Class B amplifiers in that each transistor only conducts for part of the input waveform. However, it is related to Class A amplifiers in that each transistor conducts more than half of the waveform. A Class AB amplifier's conduction angle is between 180° and 360° (Raab, et al., 2002). Each transistor is biased just beyond its threshold voltage to begin the transistor's conduction early. The efficiency of this amplifier sits between Class A and Class B. Each transistor is only conducting part of the time, unlike Class A, which is all the time but is not as efficient as Class B since each transistor is conducting more than that configuration. An advantage of this amplifier is that it fixes Class B amplifiers' distortion at the zero crossing by allowing both transistors to be still conducting (Kazimierczuk, 2015). *Figure 2.23* shows the basic design of a Class AB complementary amplifier.

Note that the bias blocks here have the same effect as in the Class B amplifier section but are adjusted to conduct the transistors before reaching the threshold voltage. *Figure 2.24* shows the typical voltage waveforms of this amplifier class (Kazimierczuk, 2015). The flat portions of the "NPN Transistor Conduction" and "PNP Transistor Conduction" waveforms are when the transistors are no longer conducting.

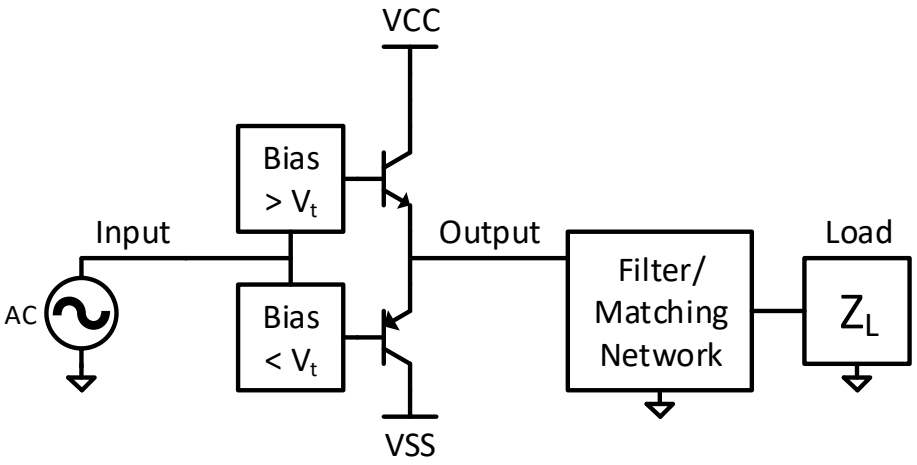


Figure 2.23: Class AB Complementary Amplifier Basic Design

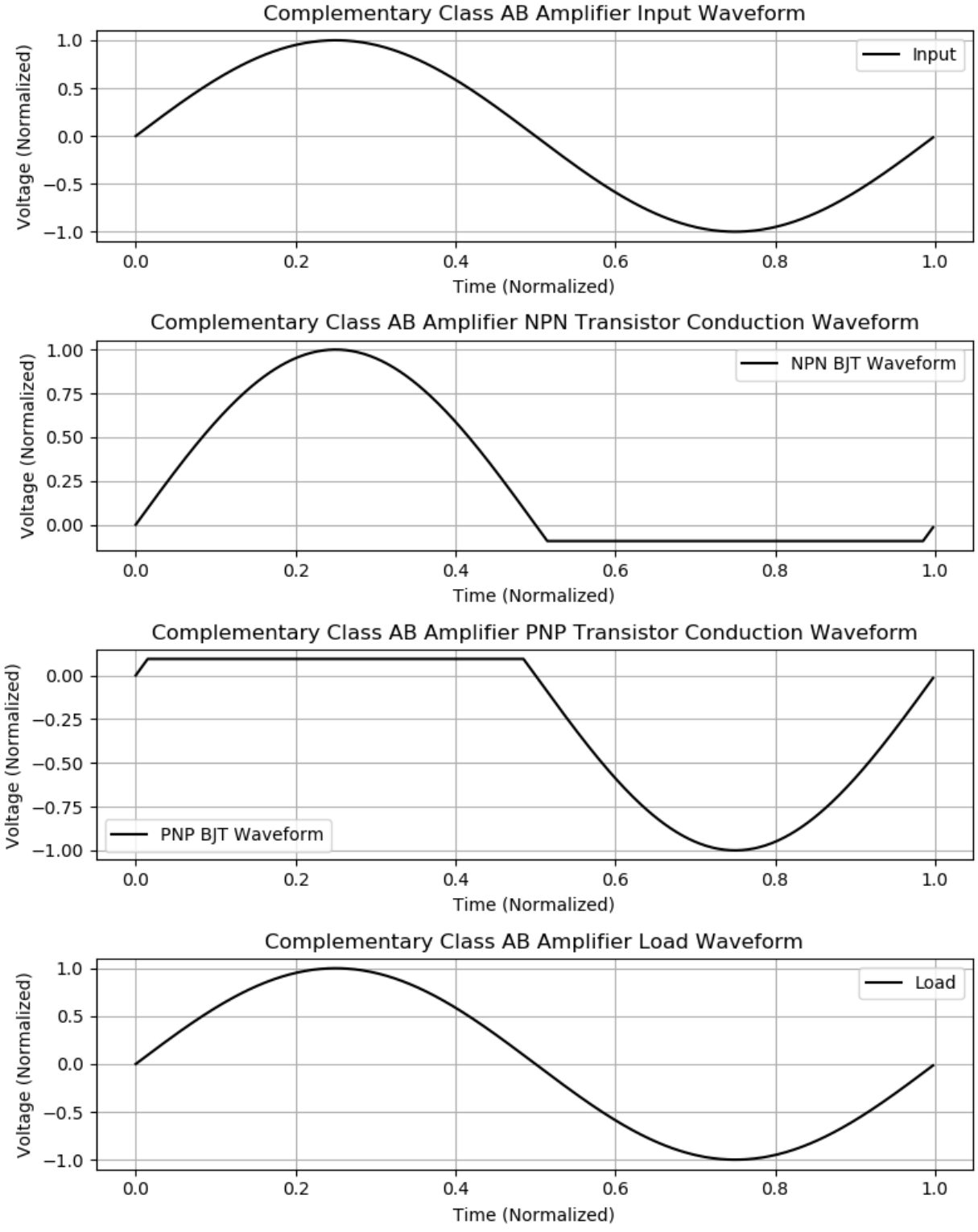


Figure 2.24: Class AB Amplifier Waveforms

2.4.2.4 Class C Amplifier

Class C amplifiers are the last form of linear amplifiers to be covered. These amplifiers have the highest efficiency and worst linearity out of all the previously mentioned linear amplifiers. This amplifier class can almost reach 100% efficiency by changing when the transistors will begin conducting. The bias of each transistor is below its respected threshold voltage. A typical conduction setting for this amplifier is to set the threshold to occur when the input waveform is conducting for 150°. This conduction angle gives the amplifier efficiency of 85%, which means that each transistor will conduct less than half of each waveform cycle. Due to the waveform not being entirely recreated, this amplifier adds a significant distortion to the amplified signal. Class C amplifiers are only commonly found in vacuum tube transmitters or when the transmitted wave has a constant envelope (Raab, et al., 2002). *Figure 2.25* shows the basic design of a Class C Amplifier. It shares the same topology as the Class B and AB amplifier, but the Bias blocks are below the transistor's threshold voltage. *Figure 2.26* shows the typical waveforms of this type of amplifier (Kazimierczuk, 2015). As in the previous designs, the flat sections of the "NPN Transistor Conduction" and "PNP Transistor Conduction" are when those transistors are not conducting. The load and output voltage are identical as well in this amplifier design.

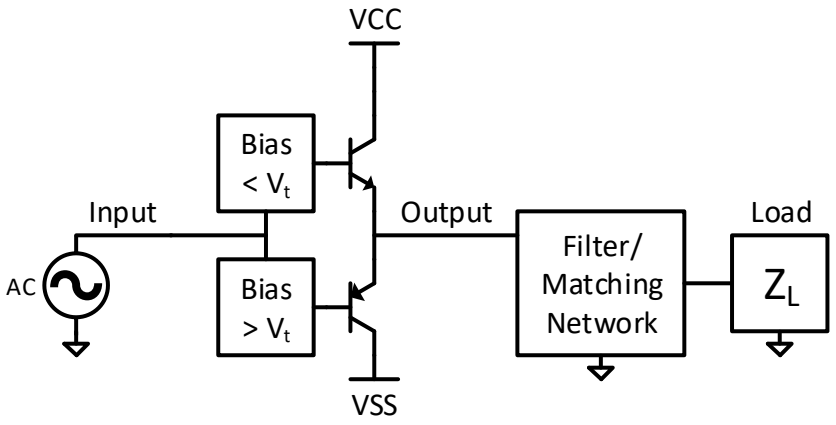


Figure 2.25: Class C Complementary Amplifier Basic Design

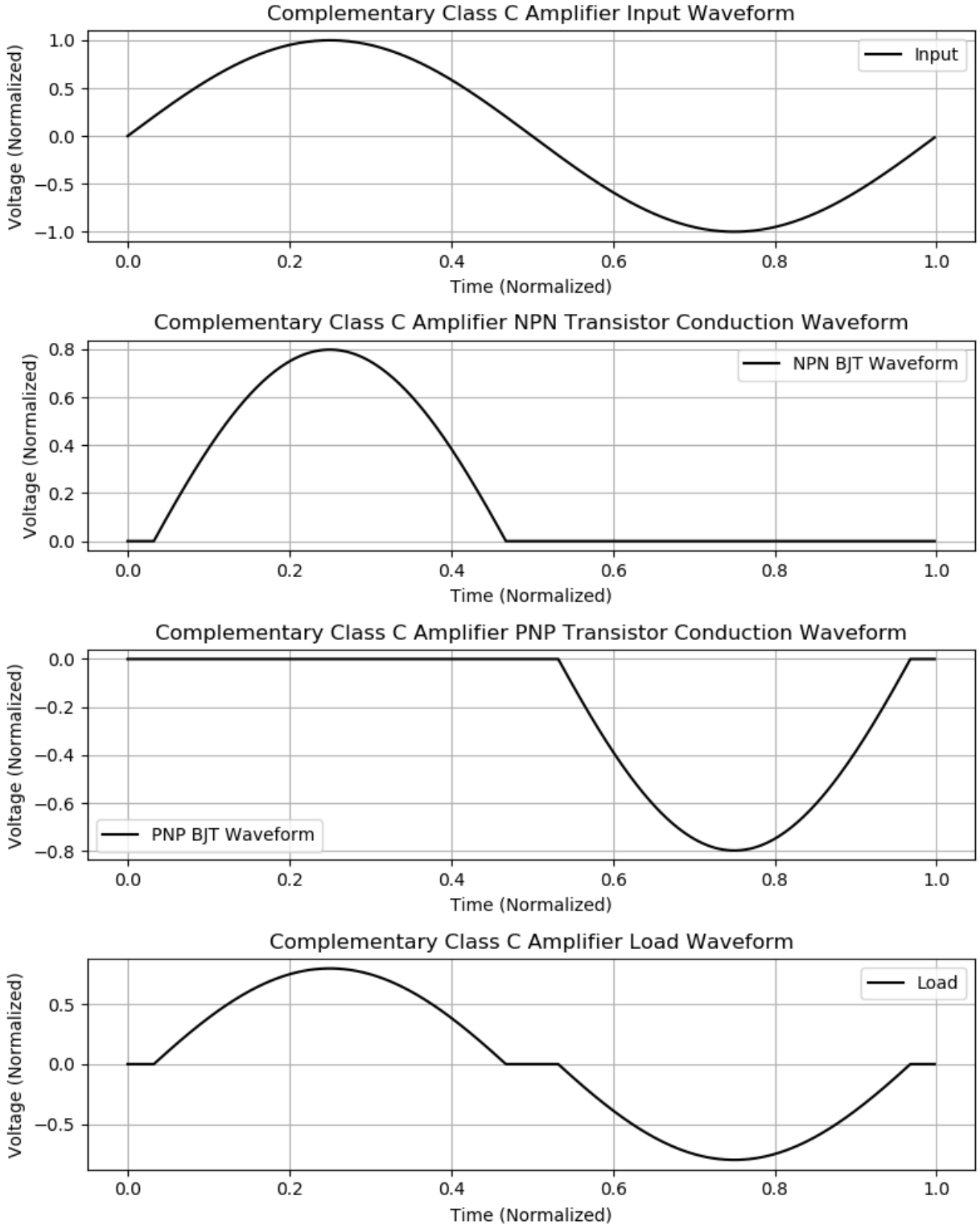


Figure 2.26: Class C Amplifier Waveforms

2.4.2.5 Class D Amplifier

Class D amplifiers fall under the classification of "Switching" amplifiers. This amplifier implements a complementary amplifier design. However, unlike the previous classes of amplifiers, each transistor will be driven into saturation, causing it to act like a switch rather than a variable source. In saturation, the transistors' resistance is minimal compared to when it is conducting in its linear region. The reduction in transistor losses leads to improved efficiencies.

This amplifier requires the input to be a PWM signal that is proportional to its output. The amplifier's output is a PWM version of the desired signal, and it must pass through a low pass filter. The filter removes the high-frequency switching and instead passes only the fundamental frequency out of the amplifier. Also, because the transistors are going into saturation, the drain to source capacitance becomes a significant issue and limits the maximum switching speed.

The switching speed needs to be several orders of magnitude higher than the desired output frequency, or else the amplifier output will show the PWM signal. Slow switching speeds lead to linearity and distortion problems. Also, if the amplifier is switching fast enough, it will spend more time in its linear region than in its saturation state, which will cause the efficiency of the amplifier to go down as well. This amplifier's realistic implementations only up to 1GHz (Raab, et al., 2002).

Figure 2.27 shows the basic design of a Class D amplifier. The bias circuitry avoids the transistors' cross conduction and drives the transistors into saturation (Kazimierczuk, 2015). Note that the transistors effectively become switches in this figure, represented by the arrow showing the transformation. *Figure 2.28* shows the input and filtered output of a Class D amplifier to remove the PWM signal. The PWM input is the direct representation of a sine wave at the normalized frequency and voltage.

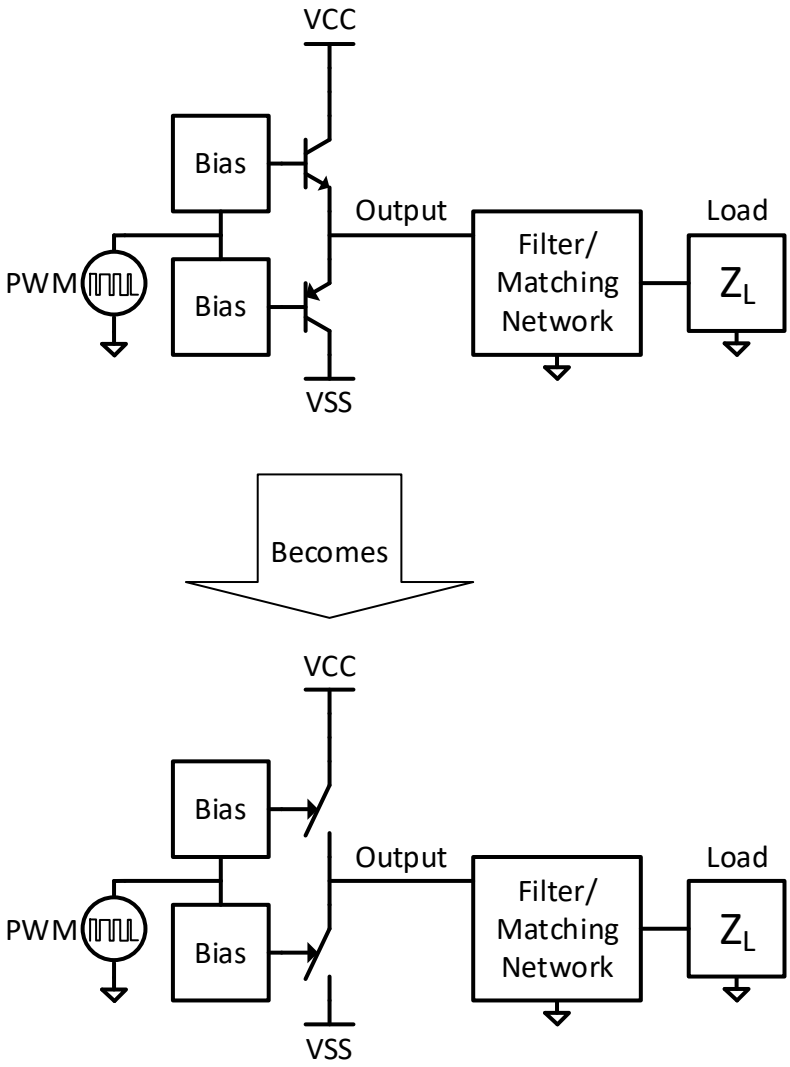


Figure 2.27: Class D Amplifier Basic Design

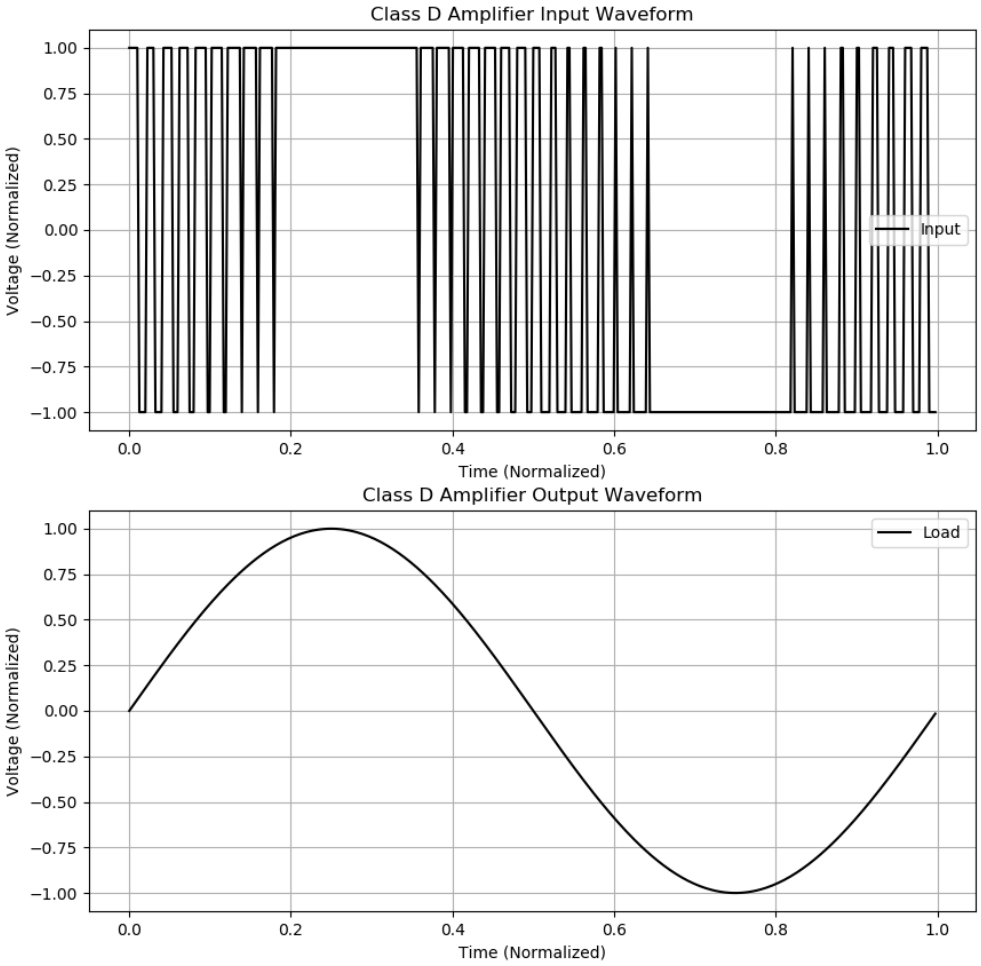


Figure 2.28: Class D Amplifier Waveforms

2.4.2.6 Class E Amplifier

The Class E amplifier is another form of switching amplifier. It can come in two configurations zero voltage and zero current switching. The amplifier operates by switching the transistor on and off at a set time and uses it to charge and discharge a resonating circuit. The resonating circuit takes the switched wave, turns it into an AC wave, and transmits it to the load. The resonating circuit is highly dependent on frequency and load impedance. When tuned correctly, the transistor switches at the zero crossings for either the current or the voltage. Any misalignment in this causes the amplifier to lose efficiency. Though incredibly efficient, the amplifier does not have a broad bandwidth and has a limited overall frequency range. *Figure*

2.29 and *Figure 2.30* show the circuit for a Class E Zero Voltage Crossing Amplifier and its subsequent waveforms. *Figure 2.31* and *Figure 2.32* show the circuit for a Zero Current Crossing amplifier and its waveforms. The output of the amplifier should be sinusoidal (Kazimierczuk, 2015).

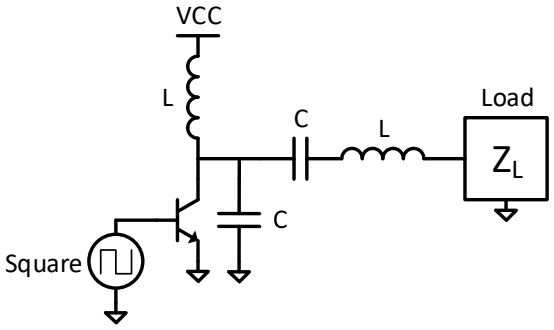


Figure 2.29: Class E Zero Voltage Crossing Amplifier

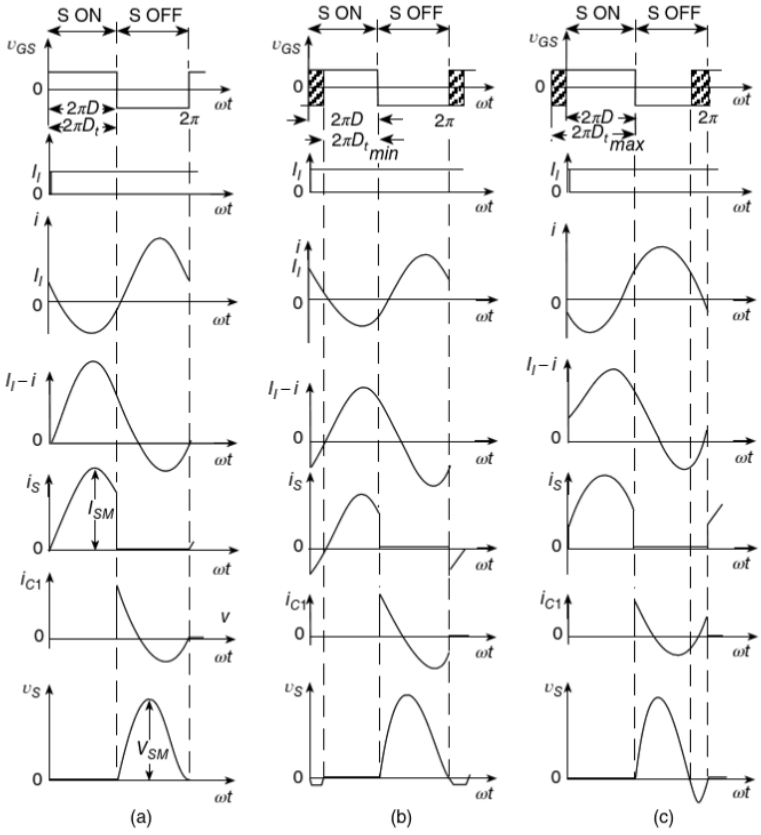


Figure 2.30: Waveforms for a Zero Voltage Crossing Amplifier. A) Optimum Operation. B) Below 50% Duty Cycle. C) Above 50% Duty Cycle. (Kazimierczuk, 2015)

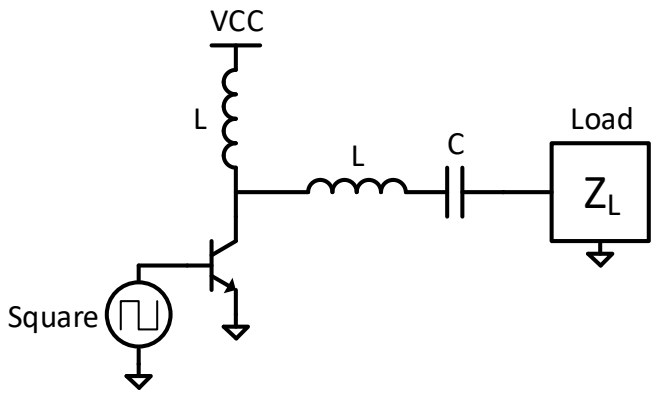


Figure 2.31: Class E Zero Current Crossing Amplifier

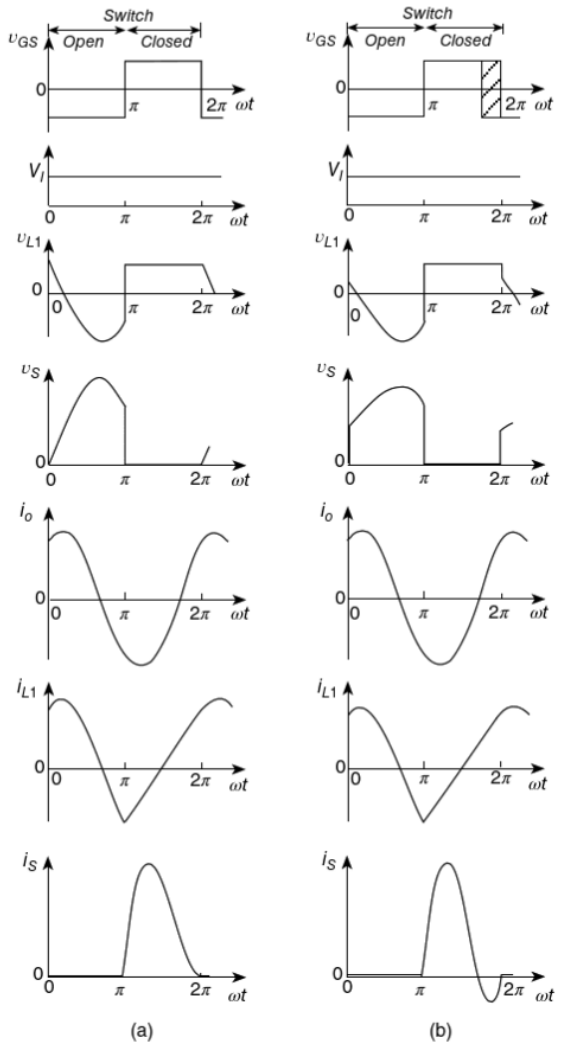


Figure 2.32: Zero Current Crossing Class E Amplifier Waveforms: A) Optimum Operation. B) Suboptimum Operation (Kazimierczuk, 2015)

2.4.2.7 Class F Amplifier

Class F amplifiers use output harmonic resonators to create a square wave and then filter it back to a sine wave. There are two kinds of Class F amplifiers; these are standard and inverse. The standard Class F amplifier uses a partially saturated transistor and odd harmonic resonators to present a high impedance to the output's voltage waveform. The resonators reflect the transistor's voltage wave at the specified harmonics, causing it to combine into a square wave with the fundamental frequency. The current sees a short through all odd harmonics and high impedances at even harmonics combining into a half-sine current waveform. Using more harmonics allows for a better approximation of a square wave at the transistor's drain. This configuration, in turn, yields higher efficiency (Kazimierczuk, 2015).

Each harmonic resonator is placed in series starting with the highest harmonic closest to the drain (Raab, et al., 2002). The inverse Class F amplifier uses even harmonics to create the voltage waveform, which resembles a half-sine and odd harmonics to generate a square wave. The more harmonics used, the better the efficiency (Grebennikov, Sokal, & Franco, Switchmode RF Power Amplifiers, 2007).

This type of amplifier can be complex to design, and it only operable at specific frequencies. *Figure 2.33* shows the circuit for a Class F amplifier and the inverse Class F amplifier in *Figure 2.34*. The waveforms for a Class F amplifier are *Figure 2.35*, and the Inverse Class F amplifier waveforms *Figure 2.36*.

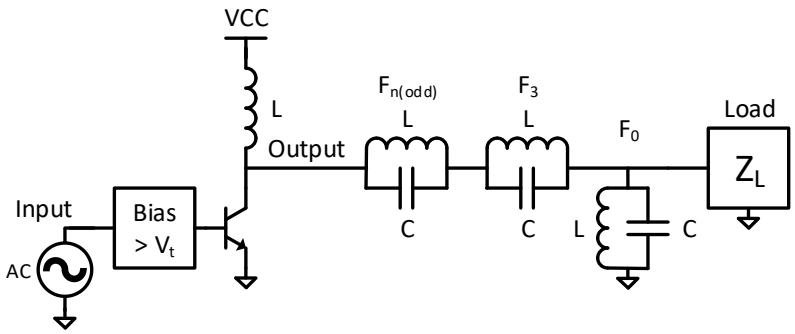


Figure 2.33: Class F Amplifier

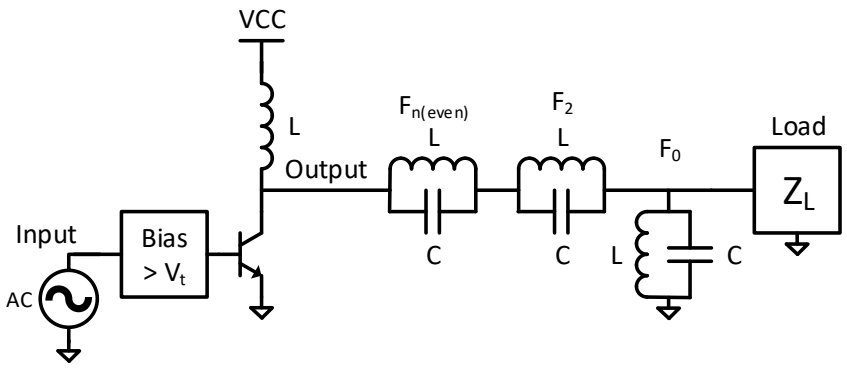


Figure 2.34: Inverse Class F Amplifier

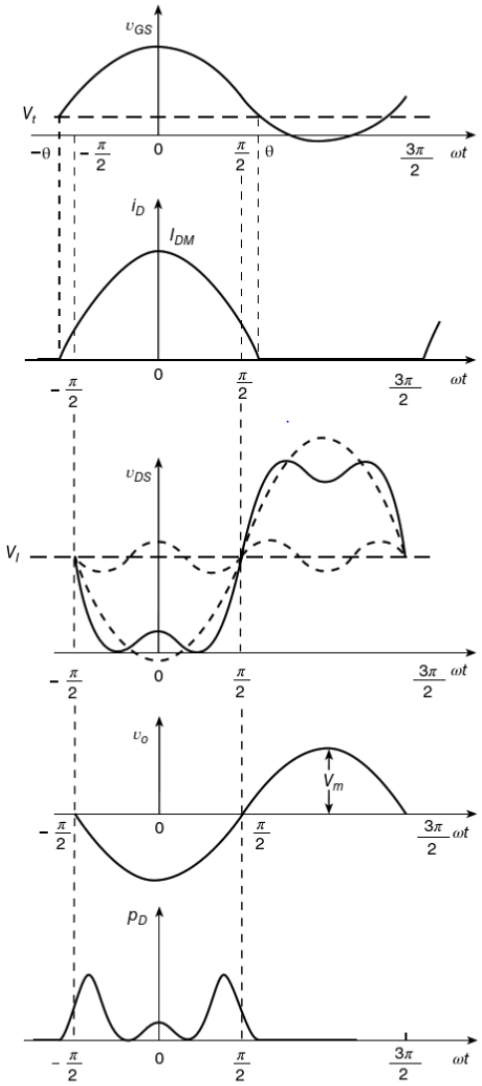


Figure 2.35: Class F Amplifier Typical Waveforms (Kazimierczuk, 2015)

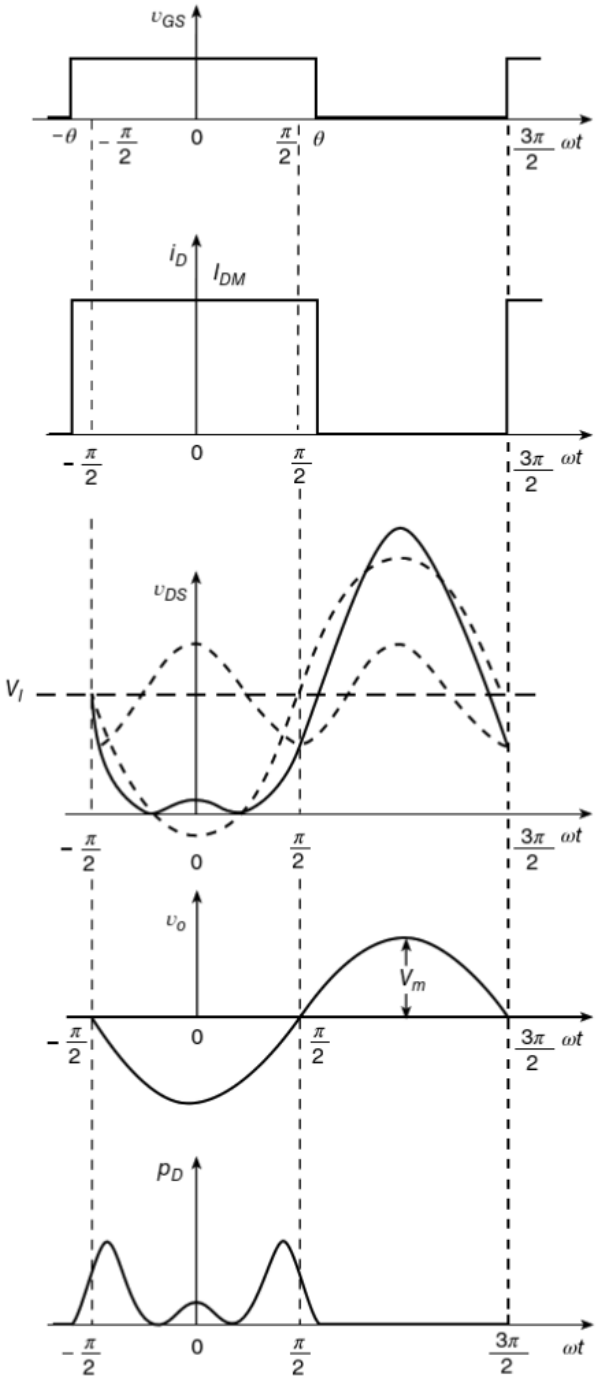


Figure 2.36: Inverse Class F Amplifier Typical Waveforms (Kazimierczuk, 2015)

2.4.3 Power Amplifier Summary

Typical power amplifier designs use either class A, AB, or B for low distortion, frequency range, and high linearity, even with lower efficiencies (Pozar, 2011). *Table 2.3* shows a comparison of all discussed power amplifier classes.

Table 2.3: Power Amplifier Summary

Amplifier Class	Pros	Cons
A	• High Linearity • Wide Frequency Operation	• Low Efficiency
B	• Wide Frequency Operation	• Medium Linearity • Medium Efficiency
AB	• High Linearity • Wide Frequency Operation	• Medium Efficiency
C	• High Efficiency • Wide Frequency Operation	• Low Linearity
D	• High Efficiency	• For sub 1GHz designs only • Not linear
E	• High Efficiency	• Low range of frequency operation due to harmonic resonators • Sensitive to changes in output load • Not linear
F	• High Efficiency	• Not linear • Low range of frequencies due to harmonic resonators

2.5 Tunable Elements

Components that can vary their value based on a controlled input are an enabling technology for tunable matching networks. The capacitors and inductors of static matching networks are replaced with these tunable components and allow the matching network's properties to be adjusted. This section covers the different types of tunable capacitors and inductors available.

2.5.1 Tunable Capacitors

This section outlines the different types of tunable capacitors and can be considered a direct drop-in replacement for matching network capacitors.

2.5.1.1 Micro Electro-Mechanical System (MEMS) Capacitor

MEMS capacitors are a mechanical-based type of variable capacitor. It consists of two conductive layers that are parallel to each other. One layer is stationary while the other layer is allowed to move. A DC bias voltage is applied to the device, changing how close the two plates are to one another. The distance changes the device's capacitance (Li, Zhang, Miao, Li, & Zhao, 2006). *Figure 2.37* shows the crossectional view of a MEMS capacitor in its two states.

MEMs capacitors operate on the order of 40GHz+ (Peroulis & Katehi, 2003) and power ranging from a few hundred microwatts (100µw) to a few Watts (Cruau, Tassetti, Nicole, & Lissorgues, 2003). MEMS capacitors also offer "good loss characteristics, very low power consumption, and wide bandwidths, and (unlike diode or transistor switches) exhibit virtually no intermodulation distortion" (Pozar, 2011). Due to the nature of MEMs, the theoretical tuning resolution is infinite; however, typically, only two states are achieved out of a MEMS capacitor, creating more of a switched capacitor. Devices that incorporate MEMS capacitors have several in an array to switch between to create a more fine resolution that is 2^n where "n" is the number of MEMS components. Another theoretical advantage of MEMS is that the device can have upwards of 100:1 tuning range; however, in a practical application, the tuning range is closer to 2-5:1 (Qin & Barker, 2006). The device's mechanical nature slows down the tuning time to 30+µs and limits the part's life (Pozar, 2011).

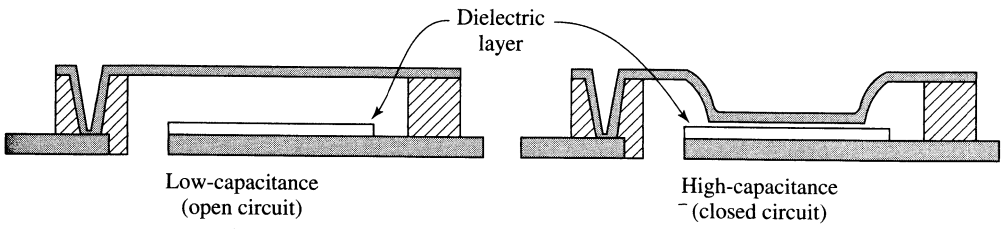


Figure 2.37: MEMS Capacitor (Pozar, 2011)

2.5.1.2 Varactor Diodes

Varactors have been around for decades and found uses in various applications, oscillators, antenna tuners, and tunable filters (Buisman, et al., 2007). *Figure 2.38* shows the diode model of a varactor with a typical back-to-back configuration. A varactor diode consists of a reversed biased diode, doped to provide a specific capacitance versus voltage (CV) curve, and placed in series, common cathode, with another varactor (Pozar, 2011). Varactors rely on applying a DC voltage to the bias line of the varactor. As the voltage changes, so does the capacitance of the device. This effect gives the device a theoretically infinite tuning resolution though the voltage source resolution limits it.

The device's solid-state nature allows quick tuning times on the order of 1-100 nanoseconds (Huang, et al., 2010). The low voltage required for operation and no junction noise make varactors ideal for low-power systems (Bahl, 2003). Varactors have a much higher capacitance density than MEMS components though it comes at the cost of nonlinearities in the CV tuning curve (Huang, et al., 2010). The other disadvantage of the varactor is that as the system power increases tuning range decreases. The degradation in power handling occurs as the RF signal's voltage interferes with the varactor's bias as RF energy passes through the device. Essentially the varactor needs to be biased with a large enough voltage that the effect of the added RF voltage is negligible.

One way to overcome power handling issues is to place varactors in an NxN array. The series varactors' capacitance will lower the RF voltage's overall effect, while the parallel varactors will increase the tuning range (Nemati, Fager, Gustavsson, Jos, & Zirath, 2009). *Figure 2.39* shows an implementation of this NxN varactor array for use with a high power amplifier, and *Figure 2.40* shows another topology for improved power handling.

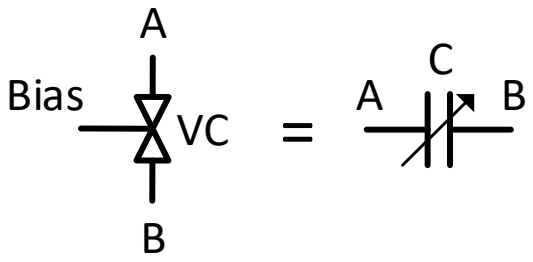


Figure 2.38: Varactor Model

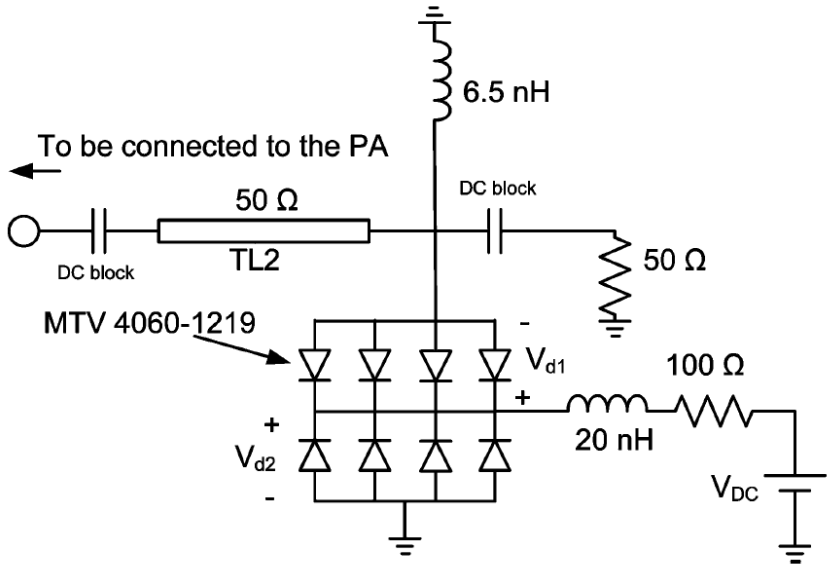


Figure 2.39: Varactor Array (Nemati, Fager, Gustavsson, Jos, & Zirath, 2009)

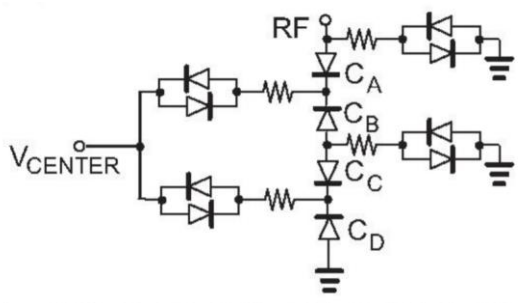


Figure 2.40: Improved Power Handling Varactor Design (Buisman, et al., 2007)

*2.5.1.3 **Digitally Tunable Capacitor (DTC)***

Digitally tunable capacitors are components that vary capacitance based on a set of digital signals sent to the device. Typically DTC's implement a set of MEMS capacitors or static capacitors that get switched between to create a total change in capacitance (United States Patent No. US 7825,715 B1, 2010). Due to the nature of the device, DTC's offer wide ranges of capacitances, power handing, scalability and have the added advantage of scalable tuning ratios (Patel & Redeiz, 2012). These devices offer a tuning resolution of 2^n where "n" is the number of internal capacitive states. The tuning ratio for these is anywhere from 1.4-8+:1. The internal components of the device cause this range. Peregrine Semiconductor offers devices that have tuning ratios of 4.6-7.7:1 (Peregrine Semiconductor Corp., 2018). Power and frequency ranges for these are on the same order as MEMS or static capacitors, as this is the underlying technology. *Figure 2.41* and *Figure 2.42* show two different types of digitally tunable capacitor circuits.

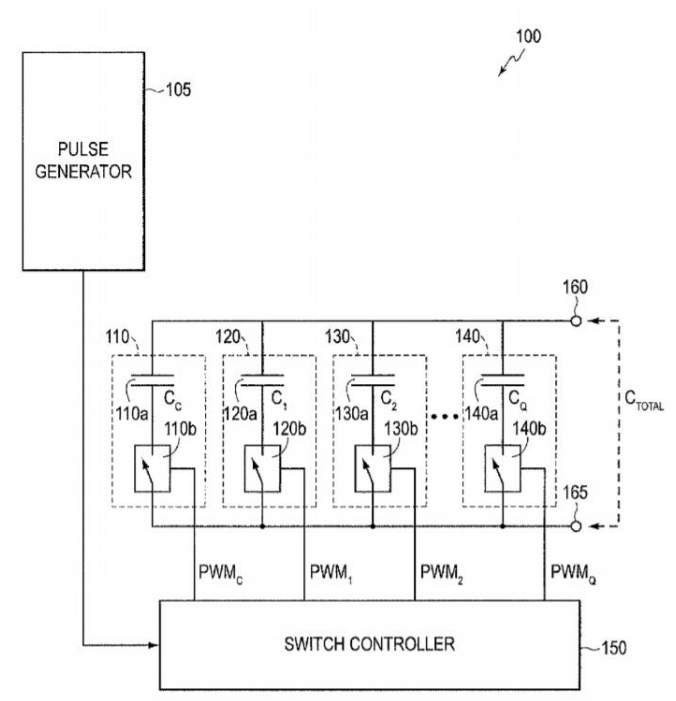


Figure 2.41: Patent Diagram for a Digitally Tunable Capacitor (United States Patent No. US 7825,715 B1, 2010)

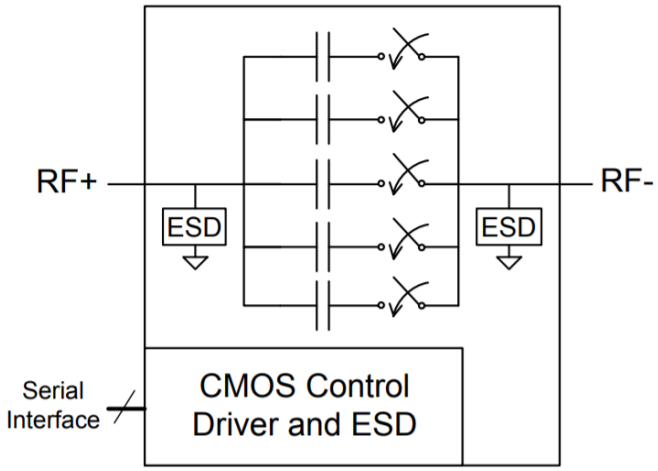


Figure 2.42: Block Diagram of Peregrine Semiconductor Corp. DTC
(Peregrine Semiconductor Corp., 2018)

2.5.2 Tunable Inductors

This section outlines the different types of tunable inductors. Due to the nature of an inductor, it is not physically possible to construct a variable inductor. Instead, capacitively tuned and switched inductors create a change in inductance (Arabi, Xingran, Morris, & Beach, 2017).

2.5.2.1 Capacitively Tuned Inductor

Capacitively tuned inductors place a capacitor in parallel (Arabi, Xingran, Morris, & Beach, 2017) or series with the inductor (Fu & Mortazawi, 2008). *Figure 2.43* shows the two topologies for variable inductors. Adjusting the capacitance of the capacitor changes the total reactance of the pair. Take care to ensure that the capacitor's reactance does not overpower the reactance of the inductor. If done correctly, the pair will appear to be a variable inductor. The equivalent inductance of the two components in parallel is in EQN(2.21) (Arabi, Xingran, Morris, & Beach, 2017). Calculate the series inductance using EQN(2.22), the derivation for which is in APPENDIX B. The power handling and tuning range of these devices are highly dependent on the value of the fixed inductor and the capacitor. Along with this, the frequency range is also highly dependent on the lumped properties of the device.

$$L_{equivalent} = \frac{L_{fixed}}{1 - \omega^2 C_{\ Variable} L_{fixed}} \qquad \text{EQN(2.21)}$$

$$L_{equivalent} = \frac{\omega^2 C_{\ Variable} L_{fixed} - 1}{\omega^2 C_{\ Variable}} \qquad \text{EQN(2.22)}$$

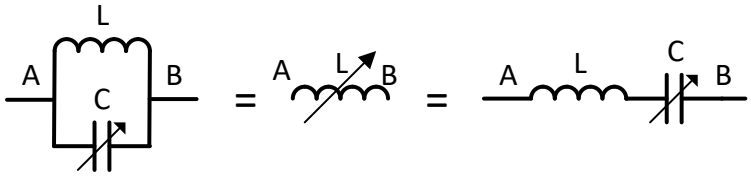


Figure 2.43: Capacitive Variable Inductor Options

2.5.3 Switched Bank Components

One way to get variable tuning of a system is to use a wide variety of static components, which switch in and out. RF FETs, MEMS switches, and PIN diodes are types of switches. *Figure 2.44* and *Figure 2.45* show what a switched bank component might look like for a capacitor and inductor. However, it is essential to note to avoid putting lossy components in series with the RF signal path. Doing so will cause increased loss through the matching network.

Reactive components can either be discrete elements or microstrip that designed for a specific reactance. Franco and Dening proposed a design for a 220MHz to 450MHz matching network using switched discrete components. *Figure 2.46* shows the schematic of this tunable matching network, while *Figure 2.47* shows the fabricated prototype. It was opted not to make the components out of microstrip because the transmission line lengths would be too big (Franco & Dening, 2011).

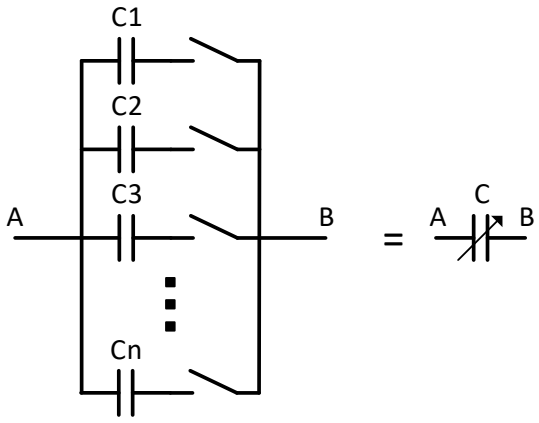


Figure 2.44: Switched Capacitor

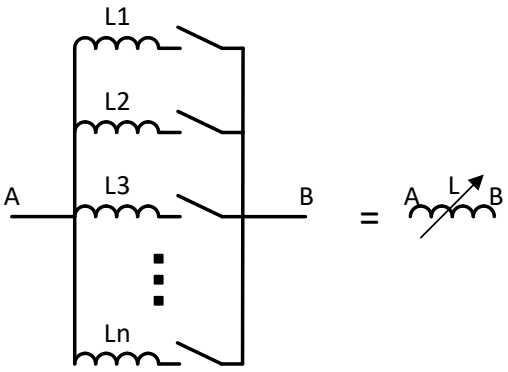


Figure 2.45: Switched Inductor

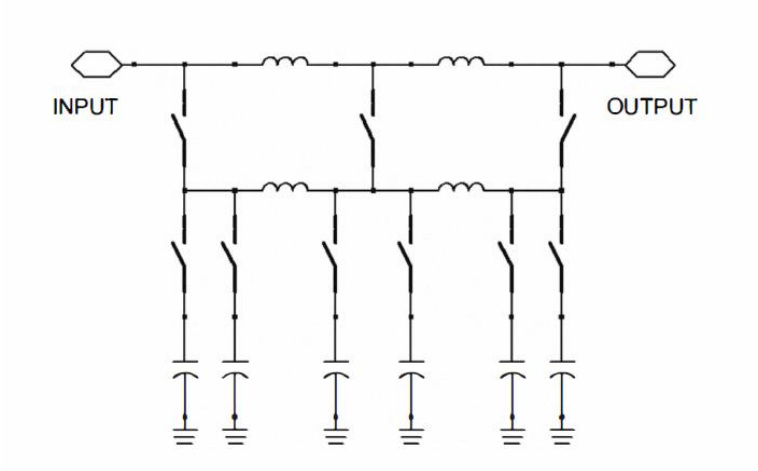


Figure 2.46: Schematic of Switched Component Tunable Matching Network (Franco & Dening, 2011)

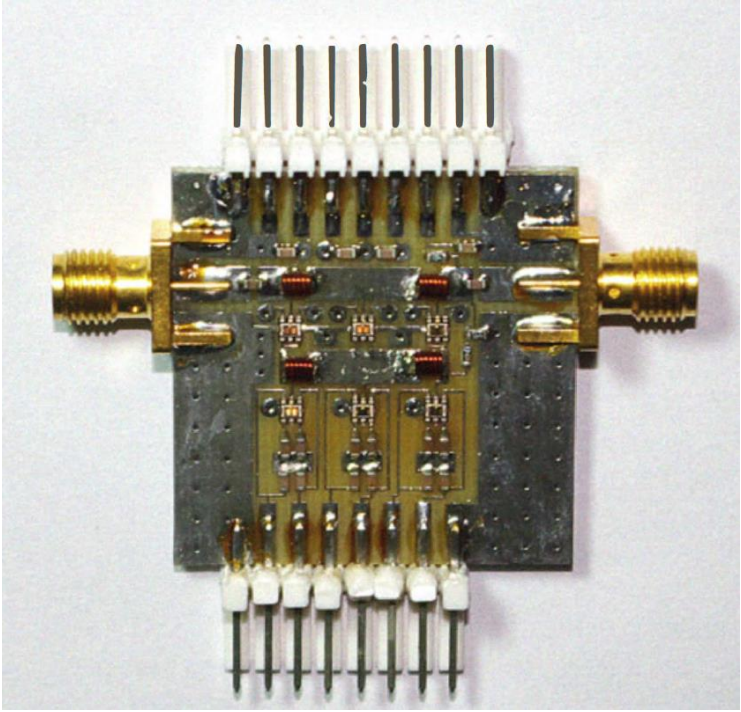


Figure 2.47: Realization of Switched Component Tunable Matching Network (Franco & Dening, 2011)

Another group has taken a similar approach but designed a cascaded cell-based tunable network. The cells consist of a static capacitor and inductor and are cascaded together. The group achieved a tuning range of 300MHz to 800MHz with better than 10dB of rejection and lower than 2dB of insertion loss (Sanchez-Perez, de Mingo, Carro, & Garcia-Ducar, 2013). *Figure 2.48* shows the group's design.

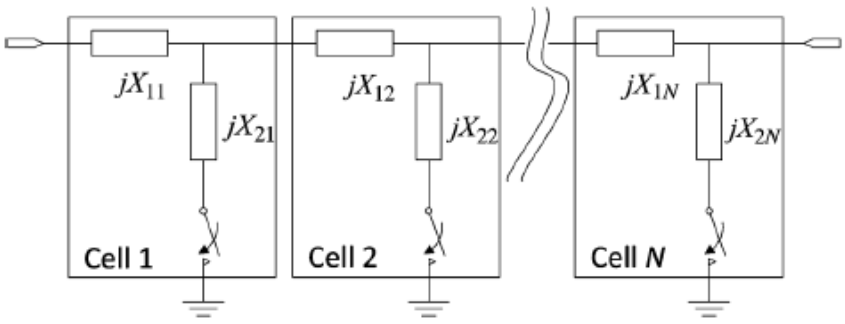


Figure 2.48: Cell Based Switch Bank (Sanchez-Perez, de Mingo, Carro, & Garcia-Ducar, 2013)

2.5.4 Summary of Tunable Components

Table 2.4 shows a quick summary of the aforementioned capacitive tuning components and parameters. Due to the wide variety of options for components and topologies, the table does not show capacitively tuned inductor and switch bank components.

Table 2.4: Tunable Capacitance Component Summary

Device Type	Frequency Range (GHz)	Tuning Ratio	Power Rating (W)	Control Voltage (V)	Resolution	Tuning Time (µs)
MEMS	2:40+	1.4-5:1	0.0001:1+	20:50	2^n	30+
Varactor	0.1:3	2-9:1	0.0001:1+	0:20	∞	0.001:0.1
Digitally Tunable Capacitors	0.1:10	4.6-7.7:1	0.0001:1+	5V	2^n	10+
Capacitively Tuned Inductor	Dependent on Capacitor	Dependent on Capacitor	Dependent on Components	Dependent on Capacitor	2^n or ∞	0.001:30+

2.6 Feedback Topologies and Control Methods

After discussing the importance of matching networks, classifications of amplifiers, and a summary of tunable components, this is enough for most current applications. The reason is that the designer would develop a tunable matching network design and then use a vector network analyzer (VNA) or some other measurement tool to perform an open-ended calibration of the system. The calibration process would create an extensive lookup table of matching network settings that correspond to specific frequencies, amplitudes, and other signal characteristics. The network controller would then receive a command to configure the matching network based on those predetermined characteristics and look up the required network settings from the table. This process would reset the matching network to a calibrated state. Though simple to develop, this requires extra memory and only produces a finite resolution of matchable networks.

Calibration does not account for variation in the components overtime or outside interference affecting the system impedance (Gu & Morris, 2013). Implementation of feedback that can sense the RF energy going through the device and, based on the information, compensate for any misalignments is a crucial next step. Adjusting a system based on feedback for its output is referred to as closed-loop control. This section outlines the different types of feedback, topologies, and control methods.

2.6.1 Measurement of Reflection Coefficients Using A Directional Coupler

One of the standard methods for sensing a tunable matching network's effectiveness is to use a directional coupler to retrieve the reflection coefficients (Γ) on the power amplifier's output. There are several different calculations for Γ. One is to state that Γ is the voltage ratio of the reflected wave (V_0^-) over the incident wave (V_0^+), where the incident wave is a forward traveling wave from the source to the load, and the reflected wave is from the load back to the source. Another way to state the reflection coefficient is by the ratio of the difference in the source (Z_0) and load (Z_L) impedances. EQN(2.23) shows the ratios. As can be seen, when the source matches the load impedance, then there is no reflected wave, and Γ is 0 (Wentworth, 2006).

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad \text{EQN(2.23)}$$

A coupler takes a small amount of the RF energy off the transmission line to be measured. The directional coupler allows energy from the forward-going wave to couple off. Energy from a reflected wave couples onto a different port. *Figure 2.49* shows a basic diagram of a directional coupler. *Figure 2.50* shows a bidirectional coupler, which transforms into a directional coupler by terminating one of the coupling ports "3" or "4", depending on the desired direction. The wave traveling from port "1" couples to port "3", and the reflection from port "2" couples to port "4". A more robust form of coupling is a dual directional coupler. This coupler implements two terminated bidirectional couplers improving isolation between the incident and reflected coupled waves. The coupling pattern of port "1" to "3" and "2" to "4" is the same. *Figure 2.51* shows a dual directional coupler schematic, while *Figure 2.52* shows one implementation of a dual directional coupler in microstrip.

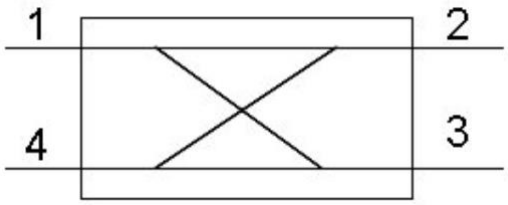


Figure 2.49: Generic Directional Coupler Schematic Symbol (Directional Couplers, 2013)

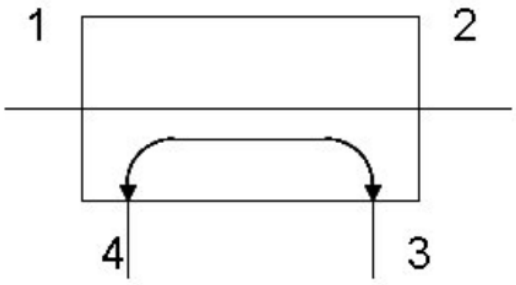


Figure 2.50: Bidirectional Coupler (Directional Couplers, 2013)

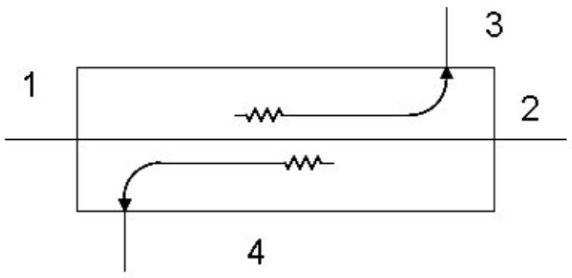


Figure 2.51: Dual Directional Coupler (Directional Couplers, 2013)

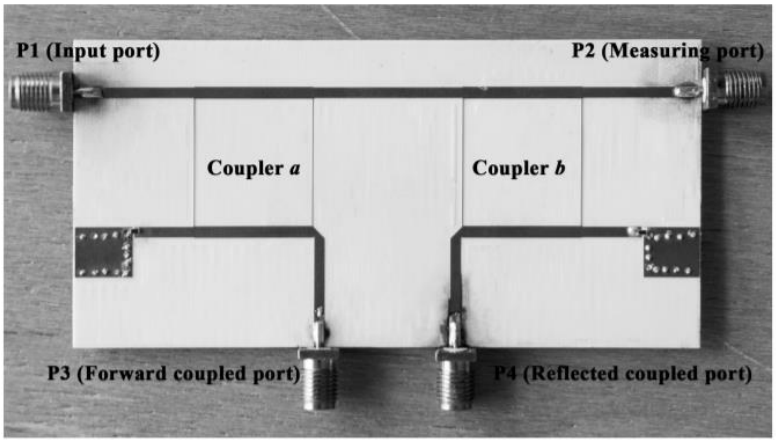


Figure 2.52: Directional Coupler Implemented (Le & Zimmer, 2015)

Once the RF energy transfers to the coupler, it is then fed into a power detector. Power detectors can either extract the magnitude or magnitude and phase based on the design. A scalar power detector combines the magnitude and phase into a single term. In this case, it finds the voltage standing wave ratio (VSWR). The VSWR of a system is related to the absolute value of the reflection coefficient, as stated in EQN(2.24). If the system impedance is normal to the source impedance, then another way of stating this is that VSWR is equal to the absolute magnitude of the load impedance EQN(2.25). EQN(2.26) shows how to convert a complex impedance into a magnitude. Note that the reactive element is squared, causing the sign to determine if a capacitance or inductance is lost. However, the information is still useful to determine the quality of the system match.

$$|\Gamma| = \frac{VSWR - 1}{VSWR + 1} \qquad \text{EQN(2.24)}$$

$$|\Gamma| = \frac{VSWR - 1}{VSWR + 1} = \frac{|Z_L| - 1}{|Z_L| + 1} \qquad \text{EQN(2.25)}$$

$$|Z_L| = \sqrt{R^2 + x^2} \qquad \text{EQN(2.26)}$$

A vector power detector gives phase along with magnitude. The phase provides information on the network's reactance and determines the sign of the reactive impedance lost in EQN(2.26).

In either condition, the output of the detectors is usually a DC voltage. Analog to digital converters (ADC) converts the voltage into a binary number, which allows for computers, microcontrollers, digital signal processing modules (DSP), field-programmable gate arrays (FPGAs) to compute how best to control the properties of the matching network. *Figure 2.53* is a basic block diagram from one research group.

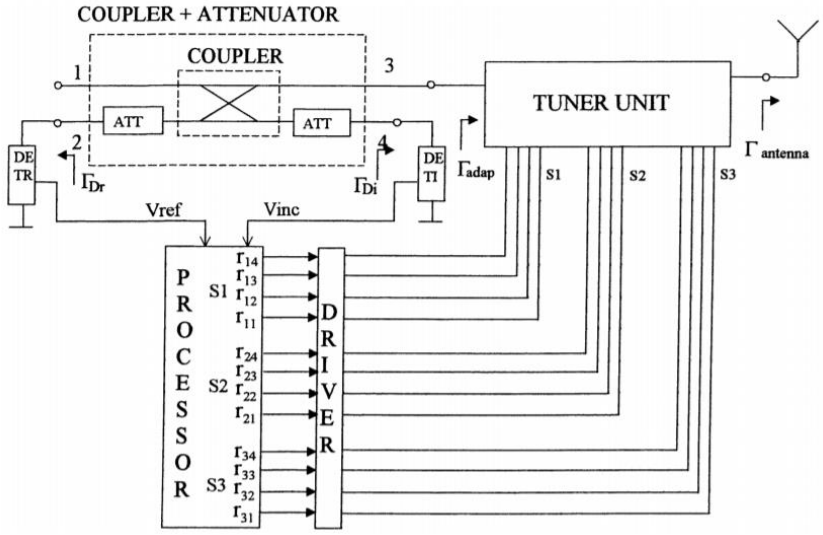


Figure 2.53: Basic Diagram of Coupler Driver Feedback for Processor Control of a Tunable Matching Network. (de Mingo, et al., 2004)

2.6.2 Iterative Search Methods Based on the Measurement of Reflection Coefficient

There are several methods for tuning the matching network. One group used open-loop control to set the matching network to roughly the right state and then used an iterative process to minimize the reflection coefficient to zero (Oh, Song, Aberle, Bakkaloglu, & Chakrabart, 2007). Another group would set the matching network to an arbitrary value and then, using different interactive methods (Hooke and Jeeves's Algorithm, Powell Algorithm, Simplex Method, Single-Step Algorithm), adjusted the tunable elements searching for an optimal match. The researchers, who used the system in *Figure 2.53*, found that the single-step algorithm provided the best results. The system used digitally tunable MEMs capacitors—the three capacitors set to a starting state. The nearest 6 points would then be searched sequentially, each having its reflected wave voltage measured. The state that produced the lowest reflected voltage was then selected and used as the new starting point. This search method would repeat until the starting point was the lowest reflected voltage or reaching the iteration limit. The research group mentioned that this could lead to false minimums and thus not the absolute best match, but still produced a better match (de Mingo, et al., 2004). Another issue is that minimizing Γ does not necessarily mean that the maximum power transfer to the load (Gu & Morris, 2013).

2.6.3 Direct Impedance Measurement

Several groups have been looking at directly calculating the load impedance based on the voltage measurement from the matching network's input and output. Instead of using a coupler as many others have done, one group used log amplifiers to measure the matching network's input and output voltage. This technique provided both phase and magnitude. Based on these values and having a known matching network impedance and known source impedance, direct calculation of the load impedance was possible. The design incorporated digitally tunable MEMs capacitors, which have very well-defined capacitance and fixed inductors. From here, the control algorithm calculated the required matching and set the impedance of the network to such. One benefit of the design was the tuning time's speed, which reported a speed increase by 1000 (Gu & Morris, 2013). *Figure 2.54* shows the block diagram of the system used.

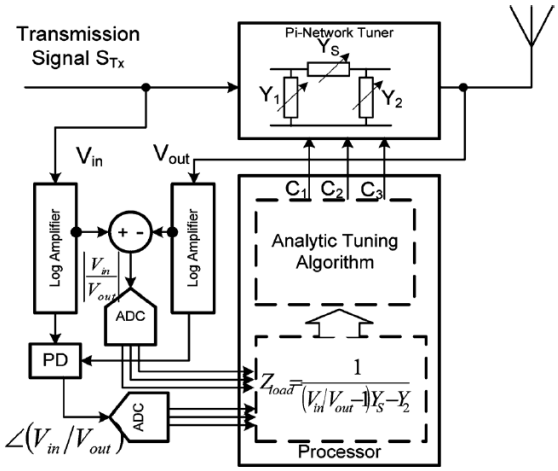


Figure 2.54: Block Diagram of an Analytical Based Adaptive Matching Network Control (Gu & Morris, 2013)

Another group used a series sensing capacitor at the matching network's input to deembed the antenna impedance. Attenuators on either side of the capacitor extract small amounts of RF energy from the waveform. The attenuated waveforms are mixed down to a lower frequency and then directly processed instead of being converted to a DC voltage. The process then uses the magnitude, phase, and sensing capacitors' impedance to calculate the system's required match by solving a standard Pi Network. This offered fast tuning times and low power consumption (Po, de Foucauld, Morche, Vincent, & Kerherve, 2011)

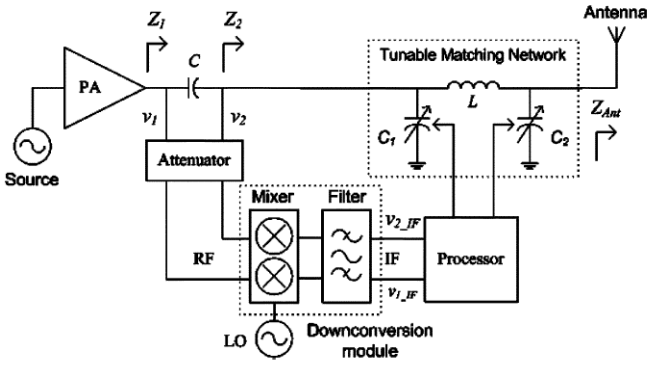


Figure 2.55: Block Diagram of a Series Capacitance Based Deembedding Approach (Po, de Foucauld, Morche, Vincent, & Kerherve, 2011)

2.7 Summary

Chapter two summarized literature that covered the fundamentals of impedance matching, the pertinent information surrounding the classifications of amplifiers, a review of tunable components, and presented several methods for controlling a tunable matching network. Having a well-matched linear amplifier with wideband operation is desirable for a large number of different applications. The concepts presented should be used to achieve a design that meets this need.

CHAPTER 3. RESEARCH METHODOLOGY

3.1 Overview

As the demand for wider bandwidths with reduced power consumption increases, having technology that can enable reconfigurability in radio frequency (RF) applications is necessary (Rodriguez, 2008). One of the most critical and highest power users of an RF system is the power amplifier. The power amplifier is typically the last stage of the transmit chain before the antenna. Linear and wideband operation of these devices reduces the potential max efficiency to 50%-78%, depending on the amplifier's classification. The linear aspect and high-frequency range mean that the amplifier's design is unlike other amplifiers with high-efficiency (Raab, et al., 2002).

This thesis addresses the issue that as the frequency and amplitude of an RF signal passing through a power amplifier changes, the amplifier changes impedance. The impedance mismatch with the source and load lowers the system's power transfer (Zannas & Vafiadis, 2016). This research aims to develop and test wideband tunable matching networks for matching the input and output impedance of a power amplifier.

The following chapter discusses the methods of designing the system and prototype amplifier. The chapter includes the specifications for success, modeling techniques used, the system block diagram, and the amplifier design.

3.2 Specifications

The proposed design needs to be able to tune from 500MHz to 2.5GHz. This frequency range allows for the tuning of several cellular bands and two scientific bands. Most mobile devices have a max output power of 1W or 30dBm. For practical implementation, the matching networks should accommodate this power range (Rodriguez, 2008). Rosolowski has proven that a power amplifier with a tunable matching network with a power of 27dBm (0.5W) is achievable. The study's frequency range was 1.3GHz-2.6GHz, which falls within this study’s operating range (Rosolowski, Wojtasiak, & Gryglewski, 2010). Several sources indicate that tuning times, depending on the sensing method and configuration topology, range from hundreds

of milliseconds (ms) to microseconds (µs) (Gu & Morris, 2013) (Po, de Foucauld, Morche, Vincent, & Kerherve, 2011) (de Mingo, et al., 2004). Based on this, the appropriate match should be determined in under 100ms. One of this study's main goals is to prove that a wideband tunable matching network will yield high power efficiency than static matching. The power added efficiency (PAE) of the amplifiers with tunable networks should be greater than that of the simulated design with several statically matched networks. The following list outlines the desired specifications for the design.

- Frequency Range: 500MHz to 2.5GHz
- System Power Output: 27-30dBm
- Tuning Time: <100 milliseconds (ms)
- PAE: must be higher than simulated static matching networks for the same amplifier
- The amplifier is to be linear

3.3 System Modeling

During the design process system, modeling took place in AWR's Microwave Office. The switches use scattering parameters (S-parameters) as the model. The transistor used a nonlinear model from Cree so that biasing of the transistor could be factored in during the design. The inductor models are standard Q-dependent models from AWR. The varactors consist of ideal capacitors and resistors that mimic the capacitance and package parasitics of the varactors. Pads and transmission lines used transmission line models from AWR. The system layout of the boards took place in Altium PCB Designer. The connector to board transition required Ansys's High-Frequency Structure Simulator (HFSS) for modeling due to the lack of accurate models. After modeling the connection, a set of S-parameters exported from HFSS provided the system model with a valid connection point.

3.4 Block Diagram

The system uses a Network Analyzer (NA) to produce a single adjustable frequency on its port 1. This signal feeds into the tunable Input Matching Network (IMN). The signal then passes through a power amplifier and then the tunable Output Matching Network (OMN) before

being measured by port 2 of the NA. Power measurements taken at the input and output of the system determine the match quality. *Figure 3.1* contains the system block diagram.

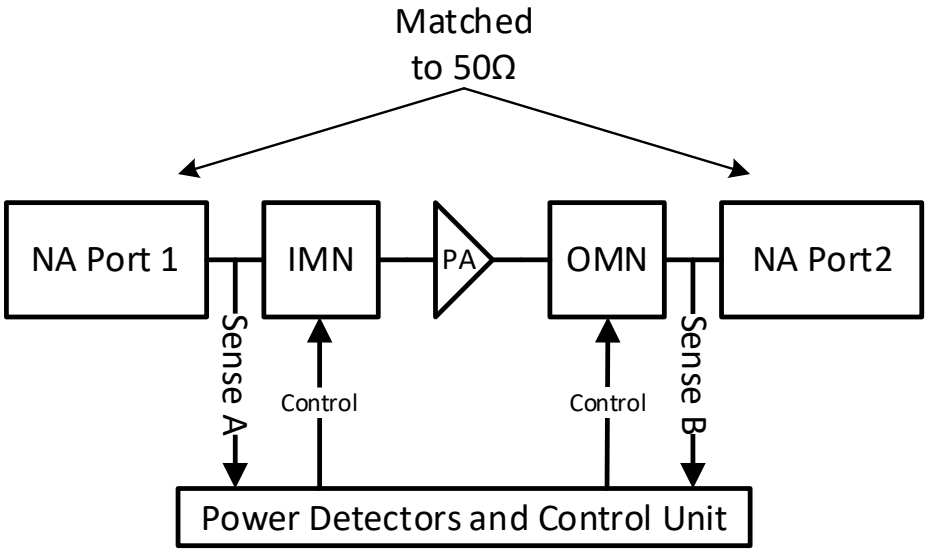


Figure 3.1: System Block Diagram

3.5 Power Amplifier

The following section outlines the design, operating procedures, and test results of the system's unmatched power amplifier. This section's results provide a minimum expectation for system performance and guide the matching circuit design outlined in section CHAPTER 4.

3.5.1 Power Amplifier Design

The design uses a discrete component Class A amplifier due to its linear nature and lack of available unmatched integrated circuit amplifiers. Unmatched integrated circuit amplifiers exist that achieve most of the requirements; however, issues arose when trying to match them dynamically. Instability in the amplifier impedance occurs due to low isolation from output to input. This instability caused issues with the needed topology of the matching network. Instead, an amplifier with higher isolation output to input is required.

The design followed a note for a 6W transistor-based amplifier from Cree (Cree Wolfspeed, 2020). Differing from the design note was the removal of the recommended

matching circuit. All remaining elements of the design are replaced with lumped element representations to achieve maximum bandwidth operations.

A test circuit verified the performance of the amplifier. Shown is the amplifier's schematic *Figure 3.2*, board layout *Figure 3.3*, final built prototype *Figure 3.4*, and bill of materials (BOM) *Table 3.1*. During initial testing, the 10uF decoupling electrolytic capacitors had to be added to the supply lines to stabilize the amplifier. The capacitors mount between the supply line pins and the ground plane on the board's bottom side. The schematic is up to date to reflect this change, but the board layout in *Figure 3.3* does not include them. The circuit board the amplifier is built on is manufactured by Oshpark using two-layer standard processing. The board is 63mils thick, consisting of one-ounce copper layers, and uses Kingboards KB6167F FR4 as the dielectric material. It is important to note that the amplifier shown is unmatched.

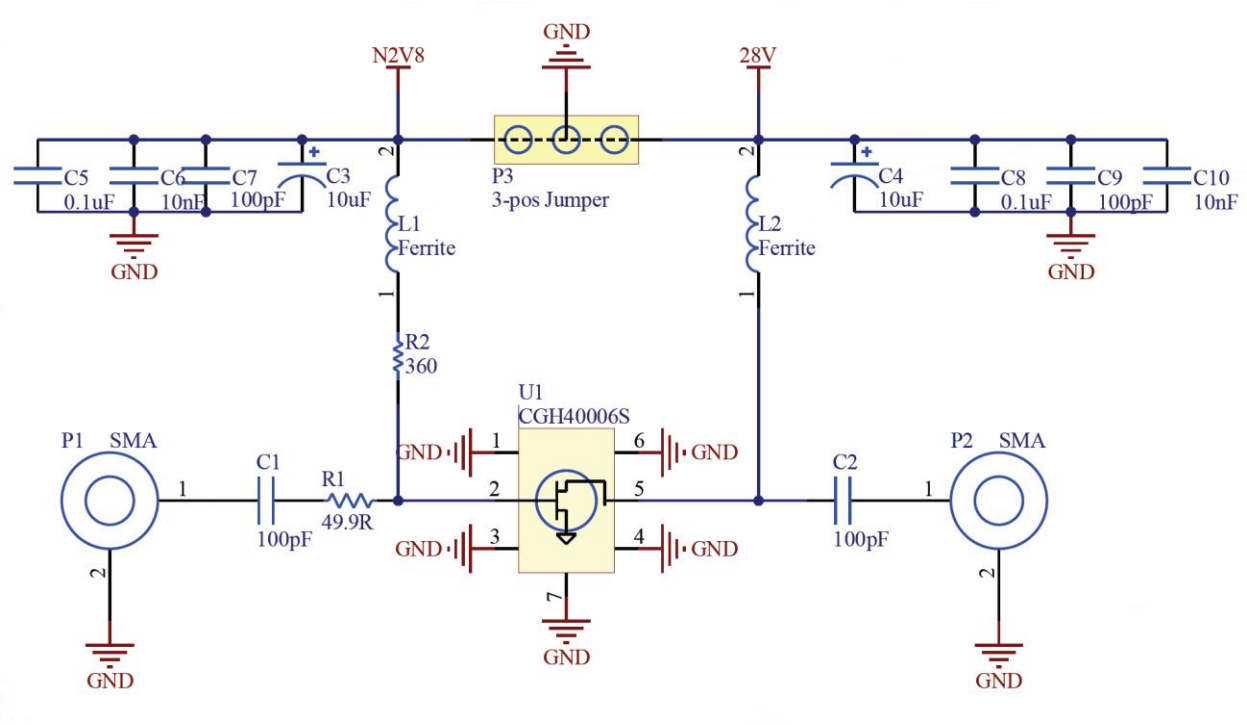
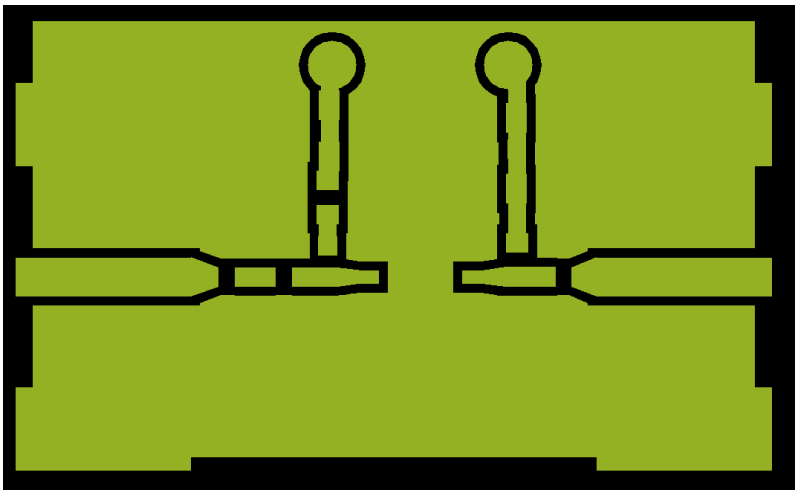
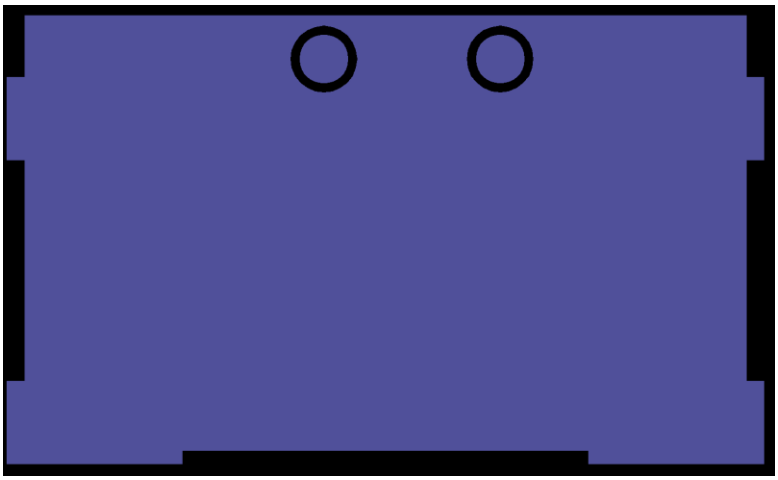


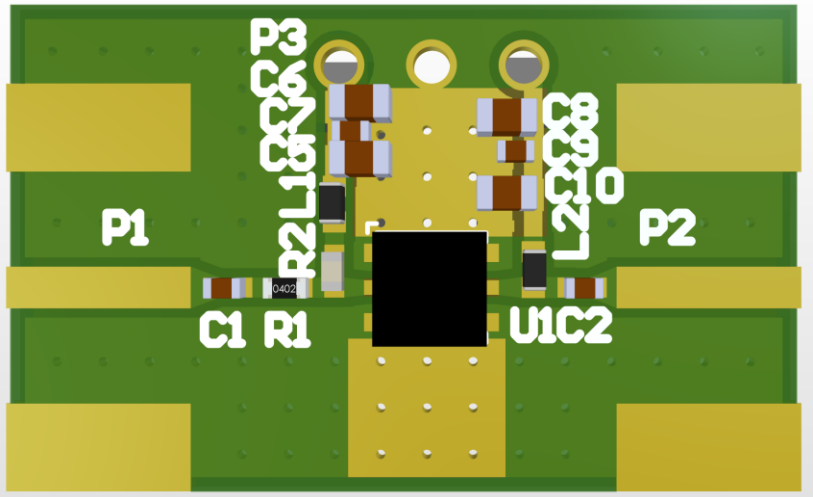
Figure 3.2: Amplifier Schematic



Power Amplifier Test Board Top Layer Gerber

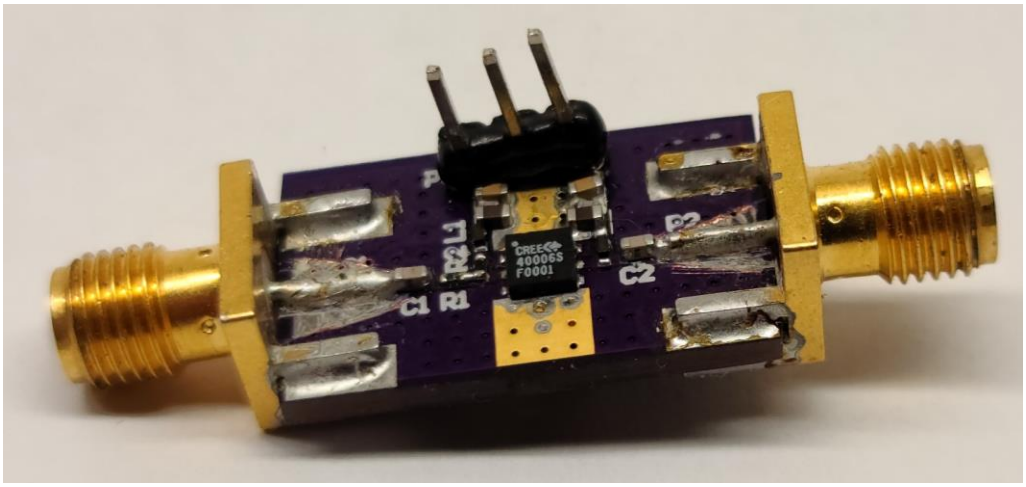


Power Amplifier Test Board Bottom Layer Gerber



Power Amplifier Test Board 3D View

Figure 3.3: Power Amplifier Test Board Top, Bottom, and 3D Layout



Power Amplifier Test Board Top

Power Amplifier Test Board Bottom

Figure 3.4: Built Power Amplifier Test Board

Table 3.1: Amplifier Test Circuit BOM

ID	Designator	Comment	Manufacturer	Part Number	Qty
1	C1, C2, C7, C9	100pF	KEMET	C0402C101J3GACTU	2
2	R1	49.9Ω	Yageo	RC0402FR-0749R9L	1
3	R2	360Ω	Vishay Dale	CRCW0402360RFKED	1
4	L1, L2	Ferrite	Coilcraft	0402DF-301XJRW	2
5	U1	HEMT	Cree	CGH40006S	1
6	P1, P2	SMA	CINCH CONNECTIVITY SOLUTIONS JOHNSON	142-0701-801	2
7	C3, C4	10uF	Vishay	293D106X9050E2TE3	2
8	C5, C8	0.1uF	Yageo	CC0603ZRY5V9BB104	2
9	C6, C10	10nF	Samsung	CL10B103KB8NCNC	2
10	P3	Wires	NA	NA	3

For the system prototype, the board uses Oshpark's four-layer process to route power and data under the RF section to other subsystems. The ground plane under the Amplifier moved up from the bottom layer (layer four) to layer two to accommodate this design requirement. This layer change moves the ground plane distance to the RF circuits from 60mils to 6.7mils. The board is 63 mils thick with a 47 mil core of FR408 and 6.7 mil prepreg spacing between the top and layer two and between the bottom and layer three.

3.5.2 Amplifier Biasing and Operating Procedures

Before moving into the following sections, it is essential to note the amplifier's biasing and operating procedures. The amplifier design uses a Gallium nitride (GaN) HEMT to amplify the input signal. The transistor is very sensitive to improper biasing and can be easily damaged. As previously discussed, the transistor bias must place it in the linear region for 100% of the waveform cycle to be a Class A amplifier. The transistor biasing requires two voltages to be biased correctly. The first is a negative voltage low current (<10mA) bias line on the gate of the amplifying transistor. The bias line controls how much DC current the transistor's drain to the source draws. The other is a positive voltage driveline with a high current (>100mA). For all tests and simulations, the transistor is biased such that the source of the transistor draws 100mA from a 28V DC digital power supply. This bias ensures standardization between different simulations, test measurements, and datasheet parameters. Below, lists the steps to turn on the amplifier. To shut down the amplifier, follow the procedures in reverse. It is crucial to follow these steps strictly. Failure to do so can result in the transistor failing.

1. Set a power supply channel to -5V DC, current limited to 10mA, for the bias line
2. Set a second power supply channel to 28V DC, current limited to 150mA, for the driveline
3. Ensure all power supply outputs are off
4. Wire the gate of the transistor to the bias line.
5. Wire the drain of the transistor to the 28V channel on the power
6. Turn on the power supply channel connected to the bias line.
    a. The bias line should draw less than 5mA of current.

7. Turn on the power supply channel connected to the driveline.
    a. The driveline should draw approximately 0mA of current.
8. Slowly raise the bias voltage until the transistor draws100mA of current from the drive channel
    a. The bias line voltage should approximately be -2.7V DC

3.5.3 Power Amplifier Testing

Two tests verified the operation of the amplifier. The first test was a constant frequency, power sweep on the spectrum analyzer. The second test was a constant power, frequency sweep on the Network Analyzer. Due to the small size of the board, the amplifier would overheat after a minute. Measurements were taken shortly after power-up to ensure that the amplifier was in a normal operating state. Note that thermal issues did not arise on any other tests due to those boards having substantial thermal dissipation in comparison.

3.5.3.1 Power Amplifier Spectrum Analyzer Test

This test measures the max output, linearity, and 1dB compression point of the amplifier. The amplifier input is wired to the RF generator while the output goes to a 20dB attenuator. The 20dB attenuator then passes the signal to the spectrum analyzer. After biasing the amplifier, the RF generator outputs a constant 500MHz wave to test the amplifier response. The power of the output sweeps from -30dBm to 10dBm in 2dBm intervals. At each interval, the spectrum analyzer measures the system power. *Figure 3.5* shows the test setup.

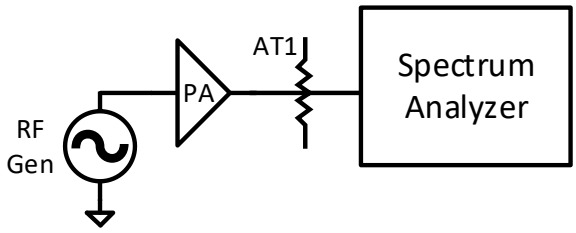


Figure 3.5: Power Amplifier Spectrum Test Setup

Before testing, calibration of the cables removes any cable error. The calibration includes wiring each cable from the RF generator to the spectrum analyzer. The generator conducts a power sweep, and the cable loss is measured. EQN(3.1) calculates the loss in a cable. During testing, an adjustment to the RF generator's power by the amount of power lost in the input cable (the cable that goes between the RF generator output and the power amplifier input) ensures proper calibration. EQN(3.2) shows how to calculate the RF generator output power to receive desired power at the amplifier. The output cable calibration uses the same procedures as the input cable. The output cable consists of the attenuators and cable that wire from the amplifier output to the spectrum analyzer input. The actual amplifier power is the addition of the output cable loss and the amplifier's measured power. EQN(3.3) shows the calculation for amplifier power. With the corrected input power and power of the amplifier known, the amplifier's gain is then calculated. Gain is the subtraction of output from input power EQN(3.4). A linear amplifier has constant gain regardless of input power up to the 1dB compression point. After this point, the amplifier can no longer be considered linear.

$$Loss_{Cable} = Power_{Ideal} - \ Power_{Measured} \quad \text{EQN(3.1)}$$

$$RF\ Gen_{Out} = Power_{Ideal} + \ Loss_{Input\ Cable} \quad \text{EQN(3.2)}$$

$$Power_{Amplifier} = Power_{Measured} + \ Loss_{Output\ Cable} \quad \text{EQN(3.3)}$$

$$Gain = Power_{Amplifier} - \ Power_{Ideal} \quad \text{EQN(3.4)}$$

Table 3.2 on page 80 contains the collected data from the power sweep and gain of the amplifier. The amplifier's operation provides a constant gain of 21dB up 6dBm of input power. After 6dBm, the amplifier begins to enter compression with a 1dB compression point of 10dBm.

Table 3.2: Power Amplifier Power Measurements

Input Power (dBm)	Simulated Power (dBm)	Measured Power (dBm)	Simulated Gain (dB)	Measured Gain (dB)
-30	-8.662	-8.897	21.338	21.103
-28	-6.662	-7.437	21.338	20.563
-26	-4.662	-5.463	21.338	20.537
-24	-2.662	-3.476	21.338	20.524
-22	-0.662	-0.603	21.338	21.397
-20	1.338	0.739	21.338	20.739
-18	3.338	2.950	21.338	20.950
-16	5.337	5.051	21.337	21.051
-14	7.336	7.089	21.336	21.089
-12	9.335	8.829	21.335	20.829
-10	11.332	11.189	21.332	21.189
-8	13.328	13.185	21.328	21.185
-6	15.322	14.736	21.322	20.736
-4	17.310	17.266	21.310	21.266
-2	19.290	18.754	21.290	20.754
0	21.253	20.599	21.253	20.599
2	23.181	22.796	21.181	20.796
4	25.032	24.693	21.032	20.693
6	26.736	26.020	20.736	20.020
8	28.361	27.688	20.361	19.688
10	30.015	29.529	20.015	19.529

Figure 3.6 on page 81 shows a graphical representation of *Table 3.2*. The graph shows the linear operation of the amplifier as well as the constant gain. From the graph the simulated and measured results are in agreement. Both simulated and measured results indicate that the amplifier meets the power specification and outputs between 27dBm and 30dBm of power while maintaining linearity.

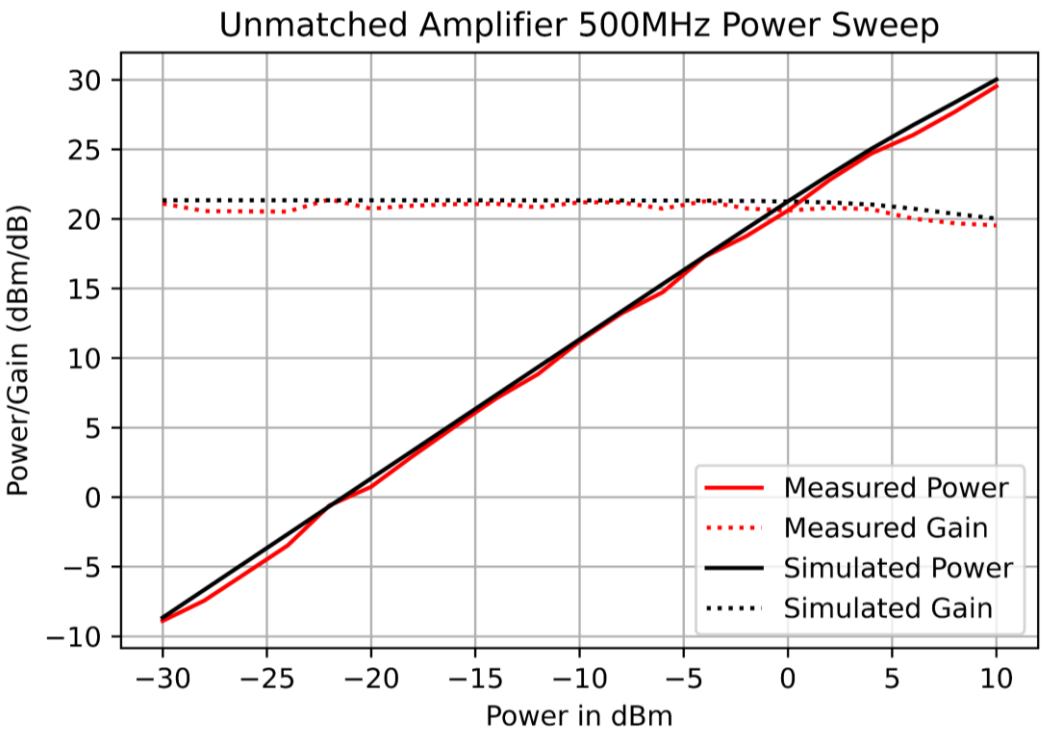


Figure 3.6: Unmatched Amplifier 500MHz Power Sweep

3.5.3.2 Power Amplifier Network Analyzer Test

The frequency test setup for the power amplifier test board uses port 1 of the VNA to measure the amplifier's input, and port 2 to measures the output. An attenuator on port 2 keeps from damaging the VNA. *Figure 3.7* shows the setup. The cable calibration also included the attenuator on the output test cable to minimize error. During testing, the VNA used a 0 and 10dBm signal to measure the S-parameters of the amplifier. The VNA measures the frequency response of the amplifier with constant power from 400MHz to 2600MHz.

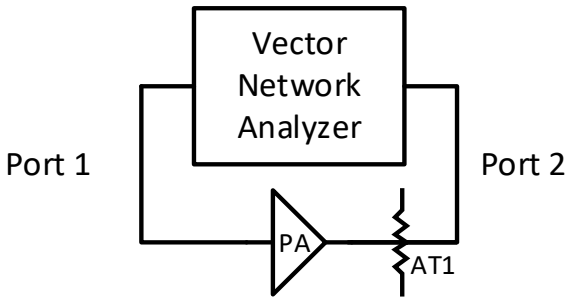


Figure 3.7: Test Setup for Power Amplifier Measurements

The amplifier's measured impedance is in *Table 3.3*. The table shows that the amplifier measured input and output impedances and gain across the frequency range. From the table, one sees that the amplifier is operable across the entire frequency range.

Table 3.3: Unmatched Power Amplifier Characteristics 10dBm Input

Frequency (MHz)	Input Impedance (Ω)	Output Impedance (Ω)	Gain (dB)
500	53.081-26.266j	46.374-10.542j	19.789
600	52.773-22.201j	44.407-9.783j	18.704
700	52.227-19.369j	42.257-9.343j	17.663
800	51.633-17.158j	40.277-8.452j	16.702
900	51.151-15.151j	38.160-6.882j	15.821
1000	50.687-13.374j	36.270-4.981j	14.985
1100	50.470-11.631j	34.523-2.429j	14.211
1200	50.557-10.065j	34.055+0.623j	13.47
1300	50.844-8.650j	33.424+3.858j	12.786
1400	50.633-7.334j	33.240+7.094j	12.221
1500	51.423-6.230j	32.864+10.787j	11.635
1600	52.402-5.455j	33.168+14.943j	11.088
1700	53.443-4.947j	34.022+19.575j	10.559
1800	54.682-4.702j	35.159+23.654j	10.06
1900	55.955-4.778j	36.930+28.303j	9.597
2000	57.293-5.239j	39.072+33.084j	9.137
2100	58.612-6.108j	42.734+37.869j	8.721
2200	59.854-7.405j	47.807+42.099j	8.308
2300	60.874-9.187j	54.771+45.996j	7.916
2400	61.582-11.524j	63.136+48.251j	7.537
2500	61.648-14.408j	73.262+49.436j	7.165

Figure 3.8 shows the measured and simulated S-parameters of the system. The graph shows that the simulated and actual amplifier is in good agreement across the entire operating band. Through testing, there were a few things to note that differ between simulation and implementation. The simulation relies on closed-form elements to represent the layout. These elements do not account for the entire geometry of the board and all the parasitics. The lack of accuracy in the model is producing most of the errors.

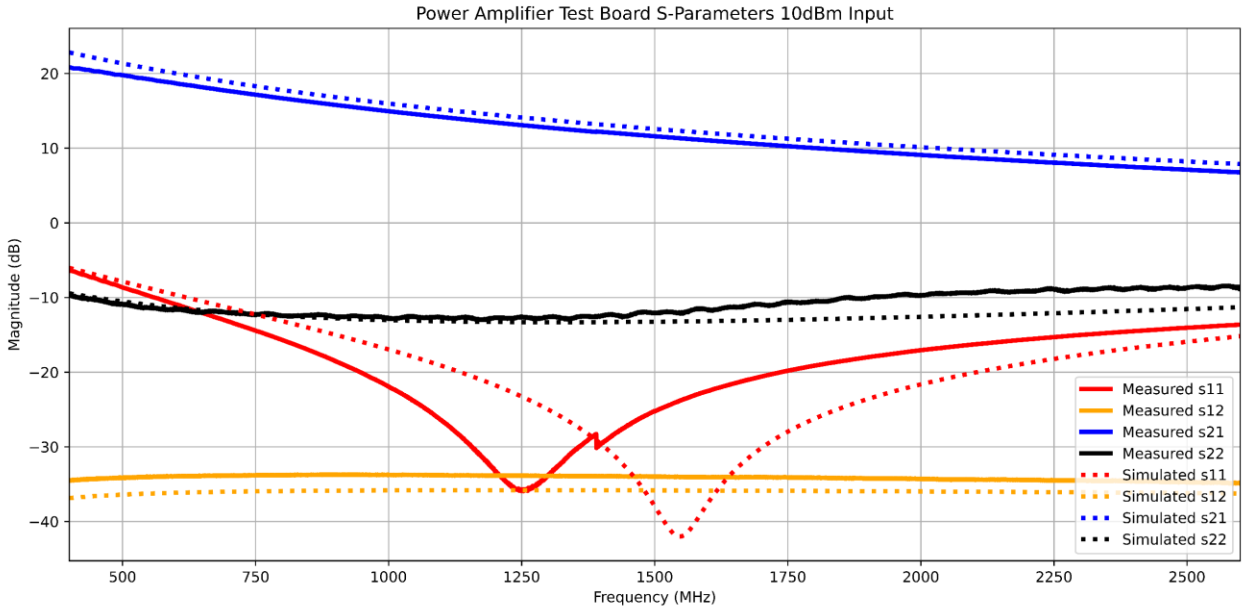


Figure 3.8: Power Amplifier Test Board S-parameters 10dBm Input

Figure 3.9 on shows the smith chart representation of the amplifier input and output impedance. From the graph, simulation and reality agree. This graph verifies the simulation for further use.

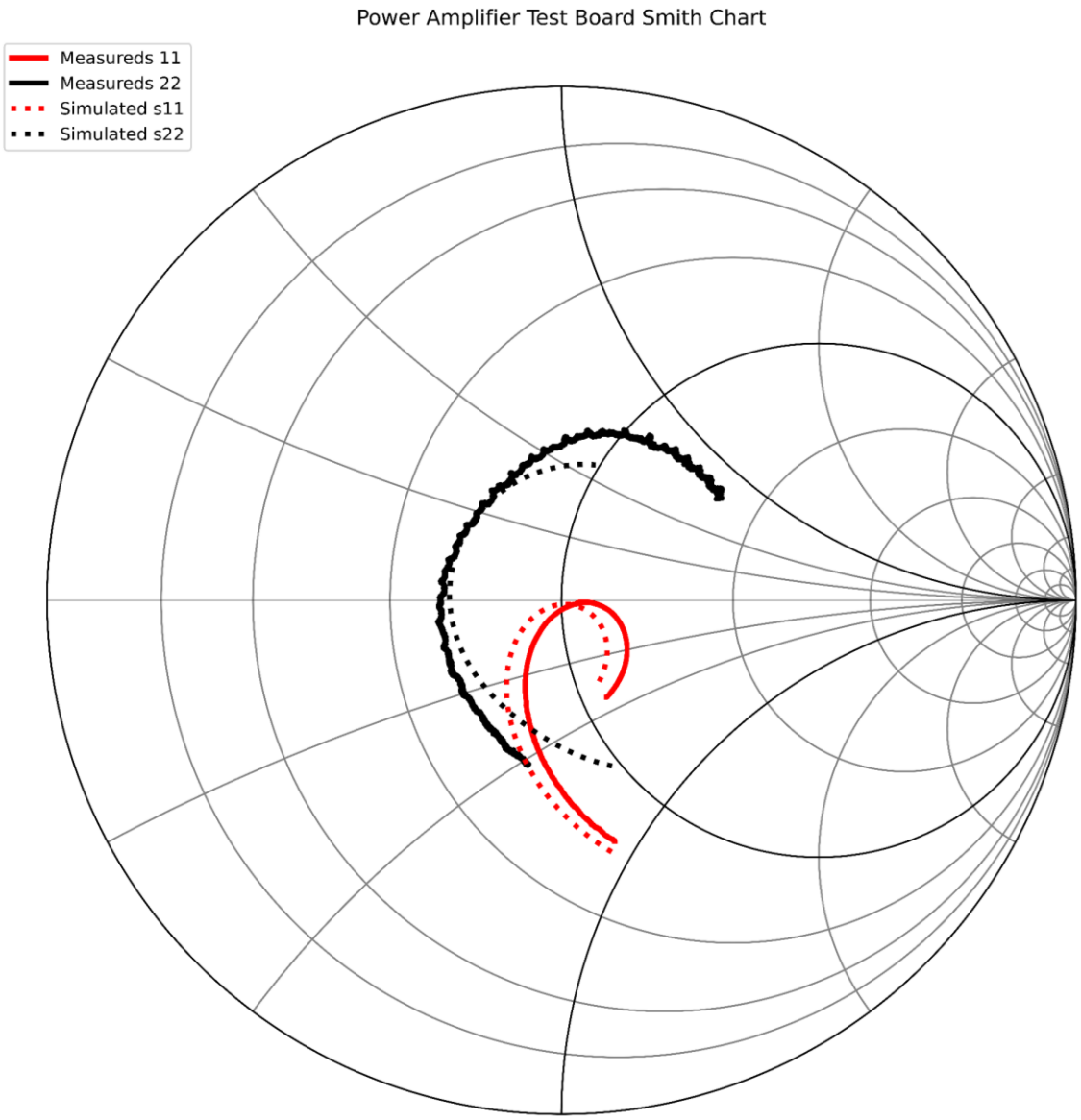


Figure 3.9: Unmatched Power Amplifier S-parameters and Smith Chart

The most significant error removed from the system simulation was the cable-to-board connection. The transmission line elements available could not recreate the effect. An HFSS simulation of the board to cable connection produced the accurate results shown in *Figure 3.9*. *Figure 3.10* shows simulated results both with and without the connectors. The results from providing connector models prove that the amplifier simulation without the connectors is sufficient to further model the rest of the system.

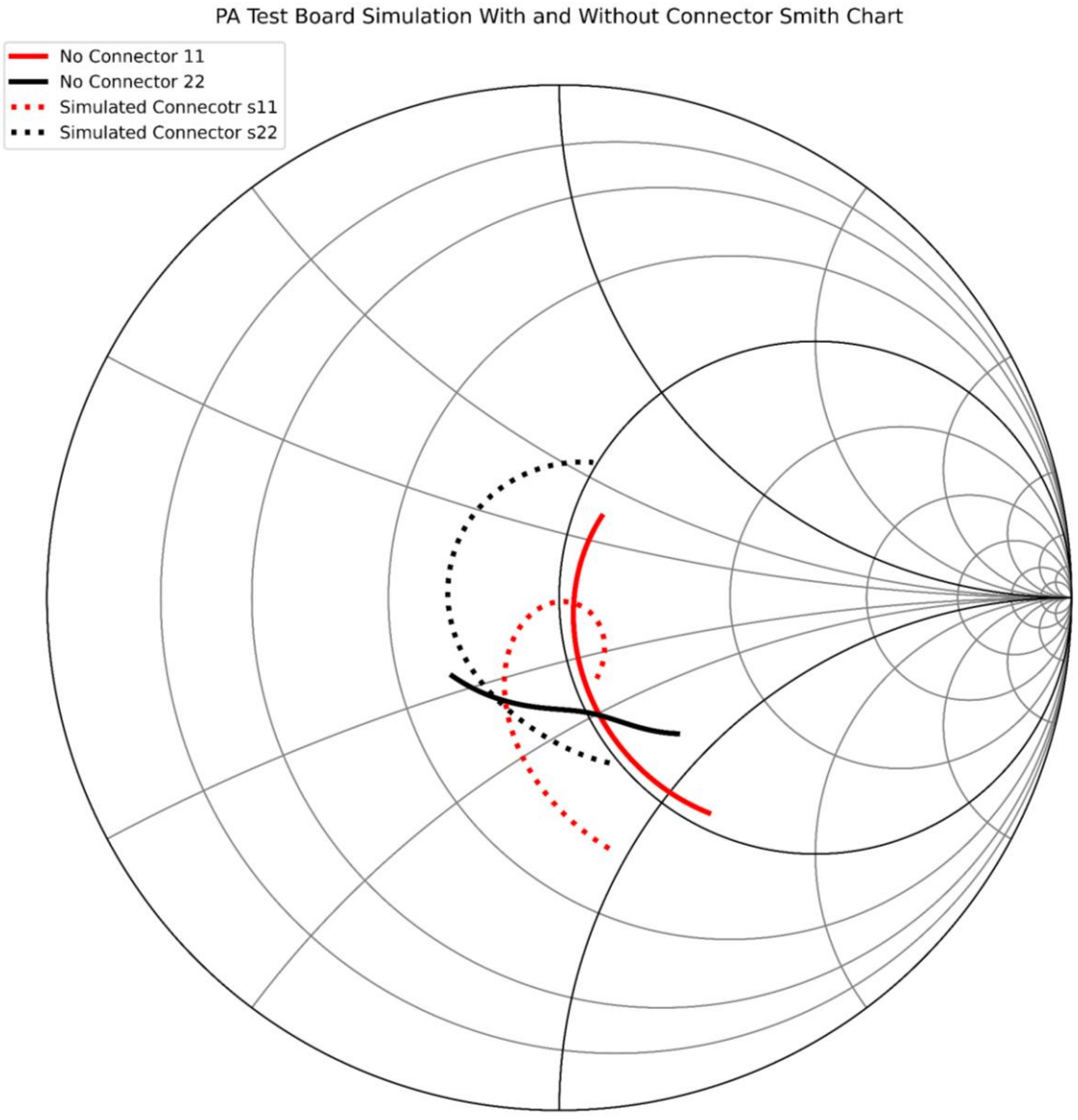


Figure 3.10: Power Amplifier Simulation With and Without Connector models

The Microwave Office simulation setup is in *Figure 3.11*. The simulation provides the starting point to designing the rest of the system. The amplifier simulation is used in conjunction with other sub-circuit simulations to gain insight into the final operation.

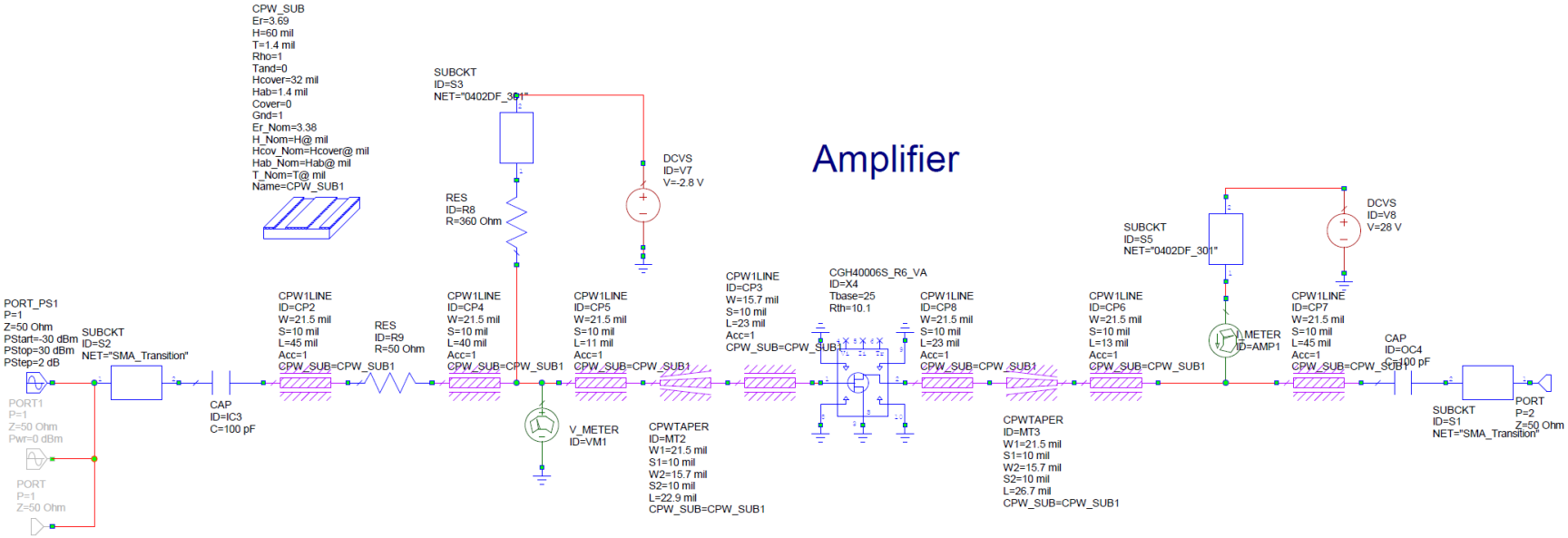


Figure 3.11: Power Amplifier Test Board Simulation Setup

3.5.4 Amplifier Test Results Summary

The amplifier is linear and operates as simulated across the entire frequency range, and can output the desired amount of power from the data presented. *Table 3.4* shows the requirements looked at in this section and whether the amplifier met the design specification.

Table 3.4: Amplifier Test Results Summary

Specification	Requirement	Achieved?
Frequency Range	500-2500	Yes
Power	27-30dBm	Yes
Classification	Linear	Yes

3.6 Summary

Chapter three discussed the methods and techniques for the system design. These included the procedures for simulations, design of the amplifier that is to be matched and system block diagram. The work presented in the chapter provides the base foundation for the design of the system and the results in the next chapter.

CHAPTER 4. RESULTS

4.1 Overview

The following chapter outlines the work completed to develop and test a prototype feedback-driven input and output matching network used with a power amplifier. Each subsystem is discussed in detail, and the results are given. The subsystems are described in order of the design process. First, the matching networks are presented as these are the crucial component to the amplifier. Next, the sensing method is discussed to provide feedback. The completed system integration is then discussed as all hardware is designed at that point. The system integration section is followed by the control method. The system power added efficiency results are then presented, followed by a summary of all the subsystems working together. The chapter concludes with the system assumptions, delimitations, and limitations of the research.

4.2 Matching Network

The following section covers the design and testing of the amplifier's input and output matching networks. For both the input and output matching networks, control of the varactors occurs using the AD5504. This component is a regulated 30V, 12bit resolution, digital to analog converter (DAC) from Analog Devices. The device receives power from the same 28V power supply as the amplifier. The DC output of the DAC then biases the different varactor bias lines. All attempts to avoid switches, especially in the transmission line, are made as parasitics cause further losses and mismatches but are unavoidable (Franco & Dening, 2011). The systems source and load impedances are set statically to 50Ω due to the ports and the Network Analyzer used for testing. Each test board uses Oshpark’s four-layer manufacturing service for construction.

4.2.1 Matching Network Design

The method of designing the match for the input and output followed similar processes. The first step was to determine the rough number of elements needed in each circuit based on the amplifier's Smith chart response. Next, add matching elements and tune manually in simulation to achieve optimal matches on the simulated amplifier. The next step

is to condense the matching circuits by removing elements that did not provide a beneficial effect. These are shunt elements with a high impedance and look like an open circuit and series elements with a low impedance that look like shorts in the frequency range. After condensing the circuits, identify the tunable element(s) in the matching network and record its required value and tuning range. Identify purchasable components that meet the simulated result and simulate. *Figure 4.1* shows a diagram of the design process listed. This design method was proven to provide a wide tuning range, from 900MHz to 2100MHz (Neo, et al., 2006). A similar configuration achieved a tuning range was from 800MHz to 7500MHz (Nesimoglu, Aydın, Atilla, Köprü, & Yarman, 2013).

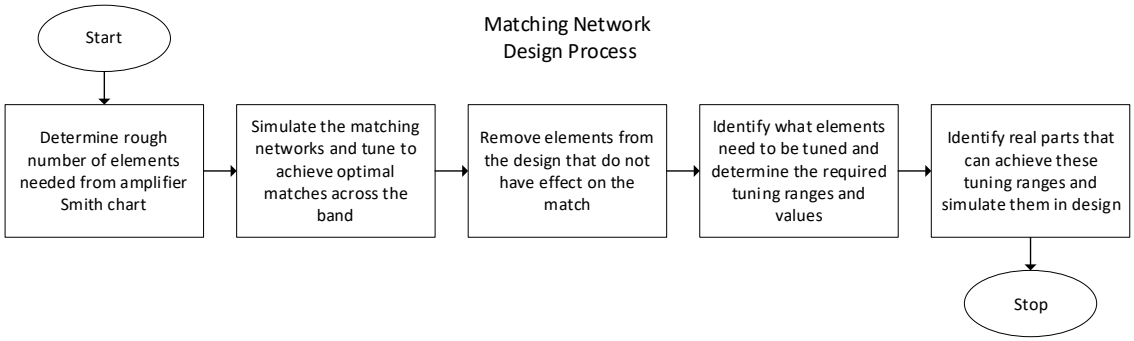


Figure 4.1: Matching Network Design Process

*4.2.1.1 **Input Matching Network Design***

A low pass T-Network is estimated to be a good starting point for the matching network's input. The reasoning stems from the input impedance being on the capacitive side of the 50-ohm circle of the Smith chart. The final design removes the shunt element due to unrealistically small capacitances required (<1pF). The series element is a tunable inductor that places a varactor in series with an inductor. This method has proven to be an effective way of tuning inductors (Arabi, Xingran, Morris, & Beach, 2017) (Nesimoglu, Aydin, Atilla, & Yarman, 2013). The varactor consists of two varactors in series wired common cathode. A single series resonator did not have enough tuning range, so a switch bank of tunable inductors provides the system's needed tuning range. Each leg used a different inductor value

instead of changing the varactor topology. Below is the input matching circuit schematic *Figure 4.2*, layout *Figure 4.3*, built board *Figure 4.4*, and Bill of Materials (BOM) *Table 4.1*.

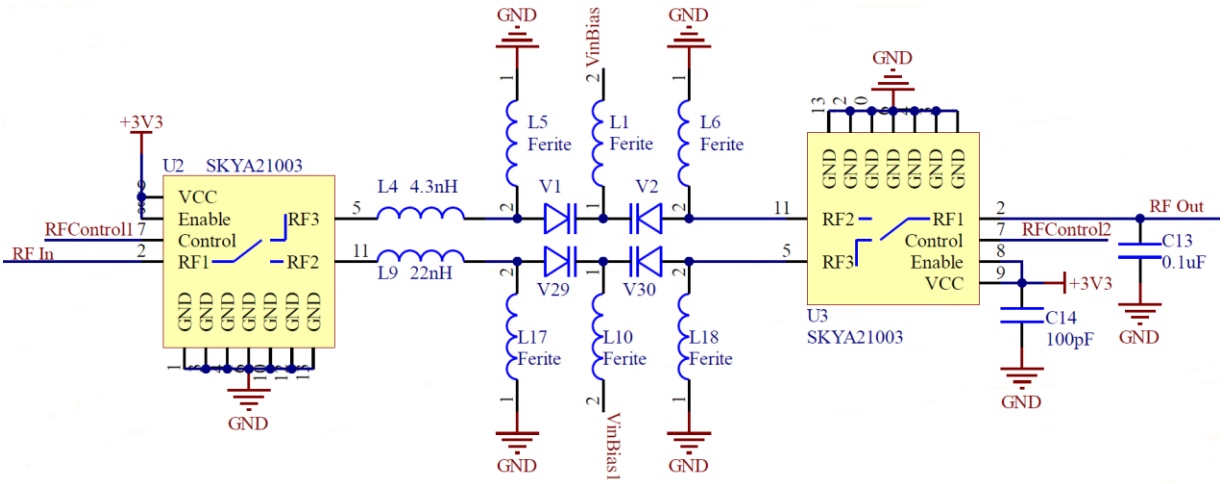


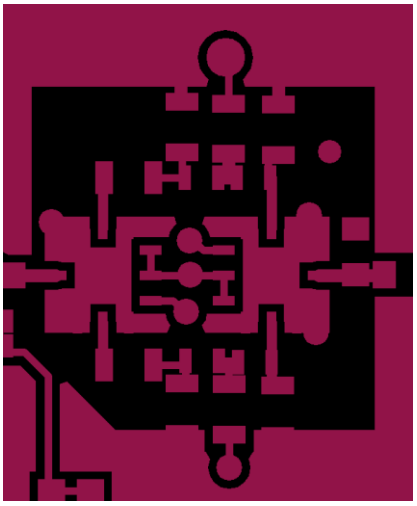
Figure 4.2: Input Matching Network Schematic

The bill of materials in *Table 4.1* shows all the components required to build the input matching network. The components are readily available from electronic component distributers. The reference designators correspond to the designators in the schematic in *Figure 4.2*.

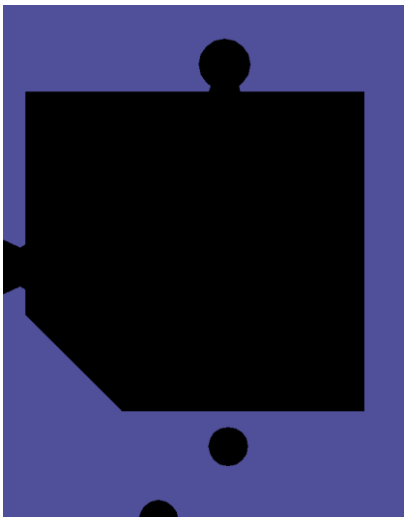
Table 4.1: Input Matching Network BOM

ID	Designator	Comment	Manufacturer	Part Number	Qty
1	C14	100pF	KEMET	C0402C101J3GACTU	1
2	L4	4.3n	Coilcraft	0402DC-4N3X_R_	1
3	L9	22nH	Coilcraft	0402DC-22NX_R_	1
4	V1, V2, V29, V30	Varactor	Skyworks	SM1265	4
5	L1, L5, L6, L10, L17, L18	Ferrite	Coicraft	0402DF-301XJRW	6
6	U2, U3	RF Switch	Skyworks	SKYA21003	2

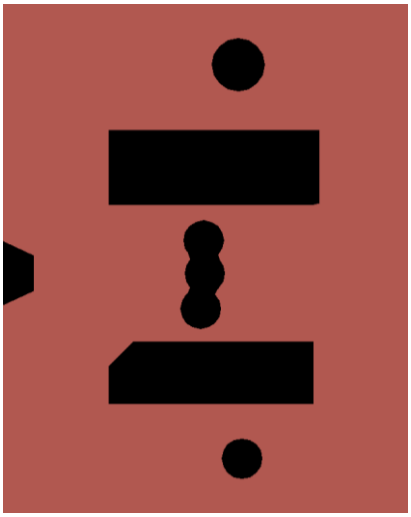
Figure 4.3 on page 91 shows the layout of the input matching network. The figure contains only the copper layers through out the board as well as the 3D model of the input matching network.



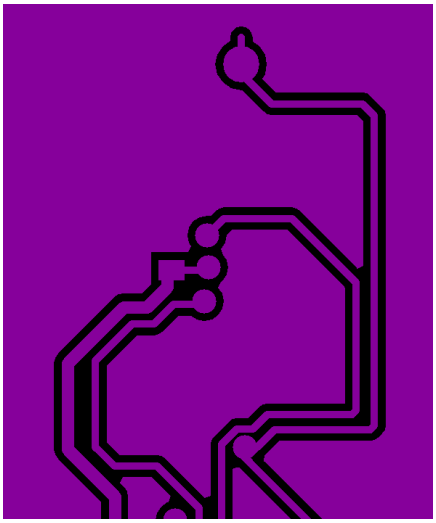
Top Layer



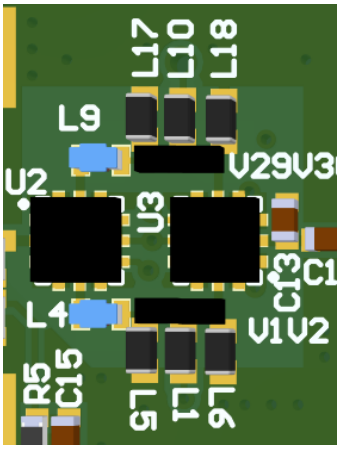
Layer 2



Layer 3



Bottom Layer



3D Model

Figure 4.3: Input Matching Network Gerber Layers and 3D Layout

Figure 4.4 shows a close up of the input matching network as built. The input to the network is on the left side and the output is on the right side of the image.

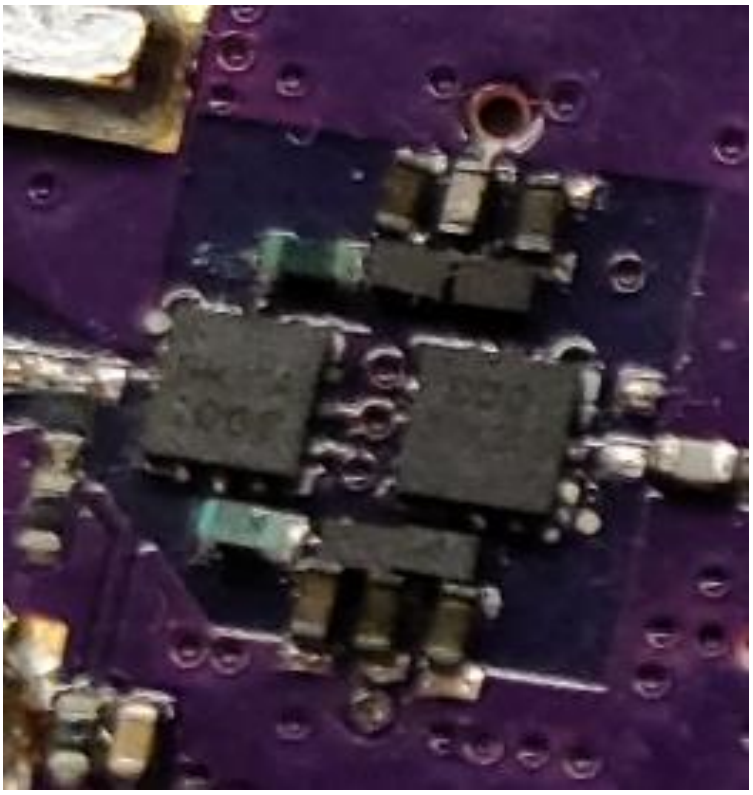


Figure 4.4: Assembled Input Matching Network

One thing to note is that the input of the system suffers from a ground problem. Between the amplifier design phase and the system design, there is an iteration where the ground plane's placement changes. The change moves ground from the bottom layer to layer two in the system, only 5mils away from the RF circuits. This change introduced unaccounted for parasitics that degrade the performance of the matching circuit. The ground plane is on layer four under the matching circuit in the final design but unintentionally left on layer two under the amplifier. Though changing the ground plane placement under the matching circuit helps, there are still issues with the RF signal coupling to ground in the amplifier section before reaching the transistor. Removal of the ground plane under the amplifier or adjusting the input match to account for this parasitic will yield better results at the upper frequencies.

4.2.1.2 Output Matching Network Design

The output started as a cascaded L matching network with four elements in a low pass configuration. The output impedance is on the Smith chart's capacitive side but moves across the resistive impedance portion meaning a more complex topology is needed. The final design is a low pass pi network that required a tunable inductor and capacitor. The tunable inductor consists of a varactor bank (VB1) in parallel with the inductor (L8) to provide relative tuning. The inductor tuning varactor consisted of a four-by-four array of varactor diodes for power handling and tuning range. This topology's other varactor (VB2) consisted of either a two by four or three by four array for less capacitance. The output matching circuit did not provide operation across the entire frequency range, as discussed later. VB2 is the limiting factor in the output tuning range, and in order to test the full frequency range, the varactor topology changes. The term “low band” used throughout the rest of the work refers to the system having a three-by-four varactor array for (VB2). The term “high band” refers to the same varactor array in a two-by-four configuration. The following shows the output matching network’s schematic *Figure 4.5*, layout *Figure 4.6*, built board *Figure 4.7*, and BOM *Table 4.2*.

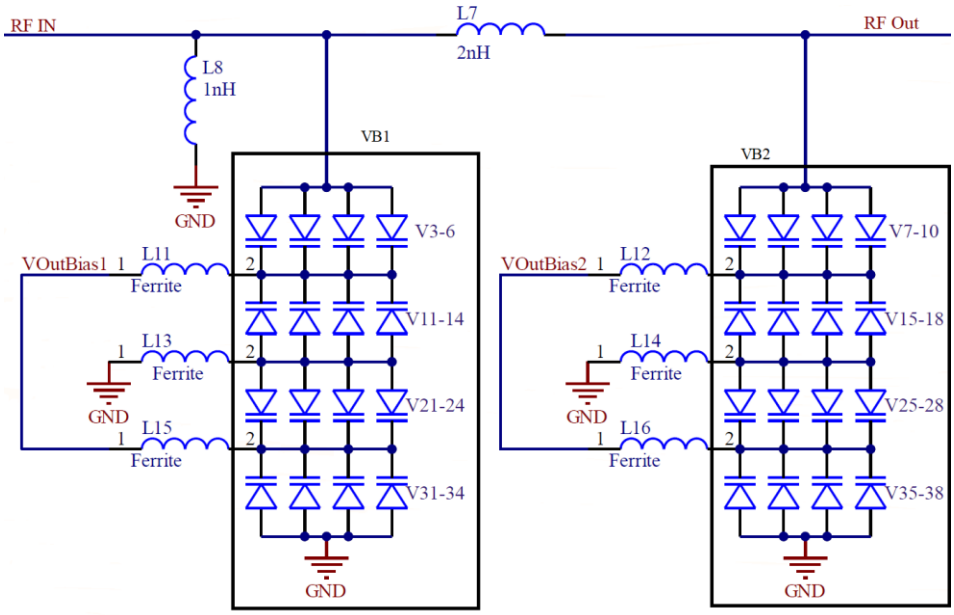


Figure 4.5: OutputMatching Network Schematic

Table 4.2 contains the parts to build the output matching network. Each of the components listed is available from electronics distributors.

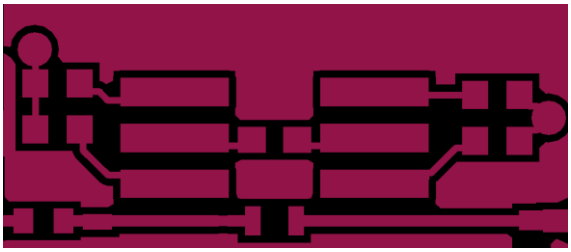
Table 4.2: Output Matching Network BOM

ID	Reference	Comment	Manufacture	Part Number	Qty
1	V3, V4, V5, V6, V7, V8, V11, V12, V13, V14, V15, V16, V21, V22, V23, V24, V25, V26, V31, V32, V33, V34, V35, V36, V9, V17, V37, V27,	Varactor	Skyworks	SM1265	30/34
2	L11, L12, L13, L14, L15, L16	Ferrite	Coicraft	0402DF-301XJRW	6
3	L8	1nH	Coilcraft	0402DC-1N0X_R_	1
4	L7	2nH	Coilcraft	0402DC-2N0X_R_	1

Notes

- Red varactor reference designators are optional varactors for VB2 for low band operation. If the system uses high band operation, do not populate these varactors.
- Do not populate V10, V18, V28, V38 in VB2

Figure 4.6 on page 95 contains the layout of the output matching circuits. The layers shown are only of the copper layers and the 3D representation of the matching network. Other than the top layer, all layers under the output matching network are ground. Components are placed close together to minimize parasitics.

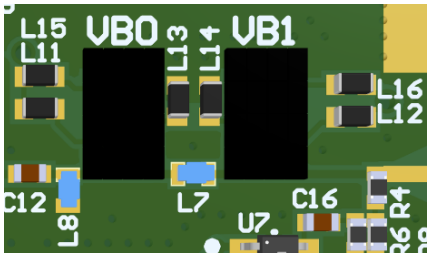


Top Layer

Layer 2

Layer 3

Bottom Layer



3D Layout

Figure 4.6: Output Matching Network Layout

Figure 4.7 on 96 shows the as built representation of the output matching circuit for high band configuration. To achieve low band configuration an extra bank of varactors is placed on the gold pads. Note that the input from the amplifier is on the left and the output to the load is on the right side of the image.

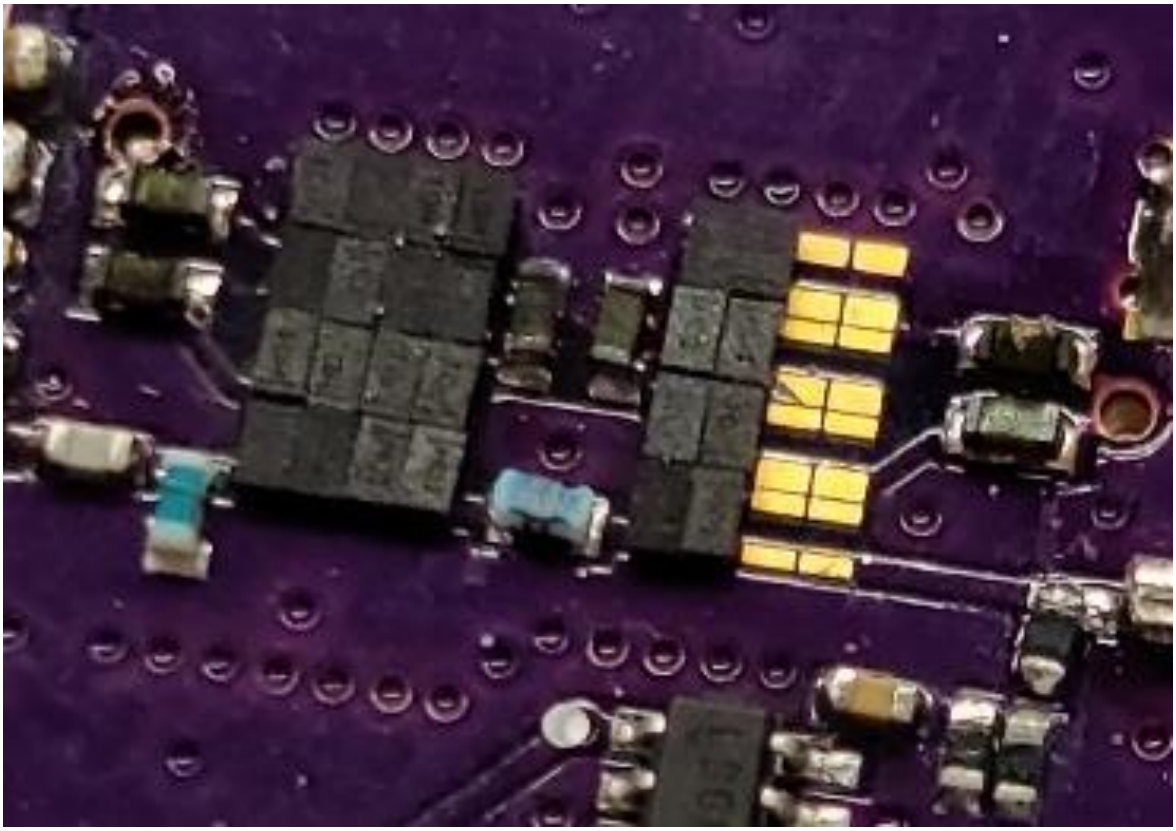


Figure 4.7: Built Output Matching Network

4.2.2 Matching Network Test Setup

The test setup for the matching networks includes building them in-system with the amplifier. The following tests show the operation of the power amplifier at fixed frequencies across the range. As will be seen, the matching networks and amplifier respond properly but lose gain and output power.

The amplifier drain is biased to 28V at 100mA. Port 1 of the VNA runs to the system's input, while port 2 runs to the output. *Figure 4.8* shows the test setup to test each matching network. The VNA is then set up to output an 8dBm signal from 400MHz to 3GHz. Each matching network is then manually tuned to a frequency between 500 and 2500MHz.

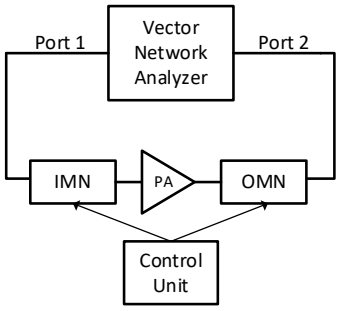


Figure 4.8: Test Setup for Matching Network Measurements

4.2.3 Matching Network Results

Figure 4.9, *Figure 4.10*, and *Figure 4.11* show the comparison of simulated and measured results at 520, 1000, and 2200MHz, respectively. From these, one can see that simulated and measured results are in good agreement. The simulated results are of the low band configuration of the output matching network. In both simulation and reality for this design, the matching network could not achieve an upper-frequency response of 2500MHz without removing the extra varactors from VB2. The discrepancy between simulated and measured is due to the linear transmission line models. The models do not account for all the layout parasitics, such as coupling to other traces.

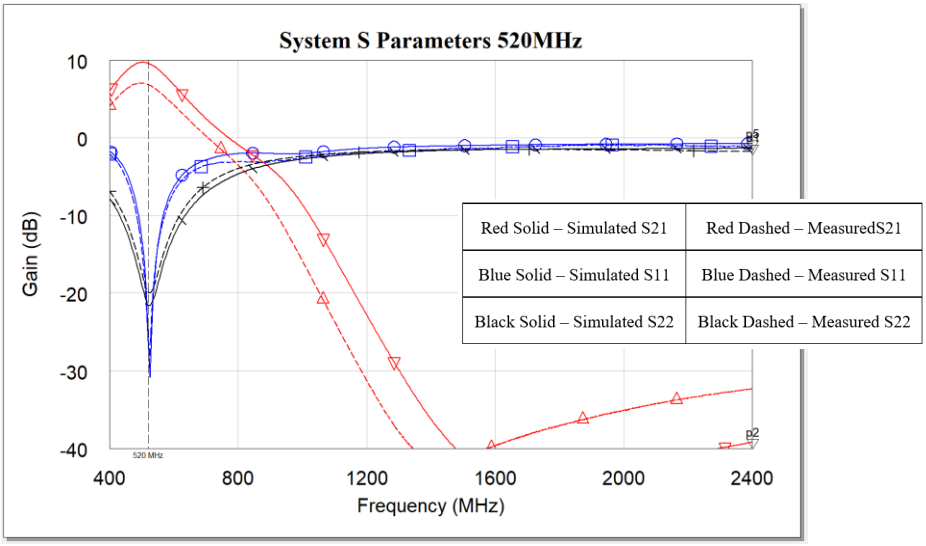


Figure 4.9: Simulated vs. Measured System S-parameters at 520MHz

Figure 4.10 shows the matching network operating at 1000MHz. The simulated and measured results are in good agreement at the operating frequency.

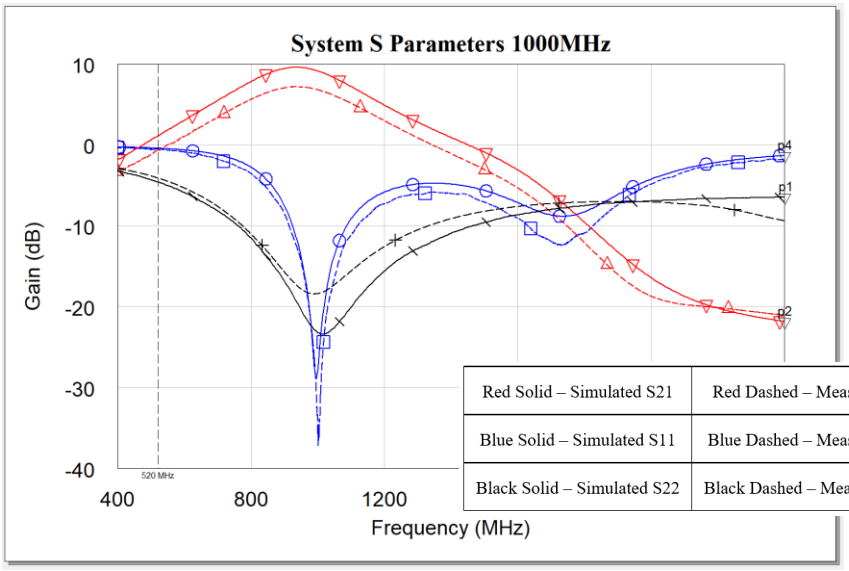


Figure 4.10: Simulated vs. Measured System S-parameters at 1000MHz

Figure 4.11 shows the system operating at 2200MHz. The input match achieved better results than simulated however the output match did not. The measured and simulated though are in agreement with eachother.

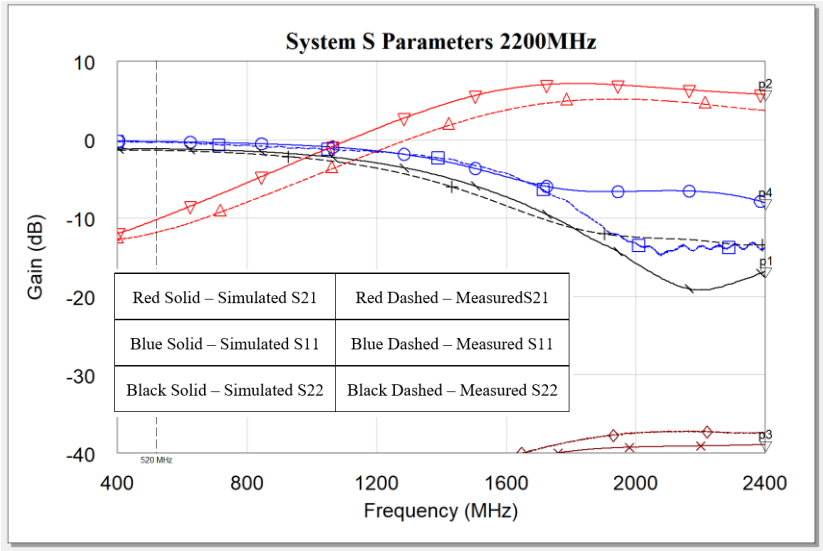


Figure 4.11: Simulated vs. Measured System S-parameters at 2200MHz

Table 4.3 records the tuning capabilities of the matching networks. From the table, the output matching network cannot achieve the maximum frequency tuning range in either configuration. This issue arises because VB2 in low band configuration, a three-by-four varactors bank, cannot produce a low enough capacitance. The low band configuration yields a tuning range of 500-2200MHz with diminishing returns after 1900MHz. When reducing VB2 to two by four, the tuning range's bottom end is lost but achieves the upper-frequency parameter 800-2500MHz.

Table 4.3: Theoretical Match to Amplifier Capability

Frequency (MHz)	Input Matching Network Impedance From Port 1 (Ω)		Output Matching Network Impedance From Port 2 (Ω)	
	Low Band	High Band	Low Band	High Band
500	62.575-5.562j	NA	40.538-66.786j	NA
600	58.242-2.875j	NA	87.043+35.047j	NA
700	53.381-4.718j	NA	21.459-85.978j	NA
800	44.165+4.681j	52.419-3.112j	44.434+3.051j	54.550-1.338j
900	42.844+5.878j	51.797-2.246j	43.651+4.531j	52.036-4.909j
1000	42.692+8.230j	50.483-1.008j	43.447+6.683j	48.017-4.525j
1100	42.780+10.530j	48.464+0.454j	42.381+8.086j	45.176-1.891j
1200	42.738+12.670j	47.961+1.510j	43.170+10.567j	45.928+2.016j
1300	43.084+14.909j	48.152+0.369j	43.615+12.689j	48.193+3.538j
1400	43.849+17.278j	49.265-0.995j	44.917+14.994j	50.869+4.258j
1500	45.636+19.696j	49.299-1.638j	46.744+17.141j	51.169+4.388j
1600	48.774+21.937j	50.093-3.186j	49.693+18.945j	51.301+1.742j
1700	53.785+23.437j	48.806+0.064j	53.349+20.053j	51.528+1.016j
1800	59.903+23.285j	47.559+2.300j	57.377+20.043j	50.411-1.778j
1900	66.342+21.142j	46.048+5.600j	60.951+19.284j	49.215-2.039j
2000	71.961+16.438j	43.738+8.230j	69.749+11.213j	46.235-3.505j
2100	75.308+9.871j	42.123+11.980j	72.632+1.812j	45.068-2.606j
2200	75.898+2.703j	39.489+15.479j	71.330-5.731j	43.845-0.343j
2300	NA	39.252+19.969j	NA	46.022+0.998j
2400	NA	46.749+24.367j	NA	47.859+0.545j
2500	NA	55.274+25.461j	NA	48.616-0.265j

To show the tuning capabilities of both sets of matching networks, *Figure 4.12* shows the system state at varying frequencies. The low band configuration shows the tuning at 500, 1000, 1500, 2200MHz, and the high band configuration shows 800, 1000, 1500, 2500MHz. From the graph, the gain performance between the two configurations is consistent. The high band and low band systems achieved good matching results on both input and output in the respected operation

frequencies. The definition of an acceptable match is having less than -12dB of reflected power on S11 or S22 for the input and output respectfully. The characterization of each matching circuit (input and output) is independent of the other circuit.

The input matching networks for both systems have an identical circuit, and the graphs show similar operations within 3dB at each matched frequency indicating good consistency. For the output matching circuits, up until 2000MHz, both configurations produce matches well below -20dB in the S22 response. The high band configuration produces a significantly better-matched result, -15dB lower than the low band configuration, at frequencies over 2000MHz. However, the high band failed to produce a match lower than 800MHz compared to the 500MHz from the low band configuration.

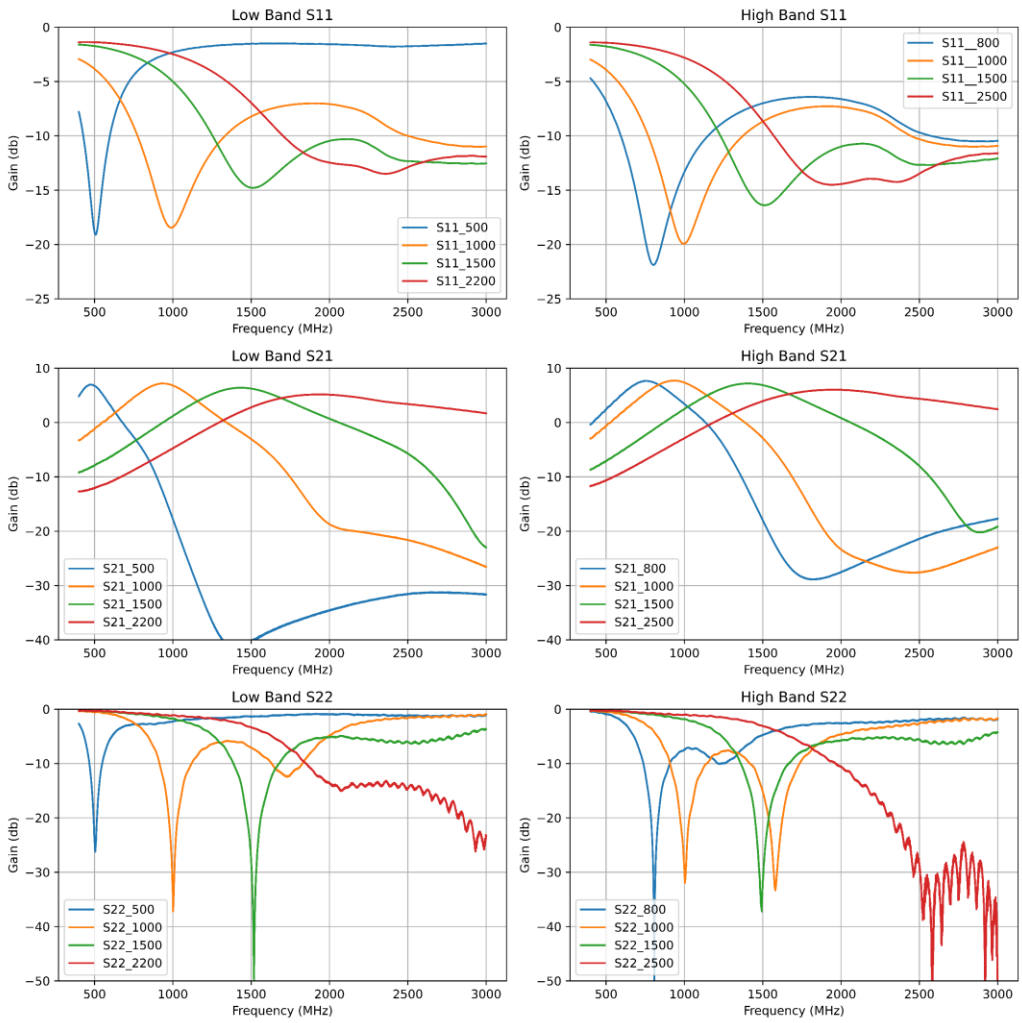


Figure 4.12: System Matching Network Swept S-parameters

As discussed, the S-parameters show the input and output match are acceptable. One point of note is that the gain (S21) was much lower than expected. The initial design's expected gain is approximately 20dB at 500MHz. Here gains of 7.5dB were measured. The lower gain affects the final output power of the system. Max power of 8dBm drove the amplifier, which should have produced 28dBm of output power. Due to the low gain, the maximum output power, however, was 15.5dBm. Since the amplifier could not produce the correct power level, there are no test results for the output matching networks operating at max power. However, at the produced output power, it will be shown that the automatic feedback tuning does operate properly, albeit with a lower gain and output power.

Due to the varactor's nature, higher output powers will cause a change in capacitance, thus changing ideal tuning frequency. The change in capacitance is due to the induced voltage from the RF signal across the varactors. When transmitting lower power levels, less than 0dBm input, through the matching networks, the response did not change from that measured at 8dBm, indicating that the output matching network is capable of power handling up to 15.5dBm and the input can handle 10dBm.

As mentioned, the matched amplifier gain is more than 10dB lower than unmatched, indicating an issue with the output matching circuit. A conjugate matched amplifier in small-signal analysis will produce more gain than when it is unmatched. A load-pull analysis on the amplifier proves that the output should have a much higher gain than it does. *Figure 4.13* shows that max gain is at the conjugate match of the amplifier. The matching circuit should present the same impedance as the max gain point to the amplifier.

When plotting the output matching network’s simulated S11 S-parameter, one can see that the match is nowhere near the maximum gain point. It is well outside the 16.5dB load-pull circle, which explains why the amplifiers gain at this frequency is so low. The matching circuit having the wrong impedance for the amplifier is in direct conflict with the measured S22 shows a proper match. Matching networks should be symmetric; if the match presented to the load is ideal, then the match presented to the amplifier should be ideal.

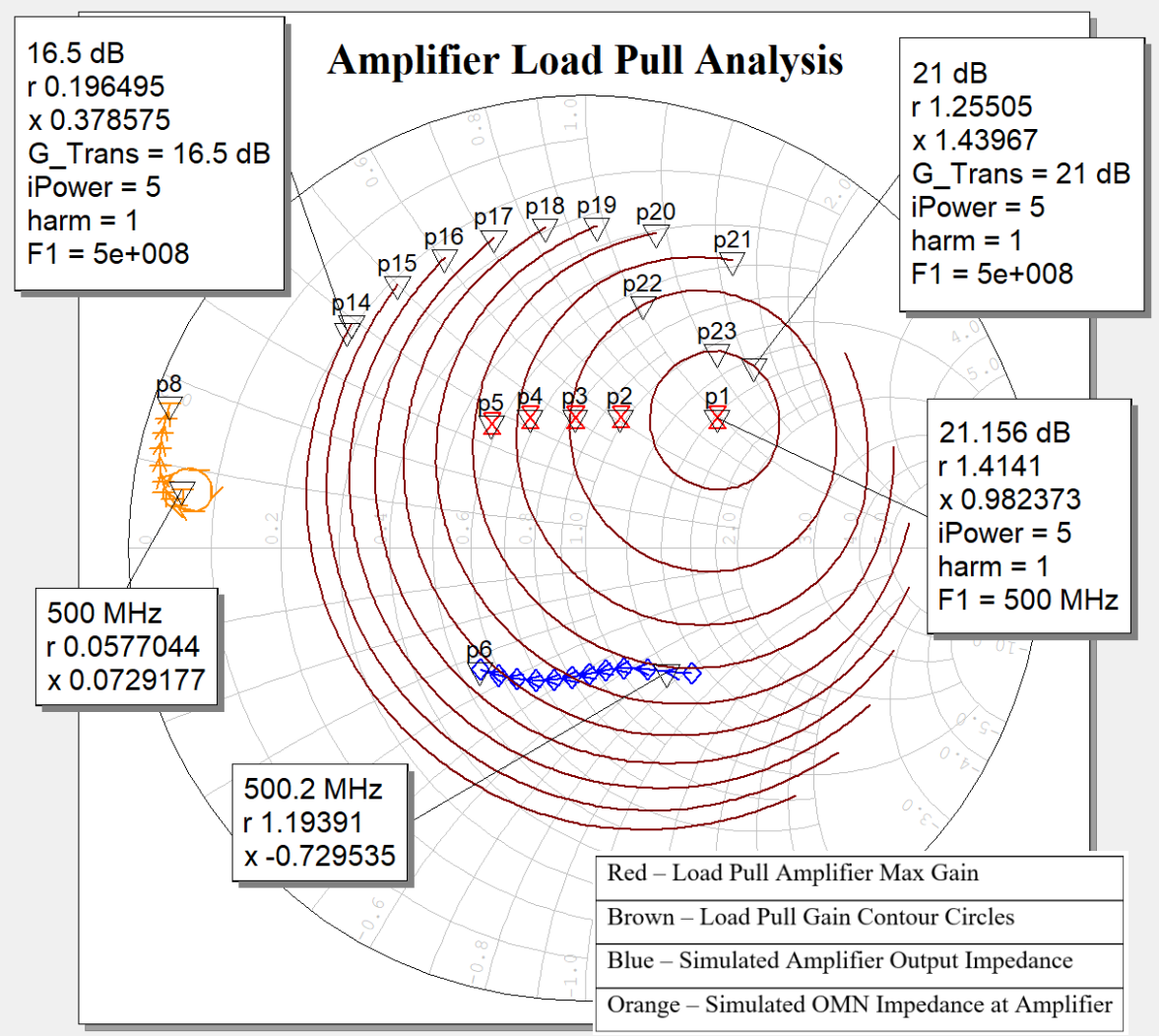


Figure 4.13: Amplifier Load Pull Analysis

To determine why the gain is low but the system sees a good match, a source port containing the same impedance as the amplifier at 500MHz replaces it. From here, the power into the source port is the power transmitted into the amplifier. *Figure 4.14* shows the simulated setup where SUBCKT S1 is the simulated model of the output matching network. Port P1 is the amplifier, and Port P2 is the load. A passive network's total power is one, which is the sum of the squares of the transmitted, reflected, and absorbed power EQN(4.1).

$$1_{Total\ Power} = Power_{S11}{}^2 + Power_{S21}{}^2 + Power_{Lost}{}^2 \qquad \text{EQN(4.1)}$$

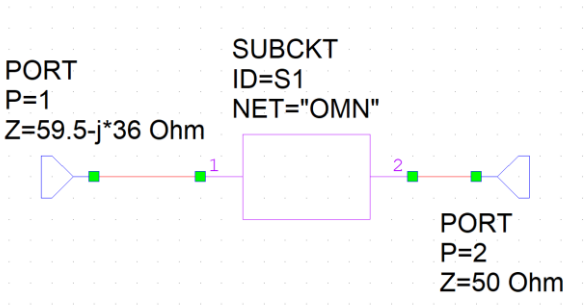


Figure 4.14: Output Matching Network Amplifier Replacement

The linear S-parameters simulation shown in *Figure 4.15* indicates that the matching network absorbs the power from Port2. The total power loss from the amplifier to the load due to the matching network is 0.270. Though lossy, a significant portion of the amplifier's power to the load is accounted for in the transmitted and reflected power and not lost. The power loss from a wave traveling from the load to the amplifier is 0.961 or almost all the power. The difference in power absorption is why the system appears to be optimally matched but produces a low gain.

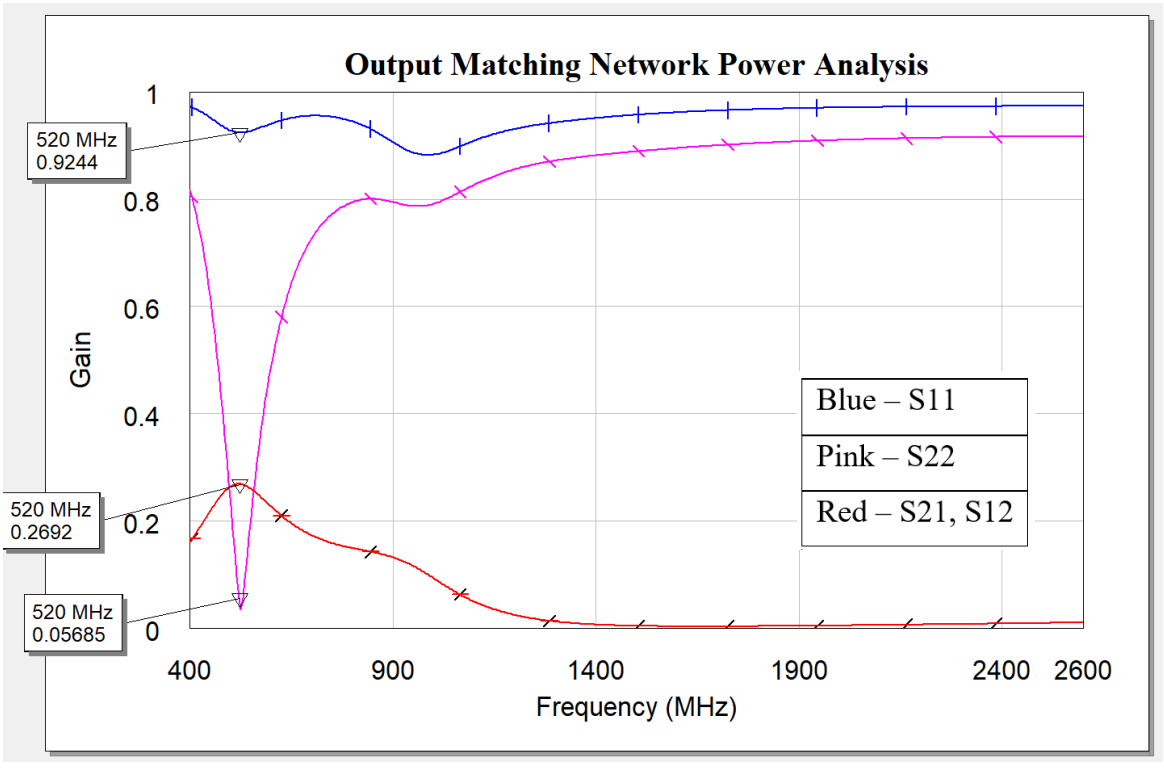


Figure 4.15: Output Matching Network Power Analysis

Table 4.4 shows the power from each port and where the power ended in the system. From the table, the transmitted and reflected power are used to calculate total power. The power loss is then calculated from the total power.

Table 4.4: Output Matching Network Power Loss

Power Port	Transmitted	Reflected	Total Power	Power Lost
Port 1	0.269	0.924	0.926	0.270
Port 2	0.269	0.057	0.075	0.961

A redesigned static L matching network verifies that a conjugate match to the amplifier produces optimal gain with low reflection and does not absorb. The L matching network consists of a 0.6pF shunt capacitor and 12nH series inductor. See *Figure 4.16* for the matching circuit. Port one goes to the amplifier, and Port 2 is the load.

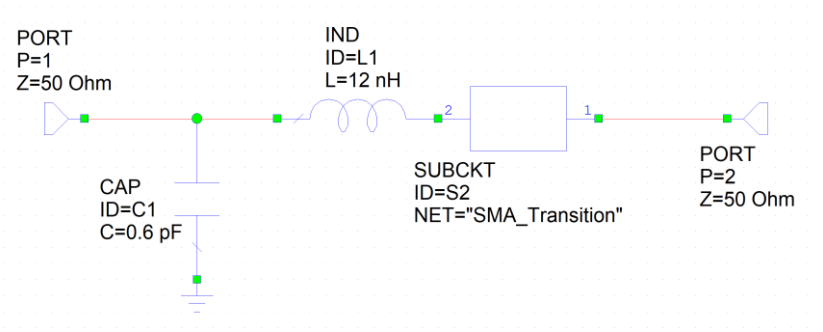


Figure 4.16: Redesigned Static Matching Circuit

The simulated results of the static matching circuit shown in

Figure 4.17 indicate that the amplifier is matched to 50Ω and produces a maximum gain with this circuit. The impedance of the matching circuit is close to the required impedance for maximum gain at 500MHz. When wired to the amplifier, the simulated matching network results show that the amplifier is matched in S22 by being close to the chart's center. The measured S22 results of the matching circuit are in good agreement with the simulation.

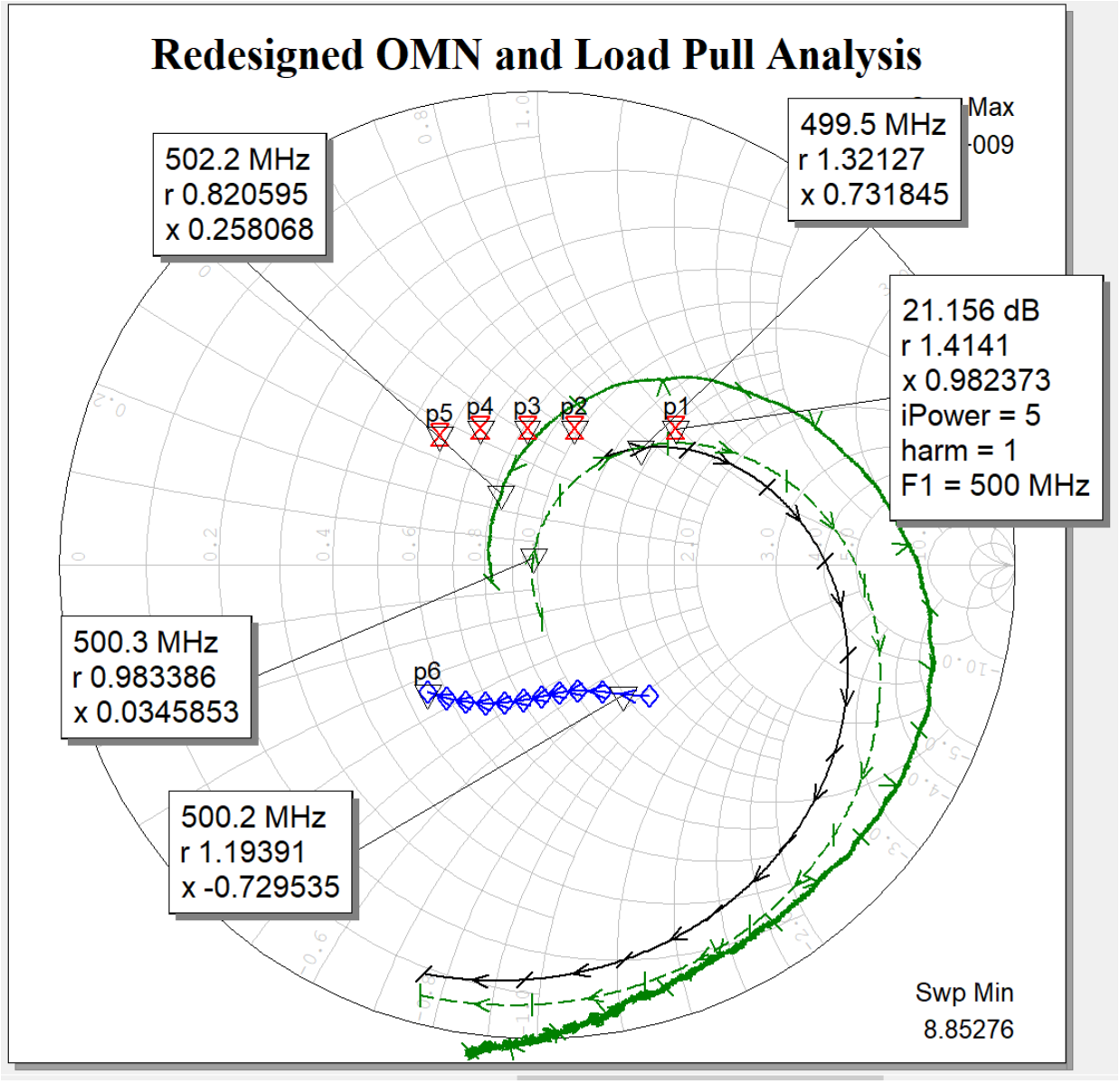


Figure 4.17: Redesigned OMN and Load Pull Analysis

The gain of the redesigned output matching network shown in *Figure 4.18* indicates that the amplifier is getting close to simulated max gain and that a good match is present at S22. The test verifies that a conjugately matched circuit of the amplifier does produce maximum gain and minimum reflections. The figure also verifies that simulation and reality are in good agreement.

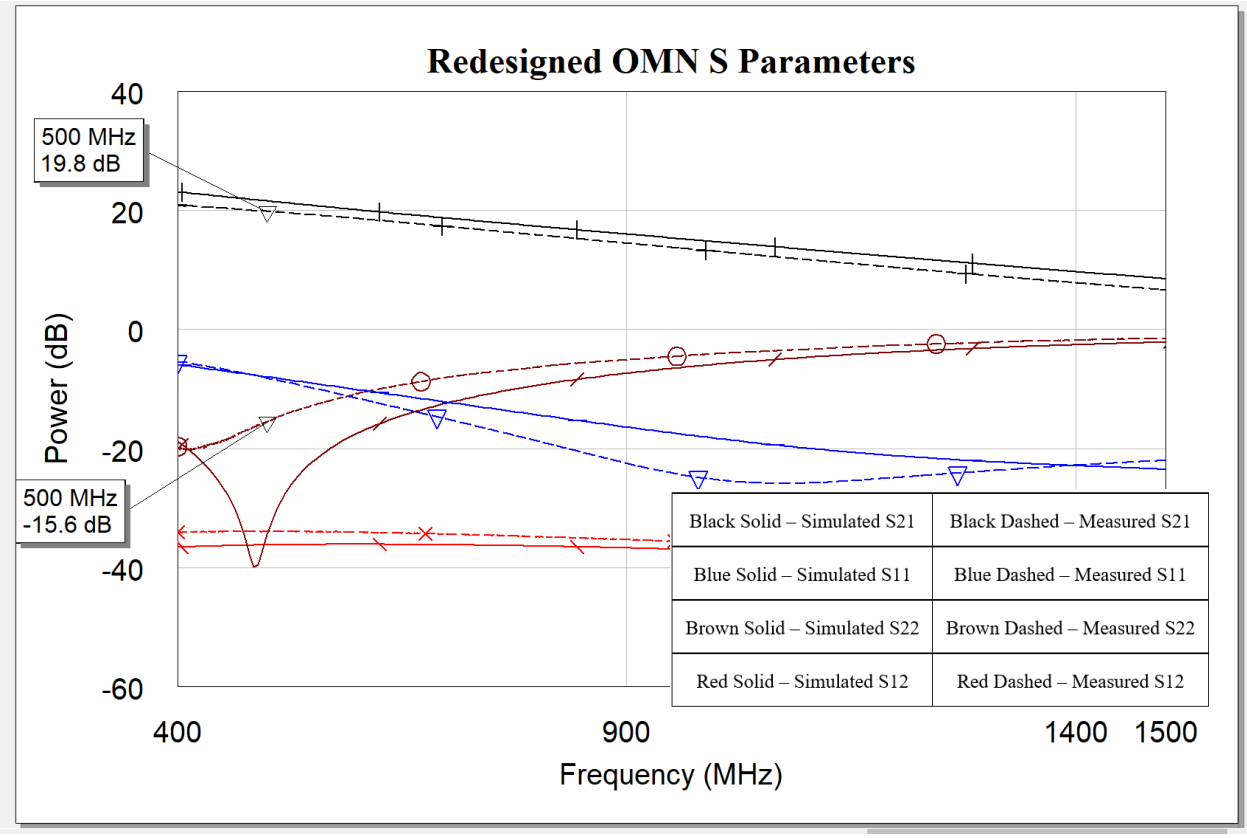


Figure 4.18: Redesigned OMN S-parameters

The last point of comparison is the power analysis of the redesigned matching network compared to the original design. From *Figure 4.19*, one can conclude that the matching network is not absorbing any signal. All the power is either reflected or transmitted to the load. *Table 4.5* shows the power transmitted, reflected, and lost to the system. The table confirms that the redesigned matching circuit does not absorb the power and produces high power transmission between source and load. This design yields a more favorable matching circuit for further investigation.

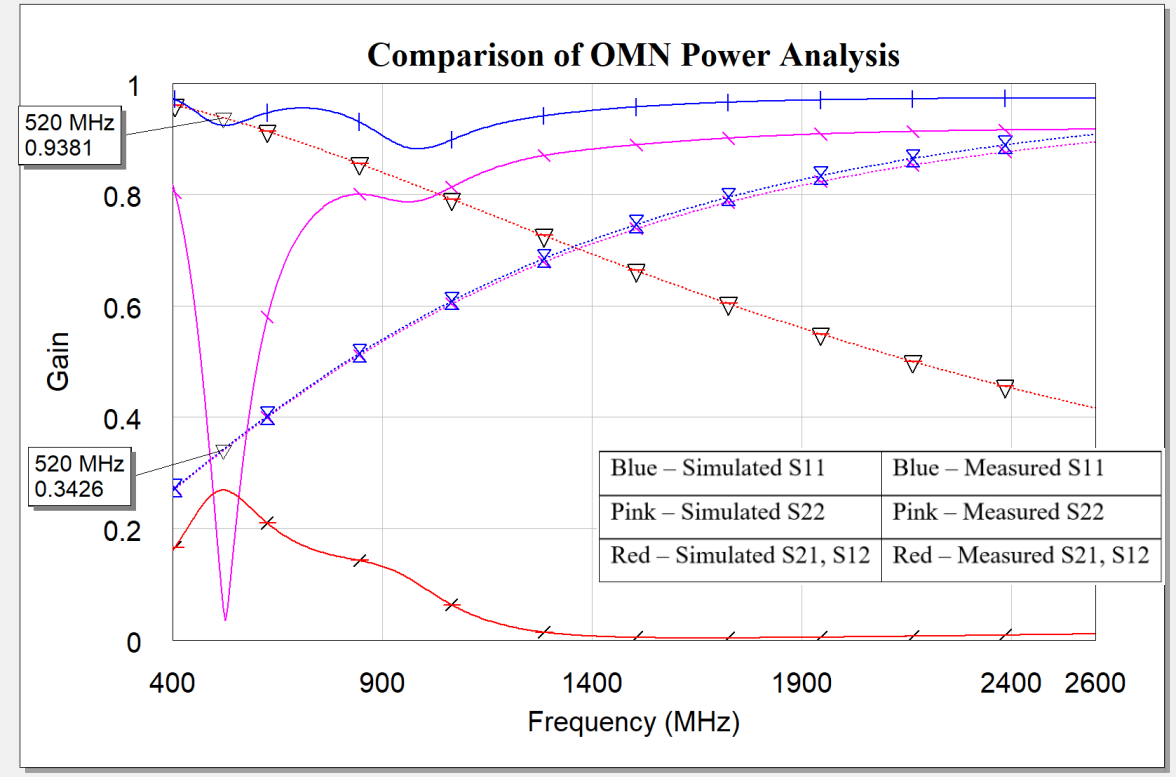


Figure 4.19: Comparison of OMN Power Analysis

Table 4.5 contains the data for how the power produced at each port is distributed throughout the system. According to the table, most of the power is transmitted to the load while little power is reflected or lost.

Table 4.5: Redesigned Output Matching Network Power Loss

Power Port	Transmitted	Reflected	Total Power	Power Lost
Port 1	0.938	0.343	0.997	0.050
Port 2	0.938	0.343	0.997	0.050

4.2.4 Matching Network Test Results Summary

The input and output matching circuits are operating as simulated. A mistake in the design phase failed to produce a circuit with an optimal match to achieve optimal power transfer from the amplifier's output. Due to the lack of power, the power requirement of the output matching circuit is untested. The input matching network did not need to handle as much power, only 8dBm, compared to the output matching network 27dBm and showed no signs of degradation during testing. The input frequency range did not meet specifications; the ground plane

placement change caused extra unaccounted for parasitics. The output matching circuit did not provide an optimal match due to the lack of tuning range of the VB2 varactors. *Table 4.6* shows the specifications for the matching circuits. However, these issues do not impede work into the prototype feedback tuning of the power amplifier.

Table 4.6: Matching Network Test Results Summary

Specification	Requirement	Achieved?	
		IMN	OMN
Frequency Range	500-2500	No	No
Power	27-30dBm	Yes	No

4.3 Sensing Method

The following section covers the design and testing of the sensing method for the feedback control system. The sensing method testing occurs in-system with the power amplifier and matching circuits. The results of this section drive the design of the control algorithm design in section 4.5.

4.3.1 Sensing Method Design

The network's sensing topology consists of resistive taps, power detectors, and analog to digital converters (ADC) on the system input and output. This design is similar to that of one proposed by Gu (Gu & Morris, 2013) in *Figure 4.20*.

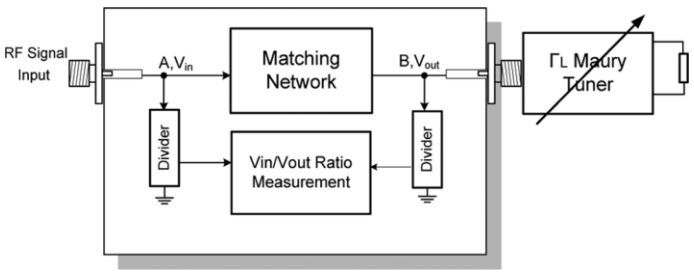


Figure 4.20: Reference Design for Sensing Method (Gu & Morris, 2013)

The resistive taps couples off small amounts of the RF chains signal to the power detectors without affecting the overall system performance. In the design, the resistive taps

provide approximately 30dB+ of attenuation. The attenuation allows for proper operation even at high power levels. The resistive nature of the taps also means that the taps do not change with frequency. The power detector then outputs a DC voltage corresponding to the power. The control system reads back the voltage through an analog to digital converter (ADC). This method also provides wideband performance and the ability to handle more power than other sensing options. The sensing technology was not tested independently but instead integrated directly into the final system prototype design. Below are the schematic *Figure 4.21* and *Figure 4.22*, layout *Figure 4.23*, built design *Figure 4.24*, and BOM *Table 4.7* of the feedback system.

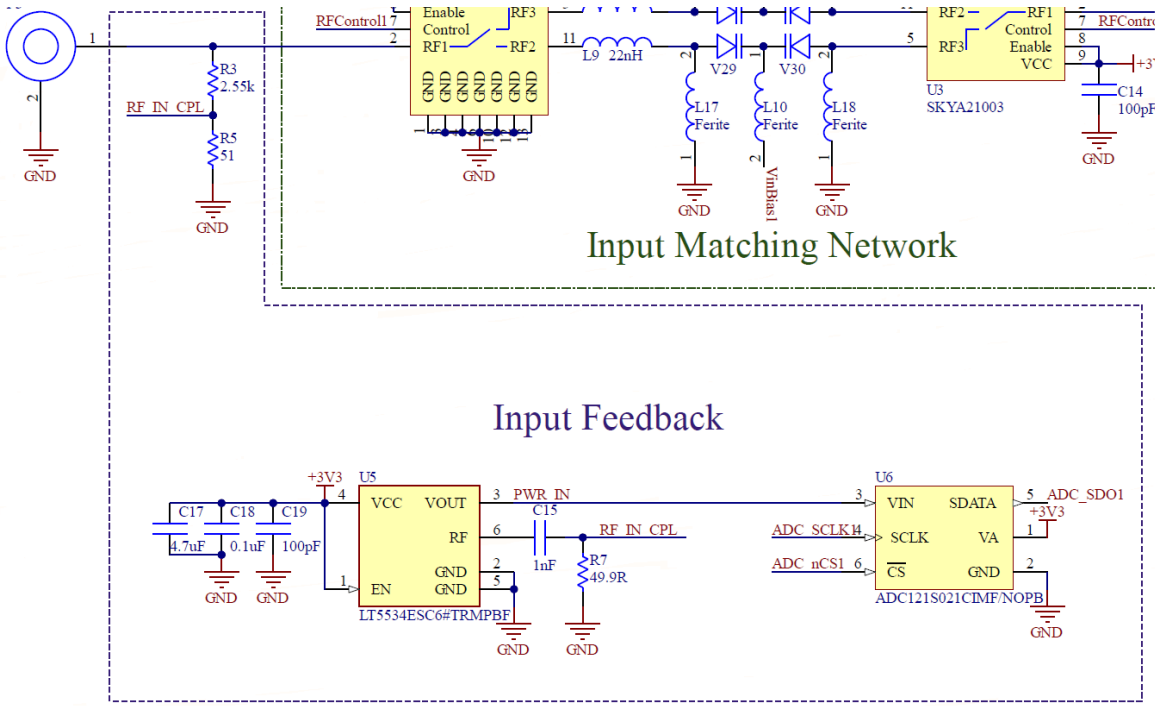


Figure 4.21: Input Feedback Schematic

Figure 4.22 shows the feedback circuit for the output match. The circuit is the same as shown in *Figure 4.21*.

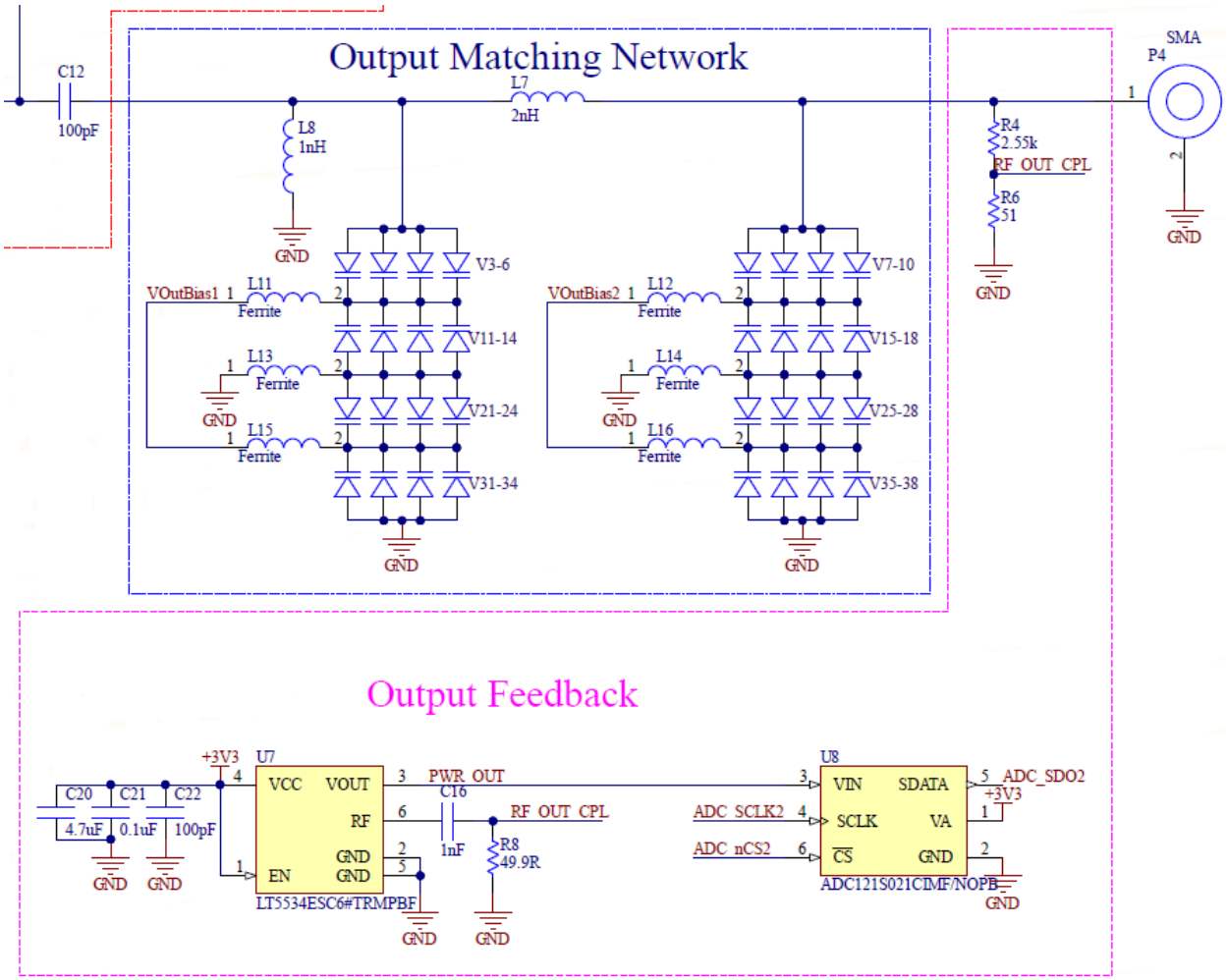


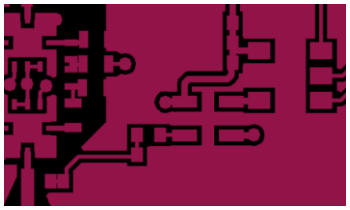
Figure 4.22: Output Feedback Schematic

Table 4.7 contains the collective BOM of the input and output feedback circuits. All parts shown are available from electronic distributors.

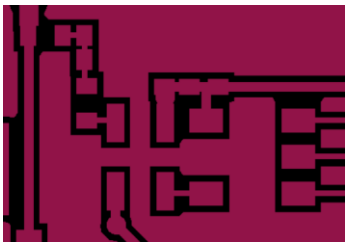
Table 4.7: Sensing BOM

ID	Designator	Comment	Manufacture	Part Number	Qty
1	C18, C21	0.1uF	Murata	GRM155R71C104KA88J	2
2	C19, C22	100pF	KEMET	C0402C101J3GACTU	2
3	C15, C16	1nF	Murata	GRM155R71H102KA01D	2
4	C17, C20	4.7uF	Murata	GRM155R60J475ME47D	2
5	R8	49.9R	Yageo	RC0402FR-0749R9L	1
6	R3, R4	2.55k	Yageo	RC0402JR-071KL	2
7	R5, R6	51	Yageo	RC0402JR-071KL	2
8	U5, U7	Power Detector	Analog Devices	LT5534ESC6#TRMPBF	2
9	U6, U8	ADC	National Semiconductor	ADC121S021CIMF/NOPB	2

Figure 4.23 on page 112 shows the copper layers for the input and output feedback circuits. Along with the copper layers, the image also contains 3D images of the circuits as well. The feedback circuit routes the singles on top and the bottom with ground planes in between.

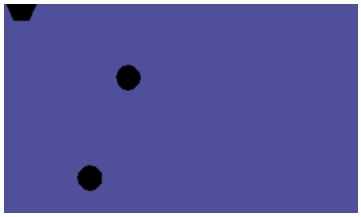


Input Top Layer



Output Top Layer

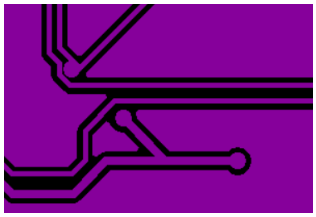
Input Layer 2



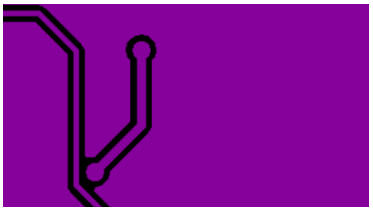
Output Layer 2

Input Layer 3

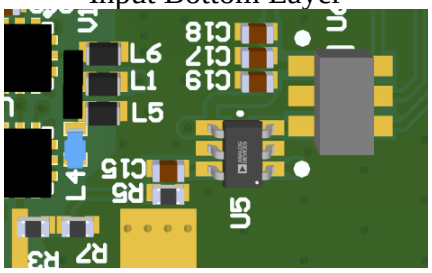
Output Layer 3



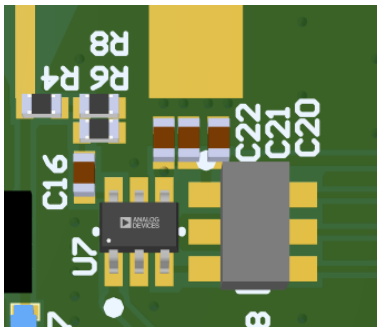
Input Bottom Layer



Output Bottom Layer



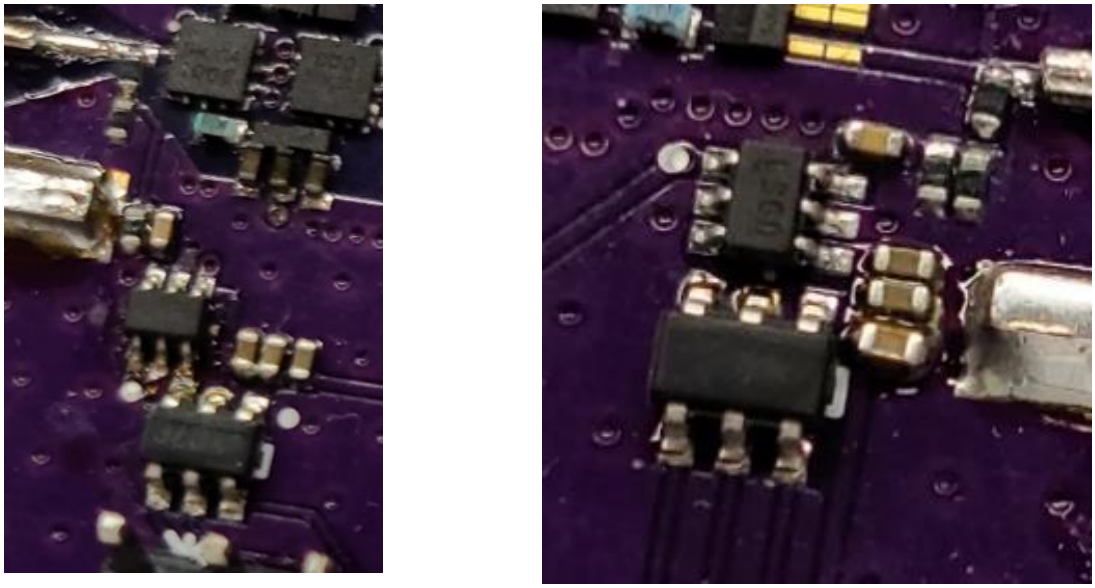
Input 3D Model



Output 3D model

Figure 4.23: Input and Output Sensing Layouts

Figure 4.24 shows the built feedback circuits. The input to each circuit is on the left, and the output is on the right.



Input Output

Figure 4.24: Built Feedback Networks

One thing to note about this design is that it is not directional. Being nondirectional means that the power detectors only show the port's total power (transmitted and reflected), not just the transmitted power. This topology makes it impossible to determine the match quality of each port independently. The input and output together provide a good approximation for the system's overall quality. The overall quality accounts for both the system match as well as amplifier gain.

4.3.2 Sensing Method Test Setup

The physical setup in this section is the same as the matching network test but adds feedback sensing to the input and output, see *Figure 4.25*. To test the sensing method, the VNA outputs a single frequency on port 1. The matching circuit sweeps across the frequency range and records the input and output power. The ideal match is when there is the most considerable difference in input to output power.

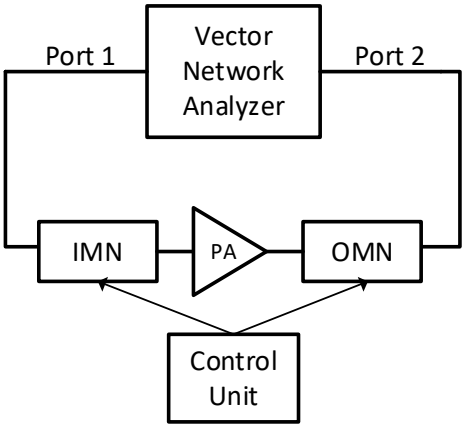


Figure 4.25: Sensing Method Physical Setup

4.3.3 Sensing Method Test Results

The output of the sensing method for a single frequency is in *Figure 4.26*. The graph shows that the matching circuits cannot identify where the best match is independent. Using the measurements together produces a more accurate result where the ideal match occurs at the maximum gain difference.

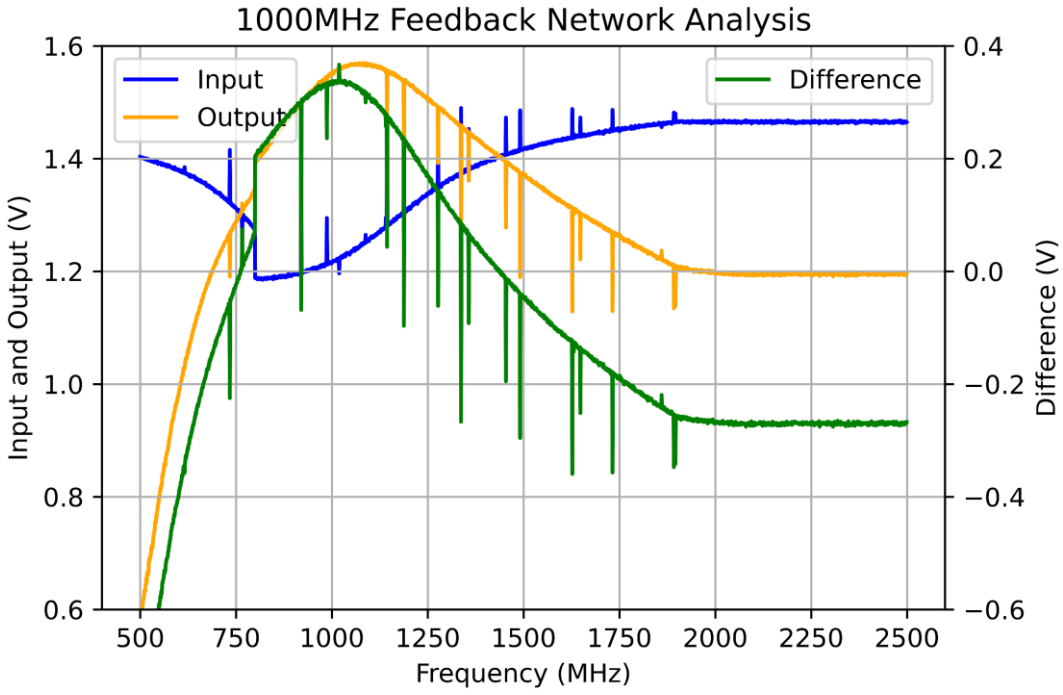


Figure 4.26: Feedback Analysis 1000MHz

4.3.4 Sensing Method Test Summary

The feedback circuit uses broad power and frequency range components to achieve feedback analysis over the desired frequency range. The sensing method is capable of detecting the system match. *Table 4.8* shows the specifications achieved in this system

Table 4.8: Sensing Method Specification Summary

Specification	Requirement	Achieved?
Frequency Range	500-2500	Yes
Power	27-30dBm	Yes

4.4 System Integration

All the previous sections have broken out the different components of the system and tested them. This section shows how all the systems integrate physically to provide context for the remaining sections in this chapter. The full system integrates all the previous subsystems discussed into a single board for testing. The schematic of the board is in *Figure 4.27*. *Figure 4.28* and *Figure 4.29* show the layout and 3D model of the system respectfully. The system as built is in *Figure 4.30*.

The system signal chain is as described. The RF transmission signal comes into the input from a source, in testing the VNA. The input feedback sensor measures the response that the input matching network has on the signal. The input matches the amplifier input, which then the amplifier increases the power of the RF signal. After the amplifier, an output matching circuit matches the amplifier output to the output port. As the RF signal leaves the board, the output feedback sensor detects the output power.

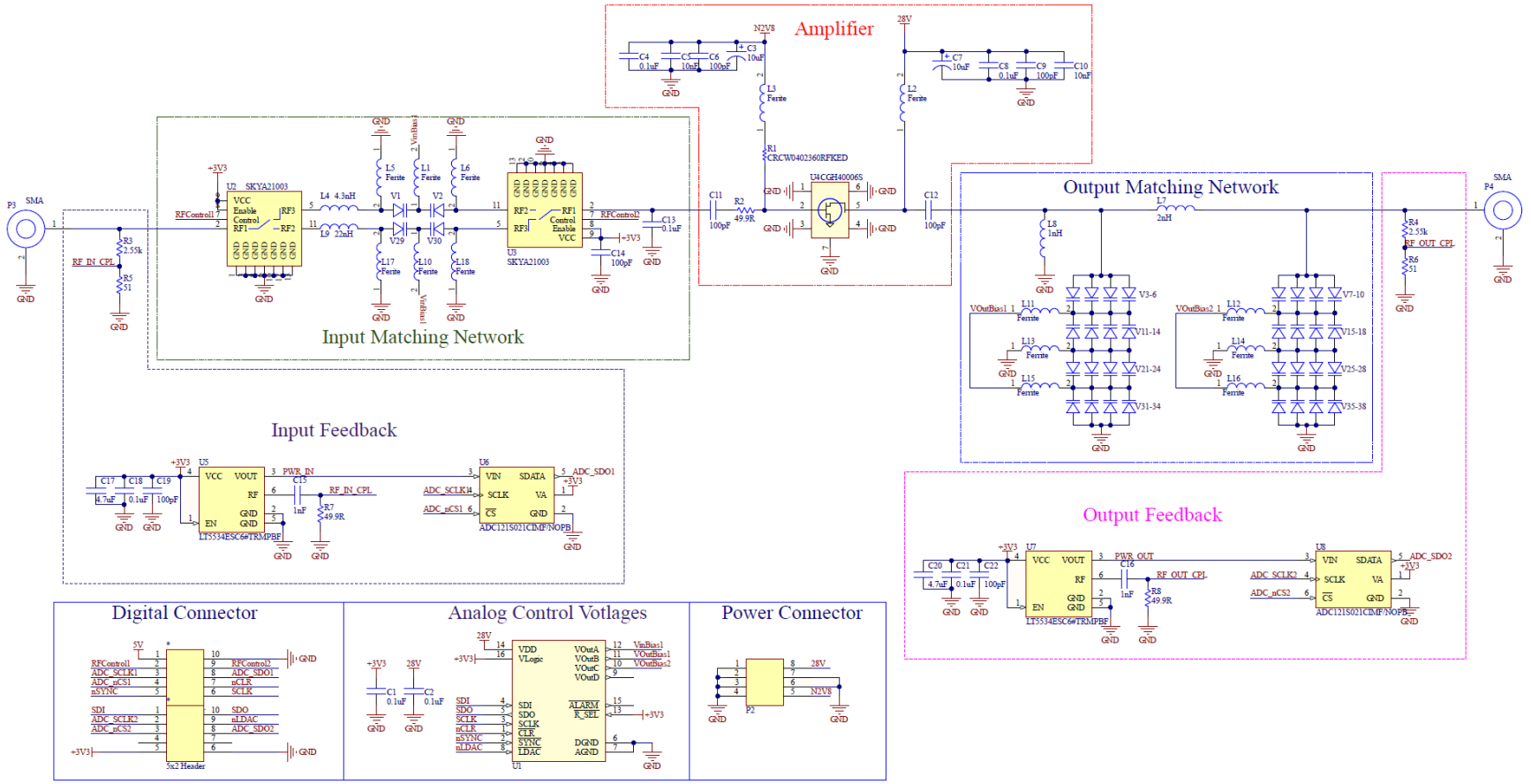


Figure 4.27: System Schematic

Table 4.9 on page 116 contains the BOM for the entire system. All components are available from electronics distributors. Each component contains the manufacturer, part number, and reference designator to purchase and place the parts.

Table 4.9: Complete System BOM

Item	Designator	Comment	MFG	MFGPN	Qty

1		5x2 Header			2
2	C1, C18, C21	0.1uF	Murata	GRM155R71C104KA88J	4
3	C2, C4, C8	0.1uF	Yageo	CC0603ZRY5V9BB104	3
4	C3, C7	10uF	Vishay	293D106X9050E2TE3	2
5	C5, C10	10nF	Samsung	CL10B103KB8NCNC	2
6	C6, C9, C11, C12, C14, C19, C22	100pF	KEMET	C0402C101J3GACTU	7
7	C15, C16	1nF	Murata	GRM155R71H102KA01D	2
8	C17, C20	4.7uF	Murata	GRM155R60J475ME47D	2
9	L1, L2, L3, L5, L6, L10, L11, L12, L13, L14, L15, L16 L17, L18	Ferrite	Coicraft	0402DF-301XJRW	14
10	L4	4.3nH	Coilcraft	0402DC-4N3X_R_	1
11	L7	2nH	Coilcraft	0402DC-1N0X_R_	1
12	L8	1nH	Coilcraft	0402DC-2N0X_R_	1
13	L9	22nH	Coilcraft	0402DC-22NX_R_	1
14	P2	4x2 Header			1
15	P3, P4	SMA			2
16	R1	360R	Vishay Dale	CRCW0402360RFKED	1
17	R2, R7, R8	49.9R	Yageo	RC0402FR-0749R9L	3
18	R3, R4	2.55k	Yageo	RC0402JR-071KL	2
19	R5, R6	51	Yageo	RC0402JR-071KL	2
20	U1	AD5504			1
21	U2, U3	RF Switch	Skyworks	SKYA21003	2
22	U4	HEMT	Cree	CGH40006S	1
23	U5, U7	Power Detector	Analog Devices	LT5534ESC6#TRMPBF	2
24	U6, U8	ADC	National Semiconductor	ADC121S021CIMF/NOPB	2
25	V3, V4, V5, V6, V7, V8, V9, V11, V12, V13, V14, V15, V16, V17, V21, V22, V23, V24, V25, V26, V27, V31, V32, V33, V34, V35, V36, V37	Varactor	Skyworks	SMV1265	30/34

Figure 4.28 shows the copper layers for the entire system. The board utilizes internal ground planes to isolate the RF signals from digital and power signals. The outer layers are used for routing. The input to the system is on the left, while the output is on the right side.

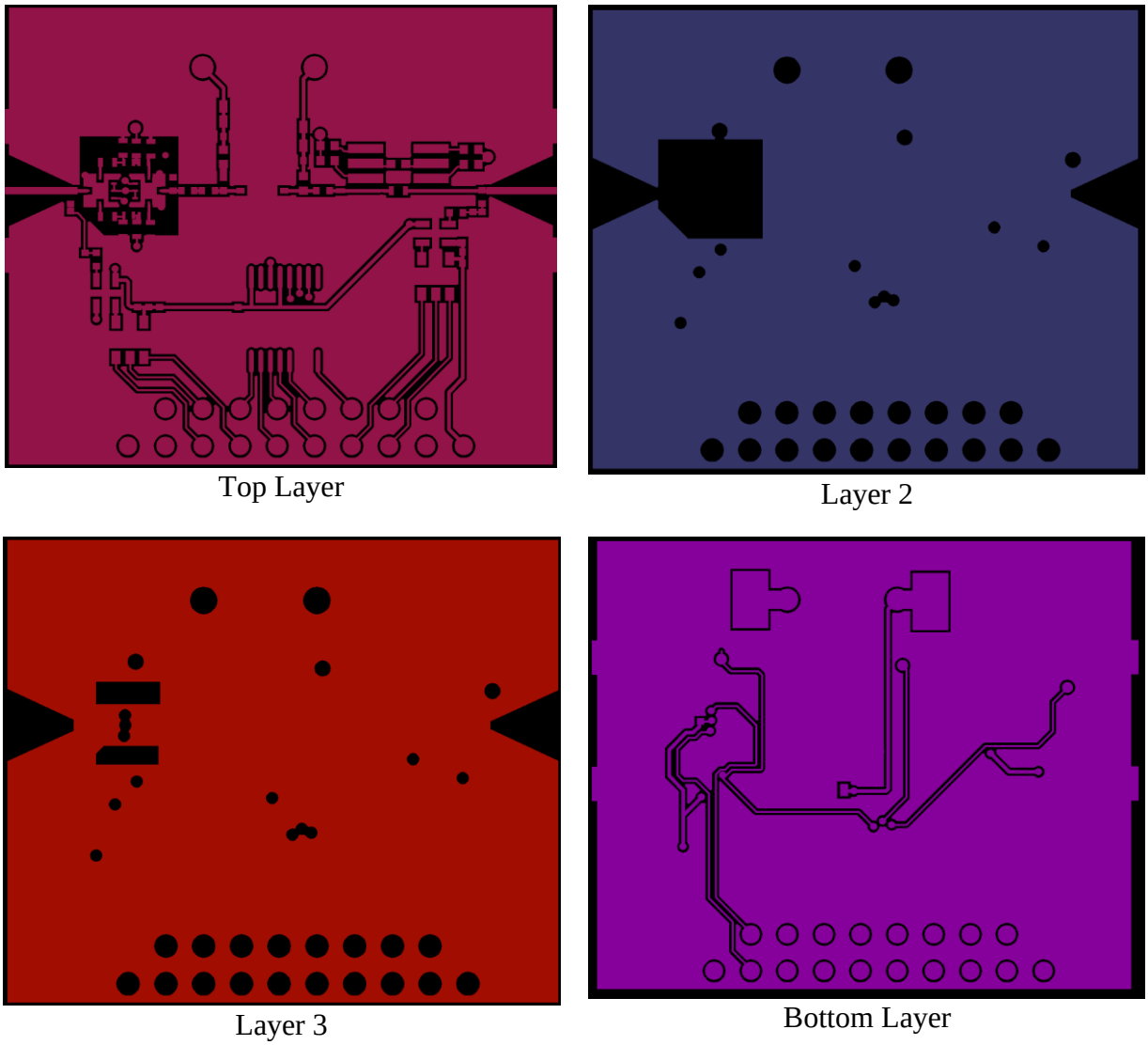


Figure 4.28: System Layout

Figure 4.29 shows the 3D model of the board. The reference designators next to each component correspond to the components in the BOM and on the schematic. The input to the board is on the left, and the output is on the right side.

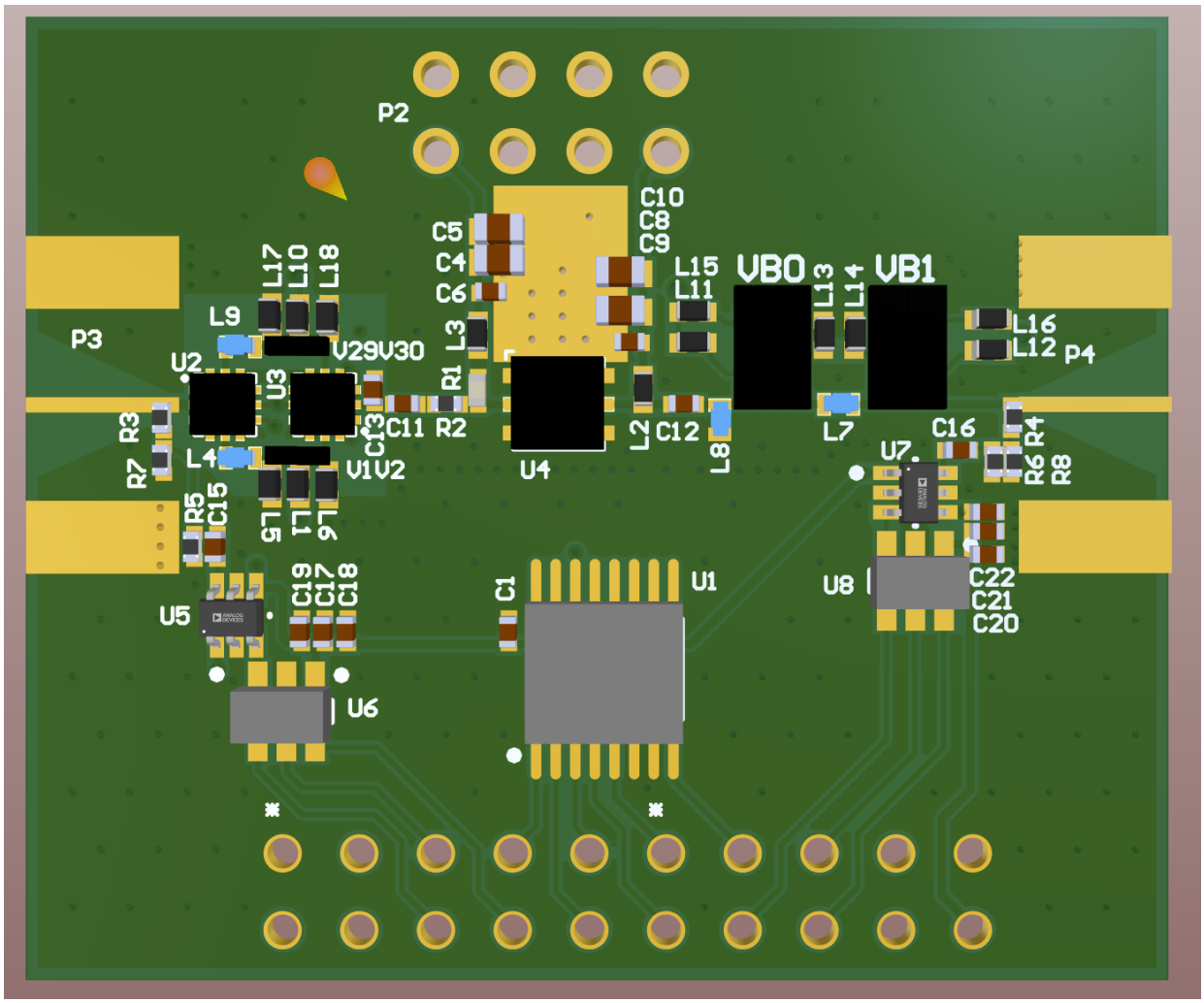


Figure 4.29: System 3D Model

Figure 4.30 contains the image for the completed test setup. Wires at the top of the board are to connect the power lines to the board. Yellow is the gate bias, black is the ground return, and red is the 28V supply. The RF connectors are on the left and right sides of the board are for

input and output. The header at the bottom of the board connects to a DE10-NANO developer kit to control the system.

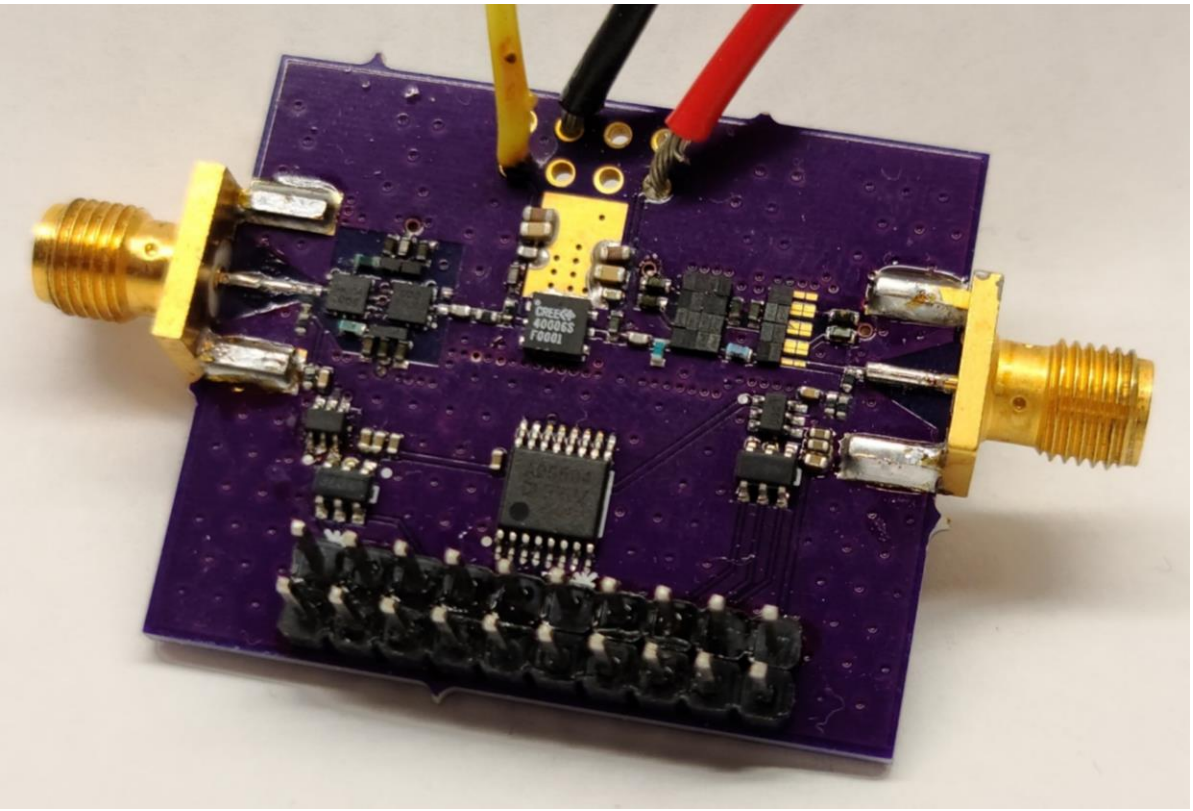


Figure 4.30: Built System

4.5 Control System

The following section uses the results from 4.3 and the circuit board discussed in 4.4 to design and test a control algorithm using the feedback sensors' data to identify an ideal match.

4.5.1 Control System Design

From the previous section, the only data available is the total power at each of the ports that do not show the direct quality of the system match. The lack of data leads to an interesting problem for the control algorithm. The tuning algorithm was precalibrated with fourth-order polynomials for each of the three varactor banks to achieve tuning times and accuracy. When

solving all three polynomials for the same state, an overlapping match at the same frequency is possible.

The implementation of the tuning algorithm is a successive searching method. Searching starts with sending a tuning word with the desired frequency to the controller. A DE10 Nano development board using the Cyclone V FPGA System on Chip (SOC) controls the entire system and implements the tuning algorithm. From here, the controller starts by setting the varactors to predefined states based on the polynomials for a match that is approximately 100MHz lower than desired. Once set, the input and output are measured. If the state provides a better match than currently stored, that state replaces the currently best match state. A better match is the largest difference between the power measured at the system's input and output. The control system then sets the varactors to the next closest frequency based on the polynomials and retakes a measurement. The control system repeats this process until it is approximately 100MHz higher than the desired frequency, where it times out. After the searching algorithm finishes, the state of the best match is recalled and set for the system. Note that during this entire process, a transmitted signal from the VNA is going through the system. A flow chart of the test bench *Figure 4.31* and the control algorithm (*Figure 4.32*) is shown.

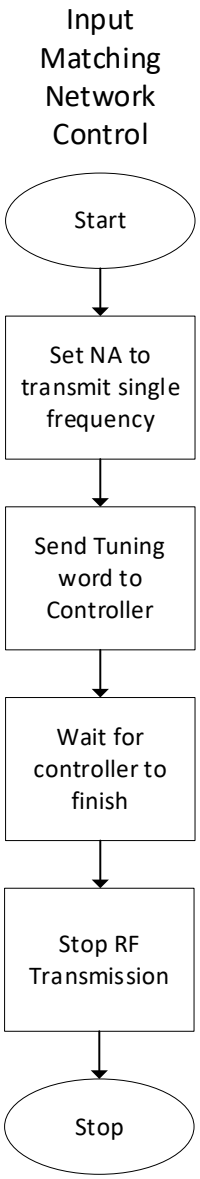


Figure 4.31: Test Bench Flow Chart

Figure 4.32 shows the completed control system flow chart. The logic implementation is system Verilog on an Altera Cyclone V FPGA. The code runs every time after receiving a new tuning word.

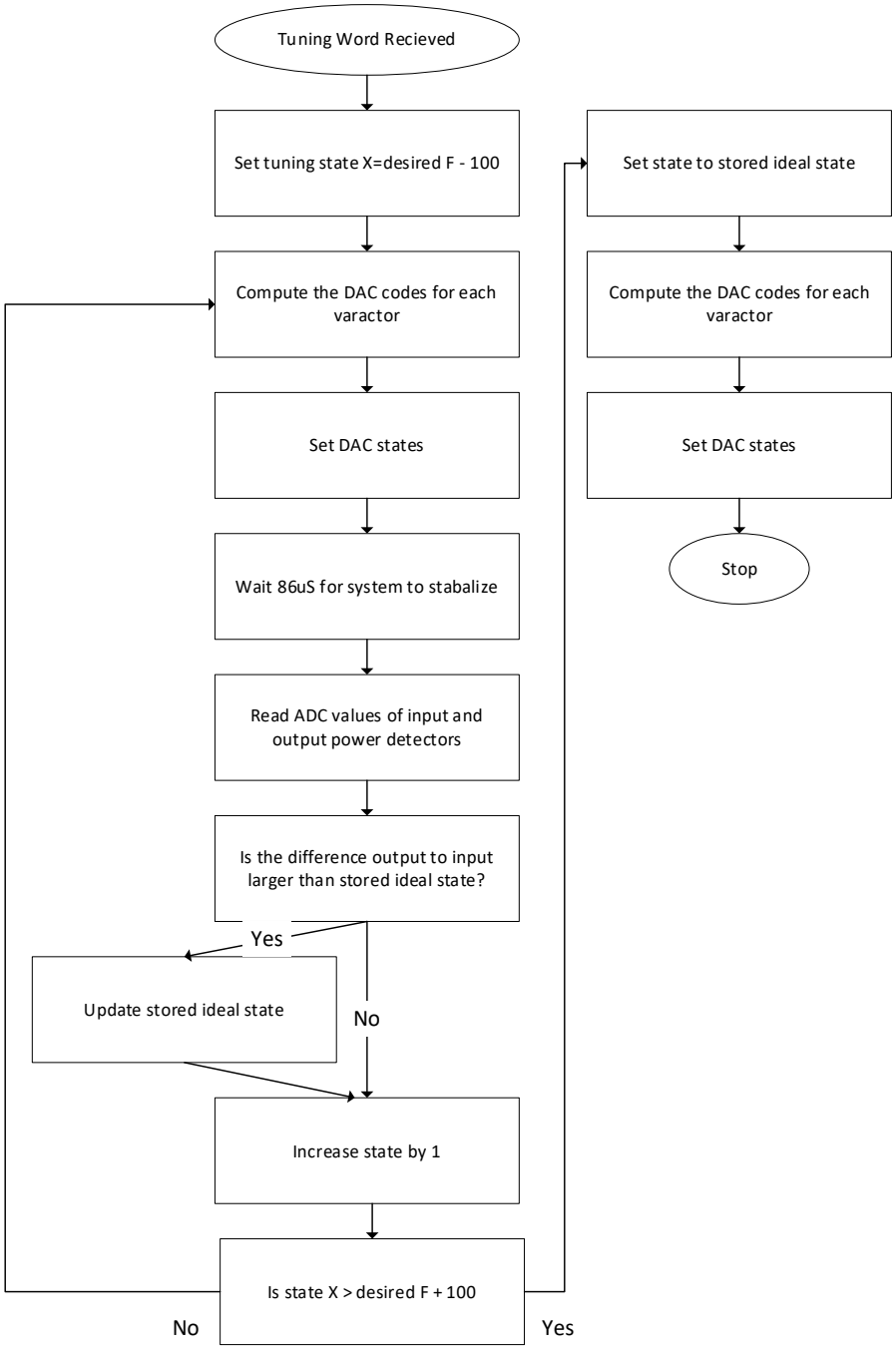


Figure 4.32: Control Algorithm Flow Chart

4.5.2 Control System Test Setup

The control system's test setup is in *Figure 4.33*. To start, the VNA produces a single frequency within the tuning range of the system. A tuning word sent from the PC to the controller starts the tuning process. At the beginning of the tuning process, the control system starts a counter and stops it after completing the system tuning. The counter is the tuning time of the system. After tuning is complete, the VNA reports S11, S22, and S21 at the desired frequency. The VNA also reports the Frequency and S-parameters of the minimum S11 and S22 and the maximum S21. The controller reports the tuning time.

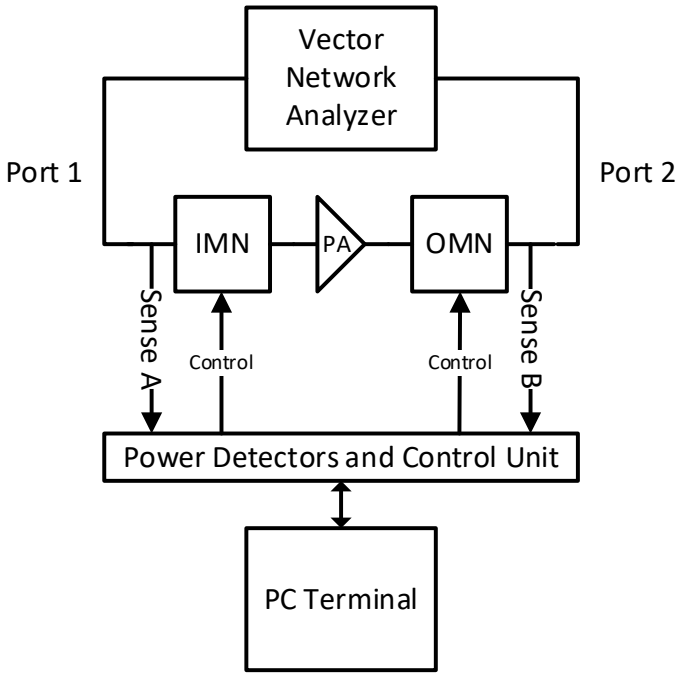


Figure 4.33: Control System Test Setup

4.5.3 Control System Test Results

The test setup uses both the low band and high band matching circuits to verify the control system's frequency range. *Table 4.10* shows the low band controller's test results. Examination of different aspects of S11, S22, and S21 determines the overall system performance. Each S-parameter shows the power at the desired frequency. The frequency of where the minimum for S11 and S22 occurs (F at Min S11/S22) is the frequency of the best

match. Ideally, the frequency of the minimum S11 and S22 are at the same as the desired frequency. Doing so means that the system ports match is optimal for the transmit frequency. Along with the quality of the match, the system consistently found the optimal match in 30.91ms.

Table 4.10: Low Band Controller Results

Frequency	S11	F at Min S11	S22	F at Min S22	S21	Tuning Time (ms)
500	-18.82	507.38	-23.63	505.3	6.68	30.91
600	-22.58	592.92	-46.88	599.68	6.86	30.91
700	-22.77	683.14	-20.74	683.4	6.53	30.91
800	-20.38	810.02	-19.94	822.5	7.33	30.91
900	-19.39	894.52	-35.41	903.36	6.99	30.91
1000	-18.37	998.26	-27.04	1010.74	6.89	30.91
1100	-17.56	1096.8	-30.97	1107.72	6.73	30.91
1200	-16.84	1191.96	-53.38	1200.28	6.53	30.91
1300	-15.44	1208.86	-13.2	1218.48	5.42	30.91
1400	-15.53	1379.42	-28.6	1384.88	6.19	30.91
1500	-14.93	1480.04	-29.01	1483.16	6.1	30.91
1600	-14.38	1579.1	-47.06	1598.08	6.01	30.91
1700	-13.74	1710.14	-27.02	1713.26	5.91	30.91
1800	-13.37	1792.3	-25.17	1804.26	5.67	30.91
1900	-12.94	2375.74	-19.83	1900.46	5.45	30.91
2000	-12.68	2375.74	-16.55	2017.72	5.22	30.91
2100	-12.66	2364.3	-14.65	2073.88	4.89	30.91
2200	-12.92	2361.18	-13.21	2078.56	4.56	30.91

Figure 4.34 shows that the match in dB for S11 and S22 at the desired frequency presents a good match (less than -12dB) across a significant portion of the tuning range. The found frequency error plot is in *Figure 4.35*. The plot shows the error of the minimum S11 and S22 frequencies compared to the ideal matched frequency. The found best match frequency shows that most of the spectrum is within 5% of the desired frequency.

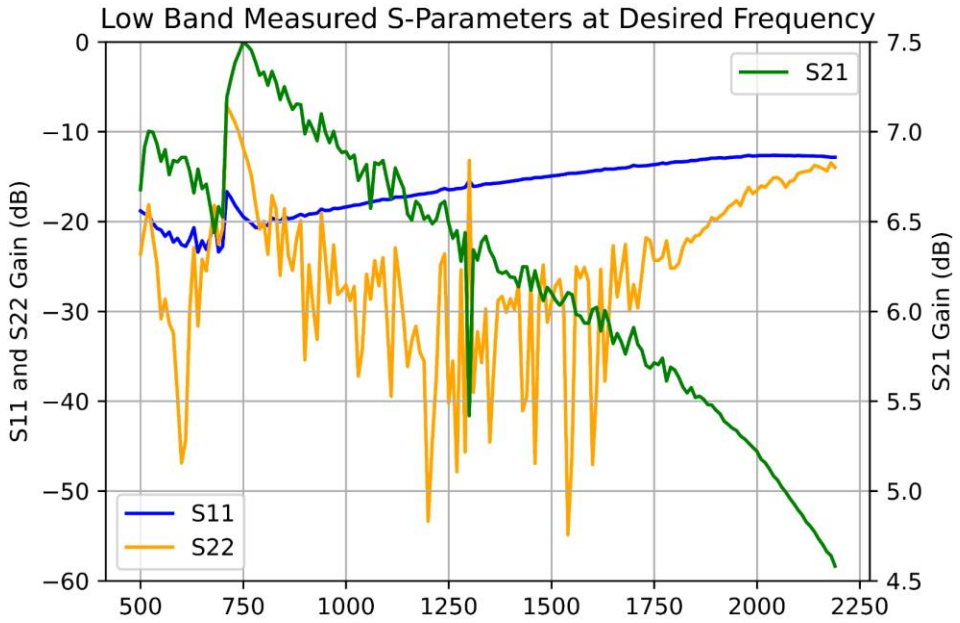


Figure 4.34: Low Band Measured S-parameters at Desired Frequency

Figure 4.35 shows the error of the system. The error is a comparison of desired frequency minimum to the frequency of the absolute minimum. The more significant errors seen are discussed further on.

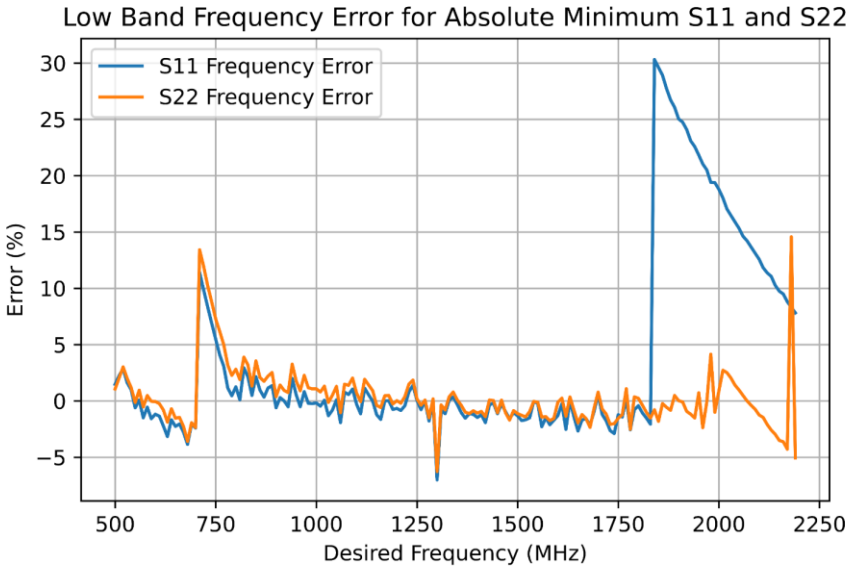


Figure 4.35: Low Band Frequency Error for Absolute Minimum S11 and S22

As discussed and shown, the system provides good matched results for much of the spectrum and has good frequency selectivity, within 5%. The following discussion looks at the causes of the larger errors. These are at frequencies at 800MHz and 1800MHz.

At 800MHz, the input switches which tunable element is in use, resulting in a jump in gain and causing the error in tuned frequency seen in *Figure 4.35*. Though the system can produce a better match at 700MHz, the system determines that the extra gain produced by a match at 800MHz for a 700MHz transmit wave yields a more optimal system setup. *Figure 4.36* shows the S-parameters at the cross-over point.

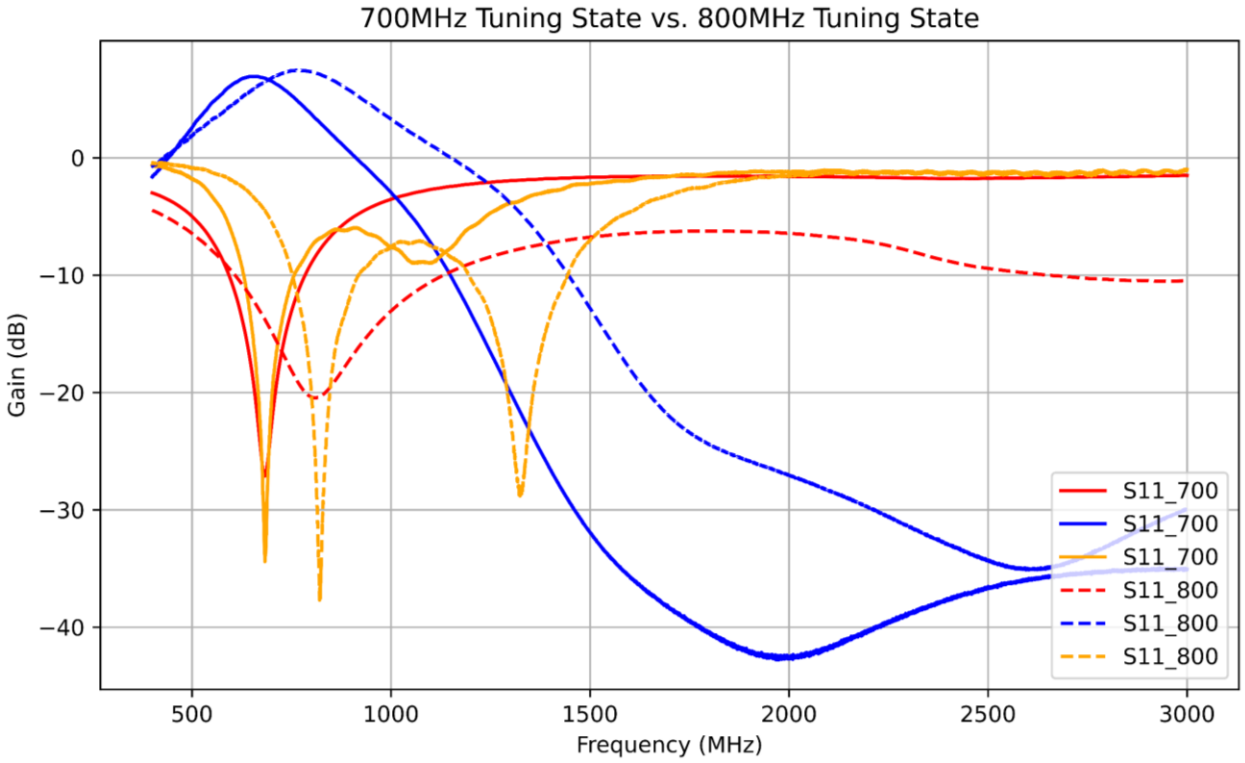


Figure 4.36: 700MHz vs. 800MHz Tuning State

At the upper end of the band, the input and output match is significantly broader, meaning the match's frequency selectivity decreases. The reduced ideal match then leads to false minimums at the high-frequency range. *Figure 4.37* shows that the S11 tuning state of 1800MHz is the minimum, but at 1900MHz, an upper mode takes over, giving a false reading at 2300MHz. This same issue is present in S22, as shown in *Figure 4.38*. The error of the S11 and S22 upper-frequency range is considered minimal because of the tuning state selectivity.

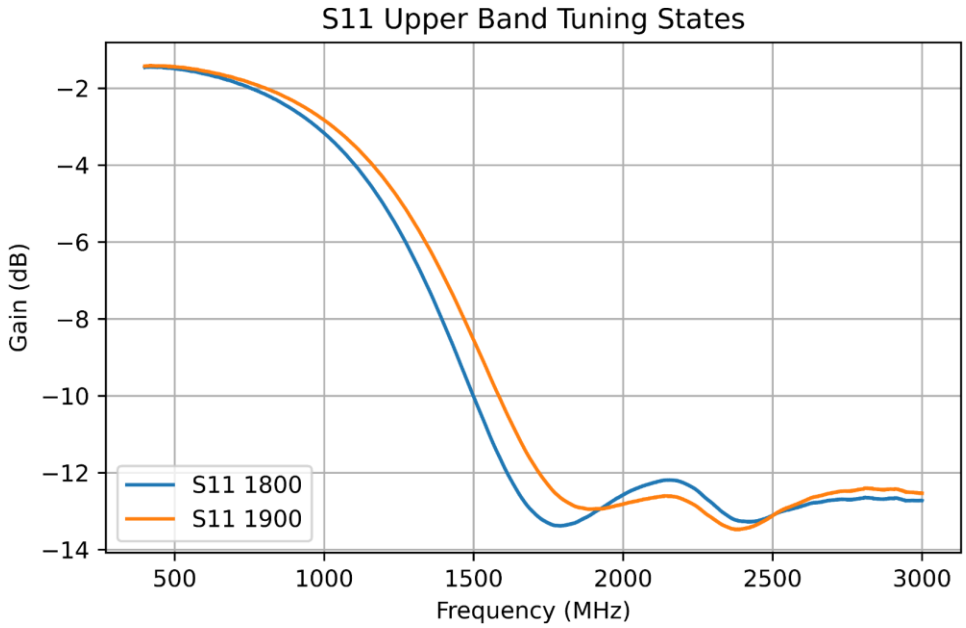


Figure 4.37: S11 Upper Band Tuning States

Figure 4.38 shows the S22 measurement of the upper band tuning states at 2100MHz and 2200MHz. Note that from the graph, the minimum at the desired frequency is acceptable at -15dB; however, the absolute minimum occurs at 3000MHz.

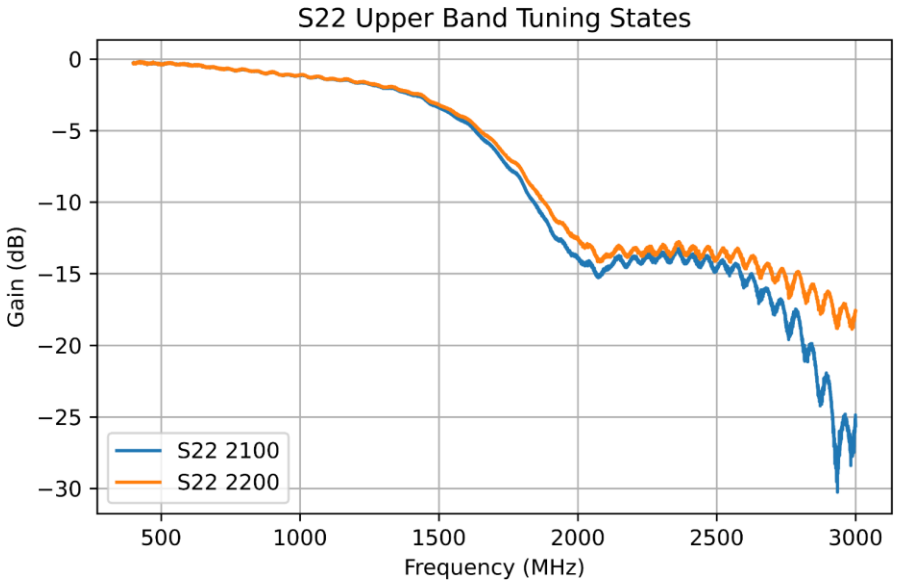


Figure 4.38: S22 Upper Band Tuning States

Table 4.11 shows the test results of the upper band matching network configuration. From the table, the S-parameters and frequency accuracy are acceptable. The tuning time to achieve a match for the upper band configuration is again 30.91ms. The system's S-parameters at each desired frequency in *Figure 4.39* indicate a good match over the entire tuning range. *Figure 4.40* shows that the frequency error of the S-parameters is minimal across the entire spectrum.

Table 4.11: High Band Controller Test Results

Frequency	S11	F at Min S11	S22	F at Min S22	S21	Tuning Time (ms)
800	-20.68	829.78	-15.95	837.58	7.64	30.91
900	-20.22	925.2	-18.94	924.16	7.62	30.91
1000	-19.07	1034.66	-17.43	1648	7.6	30.91
1100	-19.17	1089.52	-28.08	1086.66	7.17	30.91
1200	-18.46	1191.96	-28.91	1184.94	7.06	30.91
1300	-17.62	1311.82	-42.15	1299.6	7.08	30.91
1400	-17.04	1407.5	-30.01	1391.64	6.93	30.91
1500	-16.44	1506.56	-27.19	1480.56	6.82	30.91
1600	-15.73	1612.64	-38.66	1602.76	6.79	30.91
1700	-15.24	1710.14	-46.69	1697.66	6.62	30.91
1800	-14.68	1799.84	-34.16	1807.9	6.46	30.91
1900	-14.2	1928.02	-20.02	2010.18	6.33	30.91
2000	-14.12	1928.02	-27.05	2054.9	6.07	30.91
2100	-13.93	1930.62	-24.96	2178.14	5.82	30.91
2200	-13.82	1934.26	-23.26	2305.28	5.49	30.91
2300	-14.1	1939.98	-23.88	2410.32	5.04	30.91
2400	-14.15	1942.32	-25.3	2963.86	4.66	30.91
2500	-13.48	1942.32	-28.45	2918.62	4.37	30.91

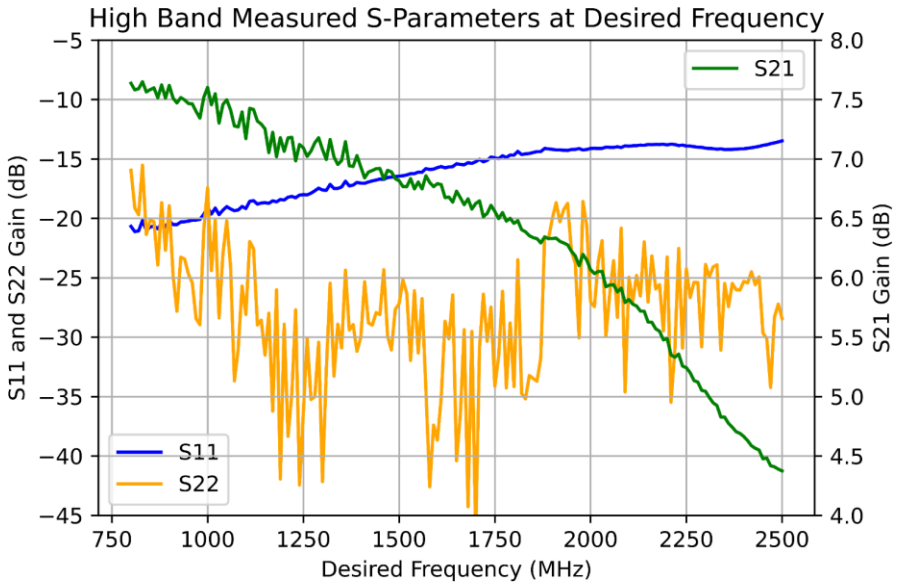


Figure 4.39: High Band Measured S-parameters at Desired Frequency

Figure 4.40 shows the error for the high band minimum frequency. From the graph, there is an error at 1000MHz that is discussed further on. The error at the upper-frequency range is due to the same error as the low band system at the upper range.

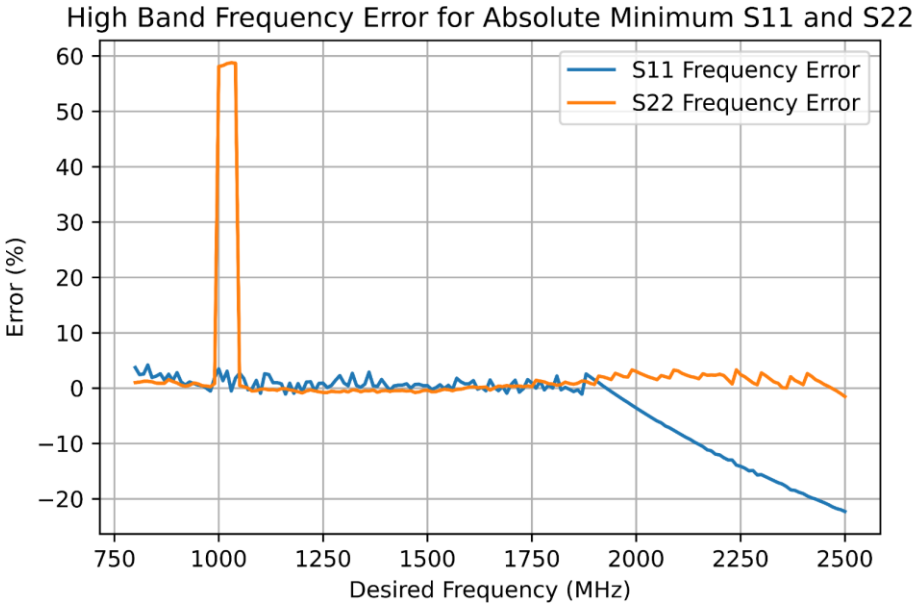


Figure 4.40: High Band Frequency Error for Absolute Minimum S11 and S22

The error at 1000MHz seen in *Figure 4.40* is due to an upper-frequency mode. The mode produces a lower minimum than that of the desired frequency, as shown in *Figure 4.41*. The match at the desired frequency is still acceptable, minimizing the error seen at 1000MHz. The same selectivity issue with the input matching circuit present in the low band configuration causes the error at the upper-frequency range for S11.

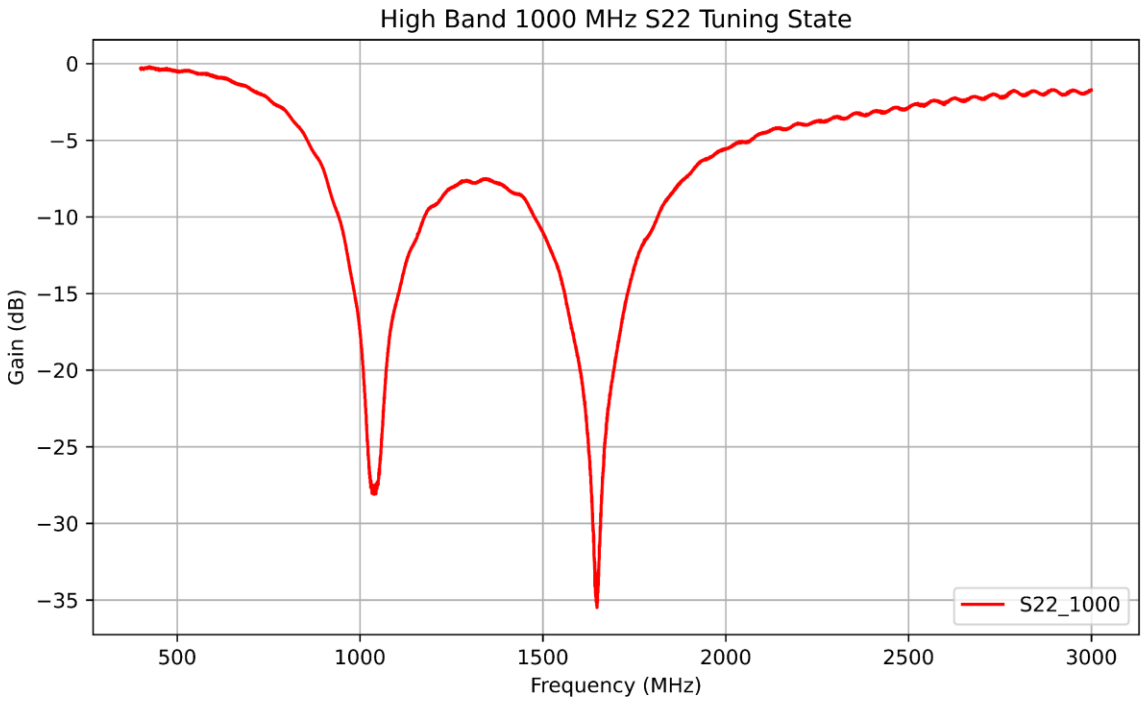


Figure 4.41: High Band 1000MHz S22 Tuning State

4.5.4 Control System Test Results Summary

The control system provides accurate feedback control of the matching networks. Typical frequency error is +/-5% across the entire frequency range, depending on the matching network's selectivity. Tuning time is a consistent 30.91ms regardless of configuration or frequency.

Table 4.12: Control System Specification Summary

Specification	Requirement	Achieved?
Frequency Range	500-2500	Yes
Tuning Time	Less than 100ms	Yes

4.6 System Power Added Efficiency

This section discusses the amplifier's power added-efficiency results using the integrated system from 4.4 and the control algorithm in 4.5.

4.6.1 Power Added Efficiency Test Setup

Port 1 of the VNA connects to the input, while port 2 connects to the system's output. The VNA provides a single frequency from port 1 to the input of the matching network. A tuning word from the PC tells the system the desired matched frequency. Following the control algorithm, the system identifies the optimal match. After locating the optimal match, the PC records the power on the DC supply. Once complete, the VNA performs a full spectrum sweep to collect the S-parameter. The test setup is in *Figure 4.42*. A flow chart of the above-described testing procedures is in *Figure 4.43*.

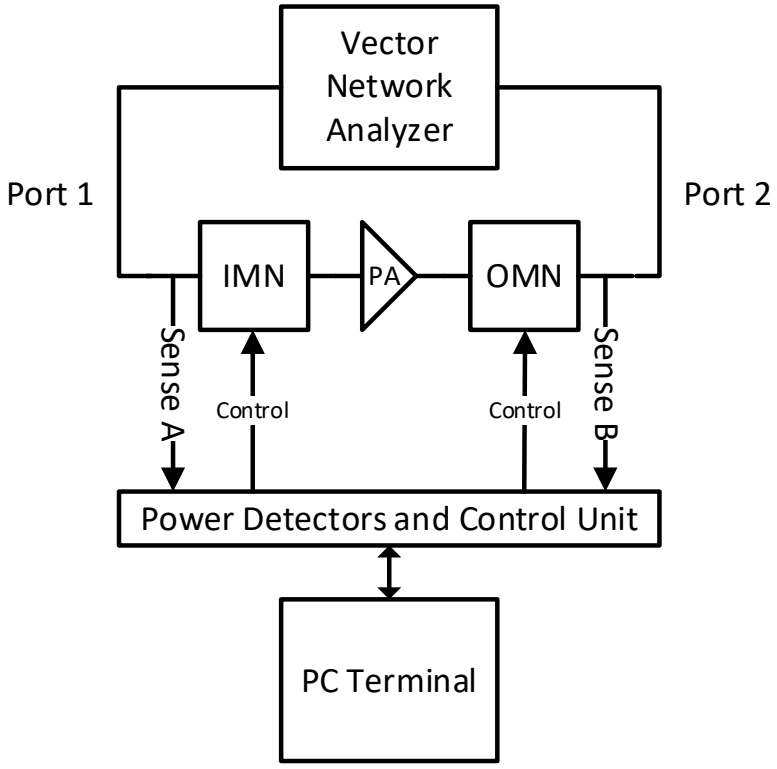


Figure 4.42: Power Added Efficiency Test Setup

Figure 4.43 contains the flow chart for how the data is collected for power-added efficiency. The process is linear, and each step must be completed before moving onto the next step.

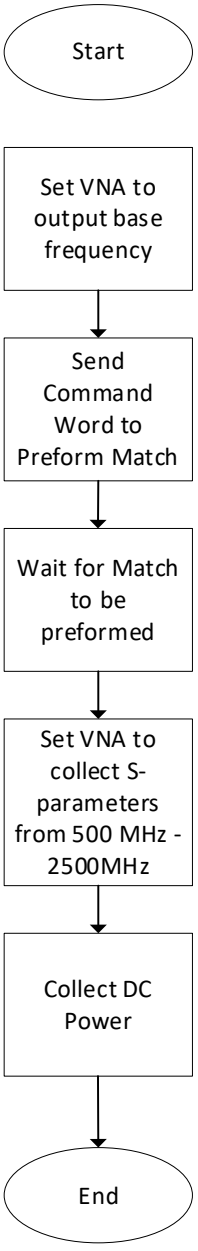


Figure 4.43: Power Added Efficiency Testing Procedures

4.6.2 Power Added Efficiency Test Results

Table 4.13, *Table 4.14*, and *Table 4.15* record the power added efficiency values for the system. The comparison of the power added efficiencies is in *Figure 4.44*. Due to the improperly matched amplifier, either system's power added efficiency did not outperform the unmatched system. The data shows that the amplifier's power added efficiency improves when presented with a better match. In this case, the unmatched circuit presented a better match to the amplifier than the matching circuits leading to significantly higher power-added efficiencies than the system.

Table 4.13: Unmatched Amplifier PAE

Frequency (MHz)	S11 (dB)	S22 (dB)	RF Input Power (dBm)	RF Output Power (dBm)	DC Power (dBm)	Gain (dB)	PAE (%)
500	-8.21	-11.05	8	27.86	34.47	19.86	21.57
600	-10.41	-11.7	8	26.75	34.47	18.75	16.66
700	-12.69	-12.09	8	25.69	34.47	17.69	13.03
800	-15.09	-12.54	8	24.74	34.47	16.74	10.42
900	-17.81	-12.67	8	23.87	34.47	15.87	8.48
1000	-21.12	-12.84	8	23.05	34.47	15.05	6.98
1100	-25.4	-12.73	8	22.29	34.47	14.29	5.83
1200	-32.08	-12.65	8	21.56	34.47	13.56	4.89
1300	-36.35	-12.45	8	20.89	34.47	12.89	4.16
1400	-29.18	-12.21	8	20.26	34.47	12.26	3.57
1500	-25.06	-11.85	8	19.66	34.47	11.66	3.08
1600	-22.38	-11.42	8	19.09	34.47	11.09	2.67
1700	-20.5	-11.04	8	18.58	34.47	10.58	2.35
1800	-19.06	-10.68	8	18.07	34.47	10.07	2.06
1900	-17.95	-10.18	8	17.61	34.47	9.61	1.83
2000	-17.02	-9.84	8	17.14	34.47	9.14	1.62
2100	-16.25	-9.55	8	16.7	34.47	8.7	1.45
2200	-15.52	-9.34	8	16.38	34.47	8.38	1.33
2300	-14.92	-9.06	8	15.97	34.47	7.97	1.19
2400	-14.42	-8.84	8	15.59	34.47	7.59	1.07
2500	-13.97	-8.82	8	15.21	34.47	7.21	0.96

Table 4.14 contains the collected data for the power added efficiency of the low band configuration. The table shows that the S11 and S22 measurements present good matches, but the system presents low gain leading to low PAE.

Table 4.14: Full System Low Band Configuration PAE

Frequency (MHz)	S11 (dB)	S22 (dB)	RF Input Power (dBm)	RF Output Power (dBm)	DC Power (dBm)	Gain (dB)	PAE (%)
500	-18.85	-23.79	8	14.73	34.47	6.73	0.83
600	-23.36	-29.26	8	14.95	34.47	6.95	0.89
700	-27.48	-29.86	8	14.77	34.47	6.77	0.85
800	-20.66	-31.66	8	15.21	34.47	7.21	0.96
900	-19.38	-32.34	8	15.02	34.47	7.02	0.91
1000	-18.41	-34.77	8	14.82	34.47	6.82	0.86
1100	-17.61	-39.78	8	14.63	34.47	6.63	0.81
1200	-16.85	-38.22	8	14.5	34.47	6.5	0.78
1300	-16.13	-42.15	8	14.41	34.47	6.41	0.76
1400	-15.41	-30.74	8	14.34	34.47	6.34	0.75
1500	-14.77	-27.99	8	14.25	34.47	6.25	0.72
1600	-14.23	-25.07	8	14.09	34.47	6.09	0.69
1700	-13.77	-28.98	8	13.9	34.47	5.9	0.65
1800	-13.37	-25.08	8	13.67	34.47	5.67	0.61
1900	-13.01	-20.18	8	13.43	34.47	5.43	0.56
2000	-12.77	-17.13	8	13.2	34.47	5.2	0.52
2100	-12.71	-15.17	8	12.88	34.47	4.88	0.47
2200	-12.88	-13.77	8	12.54	34.47	4.54	0.42

Table 4.15 on page 136 shows the PAE measurements for the high band configuration. The results in the table are similar to those in *Table 4.14*. The system has good matches but the low gain reduces the PAE.

Table 4.15: Full System High Band Configuration PAE

Frequency (MHz)	S11 (dB)	S22 (dB)	RF Input Power (dBm)	RF Output Power (dBm)	DC Power (dBm)	Gain (dB)	PAE (%)
800	-21.87	-28.16	8	15.43	34.47	7.43	1.02
900	-20.76	-28.05	8	15.47	34.47	7.47	1.03
1000	-19.92	-29.38	8	15.35	34.47	7.35	1
1100	-19.07	-29.19	8	15.22	34.47	7.22	0.96
1200	-18.41	-31.21	8	15.09	34.47	7.09	0.93
1300	-17.7	-32.71	8	15.02	34.47	7.02	0.91
1400	-17.05	-30.45	8	14.94	34.47	6.94	0.89
1500	-16.37	-32.75	8	14.88	34.47	6.88	0.87
1600	-15.76	-42.23	8	14.79	34.47	6.79	0.85
1700	-15.18	-40.24	8	14.64	34.47	6.64	0.81
1800	-14.66	-29.82	8	14.48	34.47	6.48	0.78
1900	-14.1	-29	8	14.25	34.47	6.25	0.72
2000	-14.12	-26.31	8	14.07	34.47	6.07	0.69
2100	-13.89	-29.44	8	13.78	34.47	5.78	0.63
2200	-13.77	-29.49	8	13.43	34.47	5.43	0.56
2300	-14.04	-34.25	8	12.98	34.47	4.98	0.48
2400	-14.11	-31.22	8	12.62	34.47	4.62	0.43
2500	-13.48	-28.3	8	12.37	34.47	4.37	0.39

Figure 4.44 contains the PAE measurements for the unmatched and matched configurations. From the image, it can be seen that the PAE at low frequencies is much worse, but the systems converge at the upper-frequency range.

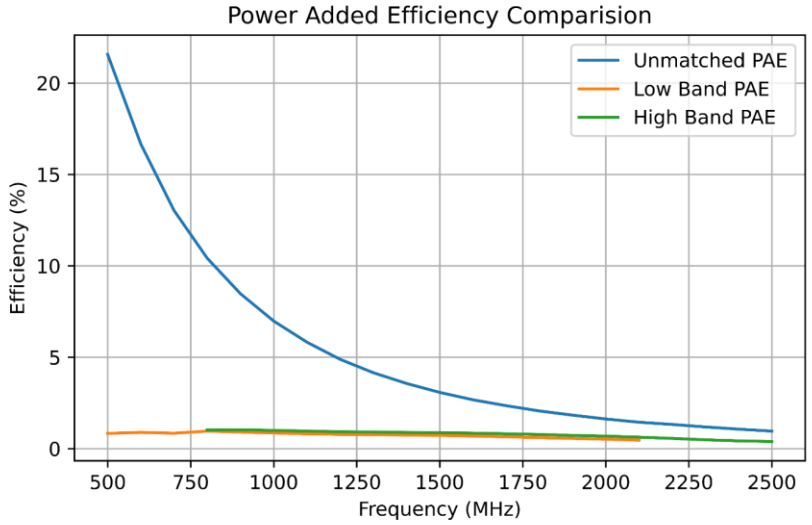


Figure 4.44: Power Added Efficiency Comparison

4.6.3 Power Added Efficiency Test Results Summary

The completed system did not meet the specification of improving power added efficiency over an unmatched amplifier. The failure to improve the system PAE is due to the improper design of the matching circuits. *Table 4.16* shows the summary of the complete system performance compared to specification.

Table 4.16: Power Added Efficiency Test Results

Specification	Requirement	Achieved?
Power Added Efficiency	Matched > Unmatched	No

4.7 Complete System Summary

This section summarizes the completed system performance results, including S-parameter response, tuning time, and power-added efficiency. Section 4.4 discusses the assembly and fabrication of the full systems circuit board. The results in section 3.6 show that the tuning range is close to the desired tuning range (500-2200MHz or 800-2500MHz) compared to the 500-2500MHz required. Section 4.3 proves that the system performance is detectable and that the algorithm presented in 4.5 performs a correction in 30.91ms. The measured tuning time is well within the required tuning times of 100ms. Though the power-added efficiency presented in 4.6 did not perform better than the unmatched amplifier in 3.5, this was due to a low gain issue addressed in the matching circuit design.

Figure 4.45 on page 138 shows the low band systems minimum, maximum, 1000MHz, and 1500MHz frequency responses to see how the system has responded after tuning.

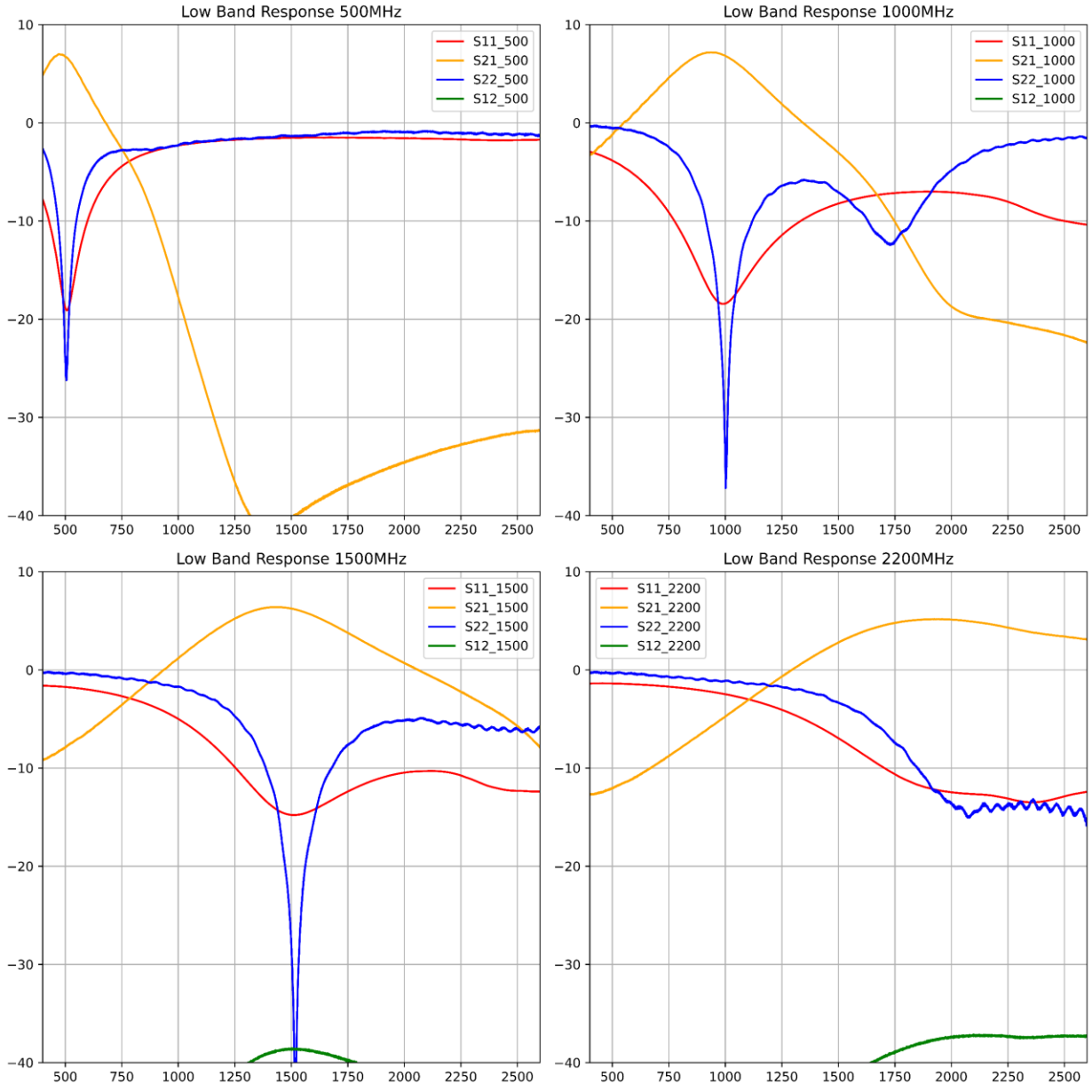


Figure 4.45: Low Band Frequency Responses

Figure 4.46 shows the response for the high bands minimum, maximum, 1500MHz, and 2000MHz tuning states. The figures show that the system matches produced in each response (S11 and S22) are acceptable. One can see that the tuning accuracy is close to the desired frequency, i.e., the minimum point for S11 and S22 is at the desired frequency. The tuning range is close to the required tuning range. The graphs also show the system gain (S21) is low.

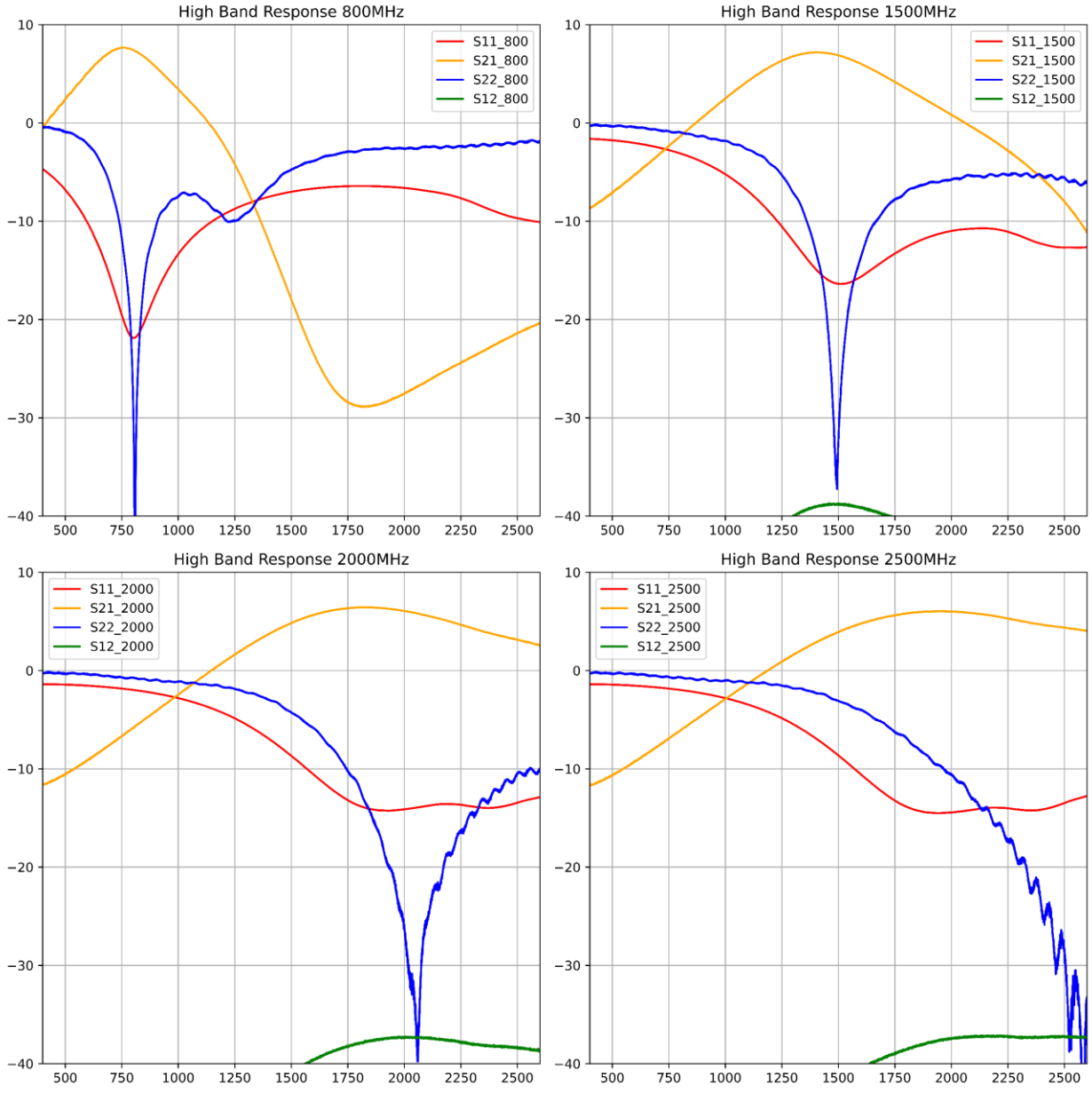


Figure 4.46: High Band Frequency Responses

Table 4.17 shows each subsystem, the specification test, the requirement, and the requirement's achievement. From the table, one can see that most of the requirements were met with the proposed sub-systems.

Table 4.17: Summary of Subsystem Results

Subsystem	Specification	Requirement	Achieved?
Amplifier	Frequency Range	500-2500 MHz	Yes
Amplifier	Power	27-30dBm	Yes
Amplifier	Classification	Linear	Yes
Input Match	Frequency Range	500-2500	No
Input Match	Power	7-10dBm	Yes
Output Match	Frequency Range	500-2500	No
Output Match	Power	27-30dBm	No
Sensing	Frequency Range	500-2500	Yes
Sensing	Power	27-30dBm	Yes
Control Algorithm	Frequency Range	500-2500	Yes
Control Algorithm	Tuning Time	Less than 100ms	Yes

The total system performance is in *Table 4.18*. For specific test results, please refer to the previous sections mentioned.

Table 4.18: Summary of System Results

Specification	Requirement	Measured	Requirement Met?
Frequency Range	500-2500MHz	500-2200 MHz or 700-2500MHz	No
System Power	27-30dBm	12-15.5dBm	No
Tuning Time	< 100 ms	30.91 ms	Yes
PAE	Matched > Unmatched	Less than 1%	No
Amp Classification	Linear	NA	Yes

4.8 Assumptions, Limitations, Delimitations

4.8.1 Assumptions

- The source impedance into the system and load impedance out of the system are 50Ω with no reactive elements.
- All circuits are designed based on the characteristics of standard FR4 printed circuit board substrates and following common RF design practices for proper manufacturing.
- The resistive taps used will assume to be linear and reactance-free.
- All signals going to and from the device under test are calibrated accurately across the entire frequency range and provide constant power at all frequencies.

4.8.2 Delimitations

- The design is limited to the designed amplifier.
- There is no consideration for the effects of phase shift in this study
- There is no examination of the processor design complexity regarding the tuning algorithm.
- All circuit boards are fabricated on FR4 with a standard thickness of 63 mils finished.
    - There is no consideration for different circuit board substrates
- The board stack up is limited to the two and four-layer process at Oshpark
- There is only one design for the matching networks.

4.8.3 Limitations

- The design only focuses on a single amplifier part and classification
- There is only one implementation for the matching circuitry.
- There was no independent testing of each sub-system.

4.9 Summary

Chapter four has discussed the designs and results to create a tunable wideband matching networks with feedback control for a power amplifier. The prototype did function appropriately. The matching networks were adjusted to maximize gain at selected frequencies. Initial matching network design errors compromised meeting some of the specifications. Corrections in future iterations should compensate for these. Chapter four concludes that it is possible to design and build tunable matching circuits for an amplifier and control them using feedback from the signal response.

CHAPTER 5. SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

The following chapter summarizes the conclusions made from the work and provides recommendations for future improvement.

5.1 Summary of Work Completed

The research conducted in this work, designed and implemented a tunable matching circuit with feedback control for use with a power amplifier. Conjugately matching an amplifier at the transmit frequency produces higher gain and power-added efficiency. By creating a tunable matching circuit, the amplifier operation can increase across a wider frequency range and provides better system performance.

The designed system consisted of an amplifier, tunable matching networks, power sensing feedback, and a control system to provide closed-loop operation. The amplifier, feedback, and control system were all capable of meeting the desired power, frequency, and tuning times. Using high order polynomials for the varactors that corresponded to the desired match frequency allowed the system to be pseudo-calibrated without requiring each tuning state to be saved independently.

Challenges arose during the matching circuit design that caused the system to miss the tuning range specification. The input design had unaccounted parasitics and thus did not allow for proper matching at frequencies over 2200MHz but could tune from 500MHz up to 2200MHz. The output matching circuit had a flaw that caused it to be absorptive and thus provided a false ideal match. The mismatch caused the system to have a low gain but still provided tuning at the desired frequencies, measurable by the feedback system. Varactors used in the output match also did not produce enough tuning range to meet the required frequency specification. However, a significant portion of the output tuning range 500-2200 or 800-2500 is still achievable with the current varactors dependent on configuration.

Even with an improperly designed match, the concept of a feedback-controlled tunable matching circuit for an amplifier proved attainable. The control system can find optimal matches within the time allotted with minimal power information.

5.2 Recommendations for Improvement

For future improvements, the first investigation area would be to redesign the amplifier to yield a more flat gain response across the frequency range. Currently, the amplifier gain at the low-frequency end is almost 10dB larger than the gain at higher frequencies.

The next step would be to redesign the input and output matching circuit to provide conjugate matches to the amplifier. The input match needs re-evaluation to remove the inline switches and change with the amplifier's redesign. The output needs a complete redesign. A static L network on the output proved that the amplifier achieves maximum gain and power transfer when conjugately matched at a single frequency providing a good starting point.

Looking at the current system's layout and interactions to determine why a matching circuit using only reactive components absorbs the RF test signal would prove beneficial. The components alone are not absorbing the signal. It is more likely that destructive interference from the reflection at the matched frequency is causing the absorption.

The varactors in the output matching circuit need analyzing at the maximum transmit power to ensure no drift from them. The varactors will likely drift with increased power at the lower tuning states as the bias voltage was close to zero volts in some cases. The maximum RF voltage across the varactors could be several volts and bias them to a different state. Should the varactors drift with increased power, different topologies need investigating to achieve the desired performance.

The feedback network uses resistive taps that measure the total power at the system's input and output. Directional couplers should replace the taps. Depending on the coupler, the transmitted and or reflected wave could be measured. The searching algorithm can then look for a minimum reflection or calculate the input impedance to determine the optimal match.

The current tuning process uses successive iterations. The search method leads to millisecond tuning times. To tune faster, computing the impedance mismatch and tuning to correct for the mismatch in a single step could cut the tuning time of this research by a factor of 200.

The work presented provides a good starting point for further investigation into feedback-driven tunable matching circuits. Along with amplifiers, the lessons learned to apply to all RF systems include Antennas, radio front ends, filters, and more.

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APPENDIX A. CONTROLLER CODE

Ctrl_config.vh

```
`ifndef _ctrl_config_vh_
`define _ctrl_config_vh_

// Command Register Addresses

`define TEST_CMD              4'h1
`define TUNE_EQN_CMD          4'h2
`define DAC_SET_CMD           4'h3
`define DAC_READ_CMD          4'h4
`define IN_ADC_READ_CMD       4'h5
`define OUT_ADC_READ_CMD      4'h6
`define SW_SET_CMD                  4'h7
`define READ_REG_CMD          4'h8
`define TUNE_FRQ_CMD          4'h9



//Read Register addresses
`define TEST_REG        4'h1
`define DAC_SET_REG           4'h2
`define DAC_READ_REG    4'h3
`define IN_ADC_REG            4'h4
`define OUT_ADC_REG           4'h5
`define SW_REG                4'h6
`define FREQUENCY_REG   4'h7
`define PROCESS_REG           4'h8

`endif
```

Thesis_ctrl_master.sv

```
`include "ctrl_config.vh"

module thesis_ctrl_master (
      /////// MASTER CONTROL SIGNALS //////
      input                   CLOCK_50,
      input                   nRST,

      input                   cmd_flag,
      input [30:0]      hps_CMD0,
      input [30:0]      hps_CMD1,
      input [30:0]      hps_CMD2,

      output      reg [31:0]  hps_READ0,


      /////// DAC EXTERNAL SIGNALS //////
      input       DAC_SDO,    //dacs data output to fpga
      output            DAC_SDI,    //dacs data input from fpga
      output            DAC_SCLK,   //dacs serial clock
```

```
      output            DAC_nSYNC,  //dacs nsync line
      output      DAC_nCLR,
      output            DAC_nLDAC,


      ///// ADC EXTERNAL SIGNALS /////
      output      reg [1:0]   ADC_SCLK,    // Clock
      input       reg [1:0]   ADC_DATA,
      output      reg [1:0]   ADC_nCS,

      ///// SWITCH EXTERNAL SIGNALS /////
      output      reg [1:0]   SW_CTRL,

      input board_selection
);


//////////////////////////
// Register Declarations //
//////////////////////////
///// DAC registers
reg               dac_rnw;
reg               dac_cmd_flag;
reg   [11:0]      dac_code;         //code to be sent to the DAC
reg   [2:0] dac_channel;      //channel of the DAC to use
reg [11:0]  dac_rx_data;
reg               dac_done;

///// Frequency Decode Registers
reg [11:0]  frequency;
reg [11:0]  in_dac_code;
reg [11:0]  out0_dac_code;
reg [11:0]  out1_dac_code;

/////ADC registers
reg [1:0]   adc_cmd_flag;
reg [1:0]   adc_done;
reg   [23:0]      adc_rx_data;

///// Switch state register
reg sw_state;

///// Read Registers
reg [15:0]  test;
reg [15:0]  dac_set_reg;
reg [15:0]  dac_read_reg;
reg [15:0]  test_reg;
reg [15:0]  sw_state_reg;
reg [32:0]  process_count_reg;

///// Internal registers
reg [3:0]   cmd_word;
reg [2:0]   channel;
reg [11:0]  data;

reg [15:0]  input_adc_reg;
reg [15:0]  output_adc_reg;
```

```
reg [11:0]  feedback_max;
reg [11:0]  feedback_temp;
reg [11:0]  frequency_max;

reg setup_wait;

reg sweep_done;

reg [15:0] wait_counter;
reg [31:0] process_counter;

/////////////////
// Assignments //
/////////////////


parameter init_test_val = 16'hAAAA;
parameter packed_read_reg = 16'hA420;
parameter input_channel = 3'b001;
parameter output0_channel = 3'b010;
parameter output1_channel = 3'b011;

typedef enum{
      INIT, IDLE, DECODE,
      TEST, TUNE_EQN, TUNE_INPUT_EQN, TUNE_OUTPUT0_EQN, TUNE_OUTPUT1_EQN,
      TUNE_FRQ, TUNE_SWEEP_FRQ, TUNE_SWEEP_DAC_IN, TUNE_SWEEP_DAC_OUT0,
      TUNE_SWEEP_DAC_OUT1, TUNE_SWEEP_WAIT, TUNE_SWEEP_ADC0, TUNE_SWEEP_ADC1,
      DAC_SET, DAC_READ,
      IN_ADC_READ, OUT_ADC_READ, SW_SET,
      UPDATE_REGS, READ_REG
} Statetype;

Statetype state, n_state;

assign cmd_word = hps_CMD0[30:27];

assign dac_cmd_flag =   (state == DAC_SET) ||
                                    (state == DAC_READ) ||
                                    (state == TUNE_INPUT_EQN) ||
                                    (state == TUNE_OUTPUT0_EQN) ||
                                    (state == TUNE_OUTPUT1_EQN) ||
                                    (state == TUNE_SWEEP_DAC_IN) ||
                                    (state == TUNE_SWEEP_DAC_OUT0) ||
                                    (state == TUNE_SWEEP_DAC_OUT1);

assign adc_cmd_flag[0] = (state == IN_ADC_READ) ||  (state ==
TUNE_SWEEP_ADC0);
assign adc_cmd_flag[1] = (state == OUT_ADC_READ) || (state ==
TUNE_SWEEP_ADC1);


always @(posedge CLOCK_50, negedge nRST) begin: STATE_MACHINE
      if (~nRST) begin
            state <= INIT;
      end else begin
            state <= n_state;
```

```
      end
end


always_comb begin : NS_LOGIC
      n_state = state;

      case(state)
            INIT: n_state = IDLE;

            IDLE: n_state = cmd_flag ? DECODE : IDLE;

            DECODE: begin
                  case(cmd_word)
                        `TEST_CMD: n_state = TEST;
                        `TUNE_EQN_CMD: n_state = TUNE_EQN;
                        `DAC_SET_CMD: n_state = DAC_SET;
                        `DAC_READ_CMD: n_state = DAC_READ;
                        `IN_ADC_READ_CMD: n_state = IN_ADC_READ;
                        `OUT_ADC_READ_CMD: n_state = OUT_ADC_READ;
                        `SW_SET_CMD: n_state = SW_SET;
                        `READ_REG_CMD: n_state = READ_REG;
                        `TUNE_FRQ_CMD: n_state = TUNE_FRQ;
                        default: n_state = IDLE;
                  endcase
            end

            TEST: n_state = UPDATE_REGS;
            TUNE_EQN: n_state = TUNE_INPUT_EQN;
            TUNE_INPUT_EQN: n_state = dac_done ? TUNE_OUTPUT0_EQN :
TUNE_INPUT_EQN;
            TUNE_OUTPUT0_EQN: n_state = dac_done ? TUNE_OUTPUT1_EQN :
TUNE_OUTPUT0_EQN;
            TUNE_OUTPUT1_EQN: n_state = dac_done ? UPDATE_REGS :
TUNE_OUTPUT1_EQN;


            TUNE_FRQ: n_state = TUNE_SWEEP_FRQ;
            TUNE_SWEEP_FRQ: n_state = sweep_done ? UPDATE_REGS :
TUNE_SWEEP_DAC_IN;
            TUNE_SWEEP_DAC_IN: n_state = dac_done ? TUNE_SWEEP_DAC_OUT0 :
TUNE_SWEEP_DAC_IN;
            TUNE_SWEEP_DAC_OUT0: n_state = dac_done ? TUNE_SWEEP_DAC_OUT1 :
TUNE_SWEEP_DAC_OUT0;
            TUNE_SWEEP_DAC_OUT1: n_state = dac_done ? TUNE_SWEEP_WAIT :
TUNE_SWEEP_DAC_OUT1;
            TUNE_SWEEP_WAIT: n_state = setup_wait ? TUNE_SWEEP_ADC0 :
TUNE_SWEEP_WAIT;
            TUNE_SWEEP_ADC0: n_state = adc_done[0]? TUNE_SWEEP_ADC1 :
TUNE_SWEEP_ADC0;
            TUNE_SWEEP_ADC1: n_state = adc_done[1]? TUNE_SWEEP_FRQ :
TUNE_SWEEP_ADC1;



            DAC_SET: n_state = dac_done ? UPDATE_REGS : DAC_SET;
            DAC_READ: n_state = dac_done ? UPDATE_REGS : DAC_READ;
```

```
            IN_ADC_READ:n_state = adc_done[0] ? UPDATE_REGS : IN_ADC_READ;
            OUT_ADC_READ:n_state = adc_done[1] ? UPDATE_REGS : OUT_ADC_READ;
            SW_SET:n_state = UPDATE_REGS;
            UPDATE_REGS: n_state = IDLE;
            READ_REG: n_state = IDLE;

      endcase
end


always @(posedge CLOCK_50, negedge nRST) begin
// always_latch begin: OP_LOGIC
      if(~nRST) begin
            test = init_test_val;
            test_reg = 16'h0000;


            dac_rnw = 0;
            // dac_cmd_flag = 0;
            dac_code = 0;           //code to be sent to the DAC
            dac_channel = 0;  //channel of the DAC to use

            /////ADC registers
            // adc_cmd_flag = 0;

            sw_state = 0;

            dac_read_reg = 0;
            dac_set_reg = 0;
            test_reg = 0;
            sw_state_reg = 0;

            data = 0;
            channel = 0;

            input_adc_reg = 0;
            output_adc_reg = 0;
            SW_CTRL = 2'b01;
            hps_READ0 = {packed_read_reg, 16'h0000};

            frequency = 0;

            setup_wait = 0;
            wait_counter = 0;
            feedback_max = 12'h000;
            feedback_temp = 12'h000;
            frequency_max = 12'h000;


            setup_wait = 0;
            sweep_done = 0;

      end else begin

            setup_wait = 0;
```

```
process_counter++;
case (state)
      INIT: begin

      end

      IDLE: begin
            process_counter = 0;

      end

      DECODE: begin
            channel = hps_CMD0[26:24];
            data = hps_CMD0[23:12];
      end

      TEST: begin
            test = ~test;
      end

      TUNE_EQN: begin
            frequency = data;
      end

      TUNE_INPUT_EQN: begin
            if (frequency < 800) begin
                  SW_CTRL = 2'b10;
            end else begin
                  SW_CTRL = 2'b01;
            end
            dac_rnw = 0;
            dac_channel = input_channel;
            dac_code = in_dac_code;
      end

      TUNE_OUTPUT0_EQN: begin
            dac_rnw = 0;
            dac_channel = output0_channel;
            dac_code = out0_dac_code;
      end

      TUNE_OUTPUT1_EQN: begin
            dac_rnw = 0;
            dac_channel = output1_channel;
            dac_code = out1_dac_code;
      end

      TUNE_FRQ: begin
            frequency = data-12'd101;
            frequency_max = 12'd500;
            feedback_temp = 12'h000;
            feedback_max = 12'h000;
      end

      TUNE_SWEEP_FRQ: begin
            //setup switches
            if (frequency < 800) begin
```

```
                              SW_CTRL = 2'b10;
                        end else begin
                              SW_CTRL = 2'b01;
                        end

                        if ((frequency >= (data-12'd100)) &&(sweep_done ==
0)) begin
                              if (adc_rx_data[23:12] > adc_rx_data[11:0])
begin
                                    feedback_temp = adc_rx_data[23:12] -
adc_rx_data[11:0];
                                    if (feedback_temp > feedback_max) begin
                                          frequency_max = frequency;
                                          feedback_max = feedback_temp;
                                    end
                              end
                        end
                        sweep_done = 0;
                        if (frequency ==(data+12'd100)) begin
                              sweep_done = 1;
                              frequency = frequency_max;
                        end else begin
                              frequency++;
                        end
                  end

                  TUNE_SWEEP_DAC_IN: begin
                        dac_rnw = 0;
                        dac_channel = input_channel;
                        dac_code = in_dac_code;
                  end

                  TUNE_SWEEP_DAC_OUT0: begin
                        dac_rnw = 0;
                        dac_channel = output0_channel;
                        dac_code = out0_dac_code;
                  end

                  TUNE_SWEEP_DAC_OUT1: begin
                        dac_rnw = 0;
                        dac_channel = output1_channel;
                        dac_code = out1_dac_code;
                  end

                  TUNE_SWEEP_WAIT: begin
                        if (wait_counter == 16'd4095) begin
                              wait_counter = 0;
                              setup_wait = 1;
                        end else begin
                              wait_counter++;
                        end
                  end

                  TUNE_SWEEP_ADC0: begin

                  end
```

```
                    TUNE_SWEEP_ADC1: begin

                    end

                    DAC_SET: begin
                          dac_rnw = 0;
                          dac_channel = channel;
                          dac_code = data;
                    end

                    DAC_READ: begin
                          dac_rnw = 1;
                    end

                    IN_ADC_READ: begin
                    end

                    OUT_ADC_READ: begin
                    end

                    SW_SET: begin
                          sw_state = data[0];
                          if (sw_state) begin
                                SW_CTRL= 2'b10;
                          end else begin
                                SW_CTRL = 2'b01;
                          end
                    end

                    UPDATE_REGS: begin
                          test_reg <= test;
                          dac_set_reg <= {1'b1, dac_channel, dac_code};
                          dac_read_reg <= {4'h0, dac_rx_data};
                          input_adc_reg <= {4'h0, adc_rx_data[11:0]};
                          output_adc_reg <= {4'h0, adc_rx_data[23:12]};
                          sw_state_reg <= {15'h000, sw_state};
                          process_count_reg <= process_counter;
                    end

                    READ_REG: begin   // Assigns the desired register to the
ethernet command read register
                          hps_READ0 = {packed_read_reg, 16'h0000};
                          case(data[3:0])
                                `TEST_REG: hps_READ0 = {packed_read_reg,
test_reg};
                                `DAC_SET_REG: hps_READ0 = {packed_read_reg,
dac_set_reg};
                                `DAC_READ_REG: hps_READ0 = {packed_read_reg,
dac_read_reg};
                                `IN_ADC_REG: hps_READ0 = {packed_read_reg,
input_adc_reg};
                                `OUT_ADC_REG: hps_READ0 = {packed_read_reg,
output_adc_reg};
                                `SW_REG: hps_READ0 = {packed_read_reg,
sw_state_reg};
                                `FREQUENCY_REG: hps_READ0 = {packed_read_reg,
frequency};
```

```
                                `PROCESS_REG: hps_READ0 = process_count_reg;
                                default: hps_READ0 = {packed_read_reg,
16'hFFFF};
                        endcase
                end
            endcase
      end

end



AD5504 AD5504(
      .CLOCK_50(CLOCK_50),
      .nRST(nRST),
      .rnw(dac_rnw),
      .cmd_flag (dac_cmd_flag),
      .code(dac_code),
      .channel(dac_channel),
      .rx_data(dac_rx_data),
      .dac_done(dac_done),
      .DAC_SDI(DAC_SDI),
      .DAC_SDO(DAC_SDO),
      .DAC_SCLK(DAC_SCLK),
      .DAC_nSYNC(DAC_nSYNC),
      .DAC_nCLR(DAC_nCLR),
      .DAC_nLDAC(DAC_nLDAC)
      );

ADC121S021 INPUT_ADC(
      .CLOCK_50(CLOCK_50),
      .nRST    (nRST),
      .adc_done    (adc_done[0]),
      .rx_data (adc_rx_data[11:0]),
      .ADC_SCLK(ADC_SCLK[0]),
      .ADC_DATA(ADC_DATA[0]),
      .ADC_nCS (ADC_nCS[0]),
      .cmd_flag(adc_cmd_flag[0])
      );

ADC121S021 OUTPUT_ADC(
      .CLOCK_50(CLOCK_50),
      .nRST    (nRST),
      .adc_done    (adc_done[1]),
      .rx_data (adc_rx_data[23:12]),
      .ADC_SCLK(ADC_SCLK[1]),
      .ADC_DATA(ADC_DATA[1]),
      .ADC_nCS (ADC_nCS[1]),
      .cmd_flag(adc_cmd_flag[1])
      );

frequency_decoder frequency_decoder(
      .frequency    (frequency),
      .in_dac_code  (in_dac_code),
      .out0_dac_code(out0_dac_code),
      .out1_dac_code(out1_dac_code),
      .board_selection(board_selection)
```

```
);
Endmodule
```

AD5504.sv

```
/*
This module is the DAC controller module. It reads in a DAC code and channel
and shifts it out
to the DAC
*/

module AD5504(
///// CLOCK and reset Signals////////////
      input CLOCK_50,
      input nRST,

///// module signals /////////////
      input                         rnw,
      input                         cmd_flag,
      input             [11:0]      code,       //code to be sent to the DAC
      input       [2:0] channel,    //channel of the DAC to use
      output      reg [11:0]  rx_data,
      output                        dac_done,

/////////DAC EXTERNAl SIGNALS//////////////////////
      input       DAC_SDO,    //dacs data output to fpga
      output      reg DAC_SDI,      //dacs data input from fpga
      output            DAC_SCLK,   //dacs serial clock
      output      reg   DAC_nSYNC,  //dacs nsync line
      output  reg DAC_nCLR,
      output      reg DAC_nLDAC
);

reg [15:0] output_buff;
reg   [11:0] input_buff;
reg [7:0] clk_counter;
reg [4:0] spi_count;
reg sclk_en;

reg DAC_CLOCK;

typedef enum{
      IDLE, SYNC, LSB,
      SPI, END
} Statetype;

Statetype state, n_state;

parameter CLOCK_DIVISION = 24;

assign DAC_SCLK = sclk_en & DAC_CLOCK;
assign dac_done = state == END;
assign DAC_nLDAC = 0;
assign DAC_nCLR = 1;


always @(posedge CLOCK_50, negedge nRST) begin : CLOCK_DIVIDER
```

```
	if(~nRST) begin
		DAC_CLOCK = 0;
		clk_counter = 0;

	end else if (clk_counter == CLOCK_DIVISION) begin
		DAC_CLOCK =~DAC_CLOCK;
		clk_counter = 0;
	end else begin
		clk_counter = clk_counter +1;
	end
end

always @(posedge CLOCK_50, negedge nRST) begin: STATE_MACHINE
	if (~nRST) begin
		state <= IDLE;
	end else begin
		state <= n_state;
	end
end

always_comb begin: NS_LOGIC
	n_state = state;

	case(state)
		IDLE: n_state = cmd_flag ? SPI : IDLE;
		SYNC: n_state = sclk_en ? SPI : SYNC;
		SPI: n_state = (spi_count[4]) ? LSB: SPI;
		LSB: n_state = (spi_count == 4'h0) ? END : LSB;
		END: n_state = IDLE;
	endcase
end

always @(negedge DAC_CLOCK, negedge nRST) begin : SHIFT_TO_DAC
	if(~nRST) begin
		DAC_SDI = 0;
		DAC_nSYNC = 1;
		spi_count = 0;
		output_buff = 0;
		sclk_en = 0;

		input_buff = 0;
		rx_data = 0;
	end else begin
		sclk_en = 0;
		DAC_nSYNC = 1;
		case(state)
			SPI: begin
				sclk_en = 1;
				DAC_nSYNC = 0;
				if (spi_count  == 4'h0)begin
					output_buff = {rnw, channel, code};
				end

				if (~rnw) begin
					DAC_SDI = output_buff[15];
					output_buff = output_buff << 1;
				end
```

```
                        if(rnw & (spi_count < 4)) begin
                              DAC_SDI = output_buff[15];
                              output_buff = output_buff << 1;
                        end

                        if(rnw & (spi_count > 4)) begin
                              input_buff = {input_buff[10:0], DAC_SDO};
                        end
                        spi_count = spi_count + 1;
                  end

                  LSB: begin
                        sclk_en = 0;
                        spi_count = 0;
                        input_buff = {input_buff[10:0], DAC_SDO};
                        rx_data = input_buff;
                  end

                  END: begin

                  end

            endcase
      end
end

endmodule
```

ADC121S021.sv

```
module ADC121S021 (
      input                         CLOCK_50,
      input                         nRST,

      input                         cmd_flag,
      output      reg         adc_done,
      output      reg   [11:0]      rx_data,
      output      reg         ADC_SCLK,
      input       reg         ADC_DATA,
      output      reg         ADC_nCS


);
reg [11:0] rx_buff;
reg [4:0] counter;
reg sclk_en;
reg [7:0] clk_counter;
reg ADC_CLOCK;
reg enabled;



typedef enum{
      IDLE, ENABLE,
      SHIFT, WAIT, END
} Statetype;
```

```
Statetype state, n_state;


parameter CLOCK_DIVISION = 12;

assign ADC_SCLK = (sclk_en) ? ADC_CLOCK : 1;
assign adc_done = state == END;

always @(posedge CLOCK_50, negedge nRST) begin : CLOCK_DIVIDER
      if(~nRST) begin
            ADC_CLOCK = 0;
            clk_counter = 0;

      end else if (clk_counter == CLOCK_DIVISION) begin
            ADC_CLOCK =~ADC_CLOCK;
            clk_counter = 0;
      end else begin
            clk_counter = clk_counter +1;
      end
end


always @(posedge CLOCK_50, negedge nRST) begin: STATE_MACHINE
      if (~nRST) begin
            state <= IDLE;
      end else begin
            state <= n_state;
      end
end


always_comb begin: NS_LOGIC
      n_state = state;

      case(state)
            IDLE: n_state = cmd_flag ? ENABLE : IDLE;
            ENABLE: n_state = (enabled) ? SHIFT : ENABLE;
            SHIFT: n_state = (counter == 16) ? WAIT : SHIFT;
            WAIT: n_state = (counter == 0) ? END : WAIT;
            END: n_state = IDLE;
      endcase
end

always @(posedge CLOCK_50, negedge nRST) begin
      if(~nRST) begin
      end else begin
            case(state)
                  IDLE: begin
                  end

                  END: begin
                  end
            endcase
      end
end

always @(posedge ADC_CLOCK, negedge nRST) begin : SHIFT_FROM_ADC
```

```
	if(~nRST) begin
		counter = 0;
		rx_buff = 0;
		rx_data = 0;
		ADC_nCS = 1;
		enabled = 0;

	end else begin
		sclk_en = 1;
		ADC_nCS = 0;
		enabled = 0;

		case (state)
			IDLE: begin
				sclk_en = 0;
				ADC_nCS = 1;
			end

			ENABLE: begin
				sclk_en = 0;
				enabled = 1;

			end

			SHIFT: begin
				if ((counter > 3) & (counter < 16)) begin
					rx_buff = {rx_buff[10:0], ADC_DATA};
				end
				counter = counter +1;
			end

			WAIT: begin
				ADC_nCS = 1;
				sclk_en = 0;
				counter = counter + 1;
				if (counter == 19) begin
					counter = 0;
					rx_data = rx_buff;
				end
			end

			END: begin
				ADC_nCS = 1;
				sclk_en = 0;

			end
		endcase

	end
end

endmodule
```

frequency_decoder.sv

```
module frequency_decoder(
      input             [11:0]      frequency,
      input                         board_selection,
      output reg  [11:0]      in_dac_code,
      output reg  [11:0]      out0_dac_code,
      output reg  [11:0]      out1_dac_code
      );

reg [63:0]  in_term1;
reg [63:0]  in_term2;
reg [63:0]  in_term3;
reg [63:0]  in_term4;
reg [63:0]  in_term5;
reg [63:0]  in_buffer;

reg [63:0]  out0_term1;
reg [63:0]  out0_term2;
reg [63:0]  out0_term3;
reg [63:0]  out0_term4;
reg [63:0]  out0_term5;
reg [63:0]  out0_buffer;

reg [63:0]  out1_term1;
reg [63:0]  out1_term2;
reg [63:0]  out1_term3;
reg [63:0]  out1_term4;
reg [63:0]  out1_term5;
reg [63:0]  out1_buffer;

reg [11:0]  in_freq;
reg [11:0]  out0_freq;
reg [11:0]  out1_freq;


assign in_dac_code = in_buffer[11:0];
assign out0_dac_code = out0_buffer[11:0];
assign out1_dac_code = out1_buffer[11:0];

always_comb begin// tune the input capacitor
      //assign each frequency to the input frequency
      in_freq = frequency;
      out0_freq = frequency;
      out1_freq = frequency;
      if(board_selection) begin
            //if the frequency is too low set it to minimum
            if (frequency < 700) begin
                  in_freq = 700;
                  out0_freq = 700;
                  out1_freq = 700;
            end

            //if frequency is to high set to maximum
            if (frequency > 2500) begin
                  in_freq = 2500;
                  out0_freq = 2500;
```

```
                  out1_freq = 2500;
            end

            if(frequency > 1900) begin
                  in_freq = 1900;
            end

            if(frequency > 2300) begin
                  out1_freq = 2300;
            end
            // Create terms for the input tuning capacitor
            if (in_freq < 800) begin
                  in_term1 = in_freq*in_freq*in_freq*in_freq/64'd44597066;
                  in_term2 = in_freq*in_freq*in_freq*64'd10/64'd214407;
                  in_term3 = in_freq*in_freq*64'd10000/64'd356877;
                  in_term4 = in_freq*64'd10000/64'd57253;
                  in_term5 = 64'd2650;
                  in_buffer = (in_term1+in_term3+in_term4)-
(in_term2+in_term5);
            end else begin
                  in_term1 = in_freq*in_freq*in_freq*in_freq/64'd2732240437;
                  in_term2 = in_freq*in_freq*in_freq/64'd323033;
                  in_term3 = in_freq*in_freq*64'd1000/64'd115263;
                  in_term4 = in_freq*64'd107378/64'd10000;
                  in_term5 = 64'd4374;
                  in_buffer = (in_term2+in_term4)-
(in_term1+in_term3+in_term5);
            end

            //Create tems for output tuning capacitor 1
            out0_term1 =
out0_freq*out0_freq*out0_freq*out0_freq/64'd18281535649;
            out0_term2 = out0_freq*out0_freq*out0_freq/64'd3098862;
            out0_term3 = out0_freq*out0_freq/64'd1780;
            out0_term4 = out0_freq*64'd1000/64'd3459;
            out0_term5 = 64'd303;

            //Create tems for output tuning capacitor 1
            out1_term1 =
out1_freq*out1_freq*out1_freq*out1_freq/64'd1078748652;
            out1_term2 = out1_freq*out1_freq*out1_freq/64'd187444;
            out1_term3 = out1_freq*out1_freq*64'd1000/64'd90677;
            out1_term4 = out1_freq*64'd10816/64'd1000;
            out1_term5 = 64'd3746;

            //Combine terms into final DAC codes
            // in_buffer = (in_term1+in_term3)-(in_term2+in_term4);
            out0_buffer = (out0_term1+out0_term3+out0_term4)-
(out0_term2+out0_term5);
            out1_buffer = (out1_term2+out1_term4)-
(out1_term1+out1_term3+out1_term5);
      end else begin
            //if the frequency is too low set it to minimum
            if (frequency < 500) begin
                  in_freq = 500;
                  out0_freq = 500;
                  out1_freq = 500;
```

```
            end

            //if frequency is to high set to maximum
            if (frequency > 2500) begin
                  in_freq = 2500;
                  out0_freq = 2500;
                  out1_freq = 2500;
            end

            if(frequency > 2200) begin
                  in_freq = 2200;
            end

            if(frequency > 2300) begin
                  out0_freq = 2300;
            end

            if(frequency > 1600) begin
                  out1_freq = 1600;
            end
            // Create terms for the input tuning capacitor
            if (in_freq < 800) begin
                  in_term1 =
in_freq*in_freq*in_freq*in_freq*64'd10/64'd104384133;
                  in_term2 = in_freq*in_freq*in_freq* 64'd10/64'd40237;
                  in_term3 = in_freq*in_freq*64'd10000/64'd42614;
                  in_term4 = in_freq*929373/10000;
                  in_term5 = 64'd12881;
                  in_buffer = (in_term1+in_term3+in_term5)-
(in_term2+in_term4);
            end else begin
                  in_term1 = in_freq*in_freq*in_freq*in_freq/64'd1055966209;
                  in_term2 = in_freq*in_freq*in_freq/64'd162248;
                  in_term3 = in_freq*in_freq/64'd68;
                  in_term4 = in_freq*64'd16017/64'd1000;
                  in_term5 = 64'd6120;
                  in_buffer = (in_term2+in_term4)-
(in_term1+in_term3+in_term5);
            end

            // Create terms for output tuning capacitor 0
            out0_term1 =
out0_freq*out0_freq*out0_freq*out0_freq/64'd3115264797;
            out0_term2 = out0_freq*out0_freq*out0_freq/64'd563417;
            out0_term3 = out0_freq*out0_freq/64'd294;
            out0_term4 = out0_freq*64'd2032/64'd1000;
            out0_term5 = 64'd373;

            //Create tems for output tuning capacitor 1
            out1_term1 =
out1_freq*out1_freq*out1_freq*out1_freq/64'd112879558;
            out1_term2 = out1_freq*out1_freq*out1_freq/64'd34002;
            out1_term3 = out1_freq*out1_freq*64'd1000/64'd28409;
            out1_term4 = out1_freq*64'd16488/64'd1000;
            out1_term5 = 64'd2567;

            //Combine terms into final DAC codes
```

```
            // in_buffer = (in_term1+in_term3)-(in_term2+in_term4);
            out0_buffer = (out0_term1+out0_term3+out0_term5)-
(out0_term2+out0_term4);
            out1_buffer = (out1_term1+out1_term3+out1_term5)-
(out1_term2+out1_term4);
      end

end


endmodule
```

APPENDIX B. EQUATION CALCULATIONS

Derivation of Series Inductance with a tuning capacitor

$$j\omega L_{Equivalent} = j\omega L_{Fixed} + \frac{-j}{\omega C_{Variable}}$$

$$j\omega L_{Equivalent} = \frac{j\omega^2 L_{Fixed} C_{Variable} - j}{\omega C_{Variable}}$$

$$\omega L_{Equivalent} = \frac{\omega^2 L_{Fixed} C_{Variable} - 1}{\omega C_{Variable}}$$

$$L_{Equivalent} = \frac{\omega^2 L_{Fixed} C_{Variable} - 1}{\omega^2 C_{Variable}} \qquad \text{EQN}(2.22)$$