A PROCESS FOR HYBRID SUPERCONDUCTING AND GRAPHENE DEVICES

by

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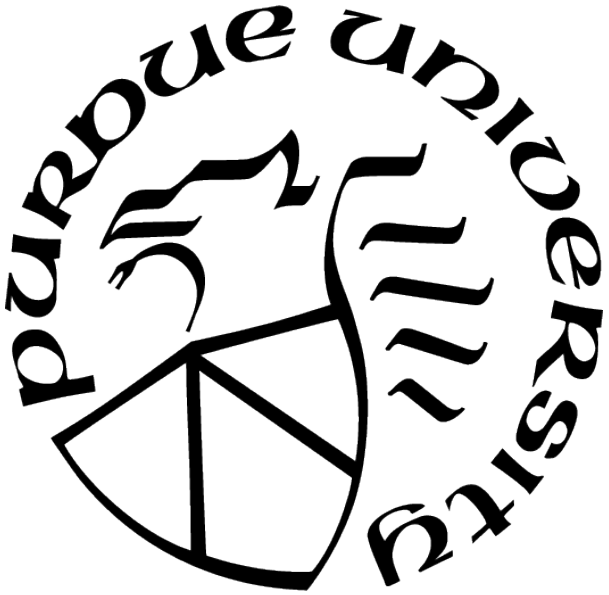

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B_c	superconducting critical magnetic field
C	capacitance
C_{ox}	transistor oxide characteristic capacitance
c	speed of light in a vacuum, $c = (\mu_0\epsilon_0)^{-1/2} = 299792458\,\mathrm{m}\cdot\mathrm{s}^{-1}$
χ_m	magnetic susceptibility, $\chi_m \equiv \mu_r - 1$
Δ	subgap potential energy at $T = 0$ K
$\tan\delta$	loss tangent
e	fundamental charge, $e = 1.60218^{-19}\,\mathrm{C}$ (not to be confused with Euler's number, e)
ϵ	material electrical permittivity
ϵ_0	permittivity of free space, $\epsilon_0 = 8.8541878 \times 10^{-12}\,\mathrm{F}\cdot\mathrm{m}^{-1}$
ϵ_r	relative permittivity/dielectric constant, $\epsilon_r = \epsilon/\epsilon_0$ (sometimes "κ")
h	Planck's constant, $h = 6.62607 \times 10^{-34}\,\mathrm{m}^2\cdot\mathrm{kg}\cdot\mathrm{s}^{-1}$, or height (usage varies)
$\hbar$	Planck's reduced constant, $\hbar \equiv h/2\pi$
I_c	superconducting critical current
I_{DS}	transistor drain-source current
k	wavevector/wavenumber, $k = 2\pi/\lambda$, or an arbitrary constant (usage varies)
k_B	Boltzmann constant, $k_B = 1.38064852 \times 10^{-23}\,\mathrm{J}\cdot\mathrm{K}^{-1}$
L	inductance or length (usage varies)
λ	wavelength
λ_L	London penetration depth
m	mass
m_e	electron mass
m_p	hole (effective) mass
μ	mobility or material magnetic permeability (usage varies)
μ_0	magnetic permeability of free space, $\mu_0 \approx 4\pi \times 10^{-7}\,\mathrm{H}\cdot\mathrm{m}^{-1}$
μ_e	electron mobility
μ_p	hole mobility

μ_r	relative magnetic permeability, $\mu_r = \mu/\mu_0$
n	charge carrier density or index of refraction (usage varies)
ω	angular frequency
ω_D	Debye frequency
ϕ	electromagnetic flux
Φ_0	single-flux quanta, $\Phi_0 = 2\pi\hbar/2e$
φ	electron momentum phase difference
R	resistance
R_N	"normal" resistance
R_{SG}	subgap resistance
σ	conductivity
σ_n	normal conductivity (sometimes σ_1)
T	absolute temperature in Kelvin
t	thickness or time (usage varies)
T_c	superconducting critical temperature
t_{ox}	transistor oxide thickness
θ_D	Debye temperature
V_{DD}	transistor drain voltage supply
V_{SG}	subgap voltage, $2\Delta/e$
v	velocity
W	width (usually transistor channel width, sometimes w)
ξ	superconductor wave coherence length (sometimes ξ_s)
ζ	magnetic energy stored in a superconducting material
Z_s	surface impedance
Z_s^{FT}	finite-thickness surface impedance

ABBREVIATIONS

AGNR	armchair graphene nanoribbon
BCS	Bardeen-Cooper-Schrieffer
BTB	band-to-band
CDA	common-drain attenuator (amplifier)
CNT	carbon nanotube
CNTFET	carbon nanotube field-effect transistor (sometimes "CNFET")
CSA	common-source amplifier
CVD	chemical vapor deposition
DOS	density-of-states
EHF	extremely high frequency
FET	field-effect transistor
FHIB	focused helium ion beam
FinFET	fin field-effect transistor
FM	frequency modulation
FOM	figure of merit
GBWP	gain-bandwidth product
GFET	graphene field-effect transistor
GNR	graphene nanoribbon
GNRFET	graphene nanoribbon field-effect transistor
HEMT	high-electron-mobility transistor
HTS	high-temperature superconductor
IBAD	ion-beam-assisted deposition
JJ	Josephson junction
LTS	low-temperature superconductor
MMIC	monolithic microwave integrated circuit
MMW	millimeter wave
NEGF	non-equilibrium Green functions
PLD	pulsed laser deposition

PLL	phase-locked loop
RCSJ	resistive capacitively-shunted junction
SB	Schottky-barrier
SBGNRFET	Schottky-barrier graphene nanoribbon field-effect transistor
SET	single-electron transistor
SN	superconductor-normal metal
SNS	superconductor-normal-superconductor
TEM	transverse electromagnetic mode
TFA-MOD	metal organic deposition using trifluoroacetate salts
TFET	tunneling field-effect transistor
TSV	through-silicon via
ULSI	ultra-large-scale integration
VCO	voltage-controlled-oscillator
VLSI	very large-scale integration
VTB	variable-thickness-bridge
ZZGNR	zig-zag graphene nanoribbon

NOMENCLATURE

ALO	aluminum oxide (Al_2O_3, sometimes "sapphire")
Au	elemental gold
$BaZrO_3$	barium-doped zirconium
BSCCO	bismuth strontium calcium copper oxide ("bisko") ceramic HTS
CeO_2	cerium oxide
h-BN	hexagonal 2D boron nitride
H_2S	metallic hydrogen sulfide
$H_2S + CH_4$	carbonaceous sulfur hydride
H_2SO_4	sulfuric acid
HfO_2	hafnium oxide
Hg	elemental mercury
$KMnO_4$	potassium permanganate
LaH_{10}	metallic lanthanum hydrogen
LAO	lanthanum aluminum oxide ($LaAlO_3$ or $LaAl_2O_3$)
LBCO	lanthanum barium copper oxide HTS
MgO	magnesium oxide
Nb	elemental niobium
NbN	niobium nitrate
Nb_3Sn	niobium tin
$NdGaO_3$	neodymium gallium oxide
Pb	elemental lead
Si	elemental silicon
SiC	silicon carbide
SiO_2	silicon oxide (sometimes just "oxide")
STO	strontium titanate ($SrTiO_3$)
TBCCO	thallium barium calcium copper oxide ("tibco") ceramic HTS
YBCO	yttrium barium cupric oxide ceramic HTS
YSZ	yttria-stabilized zirconia

GLOSSARY

BCS Theory	Bardeen-Cooper-Schrieffer theory of superconductivity
Debye Frequency	the maximum supported phonon standing-wave frequency present in an ionic lattice enclosed in a finite cube
Debye Temperature	the temperature associated with the Debye frequency, $k_B\theta_D = \hbar\omega_D$
EHF	radio wave band designation for 30-300 GHz
Heterojunction	a junction formed at the interface between two different materials
MMW	another name for EHF
quasi-TEM	an approximation of the electromagnetic fields in wires that assumes the modes are nearly TEM fields
Relativistic conduction	conduction in a material where charge velocities are comparable to the speed of light
Retroreflection	a variation on reflection, where velocity is reversed, but angle is not changed, so that which is reflected follows the path it took to reach the surface of reflection, rather than scatter off of it
SI Junction	superconductor-insulator junction
SIS Junction	superconductor-insulator-superconductor junction, frequently forms a thin Josephson junction
SN Junction	superconductor-normal metal junction
SNS Junction	superconductor-normal-superconductor junction, frequently forms a Josephson junction
TEM	an electromagnetic mode on wires that assumes the electric and magnetic fields are orthogonal
Type-I Superconductor	superconductor with zero magnetic flux penetration depth
Type-II Superconductor	superconductor with nonzero magnetic flux penetration depth

ABSTRACT

As the search for ever-higher-speed, greater-density, and lower-power technologies accelerates, so does the quest for devices and methodologies to fulfill the increasingly-difficult requirements for these technologies. A possible means by which this may be accomplished is to utilize superconducting devices and graphene nanoribbon nanotechnologies. This is because superconductors are ultra-low-power devices capable of generating extremely high frequency (EHF) signals, and graphene nanoribbons are nanoscale devices capable of extremely high-speed and low-power signal amplification due to their high-mobility/low-resistance channels and geometry-dependent bandgap structure. While such a hybrid co-integrated system seems possible, no process by which this may be accomplished has yet been proposed.

In this thesis, the system limitations are explored in-depth, and several possible means by which superconducting and graphene nanotechnological systems may be united are proposed, with the focus being placed on the simplest method by which the technologies may be hybridized and integrated together, while maintaining control over the intended system behavior. This is accomplished in three parts. First, via circuit-level simulation, a semi-optimized, low-power (~0.21 mW/stage) graphene-based amplifier is developed using ideal and simplified transmission line properties. This system is theoretically capable of 159-269 GHz bandwidth with a Stern stability $K \gg 1$ and low noise figure $2.97 \leq F \leq 4.33$ dB for all appropriate frequencies at temperatures between 77 and 90 K. Second, an investigation of the behavior of several types of possible interconnect methodologies is performed, utilizing hybrid substrates and material interfaces/junctions, demonstrating that an Ohmic-contact superconducting-normal transmission line is optimal for a hybrid system with self-reflections at less than -25 dB over an operating range of 300 GHz. Finally, a unified layout and lithography construction process is proposed by which such a hybrid system could be developed in a monolithic physical system on a hybrid substrate while maintaining material and layout integrity under varying process temperatures.

1. INTRODUCTION

1.1 Motivation

Since the discovery of the Josephson effect, there have been many significant applications: the discovery of the DC effect led to the idea for the official NIST voltage standard [1]–[6], and the ability to store electromagnetic flux quanta in a loop formed by two parallel junctions as a superconducting quantum interference device (SQUID) led to significant research in the area of low-flux magnetometers [7], quantum computing and qubit research [8]–[11], the area of physics research called parity-time-symmetry ($\mathcal{PT}$-symmetry, which studies non-Hermitian Hamiltonians) [9], [12], [13], and many other research areas. These SQUIDs also became useful for superconducting logic systems, rapid single-flux quantum (RSFQ) logic [3], [14], [15], and have been applied in a number of ways, such as VLSI/ULSI-style memory arrays [16], nano-scale inductors [17], flip-flops [18], and other computational applications [19], [20]. Recent research has used also used SQUIDs as terahertz/millimeter-wave (THz/MMW) signal generators [3], [4], [21]–[24], monolithic-microwave IC (MMIC) devices [3], [4], [25], RF/antenna applications [4], [21], [22], and phase-locked loops (PLLs), especially due to the voltage-controlled-oscillator (VCO) properties these devices exhibit and the inherent AC- and DC-effects making them ideal for signal generation and reception.

The vast number of high-speed and high-accuracy/precision applications for which these devices have been suggested makes them a desirable technology, but the challenge remains in combining them with normal technologies, such as CMOS or CMOS-like systems, due in part to their temperature requirements and due in part with the different manufacturing methods required. While graphene nanoribbon FETs (GNRFETs) can potentially handle the temperature requirements [23], [24], [26], the manufacturing methods for both are exceptionally challenging, as no one set of process rules exist because GNRFETs themselves are still experimental devices with very few process rules, and the concept of hybrid graphene-Josephson junction (JJ) systems is still theoretical. Thus, this the motivation for this research: to propose a basic, unified process and layout scheme which can be used to develop precise design rules.

1.2 Thesis Problem Statement and Research Issues

To combine superconducting devices together with non-superconducting devices, such as analog GNR nanostructures or CMOS, to create extremely high-frequency (EHF) systems, this thesis answers the following five major research questions about such a hybrid system:

- Hybrid Interfacing: How might superconductive systems, which rely on low temperatures and power, be combined with nanotechnological systems which may or may not operate properly in the same operational regions?
- Physics-based issues: With EHF systems, how does the electromagnetic physics place restrictions on the design of the system? What kind of issues may result from SN heterojunctions, especially considering Andreev reflections?
- Transmission-line analysis: At EHF ranges, how well do interconnects work? How lossy are they? Is there a benefit to utilizing nanostrip/nanoribbon interconnects compared to superconducting interconnects or nanowires? Would electromagnetically-coupled resonators operate more optimally?
- Substrate compatibility: Can superconducting devices and graphene nanotechnologies operate on the same physical substrate, or do they need separate substrates due to lattice constant-related issues? If different substrates are required, is 3D substrate layering a viable option, with TSVs, or would separate dies be required, utilizing nanowires?
- Process considerations: How could a hybrid system like the ones propose here be potentially grown or otherwise physically developed?

Here, these considerations are investigated thoroughly, and a proposed process for combining the two distinct systems into one is developed based on these questions.

1.3 Present Efforts and Current Work

Some work in regards to developing a basic hybrid system has been performed already, investigating whether or not it is conceivably possible to even interface ideal graphene-based

and superconducting-based devices, especially due to temperature differences. Utilizing a simple Josephson junction model written in SPICE (Appendix A.1) and Verilog-A (Appendix A.2), and simulated at temperature of 90 K, previous work presented in Refs. [24] and [23] demonstrate that it is theoretically possible to generate, control, and transmit a sub-terahertz signal from a Josephson junction array to a GNRFET-based amplifier chain, raising the signal level from millivolt to volt levels at frequencies between 200 and 300 GHz.

While this initial work assumes ideal wires, current and voltage sources, and noiseless devices, it remains a promising prospective means of generating such high-frequency signals. However, the liquid-nitrogen-temperatures, relative to room temperature (300 K), are somewhat of a limitation, and, as of the time those papers were published, the noise and stability properties of the junctions and amplifiers were still unknown.

The amplifier presented in [23] and [24] is also itself rudimentary and designed on the assumption that the amplifier is stable and has sufficient noise properties to work in the EHF range, without stability and noise analysis. To be a viable system model, the GNRFET CDA-CSA-CDA amplifier needs to go under a more intensive investigation that takes stability and noise into consideration, as well as some level of transmission-line effects.

1.4 Present Limitations

There are several limitations for this research. First is the inability to provide experimental results beyond those of physics-based or highly-accurate simulation modeling. Because of the combination of lack of access to the systems required to construct these devices and the sheer difficulty of precisely and consistently manufacturing devices such as the GNRFETS, according to Refs. [27]–[32], no physical results or experimental data can be acquired, relegating this research to the realm of theoretical/experimental devices.

Simulations themselves are limited due to access to physics-based simulation software primarily intended for superconductor research or 2D material exploration. As such, superconductor modeling must rely on the capabilities or limitations of material modeling in CST Studio, and simulating the GNR-based devices is restricted to the capabilities and limitations of HSPICE/Verilog-A modeling of RF, graphene, or superconducting devices in Cadence Vir-

tuoso. While software like CST Studio and Cadence Virtuoso are exceptionally-accurate for ideal systems and a significant number of realistic systems, there are some instances where their results may not be able to be properly verified, simply due to lack of experimental data or the limitations of the device models themselves.

Unrelated to the tools at hand, other limitations for this research are more physical, in that they are general challenges that physicists and engineers are, to this day, struggling against. Perhaps the most obvious of these challenges is that of the high-temperature or room-temperature superconductor. While the high-temperature superconductive ceramic YBCO is utilized or referenced here as the superconductor of choice (due to its widespread use and the easy access to liquid nitrogen), it is still severely limited by the fact that it is operable around 90 K, though typically used at temperatures closer to 77 K. Future research may one day remove this limitation and others, but until then, this point remains the greatest challenge/limitation to this research.

Other limitations are discussed in greater depth in Chapter 4, but many of them are limitations which this research seeks to address and resolve, as have been mentioned previously in Sec. 1.2.

1.5 Thesis Organization

This research follows the development of a hybrid superconducting-graphene nanotechnology system from the fundamental physics aspect to the proposed physical implementation, discussing the considerations as the thesis progresses. Starting in Chapter 2, the historical perspective and context of superconductivity and graphene nanodevices is provided, as well as a brief, high-level overview of their theory of operation, as necessary to further develop the discussion on the system limitations. In Chapter 3 the superconducting and graphene device models are reviewed, with the GNRFET-based amplifiers revisited and investigated under more thorough analysis (Chapters 3.1 and 3.2, respectively). Chapter 4 investigates, in-depth, the limitations and means of hybridization of the technologies, particularly with the substrates and interconnect methodology (Chapters 4.1 and 4.3, respectively), and finally a proposal for the possible process (Chapter 4.4). Chapter 5 proposes future work that

could extend from this research, and Chapter 6 summarizes these findings succinctly, and re-iterates the proposed hybridization process.

2. BACKGROUND AND BASIC THEORY

2.1 Superconducting Devices

An unexpected discovery was made by Kamerlingh Onnes in 1911 while measuring the temperature-dependence of conductivity in mercury [3], [4]. He described superconductivity to be the phenomenon wherein the resistivity of a material disappears when cooled below some critical temperature, T_c, leading to zero DC power dissipation. Later, a magnetic-field-effect named after one of its discoverers, Meissner and Ochsenfeld [3], [4], [33]–[37], would be found as a consequence of zero resistivity. Since then, many new superconducting compounds have been discovered, with requirements ranging from 4.2 K temperatures at ambient pressure to nearly-room-temperature (287 K) at 267 GPa pressures [38], and many parameters in between. Table 2.1 summarizes some superconductors of historical and modern importance.

One of the means used to prove a material is superconducting is the *Meissner effect*. In this effect, magnetic field lines are expelled entirely (Type-I superconductors) or nearly-entirely (Type-II superconductors) from a material, and instead either wrap around the superconductor, as illustrated in Fig. 2.1, or are completely folded back over the magnetic field source. When magnetic flux is applied near the superconductor, it induces a circulation current in the superconductor. Because there is zero resistance, the current formed by Faraday's Law is exactly strong-enough to equal and oppose the external magnetic field. Because of this, the magnetic field inside the superconductor is zero, but since magnetic flux lines cannot terminate (causing $\nabla \times \boldsymbol{B} \neq 0$, which is prohibited as far as is known), the external magnetic field lines must either go around the superconductor or otherwise double back on themselves without crossing, which results in a phenomenon called *flux pinning* [3], [4], [33], [37]. Thus, the Meissner effect is equivalent to perfect diamagnetism. The presence or absence of the Meissner effect is what is used to verify the superconductivity of a material, and was used to prove that superconductivity was not perfect conductivity and instead that a superconductor's conductivity was finite [4], [33], [37].

If superconductors were perfect conductors, then the current generated in the superconductor would be infinite, and the resulting opposing magnetic field would be, accordingly,

Table 2.1. A list of historical and common superconductors.

Material	Year	T_c (K)	Pressure
Hg [3]	1911	4.15	Ambient
Pb [3], [39]	1912	7.19	Ambient
Nb [3], [39]	1925	8.4	Ambient
NbN [3], [40]	1942	16	Ambient
Nb_3Sn [3], [41]	1954	18.3	Ambient
Nb_3Ge [3], [42]	1973	23.2	Ambient
LBCO [3], [43]	1986	≤ 35	Ambient
YBCO [3], [44]	1987	≥ 92	Ambient
BSCCO [3], [45]	1988	110	Ambient
TBCCO [3], [46]	1988	127	Ambient
H_2S [47]	2015	203	100 GPa
LaH_{10} [48]	2018	250	170 GPa
$H_2S + CH_4$ [38]	2020	287	267 GPa

infinite, which is impossible. Thus, because a finite magnetic field is created, it must mean that the superconductor has some finite conduction, despite having zero resistance. This led to the prediction of type-I and type-II superconductors [3], [4], development of the London constitutive equations [33], [49], the Ginzburg-Landau theory [3], [4], [33], [50], [51], and eventually the Bardeen-Cooper-Schrieffer (BCS) theory of superconductivity [34], [35].

The BCS theory of superconductivity was perhaps one of the biggest breakthroughs in superconductivity research. While, in its original state, it cannot directly explain HTS materials [34], [35], [44], the exact mechanism for which remains a mystery to this day, it is perhaps one of the most-successful microscopic theories of superconductivity.

The basic BCS theory of superconductivity posits that, when a material's temperature is sufficiently low enough, all valence energy bands of the material are full. Thus, any electrons added must sit in the *Fermi sea*, which is the collection of electrons in the conduction bands. If the energy of the system is low enough, then mechanical vibrations of the crystal lattices, quasiparticles called *phonons*, are still present, but are also very low energy. These phonons, which are bosonic in nature, interact with electrons, which are fermionic (and thus follow the Pauli exclusion principle by nature) with spin-1/2. However, when these phonons interact with two electrons, it is able to overcome Coulomb repulsion and instead couples them together, treating two sufficiently-close electrons as though they were a single spin-1 boson,

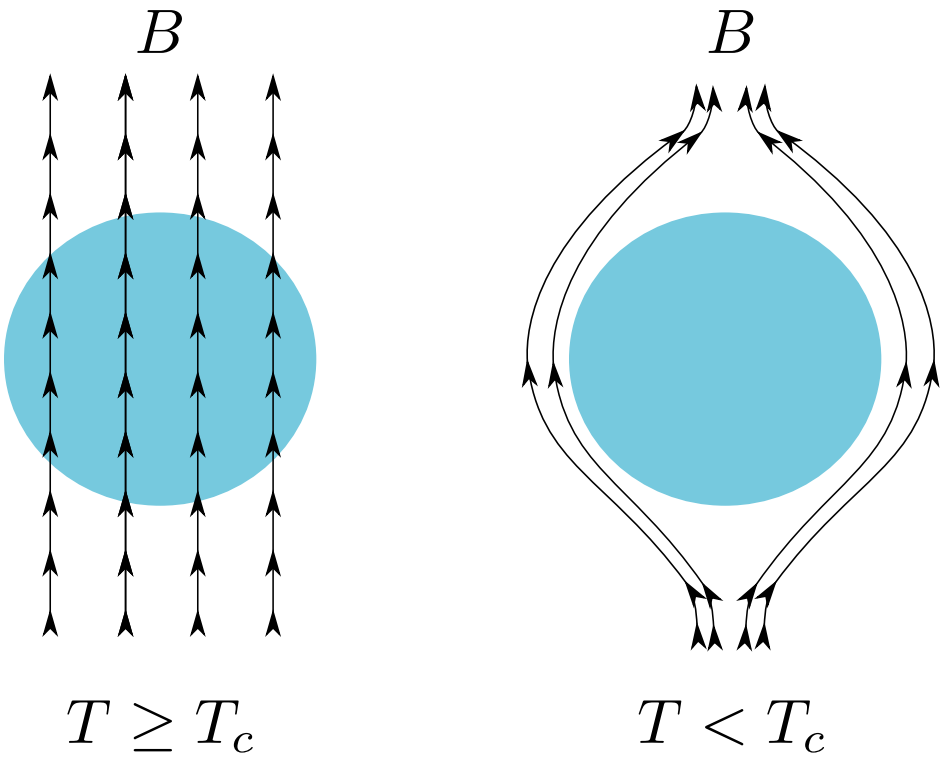

Figure 2.1. The Meissner effect on a type-I superconductor, as demonstrated with a round object. The lines of flux, when temperature $T \geq T_c$, pass through the object and, when $T < T_c$, pass around the object, completely expelled.

as illustrated in Fig. 2.2. This phonon-coupled paired-electron psuedoparticle is called a *Cooper pair*, and, because it acts as as boson, no longer follows the Pauli exclusion principle. As such, all similar Cooper pairs can occupy the same quantum states, no longer limited by their fermionic nature. This allows as many Cooper pairs to exist on any particular crystal lattice site as desired, no longer prohibited from site-to-site hopping to sites already occupied, per the Hubbard model of spin site-hopping [33], [52]. This unlimited hopping capability is what permits a zero-resistance conduction of electrons [3], [4], [33]–[36]. How quickly or easily pairs can perform this site-hopping is what leads to the finite conductivity.

Bardeen, Cooper, and Schrieffer were also able to predict the other phenomenon seen in superconduction (such as the Meissner effect, various thermodynamic properties, finite conduction, critical currents, critical magnetic fields, type-I and -II superconductors, *et cetera*), but also predicted an upper limit to superconductor critical temperatures near 30 K, as phonon coupling could not overcome thermal vibrational modes above this point [3], [4],

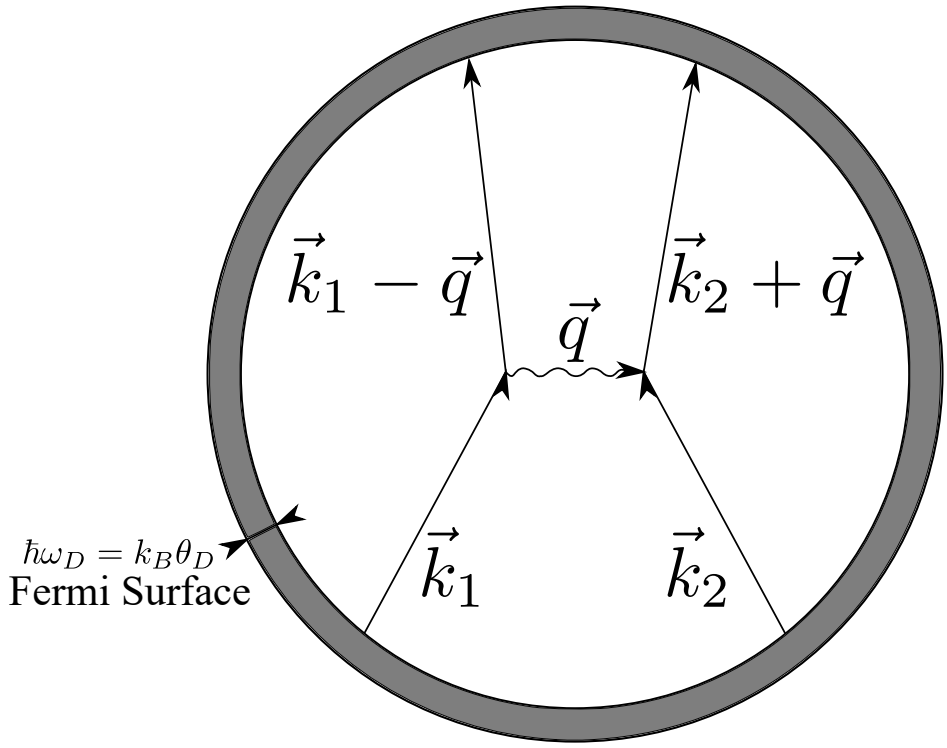

Figure 2.2. A simple illustration of a Cooper pair, where $\vec{k}_{1,2}$ are the momentums of electrons "1" and "2," respectively, in the Fermi surface with a maximum energy separation of $\hbar\omega_D = k_B\theta_D$, where θ_D is the Debye temperature and ω_D is the Debye frequency. The interaction with the phonon is represented by the momentum exchange $\vec{q}$.

[33]–[36]. Obviously, "high-T_c" superconductors *do* exist, which indicates that the BCS theory may be incomplete. Considering the success it has had everywhere else, and how HTS materials *do*, for the most part, still follow the BCS theory, physicists are inclined to believe that there must be some other kind of bosonic coupling between electrons in HTS Cooper pairs, the mechanism for which remains elusive even today.

In 1962, after some unusual results from experiments from nanoscale superconductor-insulator-superconductor (SIS) junctions where the presence of currents in the junctions was detected while no electric potential was applied, B.D. Josephson hypothesized that this was the result of Cooper pairs forming across the junctions, despite the physical separation, as long as the gap was less than the coherence length, ξ, of the superconductor. If this were the case, then the Schrödinger equation for this pair could be written in such a way that pair

tunneling probability across the junction was nonzero, even if the potential difference *was* zero. A nonzero tunneling probability indicated that it was possible that these quasiparticles would spontaneously cross the junction via a phenomenon later denoted *Giaever tunneling* [53]–[55]. If enough crossed the junction within a certain amount of time, it could constitute a noticeable amount of current. This *supercurrent* exists as a noise current when $V = 0$ with a current density $J = J_c \sin\varphi$, where φ is the momentum phase difference between the electrons in the pair (not to be confused with ϕ, which is typically magnetic flux or an angle). This phenomenon is, accordingly, called the *Josephson effect* [3], [4], [33], [36], [56], [57], and while many were initially dubious about the effect for some time, it was verified a year later [54], [58], and later discovered in superfluid helium [59].

Now, if the potential across the junction, now called a *Josephson junction*, was nonzero, then the momentum phase difference is easily predicted by:

$$\frac{\partial\varphi}{\partial t} = \frac{2e}{\hbar}V \tag{2.1}$$

If V is constant, then $\varphi(t) = \frac{2e}{\hbar}Vt = \frac{2\pi V}{\Phi_0}t$ (where $\frac{\Phi_0 \equiv 2\pi\hbar}{2e}$ is the *single flux quanta*), and $J(t) = J_c \sin\varphi(t)$. What this shows is that a DC voltage gives rise to an alternating current, at a conversion rate of 483.6 GHz per millivolt, making an ideal JJ a perfect gigahertz-level voltage-controlled-oscillator. This is known as the *AC-effect*, and is foundational for the motivation for this research.

Thus far, there have been quite a number of fabrication methodologies and applications for JJs using both original LTS and HTS junctions. Originally, superconductors and JJs were typically fabricated using LTS materials and layered structures, such as layered Nb-AlO_x-Nb LTS junctions [1], [3], [4], [36], [60], and recently superconduction had been discovered in bilayer graphene [61], [62]. However, extensive research has been put into developing HTS junctions, typically made of YBCO and utilizing a different form of junction called a *grain-boundary junction*, wherein the internal grain defects of the material, upon being deposited on its substrate, themselves form junctions [5], [21], [22], [25], [63]–[69]. This effect can be intentionally engineered or done unintentionally (which makes certain forms of deposition challenging). Another method is to create a variable-thickness-bridge (VTB)

trench junction [70]. Because ξ for HTS materials is typically an order of magnitude lower than ξ for LTS ones, these junctions are extremely challenging to manufacture, thus why they are only a more recently-viable option. Applications of these HTS junctions are thus part of the motivation for this research.

2.2 Semiconducting Devices and Nanotechnology

As Moore's Law rapidly approaches its end, the search for smaller, faster, and lower-power technologies has rapidly accelerated. Even though process node names have not reflected physical geometry since the 90s [71], technologies *equivalent to* sub-65nm processes have been developed, including, but not limited to, FinFET technologies [72], [73], of which currently-active and widely-used processes include Intel's 14 nm process [74], Samsung's 7 nm process [75], and TSMC's 7 nm process [76], each of which is on the order of roughly 50 nm in scale, give or take 20 nm; TFET devices [77]–[81]; single-electron transistors (SETs) [82]–[84]; high-mobility transistors (HEMT), like GaN, GaAs, and many other III-V materials [85]–[97]; and even superconducting transistors [19], [97], [98]. Each has its benefits and issues, as each attempts to focus on one particular issue over another (e.g.: power versus speed versus transistor density). There are a few types in particular, however, that attempt to focus on all three major issues simultaneously: carbon nanotube (CNT)-based or graphene-based transistors, which are a type of tunneling HEMT [79], [80], [99]. These kinds of devices make use of the phenomenal electrical properties of these various allotropes of carbon.

Semi-recently-discovered single-layer graphene is a material consisting of a 2D lattice of carbon atoms [31], [32], [100]. Because of its regular shape and nearly-perfect 2D properties, it and CNTs exhibit ballistic transport up to a length of 16 μm [101] and have, in certain conditions, phenomenal conductivity – up to over six times the conductivity of copper [102], [103]. Recently, however, it was discovered that these materials, in an external electric field, could also exhibit semiconducting properties [71], [104], [105], despite zero-band-gap properties (called *Dirac points* in band diagrams). This led to the development of CNTFETs and their 2D cousin, GFETs. However, due to the intrinsic lack of bandgap, these devices had some notable issues, such as scaling problems, insufficient on-to-off-current ratios, insufficient

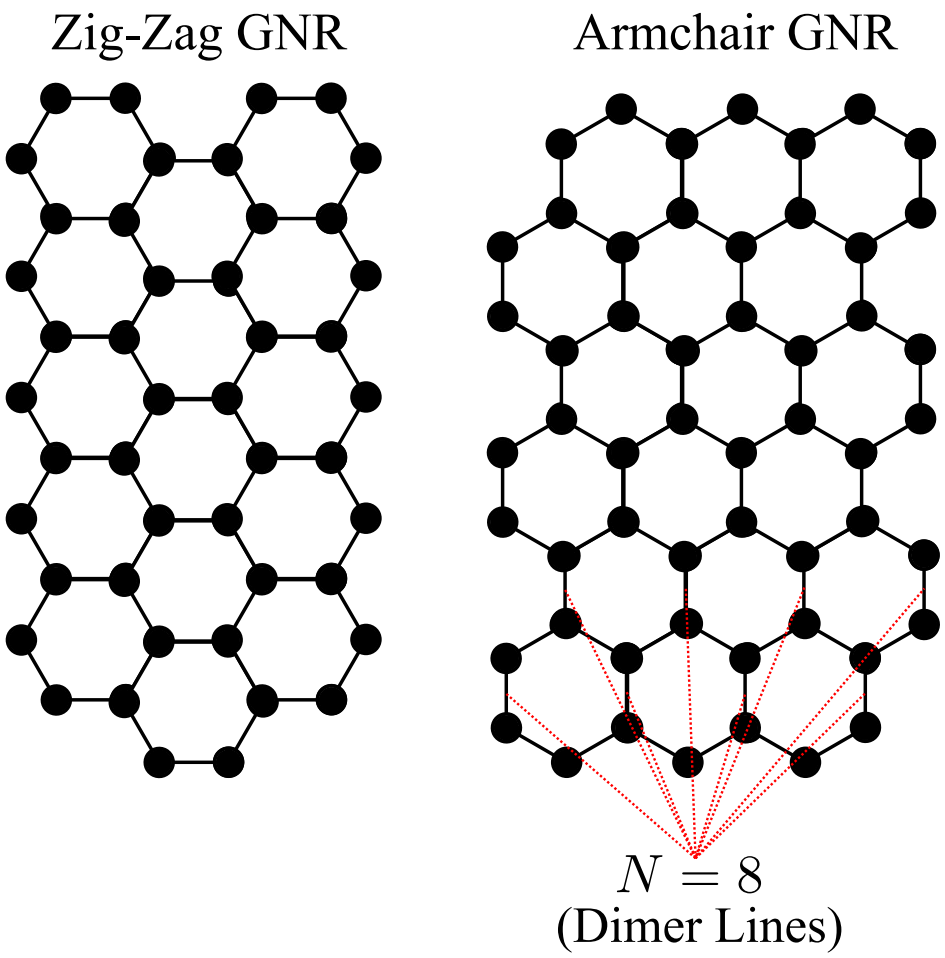

Figure 2.3. An illustration of conducting zig-zag GNR (ZZGNR – left) and semiconducting armchair GNR (AGNR – right) with $N = 8$ dimer lines (annotated).

subthreshold swings, conductivity issues, and other problems [79], [80], [106]–[108]. Thus, some kind of resolution to these particular issues was required.

In 1996, a new form of graphene was introduced, called the *graphene nanoribbon*, which exist in two types: the *zig-zag* GNR (ZZGNR), and the *armchair* GNR (AGNR), as illustrated in Fig. 2.3. Prior studies of graphene had focused primarily on graphene sheet, the behavior of which can be approximated by assuming, relative to the size of a single carbon atom site, the sheet is periodic and infinite in all directions. However, by making a ribbon – a sheet of graphene of finite width and length, new solid-state and electromagnetic properties arise. While ZZGNRs remain extremely conductive, maintaining the zero-band-gap

and Dirac points in the energy band structure, AGNRs demonstrate drastically different behavior: they are semiconducting, with a bandgap size dependent on the number of dimer lines (parallel lines of carbon atom pairs forming a Bravais lattice unit cell across the width) [109]–[111]. By choosing the width and lengths of AGNRs, the bandgap and semiconducting properties of graphene can be engineered to suit the needs of a system [88]. More recent research with AGNRs have confirmed the AGNR energy band structure [112], found discrete-step conductivity if the GNRs are edge-terminated with hydrogen [113], determined that the bandgap can also be better-controlled with hydrogen-termination [114], discovered interesting conduction properties in buckled AGNRs [115], found twisting/3D-shape formation of the GNRs with interesting electromechanical properties [106], and shown long-distance ballistic charge transport in GNRs [101], [116].

Despite their discovery being in the late-90s, it was almost 15 years between the discovery and the potential application of GNRs for transistors. This is very likely due to how GNRs could not be precisely produced until 2009, when two groups independently developed ways to unzip carbon nanotubes: one via action of $KMnO_4$ and H_2SO_4 on multi-walled CNTs [117], and the other by plasma by etching [118]. Other methods have been developed since then, either for unzipping [119], [120], direct growth [121], [122], etching [123], or by a bottom-up approach and CVD [124], [125], which may include doping as well.

The first theoretical device that could be considered a proto-GNR transistor was developed in 2007 to study quantum capacitances in GNRs. This device consisted of a GNR-on-insulator, with a top- and optional bottom-gate structure. This study found, as expected, that the GNR C-V characteristics were strongly-dependent on edge shape [126]. For $N = 41$ and $N = 42$ AGNR devices, with lengths of approximately 5 nm and a dielectric constant of the 2 nm-thick insulator $\epsilon_r = 16$, the resulting simulated capacitances were quite small: on the order of picofarads per centimeter, corresponding to roughly tenths of attofarads per nanometer, dependent on gate voltage. The results from this work demonstrate further that GNRs are good potential candidates for transistor channel materials.

Around the same time, several papers came out discussing the possibilities [127] and simulations for GNRFETs (or proto-GNRFETs) [128]–[131], especially as compared to CNTFETs, which had a number of issues. Of these, the Stanford models were, perhaps, most influen-

tial in the initial stages of research, as they were some of the first physically-implemented room-temperature sub-10 nm GNRFETs [130], [131]. However, the first formal physics-based simulation model was developed initially in 2011 by Unluer, *et al.* [132], and then a SPICE-compatible physics model in 2013 by Chen, *et al.* [30] for MOS-like GNRFETs, which included doping properties, which, as it turns out, in GNRFETs, mobilities μ_e and μ_p are nearly the same. This was followed by a Schottky-barrier-type GNRFET (SBGNRFET) the following year [28]. Both models have been refined since then [31], [32]. A comparison of these devices was released the same year, discussing the devices' capabilities, and formally classifying them as a type of TFET [80]. These models have proven to be remarkably-accurate to physical versions [27], [28], [30]–[32], and the resulting simulation models, available on Nanohub [29], have been widely-used. These devices are phenomenal, and may have many applications, from high-speed digital [27], [28], [30]–[32], to low-temperature, low-power small-signal analog amplification [23], [24].

3. DEVICE PHYSICS, MODELING, AND OPERATION

3.1 Superconductive Devices

3.1.1 Josephson Junctions

The ideal Josephson junction has a very simple equivalent circuit consisting of a phase-difference-controlled current source, but there are also several non-ideal effects that need to be considered. First is the critical current density, J_c, above which the superconducting device acts like a normal conductor and has an effective *normal resistance*, R_N. In the JJ, the potential energy required to bring the junction to this point is referred to as the *(sub)gap potential* or *quasiparticle tunneling gap*, Δ. The corresponding subgap voltage is $V_{SG} = 2\Delta/e$. Ideally, R_N can also be calculated by:

$$R_N = \frac{\pi}{4}\frac{V_{SG}}{I_c} = \frac{\pi}{2}\frac{\Delta}{eI_c} \tag{3.1}$$

The actual value of R_N varies from junction to junction, even between junctions of the same construction. For JJs, the parameter $\frac{\pi}{4}V_{SG} = I_c R_N$ is frequently given instead, and either J_c or I_c is specified separately. From this, the JJs' specific Δ and R_N may be extracted [3], [70].

Δ itself is an interesting parameter, resulting from the BCS theory of superconductivity. Its value is typically around 1 meV, and describes the energy difference between particles in a Cooper pair. Specifically, 2Δ can be seen as the binding energy of the electron pair. If the energy difference between two electrons exceeds Δ, then the two electrons cannot couple. This observation is what led to the initial prediction by Bardeen, Cooper, and Schrieffer for the maximum critical temperature a superconductor could hold [3], [4], [33]–[35].

The second major non-ideal feature of the JJ is the *subgap resistance*, R_{SG}, which exists in voltage-driven JJs and describes the quasiparticle tunneling due to typical conduction, rather than the Josephson effect. It may be considered to be infinite, generally, but it may still occur in certain conduction models for the JJ [3], [25], [58]. It may also be referred to

as the *subgap conductance*, G_{SG}, which is effectively zero. Combined with R_N, the complete conduction model for a JJ can be written as:

$$G(V) = \begin{cases} G_{SG} = R_{SG}^{-1} & |V| < V_{SG} \\ G_N = R_N^{-1} & |V| \geq V_{SG} \end{cases} \tag{3.2}$$

Finally, because JJs frequently consist of two parallel superconducting plates, the model must also include a capacitance. Sometimes an inductance is considered as well, but it depends on the model and physical junction size. How all these non-ideal parameters affect the junction are summarized with Stewart-McCumber parameter [3], [133], [134]:

$$\beta_c \equiv \frac{\omega_c}{\alpha} = \frac{\omega_c C}{G} = \frac{2e}{\hbar}\frac{I_c}{G_N^2}C \tag{3.3}$$

A junction is considered over- or under-damped based on β_c ($\beta_c < 1$ corresponding to over-damped and $\beta_c > 1$ corresponding to under-damped), which functions identically to a harmonic oscillator's Q-factor.

The simplest model to incorporate all these parameters is called the *resistive capacitively-shunted junction* (RCSJ) model, as seen in Fig. 3.1 [3], [4], [25], [55]. While it does not natively incorporate electromagnetic effects (such as the DC effect), it is sufficiently for simulation purposes. There are some non-physical additions to the model that are introduced to maintain accuracy and to allow the simulator to work with smooth, rather than piecewise or otherwise non-differentiable, equations – especially with the subgap conduction model presented in Eq. 3.2. Given $G(V) \equiv R(V)^{-1}$, the subgap resistance R_{SG}, normal resistance R_N, and the subgap potential Δ, then the conduction model can be smoothly approximated by:

$$R(V) \approx R_{SG} + \frac{R_N - R_{SG}}{1 + \exp\left(-k\left[\left(\frac{eV}{2\Delta}\right)^2 - 1\right]\right)} \tag{3.4}$$

The parameter k is an arbitrarily-large positive constant ($k \to \infty$) to achieve the sharpness of the piecewise model. The electron charge term, e, may be dropped if Δ is in units of electron-volts rather than Joules. This is implemented in the SPICE and Verilog-A models

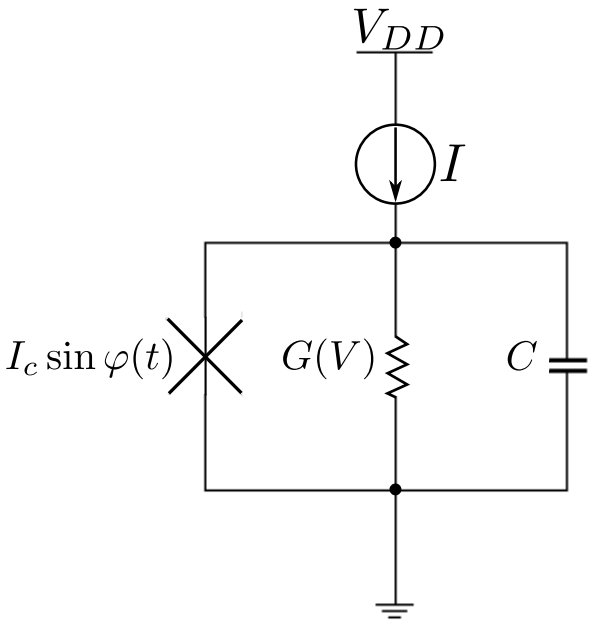

Figure 3.1. A schematic-level illustration of the RCSJ Josephson junction model. It consists of an ideal junction $I(t) = I_c \sin \varphi(t)$, a voltage-dependent conductance $G(V)$, and a capacitance C.

utilized here, originally developed and presented in Ref. [23], with an updated version of them given in Appendix A. The default values for the model are $R_N = 17\ \Omega$, $R_{SG}/R_N = 20$, $\Delta = 1.08$ meV, $I_c = 100\,\mu$A, and $k = 100$ for the SPICE model, based on example numbers given in Ref. [3] for a Nb/AlOx/Nb junction.

The Verilog-A model is slightly different, primarily based on a variation of the Nb junctions: $R_N = 10.7\ \Omega$ (calculated from I_c and Δ), $R_{SG}/R_N = 40$, $\Delta = 1.5$ meV, $I_c = 220\,\mu$A, and $k = 100$. For both, the junction capacitance is set to 18 fF. The SPICE model specifies, as parameters, I_c, R_N, the subgap ratio, and C, while the Verilog-A model specifies, as parameters, I_c, Δ, the subgap ratio, and C. They are equivalent, though the Verilog-A model is more intuitively-constructed (as it was designed sometime after the initial SPICE model). These SPICE models assume an ideally-calculated R_N, rather than an empirical R_N.

Inductances can also be included, but are typically present only in large-scale JJ models or SQUIDs. This inductance would be included at the input and output nodes of the junction, and are called the *Josephson inductance*, $L_J = \Phi_0/2\pi I_c$ [3].

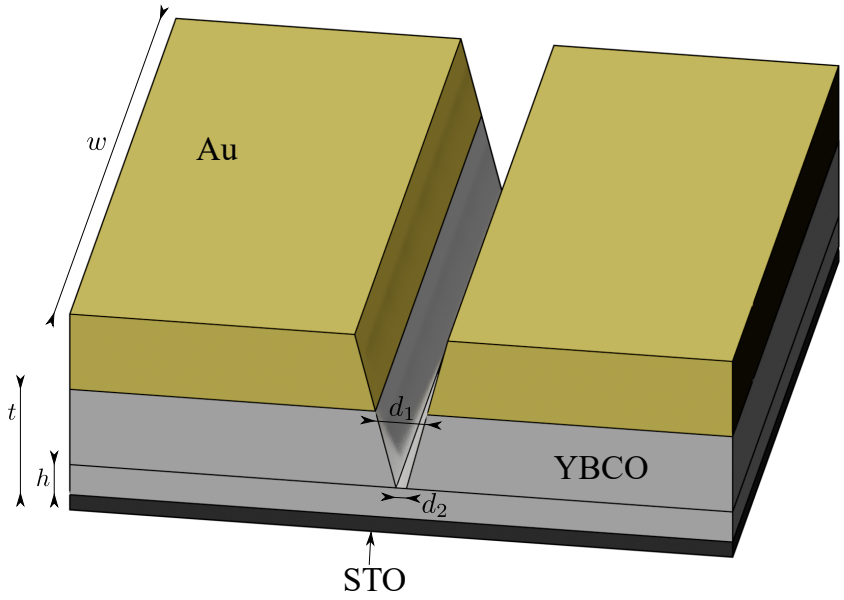

Figure 3.2. A diagram of the YBCO Josephson junction using the VTB model, as implemented in Ref. [70]. The substrate originally used was STO, but other substrates may potentially also be utilized, as discussed in Chapter 4.1.

The model parameters for a HTS JJ are a little more complicated to determine. Using the JJ developed in Ref. [70], which consists of an etched trench in gold-coated YBCO-on-STO, the model parameters are calculated by the width of the junction, w, the thickness of the YBCO, t, the unetched depth of the YBCO, h, the top trench width, d_1, and the bottom trench width, d_2, along with J_c, I_cR_N, and the subgap ratio, SGR. A diagram of the VTB model, as implemented in Ref. [70], is shown in Fig. 3.2.

For pure YBCO, $\Delta \approx 16.7$ meV (equivalent to $I_cR_N = 6.55$ mV) [135] and $J_c \approx 2.75\,\mathrm{MA \cdot cm^{-2}}$ [136], though for this junction, if $h = 80$ nm, $w = 4$ μm, $d_1 = 50$ nm, $d_2 \leq 16$ nm, and $t = 170$ nm, then Ref. [70] reports a decrease in critical temperature to 80 K and subdued $J_c = 2\,\mathrm{MA \cdot cm^{-2}}$ and $I_cR_N = 50$ μV (for $\Delta = 0.127$ meV, $I_c \approx 100$ μA

and $R_N \approx 0.5\,\Omega$). With these parameters specified, the previous models could be fit to this junction, with $SGR \approx 10$, $I_c = wtJ_c$, and capacitance approximated geometrically:

$$\tan\alpha = \left| \frac{4(t-h)\,(d_1 - d_2)}{(d_1 - d_2)^2 - 4(t-h)^2} \right| \tag{3.5a}$$

$$C \approx \frac{\epsilon_0 \epsilon_r w}{\tan\alpha} \ln\frac{d_1}{d_2} \tag{3.5b}$$

For the parameters presented in Ref. [70], $C \approx 91$ aF, assuming no insulating material with $\epsilon_r > 1$ is layered on top of the VTB junction.

A similar structure was developed recently to create a nanoscale SQUID utilizing focused helium ion beam (FHIB) lithography on YBCO, with controllable edge lengths between 10 and 900 nm, though the junctions in the SQUIDs themselves have a constant 300 nm gap. For these devices, surprisingly-high normal resistances between 25 and 32 Ω were found, increasing as the SQUID size decreased. Larger SQUIDs had higher I_c, but with a trade-off of higher inductance as well. The maximum SQUID voltage achieved was reported as 0.8 mV and 0.5 mV for a 50 nm and 10 nm SQUID, respectively. Unfortunately for these SQUIDs, their critical temperatures are still lower than that of normal YBCO, with the critical current dropping from 50 μA to 5 μA over a temperature range of 4.2 K to 52 K [137].

Despite this, however, the secondary junction layout is certainly a promising method and architecture that may be able to reduce the size of these devices further in the future, if the critical temperatures and currents can be reliably increased.

3.1.2 Wires and Striplines

If a system utilizing superconductive striplines operates at frequencies less than ~1 THz, then the superconductors do not exhibit dispersion effects. In HTS materials, this frequency is even higher, to the benefit of this research [4]. What this indicates is that the conduction model is relatively simple for an EHF superconductor stripline, compared to a model for the same device above its gap frequency ($\omega_g = 2\Delta/\hbar$), where it acts more like a conductor, rather than a superconductor. Despite this, the conduction model is still complicated. The

simplest model of the surface conduction in a superconducting film is based on the London penetration depth, λ_L (the equivalent of *skin depth*), and the film thickness, t:

$$Z_s = \mathrm{j}\omega\mu_0\lambda_L(T)\coth\left(\frac{t}{\lambda_L(T)}\right) \tag{3.6a}$$

$$\zeta = 1 - \frac{t/\lambda_L(T)}{2\coth\left(t/\lambda_L(T)\right)} + \sqrt{1 + \left[\frac{t/\lambda_L(T)}{2\coth\left(t/\lambda_L(T)\right)}\right]^2} \tag{3.6b}$$

$$Z_s^{FT} = \zeta Z_s \tag{3.6c}$$

Here, Z_s and Z_s^{FT} are the characteristic surface impedance and finite-thickness surface impedance, respectively, and ζ is a measure of the ratio of the magnetic energy stored in the superconducting material. This assumes $w/h < 7$, where w is the trace width and h is the separation distance between the microstrip and its corresponding ground plane [138], as illustrated by Fig. 3.3. In the thick metalization ($t \gg \lambda_L$) range, this simplifies significantly to $Z_s = \mathrm{j}\omega_D\mu_0\lambda_L(T)$.

An alternative for Z_s that expresses the total surface impedance per unit length is [3], [4]:

$$\begin{aligned} Z_s/l &= R_s/l + \mathrm{j}\omega L_s/l \\ &= \frac{\omega^2\mu_0^2\lambda_L^3(T)\sigma_n}{2w}\left(\frac{T}{T_c}\right)^4 + \mathrm{j}\omega\frac{\mu_0\left(h + 2\lambda_L(T)\right)}{w} \end{aligned} \tag{3.7}$$

L_s is sometimes referred to as the "kinetic inductance." This particular model assumes thick metalization, and can be corrected by incorporating the $\coth(t/\lambda_L(T))$ term:

$$L_s/l = \mathrm{j}\omega\frac{\mu_0\left(h + 2\lambda_L(T)\coth\left(\frac{t}{\lambda_L(T)}\right)\right)}{w} \tag{3.8}$$

The added factor of σ_n is the normal conductivity of the superconducting medium [3], [4]. For this reason, T is frequently chosen to be $T \leq T_c/2$ [4]. For $t = 30$ nm, normal conductivities at $T = 90K$ have been reported to be as high as $\sigma_n \approx 1.5 \times 10^6\,\mathrm{S}\cdot\mathrm{m}^{-1}$, with

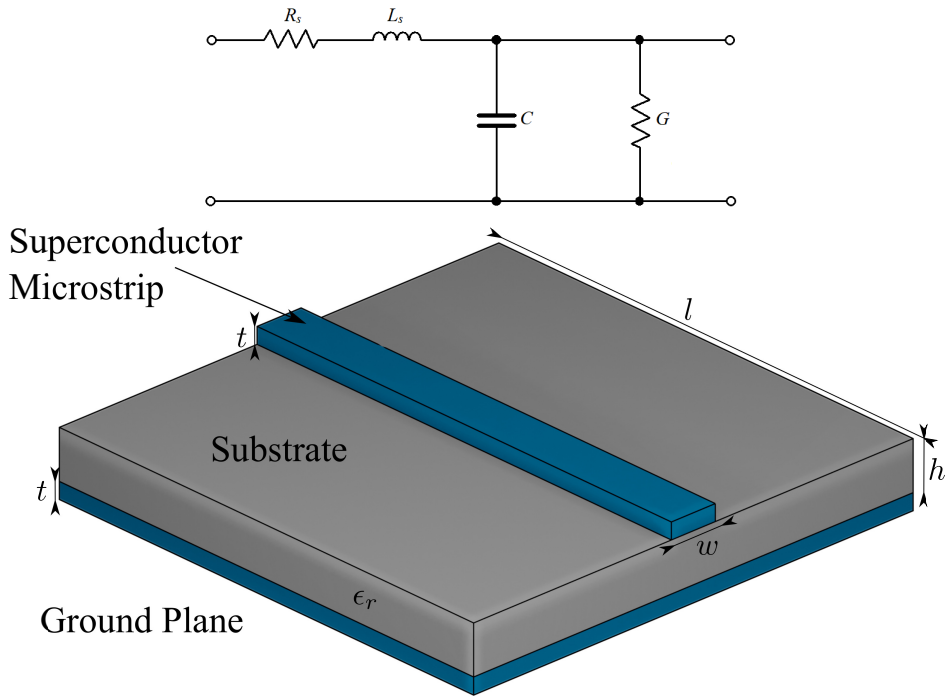

Figure 3.3. The superconductor stripline 3D model (bottom) with its equivalent circuit (top).

thicker films having even higher conductivity ($t = 280$ nm has $\sigma_n \approx 2 \times 10^6\,\mathrm{S \cdot m^{-1}}$). At $T = 77$ K, it was measured to be $\sigma_n \approx 10^6\,\mathrm{S \cdot m^{-1}}$, probed at 28.2 GHz [139].

The temperature dependence of λ_L is explicitly expressed in Eq. 3.7, following similarly to the temperature dependence on normal conduction [4]:

$$\lambda_L(T) = \lambda_L(0)\left[1 - \left(\frac{T}{T_c}\right)^4\right]^{-\frac{1}{2}} \tag{3.9}$$

This is exceptionally-important to remember when utilizing these equations, as near-T_c temperatures can greatly increase the London penetration depth, reducing the stripline's efficiency. The value $\lambda_L(0)$ is what is reported as λ_L, frequently. At $T = 77$ K, λ_L is between 81 and 94 nm for YBCO, up to roughly 150 nm, taking $T_c = 93.7$ K [140]. Looking at the data presented in Ref. [140], $\lambda_L(0) \approx 60$ nm can be determined ($\Delta\lambda_L(77) \approx 90$ nm, $\lambda_L(0)^2/\lambda_L(77)^2 \approx 0.16$). This value for $\lambda_L(0)$ is used for all simulations.

The capacitance, C, can be calculated normally, as discussed in Chapter 4.3, and the loss conductance, G, can be set to $G = 0$, as the substrate is usually insulating [3].

Appendix B.1 provides a MATLAB script that can be used to calculate and export these surface impedance values for use in electromagnetic simulation software, such as CST Studio or Ansys HFSS.

3.2 Nanotechnology Devices

3.2.1 The GNRFET Model

Model Background

The GNRFET SPICE model utilized here is one developed by the University of Illinois at Urbana-Champaign (UIUC) seven years ago (available at NanoHub: [29]) , which remains one of the most thorough models for the GNRFET available for SPICE simulation [27]–[30]. The robustness of the model is demonstrated, in particular, by how many other simulation methods for this model have arisen independently of the UIUC team's work [31], [32], [80], [132], [141]–[148]. The model, as seen in Fig. 3.4, looks simple, but is exceptionally complex. It utilizes non-equilibrium Green's functions (NEGF) formalism to solve the Poisson equations associated with the quantum states of graphene nanoribbons in order to properly simulate the electron transition probabilities and the associated currents. A wide number of physical effects are incorporated, such as the valence/conduction band calculations (in the form of a lookup table), edge-size dependencies, edge roughness, and parasitic effects (especially as contributed by capacitances). These parasitics themselves are non-static; their values need to be calculated at every time step to allow for proper simulation due to their charge- and voltage-dependency at any given moment. The currents in the device are calculated from quantum-mechanical DOS models, coupled with tunneling probabilities and charge mobility. Even the channel voltage, V_{CH}, is calculated with every step, in order to properly model the channel fields, and is based on two charge-dependent, potential-dependent effective current supplies. While this model was primarily based on a single-gated GNRFET on silicon, it is sufficiently flexible as to permit different substrates and gate insulators. It is also able to account for different oxide thicknesses (t_{ox}), channel

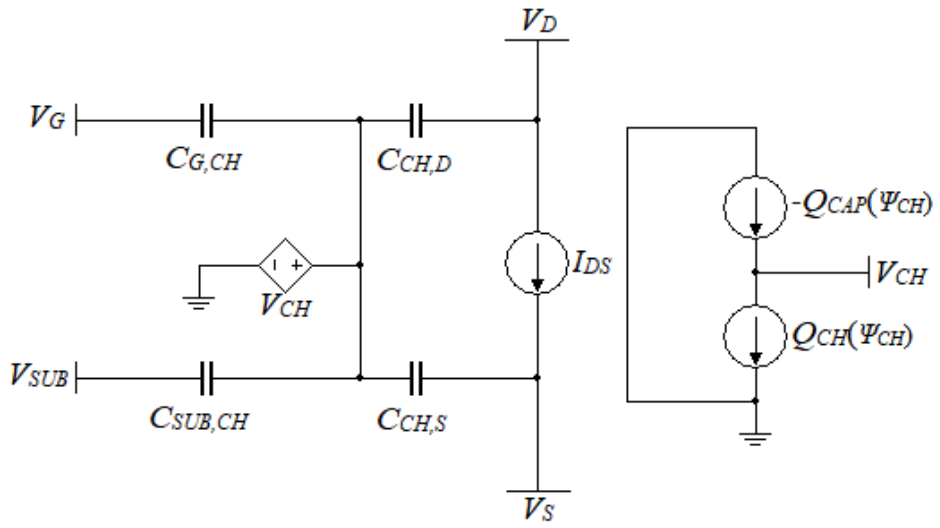

Figure 3.4. The equivalent-circuit model of the GNRFET as described in Refs. [29], [30].

widths (W_{ch} derived from N) and channel lengths (L), plus variable ribbon counts in the channel (n_{rib}).

As discussed, the device model suggests enormously-high frequency capabilities, with attofarad-level capacitances leading to predicted and measured transition frequencies in the THz range [32], [149], [150], and operational frequencies in the EHF range.

Effective Capacitances

The model for the GNRFET includes many parasitics built into the model, including several charge-dependent, geometry-dependent, and quantum-effect-dependent capacitances and state-dependent conductivities, dependent voltage sources, and current sources. Such effects include geometric capacitances, quantum capacitance, band-to-band (BTB) tunneling, fringe field effects, and variable channel density-of-states (DOS) due to the carbon lattice [27]–[32]. These work together to yield effective parasitic capacitances whose values vary with external parameters. In order to appropriately approximate these parasitics, a mean-field-approximation-like approach can yield satisfactory results to predict the overall behavior of the GNRFET model.

As discussed in Ch. 2, the basic GNRFET is constructed by several AGNRs in parallel on an insulator and connected at the ends to the drain/source terminals. On top of the channel

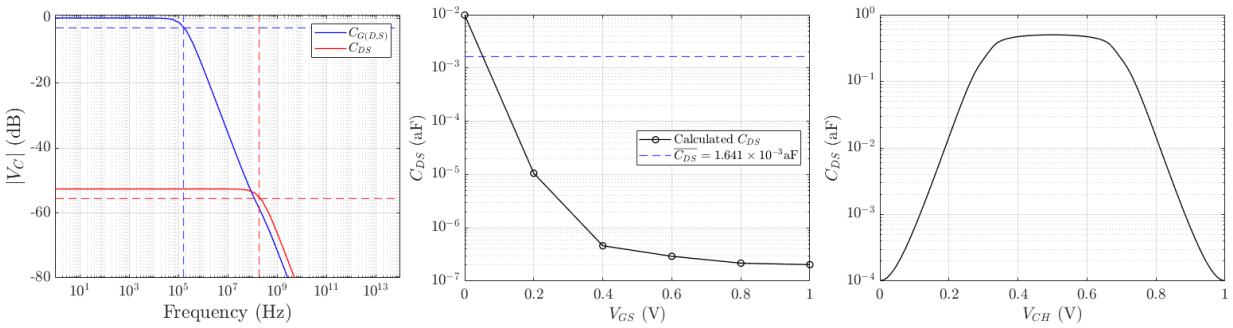

Figure 3.5. Simulated outputs used to determine capacitor values. The left image is the magnitude of the output of the low-pass filter, with resulting corner frequencies of 159 kHz ($C_{G(D,S)}$) and 192 MHz (C_{DS}). The middle image is the result of simulated Elmore delay to determine C_{DS}, with a mean simulated C_{DS} of 1.6×10^{-3} aF. The right image is the calculation of C_{DS} based on channel capacitances and terminal voltages.

is a layer of insulator and the gate terminal. Many forms also mirror this on the other side of the substrate to form a dual-gate transistor. The circuit model for the GNRFET from Refs. [27]–[30], [151], as shown in Fig. 3.4, makes the multiple charge-dependent capacitors, which depend on channel potential V_{CH}, obvious, and demonstrate that they are calculated from charge motion in the GNRs. This gives another equivalent capacitance from the existence of channel charges Q_{CH} and Q_{CAP} in Fig. 3.4. The literature estimates values for $C_{(G,SUB),CH}$ formed by the geometric gate/substrate capacitances and $C_{G(D,S)}$ based on fringe-field effects with empirically-fit equations [27], [29], [31], [32]. There is no closed-form solution for the charge or total capacitances for the effective body or channel capacitors. Instead, the SPICE model calculates the capacitances from their charge dependency over time. Fig. 3.5 shows the simulation results determining effective capacitances by three ways: by treating the system as a low-pass filter and finding the cutoff frequency, by utilizing Elmore delay over a range of V_{GS} [71], [99], and by calculating $C_{D,CH}$ and $C_{CH,S}$ utilizing the equations used in the SPICE model [27], [29], [151]. A phase-magnitude approach may not be accurate since phase variations demonstrate other sources of effective impedance that may become prevalent with high frequency large voltage swing.

Elmore delay was simulated by fixing V_{GS} and switching V_{DS} between 0 and 1 V, determining the propagation rising/falling delays with a given series resistance of 100 GΩ. By this

method, a mean C_{DS} was found to be on the order of 10^{-3} aF (though the geometric mean was much lower), and by using the channel-related capacitance calculations, it was found to potentially vary across four orders of magnitude. This makes it challenging to determine the "actual" value, though approximations of the channel capacitance yielded approximately 1.81^{-4} aF, while the low-pass method found it to be 8.31×10^{-3} aF. As can be seen, all values are exceptionally small, though the range is varied. Ultimately, the geometric mean of the values was used: 1.35×10^{-3} aF. Because of the way that delay values are both calculated via multiplicative operations ($f_{ci} \propto (RC_i)^{-1} \rightarrow f_c \propto (f_1 f_2 \cdots f_n)^{1/n} = \left[R\left(C_1 C_2 \cdots C_k\right)^{1/n}\right]^{-1}$), and utilized for low and high frequency cutoff as related to center frequency, the geometric mean is a better fit for capacitance values. From an intuitive perspective, a capacitance of this order is reasonable, as the channel is two-dimensional, so the effective capacitance is quite limited from a geometric view. Even from a charge density point of view, the overall capacitance is limited largely by available states in each carbon site. It is important to note that even if the C_{DS} simulation extrema are used, due to their comparative scale, the other capacitances in the system dominate the overall properties, such as gain, bandwidth, stability, and noise performances, as will be seen later with predicting the bandwidth of small-signal amplifier. This indicates that, even at high frequency where this feedback capacitor would potentially have a significant role, C_{DS} has minimal effect.

Using the high-frequency cutoff method associated with the low-pass filter once again, the simulated gate capacitance corner frequencies were both 159 kHz, so, using $R = 100\,\mathrm{G\Omega}$, the capacitances were both $C_{G(S,D)} = 9.99\,\mathrm{aF}$, though the predicted value of fringe-field $C_{G(S,D)}$ was closer to 2.18 aF, and $C_{(G,SUB),CH} = 2.04$ aF. This capacitance in series with calculated $C_{CH(S,D)}$ gives at most an increase in the predicted $C_{G(S,D)}$ by 0.982 aF, with a geometric mean of 0.136 aF increase over the range of V_{CH}, giving an approximate $C_{GS} \approx 2.31$ aF. This discrepancy was resolved by taking the geometric mean of the capacitances the same way that was done for C_{DS}, giving $C_{G(S,D)} = 4.81$ aF.

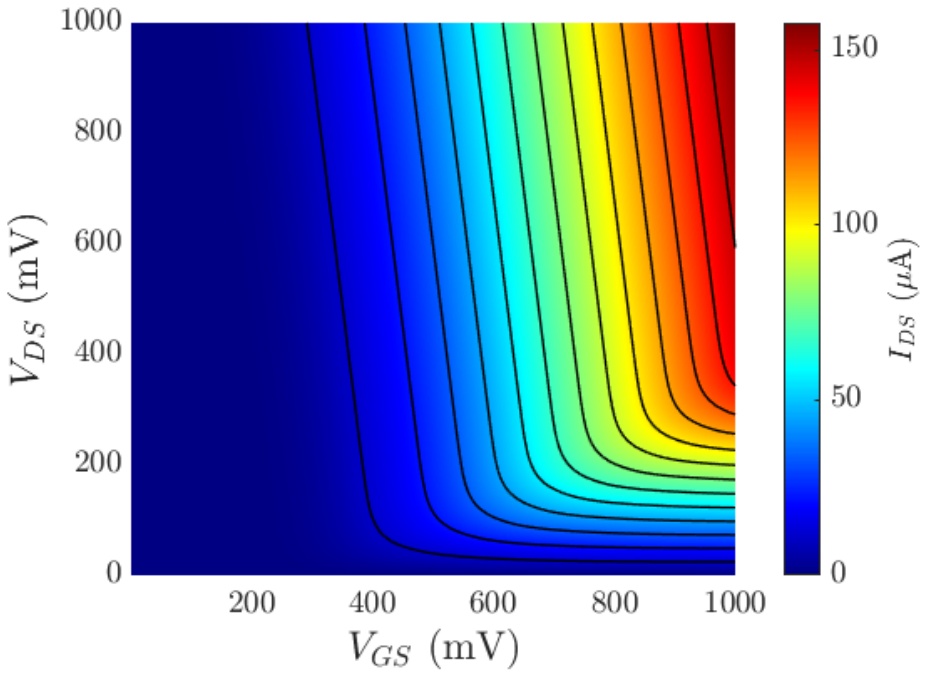

Figure 3.6. I-V Surface for I_{DS} as a function of V_{GS} and V_{DS}.

GNRFET Device Behavioral Curves

The GNRFET's DC parameters were simulated, and the AC parameters were predicted. V_{GS} and V_{DS} were both varied from 0 to 1 V. The surface seen in Fig. 3.6 shows the results of simulating I_{DS} as a function of V_{GS} and V_{DS}. The I-V curves follow the same curve patterns as a nonideal MOSFET, including a linear/ohmic region and saturation with a slight linear rise in current when V_{DS} increases due to channel-length modulation effects. Increasing V_{GS}, as expected, leads to a higher V_{DS} saturation voltage. Because the length of the channel is on the order of 15 nm [31], [32], the device exhibits channel-length-modulation effects, where, in saturation, raising V_{DS} slowly increases I_{DS} almost linearly. As can be seen in Fig. 3.7, the power consumption is also low, peaking at 151 μW for $V_{DS} = 1$ V and $I_{DS} = 151\,\mu$A. For the range of parameters used throughout this paper, however, the power consumption is limited to less than 70.3 μW per transistor.

Because temperature is typically a major factor in the operation of FET devices, the GNRFET was simulated over a wide temperature range of 90-450 K. On the high-temperature

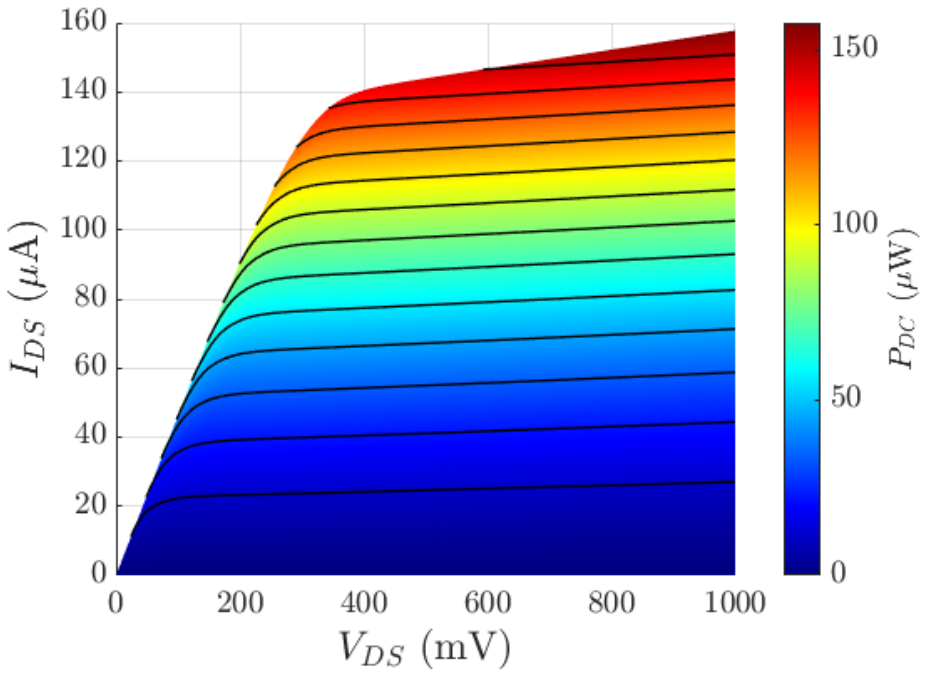

Figure 3.7. DC power consumption surface as a function of V_{DS} and I_{DS}. As can be seen, DC power consumption is quite low. In fact, for the range of values utilized here, the GNRFETs individually consume less than 50 μW of power.

side, Fig. 3.8 compares the operation at 300 K and 425 K, over varying V_{GS} (ranging from 0 V to 1 V in 100 mV increments). As can be seen, the difference between the drain-source currents at these two temperatures is very low, especially at saturation. The only major difference in operation is a degraded I_{off} at high temperature due to thermionic emission.

Over the low temperature range, Fig. 3.9 shows that for a given $V_{GS} = 300$ mV (past threshold), cryogenic temperatures impact the device operation, but not an extremely significantly. Conduction also degrades at low temperature. However, this may work to the device's advantage. Lowering the required current to reach the same operational point indicates lower DC power consumption. Meanwhile, normal devices, when operated at these temperatures (both low and high), may not function properly, if at all. Ref. [26] demonstrates similar thermal properties in a single-gated physically-implemented GNRFET on SiC, finding that not only does a GNRFET still operate at temperatures as low as 4 K, but the I_{on}/I_{off} ratio increases from 10^5 to 10^6, which is explained by the lack of thermionic

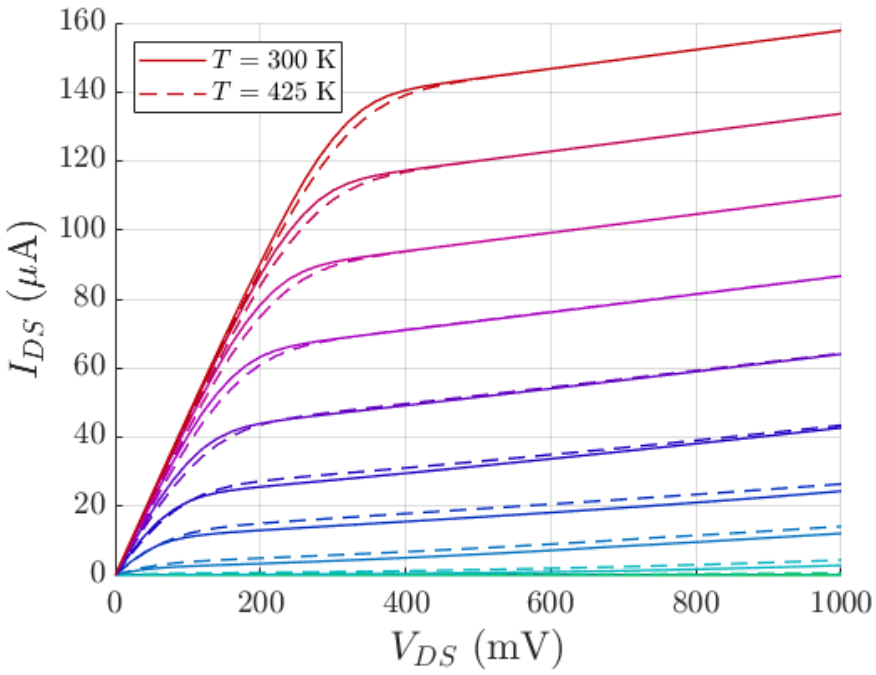

Figure 3.8. A comparison between I_{DS} at $T = 300$ K (solid) and $T = 425$ K (dashed), for varying V_{GS}. As can be seen, the difference is minimal between them. V_{GS} varies between 0 and 1 V with a step of 0.1 V. Increasing maximum curve height corresponds to increasing V_{GS}.

tunneling of electrons in the sub-threshold region. Other research has found that subthreshold swing is also largely temperature-independent between 5 and 40 K in a triple-gated GNRFET, starting at 47 mV/decade and increasing with temperature above that point. However, their reported I_{on}/I_{off} is not as high due to transistor scaling [152]. The reasons for these ultra-low temperatures chosen here are due in part to these devices' potential utility in deep-space or cryogenic applications, such as systems with superconducting devices such as in Refs. [23], [24] or other possible systems. Furthermore, because these devices have extremely low power consumption and graphene is an exceptional thermal conductor, exceeding 2000-4000 $\mathrm{W \cdot m^{-1} \cdot K^{-1}}$ for free-standing graphene (SiO_2-supported graphene is reduced to 600 $\mathrm{W \cdot m^{-1} \cdot K^{-1}}$) [153], the extended temperature range may have minimum effect on these devices.

The low dependence of operating point on temperature in a GNRFET is due to several factors. First, since the device's bandgap is direct (compared to the indirect bandgap of

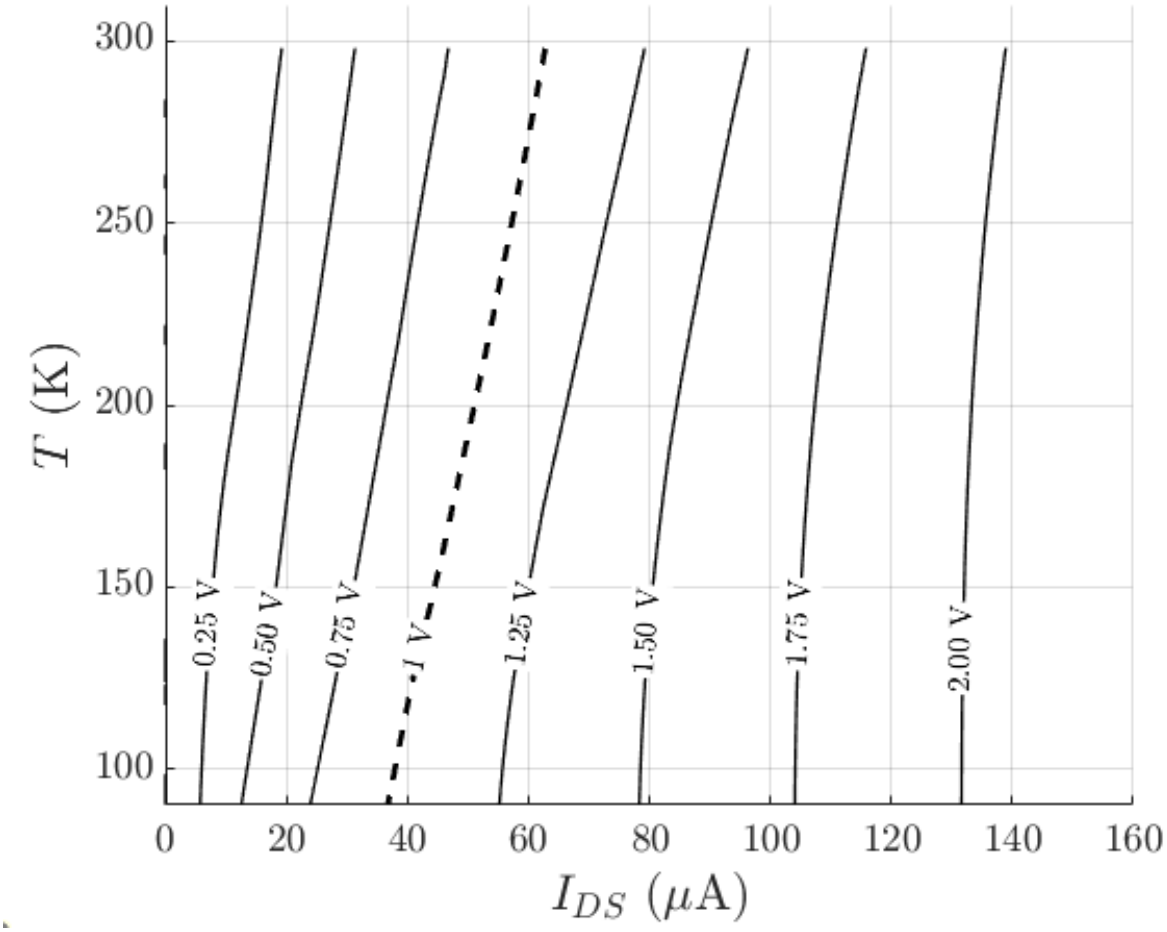

Figure 3.9. V_{DS} surface contours as I_{DS} varies from 0 to 160 μA and T varies from 90 K to 300 K, with V_{GS} fixed at 300 mV. The dashed line indicates the maximum permitted V_{DS}, indicating that, as temperature increases, the current required to reach that maximum value also increases by almost 20 μA, which also increases DC power consumption.

silicon-based devices) and controlled by the edge structure of the GNRs and dopant wells in the substrate, there is no thermal voltage necessary to allow electrons to tunnel to their conduction bands; the precise gap needed can be engineered into the material. Second, because transport is ballistic, the temperature will have very little effect on the motion of charge carriers; they are effectively free to move in the material with minimal concern of charge-phonon interaction. While the charge density in the channel is dependent on temperature, and by proxy, the current flow, the actual tunneling probability of site-to-

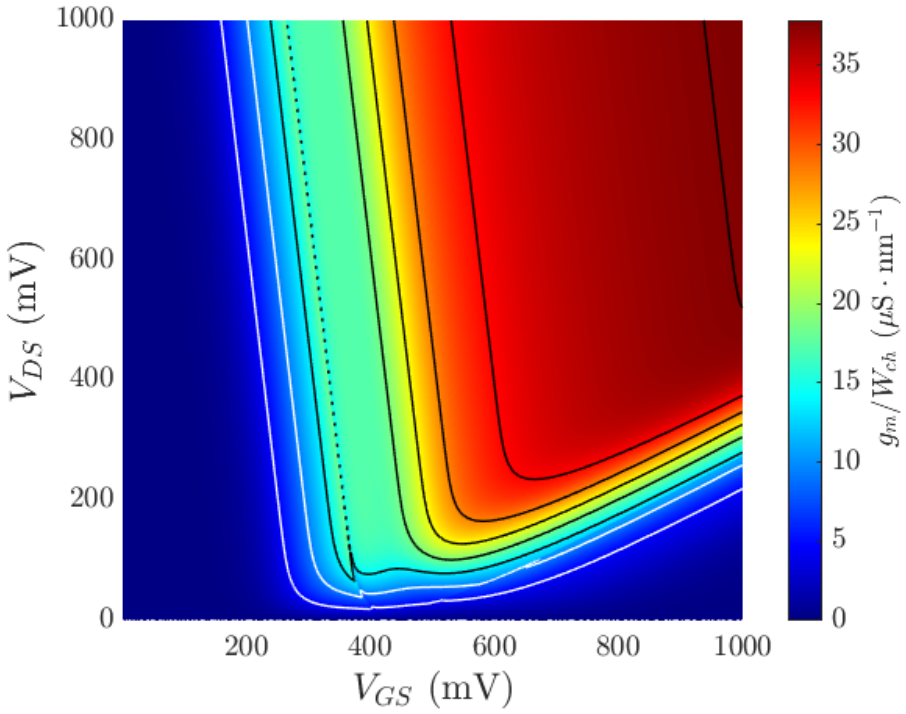

Figure 3.10. Transconductance-per-channel width g_m/W_{ch} of the transistor as a function of V_{GS} and V_{DS}. Channel width is $W_{ch} = 1.5987$ nm per nanoribbon ($n_{rib} = 4$), for a total width, excluding gaps, of 6.3948 nm.

site hopping of charges (according to a tight-binding model) is either unaffected by or has negligible dependence on temperature. Thus a decreased charge density for a given potential is the only overall effect of dropping temperatures. That is why, for a given current, the drain-source potential must increase by a factor between 1.5 and 3.3, comparing operation at 90 K to 300 K.

Potentially-unusual behavior appears in the transconductance and effective drain-source resistance curves. Transconductance, shown in Fig. 3.10, is defined as $g_m = \frac{\partial I_{DS}}{V_{GS}}$, and the effective drain-source conductance can be found by $g_o = \frac{\partial I_{DS}}{V_{DS}}$. Output resistance, r_o, is the inverse of this value, and is shown in Fig. 3.11. Given the channel width ($W_{ch} = 1.5987$ nm per ribbon), as can be seen by the scale, these devices have very low transconductance ($g_m \leq 250\ \mu$S) and a large output resistance ($r_o \geq 1$ MΩ, up to several GΩ). The "unusual" behavior mentioned previously appears in Figs. 3.10, 3.11, and 3.12 with dense contours starting at $V_{GS} \approx 300$ mV and ending at $V_{GS} \approx 400$ mV. This line initially appears anomalous, but

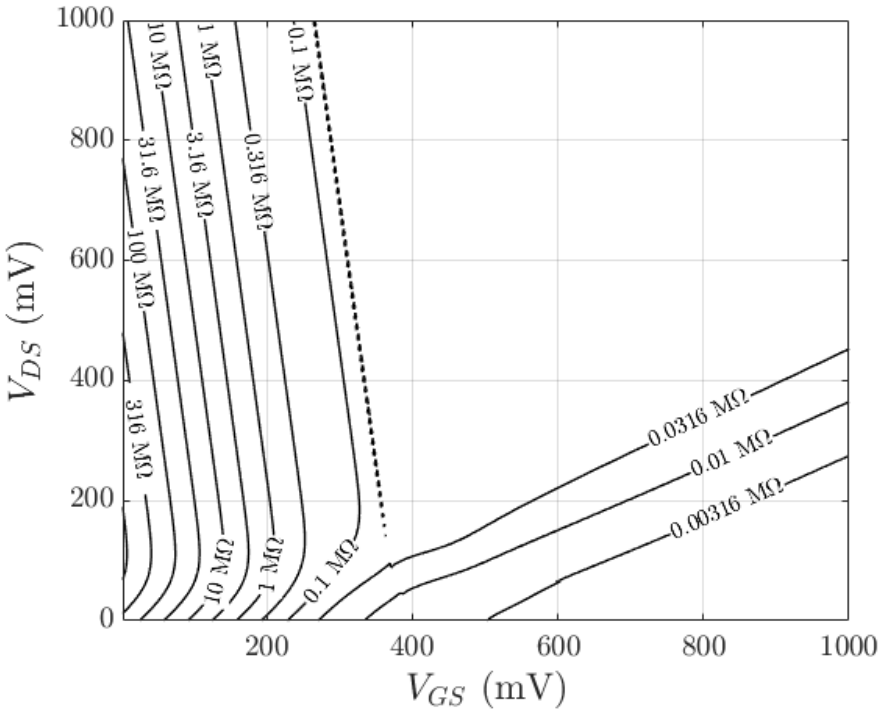

Figure 3.11. r_o resistance surface contours as a function of V_{GS} and V_{DS}.

upon inspection is actually the result data processing limitations, and not the model itself. The model has two equations used to calculate charge carrier densities in the sub-bands dependent on Fermi levels, effective charge mass due to relativistic speeds caused by ballistic transport, and temperature. These are an exponential and a Boltzmann approximation, each taken at different energy levels to match the DOS calculations in the SPICE model to those calculated continuously by the TCAD/physics simulation and experimental data. The transition between utilizing the exponential and Boltzmann approximations is a *step charge density*, intentionally tuned to be continuous and smooth, so the SPICE simulator can accurately calculate the appropriate energy levels and DOS for charges within the model at any given point [27]. However, based on how charges end up distributed in the channel, for a short range of V_{GS} the I_{DS} vs V_{GS} curves briefly flatten out, resulting in a rapid fluctuation in g_m, which is evident by the thick line indicative of a high contour density in Fig. 3.10. This actually demonstrates the electrical consequences of the model's physical state transition quite well: The range of V_{GS} at which this occurs depends on V_{DS}, as the

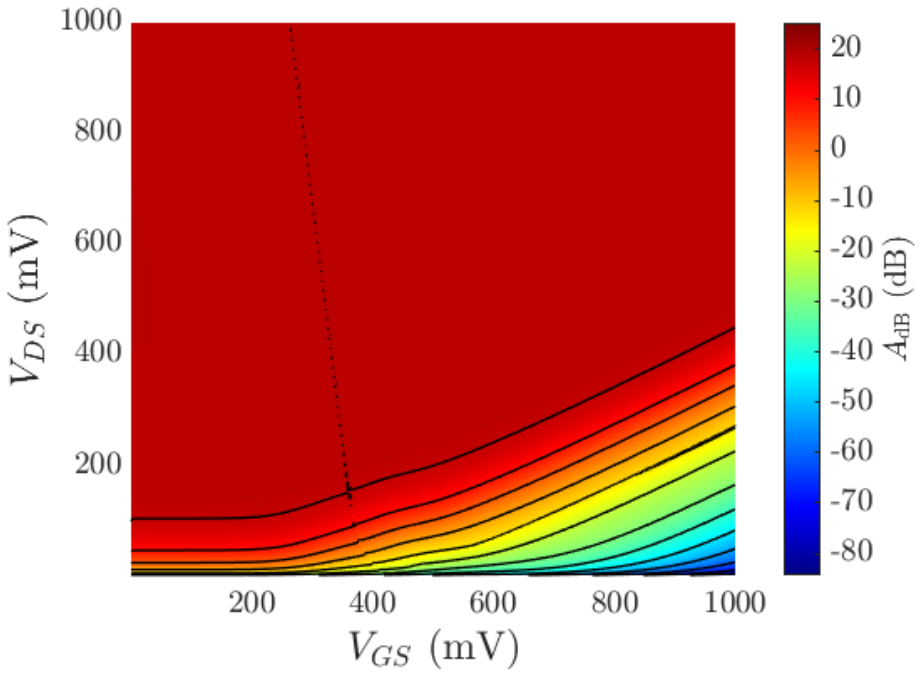

Figure 3.12. Autogain (dB) surface as a function of V_{GS} and V_{DS}.

transition between the DOS models necessarily comes "earlier" for larger V_{DS}, as the charge-carrier energy in the channel is higher because of the voltage applied. Thus, g_m decreases slightly, and then increases again, all within tens of millivolts. MATLAB displays this as a jump in the corresponding surface (or high contour density), even though a discontinuity is not present in the numeric I-V data.

By taking the product of the effective output resistance and the transconductance, an "autogain" term can be found – gain inherent to the device itself and dependent solely on its own operating region, $A = g_m r_o$.

Fig. 3.12 shows this surface (in dB), and demonstrates that the autogain for a GNRFET is largely constant over a majority of its operation, which is especially useful for designing amplifiers. The maximum autogain is approximately 18.8 dB, or about 8.73.

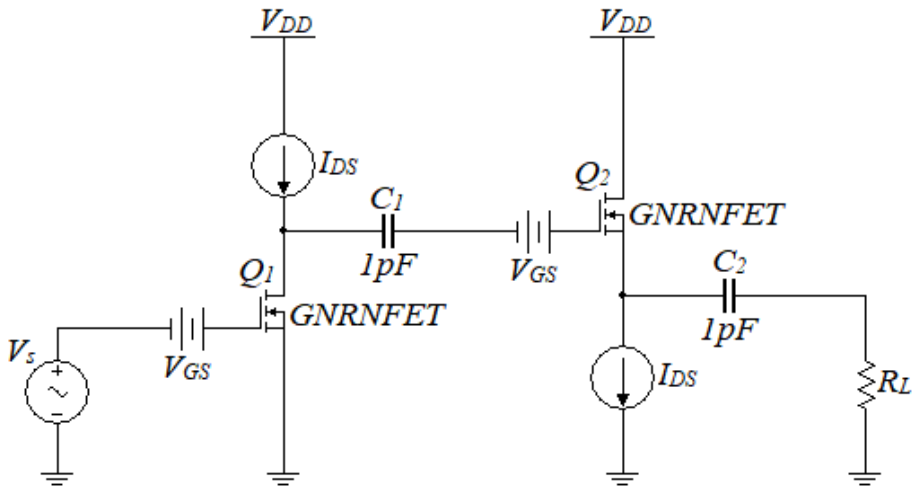

Figure 3.13. A simple two-stage amplifier.

3.2.2 The GNRFET-Based Amplifier

A Simple Two-Stage Amplifier

The amplifier presented in Refs. [23] and [24] is a simple, two-stage CS-CD amplifier made from these GNRFETs. While the cascaded form of the amplifiers presented later in those same references have an initial buffering stage, the basic two-stage form does not. As will be shown later, analysis on a two-stage amplifier is inadequate, and will be resolved by including that initial buffering stage (for a CD-CS-CD amplifier).

With the parameter space sufficiently characterized, it is now possible to more thoroughly analyze and optimize the two-stage GNRFET amplifier. With the intent of maximizing bandwidth and achieving the highest gain, while minimizing the output impedance, a simple two-stage amplifier consisting of a common-source followed by common-drain configuration is selected, each to be driven by an equivalent active load, I_{DS}, as seen in Fig. 3.13. Each stage is coupled via a 1 pF capacitor and has the same DC V_{GS}. This design in particular is chosen to minimize the external components, allowing this circuit, in theory, to be implemented in an integrated circuit with graphene-based interconnects between transistors (though metal contacts are still required for input and output stages). This circuit was simulated over a range of combinations of V_{GS} and I_{DS}, searching for an optimal set of parameters. With

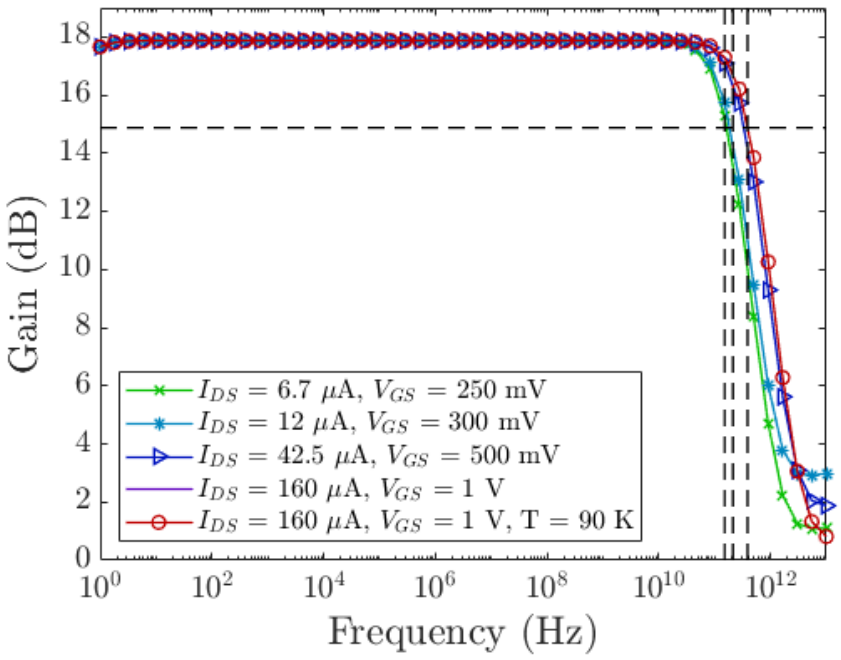

Figure 3.14. Unloaded gain for a simple two-stage amplifier.

the intent of forcing $V_{DS} \approx 1$ V, the gate-source voltage was first set to a value, then the drain-source current selected to push V_{DS} as near to 1 V as possible. Fig. 3.14 shows four unique combinations of parameters, with the fifth as a redundant setup at 90 K. For a more efficient design, at $T = 90$ K all current sources can be reduced by approximately $20\,\mu$A, resulting in even lower DC power consumption. It is interesting to observe that the results at room-temperature shows that the simulated gain – 17.875 dB – is very close to what was predicted for maximum autogain. It was also noticed that higher V_{GS}, and thus higher I_{DS}, allows for a greater bandwidth of operation. The lowest bandwidth – 151 GHz at $V_{GS} =$ 250 mV and $I_{DS} = 6.7$ μA – is almost 60 GHz less than the next-lowest bandwidth – 213 GHz at $V_{GS} = 300$ mV and $I_{DS} = 12$ μA – and half the highest bandwidth – 388 GHz at $V_{GS} \geq 500$ mV and $I_{DS} \geq 42.5\,\mu$A. After reaching this bandwidth, increasing V_{GS} and I_{DS} no longer increases bandwidth, but only affects the operation in the region of $f \geq 1$ THz. This shows that there is initially no benefit to increasing either of those parameters beyond $V_{GS} = 500$ mV and $I_{DS} = 42.5$ μA. This also puts a limit on the input signal size.

Because any AC signals passed in are in a superposition with the DC voltages, the input signal should not change the DC operating point. While the gain is relatively constant, the bandwidth is not. Thus, for maximal bandwidth operation, if $V_{GS(DC)}$ is set to 750 mV and the appropriate drain-source current given (approximately 120 μA), the maximum input signal could be $V_{GS(AC)} = 250$ mV. However, there is still the limitation that the amplifier cannot amplify beyond its source voltage, which is limited to 1 V. This puts a further restriction on an input signal size of $V_{GS(AC)} = 127.7$ mV. In this case, $V_{GS} = 627.7$ mV and $I_{DS} = 70.3$ μA, with $g_m = 224.3\,\mu$S and $r_o = 38.91\,\text{k}\Omega$ would be required. A set of values for the second stage was found to have minimal impact on the overall gain and bandwidth, while maintaining functionality. By using $V_{GS1} = V_{GS2} = 627.7$ mV and setting $I_{DS2} = 69.16\,\mu$A, V_{DS2} becomes 0.95 V, $g_{m2} = 223.7\,\mu$S, $r_o = 39.01\,\text{k}\Omega$, secondary gain $A_2 = 0.8972$, and an overall gain of 7.83, or 17.9 dB was received, which matches exactly the simulated results.

3.2.3 The GNRFET Amplifier System Stability and a Three-Stage Modification

Ideal System Simulations

An important factor for high frequency systems is stability. For a common-source configuration, the Y-parameters can be found to be:

$$Y_{CS} = \begin{bmatrix} Y_i + Y_f & -Y_f \\ g_{m1} - Y_f & Y_{o1} + Y_f \end{bmatrix} \tag{3.10}$$

and for a common-drain configuration,

$$Y_{CD} = \begin{bmatrix} Y_i + Y_f & -Y_i \\ -(g_{m2} + Y_i) & Y_{o2} + g_{m2} + Y_i \end{bmatrix} \tag{3.11}$$

where $Y_i = 2\pi f C_{GS}\text{j} + Y_{GS}$, $Y_f = 2\pi f C_{GD}\text{j}$, $Y_{o(1,2)} = 2\pi f C_{DS}\text{j} + r_{o(1,2)}^{-1}$, and Y_{GS} is some admittance in parallel to the gate-source capacitor, if necessary.

Using the voltage/current settings discussed in the previous section, $r_{o1} = 38.91\,\text{k}\Omega$ and $r_{o2} = 39.01\,\text{k}\Omega$. For multiple stages cascaded together, there needs to be a single set of Y-

parameters to describe the entire system. While, mathematically, Y-parameters cannot be directly cascaded, if they are converted to $ABCD$-parameters, or transmission parameters, they can be multiplied together, and then re-converted back into Y-parameters. For the two-stage system, if A_{CD} is the conversion of Y_{CD} to $ABCD$-parameters, and A_{CS} is the common-source equivalent, then the total set of transmission parameters is simply $A_T = A_{CS}A_{CD}$. If G_s is an input conductance ($G_s = R_s^{-1}$) and G_L is a load conductance ($G_L = R_L^{-1}$), then the Stern stability factor can be calculated by Eq. 3.12 [154]:

$$K = \frac{2\left(\mathrm{Re}\left(Y_{11}\right) + G_s\right)\left(\mathrm{Re}\left(Y_{22}\right) + G_L\right)}{\left|Y_{12}Y_{21}\right| + \mathrm{Re}\left(Y_{12}Y_{21}\right)} \tag{3.12}$$

From these, impedances and system gains may be extracted.

Analysis of these high-frequency Y-parameters, and using an approximate $C_{DS} = 1.35 \times 10^{-3}$ aF and $R_s = 1.5\,\mathrm{k\Omega}$ (selected to balance noise performance and maintain bandwidth) indicates that, in its original state, the system is stable over all ranges of frequencies, as can be seen in Fig. 3.15. However, unexpected problems arise with this setup when including a series source resistance. First off, the input impedance, while still high, is only predicted to be $|Z_{in}| < 10\,\mathrm{M\Omega}$, decreasing with frequency. Second and the more problematically is that, while the gain is predicted to be nearly 17 dB as before, due to a decreased input impedance and voltage divider that forms at high frequencies, the actual gain ceases to resemble the response shown in Fig. 3.14, and becomes the gain simulated in Fig. 3.16, which is actually severe attenuation over the entire frequency range.

However, this can be easily resolved. By incorporating a preliminary input stage to act as a buffer (thus, common-drain is selected), as seen in Fig. 3.17 the input impedance can be increased by several orders of magnitude even at high frequencies, and the gain restored, as can be seen in Fig. 3.18. In the corrected circuit, for a compromise between stability, noise figure, bandwidth, and transition frequency, R_s is selected to be $16.05\,\mathrm{k\Omega}$. This value was found by simulating the system over a range of incrementally-decreasing R_s until the gain and bandwidth no longer increased. Furthermore, its compromise between stability and noise performance is due to how increasing R_s decreases stability, but improves noise performance (decreases noise figure). This value of series resistance is in the same

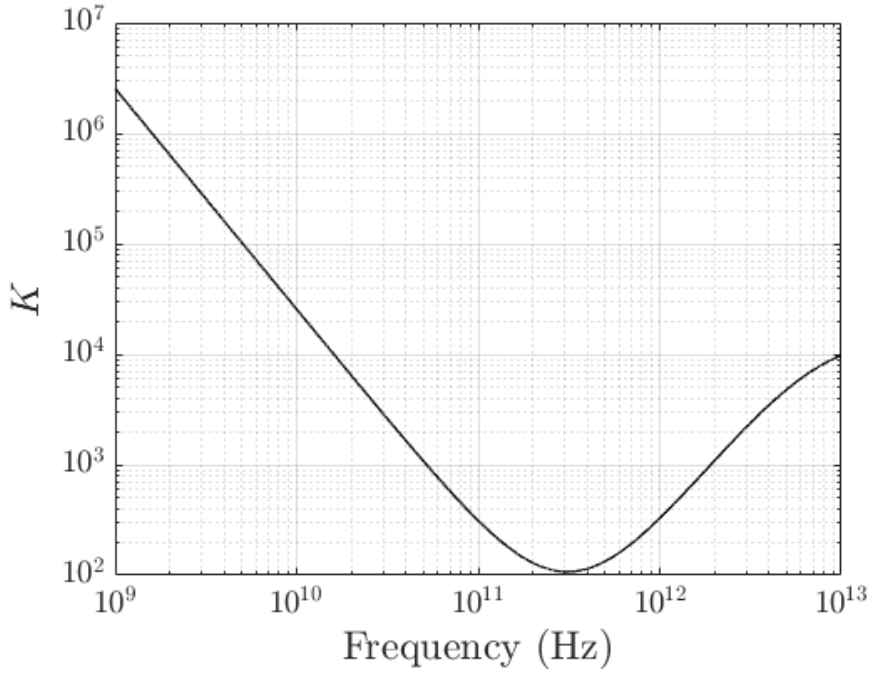

Figure 3.15. The Stern stability factor K for the original amplifier, for $R_s = 1.5\,\mathrm{k}\Omega$.

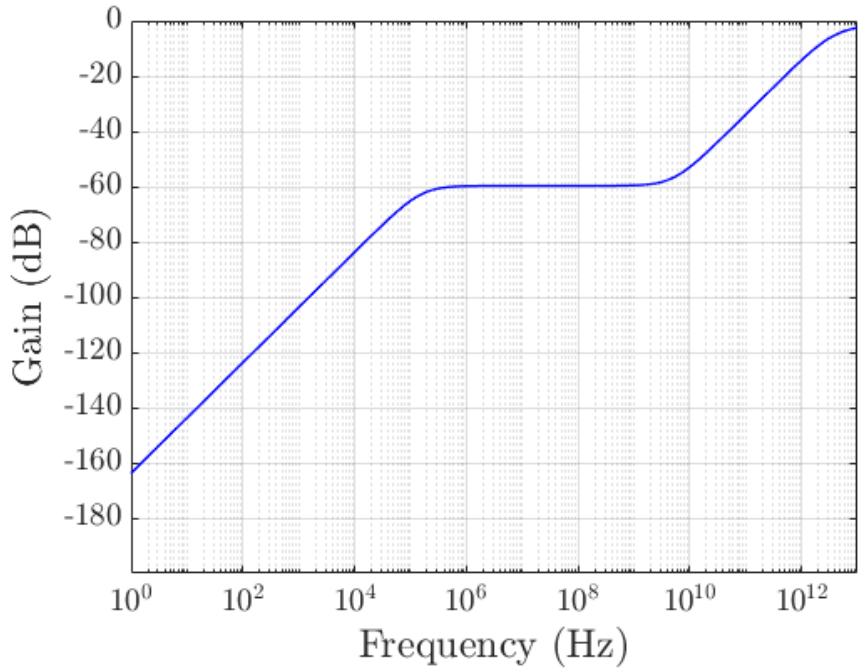

Figure 3.16. The new gain for the two-stage amplifier for $R_s = 1.5\,\mathrm{k}\Omega$.

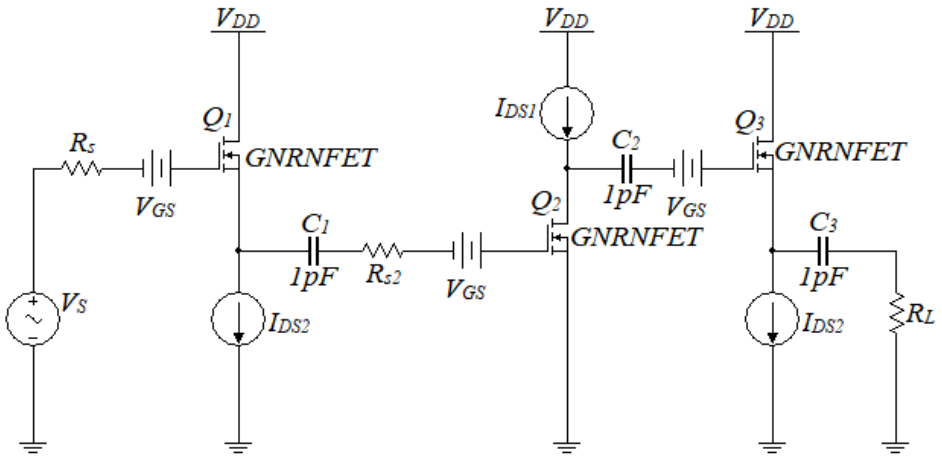

Figure 3.17. The corrected, 3-stage amplifier. Note the presence of R_s and R_{s2} for noise performance and stability. It was found that $R_{s2} = 0\,\Omega$ is an appropriate selection and does not impact stability adversely.

order of magnitude of "suggested" simulation parameters given by Refs. [27], [29] for metal-to-GNR contact vias. If GNR-based interconnects are used between stages, this contact resistance should not be present, though the "more-involved" simulation later incorporates vastly-simplified transmission line effects from GNR-based interconnects not present in this "idealized" system. More detailed transmission line effects are discussed in Ch. 4.

Noise performance is discussed and developed further later, but Fig. 3.20 demonstrates the aforementioned trade-off. The total $ABCD$-matrix can be calculated by

$$A_T = A_{CD} A_{RS2} A_{CS} A_{CD} \tag{3.13}$$

Though, for $R_{s2} = 0\,\Omega$, A_{RS2} is simply an identity matrix. This, in turn, may be converted back into Y-parameters, and the other parameters calculated per the previous equations. Incorporating R_s into the $ABCD$-matrices (as a separate step from calculating K) can predict the gain and transition frequency with increased accuracy.

The gain of the amplifier now sits at 16.90 dB, which agrees with the predicted 16.93 dB, with a bandwidth of 269 GHz (f_l = 159 kHz, f_h = 269 GHz) and a transition/unity gain frequency at approximately 1.19 THz, which is comparable with the transition frequencies predicted in Ref. [149]. For the range of the bandwidth, the system rests com-

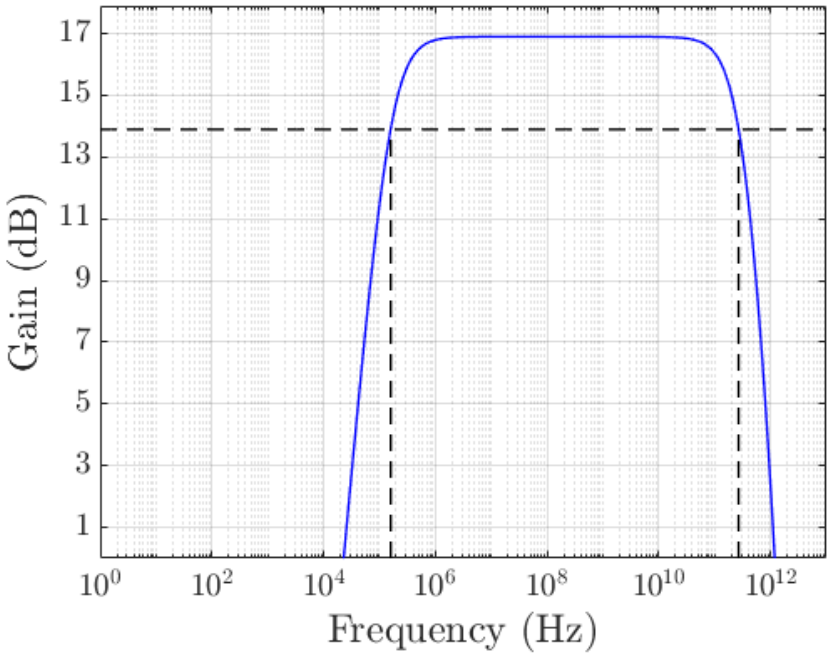

Figure 3.18. Gain of the corrected idealized amplifier. The sudden presence of a low-frequency cutoff frequency is very apparent, and should be resolved by an external sag compensation circuit.

fortably in unconditional stability ($K \gg 1$), as can be seen in Fig. 3.19. Directly using the analytically-predicted values of C_{GD} and C_{GS} in the calculations results in a predicted cutoff frequency of over double the bandwidth actually seen (571 GHz), while using the value of those capacitors found via simulation gives almost half the simulated bandwidth (132 GHz). However, using the geometric mean of the two capacitor values ($\sqrt{2.31 \cdot 9.99} = 4.81$ aF) as discussed previously gives a reasonably-accurate approximation of the bandwidth ($\approx$ 274 GHz, which matches the geometric mean of the calculated frequencies as well) and a moderate approximation of the transition frequency ($\approx$ 1.402 THz). The reason that the geometric mean is used rather than the arithmetic mean is because, for frequency calculations, if a low and a high frequency are known, then the central frequency is the geometric mean of the two. Approximating frequency cutoff based on Elmore delay [71], [99] leaves $1/\sqrt{f_L f_H} \approx 2\pi\sqrt{RC_H RC_L} = 2\pi R\sqrt{C_H C_L}$ – the geometric mean of capacitance. In the

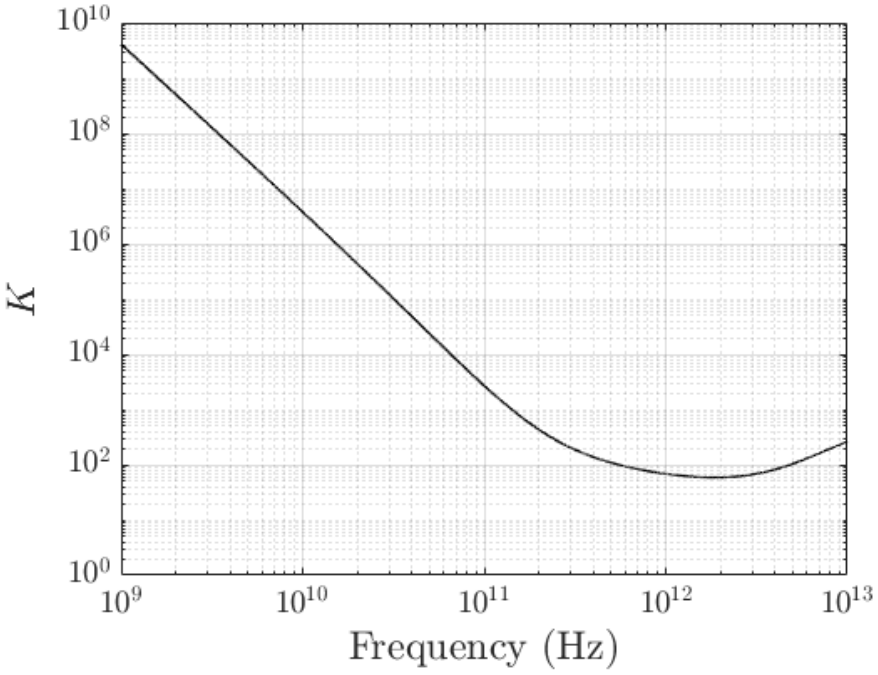

Figure 3.19. The Stern stability factor K for the idealized three-stage circuit with series resistance $R_s = 16.05\,\mathrm{k}\Omega$.

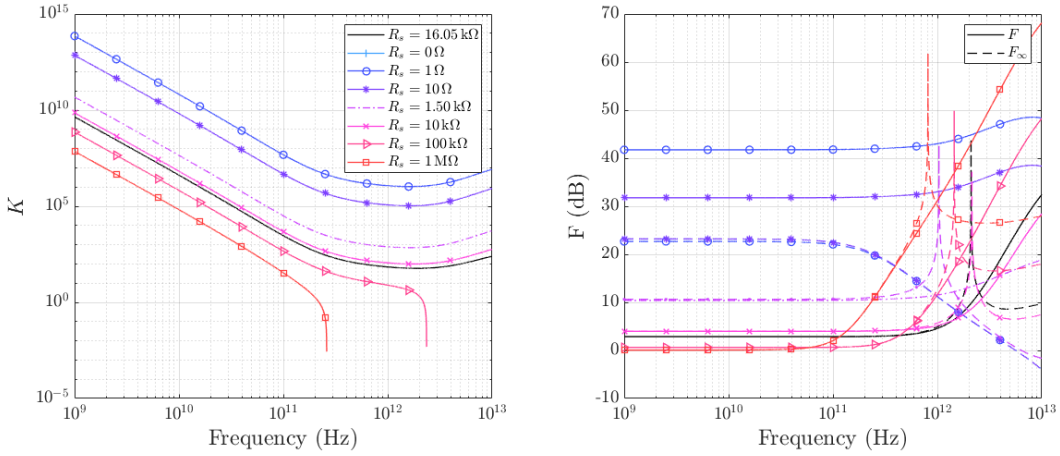

Figure 3.20. Demonstration of the trade-off between stability (left) and noise performance (right), the latter of which is discussed in greater detail later. As can be seen, low R_s improves stability greatly, but decreases noise performance (increases noise figure), and vice-versa.

meantime, using the extreme values of C_{DS} has no noticeable effect on the stability, gain, or bandwidth of the system.

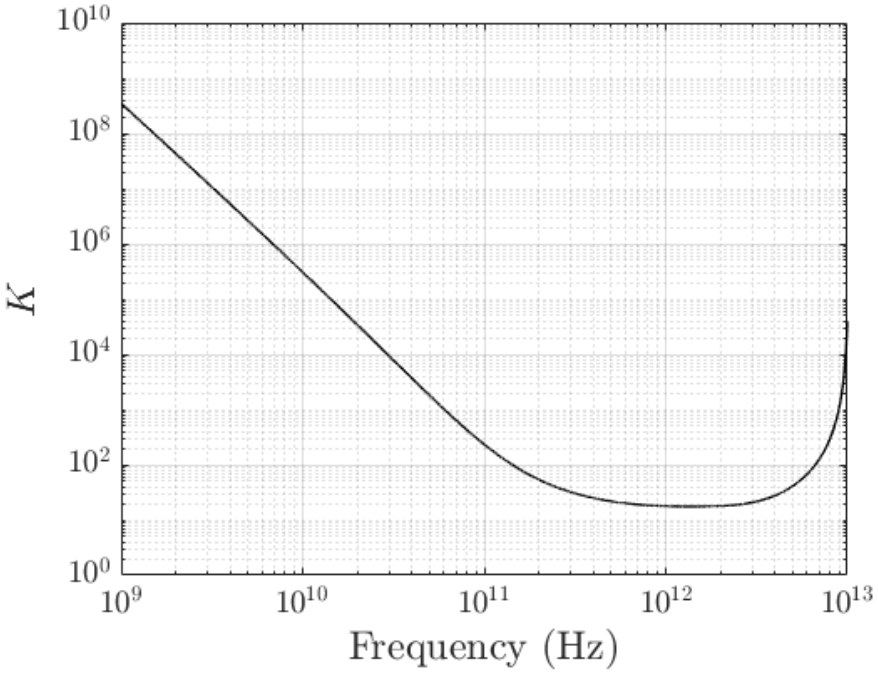

Figure 3.21. The Stern stability factor K for the three-stage circuit, $R_s = 16.05\,\mathrm{k}\Omega$, given simplified transmission lines with approximate $R = 150\,\Omega$ and $C_{SH} = 9$ aF.

Simplified Transmission-Line Effects within the GNRFET Amplifier

Graphene-based interconnects, especially with high-N GNRs, have exceptional transmission properties. These include delays of < 1 ps for interconnects of length $L < 10$ μm [155]. Multi-layer GNR interconnects that exceed 10 layers are comparable to copper, giving > 0.06 fF/μm capacitance and < 1 kΩ/μm resistance for a 10 nm "half-pitch" interconnect on SiO_2[156]. For short GNR interconnects on a hexagonal BN (h-BN) buffer layer between the GNR and substrate, resistivity can decrease by a factor of up to 17 in a single layer [157]. GNRFETs can also be constructed with this material as a buffer layer [31], [32], so separate manufacturing methods are not required during the CVD process. Given the GNRFETs channel length, if interconnects of less than ten times this length with a pitch of 20 nm are considered, then the behavior changes noticeably. Utilizing the numbers presented in Ref. [156] as a worst-case scenario (as others have reported lower numbers, such as in Ref. [157]) for simplified transmission lines consisting of a series resistor $R \approx 150\,\Omega$ and a shunt

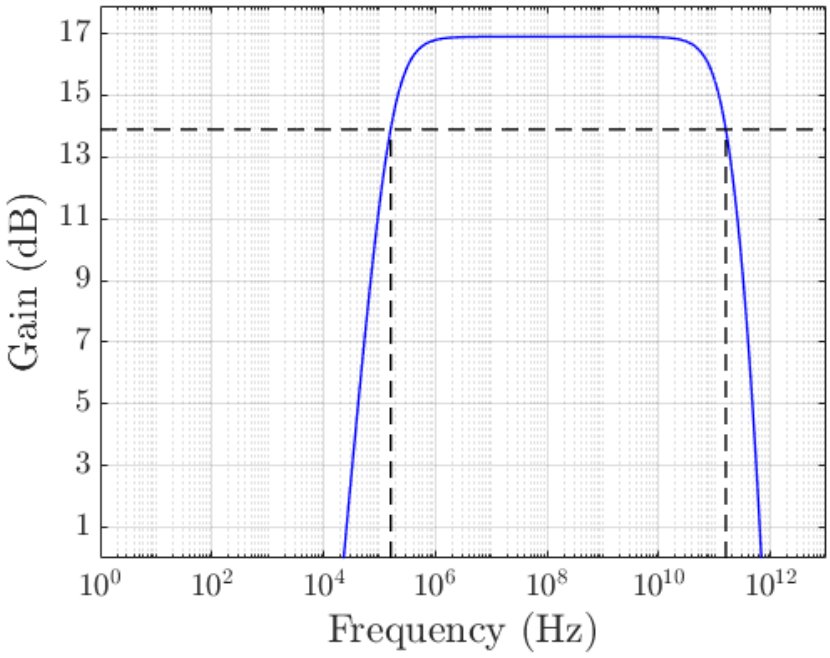

Figure 3.22. Gain of the three-stage circuit, $R_s = 16.05\,\mathrm{k}\Omega$, given simplified transmission lines with approximate $R = 150\,\Omega$ and $C_{SH} = 9$ aF.

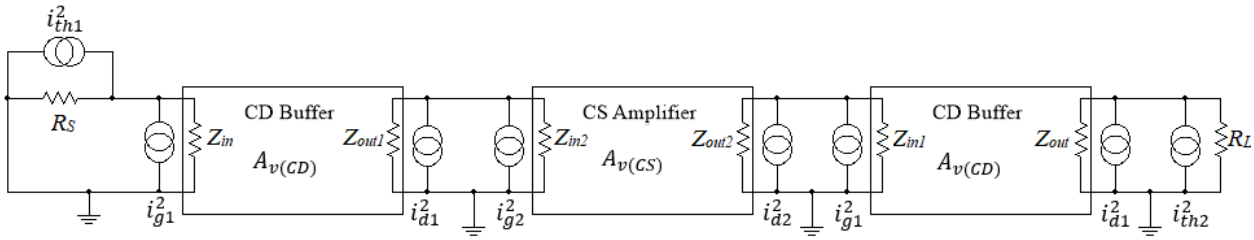

Figure 3.23. Equivalent simplified noise model for the three-stage amplifier. Each amplifier stage is represented by an equivalent block with input and output impedances. Current and voltage sources are, for simplicity, considered noiseless.

capacitance $C_{SH} \approx 9$ aF, then stability still indicates unconditional stability (Fig. 3.21), while the predicted bandwidth decreases to 161 GHz, and the predicted transition frequency drops significantly to 745 GHz. Gain, however, remains unchanged. Fig. 3.22 shows the actual gain plot, demonstrating that the gain remains at 16.9 dB as expected. The simulated

bandwidth is found to be 159 GHz, and the transition frequency to be lower than expected at 688 GHz.

3.2.4 Predicted Noise Performance of the GNRFET Amplifier

Because GNRFETs are a type of FET, they still exhibit noise properties. This includes thermal noise sources, high frequency leakage noise [158]–[163], and shot noise [164], [165]. While prior noise analysis and experimentation has been done on GFETs, the noise sources dependent on the transistor design itself are largely the same. Thus, it is prudent to incorporate these effects into the analysis of any GNRFET-based amplifier. Because they have not yet shown any unique noise phenomenon, it follows that the noise analysis used for high-frequency MOSFETs may be used. Following the methods explained in Ref. [166], the overall noise figure of the amplifier designed in the previous section can be determined using the parameters found therein and the simple approximate noise model shown in Fig. 3.23.

In the case of the amplifier in Fig. 3.13, N_i is the input noise power into the first stage, and N_o is the output noise power from the last stage, which has contributing factors from the previous stages. These will be denoted N_{i1} and N_{o2}, respectively. Using the MOSFET-based methodology, an optimal series input resistance R_s can be selected to maximize noise performance, giving the total input noise:

$$N_i = \frac{i_{th1}^2 + i_{g1}^2}{|Y_{in} + G_s|} \tag{3.14}$$

Here, $i_{g1}^2 = \frac{16}{15} k_B T \omega^2 C_{GS}^2 \Delta f$ is the mean-square high-frequency gate noise current into stage one, $i_{th1}^2 = 4 k_B T G_s \Delta f$ is the mean-square thermal noise from the input conductor, $G_s = 1/R_s$, and $Y_{in} = 1/Z_{in}$ is the input conductance of the amplifier. Here, $\Delta f = 269$ GHz is the amplifier bandwidth, ω is the operational frequency, T is temperature, and k_B is Boltzmann's constant. From this, the input noise for the three-stage amplifier was calculated to be 451 nW.

The output power is a much more involved calculation, containing contributions from the outputs of the first, second, and third stage and inputs to the second and third stages:

$$\begin{aligned} N_o = & \frac{1}{2}\left|Z_{out}\right|\left(i_{d1}^2 + i_{th2}^2\right) \\ & + \left|\frac{Z_{oi2}}{Z_{out}}\right|\left|A_{v(CD)}\right|^2\left[\left(i_{d2}^2 + \mathrm{i}_{g1}^2\right)\left|Z_{oi1}\right|\right. \\ & \left. + \left|A_{v(CS)}\right|^2\frac{\left|Z_{oi1}\right|^2}{\left|Z_{oi2}\right|}\left(i_{d1}^2 + i_{g2}^2\right)\right] \end{aligned} \tag{3.15}$$

where $Z_{oi1} = Z_{out1}||Z_{in2}$, $Z_{oi2} = Z_{out2}||Z_{in1}$, and $Z_{(in,out)(1,2)}$ may be calculated using the Y-parameters for the common-drain (1) or common-source (2) amplifier individually, given previously, $A_{v(CD,CS)}$ is the gain corresponding to the common-drain or common-source amplifiers individually, respectively, and the various new current sources may be calculated by:

$$i_{g2}^2 = i_{g1}^2 \tag{3.16a}$$

$$i_{d(1,2)}^2 = 4\gamma k_B T g_{m(2,1)}\Delta f \tag{3.16b}$$

$$i_{th2}^2 = 4k_B T G_L \Delta f = \frac{4k_B T}{\left|Z_{out}\right|}\Delta f \tag{3.16c}$$

Here, γ is a parameter related to channel length. For long-channel devices, it is 2/3, but for short-channel devices it can be two to five times larger [166]. Here it is set to $\gamma = 1$. The definitions of i_{d1}^2 and i_{d2}^2 may seem backwards, relative to $g_{m(1,2)}$, but this is due to the order in which currents are specified in Figs. 3.13 and 3.17 compared to the order of stages for the noise analysis given in Fig. 3.23. Shot noise is ignored because the input gate current is many orders of magnitude lower than other current levels. Here, the total output noise can be calculated to be $N_o = 38.34\,\mu\mathrm{W}$.

Using the previous parameters, output impedance is $|Z_{out}| = 4539\,\Omega$, and the transducer power gain was calculated to be $G_T = 91.09$ (19.595 dB) at $f = \Delta f$, and $G_T = 197.5$ (22.96

dB) at the midband. A noise figure of $F = 1.971$ (2.95 dB) was then determined. If N of these amplifiers were strung together, the noise figure could be calculated by:

$$F_T = 1 + (F - 1)\,\frac{1 - G_T^{-N}}{1 - G_T^{-1}} \tag{3.17}$$

Thus, maximum noise figure of $F_\infty = 1.983$ (2.97 dB). Incorporating the simplified transmission line effects, the noise figure increases to $F_\infty = 2.72$ (4.34 dB).

These prior calculations were given for high-frequency performance, so flicker noise can be safely ignored. However, if these devices are to be used for low-frequency systems, then flicker (or $1/f$) noise becomes an important factor. It has been shown that graphene-based devices *do* exhibit flicker noise, which, as expected, depend on a number of factors including channel area and substrate material [162], [163], [167]–[171], just as standard FETs exhibit. While little work appears to have been done on studying flicker noise in GNRFETs, a decent amount of work has gone into GFETs. Noise levels in such devices vary with each study, as expected, but generally flicker noise levels are low. Ref. [171] reports noise levels at room temperature of S_{Id} as less than $10^{-14}\text{A}^2/\text{Hz}$, decreasing approximately one order of magnitude per decade for GFET channel lengths of 350 nm. Similar or smaller numbers are reported in Ref. [169] for basic epitaxial graphene at temperatures varying between 0.4 K and 56 K, and a measured $\alpha = 0.94$ (for $1/f^\alpha$) [162] (instead given in terms of S_I/I_{ds}^2). The smallest yet, however, were the noise levels recorded in Ref. [168], which actually classifies GNRFETs under the same umbrella as GFETs. This paper records their test devices - 1500 × 300 nm GNRFETs – having $S_{Id} < 10^{-16}\text{A}^2/\text{Hz}$ (depending on I_D), and a quadratic dependence of the current parameter in the flicker noise models on the area of the GFET, and $0.91 < \alpha < 1.105$.

While these are relatively-low flicker noise levels, they are not unique, in that other FETs exhibit similar noise properties. FinFET devices show equivalent noise levels [73], as well as p- and n-MOSFETs used in CMOS technologies [172]–[174]. So, while GNRFETs and GFETs exhibit decent noise properties, they have no overall noise advantage, comparatively.

Table 3.1. A comparison of technologies and their relative performances. A higher figure of merit is better. "–" indicates the data could not be determined or was not provided.

Technology	V_{supply} (V)	$P_{DC(\text{mW})}$	A_{dB}	B_{GHz}	F_{dB}	FOM (dB·GHz/mW)	Method
Power GaN [175], [176]	≤ 20	≤ 0.9	10	8	–	≥ 88.9	Exp.
AlInN/GaN [177]	≤ 15	≤ 0.715	20	10-89	–	$\geq 2.49 \times 10^3$	Exp.
InAs/AlSb [178]	≤ 0.65	≤ 17.6	29	8	1.8	≥ 13.2	Exp.
InAs/AlSb ($T = 15$ K) [178]	≤ 0.65	≤ 6	24.2	8	0.27	≥ 32.3	Exp.
InP HBT [179]	–	≤ 97	≤ 25	190	–	≥ 49.0	Exp.
InP [92]	≤ 1	≤ 13.1	21.2	102	–	≥ 165	Exp.
SiGe HBT [180]	–	≤ 86	18.7	181	≤ 9	≥ 39.4	Exp.
50 nm mHEMT [181]	–	≤ 541	19.7	119	≤ 6.4	≥ 4.33	Exp.
65 nm CMOS [182]	1.2	≤ 35.4	21	28	≥ 10	≥ 16.6	Sim./Exp.
65 nm CMOS [183]	0.85	23.8	12.4	29.7	–	15.5	Sim./Exp.
GNRFET	1	≤ 0.211	16.9	269	2.973	$\geq 2.16 \times 10^4$	Sim.
T.L. GNRFET	1	≤ 0.211	16.9	159	4.339	$\geq 1.27 \times 10^4$	Sim.

3.2.5 Comparison of the GNRFET Amplifier to Other Technologies

A comparison of similar small-signal, low-power, sub-terahertz amplifier technologies (excluding wave and photonic amplifiers) was conducted. The figure of merit is defined as

$$\text{FOM} = \frac{A_{\text{dB}} B_{\text{GHz}}}{P_{DC(\text{mW})}} \tag{3.18}$$

where A_{dB} is the gain in dB, B_{GHz} is the bandwidth in GHz, and $P_{DC(\text{mW})}$ is DC power consumption in mW. Table 3.1 presents these and F_{dB} values, comparing technologies from high-speed devices such as as GaN [175]–[177], InP/InGaAs/InGaN [92], [178], [179] and other low-power HEMT MMIC devices [180], [181], and 65 nm CMOS processes [182], [183]. Other high-frequency devices were also considered, even though they were high-power amplifiers. The estimated power consumption is based on provided currents and supply voltages.

As can be seen from Table 3.1, while the system has average noise performance (among the other technologies), the figure of merit for the idealized system is 8.67 times than that the "best" system [177], sitting at 2.16×10^4 dB·GHz/mW. The simplified transmission-line version ("T.L. GNRFET") has slightly over half that FOM, at 1.27×10^4 dB·GHz/mW. Generally, they provide better high frequency and power performance. This is attributed to ballistic transport of charges that permits such a high frequency of operation (with a

transition frequency in the THz range, as compared to GHz), and the conduction of the nanoribbons leading to ultra-low power consumption.

One important observation is that, in spite of recent developments in the means to construct these devices, no physical devices could be constructed due to lack of available technology to do so – thus, the idealized and simplified transmission-line simulation approaches were taken. Because of this, it is exceedingly challenging to properly compare to real systems, such as those in the top part of Table 3.1. Even though it is challenging to compare practical models with simulated models as given in Table 3.1, the intention here is purely to demonstrate the *potential* of a GNRFET-based amplifier system utilized in this research. It is expected, under nonideal and more realistic conditions (e.g.: better transmission line modeling, as discussed in Chapter 4, and more contact-resistance-effects considered), or in a physically-built system the figure of merit for the amplifier may change. The simulations presented here are sufficiently reliable and accurate due to the physically-based nature of the models, which themselves contain empirical data and model fits to that data.

3.3 Normal Conductor Transmission Lines and Characteristic Impedances

3.3.1 Multilayer Substrate Effects

Because YBCO must be layered on a different substrate than what on which the graphene can be placed (the reasons for which are discussed in greater detail in Chapter 4), the dielectric effects of a hybrid or multilayer substrate need to be considered, especially when determining parasitics, like capacitance. For any material, relative permittivity is defined as $\epsilon_r = \epsilon_r' + \mathrm{j}\epsilon_r'' = \epsilon_r'(1 + \mathrm{j}\tan\delta)$ [184]. Recalling that the absolute index of refraction for a material is $n \approx \sqrt{\epsilon_r}$ for materials with $\mu_r \approx 1$ (e.g.: for dielectrics), if N layers are constructed of different materials, each of thickness t_i with relative permittivity ϵ_{ri} where $i = 1...N$, as illustrated in Fig. 3.24, then the effective index of refraction, n_{eff} can be found from a "first-principles" calculation. The time it takes for an electromagnetic wave to propagate through a material is:

$$T = \frac{d}{v} \rightarrow T_i = \frac{t_i n_i}{c} \tag{3.19}$$

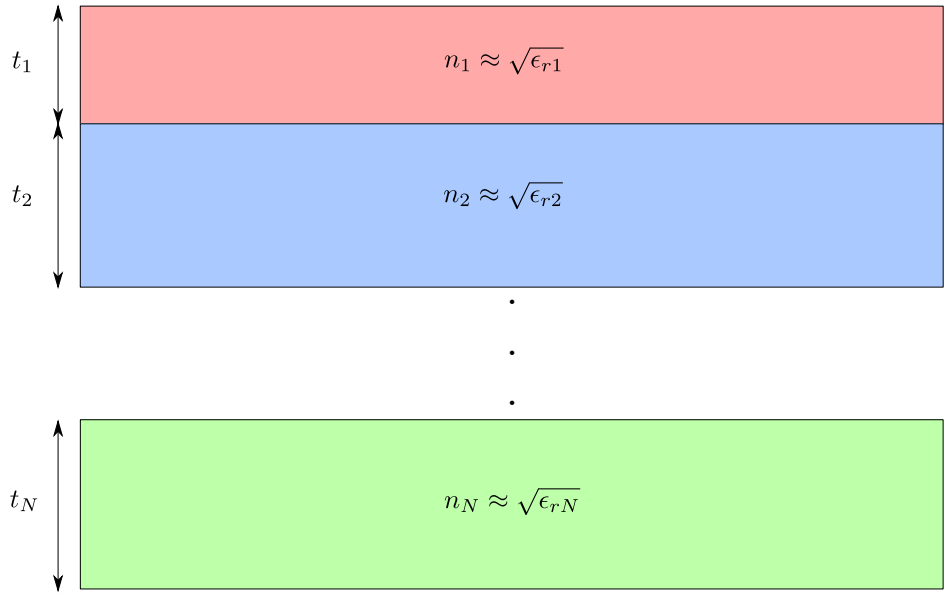

Figure 3.24. An illustration of a hybrid/multilayer substrate. The effective permittivity depends on the thicknesses and ϵ_r of each layer.

The total time T it takes the wave to propagate through the multilayer substrate is the sum of the individual layer times (ignoring reflection, other refraction, attenuation, and polarization effects):

$$T = \sum_{\mathrm{i}=i}^{N} T_i = \sum_{i=1}^{N} \frac{t_i n_i}{c} \tag{3.20}$$

With this, the propagation velocity, v_p, may be calculated for the multilayer substrate:

$$v_p = \frac{d}{T} = c \frac{\sum_{i=1}^{N} t_i}{\sum_{i=1}^{N} t_i n_i} \tag{3.21}$$

Refractive index is defined as $n \equiv c/v_p$, so this leads to an effective index of refraction:

$$n_{\mathrm{eff}} = \frac{\sum_{i=1}^{N} t_i n_i}{\sum_{i=1}^{N} t_{\mathrm{i}}} \tag{3.22}$$

For the relative permittivity, this means $\epsilon_{r\mathrm{eff}}$ can be approximated as:

$$\epsilon_{r\mathrm{eff}} \approx \left[\frac{\sum_{i=1}^{N} t_i \sqrt{\epsilon_{ri}}}{\sum_{i=1}^{N} t_i} \right]^2 \tag{3.23}$$

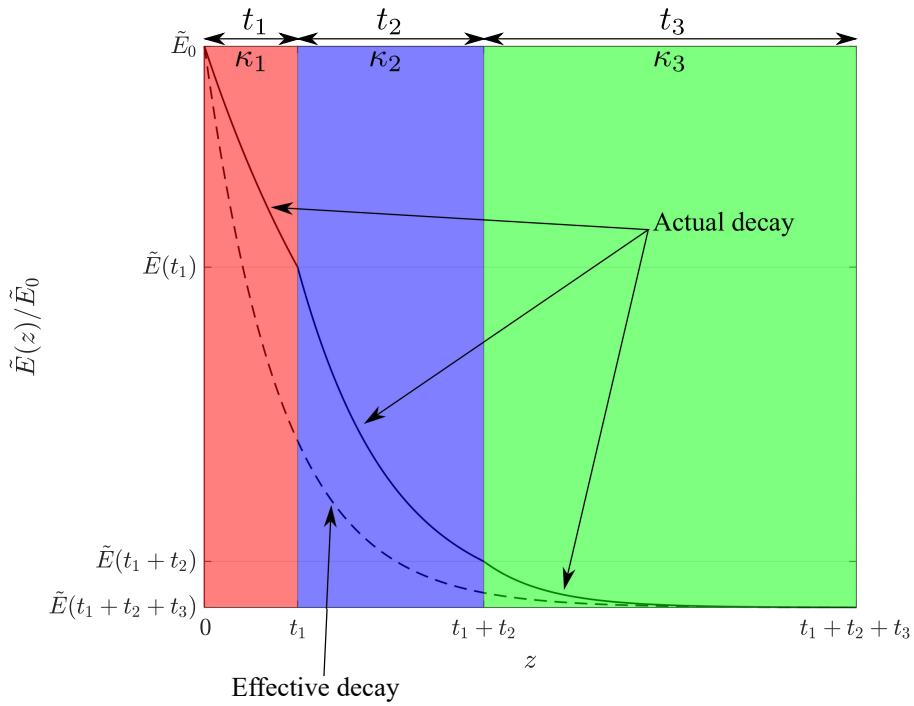

Figure 3.25. A demonstration of consecutive field decays.

The real and imaginary components may be extracted from this, allowing $\tan\delta = \epsilon''_{\text{reff}}/\epsilon'_{\text{reff}}$ to be determined for the effective substrate.

Taking a slightly more rigorous approach using the complex wavevector methodology to describe electromagnetic waves in a material, we end up with the same result. If the wavevector is defined as $\widetilde{k} \equiv \sqrt{\epsilon\mu_0}\omega = k + \mathrm{j}\kappa$, where $\epsilon = \epsilon_0\epsilon_r$, then the electric field penetrating a material at depth z at time τ is [184]:

$$\widetilde{\boldsymbol{E}}(z,\tau) = \widetilde{\boldsymbol{E}}_0 \mathrm{e}^{-\kappa z}\mathrm{e}^{\mathrm{j}(kz-\omega\tau)} \tag{3.24}$$

As it can be seen, k serves as a phase shift of the electromagnetic wave, and κ serves to attenuate the wave. Thus, with this in mind, a total κ and k can be determined.

An electromagnetic wave incident normal to the surface of a hybrid substrate will decay and shift according to the material in which is it traveling. If, as before, the thickness of

substrate level i is t_i and that substrate has wavevector $\widetilde{k}_i$, then the electric field at the end of that substrate has decayed to:

$$\widetilde{\boldsymbol{E}}_i = \widetilde{\boldsymbol{E}}_{i_0} \mathrm{e}^{-\kappa_i t_i} \mathrm{e}^{\mathrm{j}(k_i t_i - \omega\tau)} \tag{3.25}$$

It is important to remember that τ and t_i are completely unrelated: here, τ is time, and t_i is the thickness of substrate layer i.

Chaining them as before results in a total electric field at the bottom of the substrate stack of:

$$\widetilde{\boldsymbol{E}} = \widetilde{\boldsymbol{E}}_0 \mathrm{e}^{-\sum_{i=1}^{N} \kappa_i t_i} \mathrm{e}^{\mathrm{j}(\sum_{i=1}^{N} k_i t_i - \omega\tau)} \tag{3.26}$$

Treating the multilayer substrate as a singular layer of an "effective material" as before and equating the following equations:

$$\widetilde{\boldsymbol{E}}_0 \mathrm{e}^{-\kappa_{\mathrm{eff}} \sum_{i=1}^{N} t_i} \mathrm{e}^{\mathrm{j}(k_{\mathrm{eff}} \sum_{i=1}^{N} t_i - \omega\tau)} = \widetilde{\boldsymbol{E}}_0 \mathrm{e}^{-\sum_{i=1}^{N} \kappa_i t_i} \mathrm{e}^{\mathrm{j}(\sum_{i=1}^{N} k_i t_i - \omega\tau)} \tag{3.27}$$

Solving for κ_{eff} and k_{eff} and letting $\widetilde{k}_{\mathrm{eff}} \equiv k_{\mathrm{eff}} + \mathrm{j}\kappa_{\mathrm{eff}}$ and $\widetilde{k}_i \equiv k_i + \mathrm{j}\kappa_i$ yields:

$$\widetilde{k}_{\mathrm{eff}} = \frac{\sum_{i=1}^{N} \widetilde{k}_i t_i}{\sum_{i=1}^{N} t_i} \tag{3.28}$$

Which, upon solving for $\epsilon_{r\mathrm{eff}}$, is the same result as before. This is illustrated with an $N = 3$ case in Fig. 3.25, which shows the magnitude of the electric field through the layers (it does not show phase shift).

This method of approximating $\epsilon_{r\mathrm{eff}}$ is referred to as the *quasi-TEM approximation*, which assumes the elements of the transverse electromagnetic mode (TEM) fields are approximately orthogonal [185]. This form of the approximation also ignores reflection effects at the interfaces between substrates, which *will* exist in a real system. Further permittivity estimates, which are based on system geometry and size, can be based on this initial estimate.

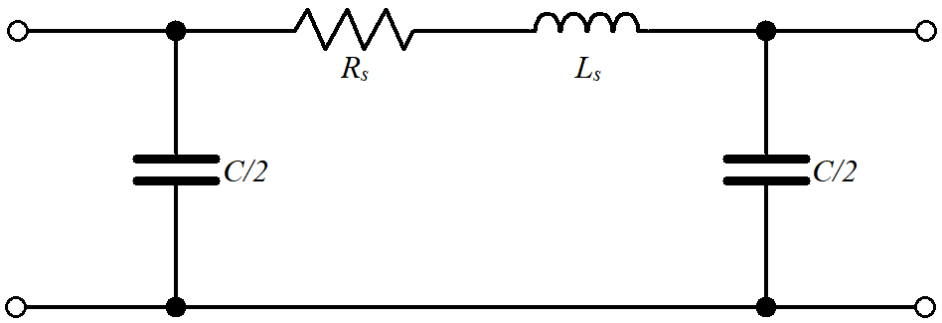

Figure 3.26. The equivalent Π-model of a simple transmission line

3.3.2 Microstrip Transmission Lines

Based on the directly-coupled system serving as the initial research motivation [23], [24], there are several types of interconnects at play: interconnects between junctions (in the YBCO), interconnects between GNRFETs (graphene-based interconnects), and, perhaps most challenging to model of all, the interconnects between the YBCO and GNRFET subsystems. In this section, these physical transmission lines will be discussed in depth.

Background Theory

Using the stripline transmission line shown in Fig. 3.3 as an example, if $v_p = c/\sqrt{\epsilon_{\text{eff}}}$ is the propagation velocity once more, and the characteristic impedance-per-unit-length is $Z_o = 1/v_p C$, then Z_o may be found, for $w/h \leq 1$ and $t/h < 0.005$ as [186]:

$$Z_o \approx \frac{60}{\sqrt{\epsilon_{\text{eff}}}} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \tag{3.29a}$$

$$\epsilon_{\text{eff}} \approx \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[\left(1 + \frac{12h}{w}\right)^{-1/2} + 0.04\left(1 - \frac{w}{h}\right)^2\right] \tag{3.29b}$$

recalling that h is the height of the substrate and w is the width of the microstrip. Thus, capacitance-per-unit-length is $C = 1/Z_o v_p$, which simplifies to:

$$C \approx \epsilon_r \left[60c \ln\left(\frac{8h}{w} + \frac{w}{4h}\right)\right]^{-1} \tag{3.30}$$

If no ground plane is present or it is considerably distant from the transmission line ($h \gg w$), then the transmission lines may be modeled with traditional interconnect capacitances-per-unit-length, assuming that the wire thickness (t) is small compared to the substrate depth as before [71]:

$$C \approx \epsilon_r \epsilon_0 \left[\frac{w}{h} + 0.77 + 1.06 \left(\frac{w}{h} \right)^{0.25} + 1.06 \left(\frac{t}{h} \right)^{0.5} \right] \tag{3.31}$$

The first term in the brackets is the geometric capacitance, and the subsequent terms are approximations for the fringe capacitances.

In a non-superconducting interconnect, the series characteristic resistance and inductance may also be calculated [71]:

$$R_s = \frac{\rho}{wt} \tag{3.32}$$

$$L_s = \frac{\mu_r \mu_0}{2\pi} \ln \left(\frac{8h}{w} + \frac{w}{4h} \right) \tag{3.33}$$

The value of μ_r varies with substrates, but is usually set $\mu_r = 1$, as it is rarely significantly above that value in nonconductors.

If the assumption about the ratio between microstrip thickness and substrate height cannot be taken as given, then the following values of effective microstrip width, w_{eff} can replace w in those equations [186]:

$$\frac{w_{\text{eff}}}{h} = \frac{w}{h} + \frac{t}{\pi h} \begin{cases} 1 + \ln \frac{2h}{t} & \frac{w}{h} \geq \frac{1}{2\pi} \\ 1 + \ln \frac{4\pi w}{t} & \frac{w}{h} < \frac{1}{2\pi} \end{cases} \tag{3.34}$$

The corresponding Π-model for the normal transmission line is shown in Fig. 3.26. For long transmission lines, it is prudent to cascade multiple Π-model defined over some fraction of the total length, l.

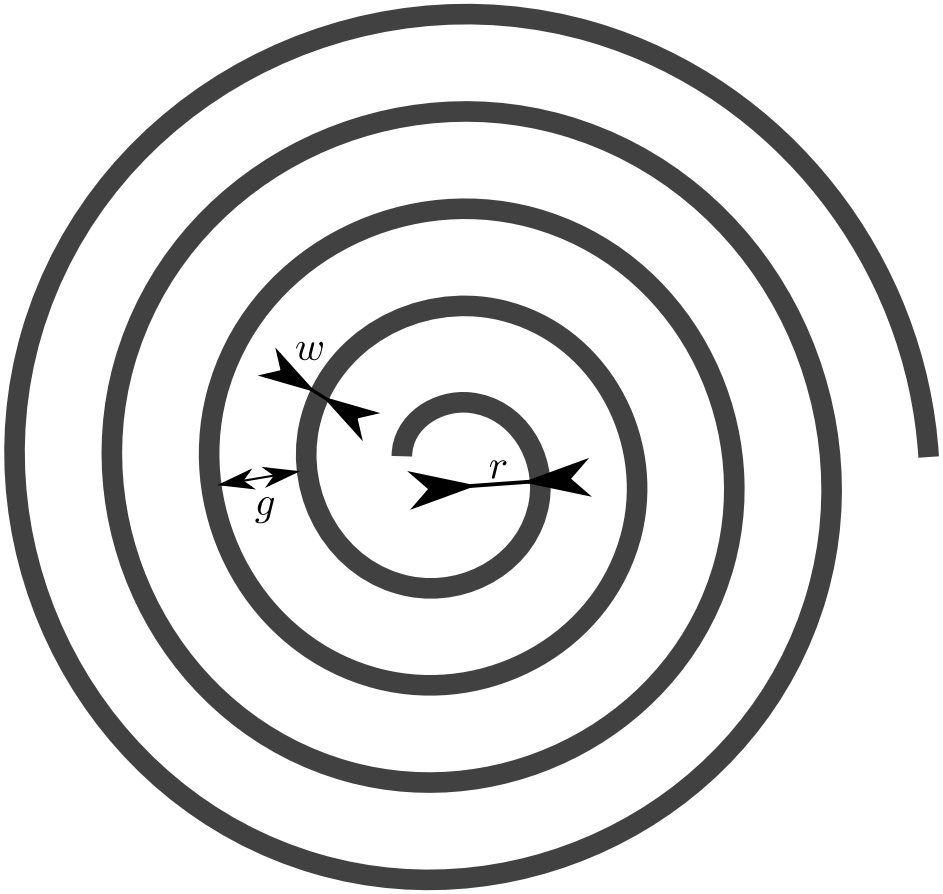

Figure 3.27. A 2D spiral inductor.

3.3.3 Planar Inductor

An alternative method to couple the YBCO and GNRFET subsystems, in order to avoid resistive contacts or possible effects from superconductor-normal conductor junctions, is to couple the two systems via mutual inductance or coupled striplines. Two planar inductors coiled together can act as a coplanar transformer with sufficiently-high coupling, though with a nontrivial self-inductance component.

Spiral inductors, like the one shown in Fig. 3.27, allow for easy 2D inductors and transformers. However, the value of their inductance is very hard to precisely calculate. Variations of the following equation are commonly used [187]:

$$L \approx K_1 \mu_0 \frac{n^2 d_{\text{avg}}}{1 + K_2 \rho} \tag{3.35}$$

$K_{1,2}$ are layout-dependent constants, $d_{\text{avg}} \approx (n+1)r$ is the average coil diameter for an inner radius of r and n turns, and $\rho = (d_{\text{out}} - d_{\text{in}})/(d_{\text{out}} + d_{\text{in}}) \approx (n-1)/(n+1)$ is the filling factor. This expression has an alternative form:

$$L \approx \frac{\mu n^2 d_{\text{avg}} c_1}{2}\left(\ln\frac{c_2}{\rho} + c_3\rho + c_4\rho^2\right) \tag{3.36}$$

with geometry-dependent constants c_{1-4}. Ref. [187] lists $c_1 = 1.00$, $c_2 = 2.46$, $c_3 = 0.00$, and $c_4 = 0.20$ for a circular inductor, with $\rho \to 1$ as the number of turns increases. These equations serve only as an approximation for L, as other factors will certainly affect the overall inductance. This reference also lists another monomial expression that better estimates inductances, but tends to be more coil- and lookup-table-dependent.

Ideally, for a pair of coupled striplines, the gap width and line length should be $\lambda/4$, where λ is the signal wavelength [188]. This is because each stripline acts, in theory, as an antenna. Because the wavelengths in this research are on the order of millimeters to centimeters, the ability to use coupled striplines is minimal. Despite this, they are still considered in Chapter 4 with prior knowledge that their transmission properties will not be optimal.

Circuit Theory

While the circuit theory for the directly-coupled system has been discussed at-length previously [23], [24], this second methodology is new to this research. In a pair of coupled inductors, the system equations take the form:

$$\begin{aligned} V_1 &= L_1\frac{dI_1}{dt} + M\frac{dI_2}{dt} \\ V_2 &= M\frac{dI_1}{dt} + L_2\frac{dI_2}{dt} \end{aligned} \tag{3.37}$$

where $V_{1,2}$ are the voltages across the inductors, $L_{1,2}$ are the inductances of each inductor, $I_{1,2}$ are the currents entering each inductor (taken from the top), and $M = k\sqrt{L_1 L_2}$ is the mutual inductance, $k \leq 1$. In this system, it will be assumed that $L_1 = L_2$ for simplicity. Noting that the voltage across an output resistor, R_s on the secondary inductory will be

defined as $V_1 = V_{out} = -I_2 R_s$, the total system equations become (ignoring coupling and parasitic capacitances):

$$\begin{aligned} V_{cc} &= V_j(t) + V_1(t) \\ I_1(t) &= N I_j(t) \\ I_j(t) &= I_c \sin\left(\frac{2e}{\hbar} V_j(t) t\right) + C_j \frac{dV_j(t)}{dt} + V_j(t) G_j\left(V_j(t)\right) \\ \frac{V_1}{L} &= \frac{dI_1}{dt} + k\frac{dI_2}{dt} \\ -\frac{I_2 R_s}{L} &= k\frac{dI_1}{dt} + \frac{dI_2}{dt} \end{aligned} \tag{3.38}$$

Taking the assumptions that $V_j(t)$ is small ($V_j(t) < \Delta/2$) and approximately constant ($d_t V_j(t) \approx 0$), and defining $\omega \equiv \frac{2e}{\hbar} V_j$, this simplifies somewhat:

$$\begin{aligned} \frac{V_{cc} - \frac{\hbar\omega}{2e}}{L} &= N I_c \omega \cos\omega t + k\frac{dI_2}{dt} \\ -\frac{I_2 R_s}{L} &= N I_c k\omega \cos\omega t + \frac{dI_2}{dt} \end{aligned} \tag{3.39}$$

Solving the second ODE with these assumptions gives $I_2 = A\mathrm{e}^{-\alpha t} - N I_c k\omega \frac{\omega \sin\omega t + \alpha \cos\omega t}{\omega^2 + \alpha^2}$, defining $\alpha \equiv R_s/L$. Assuming that $LNI_c\omega \ll V_{cc}$ (i.e.: the voltage drop across the primary inductor is approximately zero, requiring minuscule inductances), then:

$$V_{cc} - \frac{\hbar\omega}{2e} \approx 0 \tag{3.40}$$

Which simplifies the solution to $\omega \approx 2eV_{cc}/\hbar = 2\pi V_{cc}/\Phi_0$ (for a frequency of $f \approx 2eV_{cc}/2\pi\hbar = V_{cc}/\Phi_0$). In other words, the junction voltage and the source voltage are approximately equal, so the junction frequency is roughly proportional to the source voltage as though the coupling inductors were not there. This requires the system to be set in a situation where the coupling inductances *do not dominate the system behavior*. The

approximation fails for situations where the inductive reactance is high enough to cause a significant voltage drop across the inductors.

Output voltage has minimal DC component (it decays away exponentially at a rate of α), but the AC component is:

$$V_{out(AC)} \approx NR_sI_ck\frac{\omega}{\sqrt{\omega^2+\alpha^2}} \approx \frac{NR_sI_ck}{\sqrt{1+\left(\frac{R_s}{L}\frac{\Phi_0}{2\pi V_{cc}}\right)^2}} \tag{3.41}$$

Simulation using three junctions ($I_c = 220\,\mu$A, $R_N = 9\,\Omega$, SGR = 100, $C_j = 0.018$ pF), $V_{cc} = 1$ mV, $R_s = 0.1\,\Omega$, coupled microstrip inductors with $L = 6$ pH (from a $t \times l \times w = 30 \times 150 \times 20$ superconductor microstrip with units in nanometers, separated from the ground plane by a distance of 250 nm), and arbitrarily setting $k = 0.9$ gives a frequency that varies slightly between 460 and 506 GHz, for a geometric mean of 483 GHz, which is as predicted. There *is* noticeable distortion in the signal, due to the inductance, resistance, and feedback coupling, which causes the signal to be non-sinusoidal (but still periodic). Incorporating the coupling capacitor corrects this issue (taking a rough value of $C_c = 10$ aF) and stabilizes the frequency at 484 GHz with no variation. The predicted output voltage is 59.4 μV, while the simulated output voltage is 55.3 μV, which is in close agreement (the disparity likely due to the coupling capacitance).

However, using more realistic values based on approximations made using the equations for a planar transformer with the values eventually presented in Table 4.3 ($L \approx 25$ pH, $C_c \approx 4$ fF, and $C_p \approx 500$ aF, $k \approx 0.71$) gives disappointing results. Because the inductive reactance is on the same order as the normal resistance of the junctions, the transformer instead acts as a voltage divider (as before), giving a dominant frequency of nearly half the predicted value at 237 GHz, plus severe distortion and other frequencies at play.

Using a higher supply voltage *does* begin to rectify the issue ($V_{cc} = 5$ mV creates a nearly-perfect sinusoid at 2.4 THz) Above 3 mV largely rectifies the issue as well, but also has an increased operational frequency, beyond the limitations of the amplifier. Alternatively, incorporating a 200 fF shunt capacitor parallel to C_p improves the frequency estimate (for this particular set of values) and decreases the distortion, but does not completely eliminate it. Furthermore, the behavior still has a long settling time (proportional to $\tau = \alpha^{-1} =$

L/R_s, or 250 ps). Incorporating a shunt resistor to the junctions or to C_p can also help decrease the distortion, but also affects settling time and decreases the magnitude. A shunt inductor ($L_{sh} \ll L$) to C_p also reduces distortion and helps restore the signal magnitude, but also affects the frequency and introduces a signal decay. A series capacitor, C_s selected so $(\sqrt{LC_s})^{-1} \approx 2eV_{cc}/\hbar$ placed between the junctions and the coupling inductor vastly improves both the frequency approximation and signal quality (i.e.: reduces distortion), but also limits the ability to dynamically tune the frequency of operation by controlling V_{cc} alone. Instead, the system is finely-tuned to one particular frequency.

Because of these issues, this method should be used with caution, with extensive tuning performed beforehand. While this system has potential to permit easier control of the junctions, circuit-level signal generation problems are an initial indicator that this method may not be as optimal as the previously-explored methodology.

3.3.4 Simulation Considerations

For simulations, the recommended aperture size for waveport simulations is of dimensions $(2kh + w) \times ((k+1)h + t)$, where k is a constant, $5 \leq k \leq 10$, typically, as illustrated in Fig. 3.28 [189]. This port aperture defines the simulation region, and is selected to incorporate as many necessary electromagnetic modes as possible with minimal error. This will be of fundamental importance when the transmission line types are simulated in the next chapter.

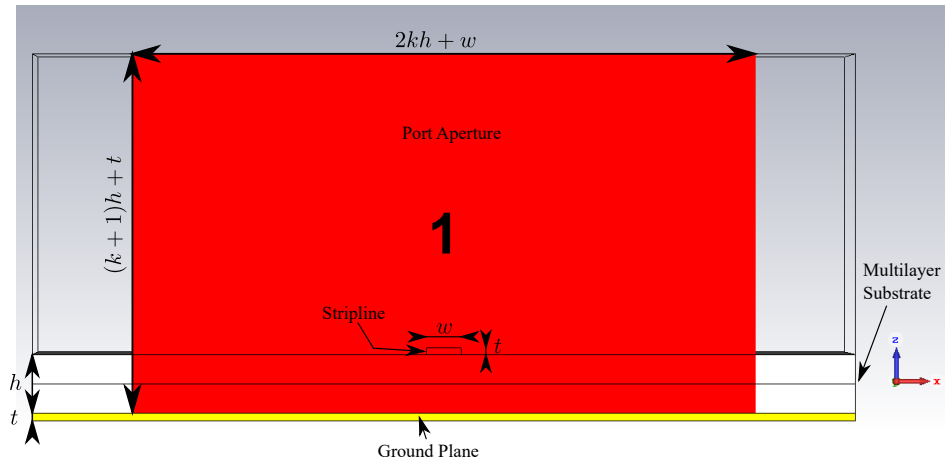

Figure 3.28. An illustration of a waveport of the appropriate aperture size, drawn in CST Studio. The "1" is the port number (port "1" of a two-port network)

4. DEVICE INTERFACING

4.1 Interface Limitations

Before the means of integrating the superconductor and nanotechnology systems can be determined, the physical limitations between them should be discussed. These show up as substrate, process, and junction limitations, primarily, as thermal limitations are not truly an issue [23], [24], [26], and the critical currents and magnetic fields for YBCO are much higher than those present in this system.

4.1.1 Substrate Limitations

Superconductors

Because of the complex mechanisms driving superconductivity, it is to no surprise, especially with the phonon-electron interactions characteristic of the BCS theory, that superconductors frequently need some form of lattice-matching between the material and the substrate in order to maintain a high J_c and regularity of crystal formation [3], [4], [190]. Indeed, it is challenging enough to grow single-crystal HTS materials [4]; trying to do so on a substrate not matched to the lattice parameters would be significantly harder. Furthermore, incorrect substrate types can lead to doping effects in materials such as YBCO, which can reduce, if not eliminate, its ability to superconduct. YBCO is particularly sensitive to oxygen, so special care needs to be taken when selecting a substrate that will not leak its oxygen into or leech oxygen from the YBCO [3], [4]. As such, a number of substrates have been utilized in the past, though they all have their own benefits and issues.

YBCO was originally investigated in free-standing situations (no substrate), as it took a decent amount of time to determine the appropriate process to deposit or grow YBCO on a substrate [44]. In such free-standing situations, YBCO of extremely-high-purity quality could be grown. However, with the desire to integrate YBCO into microwave applications, a substrate is still required. Magnesium oxide (MgO) was one of the first single substrates used, or as buffer layers between YBCO and silicon [191]–[194], along with strontium titanate (STO) [70], [191], [195]. MgO in particular has been used because of its extremely low loss-

Table 4.1. A list of substrates used for superconductive (YBCO) devices at microwave or EHF ranges and cryogenic temperatures. "–" indicates no data found.

Material	ϵ_r	$\tan\delta$	**Lattice Constant a (Å)**
MgO [196]	9.63	$< 2 \times 10^{-5}$	4.212
STO [197]–[199]	$300 - 2000$	$\sim 3 \times 10^{-4}$	3.905
Sapphire [197]	9.4	$< 2 \times 10^{-5}$	4.758
LAO [197], [199], [200]	~25-30	$< 3 \times 10^{-4}$	3.793
YSZ [201]–[203]	27.2-32.7	3×10^{-4}	5.12
$BaZrO_3$ [204], [205]	38.4	$< 2 \times 10^{-3}$	4.256
CeO_2 [206]	23-26	–	5.49

tangent, $\tan\delta \approx 10^{-6}$, at the MMW range (~100 GHz), as well as a comparatively-low $\epsilon_r = 9.6$, which helps reduce EHF losses. MgO may also be used as an insulator in typical processes as well, which benefits this research [191]. In Ref. [191], the optimal buffer layer was 15 nm MgO with 200 nm-thick YBCO is layered on top of silicon, resulting in $T_c = 82$ K, though no J_c was reported. The means of preparation of the MgO layer is also important: epitaxially-grown YBCO on MgO appears to work better than "as-prepared" MgO (i.e.: via methods akin to standard CVD) [192]. Ref. [193] reports high J_c far exceeding 1 MA·cm^{-2} below 77 K.

A second common substrate is yttria-stabilized zirconia (YSZ) [198], [207]–[212]. For EHF applications, a low ϵ_r is desired to minimize parasitic capacitances, which is what YSZ was originally intended for [212]. Single-crystal YSZ, by itself, however, does not exactly satisfy this in the EHF band, with numbers, depending on temperature and oxygen doping levels, up to $\epsilon_r = 27.2$ for 9 mol% yttria-doping, leading to high dielectric losses [201] (though this may be desirable for microwave-frequency resonators [210]). This is why thin YSZ on oxygen-annealed SiO_2 is selected to be a buffer layer, rather than the full substrate [208], [212]. The primary appeal of YSZ, however, was *not* originally as a substrate to layer on SiO_2, but as a way to form superconducting wires, as the biaxial crystal structure of YSZ is an ideal match for YBCO, allowing for higher J_c than what is offered on metallic substrates [207], and allows some means of wire-forming. An alternative to YSZ is $BaZrO_3$, which is chemically neutral at the temperatures required to grow YBCO, allowing higher-purity

single-crystal forms of YBCO to be grown [140]. A major downside to $BaZrO_3$, however, is its high dielectric constant: $\epsilon_r = 38.4$ at a little higher than 5 GHz [204].

Other substrates have been used as well. Cerium oxide (CeO_2) has been used on occasion, due to its similar physical properties to YSZ [195], [213]–[215]. It is also frequently paired with another substrate, sapphire (aluminum oxide, Al_2O_3 or ALO), which may also appear on its own due to its similar properties to MgO [139], [195], [214], [215]. It is most-frequently paired with sapphire simply because sapphire may affect the growth of YBCO in negative ways, such as causing cracks or chemical interactions with the barium in YBCO [214], [215]. Thus, the cerium oxide acts as an intermediary layer to buffer the YBCO from the ALO.

A viaration of ALO is lanthium aluminum oxide (LAO, $LaAlO_3$) [198], [216], which has even lower lattice mismatch than STO, but not as low of a mismatch as $NdGaO_3$ by comparison of absolute mismatch (-0.7 for LAO vs 0.4 for $NdGaO_3$) [198]. The $NdGaO_3$ substrate is rarely used, however, and LAO is exceptionally challenging, if not impossible, to grow on silicon [199]. Even graphene has been attempted as a substrate or buffer layer to align YBCO nanoparticles [217], though this method requires further research and refinement. All of the primary substrates are summarized in Table 4.1.

Graphene Nanoribbons

Graphene, because of its unique properties and strength, tends to have less sensitive substrate requirements than YBCO does. However, while graphene appears to be able to be layered on a great many substrates, there *are* still benefits to choosing certain materials over others, especially when comparing conductivity properties [31], [32], [146], [148], [200].

The most common of all substrates extends even to graphene: silicon-based substrates, especially SiO_2 [27]–[30], [218]. There are a couple problems with directly layering GNRs on SiO_2, in that the electrical and thermal conductivities both suffer due to phonon mode suppression/charge mobility reduction, and introduction of phonon mode scattering [32], [130], [153], [157]. Including a single layer of 2D hexagonal boron nitride (h-BN) as a buffer layer between a GNR and the real substrate significantly improves both thermal and electrical properties [32], [153], [157], [200]. As it turns out, other oxides, such as HfO_2, LAO, and

Table 4.2. A list of substrates used for GNR and GNRFET devices. "N.A." indicates the relevant information is not applicable for substrate purposes.

Material	ϵ_r	$\tan\delta$	**Lattice Constant a (Å)**
Undoped Si [224], [225]	11.7	$\sim 2.1 \times 10^{-3}$	5.431
SiO_2[199]	3.9	$\sim 10^{-3}$	4.9136
HfO_2 [199], [226], [227]	25	$\sim 5 \times 10^{-2}$	5.195
Sapphire [197]	9.4	$< 2 \times 10^{-5}$	4.758
SiC [228]	6.52-9.66	$\sim 3 \times 10^{-3}$	3.073-4.3596
h-BN Buffer [229]	N.A.	N.A.	2.502
LAO [197], [199], [200]	~25-30	$< 3 \times 10^{-4}$	3.793

sapphire (ALO), also function well with GNRs and GNRFETs, with the charge mobility increasing with ϵ_r [200]. This is particularly beneficial for GNRFETs, which do not have a proper substrate, per se, in double-gated configurations [27]–[30], [32], [160], [200]. Instead, in these devices, the gate dielectric acts identically to the substrate. Of these non-SiO_2 oxide insulators, HfO_2 is one of the most-commonly-selected insulators, due to its tried-and-true capabilities as a high-ϵ_r (high-κ) dielectric for other sub-micron transistor technologies [32], [148], [219], [220].

In single-gated GNRFET technologies, SiC is a popular second choice for the base substrate [26], [220]–[223]. This is, in part, due to its thermal properties (high thermal conductivity) [220], the ability to grow graphene directly on it from a sacrificial layer of SiC [26], [221]–[223], and its low-noise properties [221], [222]. However, GNRFETs that are constructed using SiC are typically SB-GNRFETs, as the SiC remains undoped.

The dielectric properties of these materials is summarized in Table 4.2, with some overlap with Table 4.1.

4.1.2 Process Limitations

There have been a number of ways that YBCO and graphene both have been grown or deposited on their respective substrates. However, finding a means by which both could be processes on the same chip without destroying one or the other is challenging. Not only the processes themselves, but the order they are performed may even have impact as, for

instance, preparing a YBCO process first and then a graphene process may end up resulting in extra oxygen dissolving into or leaking out of the YBCO, degrading performance [140].

YBCO itself has been layered via multiple-stage CVD and ion beam assisted deposition (IBAD) [208], [209], [212], [213], pulsed laser deposition (PLD) [192], [193], [195], [198], [217], [230], laser ablation [191], RF magnetron sputtering [191], [210], [214], plasma sputtering [215], metal organic deposition using trifluoroacetate salts (TFA-MOD) [211], thermocompression bonding [231], ink-jet colloidal solution printing [216], and the reactive thermal co-evaporation technique [194]. As can be seen, the IBAD and PLD processes are quite popular, each for their own reasons.

PLD is a process that can allow for very precise and easily-controlled growth of YBCO on its substrate, resulting in highly-ordered crystals. However, its high temperatures (650-800°C, or higher) can result in oxygen loss [212]. Furthermore, it may required the substrate to be pre-annealed, such as with oxygen-annealed MgO at temperatures exceeding 1000°C [192]. IBAD, on the other hand, after an initial annealing process, does not result in the same oxygen loss in the HTS. The reason for this is because IBAD is inherently faster [212]. While the temperatures are comparable, the speed differs sufficiently. For extremely thin films, however, this speed difference is not particularly important, and even laser ablation is comparable at a rate of approximately 4 Å/s [191]. Thus, the only real advantage IBAD has is for thick films or for systems where YBCO needs to be deposited quickly [213], or when highly-ordered YBCO needs layered on a metallic or multi-grain substrate [3], [4].

The primary issue here, and the main limitation, is when this process is combined with a graphene process. Namely, are similar or non-interfering processes possible to hybridize the system, especially if an *h*-BN buffer layer is used?

Graphene can be deposited on a substrate in a wide number of ways: Precursor molecules baked onto a substrate [124], [125], [232]–[234], surface-assisted molecular assembly [124], CNT unzipping [117]–[120], epitaxial deposition via spontaneous growth on SiC [26], [101], an improved method of CVD on a metallic catalyst [121], fabrication via a nanowire etch mask on sheet graphene [123], mechanical exfoliation [100], [128], and a combination of etching with precursor molecules and self-assembly [235]. A buffer of *h*-BN can be deposited in a very similar way, with GNRs layered on top with a variety of means [236].

Of these methods, CNT unzipping was one of the earliest methods, followed by CVD and etching. However, of the methods, the precursor molecule method appears to be more precise and accurate, allowing GNR self-assembly wherever they are to be connected, even to the point of atomically-precise fabrication [233]. This is important in particular, as the widths of AGNRs need to be controlled at an atomic level to precisely engineer the bandgap and current relations [66], [88], [106], [110], [113], [232], [237]–[239]. Another major benefit is that the precursor molecule method, particularly the one described in Ref. [233], can be performed at temperatures *below* those required for the YBCO process (between 200-400°C), indicating that the superconducting part of a hybrid chip should *not* be affected by the GNR layering process, if the GNRs are grown after the YBCO.

Thus, the process limitation is potentially resolved if an IBAD or PLD method is used to layer the HTS material on its substrate prior to the GNRs being layered via a precursor molecule methodology. Alternatively, GNRs may be layered with high precision on h-BN using a dry transfer method [236], [240].

4.1.3 Superconductor-to-Metal Junctions

When any wave experiences a heterojunction, there is simultaneously transmission and reflection of that wave [184]. This effect is not limited to classical waves, such as sound or light, but also to particles that act like waves, such electrons, or quasiparticles, like holes or phonons [33]. This is why S-parameters exist: to measure port scattering and transmission. Any kind of interface can be described as such a port [186], [241], particularly RF or quantum-mechanical systems.

In a normal system where a conductor is joined to or abutted against another conductor or an insulator, some electrons will be reflected, and some will be transmitted into the secondary material. In the case of a conductor-conductor junction, the transmission coefficients (S_{12} and S_{21}) are significantly higher than the reflection ones (S_{11} and S_{22}). As expected, in the conductor-insulator junction, the opposite is true. Furthermore, in the cases where it matters, angular momentum (spin) is also conserved: an electron (or hole) with quantum state $|s\rangle$ initially will remain in state $|s\rangle$ post-reflection [242].

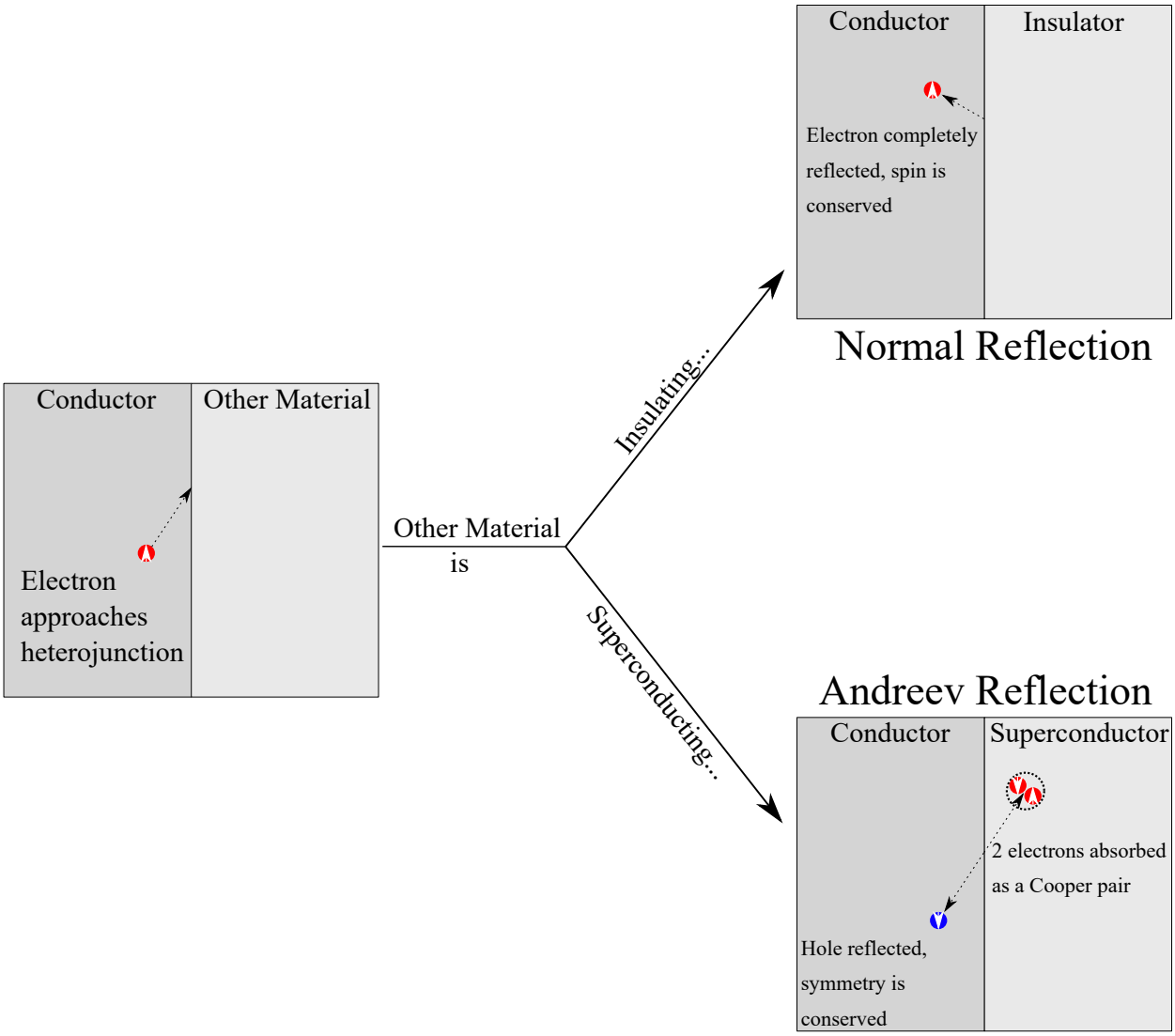

Figure 4.1. An illustration of a conductor-insulator/superconductor junction. The insulator (top) exhibits normal reflections, while the superconductor (bottom) exhibits Andreev reflections.

However, superconductor-normal metal junctions (SN junctions) exhibit more exotic properties. First, if the electrons in the normal metal are in a lower energy state than the superconducting gap Δ, then these electrons *cannot* penetrate into the superconductor, and instead reflect off of it. Current *may still flow* if a potential difference $V < \Delta/e$ exists across the junction, like in a Josephson junction, and is even referred to as a supercurrent. This is the result of a phenomenon called the *Andreev effect*, creating *Andreev reflections*. In this situation, the electron, and a secondary electron with opposite spin, are absorbed by

the superconductor to create a Cooper pair, and a hole is retroreflected off the junction with opposite velocity as to the original electron to conserve charge and momentum. This hole has a quantum state $|s_h\rangle = \mathcal{CPT}|s\rangle$, which, in a normal metal (e.g.: not ferromagnetic), has no overall effect on that metal's conductivity. Here, $\mathcal{CPT}$ represents the charge, parity, and time operators, which, in conjunction serve to invert the charge sign ($\mathcal{C}$), spin states ($\mathcal{P}$), and momentum direction ($\mathcal{T}$), causing retroreflection. This hole is also the same amount below the Fermi level as the original electron was above, indicating that energy is conserved (as a consequence of $\mathcal{CPT}$ being a unitary symmetry operation) [242]–[245]. This process is illustrated in Fig. 4.1, both for the conductor-insulator heterojunction and the SN junction.

Now, where the problem with the SN junction lies is in its overall effect: the *proximity effect*. This effect is where the normal metal starts exhibiting superconductor-like properties, such as the ability to carry Cooper pairs over extended lengths (the normal coherence length ξ_s), as the energy bands between the systems cannot change abruptly [3], [242]. This effect is, perhaps, the more troubling of the two effects because, though the metal can carry dissipation-free current for extended lengths [242], [244], the superconductor's critical temperature is reduced, depending on the film thickness, with thin ($t < 100$ nm) superconducting films having the greatest drop. However, this may be mitigated if the conductor thickness is less than the superconducting film's thickness [3], [244]. In such a case, the system may, over a short distance, benefit from the proximity effect, as the conductor is induced into quasi-superconduction.

With graphene, this distance may even extend to $\xi_s \approx 250$ nm [240], making it appealing for potential use in transmission lines between superconductor and normal conductor systems as done in this research, graphene-based Josephson junctions [240], and even *supercurrent transistors*, which are Josephson junctions whose critical current can be adjusted externally with some gate potential, V_G [246].

4.2 Proposed Schemes

Based on these limitations, there are several questions that need resolved in order to develop a proper lithography process. First is regarding the substrate. A common substrate

material is desirable and has the simplest interconnection methodology, but the possibility of a *hybrid substrate*, or a substrate consisting of different materials, is quite appealing due to thermal expansion and current density properties characteristic of the superconductor substrate limitations. There are several proposed schemes to resolve this question:

- Multilayer/3D structure: By creating floors, each with a different substrate targeting a specific technology and interconnecting them with TSVs (either normally-conducting or superconducting), the problem of thermal expansion may be resolved. However, due to the size of such constructs, the capacitances involved may exhibit parasitic effects, which introduces other issues such as: power losses, impedance mismatch, and excessive delay. Furthermore, TSVs and 3D structures are currently complicated to properly develop. As such, this methodology is not, ultimately, considered as an appropriate scheme for this system.

- Separate die structure: By creating two separate half-chips on separate dies and connecting the two via superconducting nanowires, the two structures may be capable of existing within the same packaging or system. This is not an ideal solution, as it introduces the potential for wire-based losses and undesirable electromagnetic effects.

- Embedded secondary substrate: By having a common substrate on top of which the nano-devices can be natively built, and in one section embedding a secondary or buffer substrate, it is possibility to be able to have both the superconductive devices and the nanotechnology devices on the same chip, potentially using similar lithography processes.

Now, if the common base substrate methodology is possible, then the questions regarding the types of interconnects between them has several possible solutions:

- Nanostrips/nanoribbons: The methodology of using nanostrips (with corresponding grounding plane) made of superconducting material or oriented sheet graphene is, perhaps, the simplest solution to the interconnection problem, though has its

own limitations that will need considered (such as delay, standing wave formation, and possible significant power loss).

- Superconducting nanowires: Similar to the nanostrips, nanowires made of superconducting material may permit extremely-low-loss signal transfer, with the added benefit of not requiring a direct grounding plane. They may even be constructed similarly to the nanostrips (i.e.: planar layered conductor), though may be radiative and potentially interfere with the highly-sensitive JJ/SQUID arrays.

- Coupled resonators: Due to the EHF electromagnetic waves for which the proposed systems are designed, a coupled-resonator or coupled-stripline system may be possible to minimize potential ohmic losses and maximize signal transmission speed. This could also limit superconducting-conducting junction effects, but may also result in inductive-coupling losses.

Waveguides and similar structures were initially considered as well, but two primary issues make such a scheme prohibitive. First, waveguides rely on finely-tuned sizes of antennas/tracks, which support only one wavelength or set of wavelengths and their harmonics. While narrow-bandwidth, high-selectivity systems benefit greatly from this feature, the goal of the motivation papers ([23] and [24]) requires high-bandwidth structures. Second, even with microwave-frequency CPW resonators [247]–[249], the size and scale of the resonators are prohibitively-large, needing to support millimeter or centimeter wavelengths. Thus, waveguides were eliminated from consideration.

All of these considerations need to be taken nearly simultaneously, and the results of the corresponding proposed schemes are presented in the following sections.

4.3 EHF Transmission Line Analysis

Assuming a common or hybrid substrate is possible, there are several possible means by which to transfer a signal from the superconductor subsection to the GNRFET subsection, as discussed in Chapter 3. A variety of types of interconnect schemes were simulated us-

ing CST Studio, and the dimensions used in all electromagnetic simulations testing these interconnection methods are shown in Table 4.3.

The ways the dimensions were chosen are as follows:

- Metal thickness t was selected based on the need for a thin metal layer relative to the substrate thickness h. Furthermore, work has already been done measuring electrical properties of YBCO at the listed thickness [139].
- Conductor width w was selected to be sufficiently larger than t (more than four times as large).
- Coupling distance g_c was selected to make coupled microstrips close enough to have intentional crosstalk, while maintaining distance controlled by potential design rules (keeping in mind the GNRFET channel width is 10-15 nm).
- Coil gap distance g was selected to permit two coils to be interwoven while keeping sufficient distance between them to follow potential design rules.
- Coil inner radius r was derived from w and g.
- Line length l was selected to give a worst-case line length. As the desire is to have interconnects as short as possible, a size chosen to be over fifty times larger than the GNRFETs (66-100 times as large) was chosen.
- Substrate height h was chosen to be sufficiently larger than the conductor thickness (over seven times larger). Larger heights contribute to higher surface inductances, though lower interconnect capacitances.
- Graphene height a is an empirical value.
- Aperture multiplier k is selected to simultaneously make simulations more accurate and keep the simulation times as short as possible.
- Graphene layers n_l is selected for two reasons. First, more than ten layers of graphene gives comparable or better performance of graphene-on-silicon to copper

Table 4.3. The dimensions used for transmission line simulations here. The values are approximate values, based strongly on values presented in a number of papers.

Dimension (*symbol*)	**Value**	**Units**
Conductor Thickness (t)	30	nm
Conductor Width (w)	150	nm
Coupling distance (g_c)	$w/4$	nm
Coil Gap Distance (g)	$4w$	nm
Coil Inner Radius (r)	$(g+w)/4$	nm
Line Length (l)	1	μm
Substrate Height (h)	250	nm
Graphene Height (a)	0.13	nm
Aperture Multiplier (k)	5	N.A.
Graphene Layers (n_l)	20	Layers
Coil Turns (n)	5	Turns
Hybrid Depth Ratio (p)	0.5	N.A.

[156]. Second, the simulation software does not work as well with extremely-thin/2D materials.

- Coil turns n was selected to combine the attempt to couple two spiral planar inductors while minimize their inductance and surface area.

- Hybrid Depth Ratio p is selected to give a rough approximate to the amount of the selected YBCO substrate (MgO) that could be layered on the amorphous silicon substrate. This measures the ratio of the silicon height to the total substrate height (leaving the MgO height ratio as $1-p$).

4.3.1 Directly-Coupled Transmission Lines

Fig. 4.2 shows a top-view layout method for the junction controller presented in [23] and [24] that utilizes the direct-coupling method.

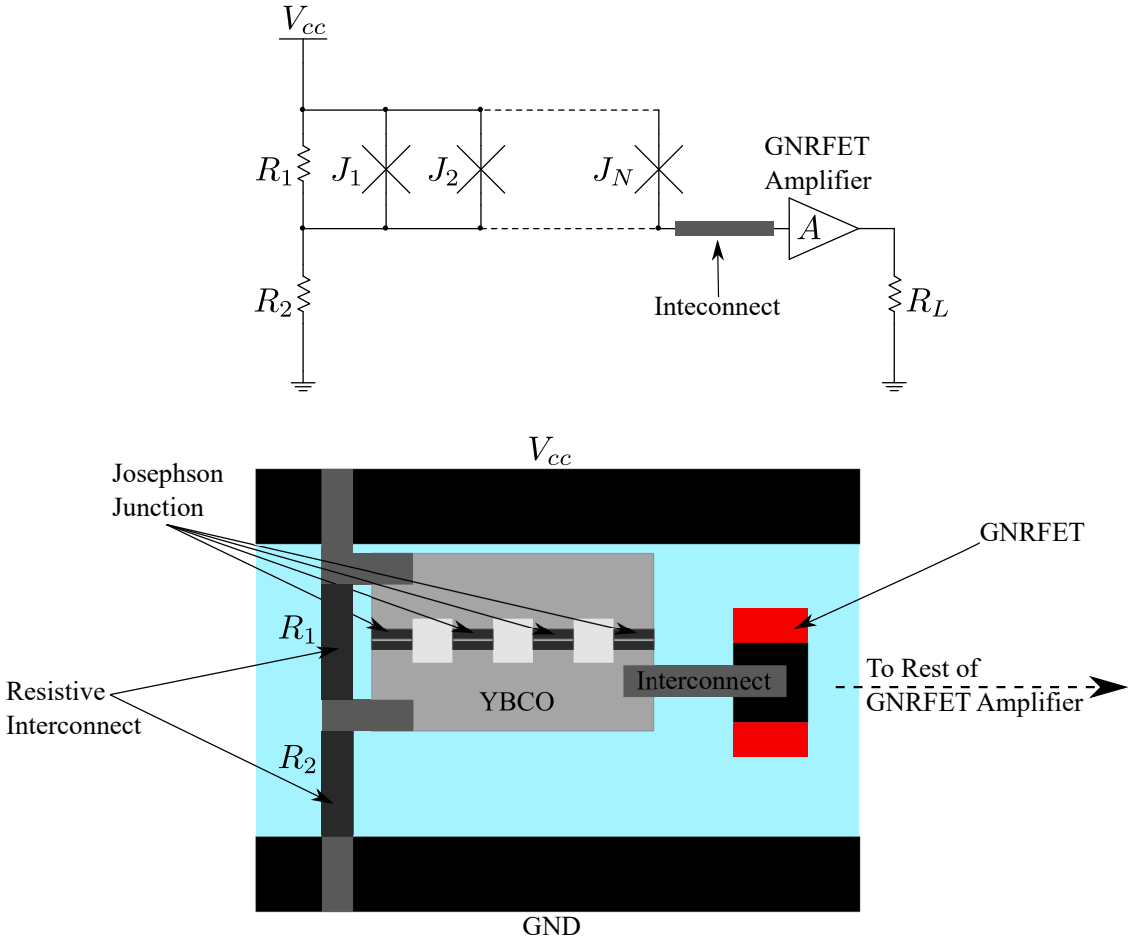

Figure 4.2. The schematic and corresponding rough layout for a system that relies upon physical interconnects between the YBCO and GNRFET systems.

Superconductive Transmission Lines

Using CST Studio, a micron-length superconducting transmission line was simulated over a frequency range of 1 to 300 GHz to determine its S-parameters over the valid range of frequencies for this system. This serves to predict the amount of signal power pulled from the superconductor that is actually transmitted to the end and the amount of power that was reflected. It was designed as shown in Fig. 3.3 using a hybrid substrate of MgO on lossy silicon. CST Studio does not have built-in superconductive materials, so the surface impedance values were generated using the code in Appendix B and imported into CST Studio as a frequency-defined conductance. Fig. 4.3 shows the input excitation power and the corresponding reflected and transmitted signals in the top plot. As can be seen, a vast

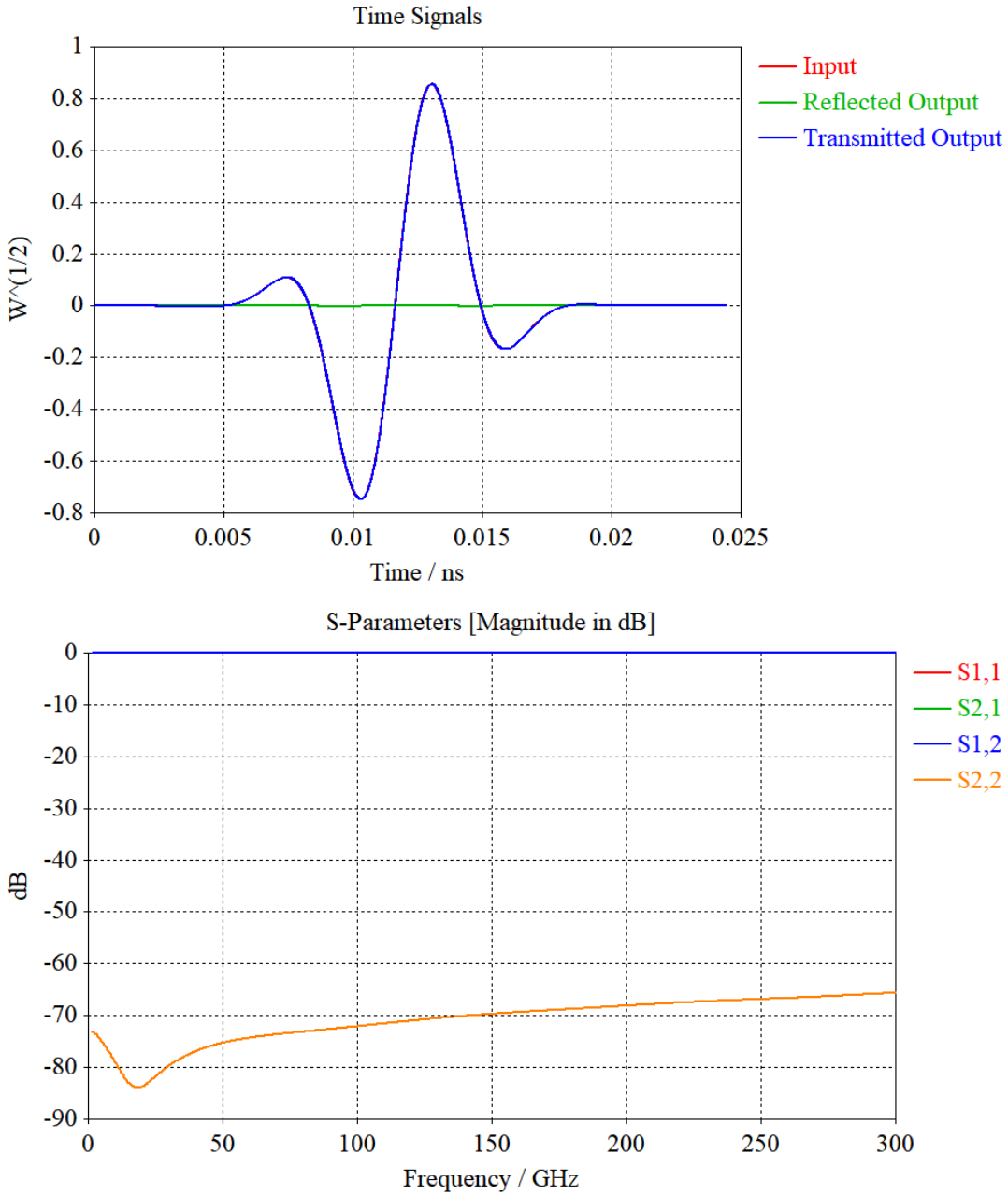

Figure 4.3. The input excitation into the superconducting microstrip line and the scattered and transmitted outputs (top), and the corresponding S-parameters (bottom).

majority of the power is transmitted rather than reflected. This is further demonstrated in the lower image in the same figure, which shows the S-parameters. As required, S_{12} and S_{21} are nearly maximal (0 dB gain), while S_{11} and S_{22} are extremely low (≤ -60 dB).

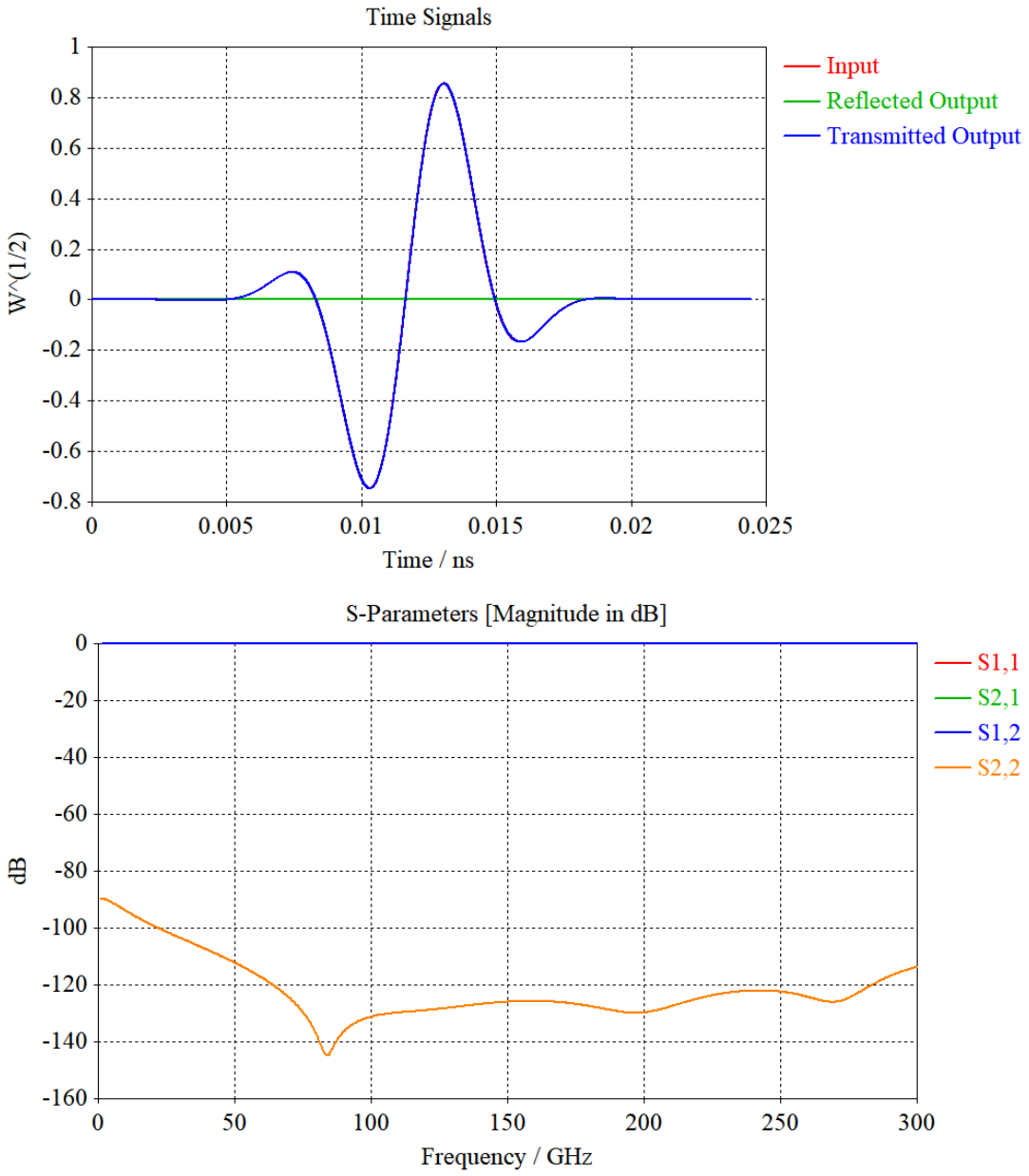

Figure 4.4. The input excitation into the graphene microstrip line and the scattered and transmitted outputs (top), and the corresponding S-parameters (bottom).

GNR-based Transmission Lines

The Superconductor-GNR Hybrid Line

Similarly, graphene is not a built-in material to CST Studio, but can be defined as a conductive material. Using the conductivity of graphene on silicon with twenty layers, a

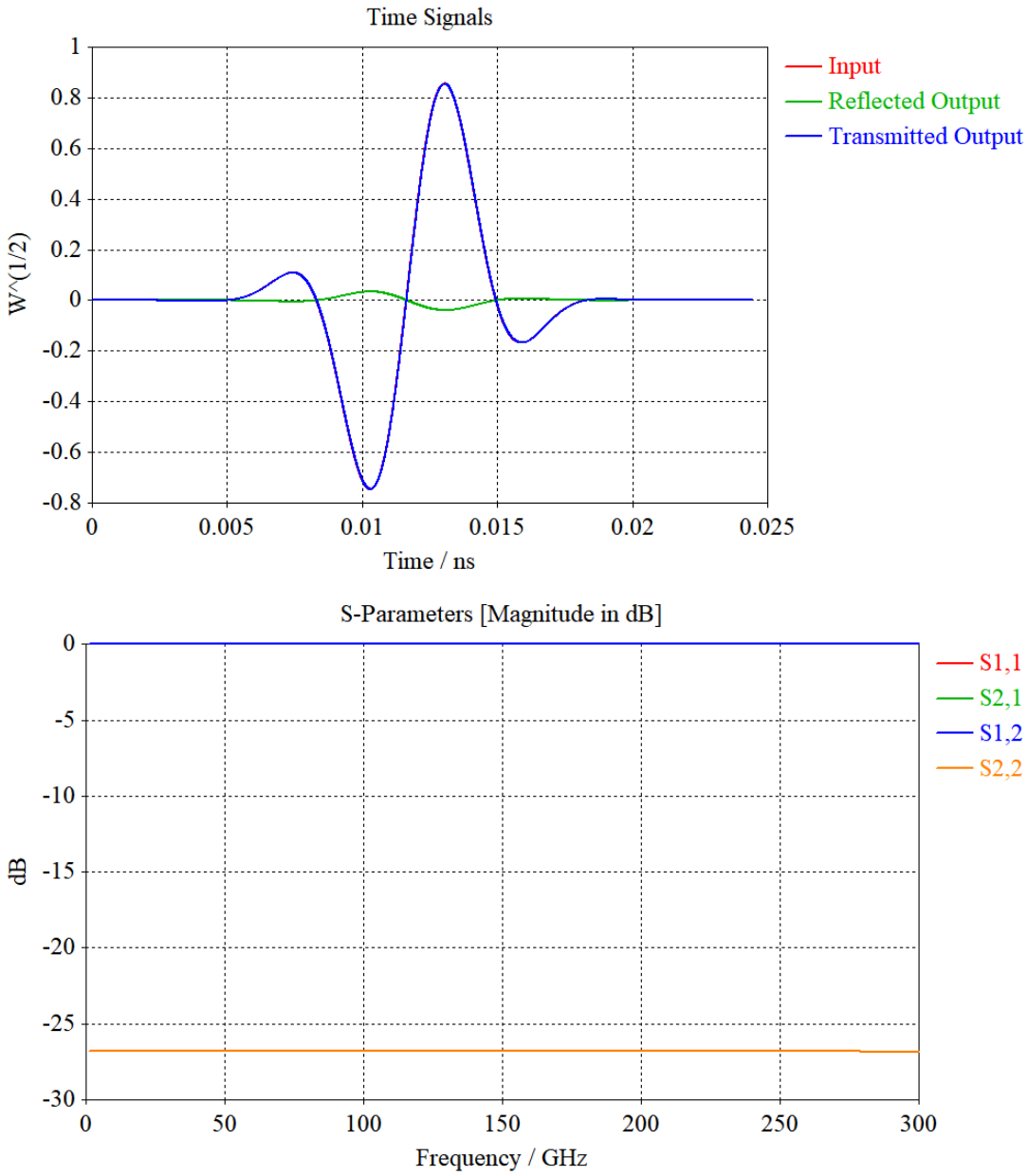

Figure 4.5. The input excitation into the hybrid microstrip line and the scattered and transmitted outputs (top), and the corresponding S-parameters (bottom).

micro-length graphene transmission line was simulated over the same frequency range. This serves to predict the amount of power the transmission lines between GNRFETs would be able to properly transmit or reflect. Fig. 4.4 shows the power signal in the top half,

with the reflected and transmitted signals, and in the bottom half shows the S-parameters. Interestingly-enough, the S-parameters for this graphene transmission line are actually *better* than the superconductive ones. This is likely due to how there are no superconductive surface impedances (kinetic impedances) combined with the higher overall normal conductivity of graphene, even graphene-on-silicon than YBCO. Graphene *is* still a lossy material, but for AC signals it appears to potentially transmit signals better.

The interface between a superconducting and graphene-based transmission line was then simulated in CST Studio over the same frequency ranges as before, with the graphene overlapping the YBCO and remaining suspended over the substrate. The conductivity of the graphene was adjusted for this suspension. As expected, the contact between the dissimilar materials leads to extremely decreased performance compared to each material type individually (with S_{11} and S_{22} increasing by between 40 and 120 dB compared to those shown in Figs. 4.3 and 4.4), as seen in the lower half of Fig. 4.5, with the reflected power signal now visible in the top half of Fig. 4.5, but still exhibits exceptionally-good transmission over the micron length transmission line.

4.3.2 Indirectly-Coupled Transmission Lines

This method utilizes the indirect-coupling method (or electromagnetic coupling) between two systems, as discussed in Ch. 3.3.3. A top-view example is given in the layout of Fig. 4.6, utilizing a coplanar transformer architecture.

Coupled Line Electromagnetic Simulations

Fig. 4.7 shows 3D layouts of the coupled microstrip and gapless coupled microstrip setups, respectively. Each one is one micron long, and the input/output feedlines are each of length $2w$ to keep them short. Each strip only has one feedline as the lower end is directly connected to the ground plane through vias. The bends are intentionally rounded off in order to reduce points of concentrated charge and electric fields. The grey striplines are made of YBCO, while the yellow ones are made from copper (as graphene on silicon has comparable

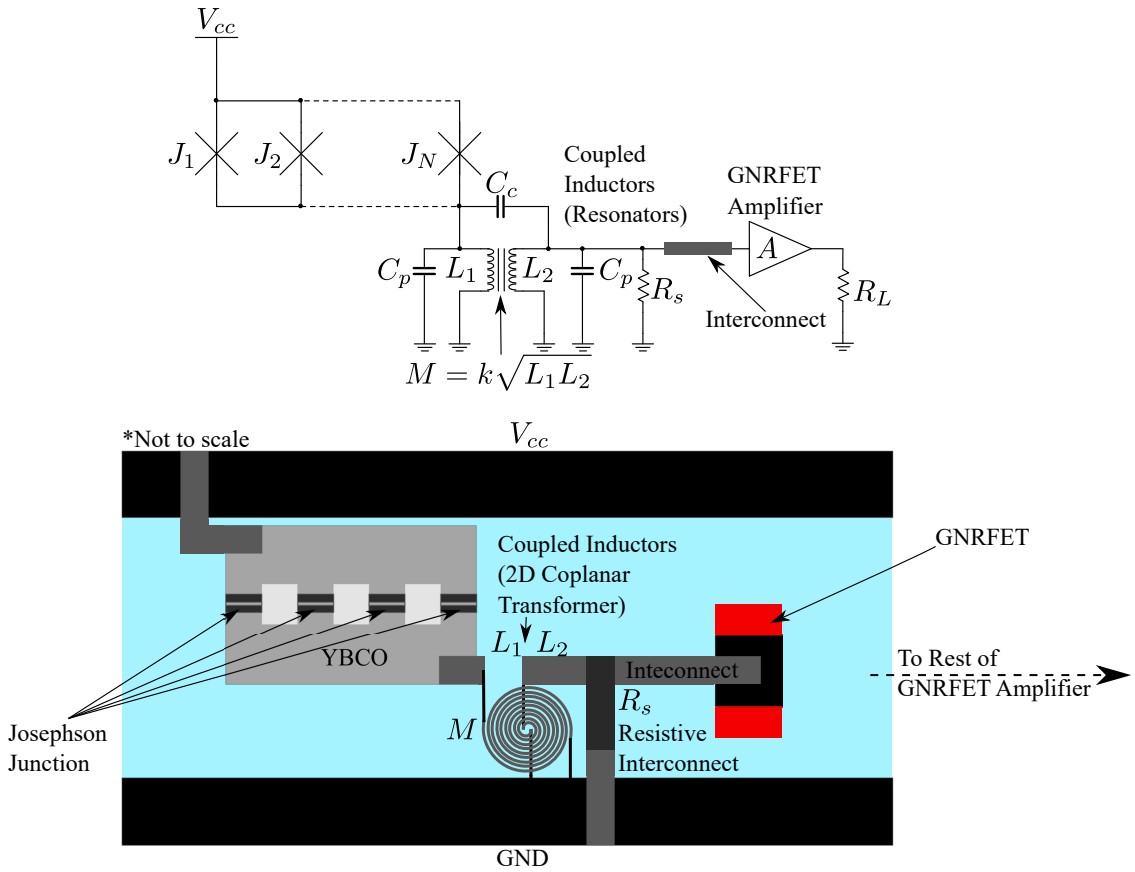

Figure 4.6. The schematic and corresponding rough layout for a system that relies upon coupling between the YBCO and GNRFET systems. The coupling method demonstrated here utilizes a coplanar transformer.

or inferior conductivity than copper [157]). The eventual graphene-to-copper transition is not considered here.

As can be seen in the power signals and S-parameters presented in Figs. 4.8 and 4.9, these types of couplers do not perform well. While the gapless coupler performs "better" than the one with a gap, both are extremely self-reflective and cause distortions in the transmitted signal as compared to the input signal. As such, these microstrip couplers are not suitable to act as coupled inductors.

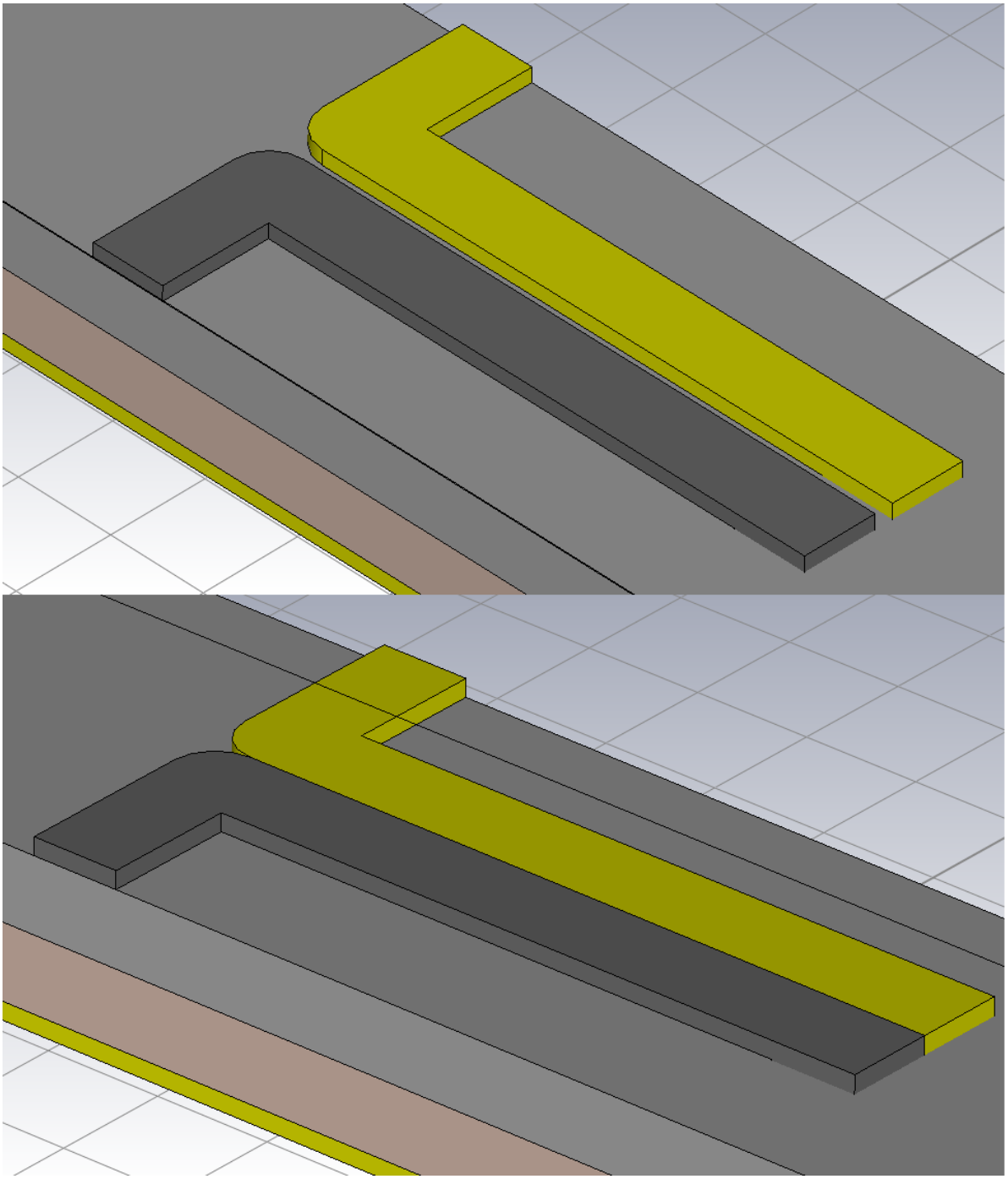

Figure 4.7. The 3D layout for the coupled microstrip setup. The ends of the strips are connected to the ground plane by vias. The grey stripline is YBCO, and the yellow one is copper. The top layout has a gap of size g_c, and the bottom layout is gapless.

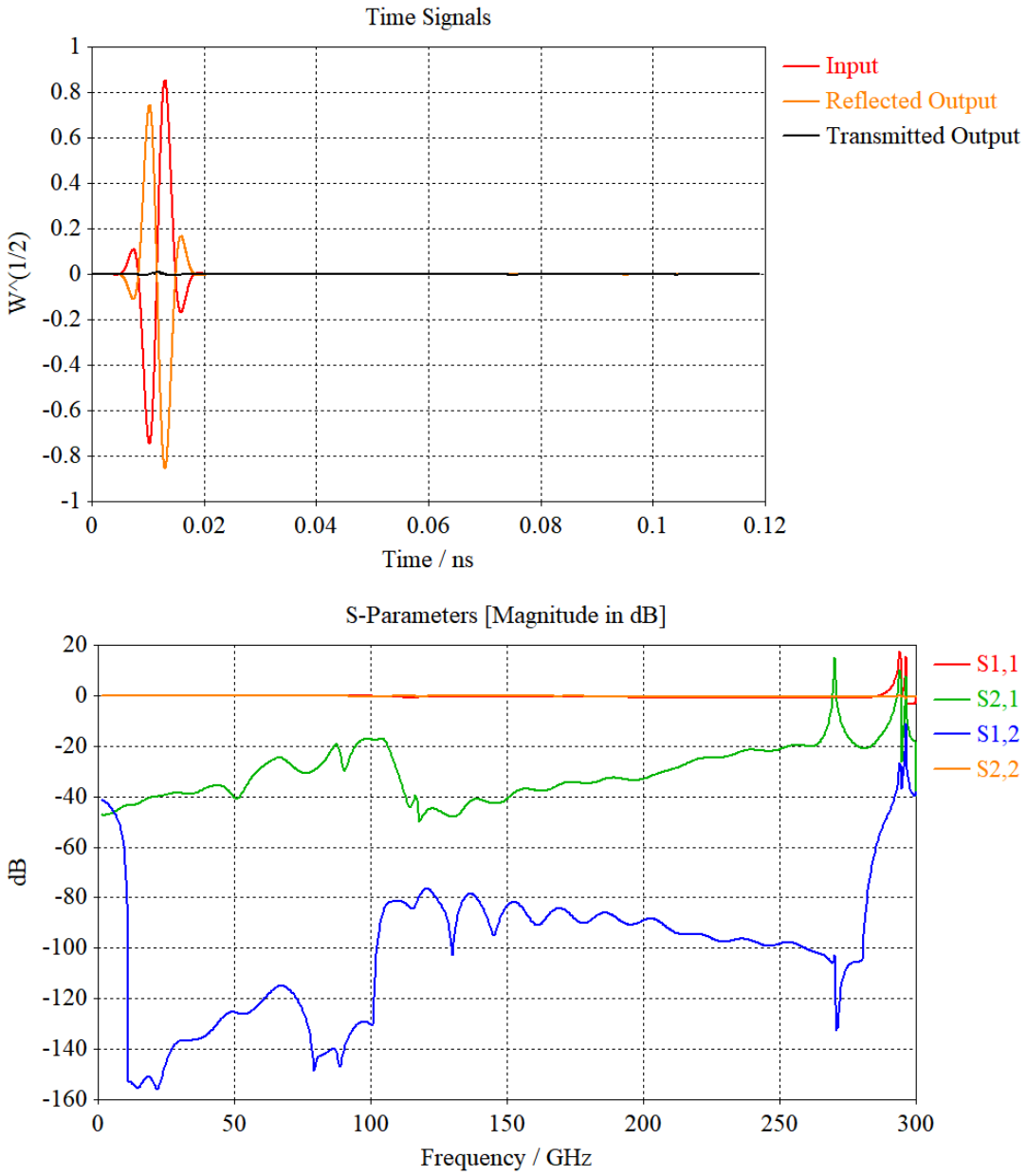

Figure 4.8. The input excitation into the coupled microstrip line and the scattered and transmitted outputs (top), and the corresponding S-parameters (bottom).

Planar Transformer Electromagnetic Simulations

The electromagnetic simulations add to this layout's issues. Fig. 4.10 shows the layout for the planar transformer, with the waveports left visible for scale. Immediately, the 8

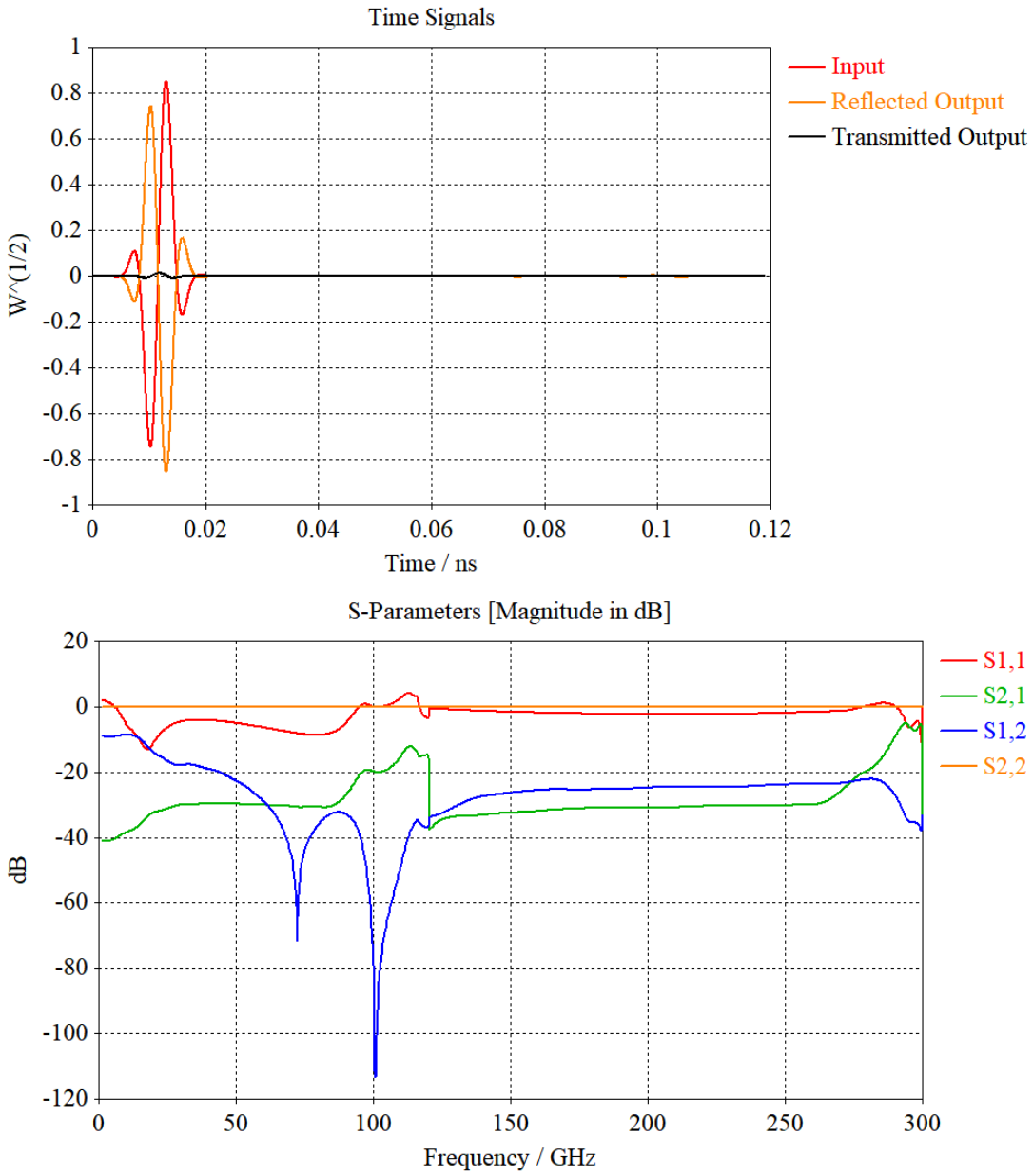

Figure 4.9. The input excitation into the direct-contact coupled microstrip line and the scattered and transmitted outputs (top), and the corresponding S-parameters (bottom).

μm outer diameter is somewhat alarming, comparing the size of this coil to the rest of the system. The approximate inductance for this coil is 24.6 pH, which, like the coil, too is large for this application. As discussed before, this large inductance causes major distortion in

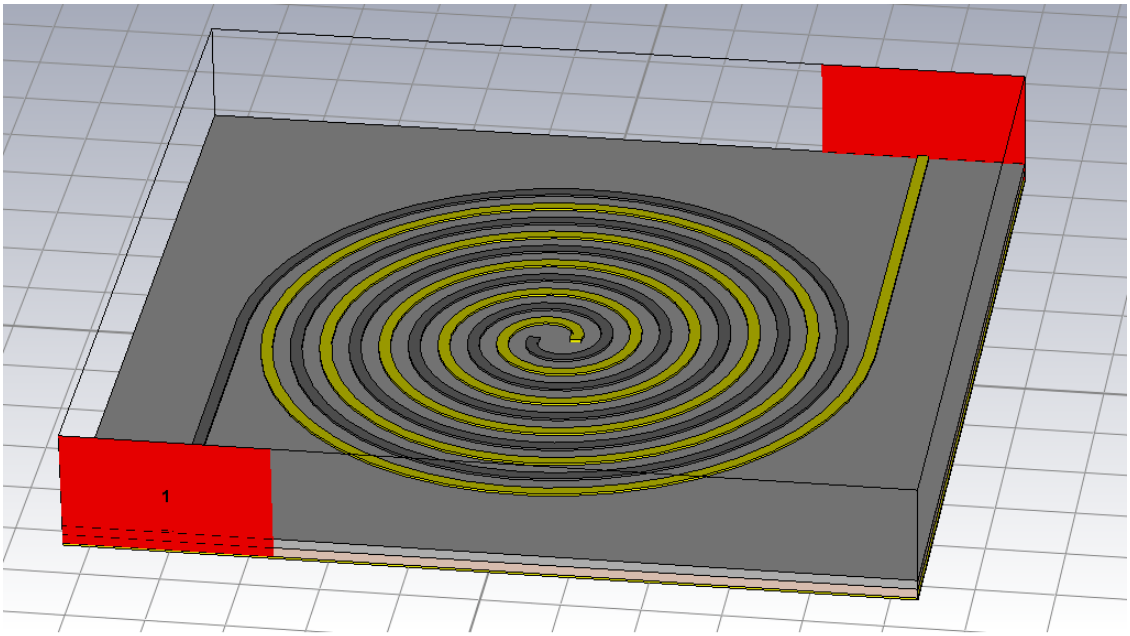

Figure 4.10. The 3D layout for the planar transformer. The grey coil is YBCO, and the yellow one is copper. The internal endpoints of both are connected to ground by vias.

the Josephson junctions' output signals and cannot be ignored in the frequency prediction calculations, leading to a high-order polynomial for ω.

Fig. 4.11 shows the transmitted power signals and S-parameters. It can be immediately seen that, while this design performs significantly better than the coupled microstrip lines, it still has unsuitably-large signal reflections (over half of the input power is reflected back). In this case, the input-to-output signal distortion is minimal, as the transmitted output signal at least resembles and keeps the shape of the input signal with a phase shift.

4.4 Conclusions and Proposed Process

Based on the substrate differences and limitations, the process limitations, the potential for the proximity effect, and the major issues with the coupled inductors tied with that particular system's frequency-control issues, there are a few potential solutions that may permit for a hybridized system.

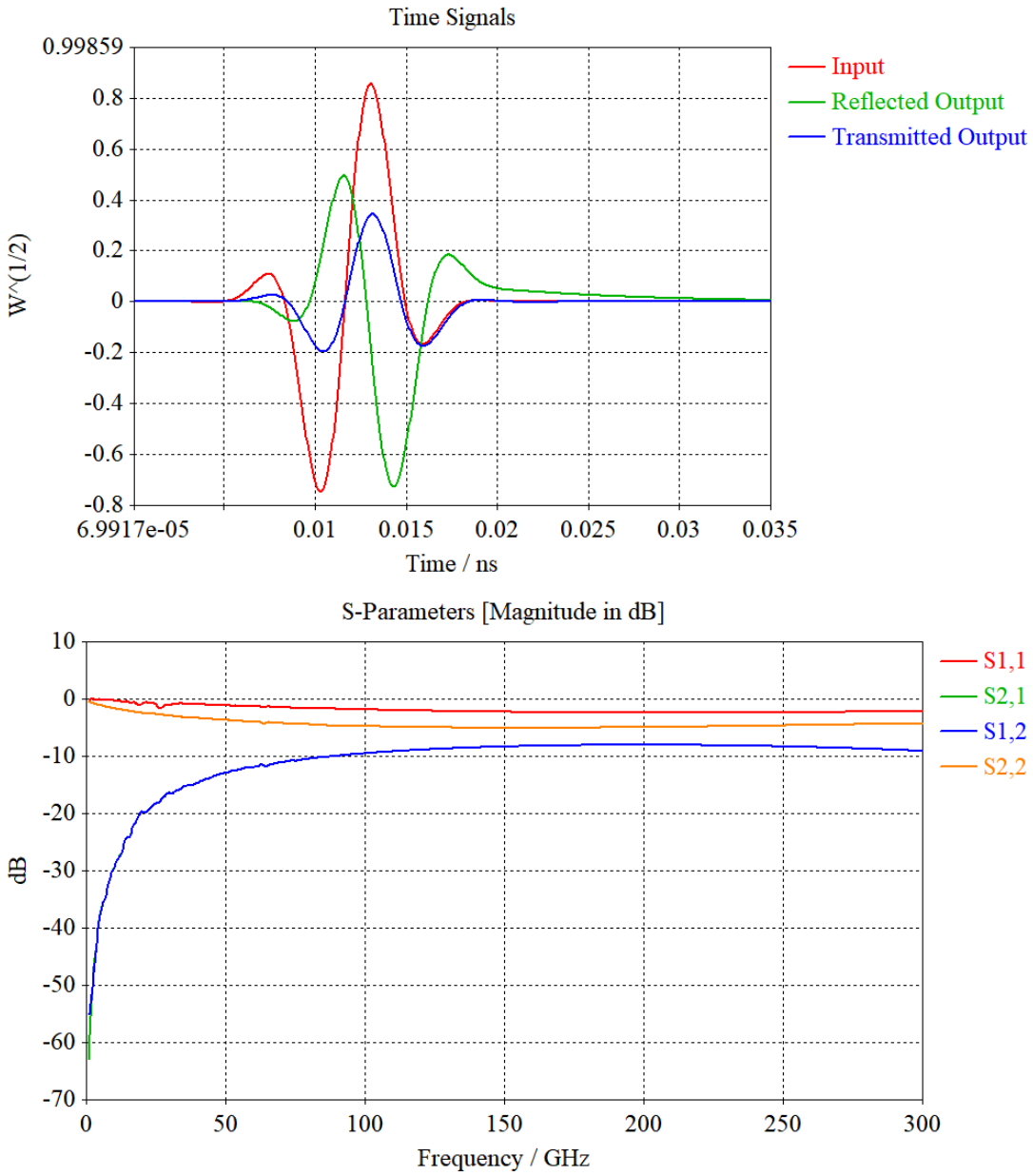

Figure 4.11. The input excitation into the planar transformer and the scattered and transmitted outputs (top), and the corresponding S-parameters (bottom). The reflections are asymmetric, while transmission parameters are approximately equal.

For the general connection type, the transmission line methodology should be used, utilizing the "direct-connection" system corresponding to the circuits designed in Refs. [23] and [24]. Connecting the YBCO to graphene, based on the simulations shown in Sec. 4.3.1,

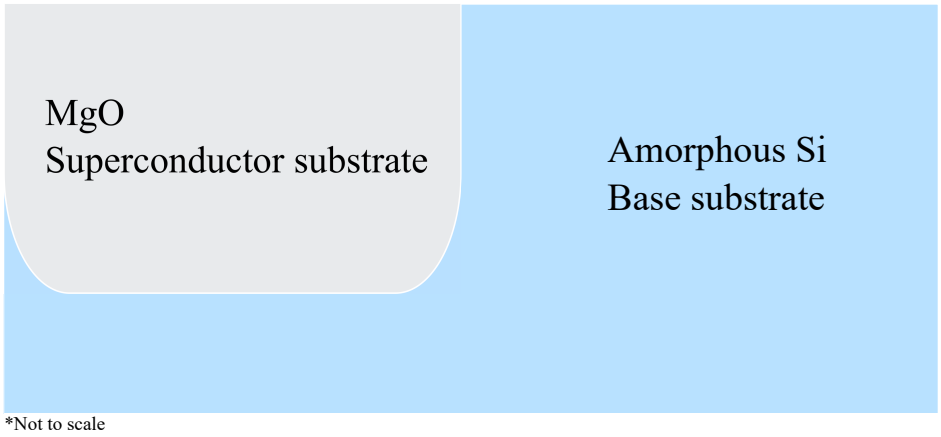

Figure 4.12. The proposed substrate solution for the hybrid system

should pose minimal issues with properly transferring power from the junction controller circuit to the GNRFET cascade amplifier.

In regards to the substrate: as it was described, there are numerous substrates upon which YBCO may be layered. However, not all of them can be layered on amorphous silicon. Of these, MgO and YSZ (or $BaZrO_3$) are the most promising. Despite how old the MgO process is, it has been proven to be able to be layered on silicon quite easily, and has one of the smallest ϵ_r and $\tan\delta$ values, which makes it desirable for this system, beating out even YSZ. It does not have the same issues that YSZ exhibits (namely, oxygen-related destruction of YBCO), and can easily hold YBCO structures. If, on the base substrate, MgO is layered in a specific etched-out region, then YBCO may be grown on the same die as the graphene-based devices. Thus, the proposed substrate would appear as shown in Fig. 4.12.

At this point is where the major process differences come into play. As discussed in Sec. 4.1.2, the process for growing graphene on its substrates differs drastically from that of the superconductor growth methodologies. Thus, the YBCO should be grown first, then the silicon doped (if necessary) and then h-BN and graphene sheets/GNRs layered on top of the appropriate regions. The exact process depends on the GNRFET in use (the double-gated GNRFET from Ref. [32] is used here), and the type of interconnects at play, but the "general" process is illustrated in Fig. 4.13.

After a layer of amorphous silicon is layered upon some kind of back gate material (gold is recommended based on how frequently it is used in the literature) and MgO is embedded

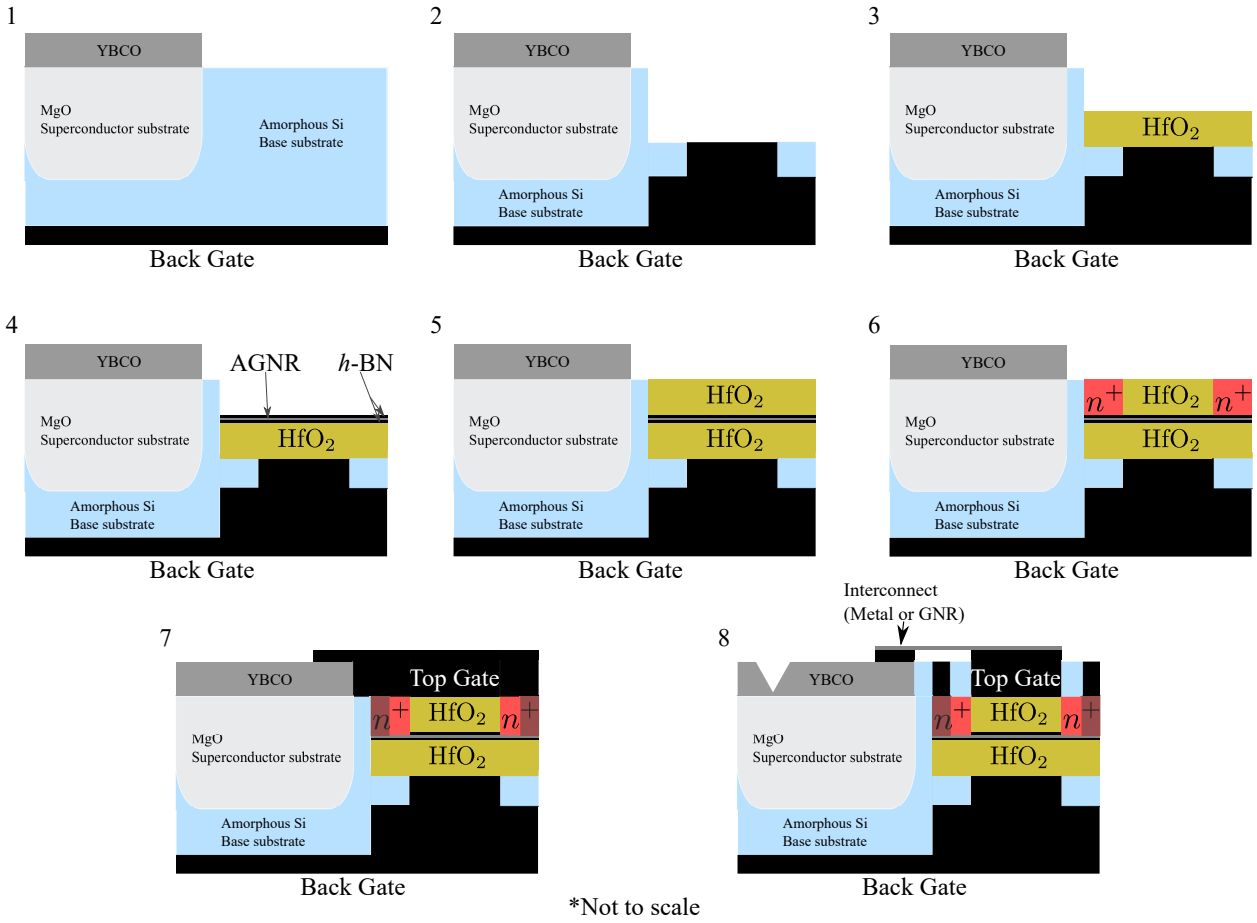

Figure 4.13. The proposed construction process.

within the silicon, then the hybrid system can be fully constructed. The proposed high-level process for a full-contact transmission line-based hybrid system is as follows (each step corresponding to that number in Fig. 4.13):

1. YBCO is layered upon MgO via the IBAD process. The YBCO thickness should be dictated by the size and style of the junctions in use.

2. The area on top of which the GNRFETs are to be grown is etched or otherwise carved away and filled with the same metal as the back gate so that the GNRFETs may sit on it approximately level with the top of the silicon, so higher metal layers may properly connect after the GNRFETs are fully grown. This back gate will be synonymous with the ground while in use. A section of the metal should be etched

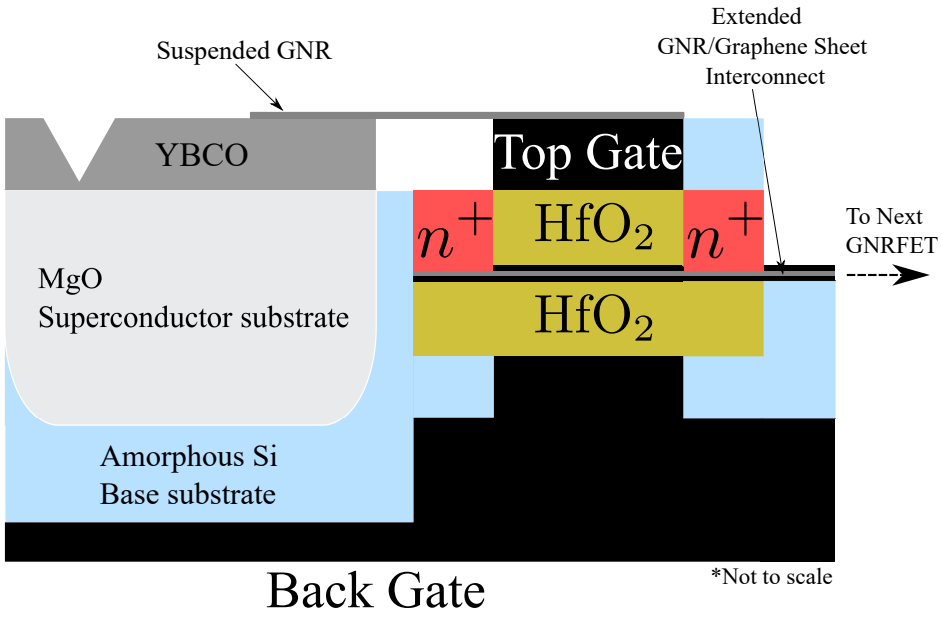

Figure 4.14. An alternative post-process layout incorporating suspended GNR/graphene sheet for an interconnect between the YBCO and gate of the GNRFET and demonstrates the GNRFET-to-GNRFET interconnect.

away to allow silicon to be sputtered back on. This forms the spacing between the gate material and the gate itself, while also controlling the actual gate width.

3. HfO_2 is grown or layered upon the back gate material and silicon to a thickness of t_{ox} for the oxide layer.

4. Single-layer h-BN is grown upon the oxide layer via a wet or dry transfer method, or via CVD. The AGNRs are then grown upon the h-BN either by a dry transfer method or precursor chemical method, and another layer of h-BN is deposited on top of the AGNRs.

5. Another layer of oxide is deposited on top of the top h-BN layer to the same thickness t_{ox}.

6. The transistor drain and source are formed via implantation into the oxide. Alternatively, these wells may be etched out first, filled with silicon, and then the dopants implanted into that silicon. Diffusion should not be used, as the high heat and dopant vapor may damage the YBCO. The construction shown in Fig. 4.13

uses n^+ doping, but because hole and electron mobilities are equal in GNRFETs ($\mu_e = \mu_p$), a p^+ doping can be performed as well using an effectively-identical process.

7. The top gate, made of the same material as the bottom gate, is layered on top of the oxide, with some overlap over the YBCO to form an SN junction. During this process, vias from the metal layer to the GNRs of the drain/source of the GNRFET need to be created to permit conduction between the contacts/metal layer (and associated external contacts on the metal layer) and these terminals.

8. Finally, the excess material between the top gate and contacts should be etched away so the top gate is no longer shorted to the drain/source, and the rest of the metal layer processed. Afterwards, the Josephson junctions should be etched (assuming the junction style from Ref. [70]) via some form of laser ablation or ion-beam etching. Finally, some extra metal is layered on the YBCO and top gate and either a metal or graphene-based interconnect ties the YBCO to the top gate (per the usage in this research).

Alternatively, to minimize metal usage and to maximize graphene's or GNRs' conductivity, a layout as seen in Fig. 4.14 can be achieved by connecting graphene directly to the top gate and YBCO (the graphene itself forming the SN junction), and the graphene at the drain/source terminals extended to physically connect elsewhere, depending on the circuit/application layout geometry.

5. FUTURE WORK

This system is entirely based on simulation, and while the individual simulations themselves are based on published experimental data, there is still inherent uncertainty in simulations, no matter how rigorous. As such, the need for physical verification is significant. In regards to future work in the experimental realm, there are several things that could take place.

First and foremost, the processes by which GNRFETs are made need to be unified. As discussed, there are a surprising number of different types of GNRFET architectures, with the double-gated GNRFET being one of the most common. However, there is no easy or singular way to make these devices, even though many advancements in creating width-precise and edge-engineered GNRs have been made in the past decade. Future work could bring a more rigorous and complete set of design rules and lithography processes to the GNRFET, making it a viable option for more widespread experimental analysis, rather than having to rely on access to an in-house nanofabrication laboratory and custom design rules for every layout and system.

Along the same lines of thought, noise in GNRFETs needs to be studied in greater depth. While noise in graphene sheet and GFETs has been studied extensively, it has not been investigated to nearly the same degree as in GNRs or GNRFETs. Between a theoretical approach and an experimental one based on the advancements made in the previous point, noise properties could be better-understood for future work with these devices, whether for analog or digital applications. This is particularly important, as GNRFETs are, theoretically, ultra-low-power devices and have the potential to operate on exceptionally-low voltage signals due to graphene's charge mobilities and ballistic transport properties. However, if the noise floor for these devices is too high, then the practicality of using GNRFETs for ultra-low-power or voltage signal amplification becomes questionable.

Putting these two pieces together could lead to one particularly-impactful piece of future research: physically constructing and testing the GNRFET amplifier designed in Refs. [23] and [24] and refined in Ch. 3.2 in order to verify or reveal unforeseen problems with such a high-bandwidth, low-power amplifier, and to unveil unanticipated or obscure limitations of the SPICE model. This would also require future work to fully design a stable series of easily-

controlled GNRFET current sources for I_{DS} and DC voltage biasing for V_{GS} for setting the operational point of the amplifier, plus fully exploring the effects of fully-realistic (e.g.: non-simplistic and based on complex 2D material phenomenon) graphene-based interconnects and a full layout for such an amplifier.

Similarly, future physical work on the Josephson junctions should explore a variety of means to construct said junctions, preferably at nano-scale sizes, utilizing YBCO. Extensive research has gone into this subject already, but still there is no one way to make them reliably and easily. Low-temperature superconductor junctions have been nearly perfected by this point, but there is still research to be done on making easily-controlled and precise YBCO junctions.

With the perfection of the junction would come experimental verification of the so-called junction controller upon which this research's motivation rests, combined with a practical GNRFET amplifier. The coupled inductor systems have, at the moment, insufficient performance for consideration, but the resistor-based controller with direct coupling to the amplifier holds promise. However, it, like the GNRFET amplifiers, lacks experimental data beyond the physical data used to construct the individual models, and, as such, needs to be physically implemented and tested to confirm that the design would work as intended, or reveal potential as-of-yet-unknown problems.

Should the system work as designed or with some experimentally-determined modifications, then there are a number of future research applications a system such as this may lend itself toward. Examples include, but are not limited to: phase-locked loops using the junctions as the VCO; terahertz imaging using the system to generate high-frequency outputs; high-speed communications or computational structures using the system to provide a several-hundred-gigahertz clock; deep-space applications where cryogenic temperatures are the norm; and various types of high-sensitivity sensor structures utilizing the inherent SQUID-like structure of the required junction array.

There are some serious practicality concerns, however, that may also be points of future research. For these frequency ranges, GNRFET systems are *not* unique. For instance, GaN- or other III-V-material-based amplifiers have become extremely popular in the past few years and have made serious advances in areas such as low-temperature power amplifiers

[96], energy-efficient systems and amplifiers [94], [250]–[252], high-temperature electronics [253], general high-bandwidth/HEMT power amplifiers [85]–[87], [175]–[177], [254], [255], and MMW/THz generation and detection [93], [256]. Photonics is another area that covers the same ranges of frequencies – or higher – and has seen many similar successes, especially in communications.

Another potential question of practicality is whether or not the method developed here is the best way to go about controlling and hybridizing superconducting devices with nanotechnology devices. The reason for this question is based on how Josephson junctions have been utilized since the early days of their existence. While the AC effect *is* notable, it is frequently combined with the junctions' ability to output a DC offset or even frequency modulation in the AC generated signal voltage signal directly proportional to the radiation frequency applied to them (Shapiro steps [3]). This in turn is frequently measured via the electric flux across the junctions/SQUIDs, making them ideal sensors for electromagnetic flux and for modulating/demodulating potential FM-type signals. Because the measurement of the signals is done indirectly by flux measurements, the junctions can be *extremely* easily-controlled, contrary to the purely-voltaic control and signal output utilized here. As such, future work should dedicate itself to determining which, in the long run, is a better approach to controlling and interfacing with these junctions, especially considering what the proximity effect may induce in the resistive components used in the motivational controller design.

Yet another major question of practicality deals with the size difference between the superconductive and the GNRFET systems. At the moment, the YBCO-based technologies are on the micron scale while the GNRFET systems are on the order of 15 nm. The mixing of these two length scales is incredibly challenging, if not entirely impractical, with the need of ultra-precise and highly-accurate lithography for the GNRFETs and the large-scale, lower-precision YBCO processes. This *can* be resolved by using LTS materials (such as niobium-based junctions), which can be formed into nanoscale Josephson junctions with relative ease [3]. Such a solution would also negate the need for different lithography processes, as LTS materials can be layered directly on silicon with minimal issues. However, the primary problem then becomes cooling, because while liquid nitrogen can be used for the

HTS junctions, putting the system at roughly 77 K, even the higher critical temperatures of Nb_3Ge ($T_c = 23.2$ K) would require extensive cooling capabilities, likely from liquid helium. And while it is known that sub-10 nm GNRFETs *can* operate at these temperatures [26], it is currently unclear as to the lower limit of GNRFETs' temperature ranges, or potential issues in the amplifier itself should the the system be cooled that far. These questions require future experimental investigation to properly answer.

With that said, in spite of the potential practicality issues, there is great potential for this system and systems derived from it for application in future work in the areas of ultra-low-power and EHF systems, especially in cryogenic environments.

6. SUMMARY

In this thesis, a method to hybridize superconducting and non-superconducting nanotechnologies into one system was explored and developed, with various processes and layout options investigated and unified into a single proposed methodology. Many practical considerations for developing such a physical superconductor-nanotechnology hybrid system were investigated, such as how the superconductive systems can be integrated on-chip with graphene-based nanotechnological systems, which have fundamentally-different layouts, scales, substrates, and manufacturing processes.

In order to confirm, from a circuit-level investigation, the feasibility of such a system, the GNRFET amplifier from the original motivational research was improved and optimized to operate at cryogenic temperatures in EHF range, between 159-269 GHz, with absolute stability and a relatively-low noise figure of 2.97-4.33 dB at 0.21 mW per stage. The inclusion of non-ideal, simple transmission lines into the simulations further demonstrated the circuit-level feasibility of such a hybrid system. The simulated cryogenic operation also showed that, if a common or hybrid substrate could be found, then the GNRFET half of the system could exist on the same chip, unaffected by the temperatures required for the superconducting components.

For the physical layout of the proposed system, it was determined that a YBCO-based junction could be grown on an intermediary substrate between the standard insulating substrate used as the foundation for the graphene/GNRFET devices. As such, from a substrate perspective, there were no physical limitations prohibiting the graphene-based subsystem from co-existing on the same overall chip structure as the superconducting subsystem. MgO was selected for this substrate, as it is a close electromagnetic match to amorphous silicon, and YBCO-on-MgO-on-silicon has been studied extensively in the past, with promising results.

A process by which the two systems could be physically built simultaneously was also proposed, given that it was shown that they could co-exist in a monolithic structure. Because the YBCO is physically much larger (~4 μm compared to ~15 nm) and its growth process requires much higher temperatures than those for graphene or GNRFETs ($>$ 1000°C com-

pared to 450°C), which may physically break down or oxidize under such temperatures and oxygen-rich atmospheres as is required (converting into carbon dioxide), it was determined that the superconducting devices should be grown first. The GNRFET growth process can then be safely performed with minimal impact on the oxygen doping levels of the YBCO, which can vary significantly if the YBCO is heated excessively on an oxygen-rich substrate. The rest of the process for each subsystem could then be completed normally, with the junctions being etched and the rest of the GNRFET layers developed. Because of this, it was not necessary to consider multi-floored structures or separate-die structures, and their corresponding interconnect methodologies.

The method for physically controlling and interfacing the two technologies was also explored in greater depth, comparing the behavior between a direct-contact controller as designed in prior research and an indirectly-coupled system as proposed here. It was found that transmission lines consisting of YBCO and graphene work exceptionally well, with even the transition from one technology to the next through ohmic contact having minimal power losses and self reflections under -25 dB over an operating range of 300 GHz. Meanwhile, the indirect coupling methodology had several problems with it from the start, from the extreme distortion in the junction-generated signals to the unpredictability of the signal frequency due to relatively-high inductances. Even if these circuit-level problems were ignored, electromagnetic simulations of various couplers revealed that the power losses and signal reflections/distortions were far too high, nearing 100% loss, and the required sizes of the systems to resolve these issues were prohibitively-large – on the order of several millimeters or centimeters. As such, the indirect coupling method was ruled out, and the original junction controller and direct-coupling system was found to be suitable for this system.

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A. SPICE AND VERILOG-A MODELING

A.1 SPICE Model

```
*****************************************
* JOSEPHSON JUNCTION MODEL
*   ZACHARY COCHRAN
*   (C) 2020
*****************************************
* Ic - critical current (A, default: 100u)
* Rn - quasiparticle current resistance
*   beyond the subgap region (Ohms, default: 17)
* SGR - quasiparticle current resistance ratio
*   in the subgap region (Unitless, default: 20)
* C - the junction capacitance (F, default: 18f)
*****************************************
* constants used throughout:
* Planck's constant h = 6.62607E-34 m^2*kg/s
* pi = 3.14159265
* Fundamental charge e = 1.60218E-19 C
* Fundamental unit of flux PHI0 = 2.0678334E-15 WB
* Permittivity of free space epsilon_0 = 8.85418782E-12 F/m
*****************************************
.SUBCKT jjunction plus minus phi phi0 PARAMS:
+ Ic = 100u Rn = 17 SGR = 20 C = 0.018p

*****************************************
* ODE MODELING
*****************************************
Gphi phi phi0 value = {3.0385352E15*sdt(V(plus,minus))}
Raux phi phi0 1

*****************************************
* SYSTEM MODEL
*****************************************
Cjj plus minus {C}
*Rjj plus minus {Gn(V(phi))}
Gjj plus minus value = {Gj(V(phi,phi0))}
Grj plus minus value = {V(plus,minus)*Gn(V(plus,minus))}

*****************************************
* FUNCTIONS
*****************************************
.func Gn(V) {1/(Rsg(SGR) +
+ Rn*(1-SGR)/(1 + exp(-100*(V**2/(4*Delta(Ic,Rn)**2)
+ -1))))}
.func Gj(phi) {Ic*sin(phi)}
.func Delta(i,rn) {2*i*rn/3.14159265}
.func Rsg(r) {r*Rn}

.ENDS jjunction

```

A.2 Verilog-A Model

```
`include "constants.vams"
`include "disciplines.vams"

//*****************************************
//      JOSEPHSON JUNCTION MODEL
//      ZACHARY COCHRAN
//      (C) 2020
//*****************************************
module jjunction(PLUS, MINUS, PHI);

output PHI;                         //phase difference
inout PLUS, MINUS;                  //input/output nodes

electrical PLUS, MINUS;             //nodes are electrical nodes
rotational PHI;                     //phase measures a momentum
                                    //rotation difference

parameter real Ic = 220u;           //critical current (A)
parameter real Delta = 1.5m;        //subgap region (eV)
parameter real SGR = 40;            //subgap ratio
parameter real C = 18f;             //shunt capacitance (F)

real h = 6.62607004E-34;            //Planck's constant (m^2*kg/s)
real pi = 3.14159265;               //pi
real e = 1.60218E-19;               //fundamental charge (Q)
real epsilon_0 = 8.85418782E-12;//permitt. of free space (F/m)
real Rn = pi*Delta/(2*Ic);          //normal resistance (Ohm)
real Rsg = SGR*Rn;                  //subgap resistance (Ohm)
real Rv = Rn;                       //nominal voltage-dependent
                                    //resistance (Ohm)
real k = 100;                       //model constant

analog begin
//model the voltage-dependent subgap resistance
Rv = Rsg + (Rn-Rsg)/(1 + exp(-k*(V**2/(4*Delta**2)-1));

//model the quasiparticle conduction
I(PLUS,MINUS) <+ V(PLUS,MINUS)/Rv;
//model the quasiparticle angle/voltage relationship
Theta(PHI) <+ 4*pi*e/h*idt(V(PLUS,MINUS),0.0);
//model the capacitor
I(PLUS,MINUS) <+ C * ddt(V(PLUS,MINUS));
//model the Josephson supercurrent
I(PLUS,MINUS) <+ Ic*sin(Theta(PHI));

end

endmodule

```

B. MATLAB MODELING

B.1 MATLAB Superconducting Transmission Line Model

```
%superconducting_microstrip.m
clear;
close all;

beyondrange = false;    %is fc > our limit (from H)?
beyondranges = false;   %is fc > our limit (from S)?

%constants
c = 2.99792458e8;           %speed of light in vacuum (m/s)
epsilon_0 = 8.8541878e-12;  %permittivity of free space (F/m)
mu_0 = 4*pi*10^-7;          %permeability of free space (H/m)

Tc = 93.7;          %YBCO critical temperature (K)
lambda_L0 = 60e-9;  %YBCO London penetration depth (m)

% epsilon_r = 3.9;    %rel. perm. of SiO2
% epsilon_r = 11.55;  %rel. perm. of cryo. SiO2
% epsilon_r = 23.4;   %rel. perm. of HfO2
% epsilon_r = 300;    %rel. perm of STO
% epsilon_r = 27;     %rel. perm of YSZ
% epsilon_r = 9.6;    %rel. perm of MgO
epsilon_r = 10.6;     %rel. perm of Hybrid base
sigma_n = 10^6;     %normal conduction of YBCO @ T = 77K

T = 77;             %Temperature (K)
l = 1000e-9;        %microstrip length (m)
w = 150e-9;         %microstrip width (m)
h = 250e-9;         %substrate depth (m)
t = 30e-9;          %superconductor thickness (m)
lambda_L = lambda_L0*(1-(T/Tc)^4)^(-1/2);

minfexp = 9;                        %minimum frequency exponent
maxfexp = log10(1.5*10^13);         %maximum frequency exponent
N = 10000;                          %number of points

fexp = linspace(minfexp,maxfexp,N); %frequency exponent list
f = 10.^fexp;                       %frequency list (Hz)
omega = 2*pi*f;                     %^ in rad/s

exticks = fix(minfexp):fix(maxfexp);    %xticks exponent list
xt = (10.^exticks)/10^9;                %xticks list
lims = [10^(minfexp-9),10^(maxfexp-9)]; %x-axis limits

rd = t/lambda_L;    %depth ratio
zeta = 1 - ...
     rd/(2*coth(rd)) + ...
     sqrt(1 + (rd/(2*coth(rd)))^2); %superfluid energy
Rs = l*mu_0^2*lambda_L^3*sigma_n/(2*w) * ...
     omega.^2 * (T/Tc)^4;           %surface resistance
```

```
    Ls = l*mu_0*(h + 2*lambda_L*...
         coth(t/lambda_L))/(w);          %surface inductance
    %Ls = l*mu_0*(h + 2*lambda_L)/(w);   %surface inductance [thick appr.]
    Zs = Rs + 1j*omega*Ls;               %surface impedance
    ZsFT = zeta*Zs;                      %finite thickness surface
                                         %impedance
    % C = epsilon_r*l/(60*c*log(8*h/w + ...
    %     w/(4*h)));        %stripline capacitance model
    C = epsilon_r*epsilon_0*l*(w/h + ...
        0.77 + 1.06*(w/h)^0.25 + ...
        1.06*(t/h)^0.5);    %interconnect wire capacitance model

    Xc = -1j./(C*omega);    %reactance

    H = Xc./(ZsFT + Xc);    %transfer function

    %find the cutoff frequency from our transfer function
    fcidx = find(20*log(abs(H)) <= -3, 1);
    if(isempty(fcidx))
        fcidx = N;
        beyondrange = true;
    end

    %Z-parameters (C > 0)
    Z11 = ZsFT + Xc;
    Z12 = Xc;
    Z21 = Xc;
    Z22 = Xc;

    %Y-parameters (C = 0)
    Y11 = 1./ZsFT;
    Y12 = -Y11;
    Y21 = -Y11;
    Y22 = Y11;

    %convert to S-parameters
    Z0 = 50; %50-Ohm probe

    %the Z-parameter version - for C > 0
    Delta = (Z11 + Z0).*(Z22 + Z0) - Z12.*Z21;
    S11 = ((Z11-Z0).*(Z22+Z0)-Z12.*Z21)./Delta;
    S12 = 2*Z0.*Z12./Delta;
    S21 = 2*Z0.*Z21./Delta;
    S22 = ((Z11+Z0).*(Z22-Z0)-Z12.*Z21)./Delta;

    %the Y-parameter version - for C = 0
    % Delta = (1 + Z0*Y11).*(1+Z0*Y22) - Z0^2*Y12.*Y21;
    % S11 = ((1-Z0*Y11).*(1+Z0*Y22)+Z0^2*Y12.*Y21)./Delta;
    % S12 = -2*Z0*Y12./Delta;
    % S21 = -2*Z0*Y21./Delta;
    % S22 = ((1+Z0*Y11).*(1-Z0*Y22)+Z0^2*Y12.*Y21)./Delta;

    %dB vrsion
```

```
    S11db = 20*log10(abs(S11));
    S12db = 20*log10(abs(S12));
    S21db = 20*log10(abs(S21));
    S22db = 20*log10(abs(S22));

    %find the cutoff frequency from the S-parameters
    %this is a better measure of fc, as it discusses
    %the standing wave properties of the transmission line better
    fcidxs = find(S12db <= -3,1);
    if(isempty(fcidxs))
        fcidxs = N;
        beyondranges = true;
    end

    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    %plot all the things

    %Z_s^{FT}
    figure()
    subplot(1,2,1)
    loglog(f/10^9,real(ZsFT),'b', 'LineWidth',1)
    xlim(lims)
    xticks(xt)
    grid on
    set(gca,'TickLabelInterpreter','latex','FontSize',12)
    xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
           'FontSize', 16)
    ylabel('$\Re{Z_s^{FT}}$ ($\Omega$)',...
           'Interpreter', 'latex', 'FontSize', 16)

    subplot(1,2,2)
    loglog(f/10^9,imag(ZsFT),'r', 'LineWidth',1)
    xlim(lims)
    xticks(xt)
    grid on
    set(gca,'TickLabelInterpreter','latex','FontSize',12)
    xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
           'FontSize', 16)
    ylabel('$\Im{Z_s^{FT}}$ ($\Omega$)',...
           'Interpreter', 'latex', 'FontSize', 16)

    set(gcf,'Position',[322 498 1070 420])

    %H(s)
    figure()
    subplot(2,2,1)
    semilogx(f/10^9,real(H),'b', 'LineWidth',1)
    xlim(lims)
    xticks(xt)
    grid on
    set(gca,'TickLabelInterpreter','latex','FontSize',12)
    xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
```

```
        'FontSize', 16)
ylabel('$\Re{H(\omega)}$', 'Interpreter', 'latex',...
        'FontSize', 16)

subplot(2,2,3)
semilogx(f/10^9,imag(H),'r', 'LineWidth',1)
xlim(lims)
xticks(xt)
grid on
set(gca,'TickLabelInterpreter','latex','FontSize',12)
xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
        'FontSize', 16)
ylabel('$\Im{H(\omega)}$', 'Interpreter', 'latex',...
        'FontSize', 16)

subplot(2,2,2)
semilogx(f/10^9,20*log10(abs(H)),'k', 'LineWidth',1)
xlim(lims)
xticks(xt)
grid on
set(gca,'TickLabelInterpreter','latex','FontSize',12)
xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
        'FontSize', 16)
ylabel('$|H(\omega)|$ (dB)', 'Interpreter', 'latex',...
        'FontSize', 16)

subplot(2,2,4)
semilogx(f/10^9,atan2(imag(H),real(H)),'k', 'LineWidth',1)
xlim(lims)
xticks(xt)
grid on
set(gca,'TickLabelInterpreter','latex','FontSize',12)
xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
        'FontSize', 16)
ylabel('$\phi_{H(\omega)}$ (rad)', 'Interpreter', 'latex',...
        'FontSize', 16)

set(gcf,'Position',[322 153 1070 765])

%S
figure()
subplot(2,2,1)
semilogx(f/10^9,real(S11),'b',...
         f/10^9,imag(S11),'r','LineWidth',1);
xlim(lims)
xticks(xt)
grid on
set(gca,'TickLabelInterpreter','latex','FontSize',12)
xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
        'FontSize', 16)
ylabel('$S_{11}$', 'Interpreter', 'latex', 'FontSize', 16)
legend('$\Re{S_{11}}$','$\Im{S_{11}}$','Interpreter','latex',...
        'FontSize', 12, 'Location','nw')
```

```
209
210     subplot(2,2,2)
211     semilogx(f/10^9,real(S12),'b',...
212              f/10^9,imag(S12),'r','LineWidth',1);
213     xlim(lims)
214     xticks(xt)
215     grid on
216     set(gca,'TickLabelInterpreter','latex','FontSize',12)
217     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
218            'FontSize', 16)
219     ylabel('$S_{12}$', 'Interpreter', 'latex', 'FontSize', 16)
220     legend('$\Re{S_{12}}$','$\Im{S_{12}}$','Interpreter','latex',...
221            'FontSize', 12, 'Location','nw')
222
223     subplot(2,2,3)
224     semilogx(f/10^9,real(S21),'b',...
225              f/10^9,imag(S21),'r','LineWidth',1);
226     xlim(lims)
227     xticks(xt)
228     grid on
229     set(gca,'TickLabelInterpreter','latex','FontSize',12)
230     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
231            'FontSize', 16)
232     ylabel('$S_{21}$', 'Interpreter', 'latex', 'FontSize', 16)
233     legend('$\Re{S_{21}}$','$\Im{S_{21}}$','Interpreter','latex',...
234            'FontSize', 12, 'Location','nw')
235
236     subplot(2,2,4)
237     semilogx(f/10^9,real(S22),'b',...
238              f/10^9,imag(S22),'r','LineWidth',1);
239     xlim(lims)
240     xticks(xt)
241     grid on
242     set(gca,'TickLabelInterpreter','latex','FontSize',12)
243     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
244            'FontSize', 16)
245     ylabel('$S_{22}$', 'Interpreter', 'latex', 'FontSize', 16)
246     legend('$\Re{S_{22}}$','$\Im{S_{22}}$','Interpreter','latex',...
247            'FontSize', 12, 'Location','nw')
248
249     set(gcf,'Position',[322 153 1070 765])
250
251     %S (dB)
252     figure()
253     subplot(2,4,1)
254     semilogx(f/10^9,S11db,'k','LineWidth',1);
255     xlim(lims)
256     xticks(xt)
257     grid on
258     set(gca,'TickLabelInterpreter','latex','FontSize',12)
259     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
260            'FontSize', 16)
261     ylabel('$S_{11}$ (dB)', 'Interpreter', 'latex', 'FontSize', 16)
```

```
262
263     subplot(2,4,2)
264     semilogx(f/10^9,S12db,'k','LineWidth',1);
265     xlim(lims)
266     xticks(xt)
267     grid on
268     set(gca,'TickLabelInterpreter','latex','FontSize',12)
269     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
270            'FontSize', 16)
271     ylabel('$S_{12}$ (dB)', 'Interpreter', 'latex', 'FontSize', 16)
272
273     subplot(2,4,3)
274     semilogx(f/10^9,S21db,'k','LineWidth',1);
275     xlim(lims)
276     xticks(xt)
277     grid on
278     set(gca,'TickLabelInterpreter','latex','FontSize',12)
279     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
280            'FontSize', 16)
281     ylabel('$S_{21}$ (dB)', 'Interpreter', 'latex', 'FontSize', 16)
282
283     subplot(2,4,4)
284     semilogx(f/10^9,S22db,'k','LineWidth',1);
285     xlim(lims)
286     xticks(xt)
287     grid on
288     set(gca,'TickLabelInterpreter','latex','FontSize',12)
289     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
290            'FontSize', 16)
291     ylabel('$S_{22}$ (dB)', 'Interpreter', 'latex', 'FontSize', 16)
292
293     % set(gcf,'Position',[322 153 1070 765])
294
295     %S (rad)
296     % figure()
297     subplot(2,4,5)
298     semilogx(f/10^9,phase(S11),'k','LineWidth',1);
299     xlim(lims)
300     xticks(xt)
301     grid on
302     set(gca,'TickLabelInterpreter','latex','FontSize',12)
303     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
304            'FontSize', 16)
305     ylabel('$\phi_{S_{11}}$ (rad)', 'Interpreter', 'latex',...
306            'FontSize', 16)
307
308     subplot(2,4,6)
309     semilogx(f/10^9,phase(S12),'k','LineWidth',1);
310     xlim(lims)
311     xticks(xt)
312     grid on
313     set(gca,'TickLabelInterpreter','latex','FontSize',12)
314     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
```

```
315             'FontSize', 16)
316     ylabel('$\phi_{S_{12}}$ (rad)', 'Interpreter', 'latex',.
317             'FontSize', 16)
318
319     subplot(2,4,7)
320     semilogx(f/10^9,phase(S21),'k','LineWidth',1);
321     xlim(lims)
322     xticks(xt)
323     grid on
324     set(gca,'TickLabelInterpreter','latex','FontSize',12)
325     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
326             'FontSize', 16)
327     ylabel('$\phi_{S_{21}}$ (rad)', 'Interpreter', 'latex',...
328             'FontSize', 16)
329
330     subplot(2,4,8)
331     semilogx(f/10^9,phase(S22),'k','LineWidth',1);
332     xlim(lims)
333     xticks(xt)
334     grid on
335     set(gca,'TickLabelInterpreter','latex','FontSize',12)
336     xlabel('Frequency (GHz)', 'Interpreter', 'latex',...
337             'FontSize', 16)
338     ylabel('$\phi_{S_{22}}$ (rad)', 'Interpreter', 'latex',...
339             'FontSize', 16)
340
341     % set(gcf,'Position',[322 153 1070 765])
342     set(gcf,'Position',[31 143 1871 765])
343
344     fprintf("Capacitance       : %.3f aF\n", C*10^18);
345     if(~beyondrange)
346         fprintf("H Cutoff Frequency: %.3f THz\n",f(fcidx)/10^12)
347     else
348         fprintf("H Cutoff Frequency: >%.3f THz\n",f(fcidx)/10^12)
349     end
350     if(~beyondranges)
351         fprintf("S Cutoff Frequency: %.3f THz\n",f(fcidxs)/10^12)
352     else
353         fprintf("S Cutoff Frequency: >%.3f THz\n",f(fcidxs)/10^12)
354     end
355
356     %save the data as a matrix and write to a CSV for later use
357     %It saves as f (GHz), Re(ZsFT) (Ohm/sq), Im(ZsFT) (Ohm/sq)
358     p = 0.01;                %percentage of data to save (1 = 100%)
359     maxpoints = fix(N*p);    %the number of points to save
360     datastep = fix(N/maxpoints);    %the datastep
361     data = [(f*10^-9)',real(ZsFT*t)',imag(ZsFT*t)'];
362     writematrix(data(1:datastep:N,:),'f_ZsFT.csv');
363
```