THE DESIGN, FABRICATION, AND CHARACTERIZATION OF WAFFLE-SUBSTRATE-BASED N-CHANNEL IGBTS IN 4H-SIC

by

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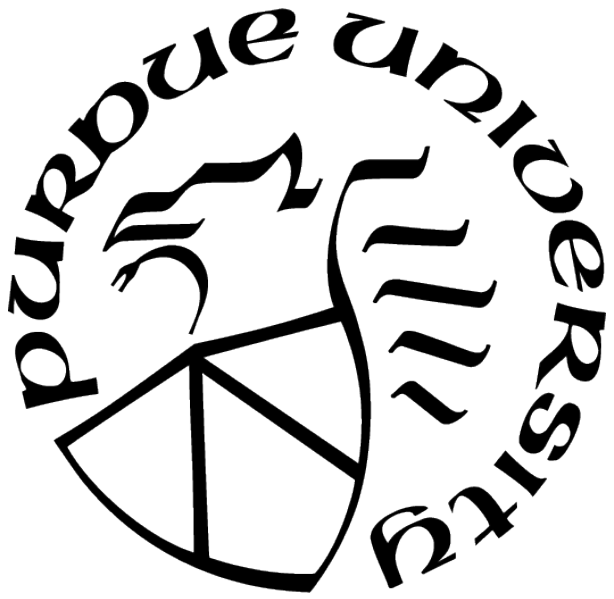

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ABSTRACT

Power semiconductor devices play an important role in many areas, including household appliances, electric vehicles, high speed trains, electric power stations, and renewable energy conversion. In the modern era, silicon based devices have dominated the semiconductor market, including power electronics, because of their low cost and high performance. The applications of devices rated 600 V - 6.5 kV are still dominated by silicon devices, but they are nearly reaching fundamental material limits. New wide band gap materials such as silicon carbide (SiC) offer significant performance improvements due to superior material properties for such applications in and beyond this voltage range. 4H-SiC is a strong candidate among other wide band gap materials because of its high critical electric field, high thermal conductivity, compatibility with silicon processing techniques, and the availability of high quality conductive substrates.

Vertical DMOSFETs and insulated gate bipolar transistors (IGBT) are key devices for high voltage applications. High blocking voltages require thick drift regions with very light doping, leading to specific on-resistance ($R_{ON,SP}$) that increases with the square of blocking voltage (V_{BR}). In theory, superjunction drift regions could provide a solution because of a linear dependence of $R_{ON,SP}$ on V_{BR} when charge balance between the pillars is achieved through extremely tight process control. In this thesis, we have concluded that superjunction devices inevitably have at least some level of charge imbalance which leads to a quadratic relationship between V_{BR} and $R_{ON,SP}$. We then proposed an optimization methodology to achieve improved performance in the presence of this inevitable imbalance.

On the other hand, an IGBT combines the benefits of a conductivity modulated drift region for significantly reduced specific on-resistance with the voltage controlled input of a MOSFET. Silicon carbide n-channel IGBTs would have lower conduction losses than equivalent DMOSFETs beyond 6.5 kV, but traditionally have not been feasible below 15 kV. This is due to the fact that the $n+$ substrate must be removed to access the $p+$ collector of the IGBT, and devices below 15 kV have drift layers too thin to be mechanically self-supporting.

In this thesis, we have demonstrated the world's first functional 10 kV class n-IGBT with a waffle substrate through simulation, process development, fabrication and characterization.

The waffle substrate would provide the required mechanical support for this class of devices. The fabricated IGBT has exhibited a differential $R_{ON,SP}$ of 160 mΩ.cm^2, less than half of what would be expected without conductivity modulation. An extensive fabrication process development for integrating a waffle substrate into an active IGBT structure is described in this thesis. This process enables an entirely new class of moderate voltage SiC IGBTs, opening up new applications for SiC power devices.

1. INTRODUCTION

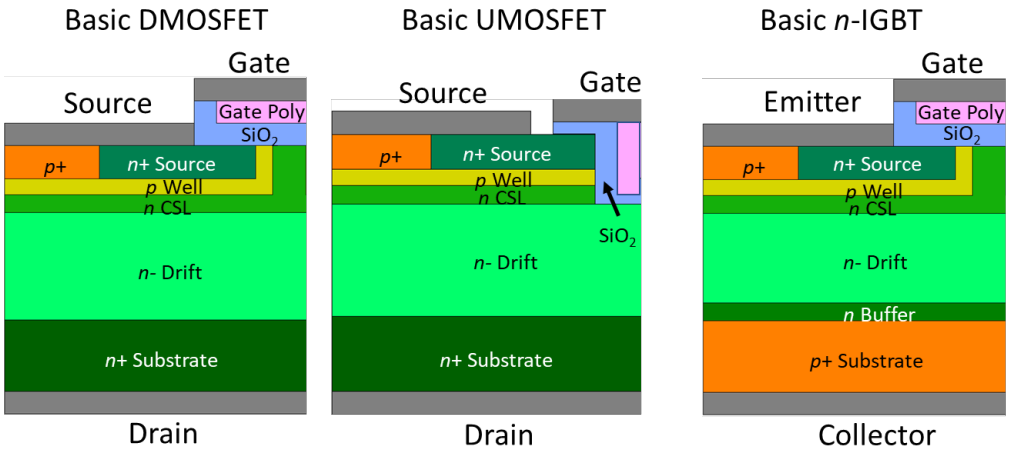
Invention and progress on semiconductor devices have changed the world dramatically over the last fifty years. Continuous progress on micro- and nano-scale fabrication has had an enormous positive impact on the industrial revolution, leading to modernization of all aspects of our daily life. Silicon-based electronic devices have dominated the field because of their low cost and high performance. The devices are operated in a wide range of voltages from very low to ultra high. The high voltage applications include household appliances, electric vehicles, high speed trains, electric power stations, and renewable energy conversion. The devices used for these applications are known as power semiconductor devices. Current research in power devices is extensive throughout the world.

1.1 Power Semiconductor Devices and Materials

Applications in power electronics require a device which has a low on-state resistance and a high off-state blocking voltage (V_{BR}). The on-state resistance is often multiplied with the area of the device, which is known as the specific on-resistance ($R_{ON,SP}$). The opposing demands of the on- and off-state modes leads us to define a performance metric, or figure of merit $FOM = V_{BR}^2/R_{ON,SP}$ [1]. When switching performance is involved then a figure of merit $FOM = R_{ON,SP}.Q_{GD,SP}$ is also commonly used where $Q_{GD,SP}$ represents the switching gate charge [2]. The general design goal of a power device is to maximize the FOM. The most popular devices in this area are metal-oxide-semiconductor field effect transistors (MOSFETs) [3], and insulated gate bipolar transistors (IGBTs) [4]. The power MOSFET incorporates the basic MOSFET structure on a thick, lightly doped drift layer and a heavily doped (same type) substrate, where the substrate acts as the drain.

The two styles of power MOSFETs are shown in Figure 1.1(a), and are knwon as the vertical planar DMOSFET and vertical trench UMOSFET. The name DMOSFET is derived from silicon devices, where source and base regions are both formed by diffusion of doping species, and hence called double diffused MOSFET (DMOSFET). The name of the UMOSFET is derived from the U-shape of the gate although it is also well known as a trench MOSFET. Figure 1.1(b) shows an insulated gate bipolar transistor (IGBT), where the sub-

strate of a DMOSFET or UMOSFET is replaced by opposite polarity of doping. This mode of operation was first experimentally demonstrated by Scharf et. *al*. [5] in a lateral device and by Baliga [6] in a vertical device.



(a) (b)

Figure 1.1. (a) Vertical Power MOSFETs (b) IGBT with DMOS structure.

Silicon (Si) is the leading material for power devices because of its low cost and high performance. Silicon power devices like IGBTs dominate the market of 600 V - 6.5 kV but they are approaching their fundamental limits[7] while 4H-SiC is a strong candidate among other wide band gap materials because of its high critical electric field, high thermal conductivity, compatibility with silicon processing techniques, and the availability of high quality conductive substrates. Another wide band gap material, gallium nitride (GaN), also possesses similar characteristics to SiC [1]. At present, material growth and device fabrication technologies are more advanced for SiC and also more cost effective because existing Si fabrication facilities can be adapted for SiC.

1.2 Properties of Silicon Carbide

Silicon carbide is a compound material with a stoichiometry of 50% silicon (Si) and 50% carbon (C). From a crystallographic view, SiC is the best known example of polytypism [8] which is the property of forming various crystal structures without changing the chemical

composition. These different crystal structures are known as polytypes. Interestingly, there are more than 200 polytypes in SiC [1], falling within the cubic (C), hexagonal (H), and rhombohedral (R) crystal systems. The most popular crystal structures for electronic devices are 3C-SiC, 4H-SiC, and 6H-SiC, where the nomenclature is based on the crystal structure and stacking sequence. It is reported that at high temperature, above $1900 \sim 2000$°C, 3C-SiC transforms into a hexagonal structure [9]. Therefore, 4H-SiC and 6H-SiC are very popular and extensively investigated in terms of material growth, device fabrication and performance [10]–[12]. The electron and hole mobilities in 4H-SiC are almost double compared to 6H-SiC [1]. Moreover, the availability of single crystalline 4H-SiC wafers with large diameter and the superior performance of the devices in comparison with 3C-SiC and 6H-SiC make it preferable to the academic and industrial researchers. Therefore, our discussion and analysis will be based on 4H-SiC in the subsequent sections.

1.2.1 Wide band gap and high critical electric field

All the SiC polytypes have an indirect band structure. It is reported that the band gap of 4H-SiC is 3.26 eV at room temperature [1]. The band gap (E_g) decreases with the increase of temperature. An empirical model given by the following equation [13] is useful to perform numerical simulation at high temperature.

$$E_g(T) = E_{g0} - \frac{\alpha T^2}{T + \beta} \tag{1.1}$$

where E_{g0} is the band gap at 0 K, T the absolute temperature and the fitting parameters, $\alpha = 8.2 \times 10^{-4}\,\mathrm{eVK}^{-1}$ and $\beta = 1.8 \times 10^{3}\,\mathrm{K}$. One can easily calculate the intrinsic carrier density (n_i) using the effective density of states for the conduction ($N_C = 1.8 \times 10^{19}\,\mathrm{cm}^{-3}$) and valence bands ($N_V = 2.1 \times 10^{19}\,\mathrm{cm}^{-3}$). At $T = 300$ K, it is found that $n_\mathrm{i} = 5 \times 10^{-9}\,\mathrm{cm}^{-3}$. The intrinsic carrier density is extremely low, even at elevated temperatures. This property makes 4H-SiC-based devices superior to Si for high temperature operation, for instance by having very low junction leakage currents. In a power semiconductor device, a study of the material property that is responsible for breakdown is very important. Avalanche breakdown is dominant in such devices, rather than Zener breakdown, which requires high doping in

both sides of the junction to have a thin depletion width and very strong band bending to bring the valence band into alignment with the conduction band over a sufficiently short distance. Avalanche breakdown occurs due to impact ionization of carriers. In a space charge region, electrons and holes are accelerated by the electric field, since they are charged particles, and gain kinetic energy. The particles occasionally undergo a collision with the lattice and fall into a lower energy state. If the kinetic energy of a particle is sufficient, then the collision can break a covalent bond and generate an electron-hole pair. This process, called impact ionization, is repeated and the generated electron-hole pairs are multiplied, eventually leading to breakdown.

The number of impact ionization events initiated by an electron (or hole) per unit length traveled is called an impact ionization coefficient. There are many articles on the impact ionization coefficients of electrons (α_n) and holes (α_p) among which a most recent analysis is presented in [14]. The impact ionization coefficients are expressed as a function of electric field (E) and the expression is known as the Chynoweth equation [15] which is given below

$$\alpha_{\mathrm{i}} = a_{\mathrm{i}}\, exp\,(-b_{\mathrm{i}}/E) \quad \text{where i} = n \text{ or } p \tag{1.2}$$

The electric field at which breakdown occurs is called the critical electric field (E_c), which is an important material property. The ionization integral is given by the following equation, and breakdown occurs when it reaches unity.

$$1 = \int_0^t \alpha_p \exp\left(-\int_0^x (\alpha_p - \alpha_n)\, dx\right) dx \tag{1.3}$$

The integral is performed in the space charge region extending from $x = 0$ to $x = t$. An estimation of the ideal blocking voltage for an one sided $p+/n$ junction with a doping N_D in the lightly doped region can be found by the following relation, available in any standard power semiconductor device book.

$$V_{BR} = \frac{\varepsilon_s E_c^2}{2qN_D} \tag{1.4}$$

where ε_s is the dielectric constant of the material. The relative dielectric constant of 4H-SiC is 10.32[1]. The critical electric field also depends on the doping concentration in the material, and doping dependent empirical expressions for 4H-SiC and Si are given below as found in [16] and [17]

$$\begin{aligned} E_{c,SiC} &= \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log_{10}\left(N_D/10^{16}\right)} \quad \text{V/cm} \\ E_{c,Si} &= \frac{4 \times 10^5}{1 - \frac{1}{3}\log_{10}\left(N_D/10^{16}\right)} \quad \text{V/cm} \end{aligned} \tag{1.5}$$

A plot of Eqn. (1.5) is shown in Figure 1.2, and shows that the critical electric field in 4H-SiC is significantly higher ($4 \sim 7$x) than that of Si.Therefore, Eqn. (1.4) shows

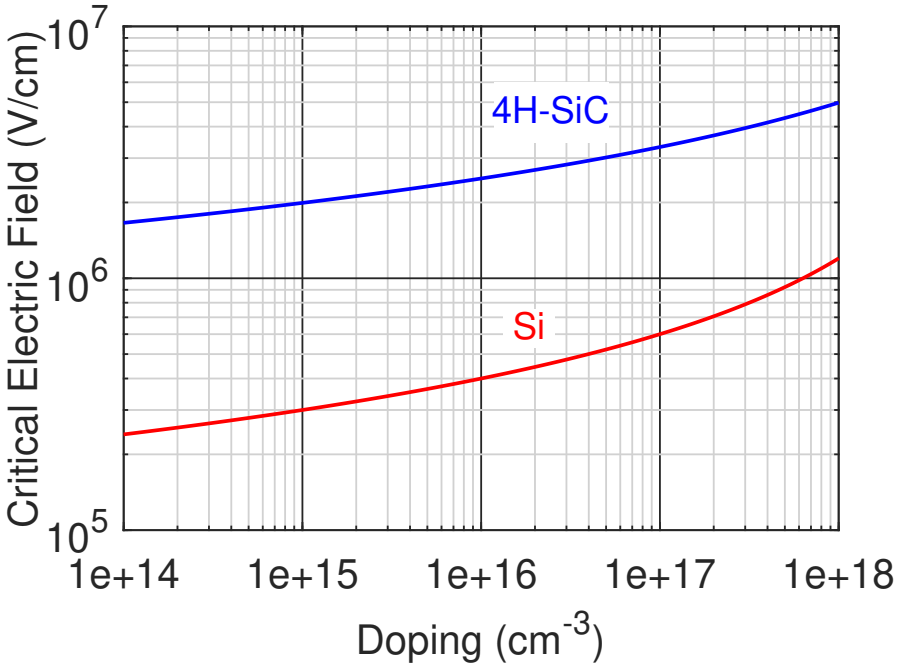


Figure 1.2. Critical electric fields in 4H-SiC and Si as a function of doping.

that at a given doping level, the achievable blocking voltage in 4H-SiC is ~ 50 times higher than that of Si. This result makes 4H-SiC an excellent material to be used in power devices.

1.2.2 High thermal conductivity

The high thermal conductivity of 4H-SiC gives its corresponding devices an added advantage for high temperature and high power operation. In general, heat sinks are used in power devices because they experience very high junction temperatures. Highly pure SiC exhibits a thermal conductivity of 3.3 $\mathrm{W\,cm^{-1}\,K^{-1}}$ at room temperature [1] while it is 1.5 $\mathrm{W\,cm^{-1}\,K^{-1}}$ for Si [17]. In general, SiC-based devices are capable of carrying significantly higher current densities than that of Si devices with same voltage rating. Therefore, high thermal conductivity helps ensure that SiC-devices maintain a reasonable junction temperature. It is reported in [18] that thermal conductivity depends on doping and temperature but is unaffected by polytype.

1.3 Prospects and Challenges of SiC MOS-Devices

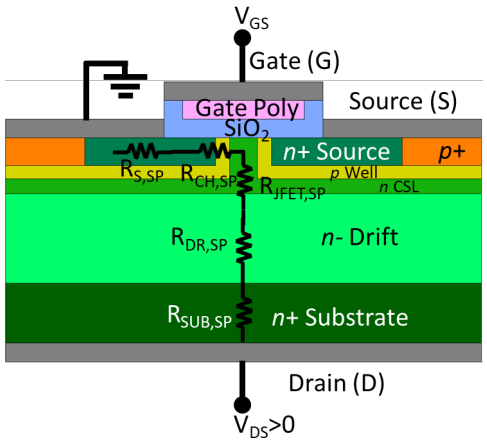
Silicon carbide can be thermally oxidized like Si to form a native silicon dioxide (SiO_2). This is the only wide band gap semiconductor material whose native oxide is SiO_2. Therefore, all manner of MOS devices are possible in SiC. In SiC, the DMOSFET was demonstrated for the first time by implantation instead of diffusion as reported in [19]. The term DMOSFET is generally used, whether the doping is performed by diffusion or implantation. The first SiC-based UMOSFET is reported in [20]. The following subsections will describe the two most common power devices, the DMOSFET and the IGBT.

1.3.1 DMOSFET

A typical vertical DMOSFET structure is shown in Figure 1.3(a), along with the five major components of on-resistance. These resistances are from the source, channel, JFET, drift, and substrate regions. All the resistances, except that of the drift region, are invariant with blocking voltage because the achievable V_{BR} depends only on the drift layer thickness

and doping. The specific resistance of an optimized drift region follows a quadratic relation [21] with the blocking voltage as given below,

$$R_{DR,SP} = \left(\frac{3}{2}\right)^3 \frac{V_{BR}^2}{\mu_N \varepsilon_s E_c^3} \tag{1.6}$$



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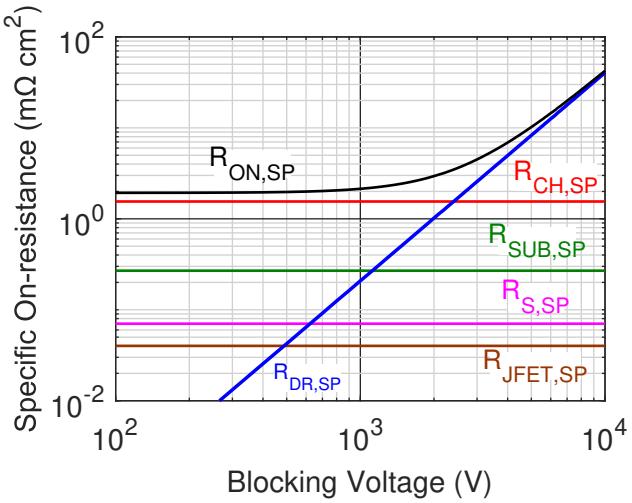


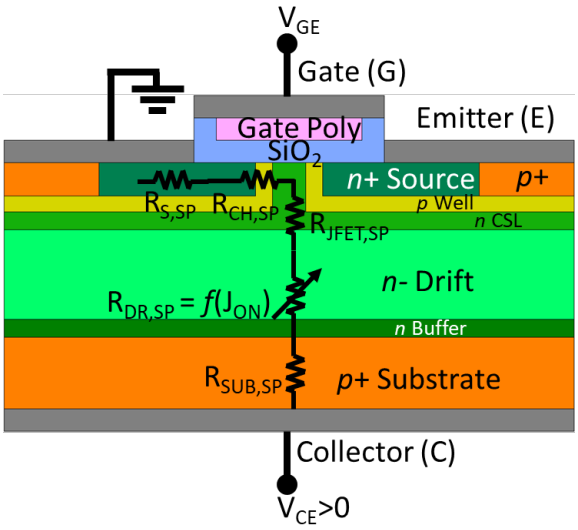
(b)

Figure 1.3. (a) 2D cross section of a standard n-channel DMOSFET with its various resistance components (b) Specific on-resistance of the standard DMOSFET as a function of blocking voltage at 27 °C. Contributions from all the components are shown.

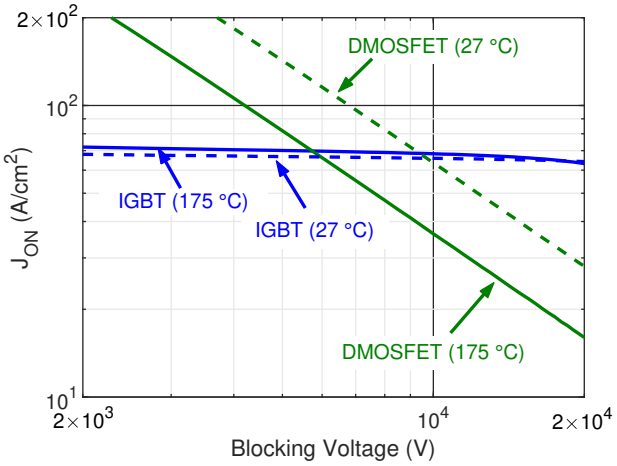
It is obvious from the $R_{ON,SP}$ plot in Figure 1.3(b) that the drift region resistance is the dominant component for a device of $V_{BR} > 2$ kV. Therefore, this is the major challenge for high voltage devices. The drift region resistance can be reduced significantly by employing a superjunction structure as will be described in Chapter 2. Nevertheless, the specific on-resistance of a DMOSFET becomes worse at very high temperature because carrier mobility goes down significantly due to increased phonon scattering.

1.3.2 Insulated gate bipolar transistor (IGBT)

The typical structure of an n-channel IGBT is shown in Figure 1.4(a) with its various resistance components. The important difference compared with the DMOSFET is that the drift resistance is reduced by conductivity modulation, and is a function of the on-state current density. All other components remain same except the substrate, which has the opposite polarity of the drift layer. However, the on-state performance of an IGBT is limited by the current density at a given maximum power dissipation density. A comparison of the DC current density of a DMOSFET and an IGBT at a power density 200 W/cm^2 is shown in Figure 1.4(b). The performance of the IGBT remains almost invariant with temperature, and is better than an equivalent DMOSFET for $V_{BR} > 6$ kV at 175°C. At high frequency the bipolar IGBT suffers from higher switching losses than the unipolar MOSFET device, but in this project we are focused primarily on low frequency applications of the IGBT.



(a)



(b)

Figure 1.4. (a) 2D cross section of a standard n-channel IGBT with its various resistance components (b) On-state current density comparison of n-channel DMOSFET and n-channel IGBT at 27°C and 175°C at 200 W/cm^2 power density.

1.4 Outline of the Dissertation

Chapter two discusses the limitations of superjunction drift regions in 4H-SiC power MOSFETs by analyzing the charge imbalance problem and fabrication challenges. An alternate solution for the high resistance of the drift region is proposed in chapter three, which

describes a 12.5 kV waffle-substrate-based n-channel IGBT. The physics and expected on- and off-state performance is also discussed in detail in this chapter. A detail discussion of the mask design and fabrication steps are illustrated in chapter four. Finally, the performance of the fabricated devices through electrical characterization is explained in chapter five. A brief summary and future work of this research is given in chapter six.

2. THE SUPERJUNCTION DMOSFET

The drift region of a high voltage vertical DMOSFET is the limiting part because of its large specific on-resistance which is proportional to the square of the breakdown voltage. The superjunction structure, proposed by Fujihira[21] in 1997, is a promising solution to this problem. In this structure, the conventional drift region (n type or p type) is replaced by an alternately stacked n and p pillars as shown in Figure 2.1. A two dimensional cross section of the superjunction drift layer is shown in Figure 2.1(b) with a $p+$ layer on the top and $n+$ layer on the bottom for 2D simulation. The widths and dopings in the n and p pillars are d_n, d_p, N_D, and N_A respectively. The axis convention is also indicated in the figure.

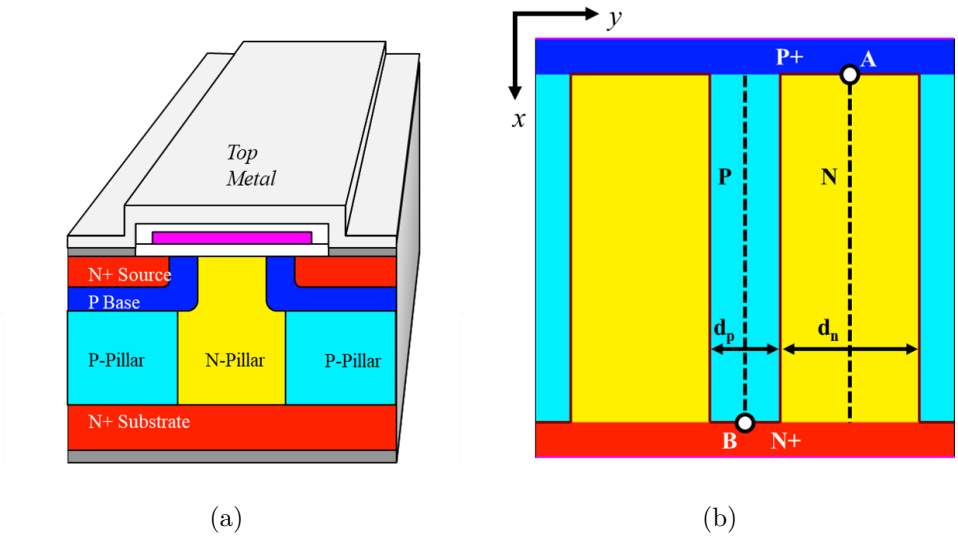
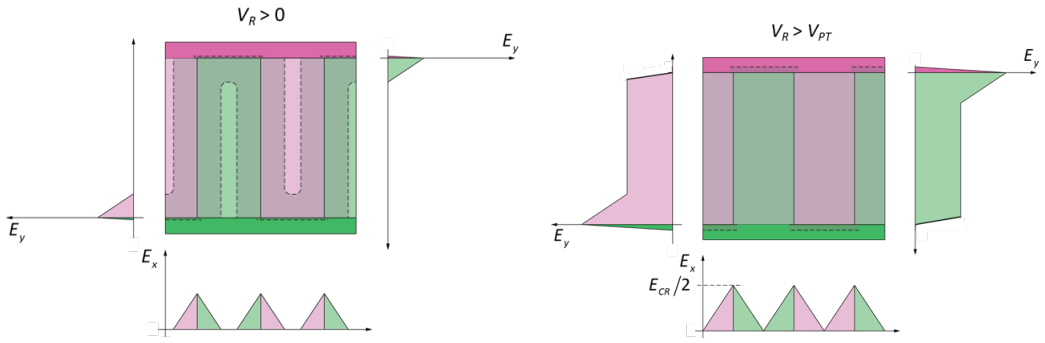


Figure 2.1. (a) Example of a DMOSFET with a superjunction drift region (b) Two dimensional cross section of a typical superjunction structure.

All the p-n junctions of a superjunction start depleting as a reverse voltage V_R is applied across the cross section. A triangular electric field profile appears across the p-n junctions as shown in Figure 2.2(a). As the applied reverse voltage increases, the junctions deplete more, and the electric field continues to increase in a triangular fashion. The pillars are completely depleted in the lateral direction at voltage $V_R = V_{PT}$, and the drift region effectively becomes an intrinsic region. Therefore, any additional applied reverse voltage beyond V_{PT} causes a

vertical electric field E_x profile along the center of the n or p pillar as shown in Figure 2.2(b). The total electric field E must be equal to E_x because $E_y = 0$ along this path.



(a) (b)

Figure 2.2. Depletion region and electric field profile in the lateral and vertical directions (pillar center) when (a) $V_R > 0$ and (b) $V_R > V_{PT}$.

2.1 2D Analytical Superjunction Model

The superjunction is ideal when the doses of the pillars are equal ($d_n N_D = d_p N_A$) to maintain the charge balance between them. A non-ideal superjunction has charge imbalance between the pillars when the doses are not equal ($d_n N_D \neq d_p N_A$). This phenomenon occurs because of geometrical and doping variations which occur during the fabrication process. The degree of charge imbalance is defined as,

$$CI = \begin{cases} \frac{d_p N_A - d_n N_D}{d_n N_D} \times 100\% & \text{for } d_n N_D > d_p N_A \\ \\ \frac{d_p N_A - d_n N_D}{d_p N_A} \times 100\% & \text{for } d_n N_D < d_p N_A \end{cases} \tag{2.1}$$

Two dimensional analytical models have been proposed by many researchers to analyze superjunction structures. However, we adopted the model proposed by Napoli, e*t al.*, [22],

[23] which agrees well with TCAD simulations. The electric field profile along the center of the pillars is calculated by

$$E_x(x) = \pm\frac{V_u}{t}\left(1-\frac{2x}{t}\right) + \frac{V_R}{t} + \pm\frac{V_{D,A}}{t}\left(1-\frac{2x}{t}\right) + \pm\frac{4(V_A+V_D)}{t} \\ \sum_{n=1}^{\infty}\frac{\left[(-1)^n-1\right]\cos\left(n\pi x/t\right)\sinh\left[n\pi d_{p,n}/\left(2t\right)\right]}{\left(n\pi\right)^2\sinh\left[n\pi\left(d_p+d_n\right)/\left(2t\right)\right]} \tag{2.2}$$

where t is the drift layer thickness, $V_u = \left(qN/2\varepsilon_s\right)t^2$, and $V_{D,A} = \left(qN_{d,a}/2\varepsilon_s\right)t^2$. The positive sign in Eqn. (2.2) and $V_{D,A} = V_D$ are used for the n pillar, and the negative sign and $V_{D,A} = V_A$ are used for the p pillar. The three effective dopings used in Eqn. (2.2) are defined as,

$$\begin{aligned} N &= \left|d_nN_D - d_pN_A\right|/\left(d_n+d_p\right) \\ N_a &= d_n\left(N_A+N_D\right)/\left(d_n+d_p\right) \\ N_d &= d_p\left(N_A+N_D\right)/\left(d_n+d_p\right) \end{aligned} \tag{2.3}$$

The ionization integral given in Eqn. (1.3) is used to calculate the breakdown voltage V_{BR} where the hole and electron ionization coefficients α_p and α_n are used from the model given by Hatakeyama e*t al*. [24], and the electric field profile given by Eqn. (2.2). The specific on-resistance is then calculated using

$$R_{ON,SP} = \frac{t}{q\mu_nN_D}\times\frac{\left(d_p+d_n\right)}{d_n-2w_{dep}} \tag{2.4}$$

where w_{dep} is the zero-bias depletion width in the n pillar. Without loss of generality, we consider $d_n = d_p = d$ throughout the discussion where $N_D = N_A$ and $N_D \neq N_A$ for the balanced and imbalanced superjunctions, respectively.

2.2 Ideal Superjunctions

Fujihira provided an 1D analytical model to calculate the electric field and the relation between the applied reverse bias voltage and specific on-resistance for an ideal superjunction. He showed that the minimum $R_{ON,SP}$ is achieved when the maximum lateral electric field (E_y) is equal to the half of the critical electric field (E_c). The most interesting result of

a superjunction structure is observed for a vertical device where the $R_{ON,SP}$ and optimum doping $N_{D,opt} = N_{A,opt} = N_{opt}$ are given by

$$R_{ON,SP} = 4d \times \frac{V_{BR}}{\mu_n \varepsilon_s E_c^2} \tag{2.5}$$

and

$$N_{opt} = \varepsilon_s E_c / (qd) \tag{2.6}$$

The linear relationship between the specific on-resistance and breakdown voltage is the most attractive feature of a superjunction. However, in this 1D analysis the critical electric field E_c is considered as a constant, which is not the case in reality. The doping dependent empirical expression given by Eqn. (1.5) is used in this calculation.

For a given pillar width d the optimum doping can be found by solving Eqns. (2.6) and (1.5) self-consistently. For example, optimum doping is found as $9.40 \times 10^{16}\,\mathrm{cm}^{-3}$ for $d = 2\,\mu\mathrm{m}$. However, 2D analytical model given by Eqn. (2.2) is more accurate because it considers the two dimensional geometrical effect on electric field. In order to find the optimum design, it is required to solve Eqns. (2.2)-(2.4) iteratively. Using this method optimum pillar dopings are found as 2.94×10^{17}, 1.29×10^{17}, 6.31×10^{16} and $3.98 \times 10^{16}\,\mathrm{cm}^{-3}$ for pillar widths of 1, 2, 4 and 6 μm respectively. The performance of these SJ structures are compared with a conventional drift regions in a logarithmic plot of $R_{ON,SP}$ as a function of V_{BR} shown in Figure 2.3. The drift layer thickness increases from left to right in each lines. An ideal superjunction is capable of giving significant improvement over conventional device as the pillar width is reduced. Any breakdown voltage is achievable as long as the required aspect ratio (t/d) is supported by the fabrication technology. The logarithmic slope of the SJ performance lines is unity, which agrees with the 1D model of Fujihira.

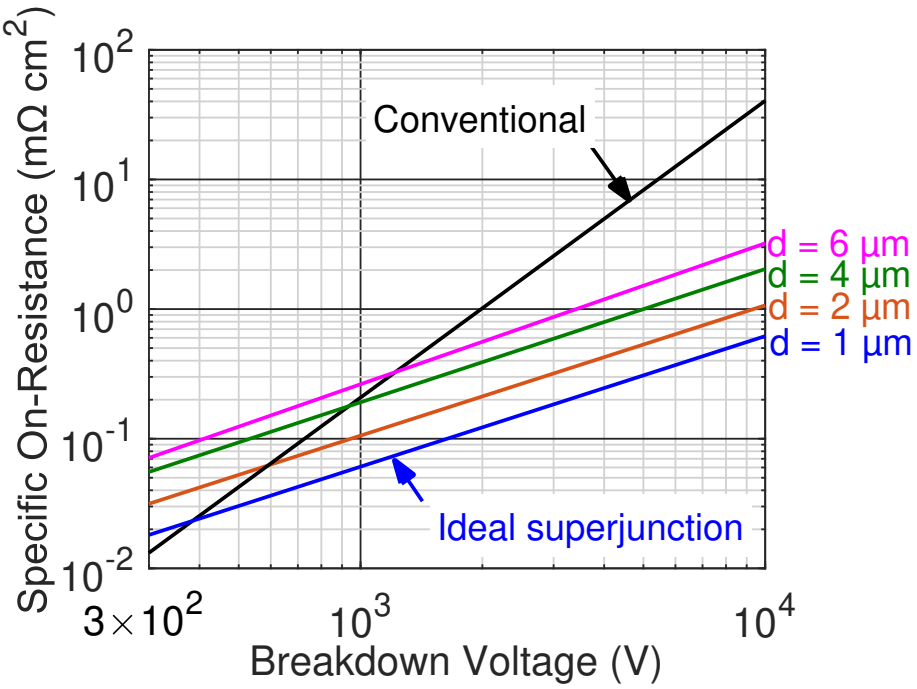


Figure 2.3. Comparison of specific on-resistance of balanced SJ drift regions and a conventional drift region as a function of breakdown voltage. Parameters of the SJ are: $d_p = d_n = d = 1$, 2, 4, and 6 µm, $N_D = N_A = 2.94\times10^{17}, 1.29\times10^{17}, 6.31\times10^{16}$, and 3.98×10^{16} cm^{-3}.

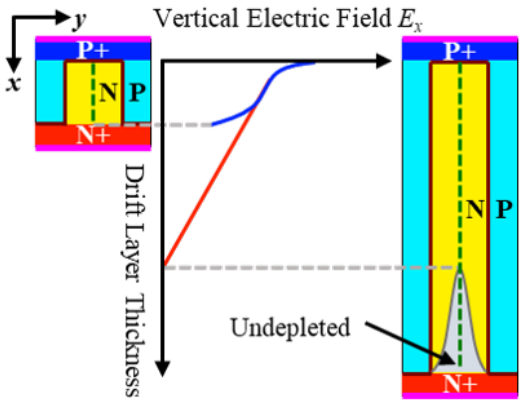
2.3 Non-Ideal Superjunction due to Charge Imbalance

The charge imbalance between the n and p pillars is a great challenge for superjunction devices, and some degree of imbalance will inevitably arise during fabrication of practical devices. The effect of charge imbalance and a procedure for optimization in its presence is discussed in the following subsections.

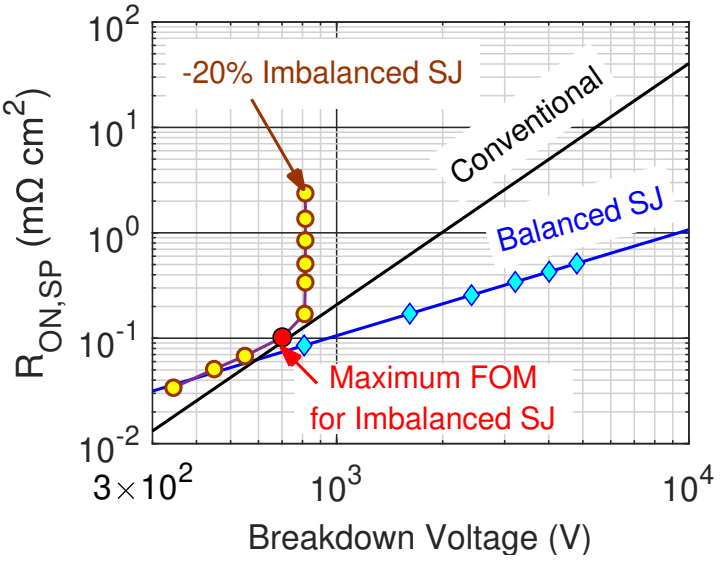
2.3.1 Performance deviation

A practical superjunction device will suffer from charge imbalance. The reason for performance deviations in the presence of charge imbalance is explained with the help of a schematic diagram of the electric field profile shown in Figure 2.4(a). In this figure, the doping in the n pillar is higher than that of the p pillar. Two SJ structures with different

drift layer thicknesses are also shown. The middle part of the electric field profile along the center of the n pillar has a non zero slope, in contrast with a



(a)



(b)

Figure 2.4. (a) Electric field profile in the center of the highly doped pillar for low and high drift layer thicknesses, (b) Performance deviation of an imbalanced superjunction compared with a balanced superjunction for $d = 2\,\mu\text{m}$, $N_D = 1.29 \times 10^{17}\,\text{cm}^{-3}$ and $CI = -20\%$.

balanced SJ. An imbalanced superjunction is a superposition of a balanced SJ with pillar doping $N_{SJ} = |N_D + N_A|/2$ and a differential drift layer with doping of $N_{diff} = |N_D - N_A|/2$.

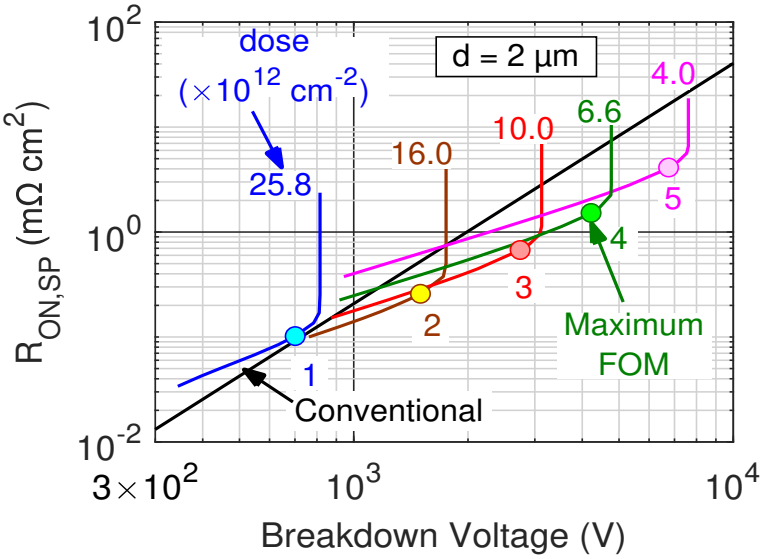
The slope of the electric field in the balanced component is zero and the slope of the electric field in the unbalanced component is equal to qN_{diff}/ε_s. Nevertheless, the structure with low drift layer thickness is depleted completely, but as the thickness is increased further a non-punch-through (NPT) phenomenon appears. Therefore, the V_{BR} saturates beyond a certain drift layer thickness in the presence of charge imbalance.

In order to understand the impact of charge imbalance, let us consider a superjunction optimized assuming charge balance, having a pillar width $2\,\mu$m, $N_D = 1.29 \times 10^{17}\,\mathrm{cm}^{-3}$ but experiencing an imbalance of -20% i.e. $N_A = 1.03 \times 10^{17}\,\mathrm{cm}^{-3}$. In the presence of charge imbalance the $R_{ON,SP} - V_{BR}$ curve starts deviating dramatically from that of a balanced device as shown in Figure 2.4(b). The imbalanced device reaches a point beyond which increasing the drift region thickness does not increase V_{BR} because the depletion width is not further increased, but $R_{ON,SP}$ does increase. This is the reason the imbalanced curve turns vertical in Fig. 2.4(b). The maximum FOM for the imbalanced SJ is found just before it enters the NPT region, while it is ever increasing for a balanced SJ, provided the available fabrication technology supports the required aspect ratio t/d.

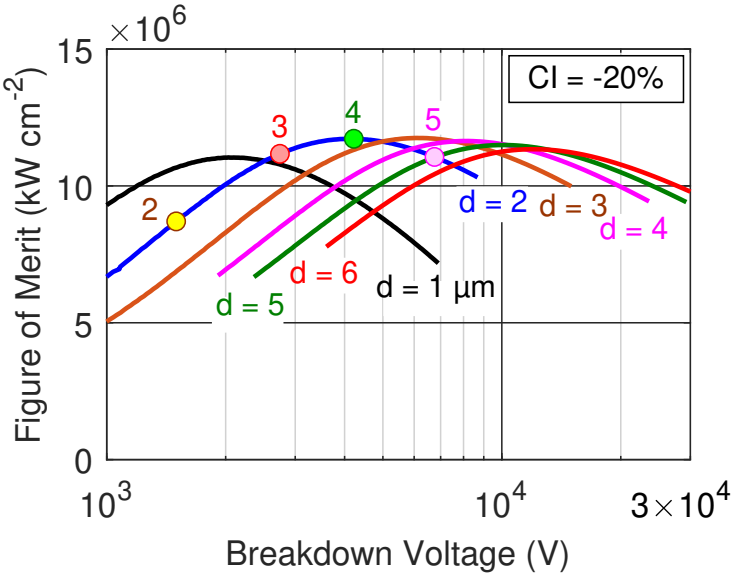
2.3.2 Optimization of imbalanced superjunction

From the result of previous section it is obvious that an anticipated level of charge imbalance must be considered to optimize a SJ structure. A numerical optimization method is feasible with the help of a 2D analytical model. It is observed that for a given d and degree of CI, varying t and N_D can produce a series of curves shown in Figure 2.5(a). In this case, d and CI are chosen as $2\,\mu$m and -20%. As the dose is reduced the FOM arrives at a peak and decreases again. The maximum FOM is achieved at a dose of $6.6 \times 10^{12}\,\mathrm{cm}^{-2}$ indicated by point 4. The plot is converted to a FOM as a function of V_{BR} as shown in Figure 2.5(b) labeled with $d = 2\,\mu$m. The similar approach is applied to the structures with $d = 1,\ 3,\ 4,\ 5,$ and $6\,\mu$m and plotted in the same figure. The tangential envelope passing through the peaks of all these curves represents the locus of optimum design points in the presence of -20% charge imbalance. The resulting optimum locus is converted to a plot of

$R_{ON,SP}$ as a function of breakdown voltage shown in Figure 2.6. The figure also contains the results from the SJ devices with -10% and -5% imbalance.



(a)



(b)

Figure 2.5. (a) Finding the optimum dose for a -20% imbalanced SJ with $d_p = d_n = 2\,\mu\text{m}$ (b) Optimum FOM as a function of breakdown voltage for $CI = -20\%$.

The $R_{ON,SP} - V_{BR}$ plot is quite interesting because it follows nearly a quadratic relation, similar to a conventional device instead of linear relationship expected from a balanced SJ. Nevertheless, the SJ can still provide 5x -14x improvement if the imbalanced is kept below -20%.

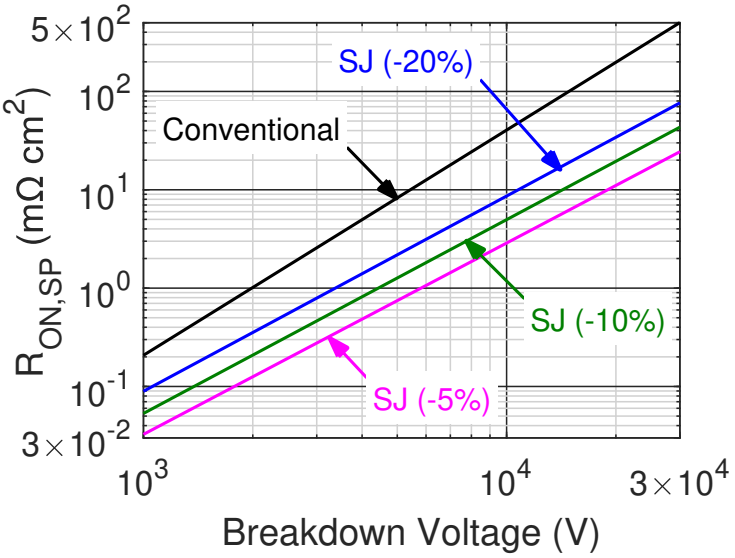


Figure 2.6. Optimum performance limits of 4H-SiC SJ drift regions with various levels of CI compared to conventional drift regions.

A simple alternative analytical model can be derived to determine V_{BR} and the t_{opt} for given pillar characteristics, such as doping and pillar width[25]. This method saves time by avoiding numerical simulations and iterative methods such as were described above. To illustrate the methodology, consider the following example. The electric field profile and the $R_{ON,SP}$ of a superjunction with pillar widths $d_n = d_p = = d = 2$ µm, dopings $N_D = 3.31{\times}10^{16}$ cm^{-3}, $N_A = 2.65{\times}10^{16}$ cm^{-3} can be calculated using the Eqn. 2.2-2.4 and 1.3. The electric field profiles for drift layer thicknesses of $t = 5$, 20, 30, and 50 µm are shown in Fig. 2.7. The electric field profile has a slope of qN_{diff}/ε_s where $N_{diff} = |N_D - N_A|/2$. Considering the electric field profile for $t = 30$ µm can be approximated by the dashed line shown in the figure. An effective critical electric field $E_{c,eff}$ can be defined by extrapolating the dashed line to the y intercept at $x = 0$. The area under the approximate electric field

curve, which represents the blocking voltage, is essentially equal to that of the the original curve. The approximated dashed line corresponds to a trapezoid with an area given by.

$$V_{BR} = E_{c,eff}t - \frac{1}{2}at^2, \text{where a} = qN_{diff}/\varepsilon_s \tag{2.7}$$

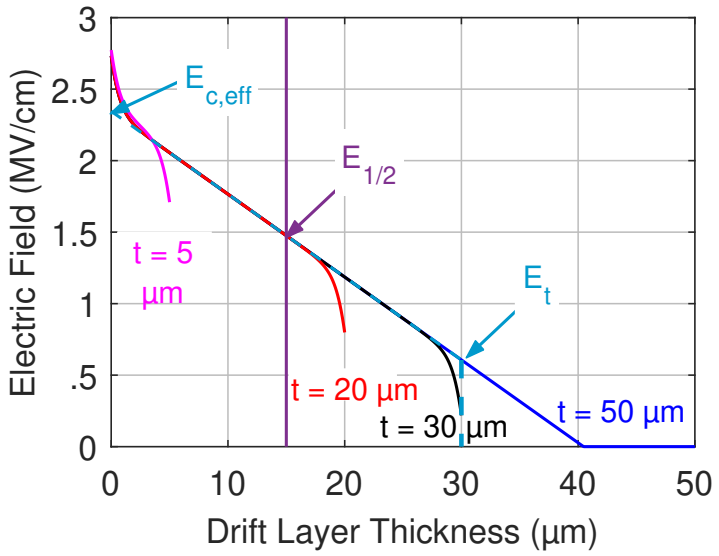


Figure 2.7. Electric field profile along the center-line of the n pillar in a 20% imbalanced SJ with drift layer thicknesses of 5, 20, 30, and 50μm, $d_n = d_p = 2$ μm, $N_D = 3.31\times10^{16}$ cm^3, and $N_A = 2.65\times10^{16}$ cm^3

Now using the Eqns. 2.4 and 2.7 the figure-of-merit FOM can be written as,

$$FOM = \frac{q\mu_n N_D}{8} \times \frac{d - 2w_{dep}}{d}(4E_{c,eff}^2 - 4E_{c,eff}at^2 + a^2t^3) \tag{2.8}$$

After taking the derivative with respect to the drift layer thickness t we solved the optimzation problem and ends up with optimum thickness given by

$$t_{opt} = \frac{2}{3}\frac{\varepsilon_s E_{c,eff}}{qN_{diff}} \tag{2.9}$$

Therefore, combining Eqns. 2.7 and 2.9 yield the V_{BR} as

$$V_{BR} = \frac{qN_{diff}}{\varepsilon_s}t_{opt}^2 \tag{2.10}$$

A step by step procedure to find the t_{opt} leading to the V_{BR} corresponding to an optimum FOM for a given level of imbalance, doping, pillar is described below.

1. Choose an arbitrary value of drift layer thickness $t >> d$, with an electric field at $t/2$ that is nonzero.

2. Find the electric field profile for the given parameters and the chosen t by solving Eqns. 2.2, 2.3 and 1.3 simultaneously.

3. Find the electric field $E_{1/2}$ at $x = t/2$ as shown in Fig. 2.7.

4. Find $E_{c,eff}$ at $x = 0$ by extrapolating the curve as described above.

5. Calculate $N_{diff} = |N_D - N_A|/2$ and t_{opt} by using Eqn. 2.9.

6. Finally, calculate the V_{BR} using the Eqn. 2.10.

The resulting optimum design parameters (d, t, N_D) as a function of breakdown voltage are plotted in Fig. 2.8. The required drift layer thickness is the same for both -20% and -10% imbalanced SJs. For a given imbalance, the dose ($d \times N_D$) remains almost constant.

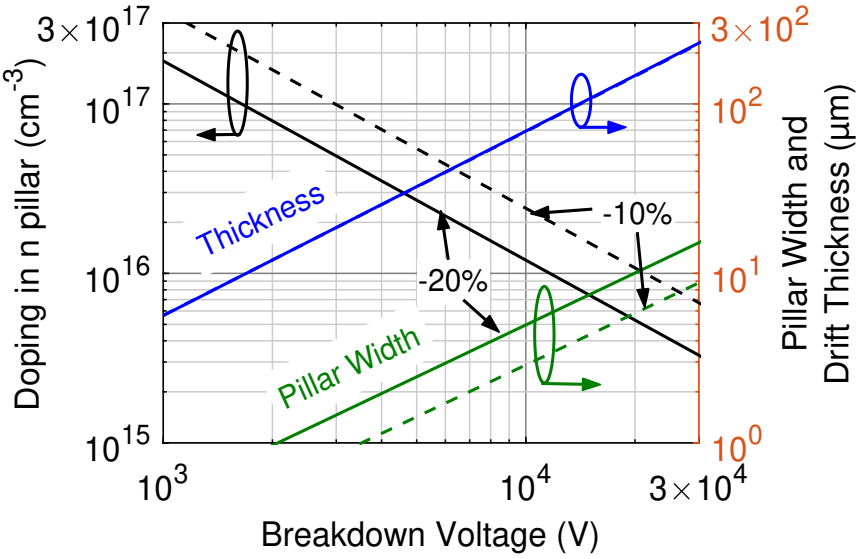


Figure 2.8. Optimum design parameters as a function of breakdown voltage for $CI = -10\%$ and -20%.

2.4 Fabrication Techniques and Challenges

Silicon based superjunctions have been commercially available for years, but maintaining charge balance remains a significant challenge. Commercial SJ devices in silicon carbide are even more challenging because of its high cost. There are several techniques used to create the SJ structure, but the two most attractive and efficient are (a) Multiple step high energy implant and epitaxial regrowth, and (b) Trench etch and refill by epitaxy. A more detailed discussion is given in the following subsections.

2.4.1 Multiple step implant-epi re-growth

The ion implantation technique is very popular for its high degree of dose control. The limiting factor is the highest energy required for a target junction depth. A typical fabrication setup for a two step implant and epi-regrowth technique is shown in Figure 2.9. The starting wafer has an n-type epi layer and a counter doping implant

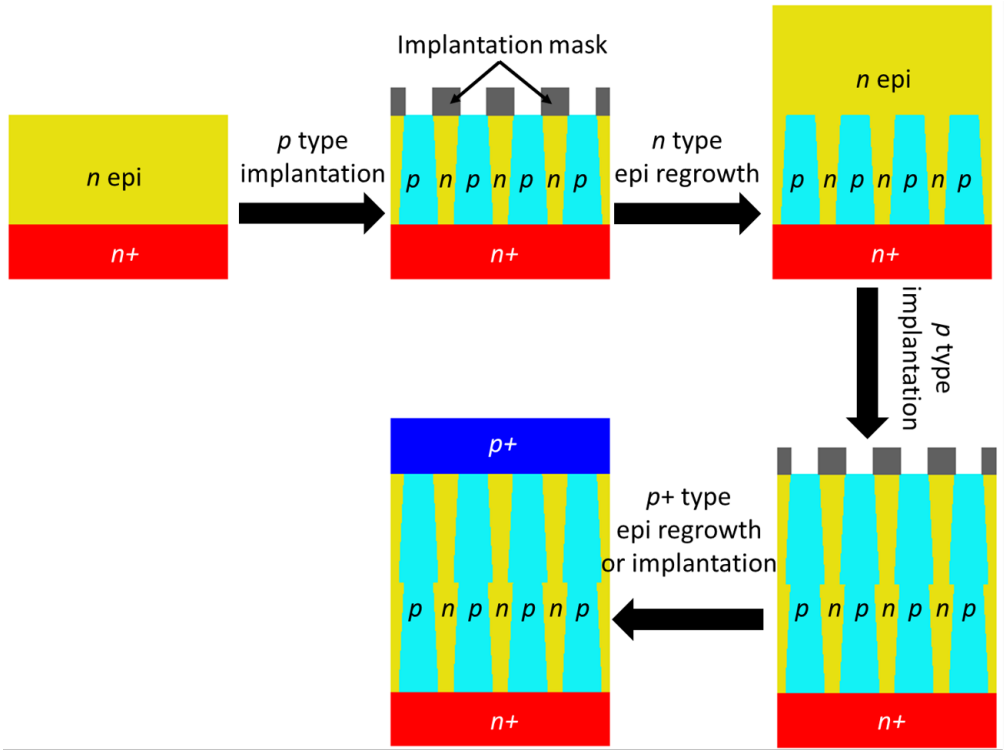


Figure 2.9. Typical multi-step (two step in this case) implant and epi-regrowth technique to fabricate a SJ p-n diode.

is applied to create p-type pillars. This requires an appropriate mask with a pattern dimension based on the designed pillar width d. The doping is also typically designed as a box profile, but the associated lateral straggle is one potential source of charge imbalance. In the next step, an n-type epitaxial layer is regrown, followed by the same patterned implantation schedule. The mask alignment in the subsequent steps may become a cause of charge imbalance. Repeated steps are followed depending on the target device. The number of implant-epi cycles required is a barrier to fabricate a reasonably rated device where drift region resistance is concerned. For example, a very high energy such as 5 MeV ion implantation can create a p-pillar of thickness 2.5 μm. So, even with a balanced design with pillar width 2 μm, pillar doping $N_A = N_D = 9.5{\times}10^{16}$ cm^{-3} a maximum blocking voltage of 500 V can be achieved in one fabrication cycle. Therefore, 8 cycles are required to fabricate a device of 4 kV which is very challenging and expensive.

2.4.2 Trench refill epi-growth

The trench refill epitaxy process is widely used in silicon based superjunction processing. The process is shown schematically in Figure 2.10. The processing starts with an n-type epi layer with the desired thickness and doping. An appropriate mask is used to etch trenches with the desired pillar width. The first challenge is to fabricate a very vertical sidewall during the etching, which is required to minimize the charge imbalance. The most challenging part for silicon carbide is to refill the trench with a p-type epitaxial layer. Sidewall epi growth suppression is required so that no voids are created in the process. Japanese researchers are now able to refill a trench by quasi-selective epitaxial growth process with sidewall epi growth suppression[26], but the doping control during the refill epitaxy remains a significant challenge. Moreover, this refill epitaxy is very slow (2 μm/hr for 25 μm trench with aspect ratio 10[26]) compared to a traditional epitaxy where hundreds of microns can be grown in an hour[27]. So, this is a very costly procedure if the target $V_{BR} \geq 4\,\text{kV}$ which requires more than 25 μm drift layer with an aspect ratio 13 or more as can be derived from Fig. 2.8. The refilled epi is then planarized. The $p+$ layer is created by ion implantation.

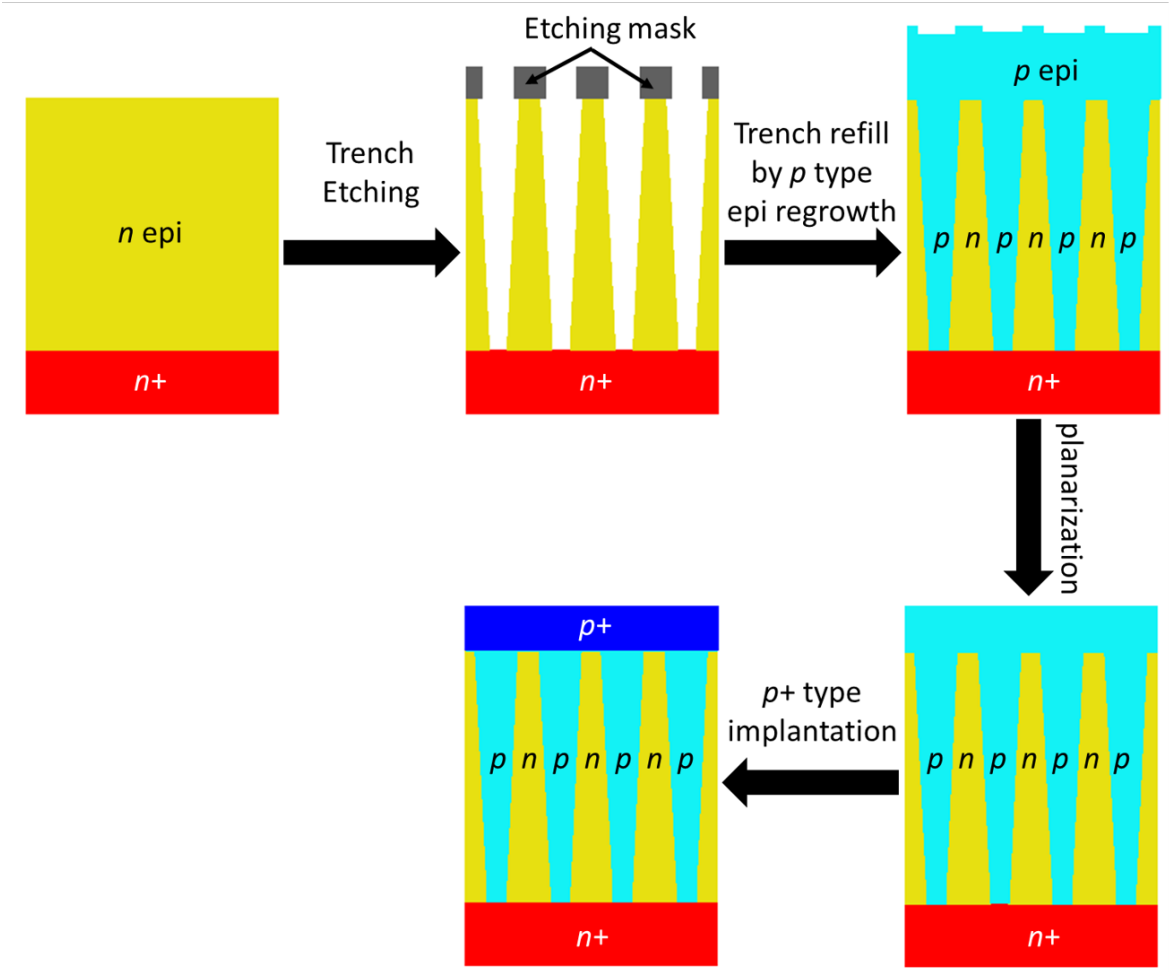
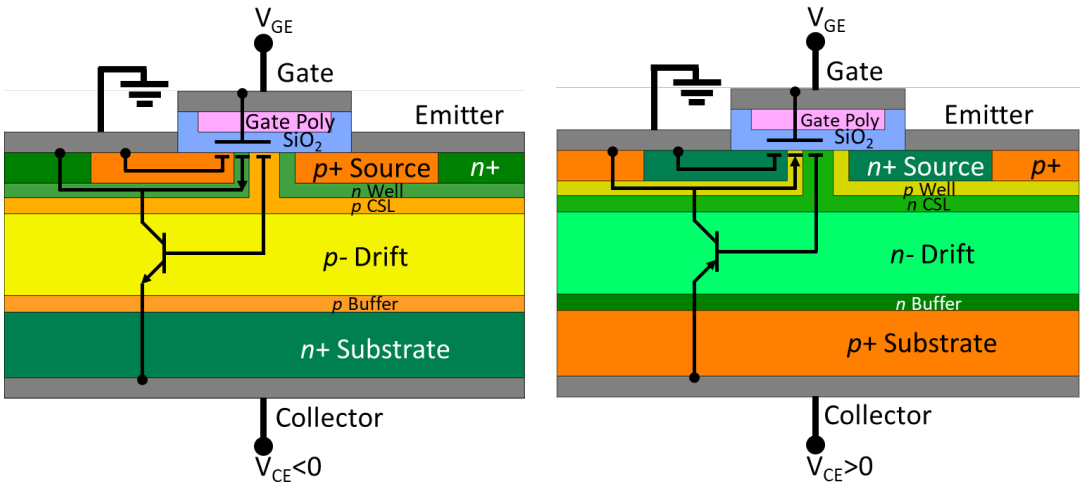


Figure 2.10. Typical process flow of the trench etch and refill method to fabricate a SJ p-n diode.

In this chapter we have discussed the practical limitations of a superjunction based power device in 4H-SiC. The lack of a mature and reliable process for fabricating such superjunction devices led us to consider the alternative approach of adapting n-channel IGBTs for use in this medium voltage range by incorporating a waffle substrate to support the thin required drift region. The design, fabrication and characterization of a such an IGBT will be discussed in the remaining chapters of this thesis.

3. A NOVEL 10 KV WAFFLE SUBSTRATE N-IGBT

The structure of an IGBT is essentially the same as a vertical MOSFET with the exception that the substrate is replaced by the opposite doping polarity. The IGBT can be seen as a combination of a bipolar junction transistor (BJT) and a MOSFET. 2D cross sections of a p-channel and an n-channel IGBT are shown in Figure 3.1(a) and 3.1(b) respectively. The p-channel IGBT is a combination of p-channel MOSFET and a thick base n-p-n BJT, whereas an n-channel IGBT is a combination of an n-channel MOSFET and a p-n-p BJT. The base current of the BJT is supplied through the channel of the MOSFET. The emitter and collector of the BJT are called the collector and emitter of the IGBT.



(a) (b)

Figure 3.1. Cross section of (a) a p-channel IGBT, and (b) an n-channel IGBT.

3.1 Analytical Model of an n-channel IGBT

The calculation of theoretical performance for any device is important for efficient design and fabrication. Advances in computational resources have enabled detailed theoretical studies using 2D and 3D numerical simulations. Nevertheless, 1D analytical models are very useful in understanding the basic physics of a device. It should be noted that the working principle of the waffle substrate n-channel IGBT remains same as a conventional n-channel

IGBT. A 1D slice shown in 3.2(b) through the p-n-p region of Figure 3.2(a) is useful to derive a simplified analytical model similar to the derivation for a p-channel IGBT described in [1]. For simplicity, we exclude the buffer and CSL layer in the structure. Carrier flow paths for electrons and holes are shown. The on-state potential drop across the device can be divided into five parts based on the following regions: anode, anode-drift junction (p-n), drift, JFET, and MOS channel. The components are shown as V_{Anode}, V_{PN}, V_{Drift}, V_{JFET}, and V_{MOS} in the 2D structure.

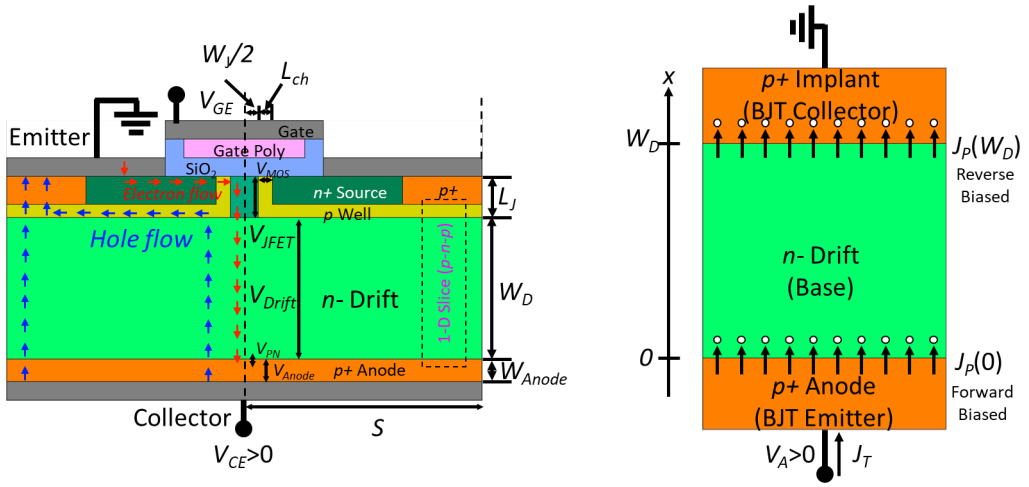


Figure 3.2. (a) 2D cross section of a n-channel IGBT identifying the main components of voltage drop, and (b) 1D slice (with BJT terminology) through p-n-p region of the IGBT for analysis where the applied voltage $V_A = V_{CE} > 0$.

The 1D cross section shown in Figure 3.2(b) is used to analyze the physics of an n-channel IGBT. This is a p-n-p BJT whose emitter (E) and collector (C) are the collector (C) and emitter (E), respectively, of the IGBT. The thick drift layer of the IGBT constitutes the base (B) of the BJT. In the on-state of the IGBT, the BJT is in the forward-active mode where $V_E > V_B > V_C$. The subscripts of the voltage and current parameters are used according to the BJT terminology throughout this section unless otherwise specified. The axis convention is shown in the figure, where the anode-drift junction is considered as the origin and the +x direction is considered as the direction of the current flowing into the collector. The base

current is supplied through the n-channel MOSFET, and it is assumed that these electrons will be available in the base region to satisfy recombination.

Let us find an expression for the carrier density in the base layer to calculate the current and potential drops in the different parts mentioned above. The equilibrium concentration of electrons and holes are represented as n_0 and p_0 while the deviations are Δn and Δp. Therefore, total electron n and p are given by

$$n = n_0 + \Delta n \qquad p = p_0 + \Delta p \tag{3.1}$$

In the on-state of the IGBT, high-level injection prevails in the very lightly doped base region, where $n \approx \Delta n \approx \Delta p \approx p$ because $\Delta n \gg n_0$ and $\Delta p \gg p_0$. Because of this high level injection of excess carriers into the drift layer, a significant reduction of resistivity occurs, which is known as the conductivity modulation. The carrier concentration (both electrons and holes) can become several orders of magnitude higher than the background doping. The continuity equations for electrons and holes can be written as

$$\begin{aligned} \frac{\partial n}{\partial t} &= \frac{1}{q}\frac{\partial J_N}{\partial x} + G \qquad \Rightarrow \qquad \frac{\partial \Delta n}{\partial t} = \frac{1}{q}\frac{\partial J_N}{\partial x} + G \\ \frac{\partial p}{\partial t} &= -\frac{1}{q}\frac{\partial J_P}{\partial x} + G \qquad \Rightarrow \qquad \frac{\partial \Delta p}{\partial t} = -\frac{1}{q}\frac{\partial J_P}{\partial x} + G \end{aligned} \tag{3.2}$$

where G is the local electron-hole net generation rate (or recombination rate if negative). The current densities $J_{N,P}$ can be found from the drift-diffusion equations as follows

$$\begin{aligned} J_N &= q\mu_N nE + qD_N\frac{\partial \Delta n}{\partial x} \\ J_P &= q\mu_P pE - qD_P\frac{\partial \Delta p}{\partial x} \end{aligned} \tag{3.3}$$

Now substituting the expression of $J_{N,P}$ from Eqn. (3.3) to Eqn.(3.2) we get

$$\begin{aligned} \frac{\partial \Delta n}{\partial t} &= \mu_N\frac{\partial}{\partial x}(nE) + D_N\frac{\partial^2 \Delta n}{\partial x^2} + G \\ \frac{\partial \Delta p}{\partial t} &= -\mu_P\frac{\partial}{\partial x}(pE) + D_P\frac{\partial^2 \Delta p}{\partial x^2} + G \end{aligned} \tag{3.4}$$

We also assume charge neutrality throughout the region, i.e. $\Delta n(x) \approx \Delta p(x)$. It is also assumed that the sample is in the dark so that only thermal generation/recombination exists. A mathematical manipulation of Eqns. (3.4) by multiplying the first by $\mu_P p$ and the second by $\mu_N n$, using Einstein relation, and adding the two equations yields

$$\frac{\partial \Delta n}{\partial t} = \left(\frac{p-n}{p/\mu_N + n/\mu_P}\right) E \frac{\partial \Delta n}{\partial x} + \left(\frac{p+n}{p/D_N + n/D_P}\right) \frac{\partial^2 \Delta n}{\partial x^2} + G \tag{3.5}$$

Under the high-level injection condition we can simplify Eqn. (3.5) further. We can define the ambipolar diffusion coefficient D_A as

$$D_A = \frac{p+n}{p/D_N + n/D_P} \approx \frac{\Delta p + \Delta n}{\Delta p/D_N + \Delta n/D_P} = \frac{2D_N D_P}{D_N + D_P} \tag{3.6}$$

The net Shockley-Read-Hall generation rate is given by

$$G = \frac{n_{\mathrm{i}}^2 - np}{\tau_P \left(n + n_1\right) + \tau_N \left(p + p_1\right)} \tag{3.7}$$

where, τ_N, τ_P are the minority carrier lifetimes of electrons and holes, n_{i} is the intrinsic carrier density, and if E_T is the energy of R-G centers then

$$\begin{aligned} n_1 &= n_{\mathrm{i}} \exp\left[\left(E_T - E_{\mathrm{i}}\right)/kT\right] \\ p_1 &= n_{\mathrm{i}} \exp\left[\left(E_{\mathrm{i}} - E_T\right)/kT\right] \end{aligned} \tag{3.8}$$

Again, under high-level injection condition G can be simplified as

$$G \approx \frac{-\Delta n^2}{\tau_N \Delta n + \tau_P \Delta n} = -\frac{\Delta n}{\tau_N + \tau_P} = -\frac{\Delta n}{\tau_A} \tag{3.9}$$

where $\tau_A = \tau_N + \tau_P$ is defined as the ambipolar carrier lifetime. Therefore, the expressions in Eqns. (3.5), (3.6) and (3.9) are used to formulate the ambipolar diffusion equation which is as follows,

$$\frac{\partial \Delta n}{\partial t} = D_A \frac{\partial^2 \Delta n}{\partial x^2} - \frac{\Delta n}{\tau_A} \tag{3.10}$$

In the steady-state condition, $\frac{\partial \Delta n}{\partial t} = 0$ which leads to a general solution of Eqn. (3.10) as

$$\Delta n(x) = \Delta p(x) = C_1 \sinh\left(x/L_A\right) + C_2 \cosh\left(x/L_A\right) \tag{3.11}$$

where $L_A = \sqrt{D_A \tau_A}$ is defined as the ambipolar diffusion length, and the constants C_1 and C_2 can be determined using the proper boundary conditions. Evaluating Eqn. (3.11) at $x = 0$ and $x = W_D$ we get,

$$\Delta p(x) = \Delta p(0) \frac{\sinh\left[\left(W_D - x\right)/L_A\right]}{\sinh\left(W_D/L_A\right)} \tag{3.12}$$

The total current at any point is equal to the sum of the electron and hole current, i.e. $J_T = J_N(x) + J_P(x)$. In case of n-channel IGBT, we assume that holes are injected from BJT emitter to the base with unity injection efficiency. Therefore, $J_P(0) = J_T$ and $J_N(0) = 0$. The condition of charge neutrality in the base region yields from Eqn. (3.3),

$$E(0) = -\frac{D_N}{\mu_N} \frac{1}{n(0)} \frac{\partial n}{\partial x}\bigg|_{x=0} = -\frac{kT}{q} \frac{1}{p(0)} \frac{\partial p}{\partial x}\bigg|_{x=0} \tag{3.13}$$

Solving for $\Delta p(x)$ we get from Eqns. (3.3), (3.12) and (3.13)

$$\Delta p(x) = \Delta n(x) = \frac{J_T L_A}{2qD_P} \frac{\sinh\left[\left(W_D - x\right)/L_A\right]}{\cosh\left(W_D/L_A\right)} \tag{3.14}$$

Conductivity modulation in IGBTs is lower than in p-i-n diodes because holes (for an n-channel IGBT) are extracted efficiently by the BJT collector-base junction and electrons are not injected from the other side.

To calculate the potential drop across the drift region, let us find an expression for electric field $E(x)$. The total current at any point x can be written as,

$$\begin{aligned} J_T = J_N(x) + J_P(x) = q\mu_N \left[n(x)E(x) + \frac{kT}{q} \frac{\partial n}{\partial x} \right] + \\ q\mu_P \left[p(x)E(x) - \frac{kT}{q} \frac{\partial p}{\partial x} \right] \end{aligned} \tag{3.15}$$

The lightly doped drift layer has a doping of N_D, and therefore we can write $n(x) = \Delta n(x) + N_D^+$ and $p(x) = \Delta p(x)$ where $\Delta n(x) = \Delta p(x)$. Solving for $E(x)$ from Eqns. (3.14) and (3.15) we get,

$$E(x) = \frac{kT}{qL_A}\left[\frac{\frac{2\mu_P}{\mu_N+\mu_P}\cosh\left(\frac{W_D}{L_A}\right) + \frac{\mu_N-\mu_P}{\mu_N+\mu_P}\cosh\left(\frac{W_D-x}{L_A}\right)}{\sinh\left(\frac{W_D-x}{L_A}\right) + \frac{qD_AN_D^+}{J_TL_A}\cosh\left(\frac{W_D}{L_A}\right)}\right] \tag{3.16}$$

Equation (3.16) indicates that the electric field in the drift region is not independent of total current. A careful observation of Eqn. (3.14) shows that $\Delta p(x) \gg N_D^+$ does not hold true near the base-collector junction of the BJT because $\sinh\left(\frac{W_D-x}{L_A}\right)$ becomes very small as $x \to W_D$. The second term $\theta = \frac{qD_AN_D^+}{J_TL_A}\cosh\left(\frac{W_D}{L_A}\right)$ in the denominator of Eqn. (3.16) ensures $E(x \to W_D)$ to be finite. However, $E(x)$ is almost uniform and independent of J_T throughout the drift layer except the region explained above. The calculated electric field is a positive quantity which drives the holes toward the BJT collector and electrons toward the BJT emitter, consistent with the carrier flow shown in Figures 3.2(a) and 3.2(b). Integrating the $E(x)$ expression we can calculate the electrostatic potential as a function of position, which is

$$\begin{aligned}\psi(x) = \psi(0) + \frac{kT}{q}\Bigg\{&\frac{\mu_N-\mu_P}{\mu_N+\mu_P}\ln\left[\frac{\sinh\left(\frac{W_D-x}{L_A}\right)+\theta}{\sinh\left(\frac{W_D}{L_A}\right)+\theta}\right] + \frac{4\mu_P}{\mu_N+\mu_P}\frac{\cosh\left(\frac{W_D}{L_A}\right)}{\sqrt{1+\theta^2}} \\ &\times\left[\tanh^{-1}\left(\frac{\theta\tanh\left(\frac{W_D-x}{2L_A}\right)-1}{\sqrt{1+\theta^2}}\right) - \tanh^{-1}\left(\frac{\theta\tanh\left(\frac{W_D}{2L_A}\right)-1}{\sqrt{1+\theta^2}}\right)\right]\Bigg\}\end{aligned} \tag{3.17}$$

It is important to note that the spatial change in electrostatic potential represents the change in $E_{\rm i}(x)$ across the drift layer. The voltage drop in the drift layer must be equal to the change in electron quasi-Fermi level F_N across the drift layer. The electron quasi-Fermi potential and electrostatic potential can be written as $\psi_N(x) = -F_N(x)/q$ and $\psi(x) = -E_{\rm i}(x)/q$. The electron density in the drift region is given by

$$n(x) = \Delta n(x) + N_D^+ = n_{\rm i}\exp\left[\frac{F_N(x) - E_{\rm i}(x)}{kT}\right] \tag{3.18}$$

Therefore, we get

$$\psi_N(x) = \psi(0) + \frac{kT}{q}\left\{\frac{\mu_N - \mu_P}{\mu_N + \mu_P}\ln\left[\frac{\sinh\left(\frac{W_D - x}{L_A}\right) + \theta}{\sinh\left(\frac{W_D}{L_A}\right) + \theta}\right] + \frac{4\mu_P}{\mu_N + \mu_P}\frac{\cosh\left(\frac{W_D}{L_A}\right)}{\sqrt{1+\theta^2}}\right.$$
$$\times\left[\tanh^{-1}\left(\frac{\theta\tanh\left(\frac{W_D - x}{2L_A}\right) - 1}{\sqrt{1+\theta^2}}\right) - \tanh^{-1}\left(\frac{\theta\tanh\left(\frac{W_D}{2L_A}\right) - 1}{\sqrt{1+\theta^2}}\right)\right] \tag{3.19}$$
$$\left. - \ln\left[\frac{J_T L_A}{2qD_P n_{\rm i}}\frac{\sinh\left(\frac{W_D - x}{L_A}\right)}{\cosh\left(\frac{W_D}{L_A}\right)} + \frac{N_D^+}{n_{\rm i}}\right]\right\}$$

The total voltage drop across the drift layer can be calculated from $V_{Drift} = \psi_N(0) - \psi_N(W_D)$ which gives

$$V_{Drift} = \frac{kT}{q}\left\{ - \frac{\mu_N - \mu_P}{\mu_N + \mu_P}\ln\left[\frac{\theta}{\sinh\left(\frac{W_D}{L_A}\right) + \theta}\right] - \frac{4\mu_P}{\mu_N + \mu_P}\frac{\cosh\left(\frac{W_D}{L_A}\right)}{\sqrt{1+\theta^2}}\right.$$
$$\times\left[\tanh^{-1}\left(\frac{-1}{\sqrt{1+\theta^2}}\right) - \tanh^{-1}\left(\frac{\theta\tanh\left(\frac{W_D}{2L_A}\right) - 1}{\sqrt{1+\theta^2}}\right)\right] \tag{3.20}$$
$$\left. - \ln\left[\frac{J_T L_A}{2qD_P N_D^+}\tanh\left(\frac{W_D}{L_A}\right) + 1\right]\right\}$$

Let us now calculate the base (J_B) and collector (J_C) current density which is used to calculate the other voltage drops. Total electron charge stored in the drift layer can be calculated by integrating the carrier density given in Eqn. (3.14) and thus we have

$$Q_{stored} = -q\int_0^{W_D}\Delta n(x)\,dx = \frac{J_T L_A^2}{2D_P}\left[\frac{1}{\cosh\left(\frac{W_D}{L_A}\right)} - 1\right] \tag{3.21}$$

The base current density (J_B) is the electron current ($J_N(W_D)$) at $x = W_D$ which can be calculated from the total recombination current in the base defined by $-Q_{stored}/\tau_A$. Therefore, we get,

$$J_B = J_N(W_D) = \frac{\mu_N J_T}{\mu_N + \mu_P}\left[1 - \frac{1}{\cosh\left(\frac{W_D}{L_A}\right)}\right] \tag{3.22}$$

The collector current can easily be calculated by subtracting the base current from the emitter current (J_T) which is also the hole current at $x = W_D$. So, we get

$$J_C = J_P(W_D) = \frac{\mu_P J_T}{\mu_N + \mu_P}\left[1 + \frac{\mu_N}{\mu_P}\frac{1}{\cosh\left(\frac{W_D}{L_A}\right)}\right] \tag{3.23}$$

The law of junction is applied to the anode-drift junction to calculate the voltage drop (V_{PN}). We know that,

$$\begin{aligned} p(0)n(0) \approx \Delta n(0)^2 = n_{\mathrm{i}}^2 \exp\left(\frac{qV_{PN}}{kT}\right) \\ \Rightarrow V_{PN} = \frac{2kT}{q}\ln\left[\frac{J_T L_A}{2qD_P n_{\mathrm{i}}}\tanh\left(\frac{W_D}{L_A}\right)\right] \end{aligned} \tag{3.24}$$

Let us assume that the thickness, doping and hole mobility in the anode layer are W_{Anode}, N_{Anode} and μ_{Anode} then the voltage drop across the anode layer is given by

$$V_{Anode} = \frac{J_T W_{Anode}}{q\mu_{Anode} N_{Anode}} \tag{3.25}$$

The MOSFET supplies the base current of the IGBT, and contributes a voltage drop due to the channel resistance. The specific on-resistance of the channel ($R_{MOS,SP}$) can be expressed in terms of the channel length (L_{CH}), cell pitch (S), inversion mobility (μ_{inv}), oxide capacitance (C_{ox}), gate voltage (V_G), and threshold voltage (V_T). Therefore, the voltage drop in the channel is given by

$$V_{MOS} = J_B R_{MOS,SP} = \frac{\mu_N J_T}{\mu_N + \mu_P}\left[1 - \frac{1}{\cosh\left(\frac{W_D}{L_A}\right)}\right]\left[\frac{L_{CH} S}{\mu_{inv} C_{ox}|V_G - V_T|}\right] \tag{3.26}$$

Only base current flows in the JFET region, and the corresponding voltage drop can be found by multiplying J_B by the specific on-resistance of the JFET ($R_{JFET,SP}$) derived in [1]. Let us consider that the width, thickness, length, and doping of the JFET are W, L_J, W_J, and N_J. The voltage drop across the JFET can be expressed as follows,

$$V_{JFET} = \frac{\mu_N J_T}{\mu_N + \mu_P}\left[1 - \frac{1}{\cosh\left(\frac{W_D}{L_A}\right)}\right]\left[\frac{L_J}{q\mu_J N_J^+}\left(1 - \sqrt{\frac{2\varepsilon_s\left(\psi_{BI} + V_S\right)}{qN_J(W_J/2)^2}}\right)^{-1}\right] \tag{3.27}$$

where $\psi_{BI} = \frac{kT}{q} \ln\left(\frac{N_A N_J}{n_i^2}\right)$, N_A is the doping in the p-well and $V_S = V_{MOS}$ is the voltage drop in the channel.

The total voltage drop across the IGBT is then calculated by

$$V_{CE} = V_{Anode} + V_{PN} + V_{Drift} + V_{JFET} + V_{MOS} \tag{3.28}$$

The I-V characteristics of the IGBT using these analytical equations are valid for the linear region only which is the region of normal operation for power switches. Equation (3.26) would need to be modified to calculate the characteristics in the saturation region.

3.2 Limitations of *n*-channel IGBTs

An n-channel MOS device is always preferable over a p-channel device in 4H-SiC because the channel electron mobility is higher than the hole mobility by about an order of magnitude. It should also be noted that conductivity modulation in the drift region is the key to IGBT operation that makes the drift region resistance essentially negligible, irrespective of its doping type. However, a traditional SiC n-channel IGBT suffers from the high resistivity of its p-type substrate. The $p+$ substrate is highly resistive because the bulk hole mobility in 4H-SiC is also almost an order of magnitude lower that that of the electron mobility [1]. Therefore, a trade-off between the resistances of the channel and substrate exists for an IGBT. The conventional way of fabricating a SiC n-channel IGBT is to epitaxially grow a thin layer of $p+$ as an anode on an $n+$ substrate, and after completing the top-side processing, grind off the substrate to make the contact to the anode layer. The effective resistance of the $p+$ anode layer is thus reduced by dramatically reducing its thickness. Resistance is also reduced by using an epitaxially grown layer, where the mobility is higher compared to a substrate grown by sublimation (or other techniques) having unwanted impurities and point defects [1]. An thick epitaxially grown $p+$ substrate could reduce the associated resistance somewhat, but is neither a significant improvement, nor a cost effective solution.

A power device is rated by its blocking voltage and on-state current density at a given power dissipation density. The blocking voltage is mostly determined by the drift layer thickness and doping. Since a thin $p+$ anode layer is used instead of a thick $p+$ substrate

in an n-channel IGBT, the drift layer must be sufficiently thick as shown in Figure 3.4(a) to support itself after substrate removal. Therefore, a conventional n-channel IGBT is limited to an ultra high voltage ($>$ 15 kV), so for low- to mid-range voltage devices a p-channel IGBT is preferred. It has been reported [28] that it is possible to fabricate an n-channel IGBT for $V_{BR} < 15$ kV where the substrate is completely removed but the robustness of this device in terms of handling and breakage is in question.

3.3 Proposed Waffle-Based n-channel IGBT

We propose for the first time the novel approach of an n-channel IGBT on a waffle-like $n+$ substrate [29] for a blocking voltage of 12.5 kV. This structure solves the problem of fabricating an n-channel IGBT for low- to mid-range blocking voltages. The revolutionary idea of a waffle substrate was initially proposed to reduce the substrate resistance for low voltage ($<$ 1 kV) SiC MOSFETs [29]. The waffle patterns are typically made up of repeated squares, hexagons or circles, arranged in a close-packed array. Figure 3.3 shows a 3D cross section of the unit cell of a square shaped waffle pattern. Let us assume that the thicknesses of the substrate and the remaining material are t_1 and t_2 respectively. The lateral outer and inner lengths are d_1 and d_2 respectively. The specific resistance of the waffle is calculated by the following expression, as described in [30].

$$R_{Waffle,SP} = \rho t_1 \left[\frac{1}{1 + (d_2/d_1)^2 (t_1/t_2 - 1)} \right] \tag{3.29}$$

where ρt_1 is the specific resistance of the material before the waffle etching. The resistance decreases as the etching depth is increased.

The mechanical strength of the waffle substrate is very important to support the n-channel IGBTs in the low- and mid-range voltages. The process development and the mechanical strength testing on the waffle substrate were completed by my colleague Dr. Noah Opondo [30], and will be explained here briefly. The stiffness of a material is an indicator of how much force is required for a given displacement. A ball on ring experiment is reported in the article along with simulation data obtained using ANSYS^{TM}. The simulations show that the stiffness of a waffle pattern on a $180 \sim 200\,\mu$m substrate with $20\,\mu$m of remaining

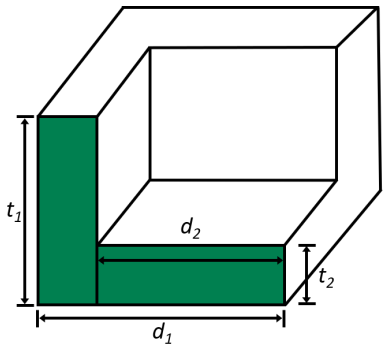


Figure 3.3. 3D Cross section of an n-type square shape waffle substrate.

material is comparable to that of a 110 µm thinned substrate, like that reported by Infineon [31].

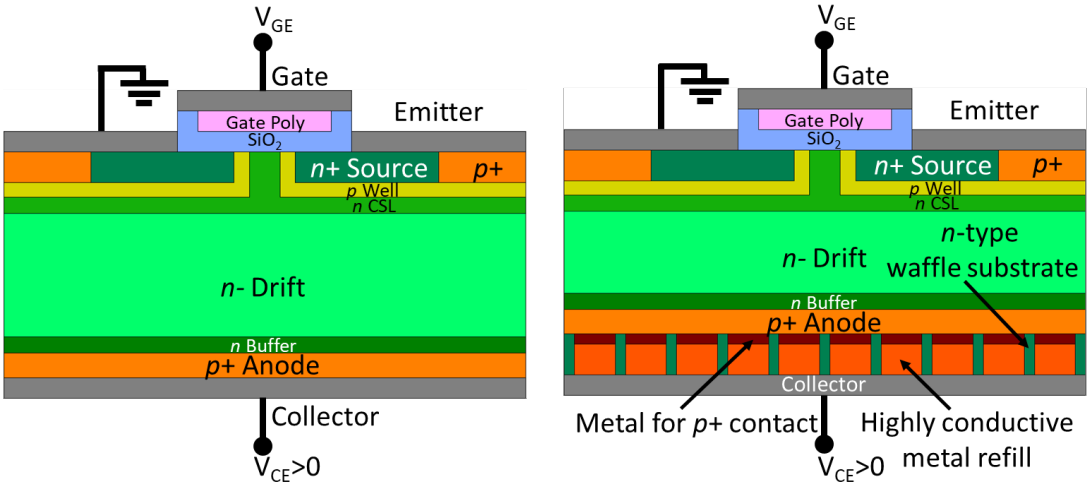


Figure 3.4. Cross section of (a) an n-channel IGBT with thin p+ anode and very thick drift layer, suitable for ultra high voltage, and (b) an n-channel IGBT with thin p+ anode, moderately thick drift layer and n-type waffle substrate, suitable for low to mid range voltages.

In the case of an n-channel IGBT, a complete removal of the n-type SiC from the etched part of the waffle pattern is necessary to expose the p+ anode. The pockets are then refilled with an appropriate highly conductive metal such as copper as shown in Figure 3.4(b). Approximately 90% of the substrate material is removed, and the refilled metal provides

both an electrical and a heat conducting path. The resulting structure has a negligible electrical resistance, and comparable thermal conductivity compared with the original substrate. The resistivity and thermal conductivity of electroplated copper is 1.7×10^{-6} Ω.cm and 4.0 $\mathrm{Wcm^{-1}K^{-1}}$ [32], while a typical n-type 4H-SiC substrate is 1.5 - 2.8×10^{-2} Ω.cm [33] and 3.3 $\mathrm{Wcm^{-1}K^{-1}}$ [1]. Therefore, a successful demonstration of waffle substrate integration in an medium voltage n-channel IGBT would open a new horizon of high voltage power devices.

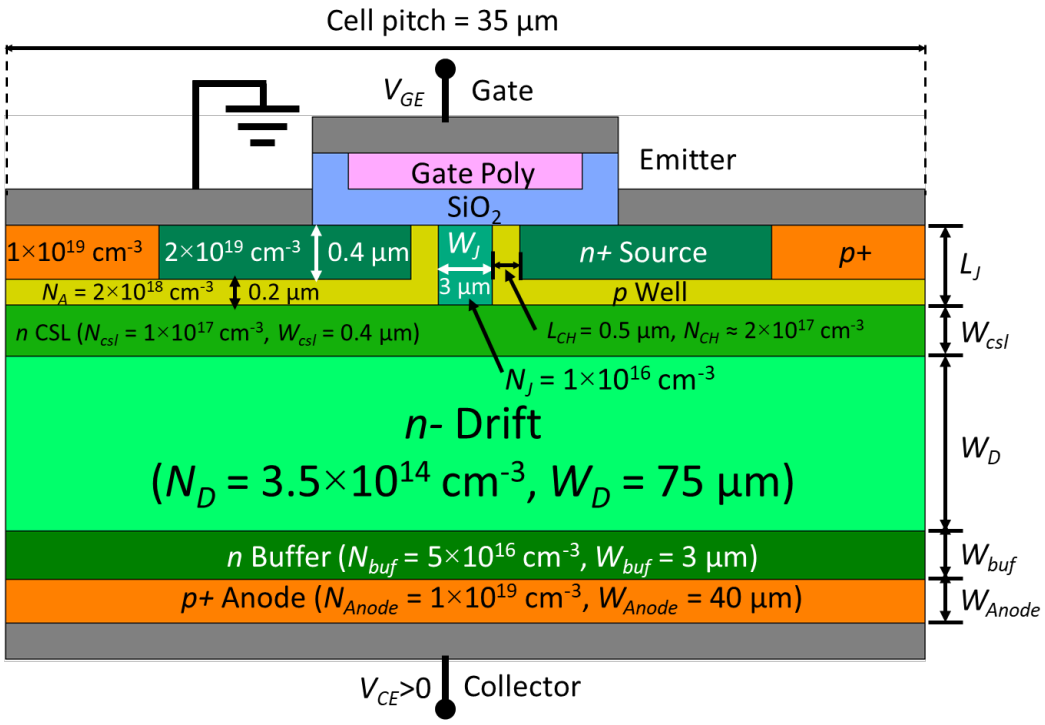
3.4 On-State Performance Analysis and Design

3.4.1 Current-voltage characteristics

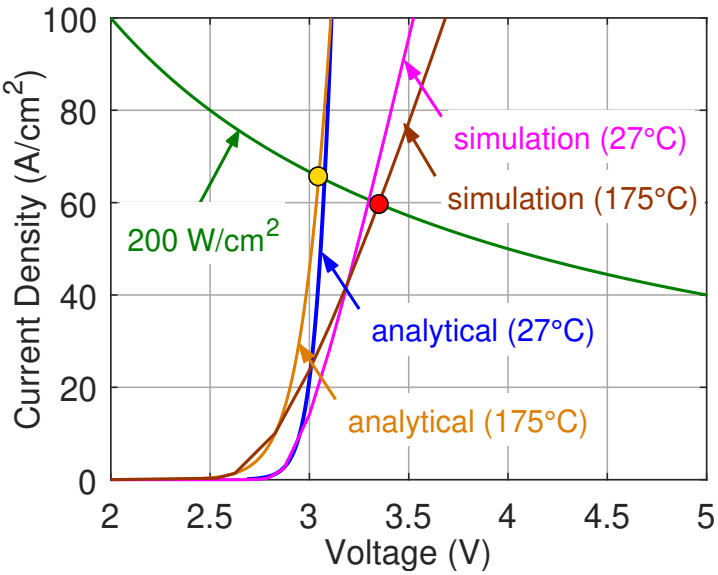
The analytical expression of the voltage drop across the IGBT as a function of total current is extremely helpful to understand the forward characteristics of the device. Let us consider an n-channel IGBT with the parameters shown in Figure 3.5(a). The half cell pitch of the device is 17.5 μm considering the alignment tolerance and minimum feature size possible by photolithography during the fabrication. The CSL and buffer layers are excluded from the analytical calculation.

The on-state performance of the n-channel IGBT is explained in a plot of on-state current density as a function of applied voltage as shown in Figure 3.5(b). The analytical model is used to compute the current at 27 °C and 175 °C. A 2D simulation is carried out based on the structure and parameters shown in Figure 3.5(a) using Sentaurus TCAD software. In both cases, the electron mobility in the inversion layer is considered as 25 $\mathrm{cm^2V^{-1}s^{-1}}$ and the gate bias is $V_{GE} = 14\,\mathrm{V}$ with a threshold voltage $V_{TH} = 6.9\,\mathrm{V}$. The carrier mobilities used in the calculation/simulation are based on the following doping and temperature dependent models [1].

$$\begin{aligned} \text{Electron mobility: } \mu_N &= \frac{1141\,(T/300)^{-2.8}}{1+\left[(N_A+N_D)/1.94\times10^{17}\right]^{0.61}} \\ \text{Hole mobility: } \mu_P &= \frac{124\,(T/300)^{-2.8}}{1+\left[(N_A+N_D)/1.76\times10^{19}\right]^{0.34}} \end{aligned} \tag{3.30}$$



(a)



(b)

Figure 3.5. (a) Device parameters used in both the analytical model (excluding the CSL and buffer layers) and the 2D simulations. Device is designed for V_{BR} = 12.5 kV (b) On-state characteristics at high temperature by both analytical calculation and numerical simulation.

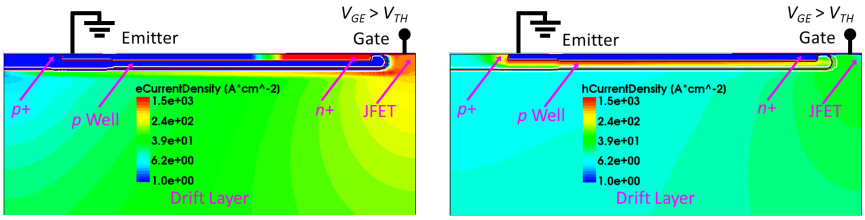
Conductivity modulation in the lightly doped drift layer is the key to the superior performance of an IGBT. In order to maintain the high conductivity, carrier lifetime must be sufficiently high so that a significant fraction of injected holes can travel through the entire layer without recombining. This typically requires an ambipolar lifetime of $\geq$ 5 μs, with longer lifetimes leading to longer diffusion lengths and thus more complete conductivity modulation. A significant voltage drop occurs at the anode/drift junction, but conductivity modulation reduces the voltage drop in the drift layer significantly, which is the dominant factor in high voltage devices. An IGBT is rated by its blocking voltage and on-state current density at a given power dissipation level. In this example, we consider 200 W/cm^2 as the expected power dissipation limit.

High power devices are prone to high junction temperatures during normal operation. Therefore they suffer from significant thermally induced mobility degradation leading to conductivity reduction. However, the IGBT is robust in this situation as can be seen from the I-V plot in Figure 3.5(b). In fact, it shows slightly better performance at higher temperature. Mobility degradation at high temperatures leads to a reduction in the ambipolar diffusion coefficient, but is roughly balanced by an increase in carrier lifetime [1]. As a result, the ambipolar diffusion length increases slightly with temperature, making the IGBT on-state performance almost independent of temperature.

We consider a constant ambipolar lifetime of 5 μs to find the I-V characteristics using the analytical model, and as shown in Figure 3.5(b), an on-state current density of 65.7 A/cm^2 is achieved at V_{ON} = 3 V for the expected power density limit. The emitter current of the IGBT is found to be about 32% of its total current density, with the remaining current flowing through the MOSFET channel.

The on-state characteristics obtained from the 2D simulations are more accurate because they include two dimensional carrier flow patterns and potential distributions. The ambipolar lifetime used in these simulations is more realistic because it is calculated as a function of temperature and excess carrier density, but with an effective ambipolar lifetime of 5 μs. It shows a current density of 59.7 A/cm^2 at V_{ON} = 3.35 V. The electron and hole current density plots at V_{ON} = 3.3 V in Figure 3.6 help illustrate the current flow paths. The electron current path is through the JFET and channel regions, while the hole current

path is through the p-well of the MOS structure, and is consistent with the flow directions shown in Figure 3.2(a). The emitter current, which is the hole current passing through the $p+$ contact, is about 18% of the total. The amount of current through the $p+$ contact is therefore significant, and the contact resistance must be as low as possible. The simulation considers a realistic doping profile in the CSL, JFET, base, and source instead of constant box profile. The mobility in the JFET region is found slightly lower compared to the analytical calculation. It is also true for channel mobility. Figure 3.6(a) shows that the current density in the JFET and channel region is very high and the percentage of channel current is higher in the simulation than the analytical model, which leads to higher voltage drop in these two regions compared to the analytical calculation.

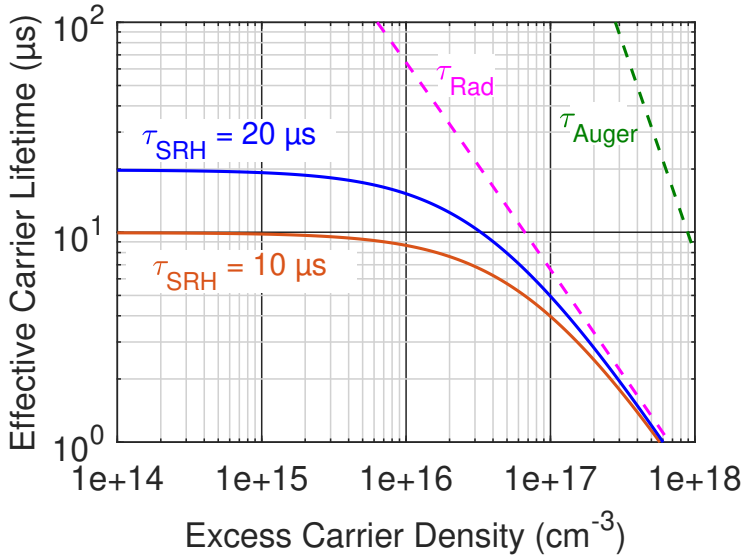


(a) (b)

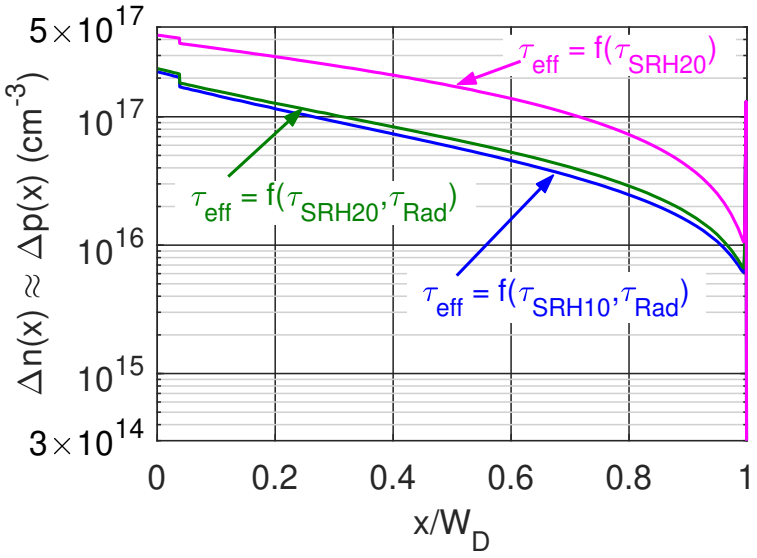
Figure 3.6. TCAD simulation at $V_{ON} = 3.35$ V (a) Electron current density (b) Hole current density.

3.4.2 Role of ambipolar carrier lifetime

Carrier lifetime has opposite effects on the on- and off- state performance of the IGBT. In the on-state, it is desirable to have a long ambipolar carrier lifetime so that conductivity modulation in the drift layer prevails. The ambipolar lifetime is calculated by adding the electron and hole high level injection lifetimes as given in Eq. (3.9). In 4H-SiC, three major recombination mechanisms are important: Shockley-Read-Hall (SRH), radiative, and Auger. There are many reported studies on this topic, but results in [34] and [35] are particularly relevant because of the high level injection and high temperature conditions prevalent in the SiC IGBT. The effective carrier lifetimes are shown in Figure 3.7(a), considering constant



(a)



(b)

Figure 3.7. (a)Ambipolar lifetime in the drift region as a function of excess carrier concentration at $T = 175\,°C$ (b) Excess carrier profile along the drift layer by simulation at 200 W/cm^2 and $T = 175\,°C$ for various effective lifetimes including SRH and/or radiative mechanisms. The anode/buffer junction is located at $x/W_D = 0$, and the CSL/p-well junction is at $x/W_D = 1$.

SRH lifetimes of 10 µs and 20 µs. Fortunately, Auger recombination is negligible in 4H-SiC at high temperature [34]. However, radiative recombination lifetime is reduced significantly

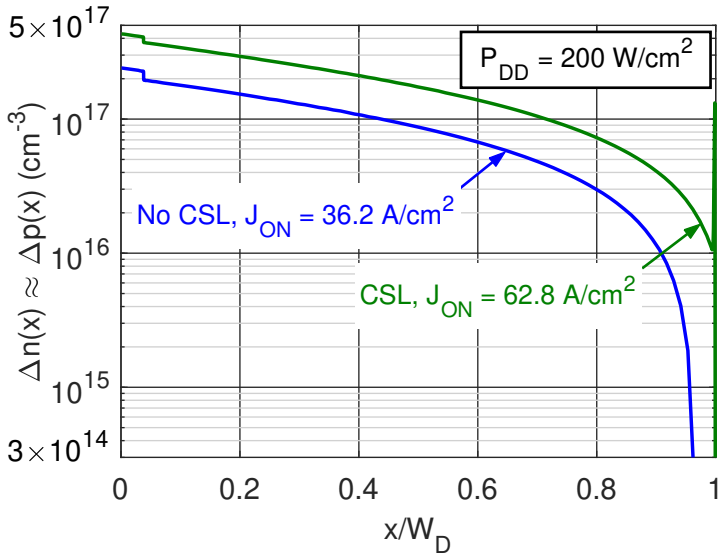
as the excess carrier concentration increases, but SRH lifetime remains unaffected [35]. A significant reduction of effective lifetime is observed as the excess carrier density exceeds $1 \times 10^{16}\,\mathrm{cm}^{-3}$. The temperature dependence of these two recombination mechanisms in SiC is not known very well to date.

The impact of effective lifetime on conductivity modulation can be explained with the help of Figure 3.7(b) where excess carrier density is plotted as a function of position in the drift layer for various lifetimes and at a power dissipation density 200 W/cm^2. The effective lifetimes τ_{eff1} and τ_{eff2} are the functions of SRH and radiative mechanisms with SRHs 10 μs and 20 μs respectively, whereas τ_{eff3} is a function of SRH lifetime = 20 μs only. The carrier injection near the anode/buffer junction is $\geq 1 \times 10^{17}\,\mathrm{cm}^{-3}$ which makes τ_{eff1} and τ_{eff2} close to 5 μs, leading to an ambipolar diffusion length of $\sim$ 37 μm, and τ_{eff3} leads to an L_A of 74 μm. Longer diffusion lengths increase the carrier injection density as seen from the figure, and the profile agrees well with the hyperbolic analytical equation (3.14). The step like profile near the origin is at the buffer/drift junction, where the density falls down abruptly near the drift/CSL junction because holes are extracted efficiently by the p-well due to the high electric field in the depletion region. The spike near the CSL/p-well junction is explained in the following section.

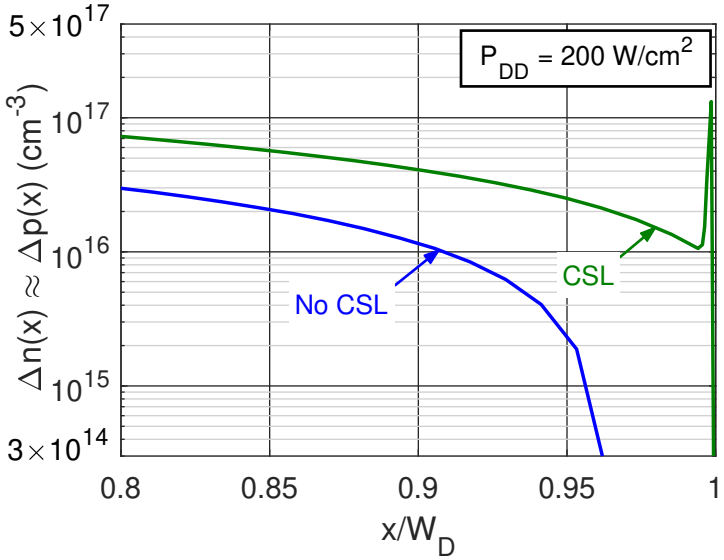
Methods to improve carrier lifetimes in SiC have been reported by many researchers to date. In [36], it is shown that deep level defects created by carbon vacancies (known as $Z_{1/2}$ centers) are responsible for short lifetimes, and can be removed by carbon implantation and diffusion. It can also be improved by high temperature (1400°C) oxidation as reported in [37].

On the contrary, a short lifetime is desirable for reducing switching losses in this bipolar device. The thin buffer layer shown in Figure 3.5(a) could be made to have very short lifetime. This could be achieved for example by vanadium doping as reported in [38]. Our interest in this project is to demonstrate the functionality of waffle substrate based IGBT through on-state I-V and off-state V_{BR} characteristics. Therefore, lifetime enhancement in the drift region was performed while no reduction procedure in the buffer layer.

3.4.3 Necessity of a carrier storage layer (CSL)



(a)



(b)

Figure 3.8. The effect of the CSL layer on drift layer conductivity modulation as demonstrated by the simulated excess carrier profile at 200 W/cm^2 and T = 175°C for a constant effective lifetime of $\tau_{eff} = 20\,\mu$s. The anode/buffer junction is located at $x/W_D = 0$, and the CSL/p-well junction at $x/W_D = 1$ (a) Full view (b) Enlarged view near CSL/p-well junction.

A thin moderately doped n layer between the drift and p-well layer is known as a "carrier storage layer" [39]. The degree of conductivity modulation in the drift region greatly depends on this layer, as observed by the simulated drift region excess carrier profile with and without a CSL layer shown in Figure 3.8. High carrier density near the CSL/p-well junctions is similar to that of a p-i-n. A retrograde diffusion potential appears in this region that prevents the easy flow of holes through to the $p+$ contact, and thus they are stored in the vicinity of this region [39]. The width of the depletion region in the drift layer is significantly higher where there is no CSL and it causes a large voltage drop that leads to a lower on-current at a given V_{ON}. It is reported in [40] that because of this depletion region, electron currents are suppressed by its high resistance. In other words, the CSL helps to spread the electron base current more uniformly. Although carrier lifetime and the corresponding ambipolar diffusion length are same for both cases, the carrier injection is remarkably lower if there is no CSL. However, the doping and thickness of the CSL layer can not be increased arbitrarily because it reduces the blocking capability in the off-state.

3.5 Off-State Performance Analysis and Design

3.5.1 Parallel plane breakdown analysis

The IGBT is said to be in the forward blocking state if the gate bias is pulled below the threshold voltage. It can also be operated in the reverse blocking state when the polarity of the applied voltage in between collector and emitter of the IGBT is reversed and $V_{GE} < V_{TH}$. However, we are interested mainly in the forward blocking state. In a power device, the blocking voltage is primarily determined by the doping and the thickness of the drift layer. A first order approximation of drift layer doping and thickness is possible using a one dimensional analysis. The doping dependent critical field model given in Eqn. (1.5) is used in this calculation.

The 1D electric field profile shown in Figure 3.9 is based on a punch through design where buffer layer acts as a field stop layer. It assumes a drift layer that is completely depleted before breakdown at 12.5 kV. Let us consider the parameters shown in Figure 3.5(a) to calculate the drift layer thickness. The slope m_1, m_2, and m_3 are calculated from the doping

values of CSL, drift, and buffer layers respectively. The area under the electric field profile represents the blocking voltage V_{BR}, and the small contribution from the buffer layer is neglected. Therefore we can write the expression for blocking voltage as follows:

$$V_{BR} \approx \frac{1}{2}E_c t_{csl} + \frac{1}{2}(t_{csl} + t_{drift})E_{csl} + \frac{1}{2}E_{buf}t_{drift} \tag{3.31}$$

where E_c is the critical electric field calculated using Eqn. (1.5) for $N = N_{csl} = 1 \times 10^{17}\,\mathrm{cm}^{-3}$, $E_{csl} = E_c - m_1 t_{csl}$ and $E_{buf} = E_{csl} - m_2 t_{drift}$. Equation (3.31) becomes a quadratic function of t_{drift}. By solving the equation we find that 50.2 μm thick drift layer is required to block 12.5 kV.

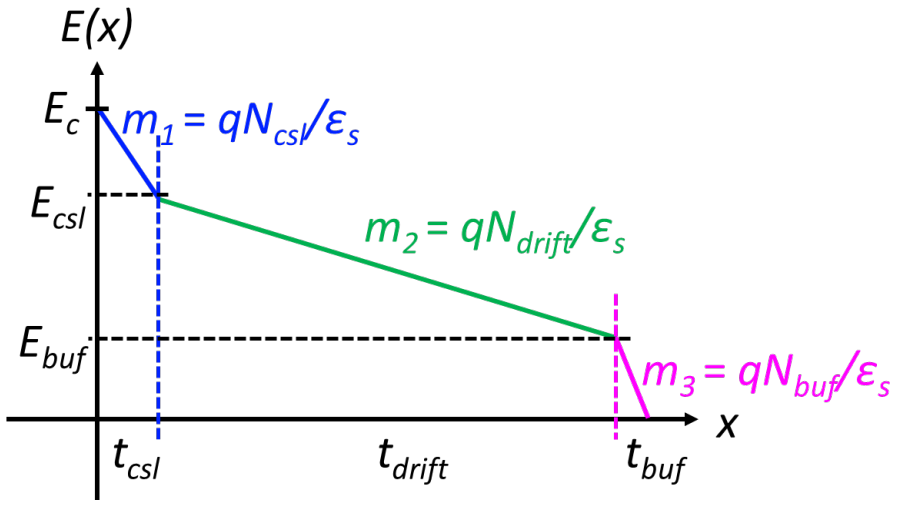
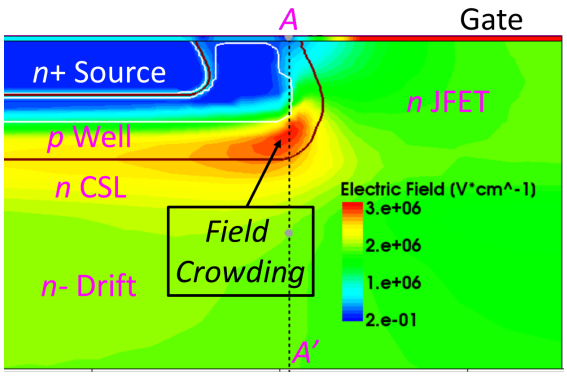


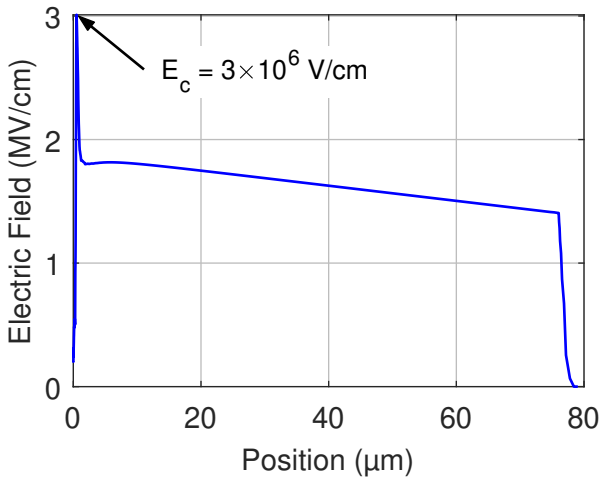
Figure 3.9. First order approximation of electric field profile in the forward blocking mode.

Numerical simulation is necessary to verify the results from the first order approximations, and corrections must be made accordingly. The Sentaurus Device simulation tool is capable of calculating the ionization integral to determine the voltage at which avalanche breakdown occurs, as well as the maximum electric field in both the semiconductor and in the gate oxide. The software solves the Poisson equation to obtain the electric field distribution, which is required to separately calculate the ionization integral for electrons and holes. The electric field profile presented in Figure 3.10(a) is more accurate than the 1D profile because

it considers the effects of the 2D distribution of charge in the device. The simulation shows that the required drift layer as calculated by the 1D analysis is not sufficient to block 12.5 kV. Instead at least 75 µm is required, which results in a maximum electric field in the oxide below 5 MV/cm and at the Base-CSL junction 3 MV/cm. This difference in estimated drift layer thickness is due to the fact that the 1D analysis does not consider any possible field crowding as seen in 2D simulation plot at the Base-CSL junction. The field crowding effect is also exacerbated by wide JFET regions.



(a)



(b)

Figure 3.10. Breakdown voltage (V_{BR}) as found by avalanche breakdown simulations. (a) Electric field distribution (b) Electric field profile along the cut line AA'.

3.5.2 Edge termination

In power semiconductor devices, premature avalanche breakdown at the edges of a device is a well known problem. It is very unlikely to obtain the parallel plane breakdown voltage described in the previous section because of 2D field crowding at the periphery of the device. There are several solutions [1] to this problem, including floating field rings (FFR), junction termination extensions (JTE), multiple floating zones (MFZ), and space modulated JTEs. In this project, we are using an FFR based scheme to solve the edge termination problem. Unfortunately, edge termination requires a significant amount of area, especially for high voltage devices. Recently, Van Brunt *et.al.* [41] reported that almost 65% of their total device area was consumed by their FFR edge termination structure.

We have used extensive Sentaurus simulations to find an appropriate FFR edge termination design for our device. In general, it is desirable that the edge termination be capable of blocking at least 80% [42] of the calculated parallel plane blocking voltage. A schematic cross section of an FFR system is shown in Fig. 3.11.

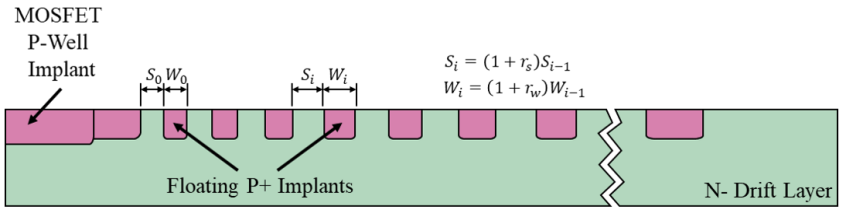
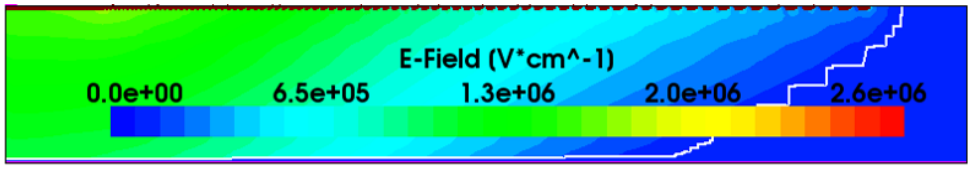
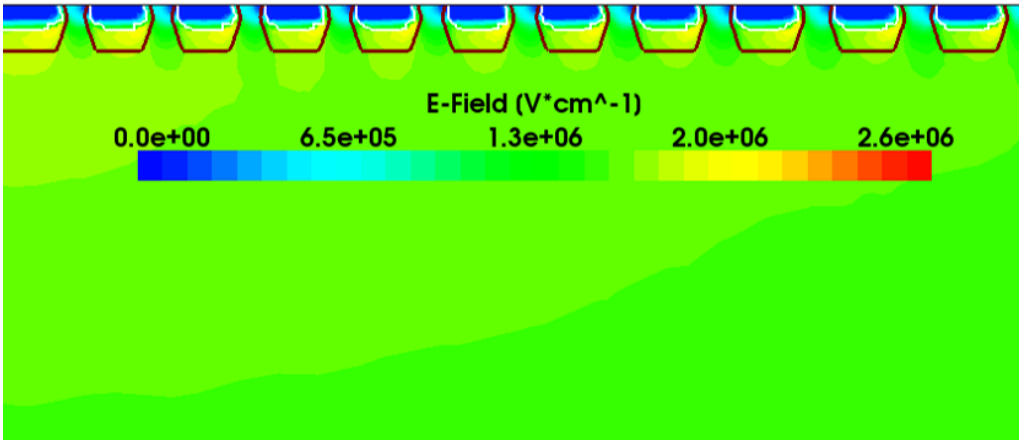


Figure 3.11. Schematic structure of an FFR system with initial spacing s_0, initial width w_o, spacing growth rate r_s, width growth rate r_w.

The purpose of the FFR structure is to distribute the electrostatic potential laterally at the edge of the device so that the peak electric field at the main p-well/n-drift junction does not reach the critical field level prematurely due to two-dimensional field crowding. Approximately 50 simulations were carried out to find the maximum blocking capability. We have found that the total required width of the FFR array is 387.5 μm, with 80 implanted FFR rings. However, in our design we included a few more rings to make it 85 so that any merging of the initial narrow dimensional rings can be compensated. The electric field distribution of this system is shown in Figure 3.12.



(a)

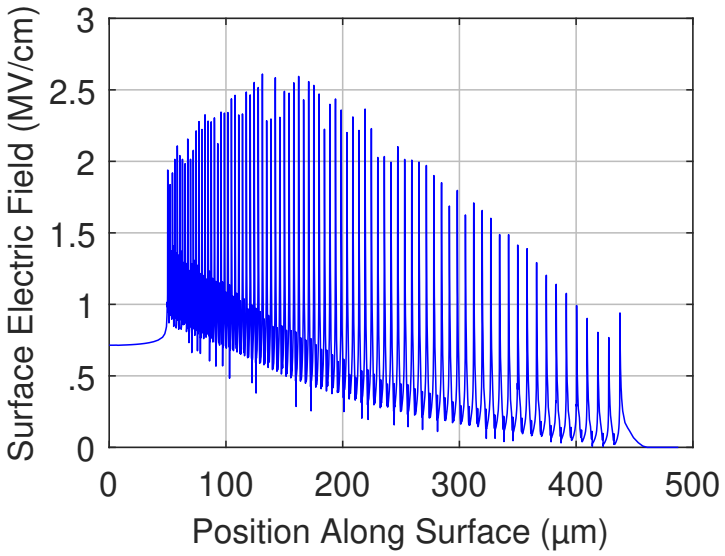


(b)

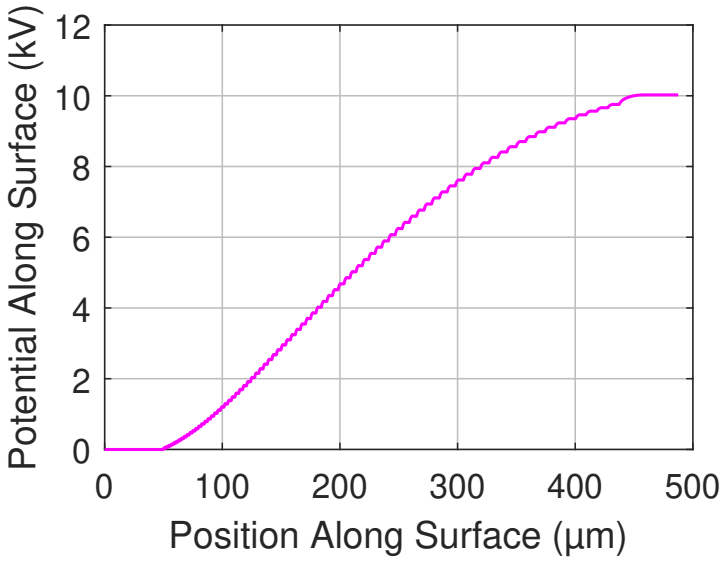
Figure 3.12. Electric field distribution in the FFR structure. The initial spacing $s_0 = 1$ μm, the first ring width $w_0 = 1$ μm, and both increase by 2%/ring (a) Complete system (b) Enlarged view of a few rings.

The spacing between the main junction and the first ring is $s_0 = 1\,\mu$m and the width of the first ring is also $w_0 = 1\,\mu$m. Both the spacing and ring width increase by 2% from one ring to the next. The simulation predicts that this design is capable of blocking 10 kV, or 80% of the drift layer 1D breakdown voltage of 12.5 kV.

The peak electric field profile and corresponding electrostatic potential is shown in Figure 3.13. The electrostatic potential rises from 0 V to 10 kV in a staircase profile since the rings are not fully depleted, and thus the potential within each ring is constant. It is desirable to have roughly equal electric field peaks laterally along the surface to maximize the blocking capability. There is room for improvement in this regard. Since the rings are floating, a transient simulation is required where the Poisson and continuity equations are solved simultaneously.



(a)

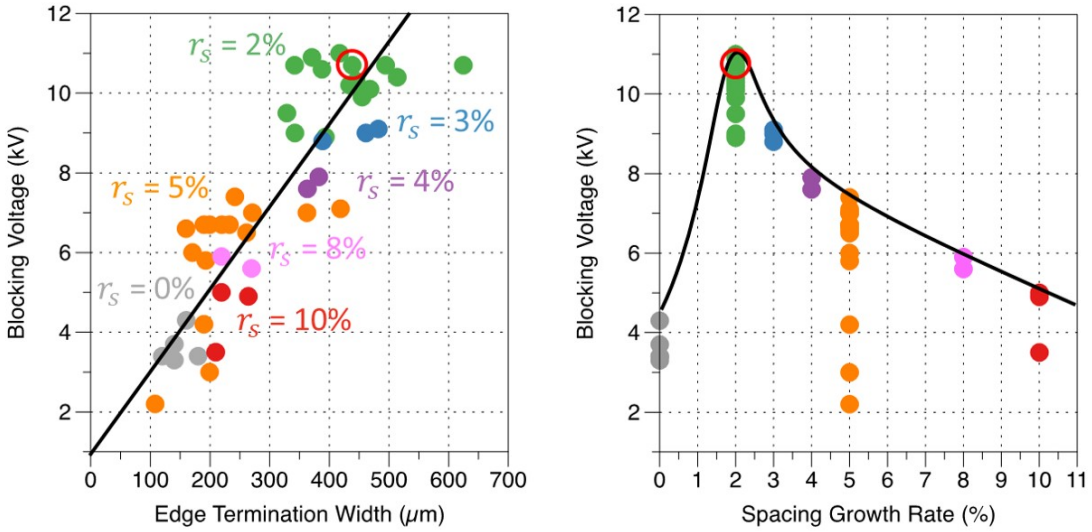


(b)

Figure 3.13. (a) Electric field and (b) electrostatic potential as a function of position along the surface.

The simulation is tremendously time consuming to fully optimize. It is a 5 dimensional optimization problem with paramters s_0, w_0, r_s, r_w, and n, the number of rings in the array. The simulated data is summarized in Fig. 3.14. The general trend line in Fig. 3.14(a) indicates that higher blocking voltage is achieved as we reduce the growth rates of the spacing

and the width, down to 2% per ring. However, Fig. 3.14(b) shows that the blocking voltage capability decreases rapidly as the spacing growth rate decreases below 2%. Therefore, a 2% growth rate was found to be optimal.



(a) (b)

Figure 3.14. (a) Blocking voltage capability as a function of total edge termination width, (b) Blocking voltage capability as a function of spacing growth rate.

4. MASK LAYOUT AND FABRICATION PROCESS OF 10 KV N-CHANNEL IGBT

4.1 Introduction of the Waffle-Substrate IGBT Process

The demonstration of a waffle-based n-channel IGBT is the primary purpose of this thesis. The MOSFET part of the IGBT could be either a UMOSFET or a DMOSFET. We plan to fabricate the device with a DMOSFET structure because its fabrication process is comparatively mature. It is a common practice to include some test structures along with the active devices in the mask layout. The test structures, also referred to as process control modules, are used to identify and debug unexpected circumstances during and after the fabrication as well as to verify the expected performance.

4.2 Mask Layout for the Fabrication

The mask layout is an essential part of device fabrication. There are many software packages that can be used for designing a layout, but we have chosen KLayout for this purpose. This is an open source software package, and includes the capability to automate the layout using scripts written in both Python and Ruby, along with conventional layout methods. We chose the approach of a script-based layout in Ruby. We identified twelve lithography masks that are required to complete the fabrication process. Eleven of them are required for processing the front side of the sample, and the remaining one is for the back side waffle substrate pattern. Front side processing includes ten photo and one e-beam lithography mask steps.

The design is based on three design rule sets (A,B, and C), based on alignment tolerance (AT) between subsequent layers and minimum feature (MF) size. The rule sets are named using (AT/MF) terminology: Rule A (2/3), Rule B (3/3) and Rule C (4/5), where bracketed numbers are in microns. In the latter two design rules the tolerances and minimum feature sizes are relaxed to increase the probability of having working devices in the worst case scenario. The original plan for the process was to use a contact lithography tool (SUSS MA6), so a quartz mask set was made by Toppan Photomasks, Inc. However, later

the Birck Nanotechnology Center introduced a maskless aligner, a Heidelberg MLA150, in which physical masks are not required. This new tool was used for most of the processes. There are two types of devices in the layout: IGBT devices and process control modules as discussed in the following subsections.

4.2.1 IGBT layout strategy

In laying out the IGBTs, we decided on three device types based on the design rules described above and denoted Device A, B, and C. The minimum feature sizes and alignment tolerances for the three device types are shown in Table 4.1.

Table 4.1. Minimum feature sizes (λ_{min}) and alignment tolerances (δ)

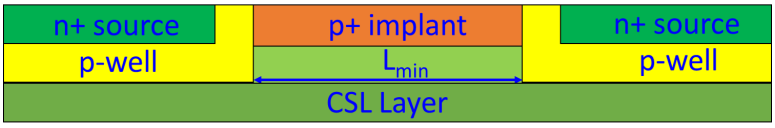
Device Type	$\boldsymbol{\lambda_{min}}$ **(μm)**	$\boldsymbol{\delta}$ **(μm)**
Device A	3	2
Device B	3	3
Device C	5	4

In this fabrication process, 13 major steps and 11 lithography masks are required to complete the top side processing. Two steps do not require masks: 1) The carbon implantation process is a blanket implantation (see Section 4.3.1), and 2) The source implantation is self aligned to the *p*-well mask. Three alignment reference mask layers are used for the subsequent layers as listed in Table 4.2.

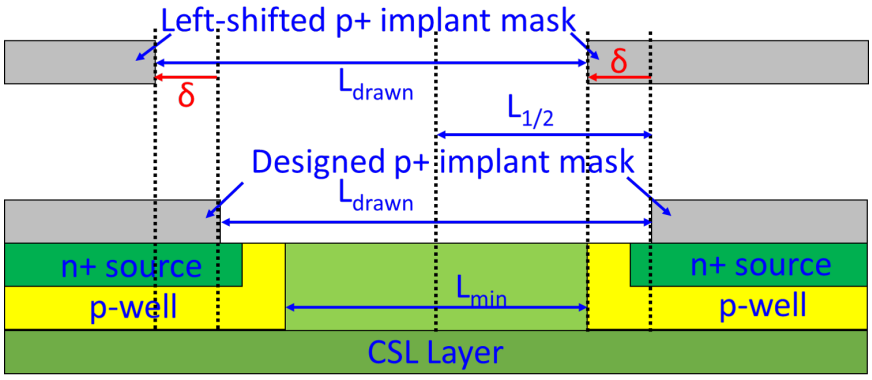
The CSL implantation mask (# 1) is the reference layer for aligning the *p*-well implantation mask (# 3), which in turn becomes the reference layer for all the remaining top side processing masks except the gate ILD etch (# 10) and top ohmic metal (# 11) masks. The polysilicon gate mask (# 7) acts as the reference layer for masks # 10 and # 11 to reduce the cell pitch by diminishing the number of stacked alignment tolerances between the layers.

Table 4.2. List of reference mask layers for the subsequent processes

Process Step	Mask ID	Mask Name	Reference Mask
2	1	CSL Implant	Not applicable
3	2	Alignment Mark 1	CSL Implant
4	3	p-well Implant	CSL Implant
6	4	Alignment Mark 2	p-well Implant
7	5	$p+$ Implant	p-well Implant
8	6	FOX Window	p-well Implant
9	7	Polysilicon Gate	p-well Implant
10	8	$p+$ Contact	p-well Implant
11	9	Source Contact	p-well Implant
12	10	Gate ILD Etch	Polysilicon Gate
13	11	Top Metal	Polysilicon Gate



(a)

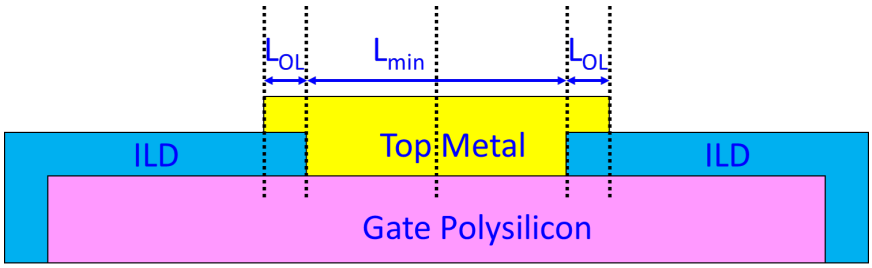


(b)

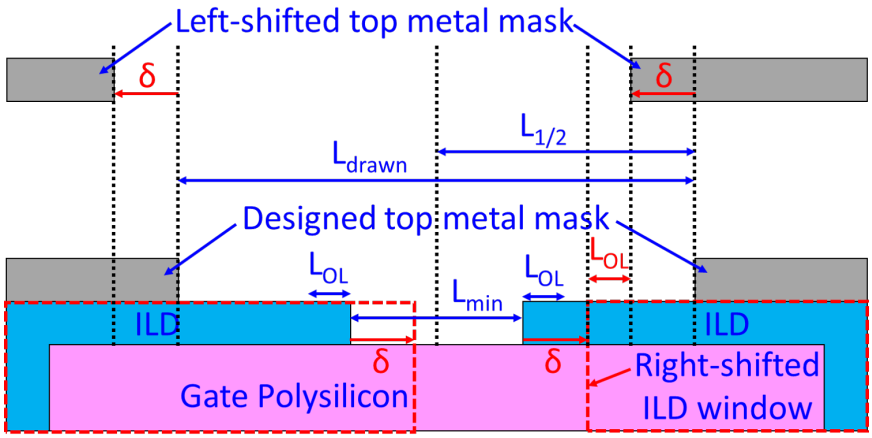
Figure 4.1. (a) Schematic cross section showing the ion implanted p-well, source and $p+$ layers (b) A worst case scenario of $p+$ implant mask misalignment.

The design rule set and the reference layer together defines various dimensions for a mask of interest. This can be understood by considering a simple example case. Calculation of required dimensions of the the $p+$ implantation window is explained with the help of Fig. 4.1. In this case, the minimum required dimension of $p+$ layer is L_{min} while the mask is aligned with the previously defined p-well implant. A worst case scenario arises when the mask is misaligned by δ to its left. In order to ensure the minimum window length, the right edge of the shifted mask should be in alignment with the right edge of the p-well. This is symmetric with the center line. The right half length of the drawn mask window can be calculated by $L_{1/2} = L_{min}/2+\delta = L_{drawn}/2$. Therefore, for $L_{min} = 4$ µm and $\delta = 2$ µm, the drawn dimension should be 8 µm.

A more complicated situation arises when a feature involves layers which are aligned to an additional common mask layer. For example, the gate ILD etch and top metal masks are each aligned to polysilicon gate mask. Figure 4.2(a) shows a window of minimum length L_{min} in the ILD, and a minimum overlap of the top metal layer and ILD of L_{OL} on both sides. Figure 4.2(b) explains how to calculate the dimension of the top metal window in order to ensure the minimum contact length L_{min} and the overlap. Once again, this is a problem of symmetry around the center line. A worst case scenario is to have a right shift of the ILD window mask by δ, combined with a left shift of the top metal mask, also by δ. The red dash line shows the shifted ILD window. In order to ensure the minimum overlap even with this shifted ILD window, the top metal mask window should be such that when it shifts to the left it still maintains the overlap. The dimensions annotated in the figure ends up with a simple equation $L_{1/2} = L_{min}/2+2\delta+L_{OL}$. Therefore, for a given $L_{min} = 10$ µm, $L_{OL} = 1$ µm, and $\delta = 2$ µm the drawn window in the top metal mask becomes 20 µm.



(a)



(b)

Figure 4.2. (a) Schematic cross section showing a top metal contact over an ILD window (b) A worst case misalignment scenario with ILD window and top metal misaligned in oppoosite directions with respect to a common p-well reference mask.

Following the methodology described above, the actual drawn dimensions of $p+$ contact length and the $n+$ source contact length are found to be 8 μm and 8 μm respectively in Device A. There is an overlap between the gate and source of 2.5 μm, and the gate and source contact metal are separated by an interlayer dielectric (ILD) of length 1 μm. The original design of $p+$ mask was based on optical lithography, but the $p+$ implantation pattern was moved to e-beam lithography because it also defines the edge termination floating field ring features with a minimum dimension of 1 μm. The e-beam lithography process has a negligible alignment tolerance compared to optical lithography. However, in the worst case misalignment of the $p+$ contact metal mask, the effective $p+$ contact length would be 4 μm. The gate can also be misaligned to the left which will make the effective source contact

length 4 μm. On the other hand, if the gate polysilicon is misaligned to the right then it will still overlap the source by a margin of 0.5 μm.

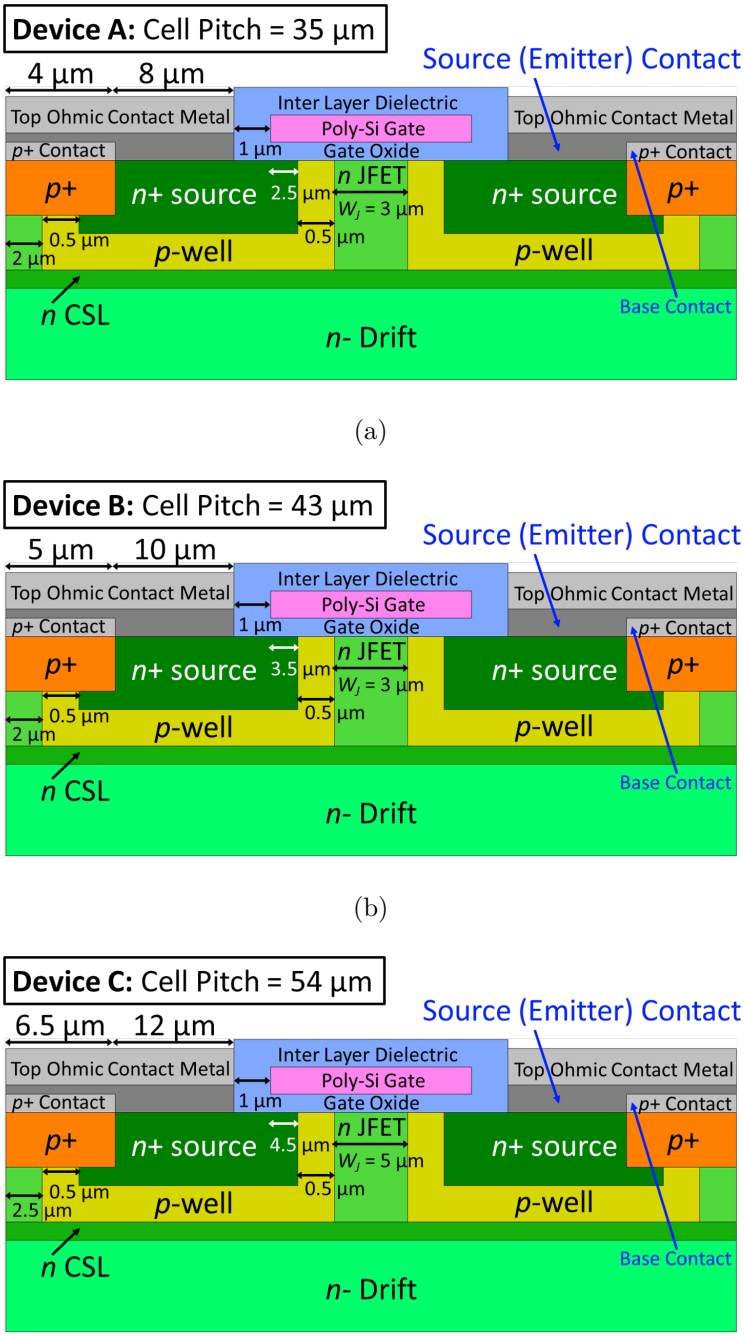


Figure 4.3. Schematic cross section of three types of IGBT devices in the mask layout and denoted as (a) Device A (cell pitch = 35 μm) (b) Device B (cell pitch = 43 μm) (c) Device C (cell pitch = 54 μm).

Figure 4.3(a) shows a cross section indicating various dimensions calculated by the above mentioned methodology, which results in a unit cell pitch of 35 μm. The required drawn dimensions of each feature depend on the design rule set used in a particular device. For example, the requirement of a 3 μm alignment tolerance in Device B increases the required dimensions compared with Device A. The effective top metal to gate contact lengths are the same as Device A, even in the worst case misalignment. The unit cell pitch of this device is found as 43 μm as shown in the cross section of Fig. 4.3(b).

The lowest possible cell pitch is always preferable to accommodate as many unit cells as possible in a given area, but to increase the probability of having some working devices in the worst case scenario, the minimum feature size and the alignment tolerance are increased for Device C. Therefore, the half cell pitch is also increased to maintain minimum $p+$ and source contact lengths in the worst case scenario. They are found to be 5.5 μm and 4 μm respectively, and the unit cell pitch of Device C is 54 μm as annotated in Fig. 4.3(c).

A methodology similar to that described above was applied to each feature, with an equation describing each drawn dimension as a function of the design rules. This produced a fully parameterized layout which can easily be adapted to different design rules.

Table 4.3. Device active area.

Device Size	**Device A (cm^2)**	**Device B (cm^2)**	**Device C (cm^2)**
Small	1.53×10^{-3}	1.35×10^{-3}	1.14×10^{-3}
Medium	1.53×10^{-2}	1.15×10^{-2}	1.05×10^{-2}
Large	-	1.19×10^{-1}	-

Figure 4.4 shows the overall n-channel IGBT mask layout. It includes three different sizes of each device type as listed in Table 4.3. The devices were designed to conduct 60 A/cm^2 at a maximum power density of 200 W/cm^2. Therefore, the maximum and the minimum currents are expected to be carried by large device B and small device C devices are 7.14 A and 0.068 A. Some of the devices of each size are protected by floating field ring

edge terminations. The total areas, including edge termination, of the small, medium, and large devices are 0.018 cm^2, 0.046 cm^2, and 0.216 cm^2 respectively.

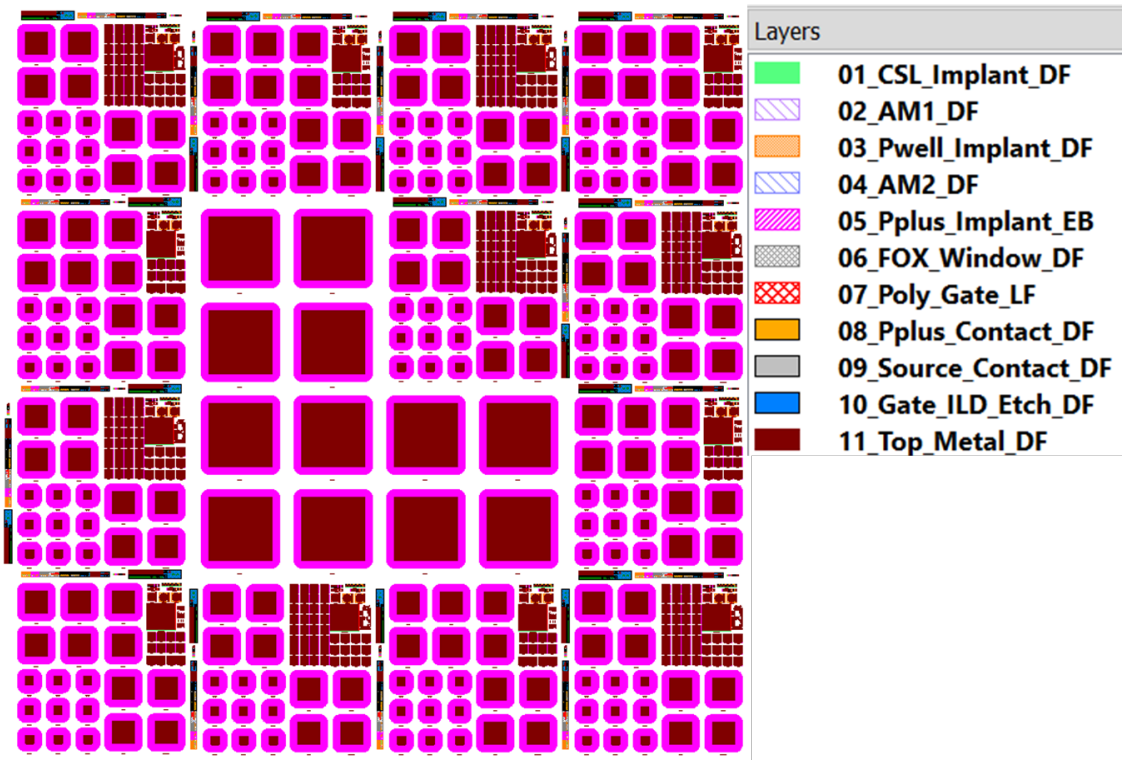
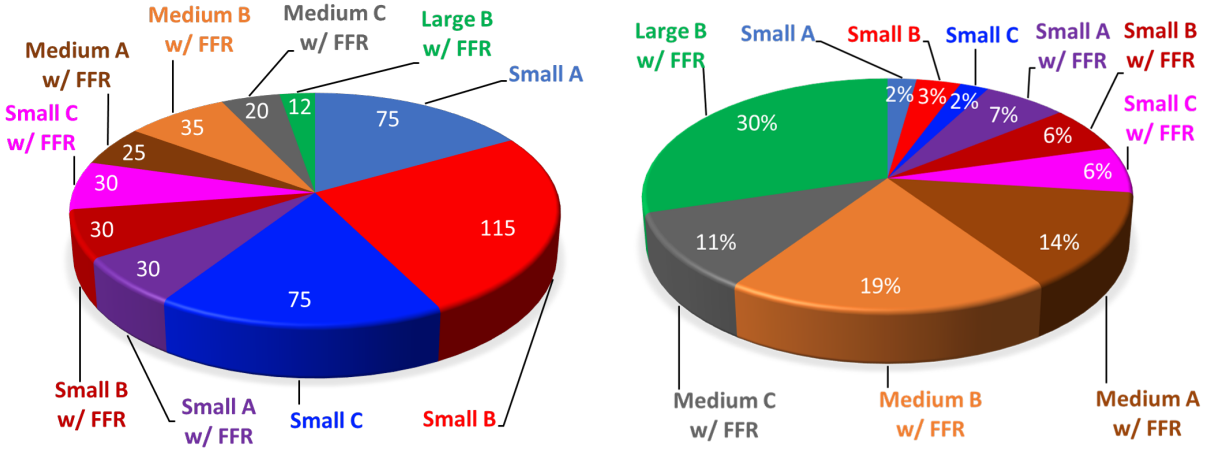


Figure 4.4. Complete n-channel IGBT mask layout.



(a) (b)

Figure 4.5. Distribution of devices in terms of (a) Number of devices (b) Total area occupied.

The mask layout is comprised of about 1 cm × 1 cm dies with various types of devices. The fabrication is carried out on samples each comprised of a quarter of a 100 mm wafer containing thirteen die. A pie chart of number of IGBT devices of different sizes is shown in Figure 4.5. Each sample contains 447 IGBT devices, with 41% protected by floating field rings, and 12 large devices occupy 30% of the total area.

4.2.2 Layout of process control modules

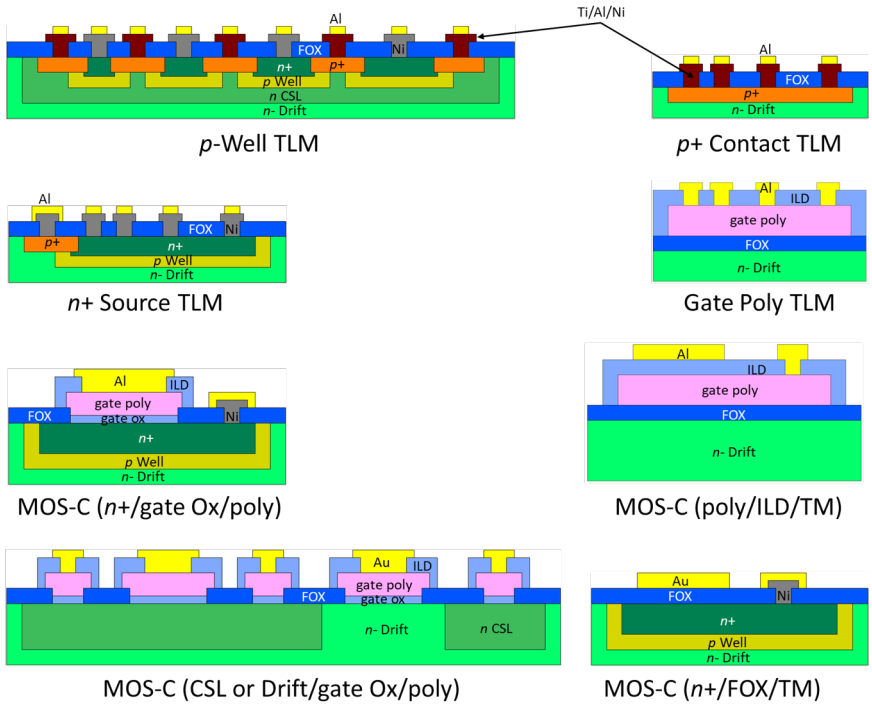


Figure 4.6. Schematic cross sections of the four TLMs and five MOSCAPs included in the mask layout.

One of the most important parameters specific contact resistivity is extracted by applying transfer length method as described in [43] where the structures are called TLM. In this structure, metal contacts pads are fabricated with variable spacing between them which are used for the analysis. We have designed four TLM structures to extract specific contact resistivity and sheet resistance of the underneath semiconductor layer. Another important modules are metal oxide semiconductor capacitors (MOSCAP) where an oxide layer is de-

posited on a semiconductor layer. This structure is useful to characterize the oxide properties as well as doping of the semiconductor. Five MOSCAPs are also included, which along with the TLMs comprise the process control modules as shown in Figure 4.6. Included are TLMs on the p-well, $p+$ implant, $n+$ source, and gate polysilicon layers. The TLM structures are 50 µm × 100 µm wide, and six contact pads are placed with varying separations (only four are shown in the cross section) which provide five data points. Three MOSCAPs are placed on the $n+$ source, n CSL, n- drift layers using gate poly and gate oxide. The other two are constructed with top metal/ILD/gate poly and top metal/field oxide/$n+$ source.

4.3 Fabrication Process

Development of the required unit processes is the first step in developing any fully integrated fabrication process. The development of an n-channel IGBT process based on a DMOSFET structure is convenient because there are many published works on the DMOSFET. Nevertheless, hands on experience is required to design, plan and improve the processes, and adapt them to the currently available fabrication equipment at Purdue. Development of the unit steps is described in the subsequent sections.

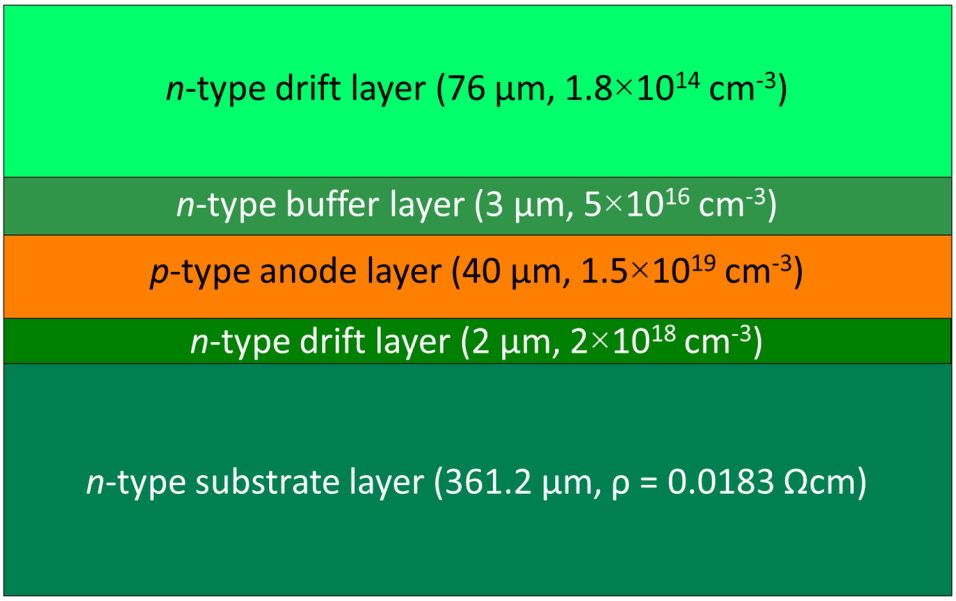


Figure 4.7. Starting wafer cross section with required layer thicknesses and doping levels.

A cross section of the wafer that we used for the fabrication along with there thickness and doping is shown in Fig. 4.7. It consists of three epi layers such as n-type drift, buffer and p-type anode layers. The n-type substrate followed by a thin n epi layer is required to grow the anode layer. We first diced two such 100 mm wafers into quarters, with the plan to fabricate IGBTs on the second and third quarters from each wafer. These samples are named PU435Q2, PU435Q3, PU436Q2, and PU436Q3, where Q stands for "quarter". The other four quarters (PU435Q1, PU435Q4, PU436Q1, and PU436Q4) were planned to be used as control samples as necessary. The fabrication process is explained in great detail in the appendix. The following subsections discuss the highlights of each major fabrication step.

4.3.1 Carbon implantation for carrier lifetime enhancement

Carrier lifetime plays an important role in IGBT operation. High dose carbon implantation followed by a high temperature anneal is a useful method of lifetime enhancement [44]. Four of the samples (PU435Q1, PU435Q3, PU436Q1, and PU436Q3) were processed using this method. A thin screen oxide is first formed on the sample to prevent the formation of unwanted surface contamination and roughness during the ion implantation. The samples were then solvent cleaned, followed by a standard RCA clean. They were oxidized in the Protemp furnace tube # 7 for 7 hours in a wet condition at 1100°C. The oxide thickness was measured using a Filmetrics F40 to be about 30 nm. Ion implantation profiles generally follow a Pearson distribution described by four moments: mean, standard deviation, skewness and kurtosis. Mean and standard deviation are popularly known as range and straggle when used in the context of ion implantation. We have used the TRIM Monte Carlo simulation tool [45] to generate the moments for carbon implantation into SiC. Then the Pearson distribution equations [46] were utilized in a Matlab program to generate an approximate 1-D box profile using 3 implants at different energies as shown in Fig. 4.8. The samples were sent to CuttingEdge Ions to perform a blanket implantation of carbon with a total dose of 1.35×10^{16} cm^{-2}. The box profile is achieved by implantation at energies of 15 keV, 50 keV,

and 110 keV with doses 2×10^{15} cm^{-2}, 5×10^{15} cm^{-2}, and 7×10^{15} cm^{-2} respectively at 500°C.

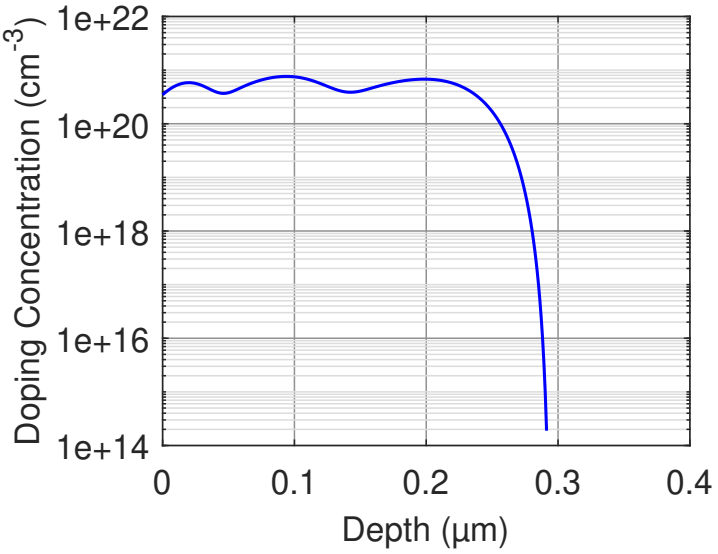


Figure 4.8. Carbon implantation profile for lifetime enhancement.

Once the implantation was done, the samples were cleaned in aqua regia and Piranha to remove unwanted contaminants like metals and organics, etc. The screening oxide was stripped by soaking in BOE for 5 minutes. A carbon cap was then formed by the pyrolization of a photoresist layer. All four samples were spin-coated with AZ1518 at 1000 rpm for 40 sec to produce a 4 μm thick film. They were then baked on a hot plate for a range of temperatures 90 - 150°C in a step of 10°C. The samples were placed in the Blue M furnace tube for 20 minutes in an Ar ambient at 675°C to form a carbon cap layer. A high temperature implant anneal and carbon drive in by diffusion was then performed in an Epigress VP-508 epitaxy system at 1600°C and improve the carrier lifetime by eliminating carbon vacancy sites in the lattice. After the anneal the carbon cap was stripped by oxidizing in an O_2 ambient in the Blue M for 1 hour at 900°C, followed by a soak in BOE for 5 minutes to strip any oxide that may have been formed. Since the implanted layer is expected to be amorphous by this high dose, about 1 μm was removed by reactive ion etching (RIE) using a Panasonic E620 with a recipe shown in appendix A.1. The surface was then oxidized for

10 hours in Protemp furnace tube # 7 to grow a 30 nm sacrificial oxide. Finally, the oxide was stripped by soaking in BOE for 5 minutes.

4.3.2 Nitrogen implantation for JFET and CSL

The dimensions and doping of the JFET region are very critical for both on- and off-state performances. A thin, moderately doped n layer below the p-well is also necessary to boost on-state performance. This layer is called the carrier storage layer (CSL) in an IGBT, but is also typically used in power MOSFETs as a current spreading layer. We expect about $0.3 \sim 0.4$ μm thick CSL layer below the p-well based on TCAD simulations. At first, the sample was oxidized in Protemp furnace tube # 4 for 3 hours at 1100°C in a wet condition to grow a thin layer (~ 30 nm) of screening oxide to protect the surface from contamination during subsequent ion implantation steps. A control SiC sample accompanied the original sample, and we performed step height measurements using a KLA Tencor P7 profilometer after patterning the oxide and found about ~ 17 nm of oxide. Therefore, the oxide was stripped in BOE for 2 minutes and re-oxidized for 6 hours. We deposited about 3.3 μm thick polysilicon layer using LPCVD in Protemp furnace tube # 6. The deposition was carried out for 230 minutes at 630°C. A photoresist (PR) mask was produced by photolithography using AZ1518 and a mask aligner (MA6) to pattern the polysilicon layer. Finally an STS-ASE tool was used to etch the polysilicon layer using a Bosch process[47] in which the etching is performed by an SF_6 ambient, and vertical sidewalls are maintained by depositing a polymer layer of C_4F_8 in alternate cycles. The sample was etched in 4 steps (3 minutes, 2 minutes, 2 minute and 1 minute), and after each etch the step heights were measured using a Bruker GT-K profilometer. After stripping the photoresist in remover PG, the polysilicon was measured to be about 3.32 μm thick. The etch rate during first 3 minutes was about 700 nm/min, while during the second etch it was reduced to 540 nm/min. The PR mask was stripped in remover PG, and the sample was shipped to CuttingEdge Ions for nitrogen implantation with eight different energies at 500°C and at room temperature for 760 keV. The expected retrograde doping profile shown in Fig. 4.9 formed the JFET and CSL layers. The net dose was calculated to be $3.76 \times 10^{12}\,\mathrm{cm}^{-2}$, with a CSL-Drift junction depth of 1 μm.

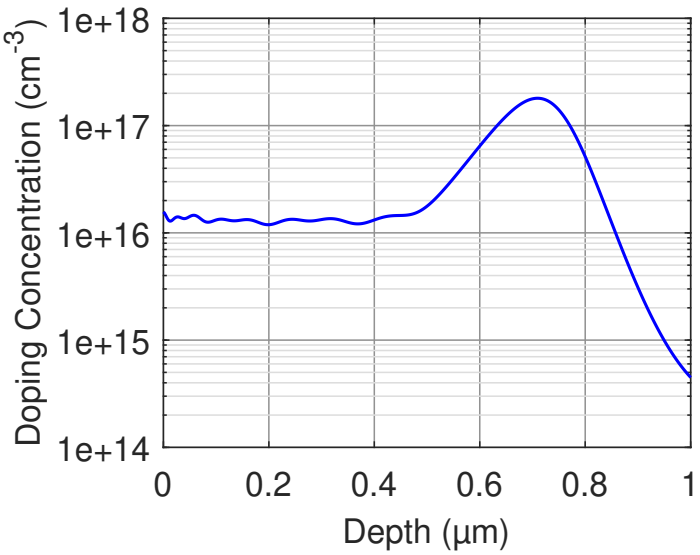
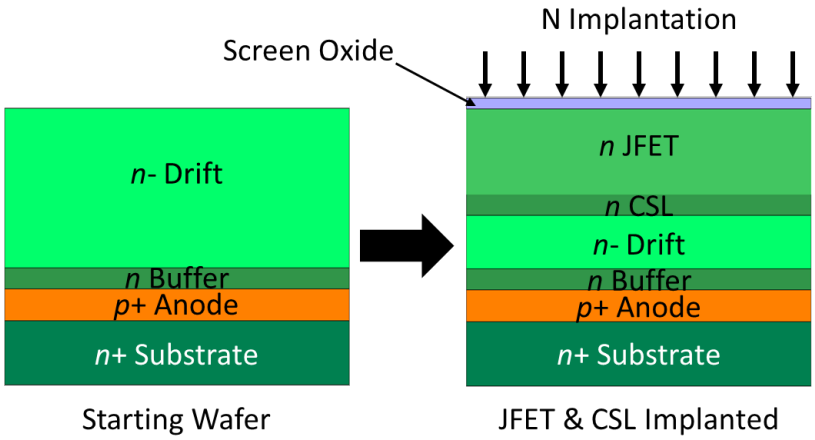
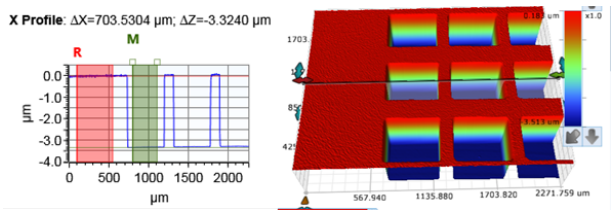


Figure 4.9. Retrograde nitrogen implantation profile to form the JFET and CSL layers.



(a)



(b)

Figure 4.10. (a) Cross section (not drawn to the scale) of JFET and CSL implantation process with polysilicon mask (not visible in this section) (b) Bruker profilometry image of as fabricated polysilicon mask of height 3.32 µm.

We predicted the nitrogen and aluminum doping profiles in 4H-SiC for all the processes in this work using the analytical model described in [48], which were also experimentally verified by our group [49]. The process cross section and the as-fabricated polysilicon mask are shown in Figures 4.10(a) and 4.10(b) respectively, indicating the mask thickness is 3.32 μm. The entire process is described in detail in appendix A.2.

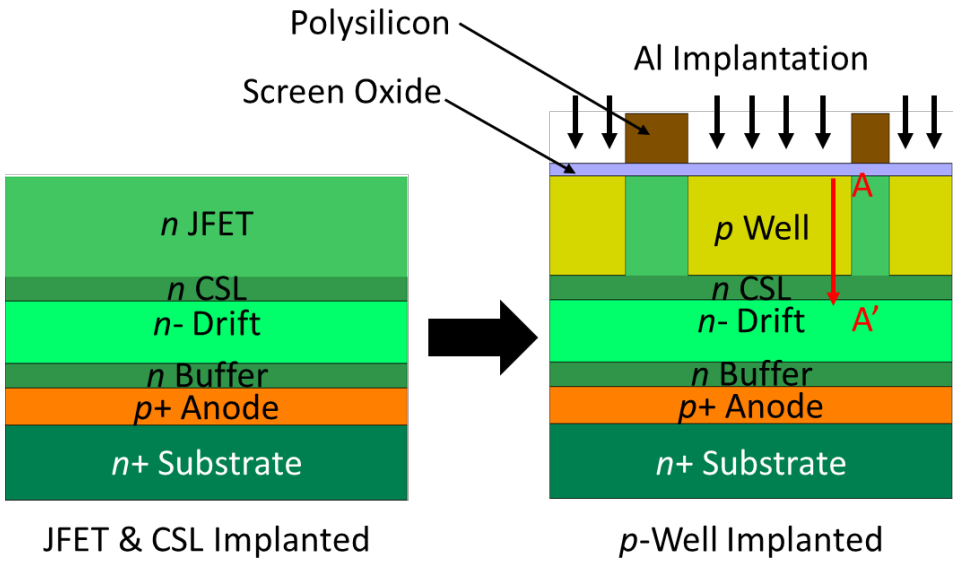
4.3.3 Alignment mark etch for *p*-well implantation mask

Once the CSL and JFET regions are formed by ion implantation it is necessary to align the *p*-well implantation with them. This was achieved by etching alignment marks in the SiC substrate. The alignment mark mask was used to cover all areas with AZ9260 by photolithography except rectangular windows where '+' shaped polysilicon trenches and mesas existed from the previous step. Alignment mark crosses were produced by RIE etching of SiC using the polysilicon layer as a hard mask in a Panasonic E620. The etching was performed in two steps of 3-5 minutes each using SF_6 gas, so that about 1 μm trenches are formed. Afterwards the photoresist mask was stripped using remover PG and the residue was removed by Branson ashing. A standard post-implantation clean using aqua regia and piranha was also performed to remove possible metal contaminants from the ion implantation as described in Section 4.3.2. The polysilicon mask from the prior process was also stripped by soaking in a mixture of DI, HF and HNO_3 for about 5 minutes. Finally, the remaining screening oxide was stripped using BOE. The procedure is described in more detail in appendix A.3.

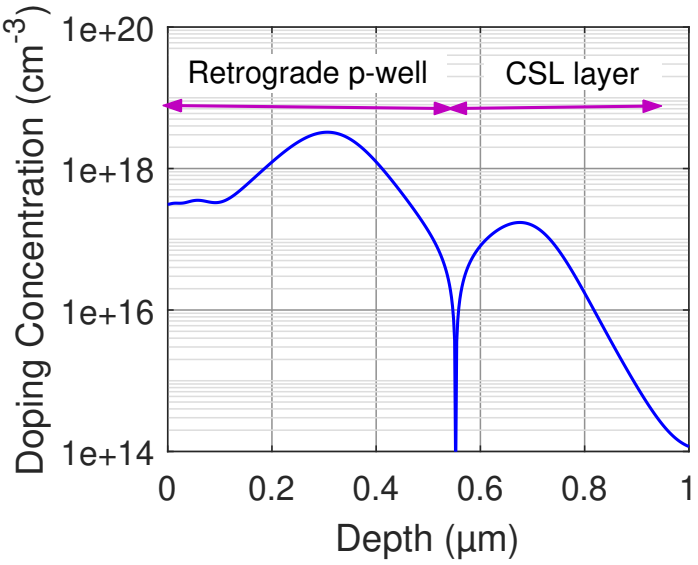
4.3.4 Aluminum implantation for *p*-well

The formation of the *p*-well is achieved by a four energy aluminum (Al) implantation with a maximum energy of 320 keV. The implantation was performed at CuttinEdge Ions at 500°C, and consists of a retrograde profile with a net dose of $6.44 \times 10^{13}\,\mathrm{cm}^{-2}$ and a junction depth of 552 nm as shown in Figure 4.11(b). This implantation scheme creates a channel doping of $\sim 3.11 \times 10^{17}\,\mathrm{cm}^{-3}$ and a 411 nm thick CSL beneath the *p*-well with a net dose $2.46 \times 10^{12}\,\mathrm{cm}^{-2}$. The retrograde profile ensures a sufficient dose beneath the source layer

to prevent the punch through in the blocking state, which will become clear in section 4.3.6 when source implant is added.

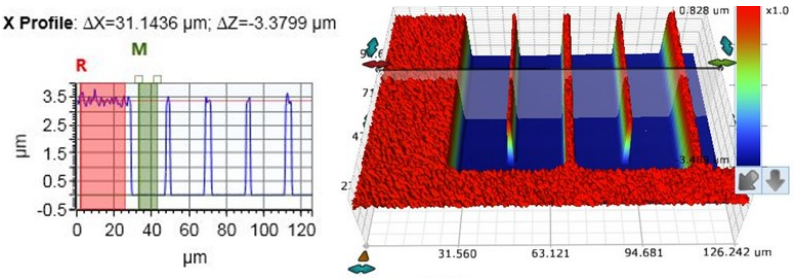


(a)

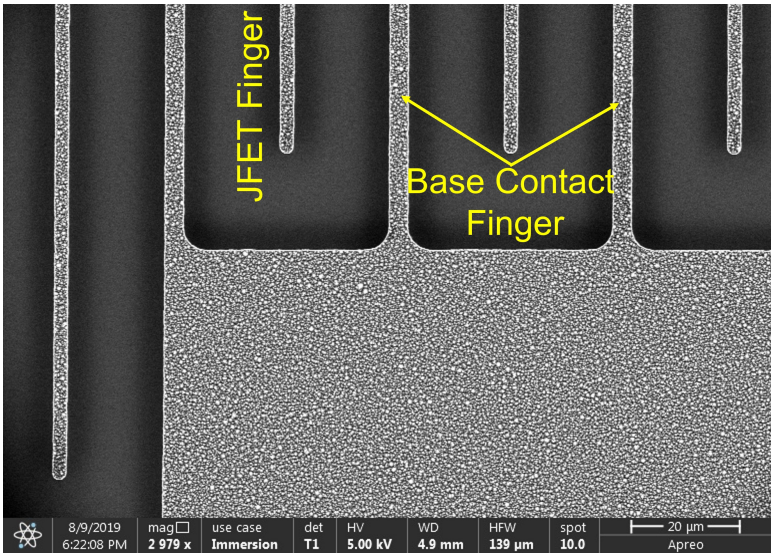


(b)

Figure 4.11. (a) Cross section of the *p*-well implantation using a polysilicon mask (b) Retrograde implantation profile to form the *p*-well, plotted along the line AA'.



(a)



(b)

Figure 4.12. Polysilicon *p*-well implantation mask as fabricated (a) Bruker image (b) SEM image.

The base implantation process is depicted by a cross section shown in Fig. 4.11(a). This process was begun by growing a thin screening oxide layer by thermal oxidation in Protemp furnace tube # 4. The oxidation was performed for 6 hours after going through standard solvent and RCA cleaning processes. A control sample accompanied the IGBT samples during the oxidation process, with which we measured about 30 nm of oxide using a P7 profilometer after patterning it by wet etching in BOE. Afterwards we deposited a polysilicon layer as an implantation mask by LPCVD in Protemp furnace tube # 6 for 230 minutes at 630°C. We created a photoresist mask using AZ1518, the *p*-well mask (# 3), and the MA6 mask aligner for the samples PU435Q2, PU436Q2, and the Heidelberg MLA150 for

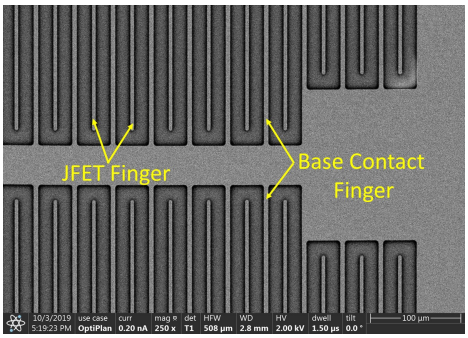
samples PU435Q3 and PU436Q3 to pattern the polysilicon mask. In case of the MA6 process, we observed about 2-3 μm misalignment in the x and y directions, which is within the design rules and not critical for this step. The polysilicon layer was etched using a Bosch process in an STS-ASE in two steps, first for 4 minutes and then for 1 minute. We measured the resulting step height in the Bruker profilometer to be about 3.4 μm as shown in Fig. 4.12(a), which is sufficient to block the highest energy Al implantation as verified by a TRIM simulation. The samples were shipped to CuttingEdge Ions for ion implantation after stripping the photoresist in remover PG. The JFET and base contact implantation windows were defined by this mask as shown in Fig. 4.12(b). The more detailed process as executed can be reviewed in the run sheet in appendix A.4.

4.3.5 Alignment mark etch

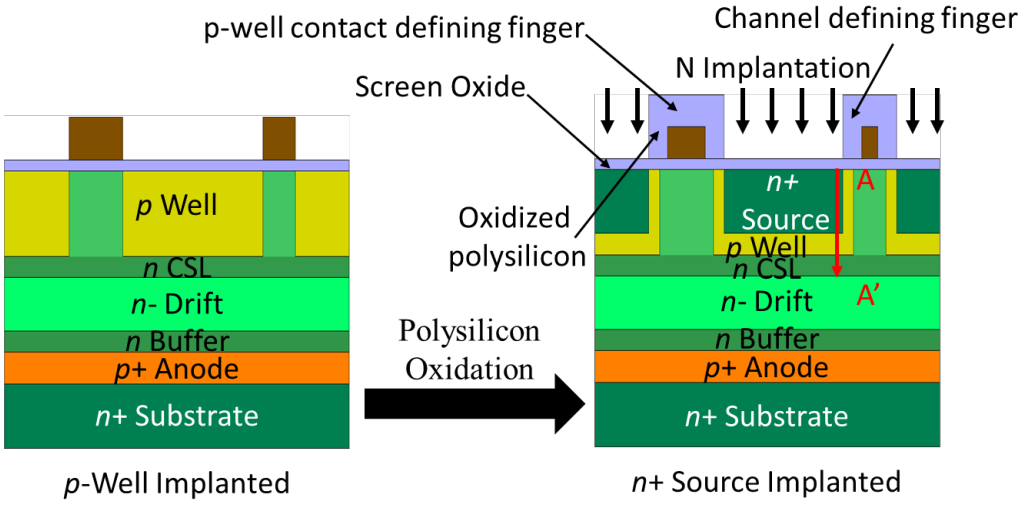
Alignment marks created within the p-well layer are used as a reference for all the top side processes except the ILD etch for the gate contact and the top ohmic metal contact, which are aligned to the polysilicon gate layer. The p-well implantation mask includes '+' shaped polysilicon marks along with the corresponding mask layer number. Therefore, in this process step we performed photolithography using AZ9260 resist, the alignment mark # 2 mask, and a Heidelberg MLA150 to open a rectangular window such that all the features are covered by photoresist except the alignment marks. We utilized a Panasonic E620 to etch SiC using SF_6 gas for 8 minutes in three steps (3 minutes, 3 minutes, and 2 minutes) in case of PU435Q2, while with a single step for other three samples. We mounted 1 cm×1 cm SiC control samples with a PR pattern on the carrier wafer along with the actual sample to estimate the etch rate and found it to be about 140 nm/min. Therefore, the alignment marks became SiC mesas about 1-1.1 μm in height. Finally, the photoresist mask was stripped using remover PG and Branson ashing to remove any residue. The process is outlined in more detail in appendix A.5.

4.3.6 Nitrogen implantation for self aligned $n+$ source

The self-aligned source implantation process was first proposed in [50] as process which ensures a uniform channel length across the sample. At this point the sample still had the polysilicon p-well implantation mask in place. The sample was cleaned using standard solvents and piranha. Then it was oxidized in Protemp furnace tube # 4 for 225 minutes at 1100°C. It should be noted that RCA cleaning process was not executed to protect the screening oxide. However, about 44% of the polysilicon is consumed during wet oxidation, and the pattern expands both laterally and vertically [51].



(a)



(b)

Figure 4.13. (a) Partial view of the source implantation mask (b) Process cross section for $n+$ source formation by ion implantation using oxidized polysilicon layer as a self-aligned mask.

Figure 4.13(a) shows a partial view of the source implantation mask captured by a Thermo Scientific Apreo SEM tool after the polysilicon oxidation. In this figure, the alternating fingers of oxidized polysilicon define both the channel and p-well contact regions by blocking nitrogen implantation. After completing the oxidation, the samples were sent to CuttingEdge Ions for six nitrogen implantations at 500°C with a maximum energy of 140 keV. The detailed implantation schedule is shown in appendix A.6 (2). The process cross section in Fig. 4.13(b) shows the MOSFET channels, which lie between the edges of the $n+$ source and p-well. A similar region is formed in an adjacent area which provides an overlap between the subsequent $p+$ implantation and the surface of the p-well as is discussed in Section 4.3.7. The net doping profile along the line AA' of the cross section is shown in Fig. 4.14. The expected thickness of the source, p-well, and CSL are 222 nm, 274 nm, and 411 nm respectively, with doses $4.86 \times 10^{14}\,\mathrm{cm}^{-2}$, $3.13 \times 10^{13}\,\mathrm{cm}^{-2}$ and $2.46 \times 10^{12}\,\mathrm{cm}^{-2}$. The sample was then post-implantation cleaned using aqua regia and piranha. Finally, the oxide and polysilicon masks were stripped by wet chemistry using HF, HNO_3 and BOE as described in appendix A.6.

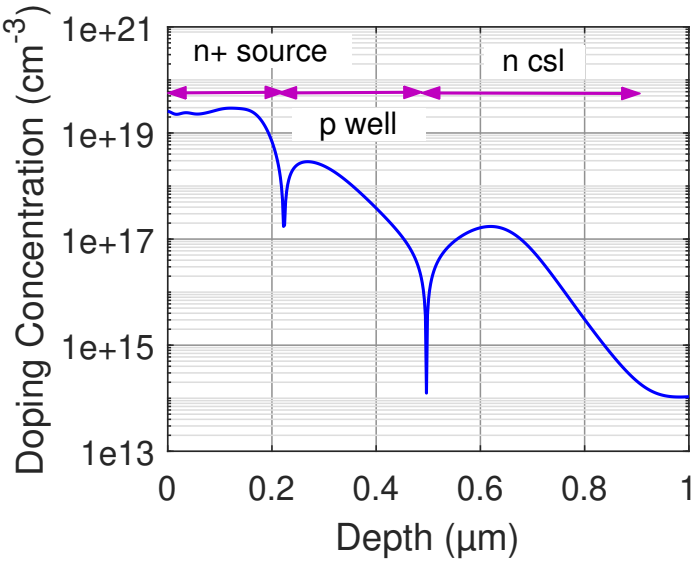
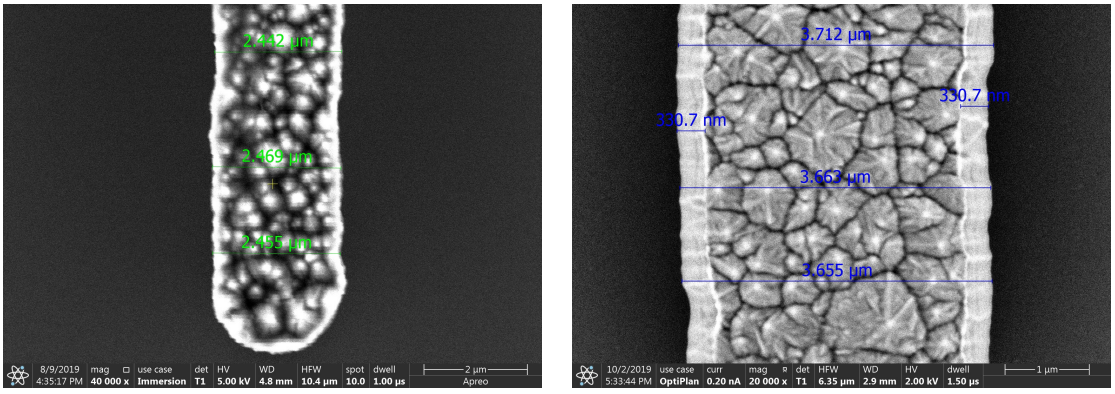


Figure 4.14. Net doping profile along the line AA' of the cross section.



(a) (b)

Figure 4.15. (a) Polysilicon *p*-well implantation mask defining the JFET fingers prior to oxidation (b) Ssource implantation mask after polysilicon oxidation. The lateral expansion of the mask defines the MOSFET channel.

Figures 4.15(a) and 4.15(b) show the polysilicon *p*-well implant mask along a JFET finger of a type A medium sized device before and after polysilicon oxidation. The estimated channel length after source implantation can be estimated from the difference between the widths of the expanded and original masks, and is found to be about 610 nm.

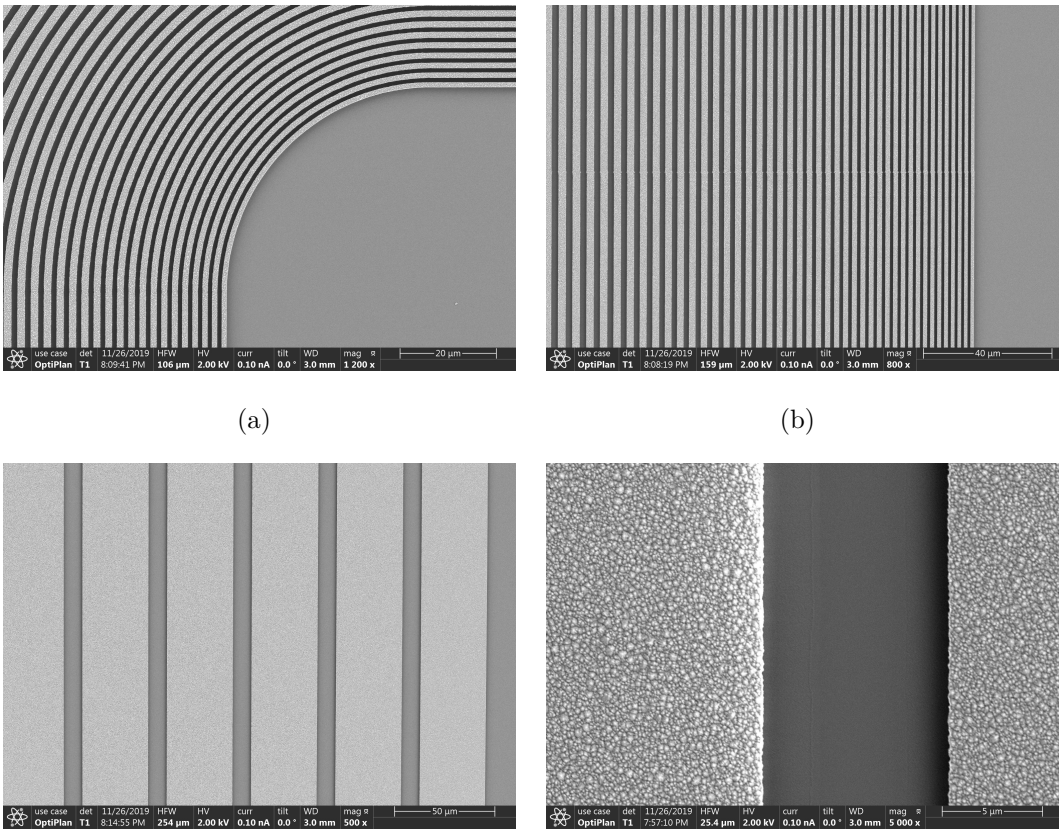
We measured the expansion of many devices all over the sample using SEM images, and listed the average JFET and channel lengths in Table 4.4 for three samples. The data from PU436Q3 was excluded as it was damaged in the next step of the processing. It is notable that JFET length of samples PU435Q2 and PU436Q2 has shrunk significantly from the original drawn dimensions, while the channel length was in the range 540-682 nm.

Table 4.4. JFET and channel lengths as defined by the base and source implant masks

Sample ID	**Device Type**	**Designed JFET Width (µm)**	**Fabricated JFET Width (µm)**	**Fabricated Channel Length (nm)**
PU435Q2	Large B	3.00	1.98	595
PU435Q2	Medium A	3.00	2.04	575
PU435Q2	Medium B	3.00	2.05	540
PU435Q2	Medium C	5.00	4.20	623
PU435Q2	Small A	3.00	1.83	555
PU435Q2	Small B	3.00	1.85	575
PU435Q2	Small C	5.00	4.14	595
PU435Q3	Large B	3.00	2.50	592
PU435Q3	Medium A	3.00	2.54	560
PU435Q3	Medium B	3.00	2.52	570
PU435Q3	Medium C	5.00	4.45	671
PU435Q3	Small A	3.00	2.47	585
PU435Q3	Small B	3.00	2.47	597
PU435Q3	Small C	5.00	4.32	682
PU436Q2	Large B	3.00	1.94	550
PU436Q2	Medium A	3.00	2.00	540
PU436Q2	Medium B	3.00	2.01	563
PU436Q2	Medium C	5.00	4.08	598
PU436Q2	Small A	3.00	2.06	575
PU436Q2	Small B	3.00	2.16	575
PU436Q2	Small C	5.00	4.05	580

4.3.7 Aluminum implantation for $p+$ base contact

In this step, a high dose of Al is implanted to make better electrical contact to the p-well. This will also form the floating field ring edge termination. Once again the sample went through a standard solvent clean, and an RCA clean in a dedicated RCA hood. The sample is then oxidized in Protemp furnace tube # 4 for 6 hours at 1100°C. We measured 36 nm of oxide in one of the SiC control samples which accompanied the IGBT sample in the furnace.



(a) (b)

(c) (d)

Figure 4.16. (a) Polysilicon mask that defines the FFR edge termination by Al implantation in (a) a device corner (b) on the side of a device (c) base contact implantation window (d) Magnified view of (c).

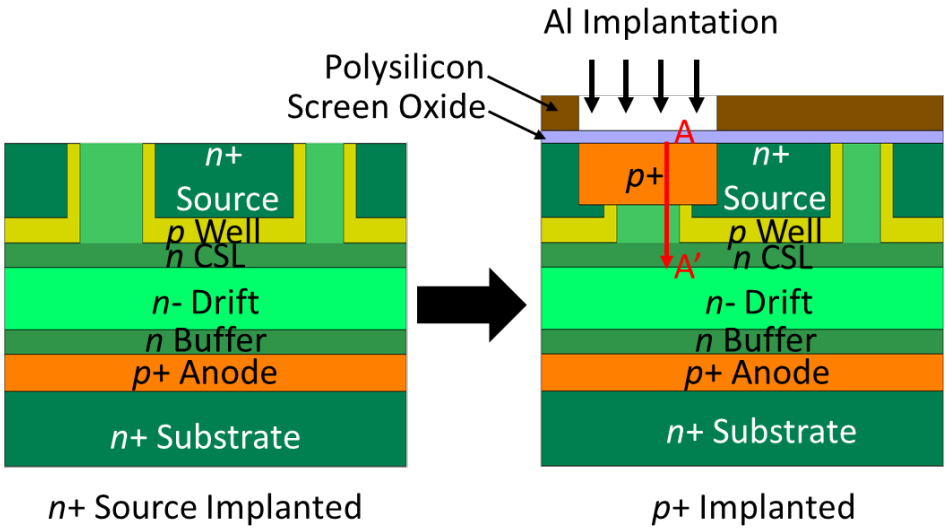
After completing the oxidation, the sample was transferred to Protemp furnace tube # 6 to deposit a 1.5 µm polysilicon layer for 120 minutes at 630°C. Due to the small dimensions and high accuracy required, e-beam lithography was used in order to achieve the 1 µm

minimum feature sizes required for the floating field rings. We performed a series of dose tests using CSAR e-beam resist on test samples, and found 280 mJ/cm^2 as an optimum dose. This step is very critical for the IGBT because the base contact carries a significant amount of current in the on-state, unlike in a MOSFET. Also, precise floating field ring spacings are required to achieve the target blocking voltage in the off-state. It is important to note that the CSAR resist should be kept out of the refrigerator for at least one hour before the lithography process begins. After completing the lithography, we etched the polysilicon by Bosch process in STS-ASE for 2.5 minutes and stripped the CSAR using remover PG. The CSAR thickness was measured to be 343 nm using a P7 profilometer, which is sufficient for etching the polysilicon. The polysilicon mask as fabricated is depicted in Fig. 4.16 as taken in the Apreo SEM.

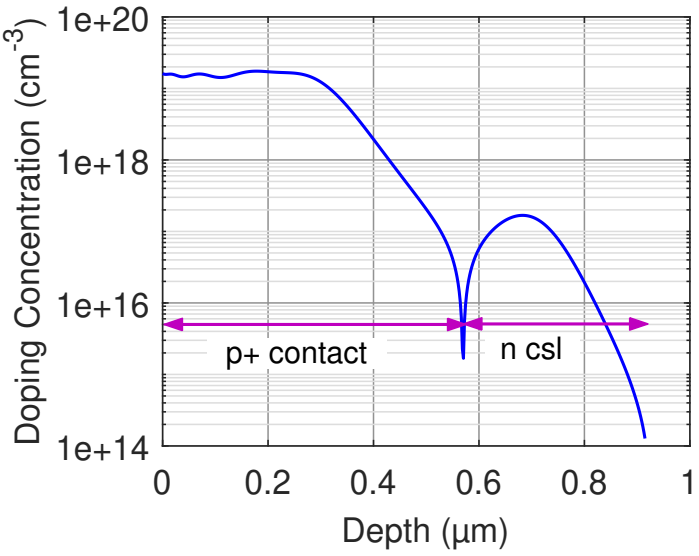
The sample was sent to CuttingEdge Ions for a five energy Al implantation schedule at 500°C with a maximum energy 270 keV. The process cross section and the net doping profile are shown in Fig. 4.17. The estimated junction depth of the base contact/CSL layer is 568 nm and the net implanted dose is $5.41 \times 10^{14}\,\mathrm{cm}^{-2}$ whereas the first 316 nm has a box doping profile of 1.5×10^{19} cm^{-3}.

As all the ion implantation processes were completed at this point, the next step was to activate the dopants. Once again a standard post-implantation clean followed by stripping of the polysilicon mask and screening oxide were completed. The sample was spin-coated with a 4 μm thick AZ1518 followed by carbonization at high temperature in the Blue M furnace to form a carbon cap layer required for the high temperature implant activation anneal. All three samples were loaded into the Epigress system, and the temperature ramped up step by step to achieve 1700°C at a pressure of 404 mbar. To maintain temperature ramp stability, above 1650°C the temperature was stepped slowly by 10-15°C per step until stabilized at 1698°C. The steady state temperature was maintained for 20 minutes, then cooled to room temperature overnight. The carbon cap was removed by oxidizing the cap in the Blue M tube as previously described in Section 4.3.1. In order to remove any other contaminants on the surface from previous processes and improve the surface roughness we oxidized the samples in Protemp furnace tube # 4 for 2.5 hours to have about 12-15 nm sacrificial oxide.

Finally, the oxide was stripped in BOE. The process detail is described with greater detail in appendix A.7.



(a)

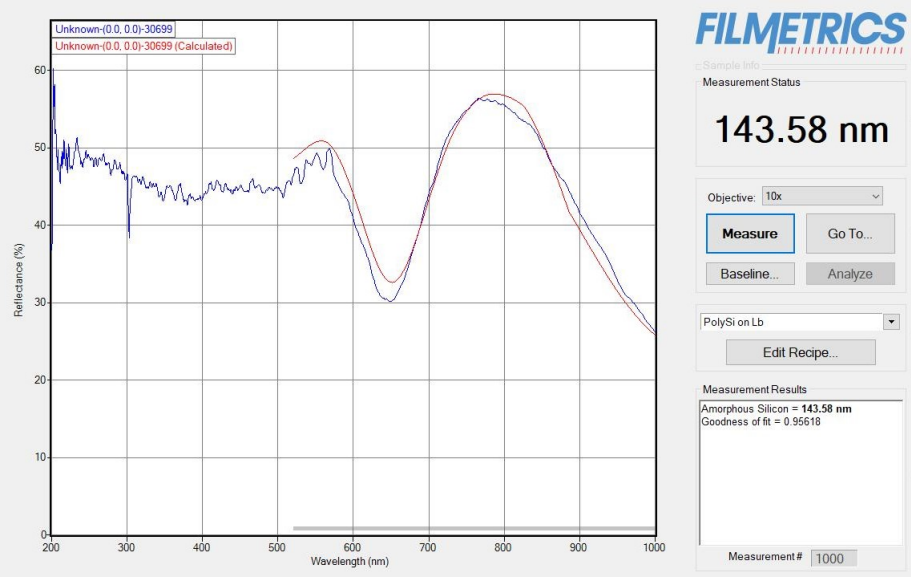


(b)

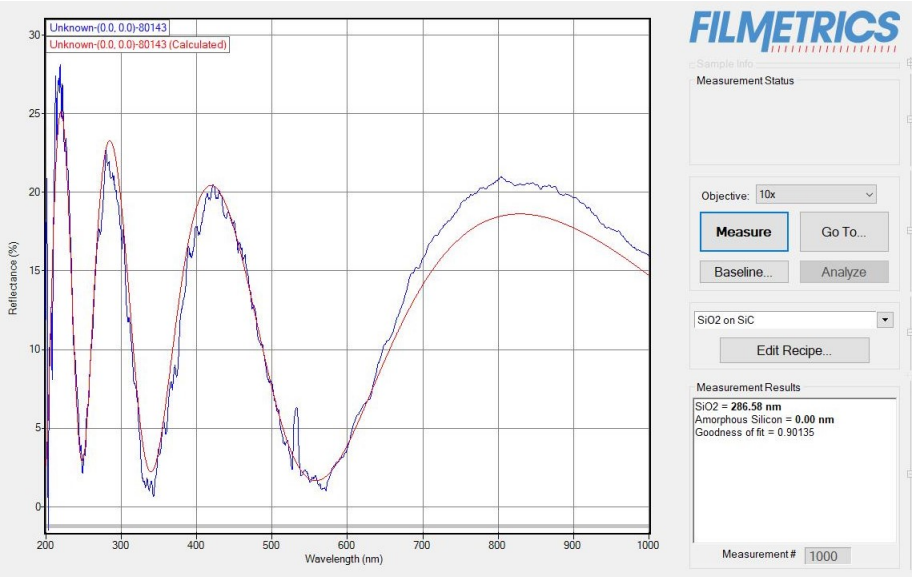
Figure 4.17. (a) Cross sections of the $p+$ base contact implantation process with a polysilicon mask. $p+$ depth is shown shallower than the $n+$ implant to show the overlap with $n+$ source (b) Net doping profile along the line AA' (actual $p+$ implant is deeper than the $n+$ source).

4.3.8 Field oxide deposition

It is a common practice to protect the silicon carbide surface with field oxide where no metallization is required. The gate probe pad is also fabricated on top of this oxide.



(a)



(b)

Figure 4.18. Measured thickness of (a) amorphous silicon (b) field oxide by the Filmetrics F40.

The samples were cleaned in piranha and polysilicon was deposited by LPCVD in Protemp furnace tube # 6 for 45 minutes at 580°C. At this temperature the deposited layer is actually expected to be amorphous silicon whose surface is smoother than polysilicon deposited at higher temperatures. The samples were cleaned through the standard solvent and RCA cleaning processes and oxidized in Protemp furnace tube # 4 for 60 minutes to oxidize the amorphous silicon layer completely. The thickness of the amorphous silicon and oxide layers were measured using the Filmetrics F40 and found to be 144 nm and 286 nm respectively, as shown in Fig. 4.18.

The thickness of the field oxide was intentionally kept low in order to avoid patterning problems during wet chemical etching[52]. We performed a careful solvent cleaning in Acetone and IPA prior, followed by photolithography using AZ1518 resist, FOX mask(# 6) and the Heidelberg MLA150. We used adhesion promoter HMDS and a dose of 185 mJ/cm^2. The oxide was patterned by wet chemical etching in BOE for 7 minutes. Finally, the photoresist mask was stripped in remover PG. The process detail is presented in the appendix A.8.

4.3.9 Gate and inter layer dielectric (ILD) formation

Formation of the gate oxide is one of the most critical steps and requires significant attention to cleanliness. The samples went through a standard solvent and RCA cleaning processes with a shorter 20 sec BOE dip instead of 1 minute to retain the field oxide as much as possible. The samples were loaded in the cleanest Protemp oxidation tube # 1 to avoid contamination as this would become the gate oxide. The oxidation recipe consists of sequence of dry and wet oxidations at different temperatures and durations as described in appendix A.9. A series of dry and wet oxidation was performed as described in appendix A.9. We measured oxide thickness in one of the control SiC samples to be 34-40 nm using the Filmetrics F40. The samples were then transferred to the cleanest tube in the cleanroom for the NO anneal, which is very crucial to minimize the D_{IT} at the oxide-SiC interface[1]. The system was purged with Ar flow at room and low temperature. The temperature was increased and gas flow was changed to NO at 850°C. The target temperature was 1175°C. However, we started counting the time when the temperature reached at 1120°C. After about

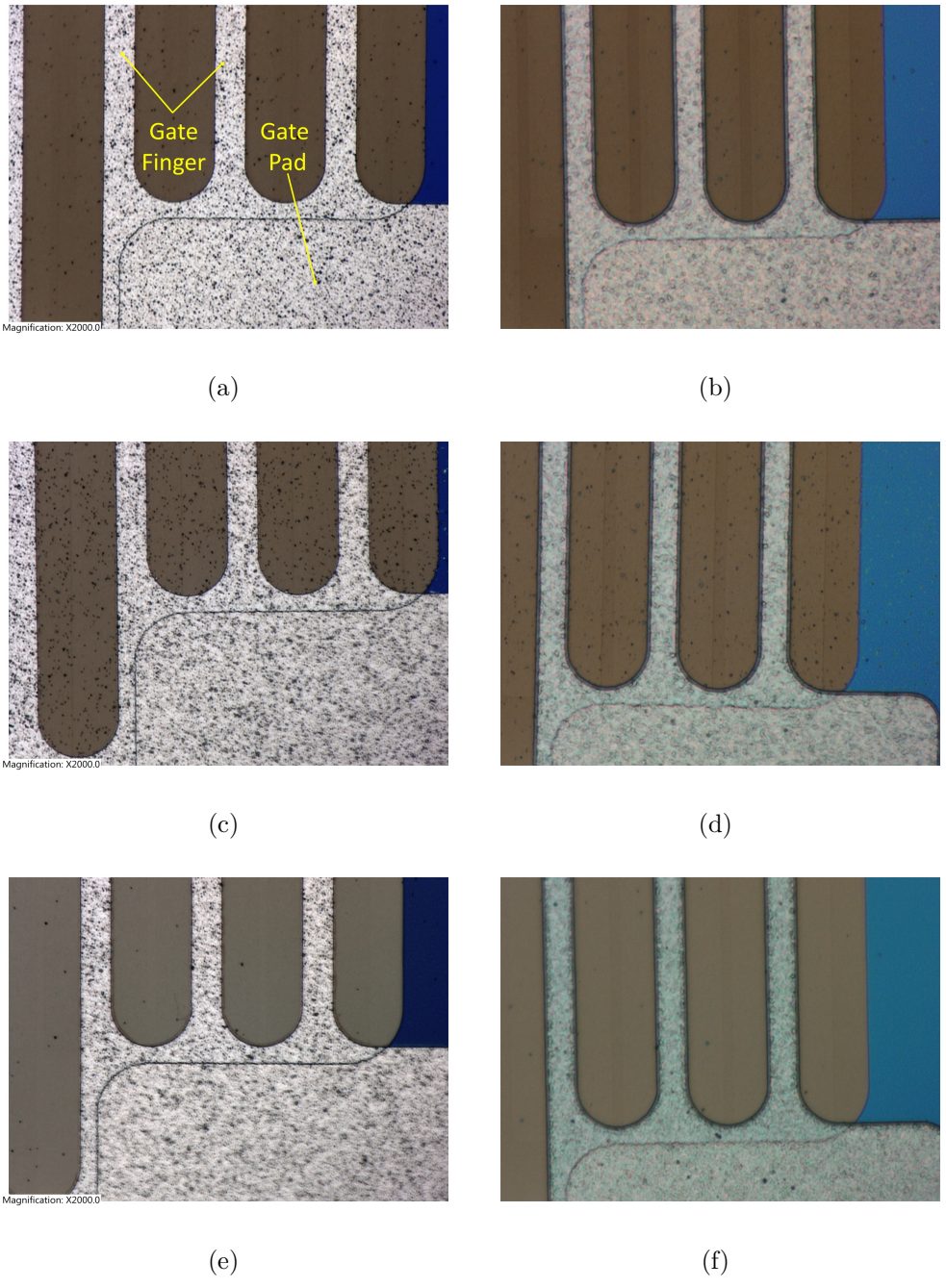
2.5 hours the temperature was ramped down step by step but we observed that NO flow was stopped at some point because the supply ran out. We decided to fabricate MOSCAPs in one of the control samples which had accompanied the actual samples. From high frequency C-V measurements on these MOSCAPs, the gate oxide thickness was estimated to be about 40 nm. The D_{IT} data extracted from high-low measurements did not indicated very high interface state density. Therefore, we decided to move on to the next steps in the process considering the timeline. We cleaned the samples with standard solvents and deposited gate polysilicon at 630°C for 80 minutes in Protemp furnace tube # 6.

The next important step is to dope the polysilicon layer with phosphorous in order to reduce the depletion width and effective oxide thickness. Phosphorous spin-on dopant P509, manufactured by Filmtronics, was spin-coated on the samples. The phosphorus dopant was then driven into the gate at 1000°C for 2 hours in Protemp furnace tube # 8 with 75% N_2 and 25% O_2 flow as per the manufacturer instructions. The dopant source must be kept out of the refrigerator for at least 2 hours for best results. The detailed procedure is outlined in appendix A.9. After completing the drive-in, the dopant layer was stripped by soaking in BOE for 5 minutes. We measured the resulting sheet resistance to be 6.737 Ω/□, 7.183 Ω/□ and 13.58 Ω/□ in PU435Q2, PU435Q3, and PU436Q2 respectively using a Jandel four-point probe tool.

Next, a polysilicon etch mask was formed by photolithography using AZ1518, the poly gate mask (# 7), and the Heidelberg MLA150. Once again polysilicon was etched using a Bosch process in the STS-ASE for 2 minutes, and photoresist was stripped in remover PG. Polysilicon gate fingers achieved through this process are shown in Fig. 4.19(a), 4.19(c) and 4.19(e). Some polysilicon residue was visible in the source region, especially for PU435Q3, which may cause high contact resistivity. A full view of a large device with annotated polysilicon gate pad and runners is shown in Fig. 4.20. Ohmic contacts to the gate will be made in these locations, as will be discussed in Section 4.3.12.1. Medium and large devices have the same design structure, whereas small devices have only a large gate pad as noted in Fig. 4.26(b).

The samples were again oxidized after solvent and piranha cleans in Protemp furnace tube # 4 for 225 minutes at 1100°C. This step ensures that the interlayer dielectric adequately

separates the gate metal contact from other contacts. Figure 4.19(b), 4.19(d) and 4.19(f) indicates that after oxidation the polysilicon residues in the source region were improved.



(a) (b)

(c) (d)

(e) (f)

Figure 4.19. Polysilicon gate fingers of (a) PU435Q2, (c) PU435Q3, and (e) PU436Q2, and the same areas after ILD growth in (b) PU435Q2, (d) PU435Q3, and (f) PU436Q2.

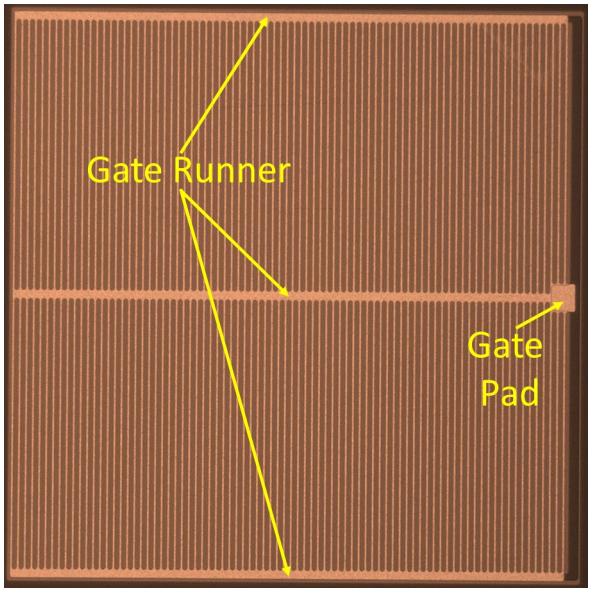


Figure 4.20. Full view of a large device with polysilicon gate and runners noted

The cross sections of the gate stack and ILD formation process are shown in Fig. 4.21. The accurate measurement of ILD thickness is very important to estimate the remaining polysilicon thickness because the RIE etching process of the ILD layer to create gate contact windows also etches polysilicon. We utilized a silicon test sample which accompanied the actual samples during the gate oxidation, gate polysilicon deposition and the ILD formation processes. A cross section of this sample created by the focused ion beam (FIB) technique and imaged using Thermo Scientific Helios G4 UX Dual Beam system is shown in Fig. 4.22(a). The measured thicknesses of the polysilicon and ILD layers were 461.7 nm and 941.4 nm respectively. The IGBT sample, shown in Fig. 4.22(b), had a gate oxide thickness of about 40 nm in Region-1, and we measured the thickness of the polysilicon fingers by step height measurements using a P7 profilometer. Let us consider the Region-1 surface as a reference level for the step height measurement. The material stack is somewhat complicated because the oxidation rate of Si and SiC are significantly different. After polysilicon oxidation, the gate pad and fingers of Region-2 extended outward in every direction except underneath to form the ILD. We also measured the step height of the gate fingers after oxidation, but the reference surface of Region-1 is also elevated by the amount of oxide which grows during the 225 minutes oxidation. This is expected to be about 20 nm, for a total of 60 nm oxide in

Region-1 after ILD formation. Therefore, the gate finger step heights before and after the oxidation should be corrected by 20 nm to keep the reference level consistent. Finally, we estimated the ILD thickness considering the fact that the amount of polysilicon consumed during the wet oxidation is about 44% of the resulting oxide thickness. Table 4.5 presents the estimated thicknesses of the ILD and the remaining gate polysilicon.

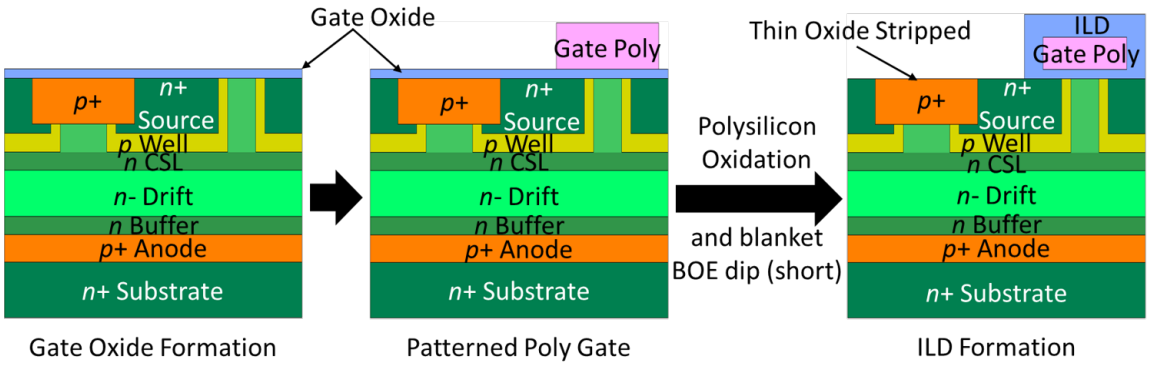
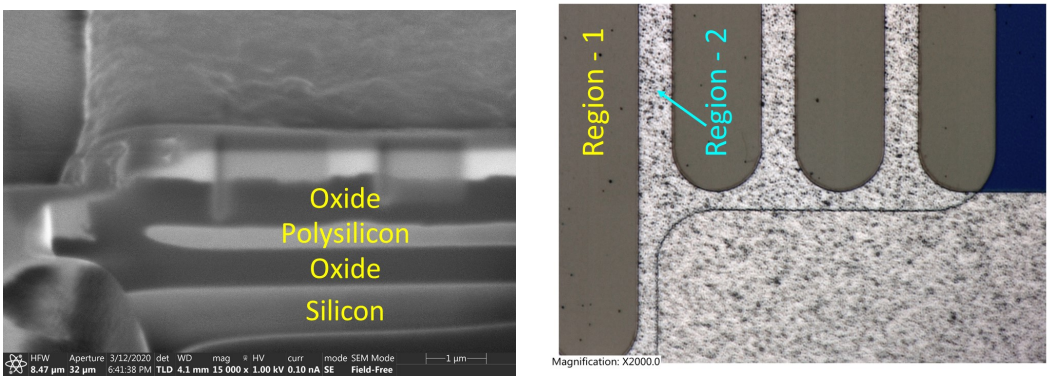


Figure 4.21. Gate oxide formation by thermal oxidation, gate polysilicon patterning by optical lithography, and ILD formation by thermal oxidation of polysilicon.



(a) (b)

Figure 4.22. Estimation of ILD thickness from (a) FIB cross section of a silicon test sample and (b) Step height measurements of IGBT sample.

Table 4.5. Estimation of ILD and remaining gate polysilicon thicknesses

Sample ID	**Polysilicon Finger Height Before Oxidation (nm)**	**Polysilicon Finger Height After Oxidation (nm)**	**Net Height Increment (nm)**	**ILD Thickness (nm)**	**Remaining Polysilicon (nm)**
PU435Q2	1051	1651	620	1107	564
PU435Q3	1097	1689	612	1093	616
PU436Q2	1060	1617	577	1030	607

4.3.10 Base contact metallization

After the gate formation process was completed, the samples were ready for top metal contacts. The first step was to deposit proper $p+$ contact metals in order to ensure ohmic contacts to the p-well. The first task was to strip the oxide from the base and source contact regions. Therefore, we performed a blanket oxide etch in BOE for 75 sec to remove about 60 nm oxide. Using the Filmetrics tool we measured the oxide thickness in the field area of PU435Q2 and found it to be 302 nm before the BOE etch, and 194 nm after. This difference of greater than 100 nm ensures that sufficient oxide was removed. We treated the other two samples in the same way with similar results. Before proceeding with the IGBT samples we conducted a run with a test sample to validate the required metal stack (33 nm Ti and 167 nm Al) as reported in [53], [54] for p-type SiC. This sample was implanted with the same Al profile as the base contact region. However, we calibrated the metal deposition system (PVD1) using other test samples and found that deposited Ti and Al were 1.95 and 0.8 times the target thickness, but Ni was as expected. Using this calibration data we deposited a metal stack of 33 nm Ti, 167 nm Al, and 100 nm Ni to fabricate transfer length method (TLM) structures by lift-off lithography which will be discussed below. The contact was annealed at 1000°C for 2 minutes in a Jipelec Rapid Thermal Annealing (RTA) system which will be discussed in Section 4.3.11.2, and contact resistivity was measured to be $1.28 - 7.63 \times 10^{-3}$ Ωcm^2 with an average of 2.48×10^{-3} Ωcm^2. The TLM characterization technique will be discussed in chapter 5.

The IGBT samples were cleaned with standard solvents and lift-off lithography was performed using LOR3B, AZ1518, base contact mask (# 8) and the Heidelberg MLA150. Prior to metal deposition the samples were descummed in the Branson asher to remove any organics. The Jupiter II system was then used for a short SF_6 RIE to roughen the surface for better metal adhesion. Finally, they were again descummed in the Branson Asher to remove any possible polymer C_xF_y formed during the previous RIE step, followed by a 10 sec BOE dip to remove any thin oxide. Using the calibrated process we evaporated 33 nm Ti, 167 nm Al, and 20 nm Ni for a total of 220 nm. The metal lift-off was performed by soaking in remover PG overnight. We measured the thickness of the total metal stack using the P7 profilometer and found it to be 224 nm in PU435Q2. The results from the other two samples were also consistent. A schematic of the process cross section is shown in Fig. 4.23. Figure 4.24 shows all types of medium and small sized devices after completing the base contact metal. The process details are described in appendix A.10.

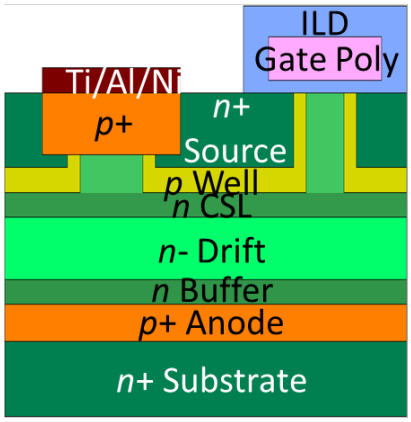


Figure 4.23. A schematic cross section of the base contact metallization process.

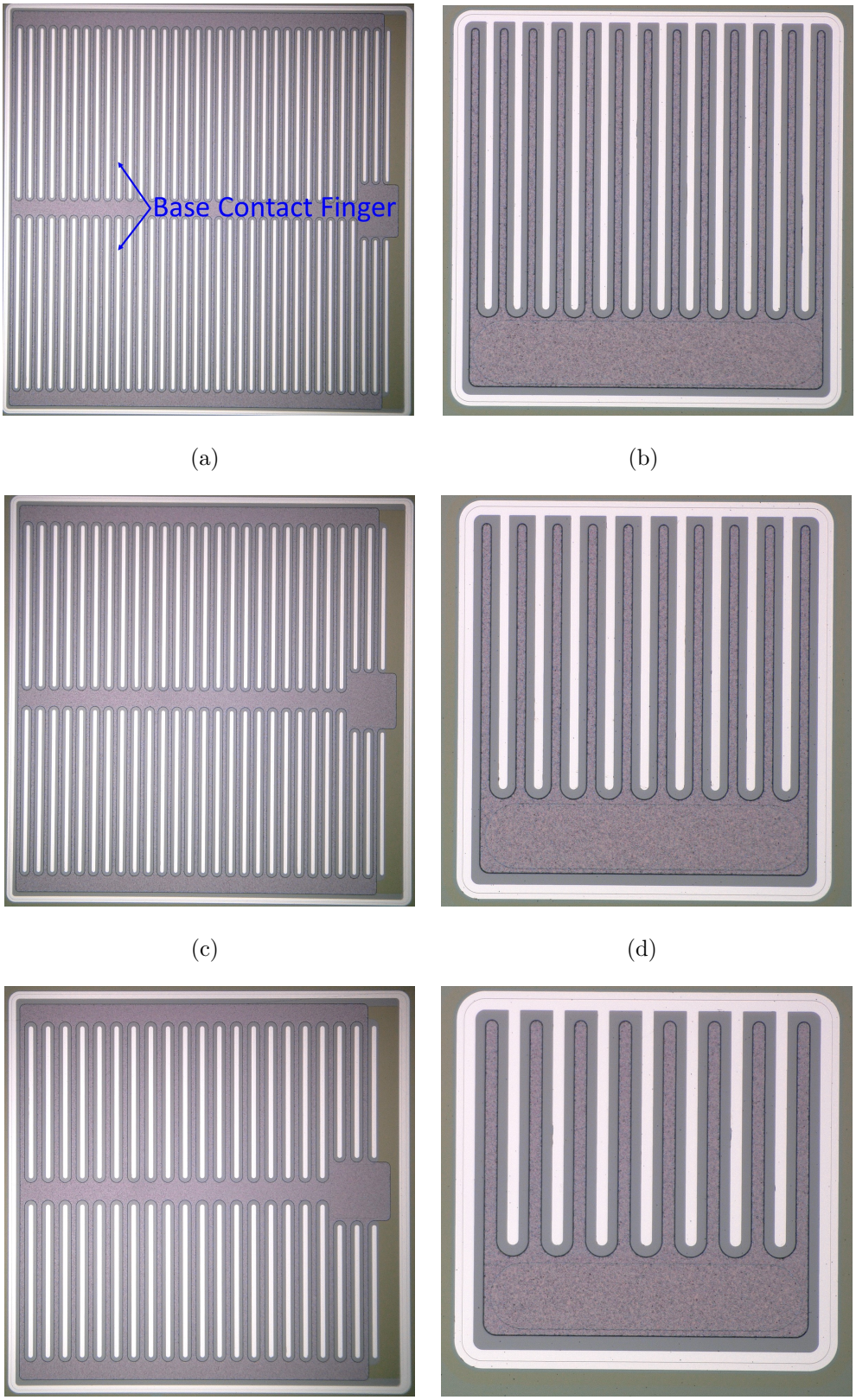


Figure 4.24. Base metal contact fingers in different devices (a) Medium A (b) Small A (c) Medium B (d) Small B (e) Medium C (f) Small C.

4.3.11 Ohmic contact

The ohmic contact process has two major steps: metallization, which creates a Schottky contact, and a high temperature anneal to create an ohmic contact with SiC. These two processes are discussed briefly in the following two subsections.

4.3.11.1 Ohmic metallization

Nickel is typically used as an ohmic metal for n-type contacts on SiC. We used the lift-off lithography technique to pattern the ohmic metal using the same recipe as discussed in Section 4.3.10. The same sequence and recipe of cleaning in the Branson, Jupiter II and BOE as the base contact metal process was followed again in this case. Finally, we evaporated 100 nm Ni in PVD1. Patterning of the metal by lift-off was done to open windows for the gate contact pad and gate runner in the active area and clear the metal from field area. Figure 4.25 presents a schematic cross section of the ohmic contact metallization process and images of all types of medium and small size devices after completion of the ohmic contact metal process are shown in Fig. 4.26. The process run sheet is available in appendix A.10.

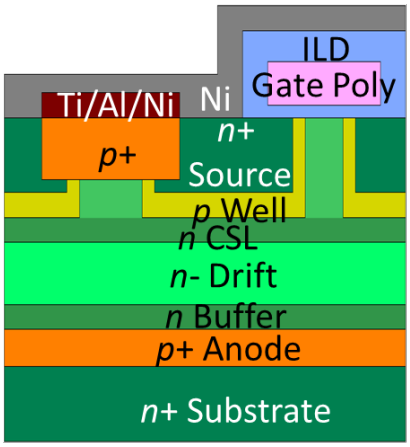


Figure 4.25. A schematic cross section of the ohmic contact metallization process

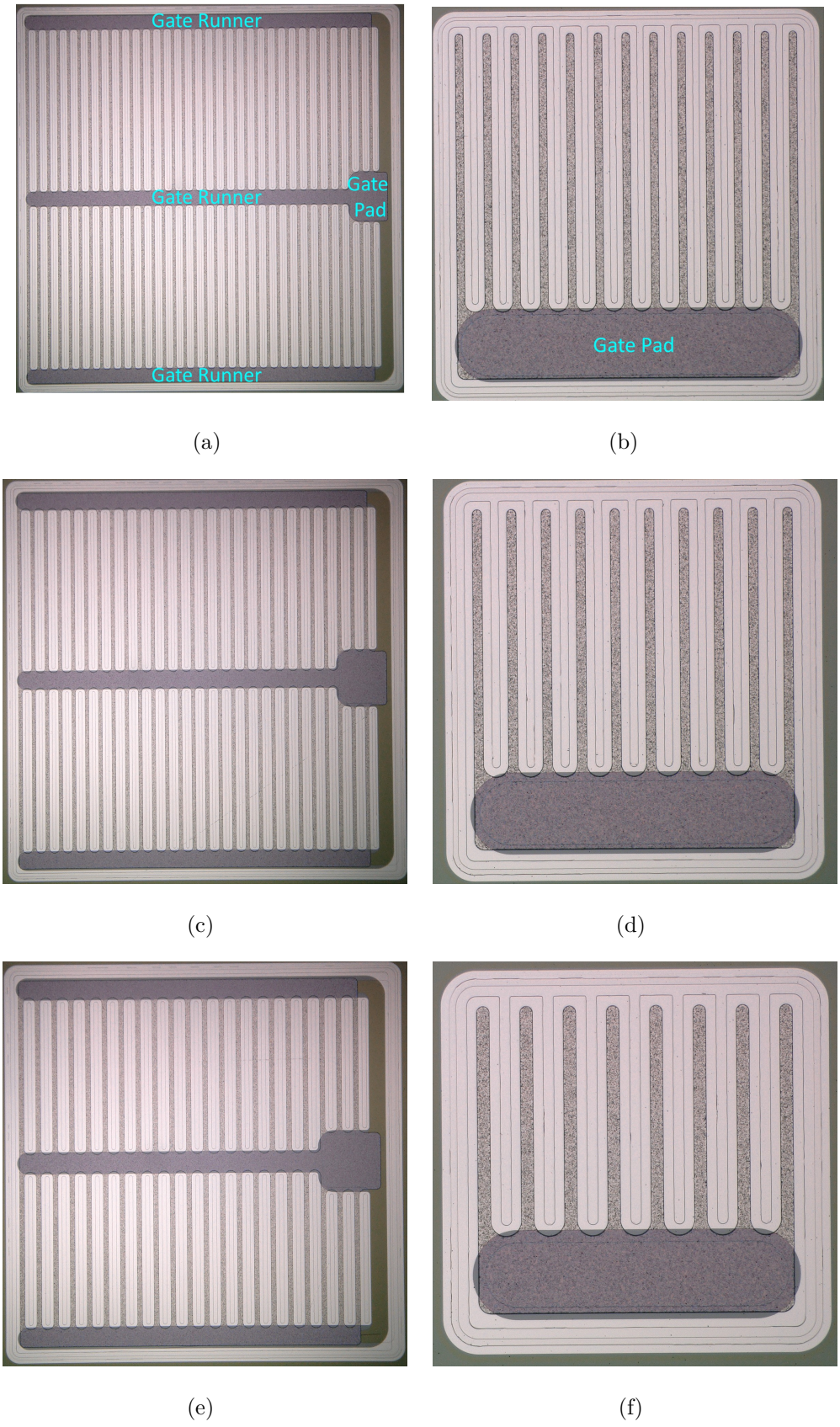
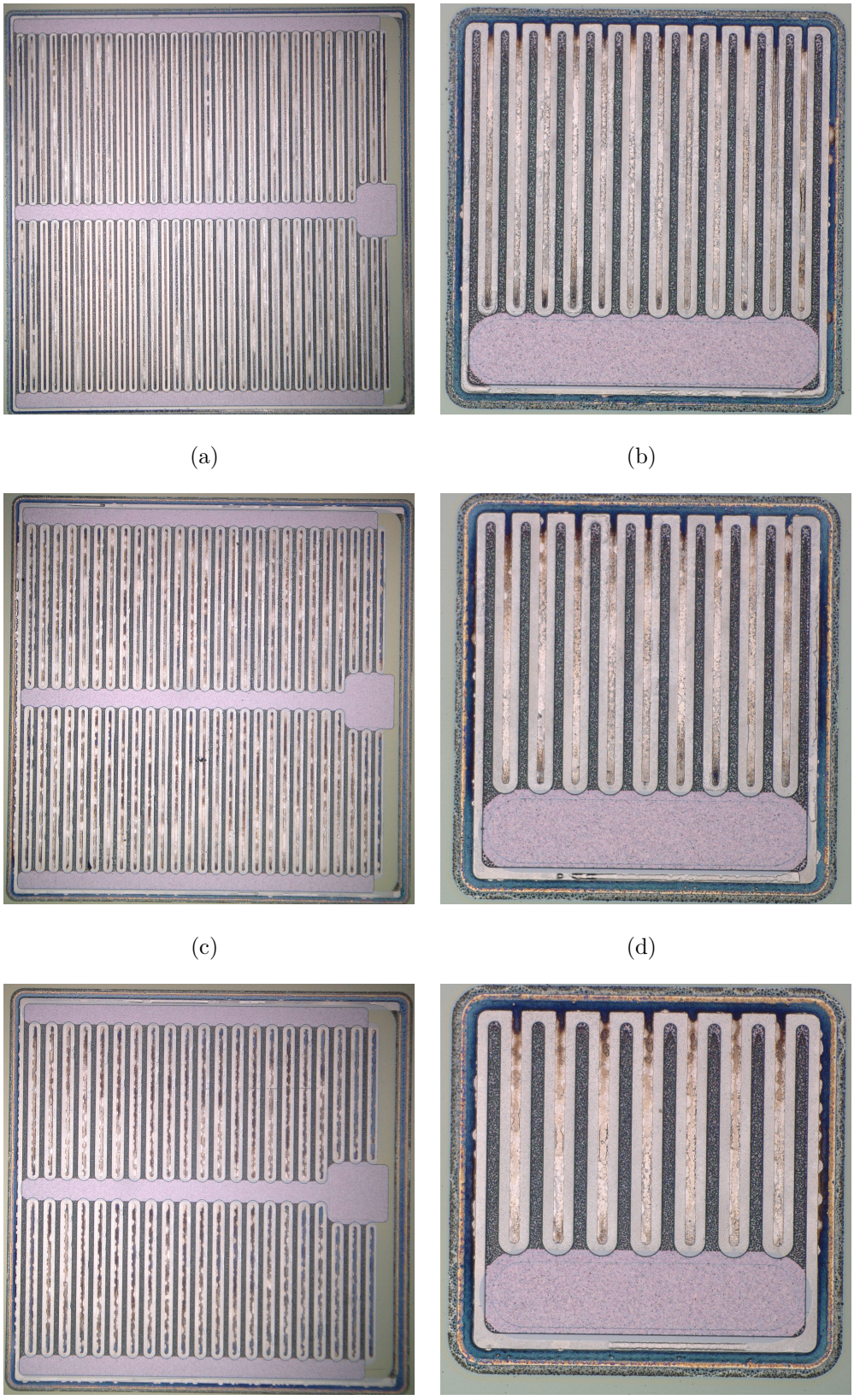


Figure 4.26. Various devices after completion of the ohmic contact metal process (a) Medium A (b) Small A (c) Medium B (d) Small B (e) Medium C (f) Small C.

4.3.11.2 Contact anneal

The contact anneal is a critical step because of its irreversible nature. Therefore, one sample was processed first and other two followed based on the success of the leading sample. Nickel is widely used in SiC ohmic contacts. The basic principle is to form a compound Ni_xSi_{1-x} at the metal-SiC interface and reduce the barrier height between the contact and the SiC substrate[55]. This is achieved by reacting Ni with SiC at high temperature.

In order to reduce the risk of contaminants, particularly oxygen, the process starts by purging the chamber with N_2 at 200°C and three purging sequences with Ar at temperatures 500°C, 500°C and 650°C. These four sequences have a duration of 30 minutes, 46 minutes, 45 minutes and 40 minutes. We then placed a clean quarter of a four inch oxidized Si carrier wafer on a six inch Si susceptor wafer. A dummy SiC sample with nickel TLM patterns and a dummy Si sample with a thin Ti layer were then placed on the carrier wafer. The carrier wafer was placed in the Jipelec RTA tool, and the contact anneal recipe was run, consisting of a 2 minute 1000°C in an Ar ambient. After cooling down, we observed to see if there was any blueish discolorization of the Ti film which could indicate the presence of O_2 during the anneal, a source of unwanted oxidation. No color was observed, and the contact resistivity of the TLM structures on the SiC dummy sample was found to be 1.40×10^{-4} Ωcm^2 which was acceptably low. After a standard solvent clean, we then loaded the lead sample PU435Q2, placing it upside down on the carrier wafer, and placed eight Ti gettering pellets around it so that any possible O_2 would react with them to reduce the effect on the actual sample. We then ran a second purging step followed by the final contact anneal recipe as previously described. The remaining two samples were processed one after the other. Figure 4.27 shows all types of medium and small size devices after the ohmic contact anneal process, and the process run sheet can be found in appendix A.11 for more detail.



(a) (b)

(c) (d)

(e) (f)

Figure 4.27. Various devices after the ohmic contact anneal process (a) Medium A (b) Small A (c) Medium B (d) Small B (e) Medium C (f) Small C.

4.3.12 Top metal

Once the ohmic contact is completed, a thick layer of top metal is deposited to reduce the sheet resistance, leading to better contact resistivity and less spreading resistance during probe testing. This top metal is also used to make ohmic contact with gate polysilicon. The following sub-sections describe the top metal contacts patterning process.

4.3.12.1 ILD opening for gate contact

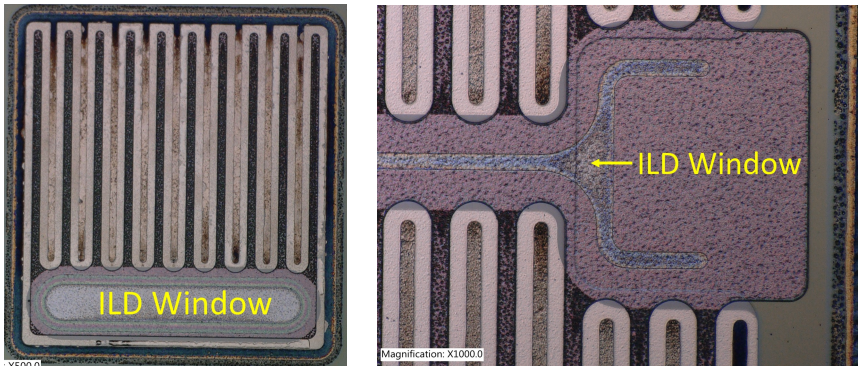
The interlayer dielectric process was described in Section 4.3.9. The process of making metal contact to the gate polysilicon starts by etching a window in the ILD on the gate pad and runners. The samples were first cleaned in standard solvents and an O_2 plasma etch using the Jupiter II. Standard optical lithography was performed using AZ9260, the gate ILD etch mask (# 10) and the Heidelberg MLA150. The detailed process is outlined in appendix A.12. Since the ILD thickness is about 1 μm, we planned to etch about 800 nm by RIE, and the remainder by a wet BOE etch. A test run was conducted to calibrate the etch rate of the RIE process in the Panasonic E620 using 10 sccm CF_4, 40 sccm CHF_3, 650 W RF Power, 50 W Bias Power and a pressure 1 Pa, and obtained an etch rate of 80.3 nm/min. Therefore, the planned RIE etch time was 10 minutes, followed by a 5 min BOE wet etch to ensure the complete removal of the ILD from the window. We etched all three samples sequentially using the RIE process for 10 minutes and by BOE in 3 steps for 3-5 minutes each. The step heights as measured with the P7 profilometer, are listed in the Table 4.6. Since the last etch step did not change the step height it was assumed that no oxide was remaining in the window. It should be noted that the step heights presented in Table 4.6 depicts a general trend of etching. The inconsistency in step heights such as after 10 min etching of PU435Q3 and after 3 min BOE of PU435Q2 comes from the fact that P7 profilometer measures by a line scan and it is not feasible to scan exactly along the same line.

The photoresist mask was then stripped using remover PG from PU435Q2. We measured the step height in several places using P7 profilometer and found the ILD window depth to be 835-950 nm. Figure 4.28 shows two representative devices of PU435Q2 with ILD windows

and trench depths measured using the P7 profilometer. We also measured current conduction by placing two probes inside the ILD window of a device, and then applying a small DC voltage and measuring the resulting current. This was repeated on several randomly selected devices, looking for a linear I-V characteristic, which would indicate direct contact to exposed polysilicon, and found some were conductive and some were not. It was surprising to find an oxide layer remaining in the window after such a long etch. However, we decided to proceed with sputtering about 400 nm of Al as a top metal, which will be discussed in the following section.

Table 4.6. Estimation of etched ILD thickness.

	Photoresist	**Photoresist Mask+Oxide Trench**			
Sample ID	**Pre-RIE (nm)**	**10 min RIE (nm)**	**3 min BOE (nm)**	**4 min BOE (nm)**	**5 min BOE (nm)**
PU435Q2	5156	5338	5210	5633	5556
PU435Q3	5183	5189	5599	5670	5629
PU436Q2	5248	5308	5550	5447	-

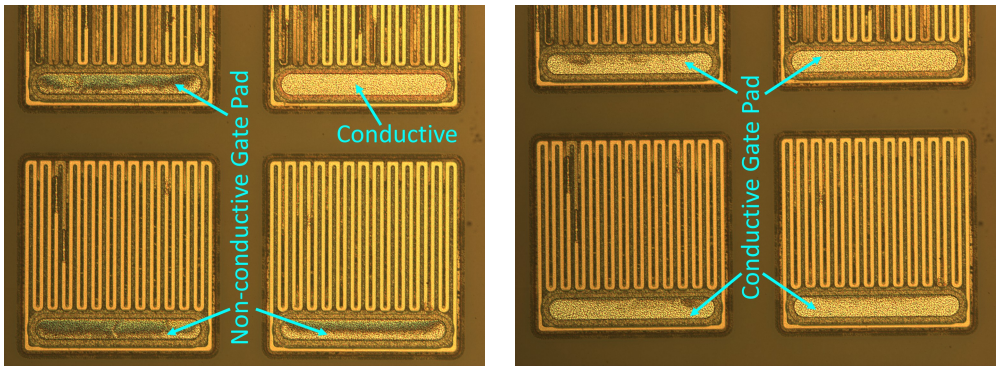


(a) (b)

Figure 4.28. Images from PU435Q2: (a) ILD window in a small device (b) ILD window in a large device.

By this time the PU435Q3 and PU436Q2 samples were waiting with a PR mask, and more careful observation of the ILD windows with an optical microscope and electrical conductivity testing on the other two samples indicated that the oxide needs to be further

etched. Therefore, we started etching with BOE step by step, each time checking for residual oxide. For example, Fig. 4.29(a) shows one conductive and three non-conductive ILD windows after etching 10 min by RIE and 8 min by BOE. The color contrast between the conductive and non-conductive pads highlights the presence of oxide in certain pads, even after 5 min of additional etching in BOE as shown in Fig. 4.29(b). We treated PU436Q2 similarly and ended up etching for 10 min by RIE and 13 min by BOE.



(a) (b)

Figure 4.29. Images from PU435Q3: (a) one conductive and three non-conductive ILD windows after 10 min RIE and 8 min BOE etch (b) four conductive ILD windows after 10 min RIE and 13 min BOE etch.

Sample PU435Q2 was patterned with photoresist again using the gate ILD etch mask (# 10) and Al was etched from the ILD windows for 80 sec at 50°C in a manually prepared Al etchant type A (H_3PO_4: HNO_3:CH_3COOH:DI::400 ml:25 ml:25 ml:50 ml). Photoresist was stripped by soaking in acetone for 60 minutes and methanol for 10 minutes. The lithography was repeated with the same recipe and mask for further etching the ILD with a fresh mask in place. We continued to etch oxide in BOE in steps, and stopped after a total of 10 minutes by RIE and 16 minutes by BOE. We verified that the cleanliness of the ILD windows was similar to the other samples by optical microscope and electrical conductivity testing. Finally, photoresist masks were stripped by soaking in remover PG for overnight. We found that the large devices of PU435Q2 and PU436Q2 did not have very clear ILD windows, with a few exceptions which should be functional. Gate runner of a few of the large devices were

over etched laterally, leading to a potential risk of source and gate contact metal merging. However, most all other devices appeared reasonably clean upon final inspection.

4.3.12.2 Top ohmic metal

The samples were solvent cleaned followed by an O_2 plasma etch in the Branson asher for 1 min at 100 W. The samples were dipped in BOE for 10 sec to strip any unwanted thin oxide in the active region and loaded together in the PVD sputtering system. Aluminum was deposited for 3 hours 30 minutes with the following parameters: power = 350 W, Ar flow = 15 sccm. The expected deposition rate was 2.6 nm/min as previously calibrated by the staff. Therefore, the estimated Al thickness was 546 nm. However, PU435Q2 had a pre-existing 400 nm Al, which made for a total of 946 nm.

We next performed photolithography using HMDS, AZ1518, top metal mask (# 11) and the Heidelberg MLA150. We prepared Al etchant type A as previously described, and etched the top metal of PU435Q2 for 12 minutes at room temperature. Although process run sheet in appendix A.13 indicates 2 minutes etching at 50°C we decided to etch at room temperature for longer time in order to avoid using the hot plate and thermocouple setup. After the etch, Al residue was observed in various places under the optical microscope, and therefore etching was continued for another 2 minutes in a fresh solution, after which the features looked clean. A similar approach was followed for PU435Q3 and PU436Q2, which were etched for a total of 13 minutes and 10.5 minutes, respectively. Finally, the processing of the top of the samples was concluded by stripping the photoresist overnight in remover PG. Figure 4.30 shows all types of small and medium devices after completing the top side fabrication process. A schematic cross section of the top ohmic metallization process is shown in Fig. 4.31. The processing details can be found in appendix A.13.

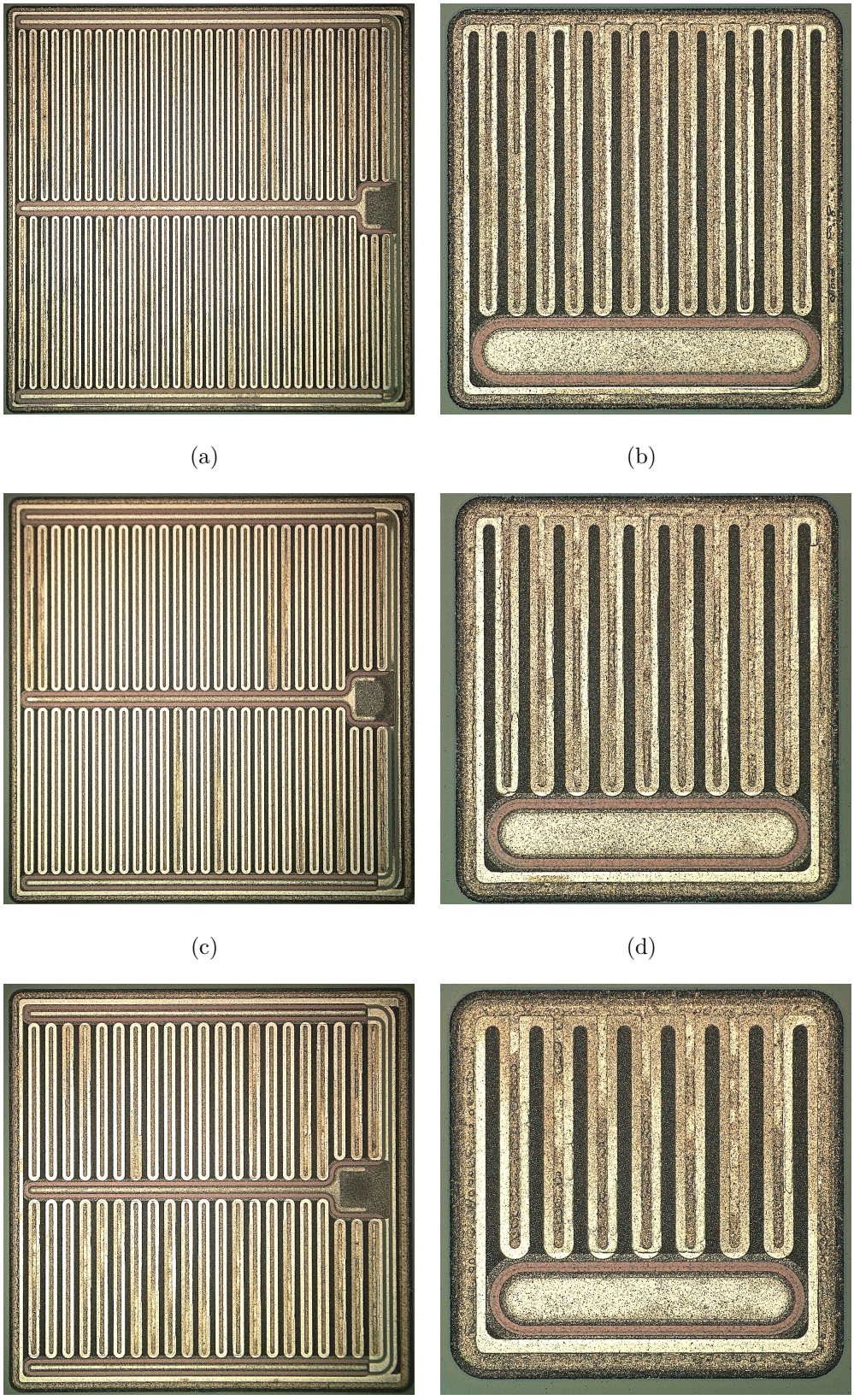


Figure 4.30. Devices after completing the top side processing (a) Medium A (b) Small A (c) Medium B (d) Small B (e) Medium C (f) Small C.

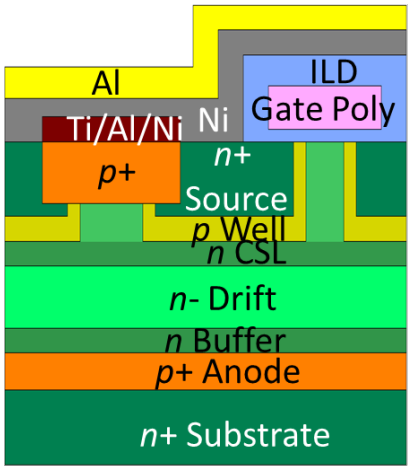


Figure 4.31. A schematic cross section of the top ohmic contact metallization process

4.3.13 Waffle substrate

The waffle substrate processing can be divided into six major tasks as will be discussed in the following sections. The waffle process development was first reported in [56], but had not yet been integrated with any devices. In this research, a significant amount of time was spent to develop a reliable unit process using test samples, which was then integrated into the waffle substrate IGBT process. However, some of the process developments described in the first three sections 4.3.7, 4.3.13.2 and 4.3.13.3 were conducted simultaneously. One of my fellow graduate students Rajni Sah also conducted some of the trials alongside to expedite the process development as a part of her hands-on training. Therefore, new recipes were adopted as needed based on the outcome of these trials. The etching process was completely accomplished using an STS-AOE ICP-RIE tool. The waffle substrate process was completed for PU435Q2 and PU435Q3, but only a partial process was applied to PU436Q2. Therefore, we will discuss only the first two samples. More detail processing information is well-documented in appendix A.14.

4.3.13.1 Thinning the substrate by RIE

The first step in the waffle substrate process is to thin the substrate from 360 um to 150-200 µm before applying the waffle etch process. This is typically done by grinding and

chemical mechanical polishing. However to save time this was done with our well-established RIE etch process. This process requires a good estimation and/or measurement of the total thickness of the sample. According to the manufacturer specifications, the total thickness of PU435 is 482.2 ± 8.5 µm as shown in Fig. 4.7. The IGBT was processed in Q2 and Q3 while we measured the thickness of the other two quarters using a micrometer. The thickness map presented in Fig. 4.32 varies in the range 479 - 483 µm which is comparable with the manufacturer's data.

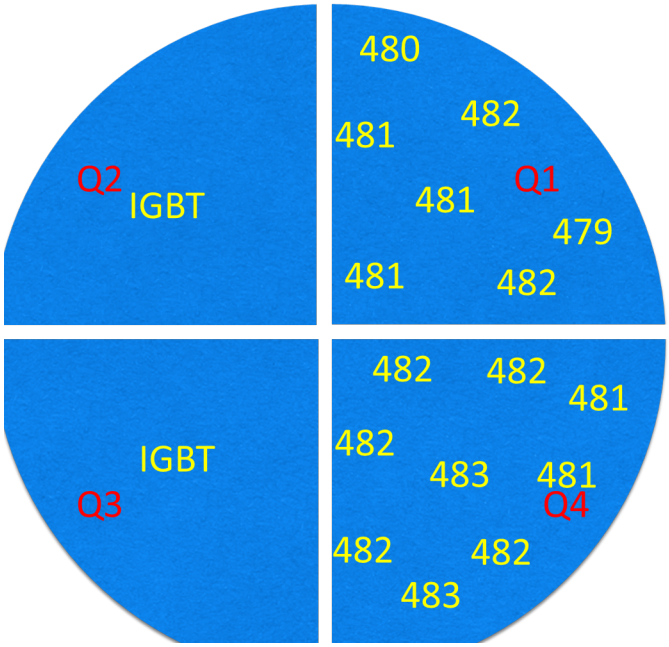
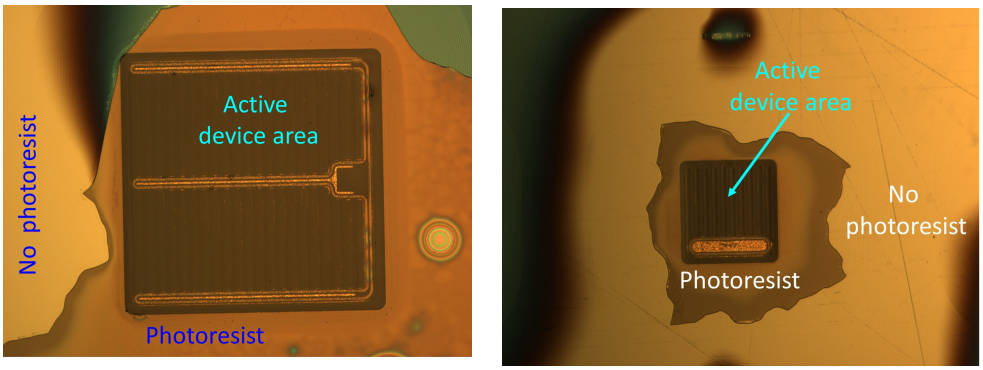


Figure 4.32. Thickness (µm) map as measured by a micrometer.

We started the processing with a dummy quarter wafer PU435Q4 followed by the actual IGBT sample PU435Q2. The sample was thinned by RIE in the STS-AOE whereas the originally proposed method [56] was to grind the substrate to a desired thickness. At this point, all the IGBT samples still had residual oxide and polysilicon layers on the back surface built up during the front side processing. Sample PU435Q2 was solvent cleaned, then the top side of the sample was spin-coated using AZ9260 at 4000 rpm, 30 sec followed by baking at 110°C and 145°C for 3 minutes and 5 minutes respectively. This resist film acts as a protective layer during the subsequent wet etching. Hard baking at high temperature (> 130 - 140°C) is recommended by the manufacturer for harsh environments like HNO_3

[57]. It was soaked in the mixture DI:HF:HNO_3::50 ml:50 ml:250 ml for 5 minutes to strip the polysilicon layer. However, after few minutes we noticed that PR was stripped/etched very aggressively. Therefore, the sample was pulled out of the solution immediately and thoroughly rinsed in DI. Figure 4.33 shows a couple of images after this incident. Luckily, active areas most of the devices were still protected by the mask. However, the field oxide was most likely thinned or completely etched in random locations, but most devices were expected to remain functional. The photoresist mask was stripped by soaking in remover PG for overnight and the top side was spin-coated with AZ1518 at 1000 rpm, 40 sec followed by baking at 100°C and 120°C for 1 minute and 20 minutes respectively as a replacement protective layer during the wet etching of the remaining oxide. The sample was then soaked in BOE for 8 minutes followed by stripping the PR in remover PG.



(a) (b)

Figure 4.33. Images of small and medium devices with stripped/peeled-off PR mask during back side polysilicon wet etching of PU435Q2.

We used AZ9260 photoresist to mount the sample on a 4" silicon carrier wafer compatible with the STS-AOE in order to reduce the risk of residue forming on the top surface of the sample where the IGBT structure had already been fabricated. The carrier sample was spin-coated with AZ9260 at 4000 rpm, 30 sec. Sample PU435Q2 was then placed in the center and baked at 110°C for 3 minutes. In order to estimate the thickness after etching we included six 1 cm × 1 cm SiC samples mounted around the original sample as shown in Fig. 4.34.

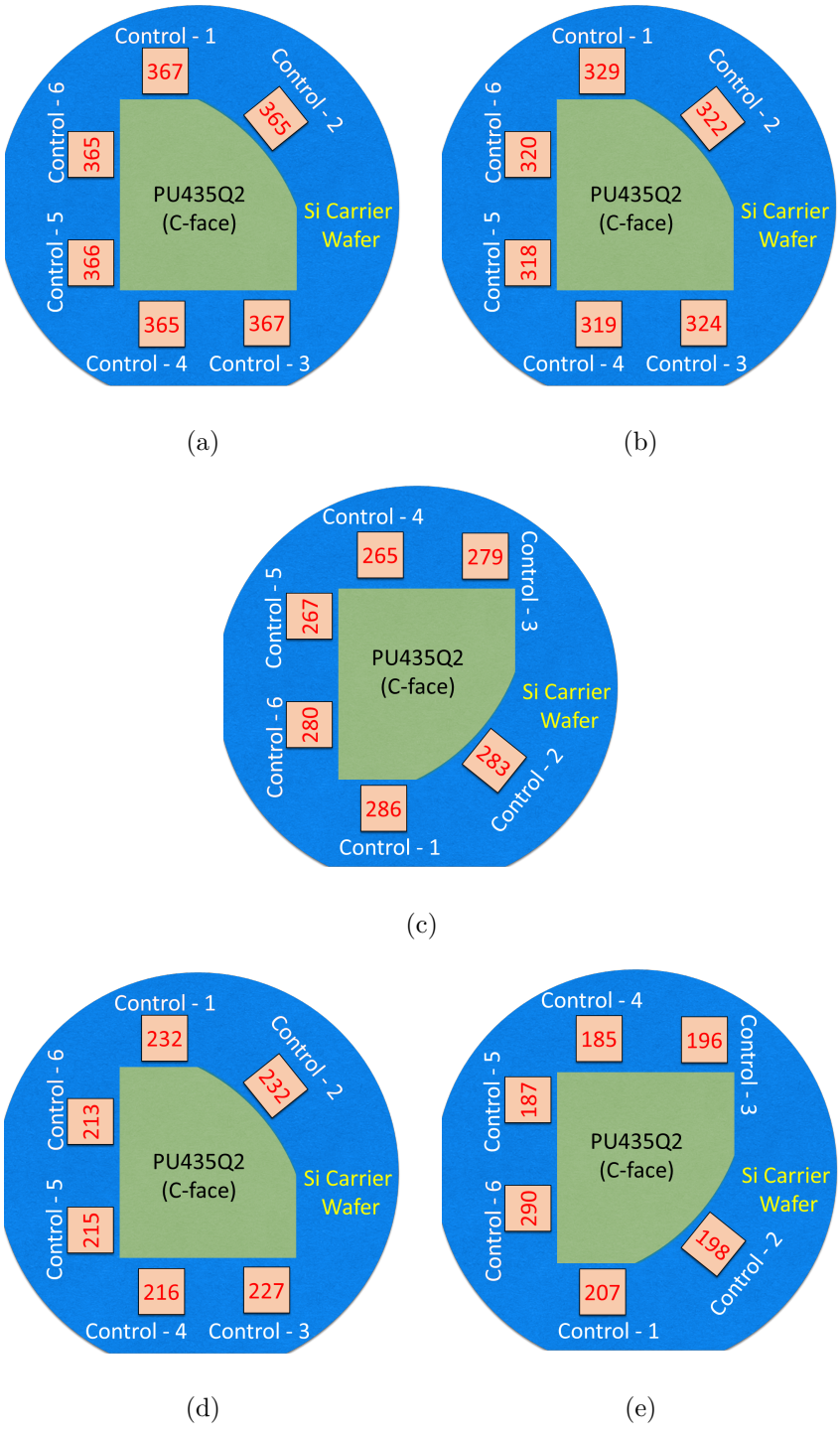


Figure 4.34. Estimated thickness of PU435Q2 measured by micrometer during substrate thinning by RIE using the recipe: RF Power - 1800 W, Bias Power - 50 W, SF_6 flow - 6 sccm, Ar flow - 10 sccm, Pressure - 10 mTorr (a) Before etch (b) After 1st 4 hr round (Orientation of mounting for next round) (c) After 2nd 4 hr round (Orientation of mounting for next round) (d) After 3rd 4 hr round (Orientation of mounting for next round) (b) After 4th 2 hr round.

We started the etch with the following recipe: STS-AOE RF Power: 1800 W, Bias Power: 50 W, SF_6 flow: 6 sccm, Ar flow: 10 sccm, Pressure: 10 mTorr. We expected to etch a maximum of 4 hours and replace the carrier wafer in order to prevent its breakage. For a given 4 hour etch the sequence was 1 hour etch - cool down - 3 hour etch to prevent the hardening of PR. Sample PU435Q2 was etched for two 4 hours rounds by mounting with photoresist and two more rounds of 4 hours and 2 hours by mounting with the crystal bond (CB). Photoresist bonding is less thermally conductive than CB, allowing the sample to heat significantly during long duration RIE etches, which affects the trench geometry significantly and the etch rate moderately, as will be discussed in the following section. Crystal bond was cleaned from the sample with running DI water, and no significant amount of residue was observed. Figure 4.34 presents the thickness of the control samples before and after the etch, and it is assumed that they represent the etch rate of the actual sample. The orientation of the samples were changed at every round of etches as can be seen from Fig. 4.34(c) and 4.34(e) to reduce the thickness variation across the sample. It is interesting to note that the average etch rate increased gradually during the etch: 10.96 μm/hr, 11.33 μm/hr, 13.54 μm/hr, and 14.33 μm/hr. The switch to crystal bond contributed to this increase in etch rate as expected. Based on the change in thickness of the control samples, we estimate that the sample was thinned by about 160 - 180 μm. In other words, the remaining substrate thickness of PU435Q2 was estimated to be in the range 181.2 - 201.2 μm.

However, after performing a few more trials using test samples while processing PU435Q2, we arrived at an improved recipe: RF Power: 1800 W, Bias Power: 70 W, SF_6 flow: 17 sccm, Pressure: 10 mTorr, mounting: CB. This became the standard waffle etch recipe, due to significantly increased etch rate and better trench geometry as will be discussed in the following section.

PU435Q3 went through the same process steps to strip the oxide and polysilicon layers from the gate processing with a slight change in the top side protective layer and timing of the polysilicon etching. The top side was this time protected by an AZ1518 layer which was spun at 1000 rpm for 40 sec and baked at 100°C and 120°C for 1 minute and 20 minutes, as described in [58], and as is used by many other previous students in the group.

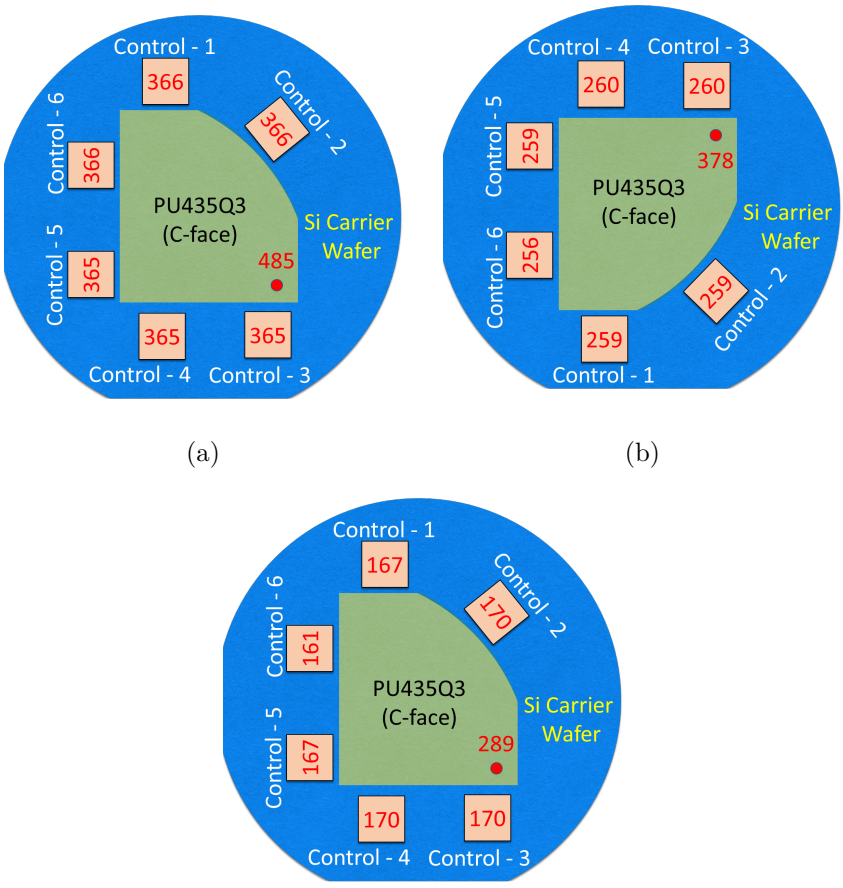


Figure 4.35. Estimated thickness of PU435Q3 measured (red dot indicates the measurement point of the actual sample) by micrometer during substrate thinning by RIE using the recipe: RF Power - 1800 W, Bias Power - 70 W, SF_6 flow - 17 sccm, Pressure - 10 mTorr (a) Before etch (b) After 1^{st} 4 hr round (Orientation of mounting for next round) (c) After 2^{nd} 3 hr round.

We etched polysilicon with the same wet chemical etchant as used for PU435Q2 but only for 80 sec. Surprisingly we noticed the same aggressive etching of PR when the etch duration exceeded 80 sec. The sample was immediately taken out of the solution and rinsed thoroughly in DI. The remaining oxide was stripped following the same steps of PU435Q2. The active areas on PU435Q3 appear to be unaffected, but finding the root cause of this problem remains an outstanding problem. To thin PU435Q3 we used the standard recipe described above, which led to an etch of about 196 μm in 7 hours. This time the thickness was measured directly at one of the corners of the sample using a micrometer for better accuracy,

although six control samples were included as before. The etch rates were 26.75 μm/hr and 29.70 μm/hr in two rounds of 4 hours and 3 hours respectively. Therefore, the remaining substrate thickness was estimated to be 165.2 μm. Figure 4.35 presents the thickness data aquired during the RIE.

4.3.13.2 Masking procedure for waffle pattern

The waffle etch process requires a highly selective mask material that can be used to do a very deep trench etch. This requirement is fulfilled with a thick layer of nickel deposited by electroplating. The electroplating process requires a thin seed layer of highly electrically conductive metal. We experimented with two different seed layers: chromium (Cr) and Titanium/Gold (Ti/Au). We also experimented with both hexagonal and circular trench shapes. The front Si-face of the sample was first spin-coated with AZ9260 at 4000 rpm, 30 sec followed by baking on a hotplate at 110°C for 3 minutes to protect the completed IGBT devices. Next a 100 nm thick layer of Cr was deposited on the C-face by metal evaporation in the CHA-1 system. Then standard photolithography using 6.75 μm thick AZ9260 was carried out to create hexagonal patterns. The sample was cleaned in an O_2 plasma using a Branson asher for 1 min at 100 W to cleanup any residual PR that might prevent Ni deposition. We used a manually operated beaker-based setup with about 750 ml of nickel sulfamate as the electrolyte. The sample was connected to a cathode, submerged in the solution, and a current of 80 mA was supplied from a dc power supply for 45 minutes. The solution was continuously stirred at 100 rpm and the temperature was maintained at 40°C using a thermocouple. Figures 4.36(a) and 4.36(b) show images of the sample before and after the electroplating. The purpose of the photolithography was to prevent Ni deposition where the PR pattern was present because it is not electrically conductive. However, the features clearly indicate a discontinuous Ni film, most likely because of a native oxide forming on the Cr seed layer due to air exposure. Since gold does not corrode in air, we then deposited 25 nm Ti and 75 nm Au as a seed layer using the CHA-1 evaporator on another test sample. All other processes describe above were followed, and the result is shown in Figs. 4.36(c) and 4.36(d).

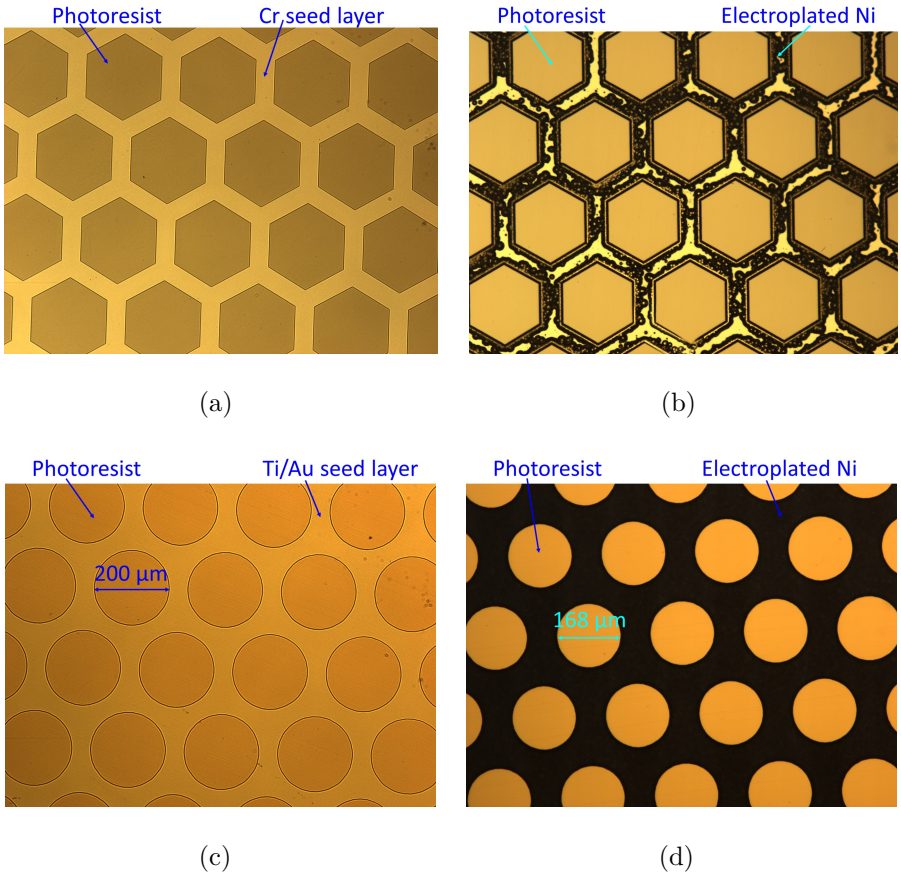
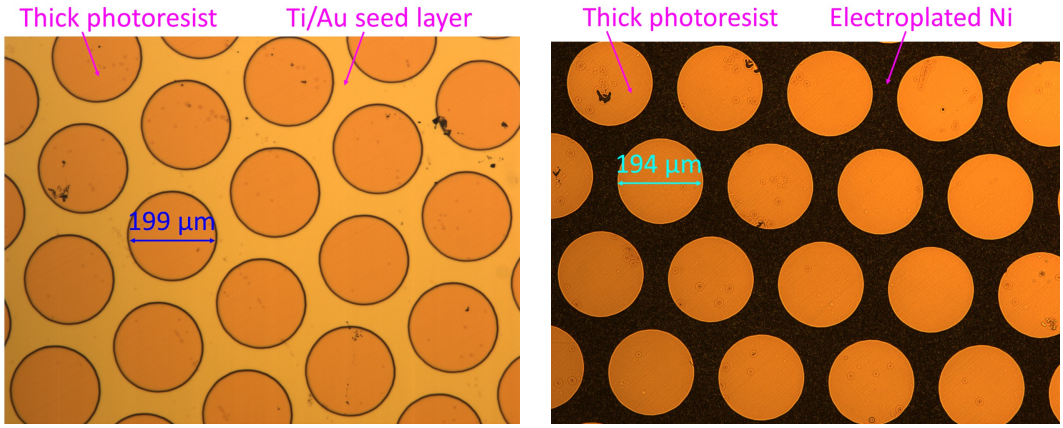


Figure 4.36. (a) Photoresist pattern on a Cr seed layer (b) After electroplating on the Cr seeded sample (c) Photoresist pattern on a Ti/Au seed layer (d) After electroplating on a Ti/Au seeded .

The problem of a discontinuous Ni film was resolved with a Ti/Au seed layer, but as can be seen in Fig. 4.36(d), the circular patterns shrank significantly. This occurs because whenever the film thickness grows beyond the photoresist height it begins to grow laterally as well as vertically. We solved this problem by doing a double coated AZ9260 photolithography as described in A.14 2(iv) which produced an approximately 20 µm thick resist pattern. The result after electroplating with this modified resist process is shown in Fig. 4.37 where the lateral expansion of the electroplated metal was significantly suppressed.

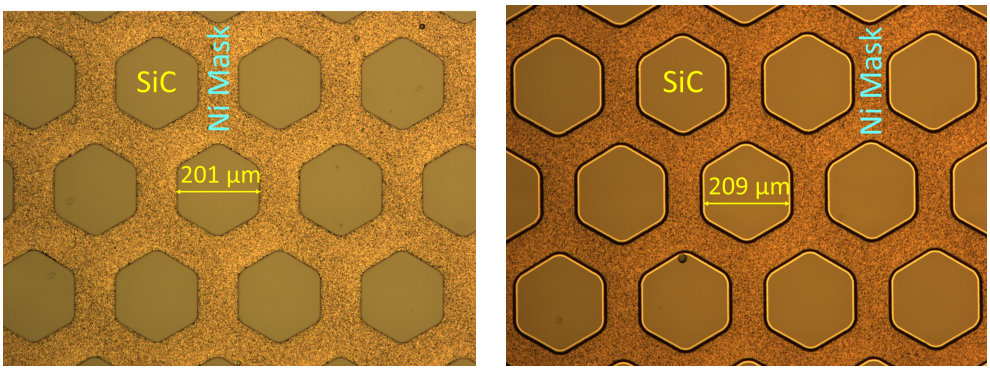


(a) (b)

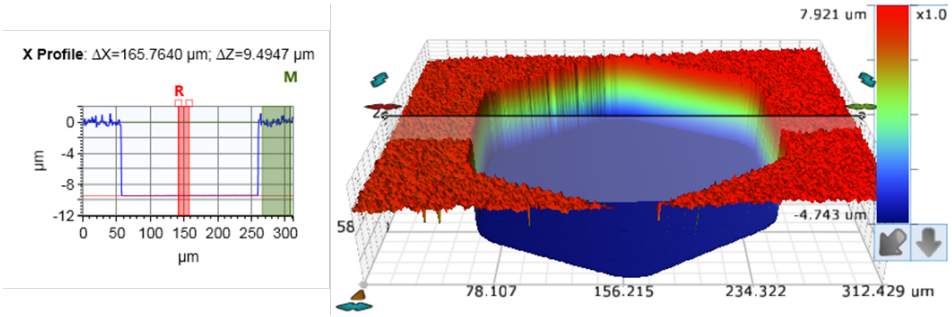
Figure 4.37. (a) Thick photoresist pattern on a Ti/Au seed layer (b) After electroplating Ni.

Once a suitable recipe was developed, we cleaned PU435Q2 and PU435Q3 in standard solvents, and applied a protective AZ9260 coating on the top side. A (25 nm Ti and 75 nm Au) seed layer was deposited on the back side of both samples in the CHA-1. The waffle mask photolithography was carried out by twice coating with AZ9260 for about 20 µm thick features. The process detail is described in appendix A.14 2(iv). To increase the etched area, we decided to use a hexagonal waffle pattern with rounded corners. Any residue from the photoresist was cleaned by O_2 plasma etching in a Branson asher at 100 W for 1 minute. The standard Ni electroplating was conducted as described above for 1 hour 30 min for one sample at a time followed, by stripping the PR in remover PG, which exposed the seed layer in the hexagonal features. The top side was again protected by spin coating AZ1518 at 1000 rpm, 40 sec followed by baking at 100°C and 120°C for 1 minute and 20 minutes. The Au and Ti layers of PU435Q2 were removed in a GE-8148 solution and in a mix of DI:H_2O_2:HF::400 ml:20 ml:20 ml for 30 sec each. We initially observed some seed layer residue, and thus re-etched by 10 more seconds to fully remove the seed metals. PU435Q3 went through the same steps but the seed layers were over-etched by 30 sec to clean up the residue. Figure 4.38 shows the top view and the thickness of the electroplated Ni mask of the two samples as determined using a Bruker optical profilometer. The thickness was measured at different points of the samples PU435Q2 and PU435Q3 and found a range of

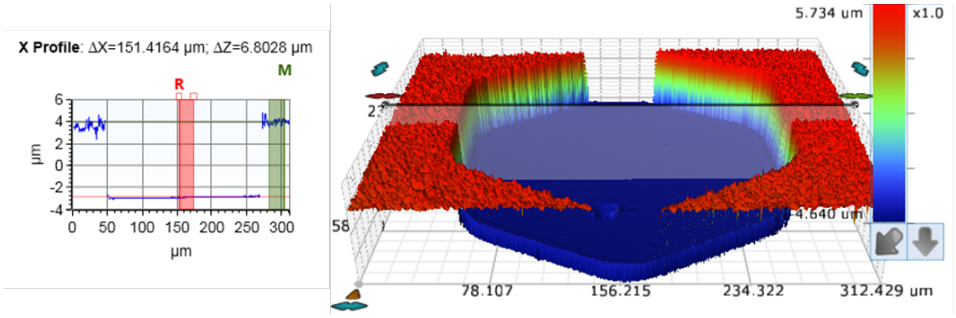
values such as 9.5 - 13.5 µm and 5.4 - 10.0 µm respectively. It should be noted that before etching the seed layer of PU435Q3 we measured the thickness of the mask at the center of the sample as 11.5 µm while it came down to 6.8 µm unlike PU435Q2. The hypothesis is that the electroplated Ni was contaminated because of re-using expired electrolyte which could not survive during the seed layer etching process.



(a) (b)



(c)



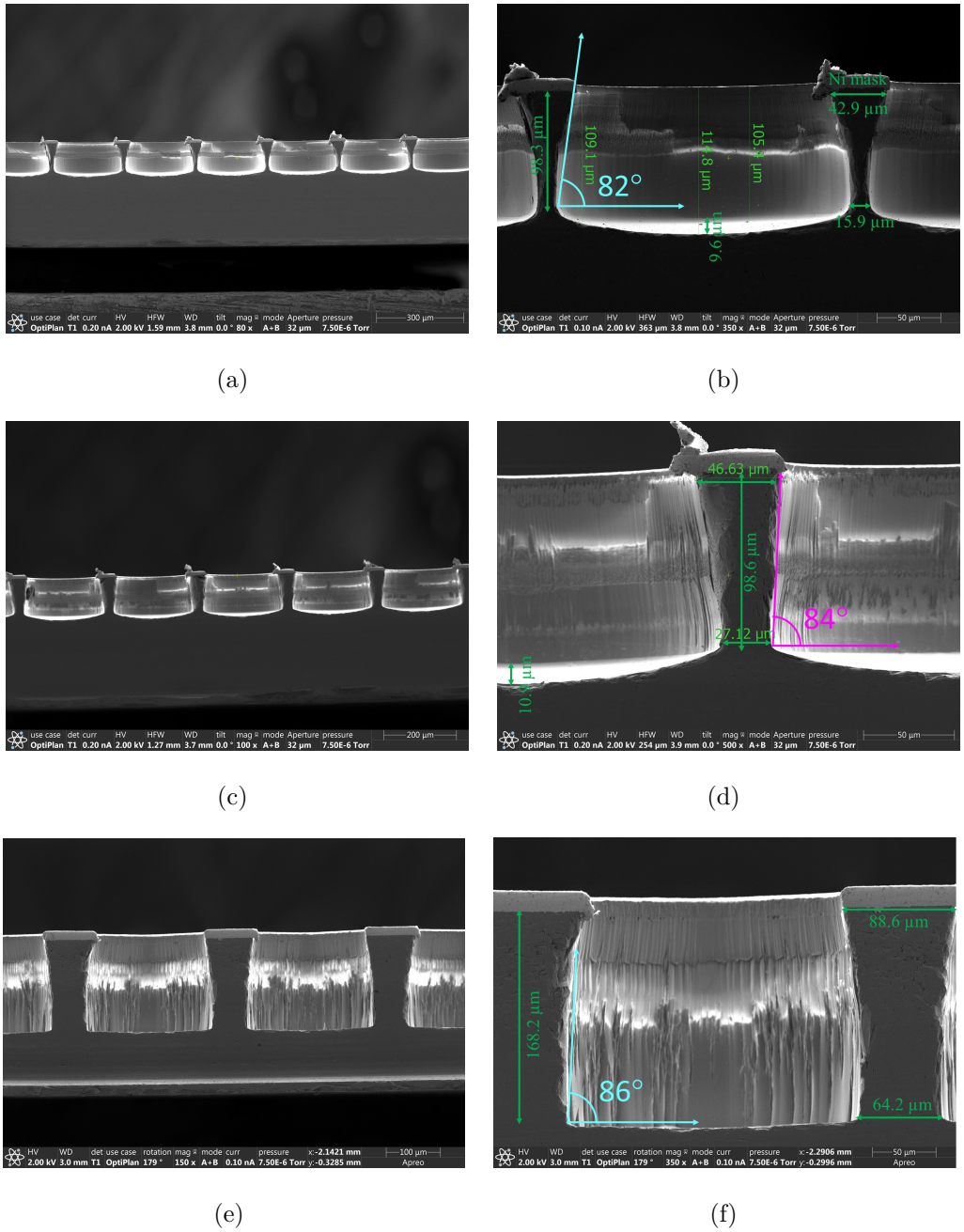
(d)

Figure 4.38. Electroplated Ni waffle etch mask (a) Top view from PU435Q2 (b) Top view from PU435Q3 (c) Mask thickness (ΔZ) of PU435Q2 measured by Bruker (d) Mask thickness (ΔZ) of PU435Q3 measured by Bruker.

4.3.13.3 Waffle pattern by RIE

The waffle pattern RIE etch recipe was developed based on many test sample trials. In all cases, the waffle etch mask was formed by Ni electroplating using Ti/Au as seed layers as described above. We used PR and crystal bond as mounting materials, and mounted as described in Section 4.3.7. We also varied certain etch parameters to find the best possible recipe in the STS-AOE ICP-RIE etcher. The main issues were the limitation of maximum etch time in a single run, obtaining a suitable etch rate to achieve a sufficiently deep trench, and the STS-AOE system availability due to its age and frequent down-time. However, we had to etch at least around 100 μm deep trenches which took about 4 - 8 hours depending on the recipe to see the geometry of the trenches because vertical trench wall is desired for robustness.

Figure 4.39 presents cross section images of waffle patterns taken by an Apreo SEM tool for three different trials out of many. Since the features are very large they were diced instead of cut by the focused ion beam method. The highlights of the outcome of these trials are as follows. The photoresist mounting technique increases the undercut angle of the sidewall compared to crystal bond even with the same recipe. Both of these recipes created a significant amount of bow in the middle of the trench as illustrated in the images, which is due to the high bias power. The effect of the bias power is not clear from these images but was observed in other trials. Comparing Figs. 4.39(d) and 4.39(f), we see that the side wall became more vertical when Ar flow is excluded from the recipe. Therefore, we concluded the trials with this as the standard recipe used for processing PU435Q2 and PU435Q3.



(a) (b)

(c) (d)

(e) (f)

Figure 4.39. SEM images of waffle pattern cross sections with RIE Recipe 1: RF Power - 1800 W, Bias Power - 100 W, SF_6 flow - 6 sccm, Ar flow = 10 sccm, Pressure - 10 mTorr, PR mounted (a) Full view (b) Magnified view; Recipe 2: RF Power - 1800 W, Bias Power - 100 W, SF_6 flow - 6 sccm, Ar flow = 10 sccm, Pressure - 10 mTorr, CB mounted (c) Full view (d) Magnified view; Recipe 3: RF Power - 1800 W, Bias Power - 70 W, SF_6 flow - 17 sccm, Pressure - 10 mTorr, CB mounted (e) Full view (f) Magnified view.

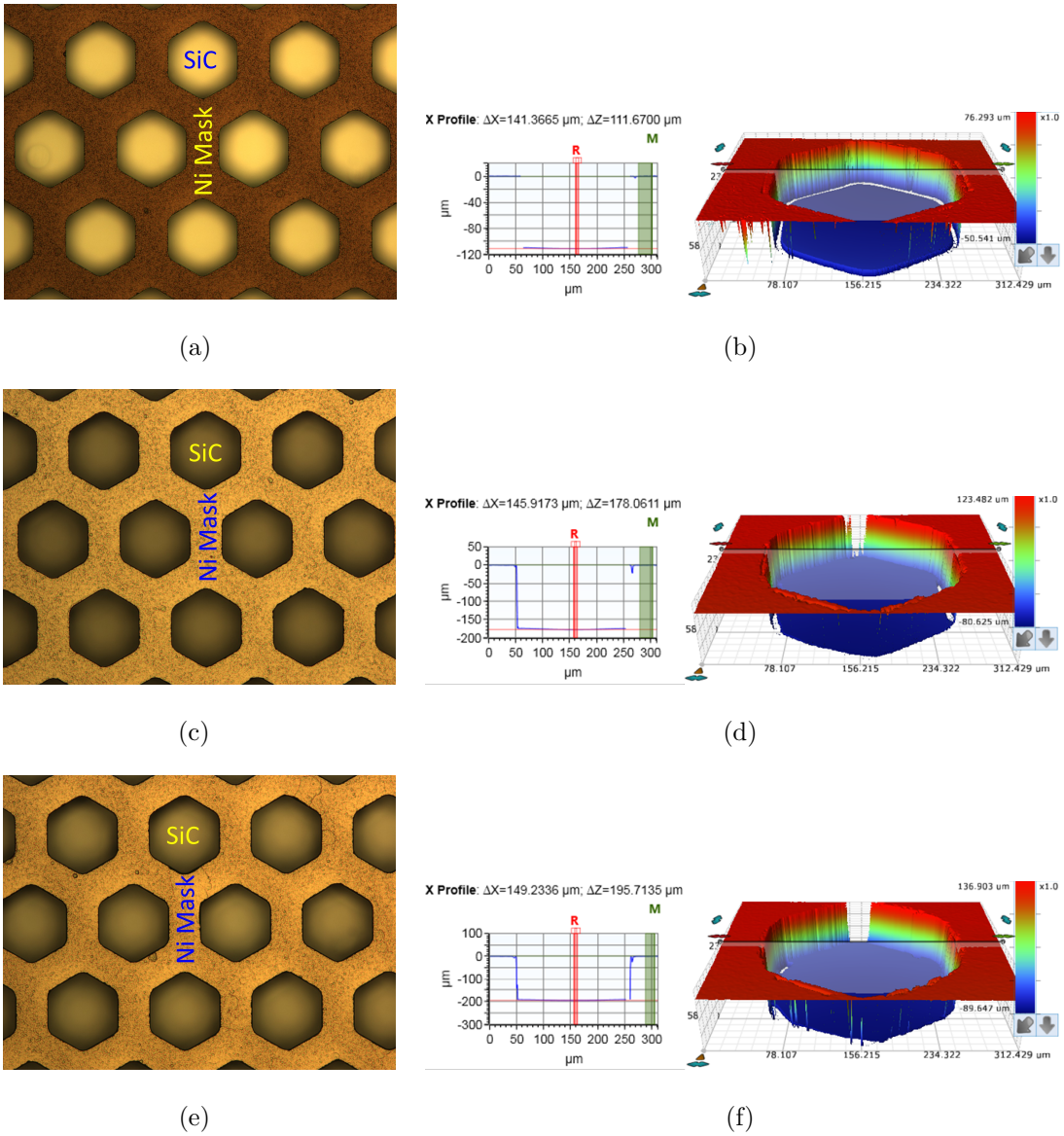
Waffle etching of PU435Q2:

The most important part of waffle etching in the actual IGBT samples is to etch enough to remove the n-type substrate completely and stop within the p-type anode layer. We tracked the trench depth using a Bruker profilometer at various places on the sample. It was etched in three steps of 4 hours, 3 hours, and 45 minutes. The top view of the waffle patterns and measured trench depths at the center of the sample are shown in Fig. 4.40. In order to estimate the actual trench depth of this sample excluding the Ni mask, the Ni etch rate must be accurately known. Three small samples accompanied PU435Q2 on the same carrier and one of them was etched only for first 4 hours. Later on the Ni layer was stripped in TFG for 2 hours. Table 4.7 shows that the Ni etch rate with the standard recipe was about 295 nm/min. Therefore, from Figs. 4.38(c) and 4.40(f) we can estimate that actual trench depth in PU435Q2 after 7 hours and 45 minutes RIE was 188.5 μm.

In addition to using etch depth measurements and Ni etch rate estimates, the p-type anode layer was detected by measuring the I-V characteristics using a dc voltage sweep at each etching step as shown in Fig. 4.41. The left-most three curves clearly represent a low barrier height Schottky I-V characteristic, while the fourth curve (red) represents the I-V characteristics of a Schottky in series with a p-n junction diode. Therefore, we stopped etching PU435Q2 as p-type anode layer was clearly reached.

Table 4.7. Estimation of the Ni etch rate after 4 hours of RIE in STS-AOE from a test sample accompanying PU435Q2.

Thickness of Ni Before Etch (μm)	**Trench Depth Before Ni Stripped (μm)**	**Trench Depth After Ni Stripped (μm)**	**Remaining Ni After RIE (μm)**	**Etched Ni During RIE (μm)**	**Etch Rate of Ni (nm/hr)**
14.81	110.05	96.42	13.63	1.18	295

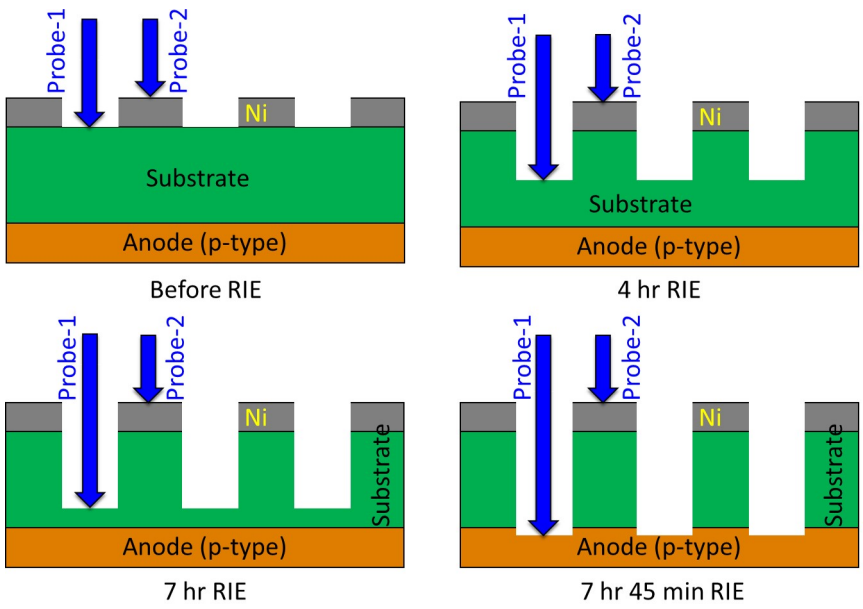


(a) (b)

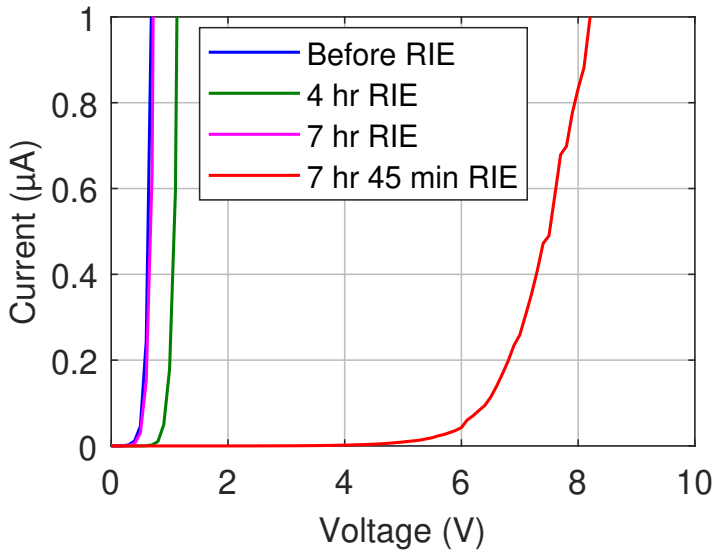
(c) (d)

(e) (f)

Figure 4.40. Waffle etching of PU435Q2 in STS-AOE with recipe: RF Power - 1800 W, Bias Power - 70 W, SF_6 flow - 17 sccm, Pressure - 10 mTorr, CB mounted (a) Top view after 4 hours RIE (b) Trench depth after 4 hours RIE (c) Top view after 7 hours RIE (d) Trench depth after 7 hours RIE (e) Top view after 4 hours and 45 min RIE (f) Trench depth after 7 hours and 45 min RIE.



(a)



(b)

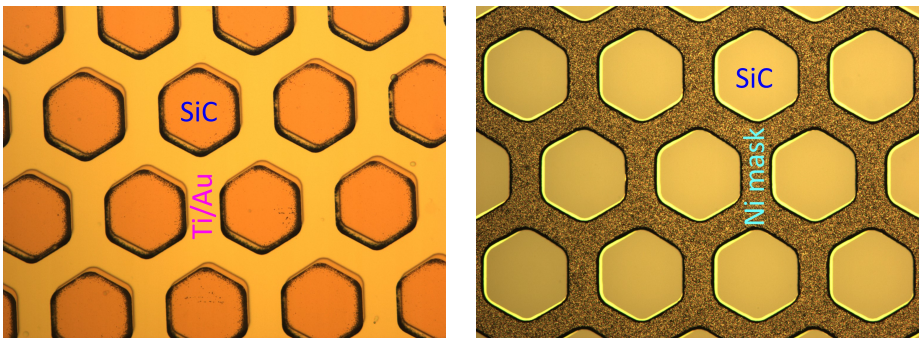
Figure 4.41. PU435Q2 processing: etch stop detection by I-V characteristics (a) Schematic diagram of probe station I-V measurements at various steps of the waffle etch (b) I-V characteristics as etching progresses.

Waffle etching of PU435Q3:

We started etching PU435Q3 in STS-AOE using the standard waffle etch recipe. The etching process was stopped after 10 minutes because the tool was malfunctioning. After

restarting the error happened again after 10 minutes. This interrupted RIE process created 5.2 - 5.7 μm trenches in the SiC substrate. However, since the sample had a thinner Ni mask compared to PU435Q2 we decided to deposit more Ni by electroplating to be in the safe side. At this point, there was no PR pattern present on the sample, so the standard Ni electroplating procedure was executed without a photoresist pattern and it was observed that Ni was deposited everywhere because the substrate acted as electrically conductive surface due to its high doping. Therefore the waffle etch mask had to be completely reworked.

The Si-face of the sample was spin-coated with a protective layer of AZ9260 at 4000 rpm, 30 sec followed by baking at 110°C and 155°C for 3 minutes and 5 minutes respectively. The electroplated Ni was stripped in Ni etchant TFG for 3 hours 40 minutes at a thermocouple controlled 50°C, followed by Au and Ti etching in their respective etchants mentioned above for 90 sec each. The seed layer (Ti/Au) was again deposited using the CHA-1. The existince of the previously etched shallow trenches made the waffle pattern lithography challenging because there were no alignment marks. However, a standard lithography recipe for the waffle mask was followed with an attempt to align with the existing waffle trenches manually. Then the standard Ni electroplating process was run for 90 min followed by PR stripping in remover PG and Ti/Au etching in their respective etchants. Unfortunately a similar issue occurred with the Ni during seed layer etching. We measured the step heights using the Bruker profilometer, and found that the Ni mask thickness ranged from 6.2 - 12.1 μm. By this time we had gained an accurate knowledge of the Ni etch rate and decided to proceed for waffle etching. Figures 4.42(a) and 4.42(b) represent the lithography mask and final waffle mask after re-electroplating the Ni mask layer. The slightly misaligned features are visible, but do not pose a significant problem.

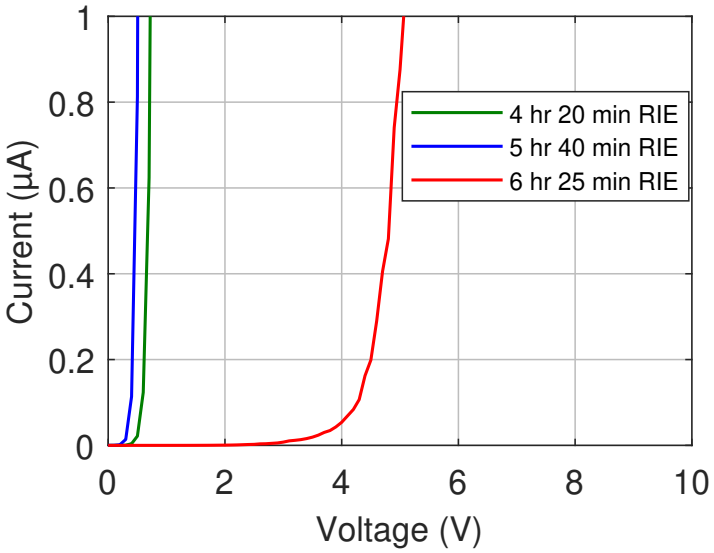


(a) (b)

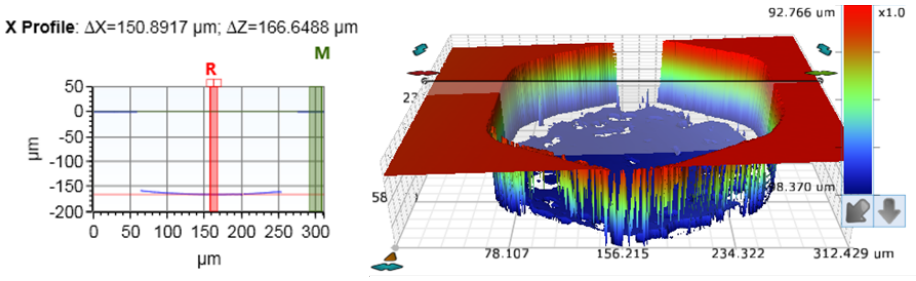
Figure 4.42. PU435Q3 processing: (a) PR pattern for Ni re-electroplating (b) Final waffle etch mask after re-electroplated Ni.

The waffle etching of this sample was conducted in three steps for 4 hours, 1 hour 20 minutes and 45 minutes. Considering the interrupted RIE the total etch time of this sample was 6 hours 25 minutes. We stopped the etching after verifying the trench depth using Bruker and I-V characteristics obtained in the same way as sample PU435Q2. The results are shown in Fig. 4.43(a) which clearly indicates the *p*-layer has been reached. Unlike PU435Q2, we stripped the Ni mask in etchant TFG for 2 hours at 50°C after the waffle etching was complete. The trench depth was measured at different places of the sample to be in the range 162.2 - 166.6 μm, and an example of the measured data is shown in Fig. 4.43(b).

However, re-working this sample led to Ni residues at the bottom of the trenches which is likely to contribute high contact resistivity. Figure 4.44 shows two images of the waffle pattern taken by optical microscope focusing at the top of the fins and at the bottom of the trenches which shows some dark spots at the bottom which are presumably Ni residue. After stripping the Ni mask from PU435Q3 we found an average Ni etch rate of 470 nm/hr, and SiC etch rate of 25.7 μm/hr, which gives an etch selectivity of electroplated Ni to 4H-SiC as 1:55. The etching process was accompanied by two small samples mounted on the same carrier wafer, and the images of the waffle geometry of these samples should be representative of the actual sample. Figure 4.45 presents both top and tilted views of the waffle pattern from a control sample processed simultaneously with PU435Q3.

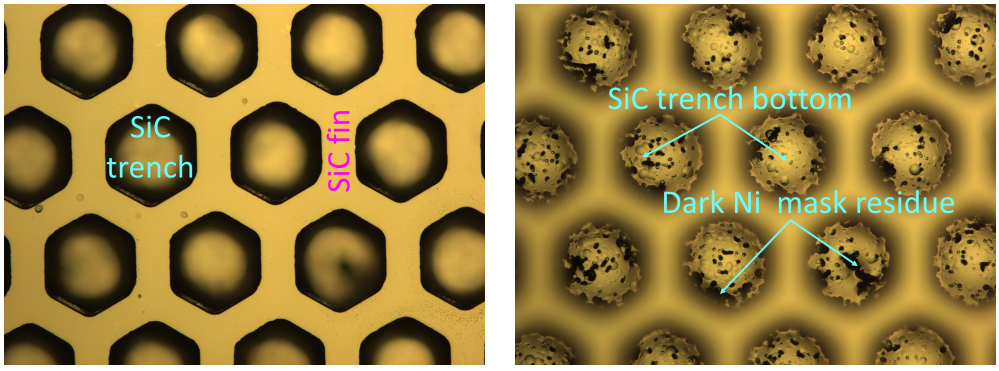


(a)



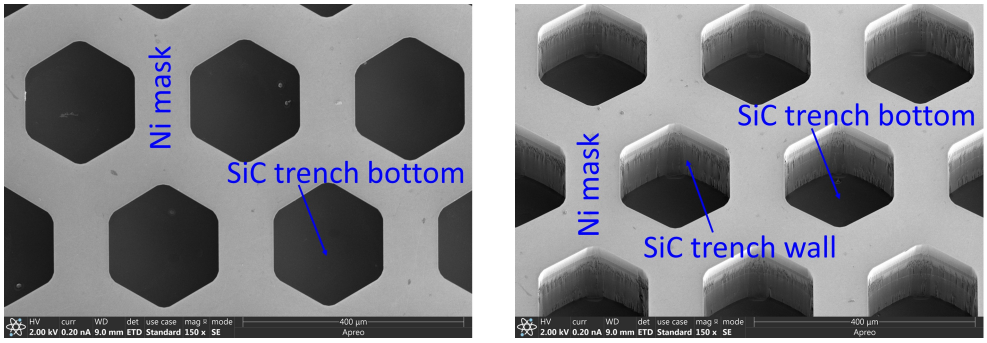
(b)

Figure 4.43. PU435Q3 processing: etch stop detection (a) I-V characteristics (b) Trench depth measurement using a Bruker profilometer after stripping the Ni mask.



(a) (b)

Figure 4.44. PU435Q3 processing: Images of the waffle patterns after stripping the Ni mask (a) Top of the fin (b) Bottom of the trench showing Ni residue.



(a) (b)

Figure 4.45. SEM images of the waffle patterns from a control sample processed together with PU435Q3 presenting (a) Top view (b) 30° tilted view.

4.3.13.4 Ohmic contact metallization

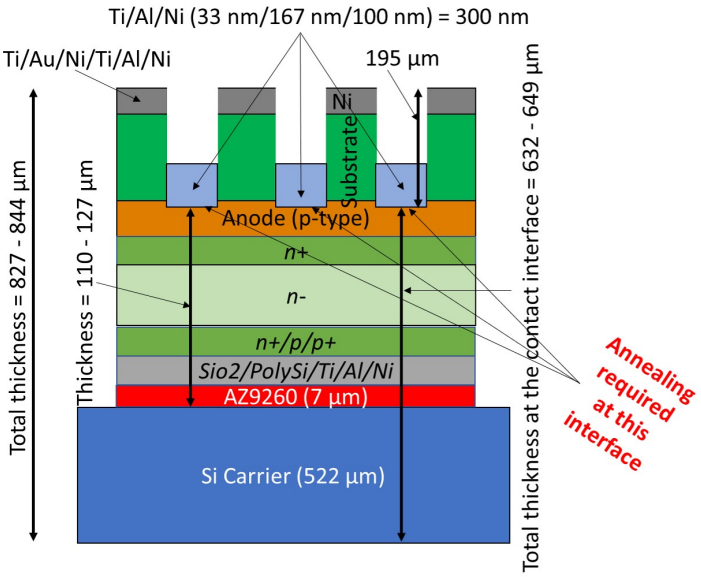
The metallization and the subsequent processing on the waffle substrate were executed one sample at a time. PU435Q2 went through a short RIE process in Jupiter II using SF_6 and Ar plasma at 100 W for 15 sec to roughen the surface for better adhesion. An oxygen plasma etch for 1 min was also executed in a Branson asher to remove any polymer that may form during SF_6 etch. Finally, a short 10 sec BOE dip was performed to remove any thin oxide, and the sample was loaded into the PVD1 metal deposition system where

33 nm Ti, 167 nm Al, and 100 nm Ni were deposited. It should be mentioned that the Ni mask from PU435Q2 was not stripped after the waffle etch. The same steps were followed for PU435Q3 after completion of fabrication process for PU435Q2. However, we did not verify the thickness of the individual metal layers in the stack for any of the samples.

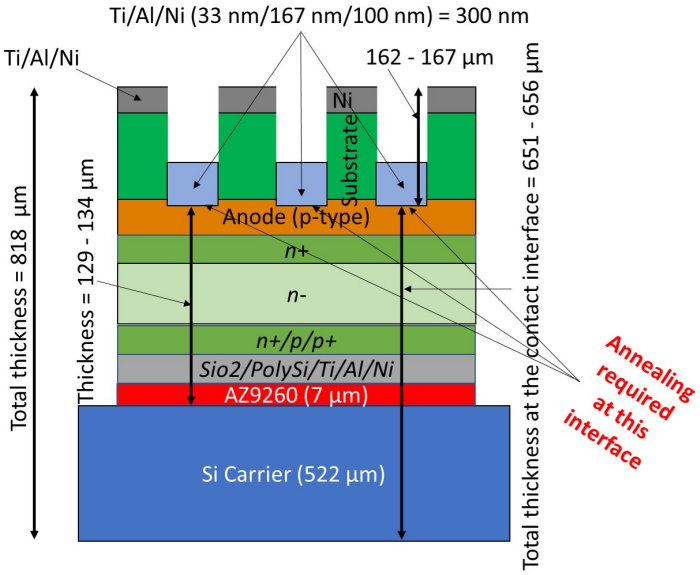
4.3.13.5 Laser annealing for ohmic contact formation

The ohmic contact anneal is an important step, particularly for SiC power devices. However, the waffle process removed a significant amount of SiC in the trenches, and approximately 121±8.5 μm of the epi layer was remaining. The rapid thermal cycling of an RTA process to form ohmic contacts on the mechanically weakened waffle substrate is very likely to break the wafer. Therefore, we chose to perform a laser anneal with the help of colleagues at Fraunhofer IISB in Germany who agreed to help us as a courtesy. First we performed a test run with a sample which had the same Al implant profile as the base contact region. Later we created TLM structures on the Si-face with a $p+$ contact metal stack, Ti/Al/Ni (33 nm/167 nm/120 nm). The sample was then laser annealed at Fraunhofer with typical anneal parameters including an energy density of 3.3 J/cm^2, a scan overlap of 67%, and a step overlap of 50% as described in [59]. After characterizing the TLM structure we found ohmic contact resistivity to be in the range of 2.43 - 6.56 $\times$ 10^{-2} Ωcm^2 with an average of 4.10 $\times$ 10^{-2} Ωcm^2, which is about 16.5 times higher than its RTA processed counterpart described in Section 4.3.10. Therefore we requested Fraunhofer to increase the power if possible for actual IGBT sample.

For ease of handling, the laser annealed samples were mounted on 4" Si wafers which were spin-coated with AZ9260 at 4000 rpm for 30 sec. After mounting the IGBT sample, the wafers were baked at 110°C for 3 minutes. The PR from the field area of the carrier wafer was cleaned by a cloth wipe soaked in acetone. For proper focus of the laser it was necessary to estimate the height of the surface where annealing is needed. Figure 4.46 shows a schematic cross section of PU435Q2 and PU435Q3 after mounting on their respective carrier wafers. The energy density of the laser was already at its maximum during the test run described above, so instead of increasing the power, the x and y overlaps were increased.



(a)

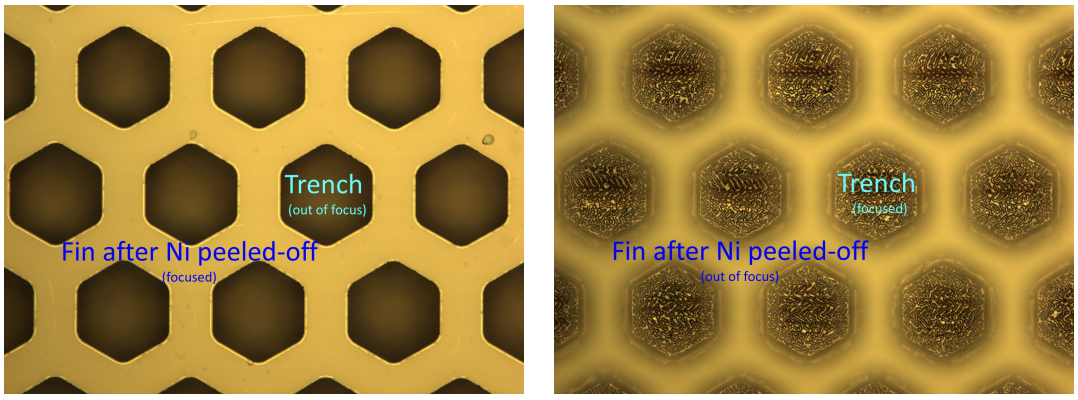


(b)

Figure 4.46. Schematic cross sections of the IGBT samples including layers and thicknesses after mounting on carrier wafers before laser annealing (a) PU435Q2 (b) PU435Q3.

The samples were sent separately to Fraunhofer to execute the laser annealing. Interestingly, the thick metal stack on the fin of PU435Q2 completely peeled off during the annealing process. Figures 4.47(a) and 4.48(b) show the fin as a smooth surface whereas the bottom

of the trench of PU435Q2 as a rough surface after laser annealing. The smoothness of the fin is due to the fact that nickel silicide did not form because the metal stack was too thick and out of focus to react with SiC.

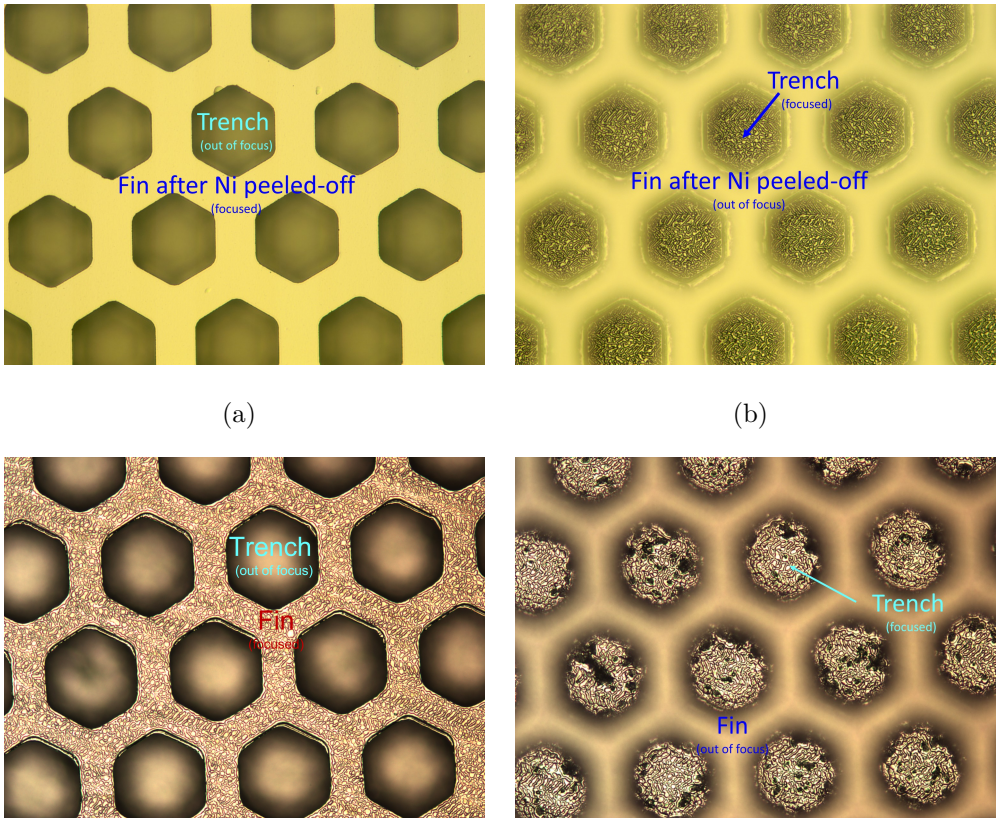


(a) (b)

Figure 4.47. Images from PU435Q2 after laser annealing to create ohmic contacts (a) Image focused at the top of the fin and (b) at the bottom of the trench.

4.3.13.6 Backside top metallization

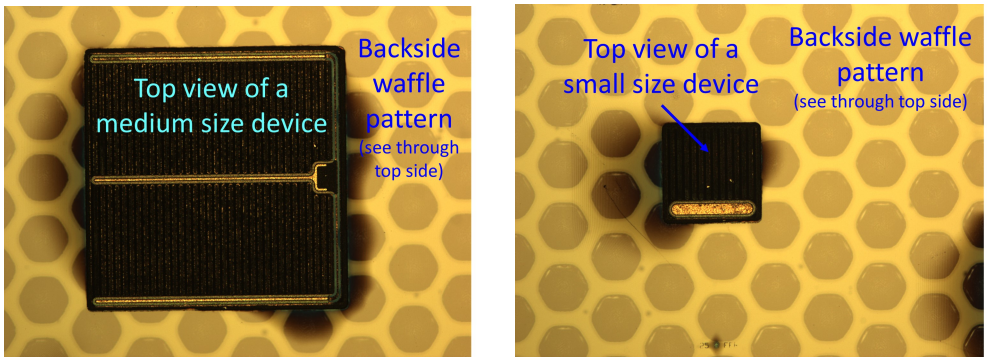
The final step is to deposit Al as a top metal on the back side of the waffle etched samples. The samples were cleaned in standard solvents and spin-coated the Si-face with a protective layer of AZ9260 using a standard recipe described previously. The samples were cleaned in a Branson asher using O_2 plasma at 100 W for 1 minute followed by a BOE dip for 10 sec. Aluminum was then deposited using the PVD sputtering system for 200 minutes with a deposition rate 2.6 nm/min leading to about 500 nm at a power of 350 W. The protective photoresist was stripped in remover PG, and the samples were complete and ready for characterization. Figure 4.48 shows images of the waffle pattern on both samples after laser annealing and top metal. An interesting image is presented in Fig. 4.49 where waffle patterns are clearly visible even from the Si-face of the sample because of its transparent nature.



(a) (b)

(c) (d)

Figure 4.48. Images after Al top metal sputtering on the laser annealed waffle structure. Focus on the (a) top of the fin of PU435Q2 (b) bottom of the trench of PU435Q2 (c) top of the fin of PU435Q3 (d) bottom of the trench of PU435Q3.



(a) (b)

Figure 4.49. Images of the waffle pattern from the top side of the wafer visible due to its transparency (a) A medium size device (b) A small size device.

5. EXPERIMENTAL RESULTS AND DISCUSSION

5.1 Electrical Characterization

Electrical characterization is planned to measure the on-state I-V characteristics, resistivity of the contacts, threshold voltage (V_{TH}), off-state blocking voltage, and minority carrier lifetime. The measurement and analysis techniques used along with the outcomes are discussed in the following sections.

5.1.1 *I-V* characteristics and differential specific-on resistance ($\Delta R_{ON,SP}$)

In the on-state, IGBT devices are typically operated in the linear region. We are interested to know the current at a given power dissipation. Although switching performance is an important matter, especially for a bipolar devices like the IGBT, we are interested primarily in its zero frequency (DC) performance in this project. A Keithley 4200 parameter analyzer was used to characterize the devices in the on-state. The output characteristics of an IGBT are defined as the collector current as a function of collector voltage for a given gate voltage as discussed in the following paragraphs.

On-state device performance of PU435Q2:

Sample PU435Q2 is an as-grown sample without lifetime enhancement. The I-V characteristics were measured using a Kelvin measurement configuration[60] in order to nullify the parasitic resistances in the measurement circuit. All the devices of this sample were characterized and it was found that several devices of all types and sizes worked except the large devices. A family of collector current vs. collector voltage curves for various gate biases is shown in Fig. 5.1. The measurement was conducted at room temperature (RT), and the applied maximum gate bias was 22 V corresponding to a gate oxide field of 4 MV/cm, which is considered to be the maximum electric field for long term oxide reliability[1]. The curves show the expected 3 V offset near the origin which comes from the forward voltage drop of the $p+$ anode - $n+$ buffer junction. The measurement was limited by the tool at a maximum current of 0.1 A. The differential specific on resistance ($\Delta R_{ON,SP}$) is calculated by taking the inverse slope of the curves in the linear region multiplied by the active area 1.05×10^{-2} cm^2.

The inverse slope is calculated by taking two data points in the linear region. In this case, the coordinates of data points A and B are (5.83, 47.6) and (6.19, 54.3) respectively. So, the calculated $\Delta R_{ON,SP}$ is 563.6 mΩ.cm^2 for V_G = 22 V.

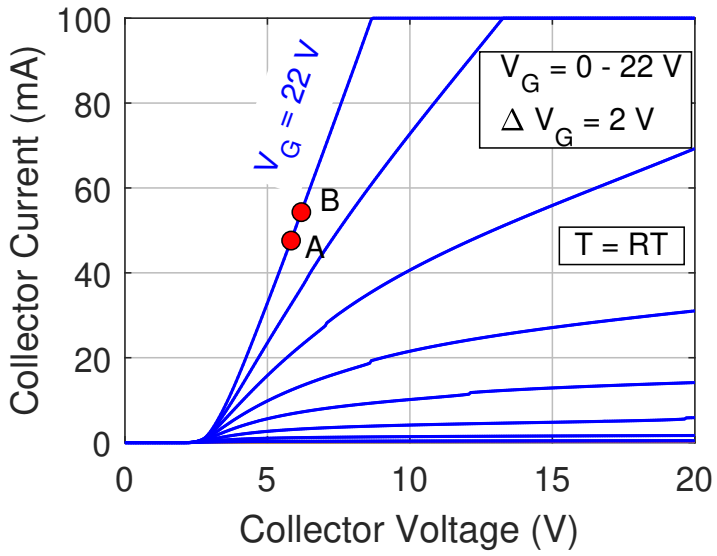


Figure 5.1. PU435Q2: Output characteristics (collector current vs. collector voltage) of a Medium Device C with area 1.05 $\times$ 10^{-2} cm^2. The gate voltage was stepped from 0 to 22 V with a 2 V increment. Data points A and B in the linear region are used to calculate the slope of the curve.

On-state device performance of PU435Q3:

Sample PU435Q3 is the carrier lifetime enhanced sample, and is expected to exhibit better performance than PU435Q2. Almost all the devices of this sample were characterized using a Kelvin probe setup, and several small devices of all types were found working, while only few type B medium size devices were functional. Unfortunately no large devices were found working. Figure 5.2 shows the measured output characteristics of a representative Medium Device B at room temperature. Once again the I-V curves indicate the classic functionality of an IGBT. The $\Delta R_{ON,SP}$ of this device is found to be 160 mΩ.cm^2 for V_G = 22 V which is a 3.5 fold improvement over PU435Q2.

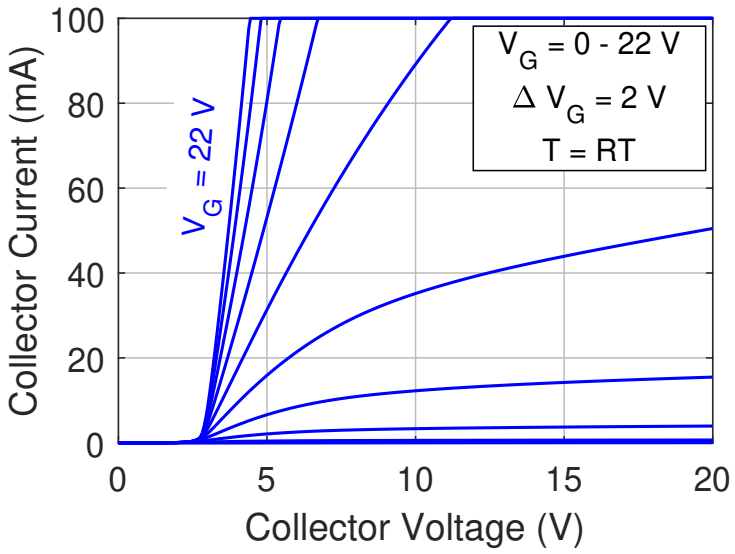


Figure 5.2. PU435Q3: Output characteristics (collector current vs. collector voltage) of a Medium Device B with area 1.15×10^{-2} cm^2. The gate voltage was stepped from 0 to 22 V with a 2 V increment.

5.1.2 Calculation of threshold voltage

The gate threshold voltage is an important parameter. It is calculated with the help of collector current vs. gate voltage ($I_C - V_G$) plot for a given collector voltage in the linear region of its output characteristics. It is commonly estimated by extrapolating a tangent on the $I_C - V_G$ curve where the transconductance $g_m = \partial I_C / \partial V_G$ is maximum[61]. Figure 5.3 presents a plot of $I_C - V_G$ curve along with $g_m - V_G$ in the secondary y axis. The threshold voltage is estimated by extrapolating a tangent line (red broken line) from the point where $g_{m,max} = 49.7$ μA/V to $I_C = 0$. Using this method the threshold voltage was found to be $V_{TH} = 8.5$ V.

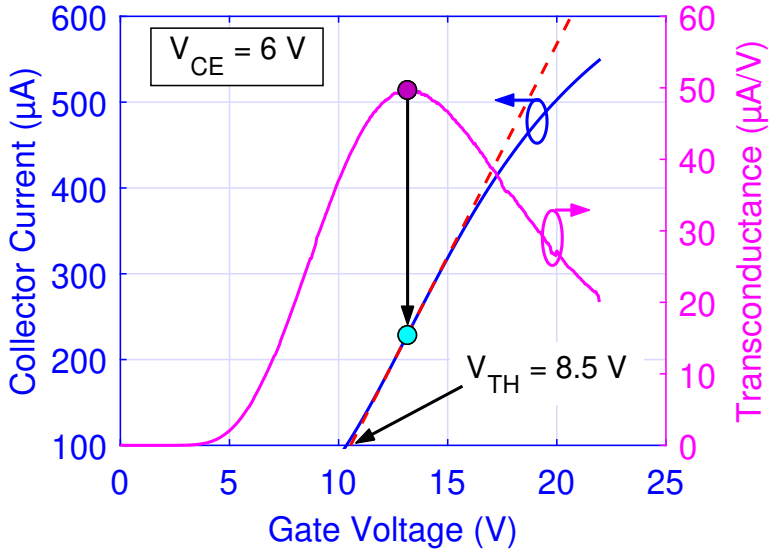


Figure 5.3. PU435Q2: Estimation of threshold voltage using a Small Device A.

Similarly, the threshold voltage was calculated using the $I_C - V_G$ curve of a Medium Device B of PU435Q3. In this case, we have considered $V_{CE} = 3$ V. Figure 5.4 shows the corresponding curves and the estimated threshold voltage was 8.5 V as in the case of PU435Q2.

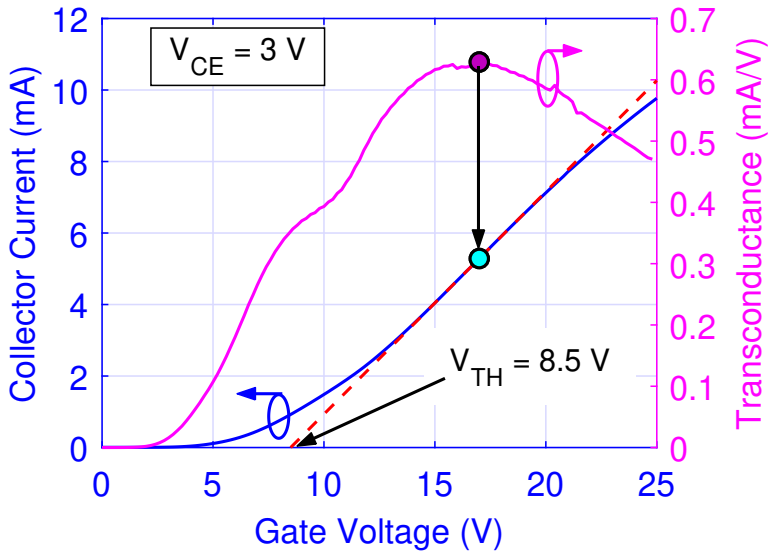


Figure 5.4. PU435Q3: Estimation of threshold voltage using a Medium Device B.

5.1.3 Measurement of contact resistivity

The resistance of the metal contacts are very important and required to be as low as possible in order to avoid a significant voltage drop across them. The parameter commonly used to characterize the resistance of metal contacts is the specific contact resistivity ρ_c which is the product of its resistance and area. We fabricated test structures to measure the specific contact resistivities of the $p+$ base contacts and $n+$ source contacts using the transfer length method (TLM)[43]. Figure 5.5 shows examples of the fabricated TLM test structures on both samples for both base and source contacts. The contact length L and width Z are annotated in Fig. 5.5(a), which were designed to be 50 μm and 100 μm respectively, although the fabricated structures deviated slightly from the design. First of all, it is important to check whether the contacts are ohmic or not by measuring the I-V characteristics between the contact pads. A representative I-V plot of each type of TLM structure is shown in Fig. 5.6. It is very clear from the linear nature of the I-V plots that all of them are ohmic.

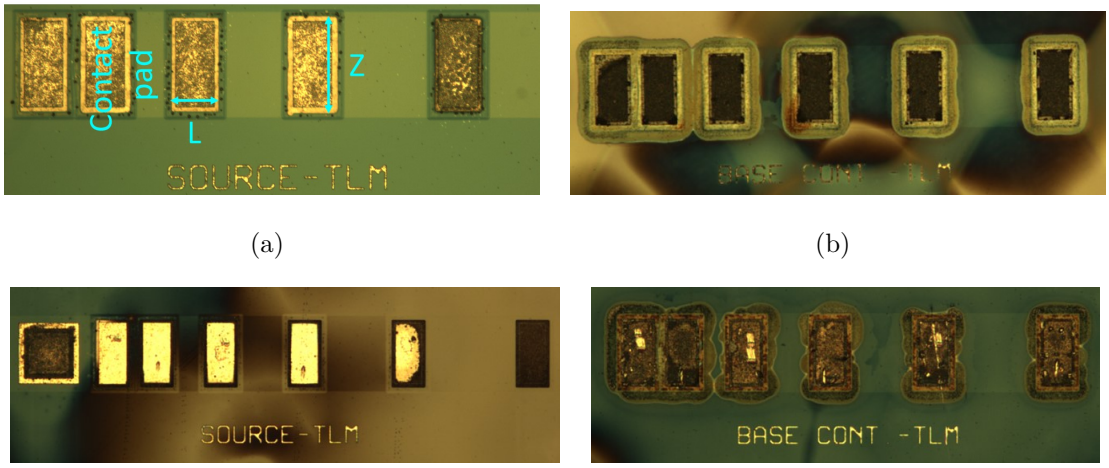


Figure 5.5. As fabricated TLM test structures for (a) Source contact of PU435Q2 with Z = 100 μm (b) Base contact of PU435Q2 with Z = 100 μm (c) Source contact of PU435Q3 with Z = 101 μm (d) Base contact of PU435Q3 with Z = 101 μm.

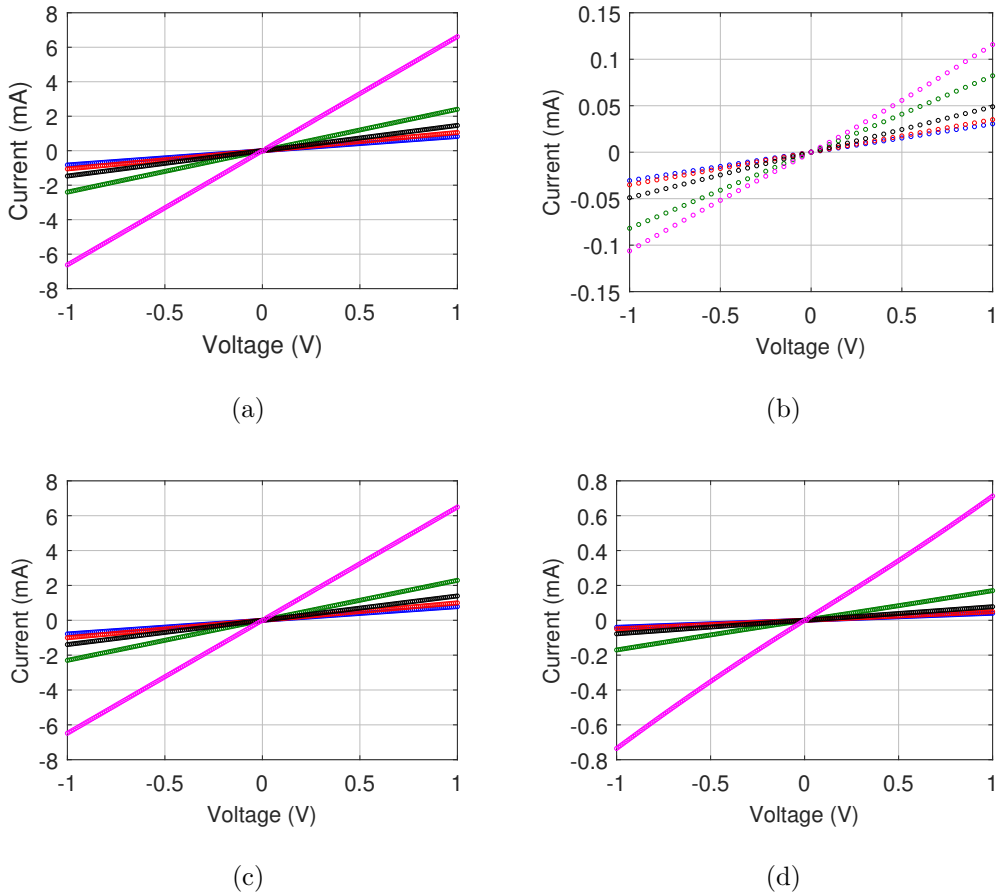


Figure 5.6. Plot of I-V data from adjacent contact pads of the TLM test structures for (a) Source contact of PU435Q2 (b) Base contact of PU435Q2 (c) Source contact of PU435Q3 (d) Base contact of PU435Q3.

The ρ_c is calculated by extracting contact resistance R_c, transfer length L_T, and the sheet resistance R_{sh} of the semiconductor layer underneath and between the contacts from a plot of total resistance as a function of distance between the contact pads.

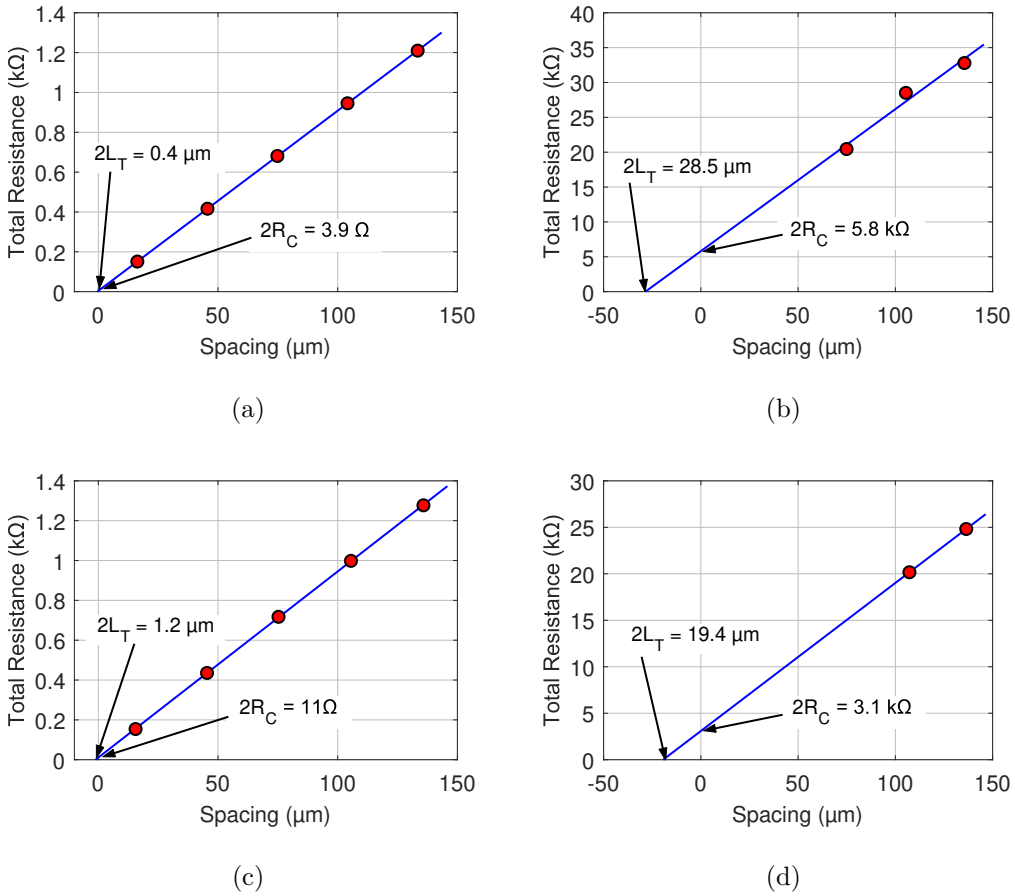


Figure 5.7. Plot of total resistance as a function of contact spacing in the TLM test structures for (a) Source contact of PU435Q2 (b) Base contact of PU435Q2 (c) Source contact of PU435Q3 (d) Base contact of PU435Q3.

Figure 5.7 shows four representative plots used to calculate ρ_c. Sheet resistance R_{sh} is calculated as a product of the slope and contact width Z. Finally, the equation $\rho_c = L_T^2 \times \mathrm{R}_{sh}$ leads to the specific contact resistivities of the respective contacts as shown in Table 5.1. It should be noted that base contact TLM data was fitted only for last 2 or 3 data points because first few metal pads seem to be shorted as can be seen from Figs. 5.5(b) and 5.5(d).

Table 5.1. Calculated specific contact resistivity of TLMs from Fig. 5.7

Contact Type	**TLM Width, Z (μm)**	**Contact Resistance, R_C (kΩ)**	**Transfer Length, L_T (μm)**	**Sheet Resistance, R_{sh} (kΩ/□)**	**Contact Resistivity, ρ_C (Ω.cm²)**
PU435Q2-Source	99.8	0.004	0.217	0.898	4.22×10^{-7}
PU435Q2-Base	99.7	5.807	14.254	20.309	4.13×10^{-2}
PU435Q3-Source	100.5	0.011	0.591	0.935	3.27×10^{-6}
PU435Q3-Base	101.2	3.088	9.693	16.115	1.51×10^{-2}

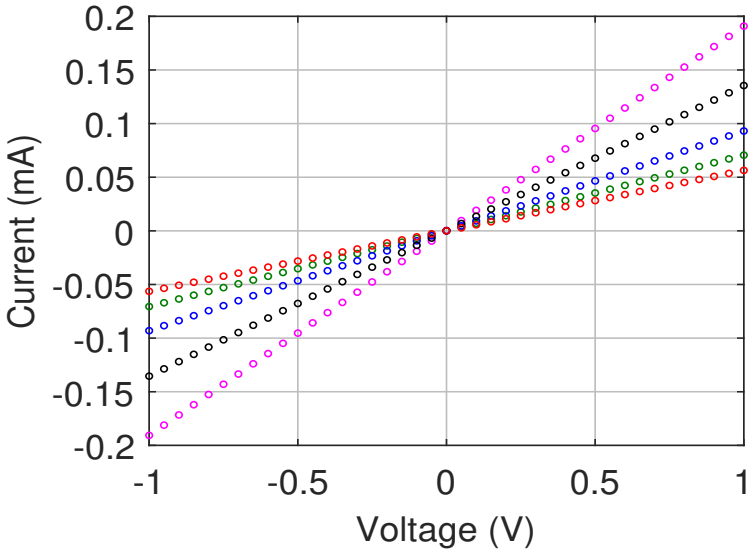
A few more TLMs were also characterized similarly and the average over the collected data is presented in Table 5.2. We found the source contacts significantly better than the base contacts. A quick calculation of the sheet resistance of the $n+$ implanted (source) layer underneath the source contact TLMs and the $p+$ implanted (base contact) layer underneath the base contact TLMs can be performed as follows. The implantation dose and thickness of the source layer are $dose = 4.86\times10^{14}$ cm^{-2} and $t = 222$ nm, which leads to the doping $N_s = dose/t = 2.19\times10^{14}$ cm^{-2} as given in Section 4.3.6. The mobility of this layer becomes $\mu_N = 60.5$ cm^{2}V^{-1}s^{-1} as per Eq. 3.30 leading to the sheet resistance of the layer $R_{sh} = 1/(q\mu_N N_s t) = 212\ \Omega/\square$. This is about 4 times lower than the average value presented in Table 5.2. Now, the actual thickness of the source layer could be much lower than 222 nm because the sample went through several oxidation processes such as sacrificial oxide for $p+$ layer implantation, post-implant anneal oxidation, field oxide formation, gate oxide and ILD formation. All these steps should have consumed a significant amount of SiC leading to a shallower source layer. Moreover, the doping concentration near the source-base junction

is lower and affects the sheet resistance. Considering these two factors, the measured sheet resistance of the $n+$ source layer is indeed reasonable.

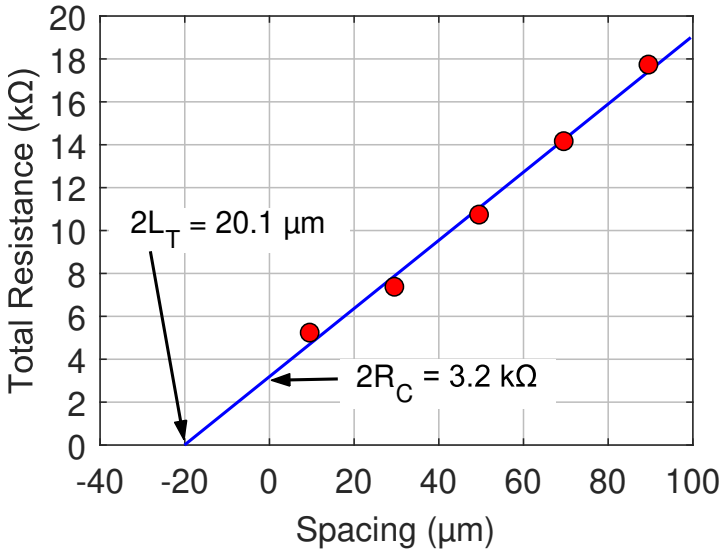
Table 5.2. Mean specific contact resistivity over all measured TLMs.

Contact Type	**Mean L_T (μm)**	**Mean R_{sh} (kΩ/□)**	**Minimum ρ_C (Ω.cm²)**	**Maximum ρ_C (Ω.cm²)**	**Mean ρ_C (Ω.cm²)**
PU435Q2-Source	0.668	0.918	4.22×10^{-7}	2.07×10^{-5}	7.34×10^{-6}
PU435Q2-Base	51.542	13.881	4.13×10^{-2}	7.59×10^{-1}	3.73×10^{-1}
PU435Q3-Source	0.748	0.945	3.27×10^{-6}	7.82×10^{-6}	5.55×10^{-6}
PU435Q3-Base	7.524	16.292	4.72×10^{-3}	1.51×10^{-2}	9.93×10^{-3}

We conducted an experiment to measure the ρ_c of a laser annealed p-type contact by fabricating TLMs on the Si-face in order to estimate the specific contact resistivity of the waffle patterns on the C-face. The test samples were blanket $p+$ implanted during the actual IGBT $p+$ base contact implantation. We conducted this experiment with on the Si-face for several reasons. First of all, C-face $p+$ substrates and/or epilayers are not readily available, and the processing would require a deep etching to isolate a thick $p+$ mesa in order to fabricate effective TLM structures. In addition, the implanted samples had a shallow $p+$ implant which is easily isolated with a shallow mesa etch. Figure 4.17(b) shows that the $p+$ layer has about 286 nm box profile with doping 1.4×10^{19} cm^{-3} whereas the $p+$ anode layer has a doping 1.5×10^{19} cm^{-3} with thickness 40 μm. Since the doping of the anode layer in the actual sample is very close to that of the test samples, the only significant difference between the test and IGBT samples is that the former is on the Si-face and the latter on the C-face.



(a)



(b)

Figure 5.8. Specific contact resistivity of laser annealed contacts on an implanted p-type layer: (a) I-V curve of the adjacent contact pads of a TLM structure (b) Plot of total resistance as a function of contact spacing of TLM structures.

Figure 5.8 shows an example of the data and analysis from one such TLM where the contact width Z was 152 μm. The ρ_c was calculated to be 2.43×10^{-2} Ω.cm^2. Several other TLMs were also characterized and the ρ_c was found to be in the range of 2.43×10^{-2} -

6.56×10^{-2} Ω.cm^2 with an average 4.10×10^{-2} Ω.cm^2. We also experimented with a similar sample using rapid thermal annealing at 1000°C for 2 min in Ar ambient at Jipelec RTA. The resulting ρ_c was in the range 1.28×10^{-3} - 7.63×10^{-3} Ω.cm^2 with an average 2.48×10^{-3} Ω.cm^2. The RTA process gave 16.5 fold improvement in contact resistivity compared to the laser anneal process on the Si-face.

5.1.4 Gate oxide thickness measurements through *C-V* analysis

Several MOSCAPs were included in the mask set as described in subsection 4.1.2. High frequency C-V characterization of a MOSCAP on the gate structure was performed using Keithley 4200 parameter analyzer. The gate oxide was fabricated on a 222 nm thick $n+$ source implanted region having a doping 2.2×10^{19} cm^{-3} and a standard phosphorus doped 500 nm thick polysilicon on top of it. The purpose of this characterization was to estimate the thickness of the gate oxide. Figure 5.9 shows an image of a fabricated MOSCAP with diameter 440 µm. The MOSCAP pad was grounded while the DC bias was swept from -20 V to +20 V on the $n+$ contact pad with a small 30 mV ac signal

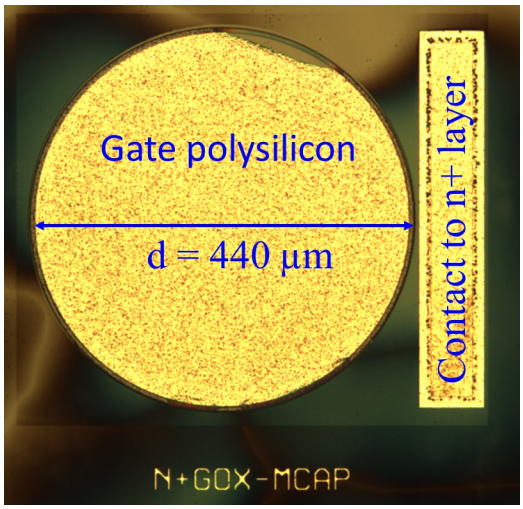


Figure 5.9. As fabricated MOSCAP on the $n+$ source implanted region with the standard doped polysilicon on NO annealed thermal oxide gate stack.

of 100 kHz. The high frequency $C-V$ curve is shown in Fig. 5.10 for PU435Q2 and PU435Q3. The area (A) of the MOSCAP is 1.52×10^{-3} cm^2 and the oxide permitivity is assumed to be

3.45×10^{-11} F/cm, based on the ideal value for silicon dioxde. The oxide capacitance (C_{OX}) of the MOSCAPs can be estimated from the maximum capacitance in the accumulation region as annotated in Fig. 5.10. The oxide thickness $t_{OX} = (\varepsilon_s.\mathrm{A})/C_{OX}$ equation leads to an estimated oxide thickness of 54 nm and 51 nm respectively.

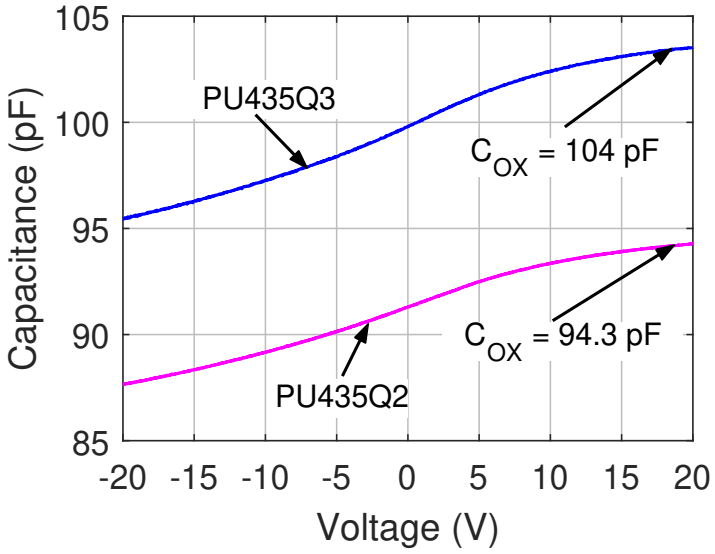


Figure 5.10. High frequency (100 kHz) $C-V$ characteristics of MOSCAPs having a gate stack fabricated on the $n+$ source implanted region with the standard doped polysilicon on NO annealed thermal oxide gate stack.

5.1.5 Carrier lifetime measurements

Carrier lifetime in an IGBT plays an important role: a longer lifetime would increase the fraction of injected minority carriers which diffuse through the drift layer without recombining, and thus would increase its conductivity. We planned to measure carrier lifetime in two samples, with and without a lifetime enhancement procedure. We were graciously offered assistance with lifetime measurements by Dr. Robert Stahlbush's group at the Naval Research Laboratory. The first and fourth quarters of PU435 were sent to them for the characterization. Sample PU435Q1 was treated with a lifetime enhancement process as described in Section 4.3.1, while PU435Q4 was measured as-grown, without lifetime enhancement.

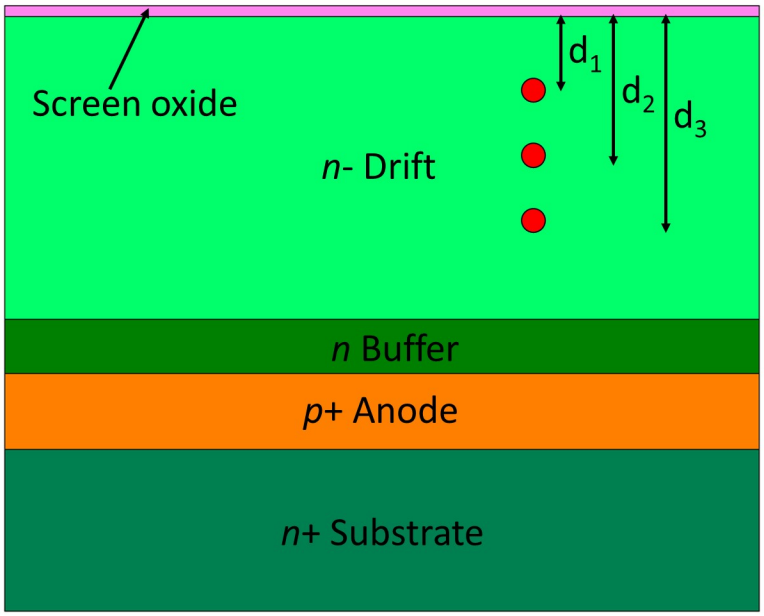


Figure 5.11. The cross section of the sample for lifetime measurement at three depths (red dots) $d_1 = 20$ μm, $d_2 = 40$ μm, and $d_3 = 60$ μm inside the drift layer.

Figure 5.11 shows a cross section of the samples with a thin screen oxide on the top. The measurement was conducted by the team for the depths of $d_1 = 20$ μm, $d_2 = 40$ μm, and $d_3 = 60$ μm from the surface. The target depths were excited by two photons generated by a 586 nm laser, and a photoluminescence (PL) decay signal was recorded and later fitted with an appropriate exponential function. A TRPL decay curve is a plot of PL intensity as a function of time. An inverse slope is calculated from the decay curve with the formula inverse slope $= (t_2\text{-}t_1)/\ln(y_2/y_1)$ and plotted as a function of time. Figure 5.12 shows the measured/estimated data at $d_1 = 20$ μm from the surface. The inverse slope is plotted in Fig. 5.12 (b) for the early part of the TRPL data ($\leq$0.5 μs) whereas the later part is plotted in Fig. 5.12 (d). The whole analysis process is well described in [62]. This result was analyzed using a formalism proposed in [63], where the TRPL data is curve fit to an analytical model which is used to extract model parameters. The model is then used to construct a plot of inverse slope as a function of time, from which the effective lifetime τ_{eff} is extracted. This procedure estimated the lifetimes to be 1 μs and 4 μs in PU435Q4 and

PU435Q1, respectively at a depth of $d_1 = 20$ μm. Following the same procedure, it was concluded the lifetimes at $d_2 = 40$ μm and $d_3 = 60$ μm are exactly the same.

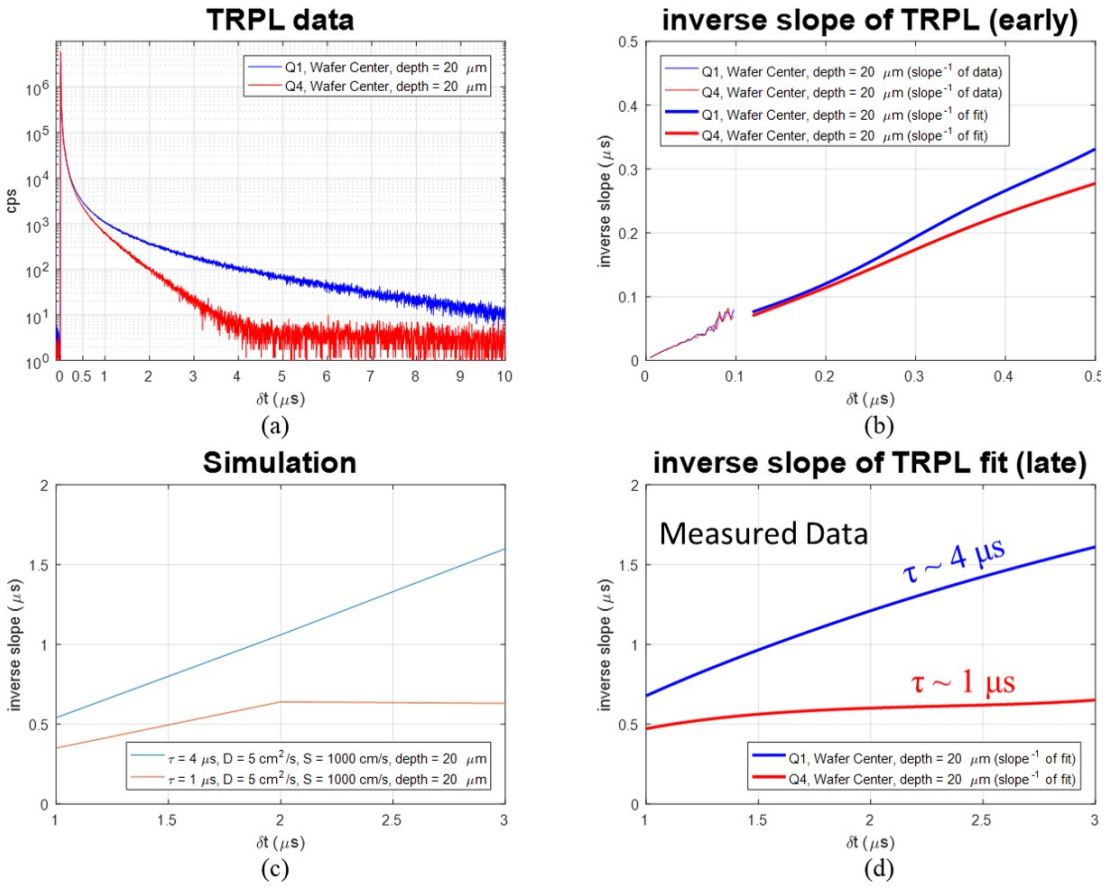


Figure 5.12. Lifetime measurement data at a depth of $d_1 = 20$ μm (a) TRPL decay data (b) Plot of inverse slope in the early part of the TRPL decay (c) Plot of inverse slope by simulation (d) Plot of inverse slope in the later part of the TRPL decay.

It is interesting to note that the same recipe of carbon implantation followed by a high temperature annealing resulted an increase of carrier lifetime from 2 μs to 13 μs in the work reported in [44]. The effective lifetime models described in [34] and [35] can be used to explain the difference.

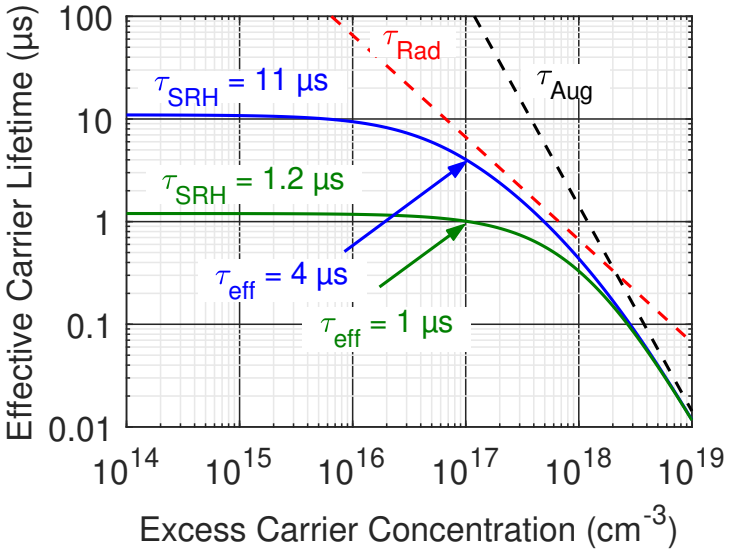


Figure 5.13. Lifetime model indicating effective lifetimes 1 µs and 4 µs at an assumed excess carrier concentration 1×10^{17} cm^{-3} at room temperature [35].

Figure 5.13 shows an effective lifetime plot as a function of excess carrier concentration. The effective lifetime is calculated using the Matthiessen rule where three major processes are responsible in 4H-SiC such as Shockley-Read-Hall(SRH), Radiative recombination and Auger. Figure 5.13 indicates that radiative recombination becomes dominant for excess carrier concentration $> 1\times10^{16}$ cm^{-3} and the effect of Auger process is negligible while SRH dominates at low concentration level. So, depending on the carrier injection level the reported effective lifetime can be very different. However, the lifetime enhancement procedure was successful to reduce the carbon vacancy as deep as was measured.

5.1.6 Comparative study of as-designed and as-measured Δ $R_{ON,SP}$

The IGBTs were designed based on the expected on- and off-state performance predicted by TCAD simulations. The measured effective lifetimes reported in Section 5.1.5 were considered in the simulation. In order to match up the measured lifetimes, we assumed τ_{SRH} to be 1.2 µs for the non-enhanced sample, and 11 µs for the enhanced sample, so that the effective lifetimes become 1 µs and 4 µs respectively for PU435Q2 and PU435Q3 at an excess carrier concentration of 1×10^{17} cm^{-3}. Higher concentrations are not reasonable to consider

because the effective lifetimes coincide irrespective of low level lifetime, and 4 μs may not even be possible. Figure 5.13 depicts the effective lifetime as a function of excess carrier concentration considering the three most important recombination mechanisms.

Table 5.3. Parameters used in TCAD simulations.

	Device C - PU435Q2		**Device B - PU435Q3**	
Parameter	**Designed**	**Fabricated**	**Designed**	**Fabricated**
JFET (μm)	5.00	4.20	3.00	2.52
Channel (nm)	500	623	500	570
$\rho_{C,Base}$ (Ω.cm^2)	Negligible	3.73×10^{-1}	Negligible	9.93×10^{-3}
$\rho_{C,Source}$ (Ω.cm^2)	Negligible	7.34×10^{-6}	Negligible	5.55×10^{-6}
$\rho_{C,Waffle}$ (Ω.cm^2)	Negligible	9.23×10^{-2}	Negligible	9.23×10^{-2}
τ_{eff} (μs)	5	1	5	4

The on-state simulations were performed before the fabrication with some best-guess ideal parameters, and after fabrication with parameters extracted from actual measurements to compare the simulated performance with the characterized devices as illustrated in Section 5.1.1. Table 5.3 presents the parameters used in the TCAD simulations to predict the I-V characteristics in the on-state. The fabricated parameters were obtained by taking the average of data collected from many devices. However, the contact resistivity of the waffle substrate is estimated based on the available data of the test run described in Section 5.1.3. The average ρ_C of a planar p-type surface annealed by laser was estimated as $\rho_{C,Planar} = 4.10\times10^{-2}$ Ω.cm^2. However, we did not have any means to measure the contact resistivity of the waffle structure on the back side of the wafer. Therefore, the estimated planar contact resistivity was used with a proper correction factor based on the area of the etched portions

of the waffle patterns, because only these regions had an ohmic contact to the collector region. Figure 5.14 shows a part of the waffle mask with various relevant dimensions where the side of the regular hexagon is a = 115.47 μm, leading to the area of a single hexagon of $A_h = (3\sqrt{3}/2)*a^2 = 3.46\times10^{-4}$ cm^2. For simplicity, let us consider an waffle mask of dimension 90 mm×77.94 mm so that 300 hexagons (90 mm/300 μm and/or 77.94 mm/259.8 μm) can fit in x and y directions. So, the area of the hexagonal waffle patterns becomes $A_H = A_h*300^2$ = 31.14 cm^2 whereas the total area is A_T = 90*77.94/100 = 70.15 cm^2. Thus the area correction factor $A_{cf} = A_T/A_H$ = 2.25 leads to the estimated contact resistivity as $\rho_{C,Waffle} = A_{cf}*\rho_{C,Planar} = 9.23\times10^{-2}$ Ω.cm^2.

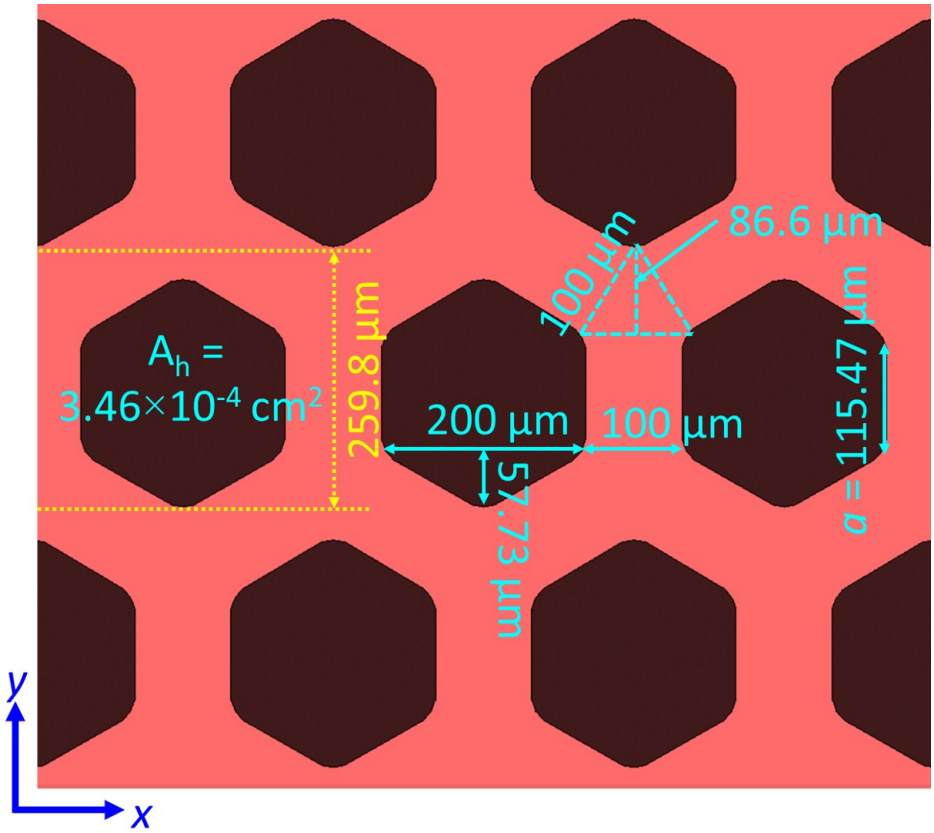


Figure 5.14. A part of the hexagonal waffle mask with various dimensions.

A comparison of the simulated and measured I-V curve of a Medium Device C from PU435Q2 is presented in Fig. 5.15. The simulation parameters are shown in Table 5.3. The expected $\Delta R_{ON,SP}$ of the as-designed and as-fabricated devices were found through

simulation to be 15 mΩ.cm^2 and 94.2 mΩ.cm^2, respectively, whereas the actual measured $\Delta R_{ON,SP}$ was 563.6 mΩ.cm^2. It is interesting to note that the $\Delta R_{ON,SP}$ extracted from the simulation based on as-fabricated parameters is almost the same as the expected contact resistivity of the waffle substrate. However, the actual measured $\Delta R_{ON,SP}$ is 6 times higher than its simulation counterpart. Although there was no provision of measuring the contact resistivity of the waffle from the actual sample, the following argument could explain the results. An important factor in laser annealing is to have an accurate knowledge of the height of the surface where annealing is required. The advantage of laser annealing is its ability to generate extremely localized heating, unlike global heating in an RTA. This requires a precise focusing to provide the maximum energy at the spot of interest[59]. If the target spot is out of focus, the energy will be distributed over a much larger area, leading to a lower energy density and thus lower peak temperature. For PU435Q2, the estimated height of the ohmic metal-*p*-anode interface as shown in Fig. 4.46(a) had a wide range of 110 - 127 µm. Therefore it is reasonable to assume that if the laser was not properly focused on the bottom of the waffle pockets the contacts would have been insufficiently annealed, leading to a much higher contact resistivity and consequently a much higher $\Delta R_{ON,SP}$ than expected.

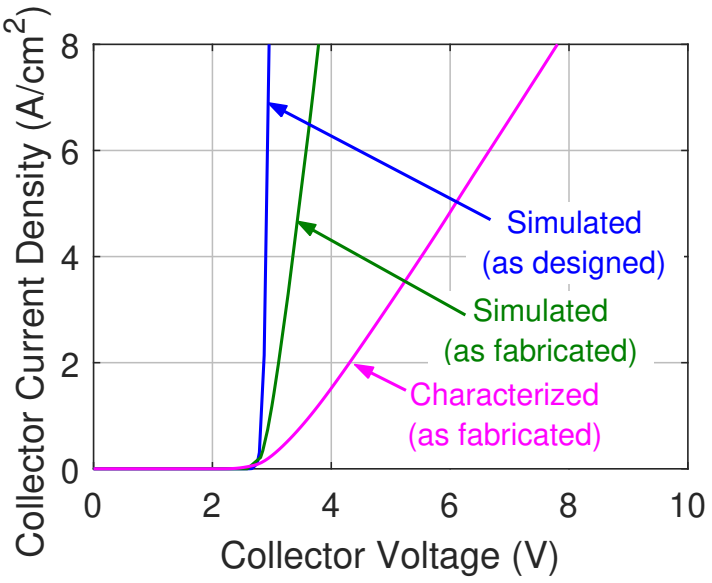


Figure 5.15. Comparison of output characteristics between simulated and measured Medium Device C from PU435Q2 measured at room temperature.

A similar comparative study is shown in Fig. 5.16 for a Medium Device B of PU435Q3. In this case, the ideal $\Delta R_{ON,SP}$ is 11 mΩ.cm^2 which is lower than PU435Q2 as expected because of its relatively long ambipolar (effective) carrier lifetime. The simulation assuming as-fabricated parameters predicts a $\Delta R_{ON,SP}$ of 99.7 mΩ.cm^2, while the actual measured value was 160 mΩ.cm^2. This time the range of estimated interface height for laser annealing was much narrower, possibly leading to a better ohmic contact. However, there is still a significant difference between the simulated and the measured value. Figure 4.44(b) shows some residue at the bottom of the trench which was severe in some other parts of the sample (not shown in the image). This may result in a smaller than intended contact area and lead to this remaining difference.

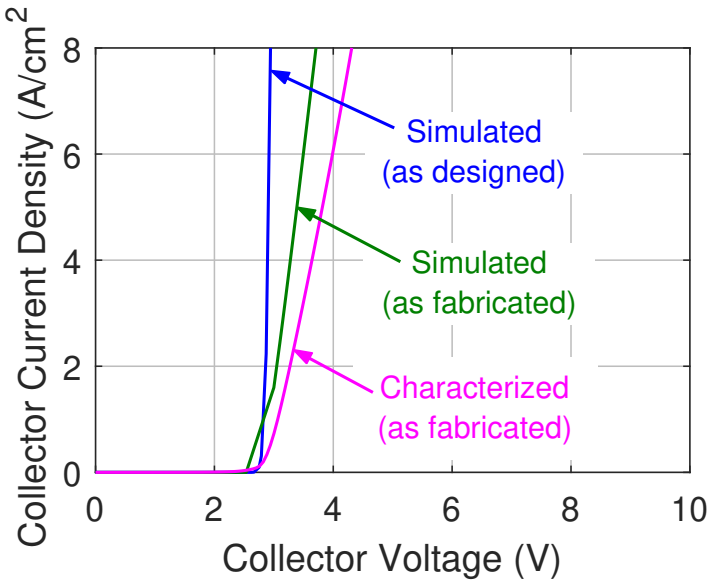


Figure 5.16. Comparison of output characteristics between simulated and measured Medium Device B from PU435Q3 measured at room temperature.

It is worth mentioning that an optimized 12.5 kV DMOSFET corresponds to a specific on resistance of the drift layer as 67.5 mΩ.cm^2 and 207.4 mΩ.cm^2 at 27 °C and 175 °C calculated by using the analytical formula $R_{ON,SP} = 2.8\times10^{-8}*(T/300)^{2.8}*V_{BR}^{2.29}$ [1]. An IGBT is expected to show the same $\Delta R_{ON,SP}$ at high temperature as at low temperature. So, in spite of having high back side contact resistivity the fabricated IGBT in PU435Q3 performs better than its DMOSFET counterpart at elevated temperature although the DMOS-

FET does not have initial 3 V offset. Moreover, the specific resistivity of the drift region without any conductivity modulation can be calculated using the analytical formula $R_{DR,SP} = [1/(q\mu_N N_D)]^*[S\ln(1 + \frac{S-L_j/2+x_{dj}}{L_j/2-x_{dj}}) + (t_d - S + L_j/2 - 2x_{dj})]$ [52]. Here, the drift thickness $t_d = 75$ μm, doping $N_D = 1.8\times10^{14}$ cm^{-3}, JFET length $L_J = 3$ μm, half cell pitch $S = 21.5$ μm and x_{dj} the depletion width between the p-well and JFET. The dopings in the JFET and p-well are $N_j = 1.5\times10^{16}$ cm^{-3} and $N_b = 3\times10^{17}$ cm^{-3} as shown in Figs. 4.9 and 4.11(b) leads to a built-in potential $V_{bi} = 3.05$ V and $x_{dj} = 0.47$ μm using standard formula and parameters. Hence, the $R_{DR,SP}$ becomes 368 mΩ.cm^2. Therefore, despite the fact that the specific on-resistance is higher than expected from simulation, it is significantly lower than would be expected without conductivity modulation. The device clearly is behaving as an IGBT with significant conductivity modulation of the drift layer, although contact and perhaps other parasitic resistances are limiting its performance to some extent.

5.1.7 Breakdown voltage measurements

The IGBTs in this study were designed for an ideal parallel plane blocking voltage 12.5 kV, with a rating of 10 kV achievable in reality with the help of a floating field ring edge termination. We utilized a high voltage Spellmann SL30 DC power supply capable of 40 kV, an SMU to supply gate voltage, a bidirectional surge protecting diode, a 100 kΩ resistor and an HP 3478A digital multimeter (DMM) to construct the circuit shown in Fig. 5.17 and measure the blocking voltage of the IGBT. The high voltage power supply is limited to a maximum 0.8 mA current, above which it turns the voltage supply off to protect itself. The digital multi-meter (DMM) was used to measure the voltage V_R accross the series resistor R_S so that ohm's law gives the current $I_R = V_R/R_S$. The purpose of the bidirectional surge protecting diode was to clamp the voltage at a maximum of 100 V to protect the DMM when device breakdown occurs. The waffle side (Terminal C) of the IGBT sample was bonded on a gold coated Si sample with a flash dry silver conductive paint and submerged in Fluorinert contained shallow plastic box. This chemical is a strong insulator, and prevents any possible arcing in the air above the device due to the high lateral voltage drops at the edge of the devices. The box is placed on the chuck of Cascade MPS150 DC probe station and the

output of the HV supply was fed to the carrier wafer through a high voltage probe arm. The gate voltage is supplied from an external SMU to the gate terminal (G) and the ground of the unit is connected to the emitter (E) of the device. One terminal of the surge protection diode, resistor, and DMM are connected to the emitter as shown in the diagram, and the other terminals were connected to the ground of the HV supply. The external SMU output was set to $V_{GE} = 0$ V for the off-state breakdown measurement as the threshold voltage was measured in the on-state as 8.5 V. The actual voltage across the device would be V_C-V_R.

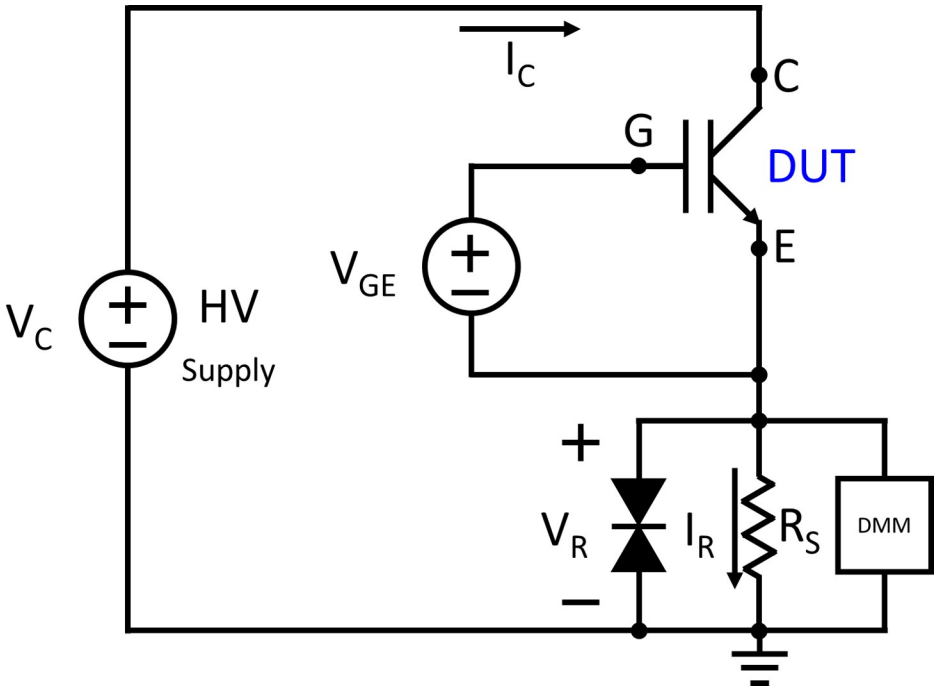
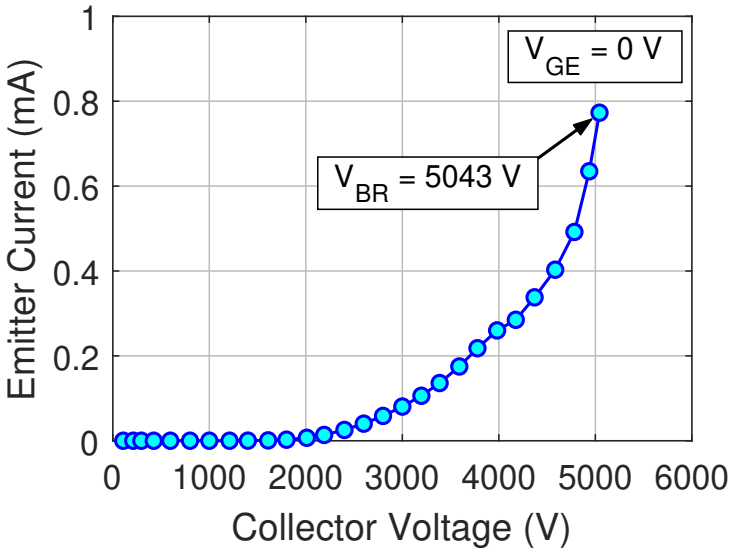
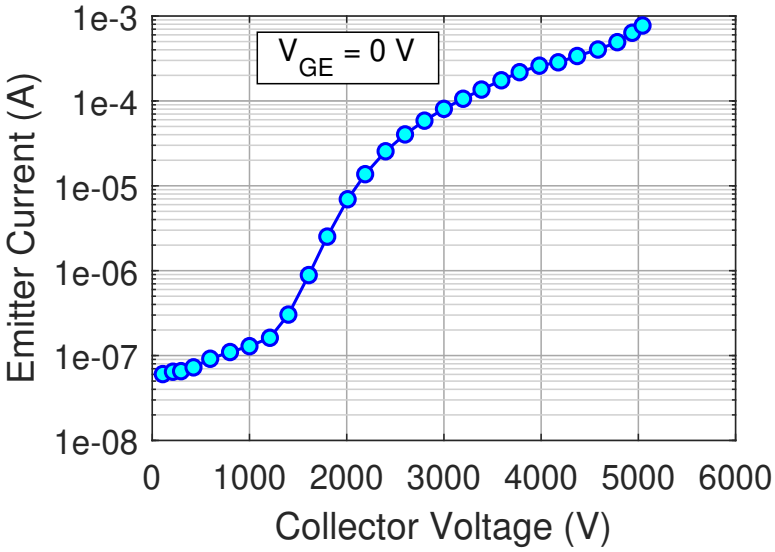


Figure 5.17. Circuit diagram of the IGBT blocking voltage measurement setup.

We attempted to measure many devices with FFR edge termination, and Fig. 5.18 shows the off-state I-V characteristics of a Small Device B from PU435Q2. The emitter current was recorded and plotted in this figure, rather than the collector current. However, as long as there is no significant leakage current flowing through the gate, the collector and emitter currents should be equal. The measurement was conducted in the dark by closing the box of the probe station.



(a)

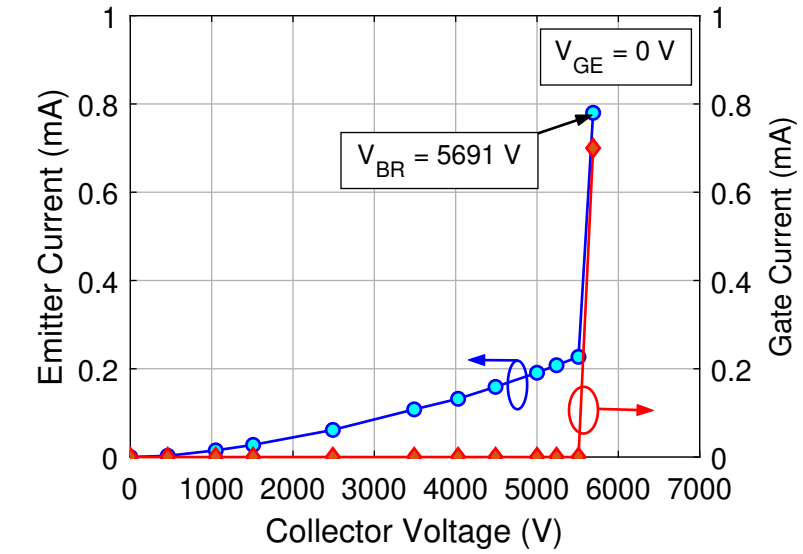


(b)

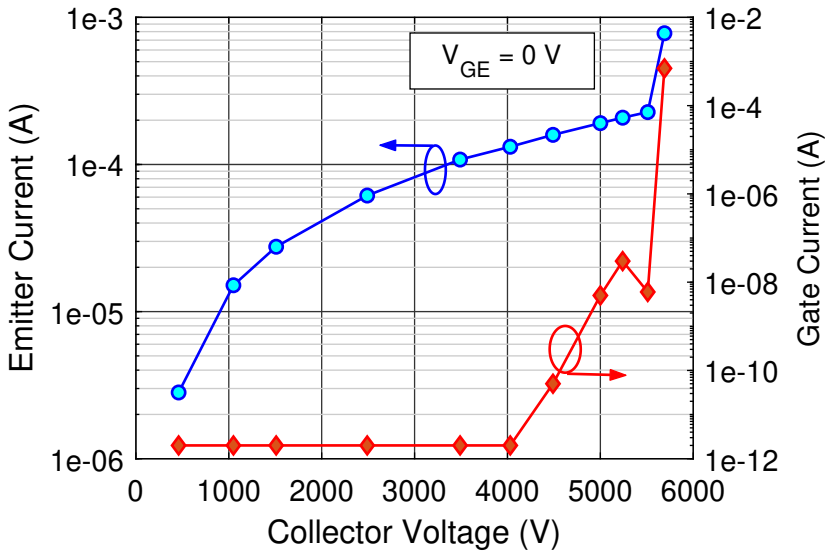
Figure 5.18. PU435Q2: Off-state I-V characteristics (emitter current vs. collector voltage) at $V_{GE} = 0$ V (a) Linear scale (b) Logarithmic scale.

The curves show a slow rise in current from 60 nA to 0.8 mA as the collector voltage was increased. As soon as the collector current reached at 0.8 mA for $V_{CE} = 5043$ V, the HV supply unit turned-off its supply and we could not proceed to higher voltage. The gradual increase in leakage current is not consistent with avalanche breakdown. Instead a sudden

increase of gate current was observed, indicating a gate oxide failure. Unfortunately, the gate current was not recorded to present for this sample. However, PU435Q3 gives us more insight about the phenomenon.



(a)

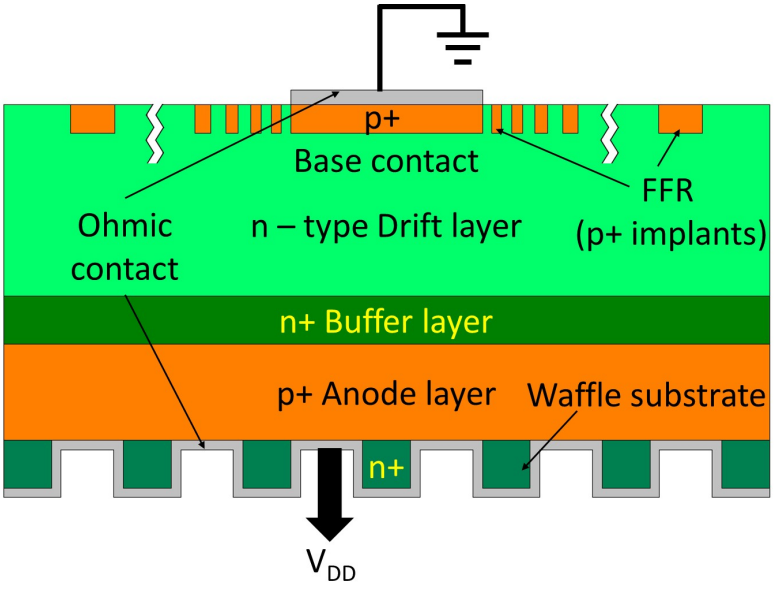


(b)

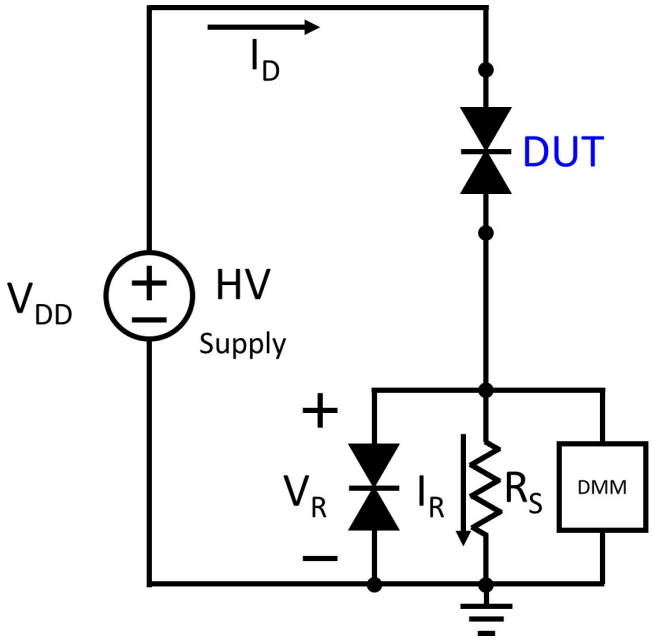
Figure 5.19. PU435Q3: Off-state I-V characteristics at $V_{GE} = 0$ V (a) Linear scale (b) Logarithmic scale.

Similarly, many edge terminated devices of PU435Q3 were characterized using the circuit diagram shown in Fig. 5.17. This time, the gate current was also observed and recorded, and again the gate voltage V_{GE} was set to 0 V. Figure 5.19 shows a plot of emitter current as a function of collector voltage in the off-state. A gradual increase in current was observed, but a sudden rise of gate current led to HV supply shut down due to its maximum current limit. Figure 5.19(a) shows that the total current measured through the series resistor is almost same as the gate current above a collector voltage of about 5.5 kV. The circuit setup was not capable of conclusively determining whether the short happened between gate and emitter or between gate and collector due to oxide breakdown. The maximum applied voltage was recorded as 5691 V but the device was clearly not in avalanche breakdown. It should be noted that the JFET region was deliberately made wider than optimal in order to fabricate the devices primarily by contact photolithography. One possible explanation is that the shielding of the oxide by the closely spaced p-wells on either side of the JFET region was not as effective in reality as was expected from simulations where we observed that at $V_{BR} = 12.5$ kV the maximum oxide electric field was 5 MV/cm.

Although the main goal was to measure the blocking capability of the edge terminated IGBTs, several edge terminated diodes were also fabricated on the same samples as the IGBTs. Figure 5.20 presents a schematic cross section of the diode and the circuit setup used to measure the blocking voltage. The cross section shows the diode is actually two back-to-back p-n junctions in series, specifically the Anode-Buffer (p+n+) junction and the Drift-Base Contact (n-p+) junction. The back side was connected to the HV supply V_{DD}, which would make Anode-Buffer junction forward biased and Drift-Base Contact junction reverse biased. Therefore, the junction of interest is Drift-Base Contact to observe avalanche breakdown with a functional edge termination as shown. This should represent the blocking capability of the IGBTs because they have the same drift layer, but one notable difference is that the avalanche breakdown in an IGBT is expected to happen at Drift-Base junction.



(a)



(b)

Figure 5.20. (a) A schematic cross section of edge terminated diode (b) Circuit setup to measure the breakdown voltage of the diode.

The I-V characteristics of a representative diode is shown in the plot of Fig. 5.21. The last data point in the plot represents the avalanche breakdown point i.e. $V_{BR} = 9020$ V. A

slight increment of the applied voltage beyond this point caused an abrupt increase in the current, and the HV supply turned itself off. Although it is not possible to infer from this plot whether the avalanche happened in the diode itself or somewhere in the edge termination area, it can be said that the edge termination design is at least capable of withstanding 9 kV.

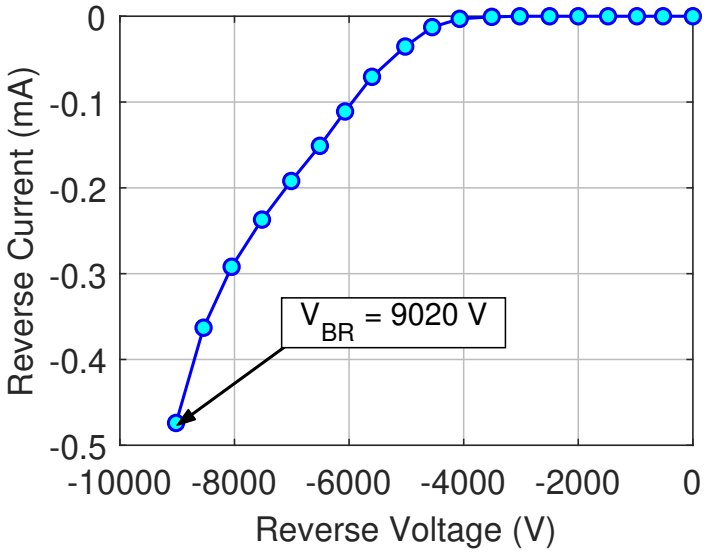


Figure 5.21. I-V characteristics of a back-to-back diode for breakdown voltage measurement.

6. CONCLUSION AND FUTURE RESEARCH

6.1 Summary of Achievements

We studied the feasibility of a superjunction drift region for a power MOSFET using both analytical models and 2D TCAD simulations to improve the drift layer resistance. After performing a detailed analysis we found that in the presence of charge imbalance the specific on-resistance increases with the square of the blocking voltage, which is not commonly known to date. We developed an iterative methodology to find an optimum design space and plotted the key design parameters as a function of blocking voltage as shown in Fig. 2.8. A simple figure-of-merit based analytical model was proposed to identify the optimum drift layer thickness and corresponding blocking voltage for a given pillar width and doping without performing numerical simulations [25]. The proposed method has been used as a foundation and extended to additional variables by other researchers in the community [64]–[67].

The current state-of-the-art technology for fabricating a superjunction structure in 4H-SiC MOSFET, and especially the technology to maintain a reasonable charge imbalance is not yet mature. Therefore, we refocused on the study and fabrication of a novel an n-channel IGBT to improve the drift layer resistance using conductivity modulation, and apply this technology to a lower blocking voltage range than previously possible through the use of our novel waffle substrate process. The physics of operation of an IGBT was understood through analytical models and 2D TCAD simulations. We simulated the expected performance based on realistic doping profiles in various regions so, and used the simulations to optimize the design.

In this project, we demonstrated the functionality of the world's first waffle substrate 10 kV class n-IGBT through successful simulaiton, design, fabrication and characterization. The IGBTs were characterized in the on-state at room temperature and $\Delta R_{ON,SP}$ was found to be 565.5 mΩ.cm^2 and 160 mΩ.cm^2 in samples with carrier lifetimes 1 μs and 4 μs respectively. A theoretical calculation shows that the drift region specific resistance without conductivity modulation would be 368 mΩ.cm^2. Therefore, the reported lifetime enhanced device showed good conductivity modulation in spite of having unexpectedly high contact resistivity. Since the on-state performance of IGBTs do not degrade at high temperature, it

can be said that the fabricated IGBT device performs better than a DMOSFET at a typical junction temperature of at 175 °C, where the theoretical optimum DMOSFET $R_{ON,SP}$ is 207 mΩ.cm^2. The novel idea of integrating the waffle substrate enables a new class of n-channel IGBTs of rating 15 kV where the standalone drift layer is too thin to support the device after substrate removal. The maximum blocking voltage due to avalanche was measured using a diode having the same FFR structure as 9 kV.

6.2 Recommended Future Work

The main target of this research, to demonstrate the feasibility of a waffle-substrate based n-IGBT, was achieved. Nevertheless, there is room for several future improvements. Suggestions for future work in this area are discussed below.

6.2.1 Improvement of p-type SiC ohmic contacts

As described in Section 3.4.1, n-channel IGBTs require better p-well ohmic contacts than necessary in DMOSFETs because about 20% of the total current is typically carried through the base contact. In addition, the back contact of the device, which carries all of the load current, is also a p-type contact. The summary of Section 5.1.6 indicates that the fabricated IGBT devices suffered greatly in the on-state due to the high p-type contact resistivity. The waffle substrate on the back side had an ohmic contact to the p-layer on the 4H-SiC C-face. The contribution of the high waffle contact resistivity to the degraded performance of the device was significant compared to the p-well contact because the former carries the total current while the later carries an relatively small portion. A rigorous experiment is needed to address several aspects of this problem as pointed out below.

i. Understand the difference between p-type 4H-SiC contact resistance on the C- and Si-faces.

ii. Develop an improved laser anneal process specifically optimized for p-type contacts on the C-face.

iii. An optimization of the geometric pattern of the waffle is also required to reduce the contact resistivity by increasing the footprint of the waffle depressions.

iv. Modify design to achieve 10 kV operation in IGBTs. Off-state voltage in current devices is limited by leakage current and gate dielectric failure, likely due to relatively wide JFET regions.

v. Optimize the waffle-substrate IGBT for better switching performance, since this work focused exclusively on on-state performance. One possibility is to decrease the lifetime in the buffer layer using vanadium doping [38], [68]

vi. Improve conductivity modulation using injection enhancement techniques [69].

6.2.2 Waffle trench filling

This research was concluded with a successful fabrication process of a functional n-IGBT with a waffle substrate collector contact. The waffle substrate fabrication was a major challenge because it made the sample very thin and fragile. We overcome the processing challenge and completed both of the samples. However, in a commercial device it woulid be necessary to fill the waffle trenches with highly conductive metal such as copper. The IGBTs are expected to be operated at high temperature and high power density leading to significant heat generation. Therefore the thermal conductivity of the refilled metal is critical, and temperature cycling of the devices will also stress the devices due to the mismatch in thermal expansion coefficients between the refilled metal and the SiC substrate. The deep waffle trenches with large openings can be filled with metal by electroplating, but the challenges of minimize voids inside the trench and to polishing the resulting surface need to be addressed. Therefore, a series of experiments are required to fill the trench with a suitable metal and quantify the mechanical strength and thermal stability of the completed waffle substrate.

6.2.3 Carrier lifetime engineering

In this project, one of the completed samples was treated to have a higher ambipolar carrier lifetime than the other, and the resulting improvement in on-state performance was noted during on-state characterization. It can be inferred from Fig. 5.13 that the effective carrier lifetimes coincide with excess carrier concentration of $\geq 1\times10^{18}$ cm^{-3} for a wide range of SRH lifetimes because other recombination mechanisms become dominant at these carrier concentrations. Therefore an important topic to explore is the usefulness of the higher SRH lifetimes if the excess carrier concentration is $\geq 1\times10^{18}$ cm^{-3}, since the effective lifetime is limited by radiative recombination. As a bipolar device, switching performance of IGBTs is also important, but it was beyond the scope of this project. Improved switching performance could be achieved through lifetime engineering. For instance, the buffer layer lifetime could be reduced by vanadium doping without significantly affecting the on-state performance [68].

A. WAFFLE-SUBSTRATE N-IGBT PROCESS RUN SHEET

A.1 Carrier Lifetime Enhancement

1. Screening oxide by wet oxidation

   i. Standard Solvent clean

      * Acetone soak, 5 min
      * Toluene soak, 5 min
      * Acetone soak, 5 min
      * Methanol soak, 5 min
      * Blow dry with N_2

   ii. RCA clean by beaker setup

      * Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
      * Rinse in DI thoroughly
      * BOE soak, 2-5 min [Oxide etch rate: 80 nm/min]
      * Rinse in DI thoroughly
      * SC1 (DI:H_2O_2:NH_4OH::10:3:3::250 ml:75 ml:75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min
      * Rinse in DI thoroughly
      * BOE soak, 2-5 min [Oxide etch rate: 80 nm/min]
      * Rinse in DI thoroughly
      * SC2 (DI:H_2O_2:HCl::10:3:3::250 ml:75 ml: 75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min
      * Rinse in DI thoroughly
      * BOE soak, 2-5 min [Oxide etch rate: 80 nm/min]
      * Rinse in DI thoroughly
      * Blow dry with N_2

   iii. Thermal oxidation in protemp furnace tube # 7

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* Steam flow at 6 slpm, 1100°C, 180 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

2. Carbon implantation

   i. 250 nm box profile with a dose of 1.35×10^{16} cm^{-2}

   * Energies: 110 keV, 50 keV, 15 keV
   * Doses: 7×10^{15} cm^{-2}, 5×10^{15} cm^{-2}, 2×10^{15} cm^{-2} at 500°C

   ii. Post-implantation clean and removal of screen oxide

   * Aqua Regia (HNO_3:HCl::1:3) soak, 15 min
   * Aqua Regia (HNO_3:HCl::1:3) soak again, 15 min
   * Thoroughly Rinse in DI thoroughly
   * Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
   * Rinse in DI thoroughly
   * BOE soak, 2-5 min
   * Rinse in DI thoroughly
   * Blow dry in N_2

3. Carbon cap formation

   i. Spin coat AZ1518

   * Spin at 1000 rpm, 40 sec, ramp 4 sec
   * Soft bake at 90°C, 10 min
   * Hard bake: 120-150°C in steps of 10°C, 1 hr

ii. Carbonization

* Preheat the Blue M tube with N_2 flow, 1 hr
* Turn on Ar flow, 250°C, 30 min
* Load the sample
* Set temperature at 675°C with Ar ambient, 20 min
* Set temp at 0°C
* Unload the sample at 147°C

4. High temperature annealing

i. 1600°C, 30 min

5. Carbon cap removal

i. Oxidation in Blue M tube

* Preheat with O_2 flow = 25 at 150°C, 20 min
* Preheat with O_2 flow = 25 at 150°C, 20 min
* Load the sample and keep 5 min
* Set T = 900°C, 30 min to reach the set point
* Steady state T = 900°C, 1 hr
* Set T = 0°C
* Unload sample at 150°C

6. Remove damaged SiC by RIE

i. Oxide removal

* BOE soak, 2-5 min
* Rinse in DI thoroughly

ii. Etching in Panasonic E620

* Mount the sample on the carrier wafer with crystal bond 555 and load

* Parameter set: RF power = 600 W, Bias power = 200 W, SF_6 flow rate = 20 sccm, Pressure = 3 Pa
* Etch time, 7 min

7. Sacrificial oxide by wet oxidation and removal

   i. Standard solvent clean

   * Acetone soak, 5 min
   * Toluene soak, 5 min
   * Acetone soak, 5 min
   * Methanol soak, 5 min
   * Blow dry with N_2

   ii. RCA clean using beaker setup

   * Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
   * Rinse in DI thoroughly
   * BOE soak, 2-5 min [Oxide etch rate: 80 nm/min]
   * Rinse in DI thoroughly
   * SC1 (DI:H_2O_2:NH_4OH::10:3:3::250 ml:75 ml:75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min
   * Rinse in DI thoroughly
   * BOE soak, 2-5 min [Oxide etch rate: 80 nm/min]
   * Rinse in DI thoroughly
   * SC2 (DI:H_2O_2:HCl::10:3:3::250 ml:75 ml:75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min
   * Rinse in DI thoroughly
   * BOE soak, 2-5 min [Oxide etch rate: 80 nm/min]
   * Rinse in DI thoroughly
   * Blow dry with N_2

iii. Thermal oxidation in protemp furnace tube # 7

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* Steam flow at 6 slpm, 1100°C, 600 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

iv. Stripping the sacrificial oxide

* BOE soak, 2-5 min
* Rinse in DI thoroughly

A.2 CSL Implantation

1. Screening oxide by wet oxidation

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. RCA clean using beaker setup

* Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
* Rinse in DI thoroughly
* BOE soak, 5 min [Oxide etch rate: 80 nm/min]
* Rinse in DI thoroughly

* SC1 (DI:H_2O_2:NH_4OH::10:3:3::250 ml:75 ml:75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min
* Rinse in DI thoroughly
* BOE soak, 5 min [Oxide etch rate: 80 nm/min]
* Rinse in DI thoroughly
* SC2 (DI:H_2O_2:HCl::10:3:3::250 ml:75 ml:75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min
* Rinse in DI thoroughly
* BOE soak, 5 min [Oxide etch rate: 80 nm/min]
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Thermal oxidation in protemp furnace # 7

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* Steam flow at 6 slpm, 1100°C, 180 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

2. Polysilicon film deposition

i. Solvent and acid clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

* Piranha clean, 15 min
* Rinse thoroughly with DI
* Blow dry with N_2

ii. Polysilicon deposition by LPCVD

* Load the sample in protemp tube # 6
* Run for 230 min at 630°C

3. PR pattern as polysilicon etch mask

i. Photolithography using AZ1518, CSL implant mask (# 1) and MA6

* Puddle AZ1518 and spin at 4000 rpm, 40 sec, ramp 4 sec
* Bake at 100°C, 2 min (Set hot plate at 110°C)
* Expose at 14 mW/cm^2 (λ = 405 nm), 11.5 sec [161 mJ/cm^2] in MA6
* Develop in MF26A, 30 sec
* Rinse in DI thoroughly
* Blow dry with N_2

ii. Polysilicon RIE using STS-ASE

* Mount the sample on a carrier wafer using crystal bond 555 and load
* Parameter set: Etch Pressure = 18, Dep Pressure = 18,
  Etch Coil RF = 500 W, Dep Coil RF = 600 W,
  Etch Platen HF = 20 W, Dep Platen HF = 0, Dep C_4F_8 = 100 sccm,
  Etch SF_6 = 130 sccm, Etch O_2 = 13 sccm
* Etch for 8 min

iii. Stripping photoresist

* Soak in remover PG (1st bath), 80°C, long time (preferably overnight)
* Soak in remover PG (2nd bath), 80°C, 30 min
* Soak in IPA, RT, 10 min
* Rinse in DI thoroughly

* Blow dry with N_2

ii. Residue removal by Branson ashing

* Load the sample on a glass slide
* Set O_2 flow = 14/6, Ar flow = 135, Power = 200 W
* Run for 30 min

4. Nitrogen implantation

i. Box profile with a dose of 3.76×10^{12} cm^{-2}

* Energies: 350 keV, 250 keV, 180 keV, 120 keV, 80 keV, 50 keV, 30 keV, 15 keV at 500°C
* Doses: 11×10^{10} cm^{-2}, 11×10^{10} cm^{-2}, 9×10^{10} cm^{-2}, 8×10^{10} cm^{-2}, 6×10^{10} cm^{-2}, 5×10^{10} cm^{-2}, 3×10^{10} cm^{-2}, 3×10^{10} cm^{-2},
* 680 keV w/ dose 3.2×10^{12} cm^{-2} at RT

A.3 Alignment Mark for Base Layer

1. PR pattern for alignment mark etch

i. Photolithography using AZ9260, alignment mark # 1 mask (# 2) and MA6

* Puddle AZ9260
* Spin at 4000 rpm, 30 sec, ramp 4 sec [Expected thickness 6.75 μm]
* Soft bake at 110°C, 3 min
* Expose in MA6 at 14 mW/cm^2, 43 sec [600 mJ/cm^2]
* Develop in AZ400K:DI (1:3 :: 75 ml : 225 ml), 3.5 min in 1^{st} bath and 30 sec in 2^{nd} bath
* Rinse in DI thoroughly
* Blow dry with N_2
* Hard bake at 110°C [Hotplate set point = 120°C], 5 min

2. Etching SiC by RIE

    i. Etching in Panasonic E620

        * Mount the sample on the carrier wafer with crystal bond 555 and load
        * Parameter set: RF power = 600 W, Bias power = 200 W, SF_6 flow rate = 20 sccm, Pressure = 3 Pa
        * Etch time, 1st step 3 min and 2nd step 5 min

3. Stripping photoresist

    i. Stripping by solvent

        * Soak in remover PG (1st bath), 80°C, long time (preferably overnight)
        * Soak in remover PG (2nd bath), 80°C, 30 min
        * Soak in IPA, RT, 10 min
        * Rinse in DI thoroughly
        * Blow dry with N_2

    ii. Residue removal by Branson ashing

        * Load the sample on a glass slide
        * Set O_2 flow = 14/6, Ar flow = 135, Power = 200 W
        * Run for 30 min

4. Post-implantation clean

    i. Acid clean due to CSL implantation

        * Aqua Regia (HNO_3:HCl::1:3) soak, 15 min
        * Rinse in DI thoroughly
        * Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
        * Rinse in DI thoroughly
        * Blow dry with N_2

5. Stripping polysilicon layer

i. Wet etching of polysilicon

* Soak in DI:HF:HNO_3::1:1:5 :: 50 ml:50 ml:250 ml, 5 min
* Rinse in DI thoroughly
* Blow dry with N_2

6. Stripping screening oxide

i. Wet etching of oxide

* Soak in BOE, 3 min
* Rinse in DI thoroughly
* Blow dry with N_2

A.4 Base Implantation

1. Screening oxide by wet oxidation

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. RCA clean using beaker setup

* Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
* Rinse in DI thoroughly
* BOE soak, 5 min [Oxide etch rate: 80 nm/min]
* Rinse in DI thoroughly
* SC1 (DI:H_2O_2:NH_4OH::10:3:3::250 ml:75 ml:75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min

* Rinse in DI thoroughly
* BOE soak, 5 min [Oxide etch rate: 80 nm/min]
* Rinse in DI thoroughly
* SC2 (DI:H_2O_2:HCl::10:3:3::250 ml:75 ml:75 ml) soak on a hot plate at 70°C (set point: 225°C), 15 min
* Rinse in DI thoroughly
* BOE soak, 5 min [Oxide etch rate: 80 nm/min]
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Thermal oxidation in protemp furnace tube # 4

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* Steam flow at 6 slpm, 1100°C, 240 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

2. Polysilicon film deposition

i. Polysilicon deposition by LPCVD

* Load the sample in protemp tube # 6
* Run for 230 min at 630°C

3. PR pattern as polysilicon etch mask

i. Photolithography using AZ1518, p-well mask (# 3) and MA6 or Heidelberg MLA150

* Puddle AZ1518
* Spin at 4000 rpm, 40 sec, ramp 4 sec

* Bake at 100°C, 1 min (Set hot plate at 110°C)
* Align with mark # 3T in MA6 and expose at 14 mW/cm^2 (= 405 nm), 11.5 sec [161 mJ/cm^2]
* Or align with mark # 3T in Heidelberg MLA150 and expose at dose = 290 mJ/cm^2
* Develop in MF26A, 30 sec
* Rinse in DI thoroughly
* Blow dry with N_2

4. Polysilicon RIE using STS-ASE

i. Bosch process

* Mount the sample on a carrier wafer using crystal bond 555 and load
* Parameter set: Etch Pressure = 18, Dep Pressure = 18, Etch Coil RF = 500 W, Dep Coil RF = 600 W, Etch Platen HF = 20 W, Dep Platen HF = 0, Dep C_4F_8 = 100 sccm, Etch SF_6 = 130 sccm, Etch O_2 = 13 sccm
* Etch time, 1st step 4 min and 2nd step 1 min

5. Stripping photoresist

i. Stripping by solvent

* Soak in remover PG (1st bath), 80°C, long time (preferably overnight)
* Soak in remover PG (2nd bath), 80°C, 30 min
* Soak in IPA, RT, 10 min
* Rinse in DI thoroughly
* Blow dry with N_2

ii. Residue removal by Branson ashing

* Load the sample on a glass slide
* Set O_2 flow = 14/6, Ar flow = 135, Power = 200 W

* Run for 30 min

6. Aluminum implantation

   i. Box profile with a net dose of 6.44×10^{13} cm^{-2}

      * Energies: 320 keV, 80 keV, 40 keV, 15 keV at 500°C
      * Doses: 6.3×10^{13} cm^{-2}, 1.8×10^{12} cm^{-2}, 7.5×10^{11} cm^{-2}, 6.3×10^{11} cm^{-2}

A.5 Alignment Mark for Subsequent Layers

1. PR pattern for alignment mark etch

   i. Photolithography using AZ9260, alignment mark # 2 mask (# 4) and Heidelberg MLA150

      * Puddle AZ9260
      * Spin at 4000 rpm, 30 sec, ramp 4 sec [Expected thickness 6.75 μm]
      * Soft bake at 110°C, 3 min
      * Align with mark # 4A in Heidelberg MLA150 and expose at dose = 590 mJ/cm^2
      * Develop in AZ400K:DI (1:3 :: 75 ml : 225 ml), 3.5 min in 1^{st} bath and 0.5 min in 2^{nd} bath
      * Rinse in DI thoroughly
      * Blow dry with N_2

2. Etching SiC by RIE

   i. Etching in Panasonic E620

      * Mount the sample on the carrier wafer with crystal bond 555 and load
      * Parameter set: RF power = 600 W, Bias power = 200 W, SF_6 flow rate = 20 sccm, Pressure = 3 Pa
      * Etch time, 1^{st} step 3 min, 2^{nd} step 3 min and 3^{rd} step 2 min

3. Stripping photoresist

   i. Stripping by solvent

      * Soak in remover PG (1^{st} bath), 80°C, long time (preferably overnight)
      * Soak in remover PG (2^{nd} bath), 80°C, 30 min
      * Soak in IPA, RT, 10 min
      * Rinse in DI thoroughly
      * Blow dry with N_2

   ii. Residue removal by Branson ashing

      * Load the sample on a glass slide
      * Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
      * Run for 1 min

A.6 Source Implantation

1. Source implant mask by wet oxidation of polysilicon

   i. Standard solvent clean

      * Acetone soak, 5 min
      * Toluene soak, 5 min
      * Acetone soak, 5 min
      * Methanol soak, 5 min
      * Blow dry with N_2

   iii. Acid clean

      * Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
      * Rinse in DI thoroughly
      * Blow dry with N_2

   iii. Thermal oxidation of polysilicon in Protemp tube # 4

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* Steam flow at 6 slpm, 1100°C, 225 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

2. Nitrogen implantation

   i. Box profile with a net dose of 4.86×10^{14} cm^{-2}

   * Energies: 140 keV, 100 keV, 70 keV, 50 keV, 30 keV, 15 keV at 500°C
   * Doses: 2.5×10^{14} cm^{-2}, 1.35×10^{14} cm^{-2}, 6.3×10^{13} cm^{-2}, 7.2×10^{13} cm^{-2}, 6.3×10^{13} cm^{-2}, 6.3×10^{13} cm^{-2}

3. Post-implantation clean

   i. Acid clean due to source implantation

   * Aqua Regia (HNO_3:HCl::1:3) soak, 15 min
   * Rinse in DI thoroughly
   * Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
   * Rinse in DI thoroughly
   * Blow dry with N_2

4. Stripping oxide

   i. Wet oxide etching

   * Soak in BOE, 20 min
   * Rinse in DI thoroughly
   * Blow dry with N_2

5. Stripping polysilicon layer

i. Wet etching of polysilicon

* Soak in DI:HF:HNO_3::1:1:5 :: 50 ml:50 ml:250 ml, 5 min
* Rinse in DI thoroughly
* Blow dry with N_2

6. Stripping screening oxide

i. Wet oxide etching

* Soak in BOE, 3 min
* Rinse in DI thoroughly
* Blow dry with N_2

A.7 Base Contact Implantation

1. Screening oxide by wet oxidation

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. RCA clean in the RCA hood

* In the standard acid hood: Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
* Rinse in DI thoroughly
* In the RCA hood: SC1 (DI:H_2O_2:NH_4OH::5:1:1::7.1 L:1.4 L:1.4 L) bath, 80°C, 10 min
* Rinse in DI thoroughly
* SC2 (DI:H_2O_2:HCl::6:1:1::7.5 L:1.25 L:1.25 L) bath, 80°C, 10 min

* Rinse in DI thoroughly
* HF [HF:DI::1:49::0.105 L:5.14 L]bath, 1 min
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Thermal oxidation in protemp furnace tube # 4

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* Steam flow at 6 slpm, 1100°C, 360 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

2. Polysilicon layer deposition

i. Polysilicon deposition by LPCVD

* Load the sample in protemp tube # 6
* Run for 120 min at 630°C

3. E-beam resist pattern as polysilicon etch mask

i. E-beam lithography using CSAR, p+ implant mask (5) and JEOL

* Keep CSAR out of refrigerator for 1 hr
* Puddle CSAR
* Spin at 4000 rpm, 60 sec [Expected thickness 400 nm]
* Soft bake at 155°C, 3 min
* Align with mark # 5 of dies 44T, 67T, 46T, 64T and expose in JEOL with dose = 280 mJ/cm^2, [4 hr 16 min]
* Develop in Xylene, 70 sec

* Rinse in IPA
* Blow dry with N_2

4. Polysilicon RIE using STS-ASE

   i. Bosch process

   * O_2 clean of the chamber using dummy wafer, 20 min
   * Mount the sample on a carrier wafer using crystal bond 555 and load
   * Parameter set: Etch Pressure = 18, Dep Pressure = 18,
     Etch Coil RF = 500 W, Dep Coil RF = 600 W, Etch Platen HF = 20 W,
     Dep Platen HF = 0, Dep C_4F_8 = 100 sccm, Etch SF_6 = 130 sccm,
     Etch O_2 = 13 sccm
   * Etch time, 1^{st} step 1 min, 2^{nd} step 1 min and 3^{rd} step 30 sec

5. Stripping e-beam resist (CSAR)

   i. Stripping CSAR by solvent

   * Soak in remover PG at 80°C, long time (preferably overnight)
   * Soak in IPA, 10 min
   * Blow dry with N_2

6. Aluminum implantation

   i. Box profile with a net dose of 5.41×10^{14} cm^{-2}

   * Energies: 270 keV, 170 keV, 85 keV, 40 keV, 15 keV at 500°C
   * Doses: 2.5×10^{14} cm^{-2}, 1.6×10^{14} cm^{-2}, 1.0×10^{14} cm^{-2}, 4.5×10^{13} cm^{-2},
     3.5×10^{13} cm^{-2}

7. Post-implantation clean

   i. Acid clean due to p+ base contact implantation

   * Aqua Regia (HNO_3:HCl::1:3) soak, 15 min

* Rinse in DI thoroughly
* Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
* Rinse in DI thoroughly
* Blow dry with N_2

8. Stripping polysilicon layer

   i. Wet etching of polysilicon

   * Soak in DI:HF:HNO_3::1:1:5 :: 50 ml:50 ml:250 ml, 5 min
   * Rinse in DI thoroughly
   * Blow dry with N_2

9. Stripping screening oxide

   i. Wet etching of oxide

   * Soak in BOE, 2 min
   * Rinse in DI thoroughly
   * Blow dry with N_2

10. Carbon cap formation

    i. Spin coat AZ1518

    * Spin at 1000 rpm, 40 sec, ramp 4 sec
    * Soft bake at 90°C, 10 min
    * Hard bake: 120-150°C in steps of 10°C, 1 hr

    ii. Carbonization

    * Preheat the Blue M tube with N_2 flow, 1 hr
    * Turn on Ar flow, 250°C, 30 min
    * Load the sample
    * Set temperature at 675°C with Ar ambient, 20 min
    * Set temp at 0°C

* Unload the sample at 147°C

11. High temperature annealing (implant) at Epigress

    i. Load the samples in Epigress system

    ii. Ramp the temperature to 1700°C

    iii. Maintain steady state temperature, 20 min

    iv. Ramp down the temperature to RT and keep the samples inside overnight

12. Carbon cap removal

    i. Oxidation in Blue M tube

        * Preheat with O_2 flow = 25 at 150°C, 20 min
        * Preheat with O_2 flow = 25 at 150°C, 20 min
        * Load the sample and keep 5 min
        * Set T = 900°C, 30 min to reach the set point
        * Steady state T = 900°C, 1 hr
        * Set T = 0°C
        * Unload sample at 150°C

13. Sacrificial oxide by wet oxidation

    i. Standard solvent clean

        * Acetone soak, 5 min
        * Toluene soak, 5 min
        * Acetone soak, 5 min
        * Methanol soak, 5 min
        * Blow dry with N_2

    ii. RCA clean in the RCA hood

        * In the standard acid hood: Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min

* Rinse in DI thoroughly
* In the RCA hood: SC1 (DI:H_2O_2:NH_4OH::5:1:1::7.1 L:1.4 L:1.4 L) bath, 80°C, 10 min
* Rinse in DI thoroughly
* SC2 (DI:H_2O_2:HCl::6:1:1::7.5 L:1.25 L:1.25 L) bath, 80°C, 10 min
* Rinse in DI thoroughly
* HF [HF:DI::1:49::0.105 L:5.14 L]bath, 1 min
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Thermal oxidation in protemp furnace # 4

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* Steam flow at 6 slpm, 1100°C, 150 min
* O_2 flow at 1.5 lpm, 1100°C, 10 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

A.8 Field Oxide

1. Amorphous silicon film deposition

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. Acid clean

* BOE soak, 5 min
* Rinse in DI thoroughly
* Piranha(H_2SO_4:H_2O_2::1:1) soak, 15 min
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Amorphous silicon deposition by LPCVD

* Load in protemp tube # 6

2. Wet oxidation of amorphous silicon

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. RCA clean in the RCA hood

* In the standard acid hood: Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
* Rinse in DI thoroughly
* In the RCA hood: SC1 (DI:H_2O_2:NH_4OH::5:1:1::7.1 L:1.4 L:1.4 L) bath, 80°C, 10 min
* Rinse in DI thoroughly
* SC2 (DI:H_2O_2:HCl::6:1:1::7.5 L:1.25 L:1.25 L) bath, 80°C, 10 min
* Rinse in DI thoroughly
* HF [HF:DI::1:49::0.105 L:5.14 L]bath, 1 min
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Thermal oxidation in protemp furnace # 4

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 5 min
* Steam flow at 6 slpm, 1100°C, 60 min
* O_2 flow at 1.5 lpm, 1100°C, 5 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

3. PR pattern for oxide etching

i. Pre- clean with solvent

* Acetone soak in 1^{st} bath, 5 min
* Acetone soak in 2^{nd} bath, 5 min
* IPA soak in 1^{st} bath, 5 min
* IPA soak in 2^{nd} bath, 5 min
* Blow dry with N_2
* Soft bake at 120°C [hot plate set point 130°C], 5 min

ii. Lithography using AZ1518, FOX mask (# 6) and Heidelberg MLA150

* Puddle HMDS and wait for cooling down
* Spin at 0 rpm, 20 sec
* Spin at 4000 rpm, 40 sec [ramp 4 sec]
* Soft bake at 120°C [hot plate set point 130°C], 2 min
* Puddle AZ1518 and wait for cooling down
* Spin at 4000 rpm, 40 sec
* Bake at 100°C, 1 min (Set hot plate at 110°C)
* Align with mark (# 6)in Heidelberg MLA150 and expose at dose = 185 mJ/cm^2

* Develop in MF26A, 25 sec
* Rinse in DI thoroughly
* Blow dry with N_2

4. Oxide etching by wet chemistry

   i. Wet ethcing in BOE

   * Soak in BOE, 7 min
   * Rinse in DI thoroughly
   * Blow dry with N_2

5. Stripping photoresist

   i. Stripping by solvent

   * Soak in 1st bath Acetone, 5 min
   * Soak in 2nd bath Acetone, 5 min
   * Soak in Methanol, 10 min
   * Blow dry with N_2
   * Soak in remover PG at 80°C, long time (preferably overnight)
   * Soak in IPA, RT, 10 min
   * Rinse in DI thoroughly
   * Blow dry with N_2

A.9 Gate Formation

1. Gate oxide by wet oxidation

   i. Standard solvent clean

   * Acetone soak, 5 min
   * Toluene soak, 5 min
   * Acetone soak, 5 min

* Methanol soak, 5 min
* Blow dry with N_2

ii. RCA clean in the RCA hood

* In the standard acid hood: Piranha (H_2SO_4:H_2O_2::1:1) soak, 15 min
* Rinse in DI thoroughly
* In the RCA hood: SC1 (DI:H_2O_2:NH_4OH::5:1:1::7.1 L:1.4 L:1.4 L) bath, 80°C, 10 min
* Rinse in DI thoroughly
* SC2 (DI:H_2O_2:HCl::6:1:1::7.5 L:1.25 L:1.25 L) bath, 80°C, 10 min
* Rinse in DI thoroughly
* HF [HF:DI::1:49::0.105 L:5.14 L]bath, 20 sec
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Thermal oxidation in protemp furnace # 1

* Dry oxidation (O_2 = 3 lpm) at 850°C, 4 min
* Wet oxidation (Steam = 6 slpm) at 850°C, 15 min
* Dry oxidation (O_2 = 3 lpm) at 1100°C, 90 min
* Wet oxidation (Steam = 6 slpm) at 1100°C, 390 min
* Dry oxidation (O_2 = 3 lpm) at 1100°C, 10 min
* Dry oxidation (O_2 = 3 lpm) at 950°C, 4 min
* Wet oxidation (Steam = 6 slpm) at 950°C, 120 min
* Dry oxidation (O_2 = 3 lpm) at 950°C, 4 min

2. NO anneal

i. NO anneal process

* Purge the tube at RT with Ar flow = 5
* Set T = 110°C with Ar flow = 10 and load the sample when it's stabilized

* Set T = 850°C and switch the gas to NO with a flow rate = 0.3 after T is stabilized
* Set T = 1175°C with NO flow rate = 0.3 and counting the time starts at 1120°C
* Set T = 850°C after 2.5 hrs and approach to switch Ar with flow = 5 and set NO flow = 0

3. Polysilicon film deposition

   i. Standard solvent clean

      * Acetone soak, 5 min
      * Toluene soak, 5 min
      * Acetone soak, 5 min
      * Methanol soak, 5 min
      * Blow dry with N_2

   ii. Polysilicon deposition by LPCVD

      * Load the sample in protemp tube # 6
      * Run for 80 min at 630°C

4. Phosphorous doping in polysilicon

   i. Standard solvent clean

      * Acetone soak, 5 min
      * Toluene soak, 5 min
      * Acetone soak, 5 min
      * Methanol soak, 5 min
      * Blow dry with N_2

   ii. Acid clean

      * BOE soak, 5 min

* Rinse in DI thoroughly
* Piranha (H_2SO_4:H_2O_2::1:1) soak, 2 min
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Solvent clean

* IPA soak, 5 min
* Blow dry with N_2

iv. Spin coating P509

* Puddle P509
* Spin at 500 rpm, 5 sec, ramp 4 sec
* Spin at 3000 rpm, 12 sec
* Bake at 200°C, 20 min

v. Dopant drive in protemp tube # 8

* Load at 850°C
* Steady state drive in at 1000°C, 2 hrs, w/ N_2 = 75%, O_2 = 25%

vi. Stripping the dopant film

* Soak in BOE, 5 min
* Rinse in DI thoroughly
* Blow dry with N_2

5. PR pattern as polysilicon etch mask

i. Pre-clean with solvent

* Acetone soak in 1st bath, 5 min
* Acetone soak in 2nd bath, 5 min
* IPA soak in 1st bath, 5 min
* IPA soak in 2nd bath, 5 min

* Blow dry with N_2
* Soft bake at 120°C [hot plate set point 130°C], 5 min

ii. Photoresist pattern using Poly Gate mask (# 7)

* Wait for cooling down and Puddle HMDS
* Spin at 0 rpm, 20 sec
* Spin at 4000 rpm, 40 sec, ramp 4 sec
* Soft bake at 120°C [hot plate set point 130°C], 2 min
* Wait for cooling down and Puddle AZ1518
* Spin at 4000 rpm, 40 sec
* Bake at 100°C, 1 min (Set hot plate at 110°C)
* Align with mark (# 7)in Heidelberg MLA150 and expose at dose = 235 mJ/cm^2
* Develop in MF26A, 25 sec
* Rinse in DI thoroughly
* Blow dry with N_2

6. Polysilicon RIE in STS-ASE

i. Bosch process

* O_2 clean the chamber using dummy wafer, 15 min
* Mount the sample on a carrier wafer using crystal bond 555 and load
* Parameter set: Etch Pressure = 18, Dep Pressure = 18, Etch Coil RF = 500 W, Dep Coil RF = 600 W, Etch Platen HF = 20 W, Dep Platen HF = 0, Dep C_4F_8 = 100 sccm, Etch SF_6 = 130 sccm, Etch O_2 = 13 sccm
* Etch time, 2 min

7. Stripping photoresist

i. Stripping by solvent

* Soak in remover PG at 80°C, long time (preferably overnight)
* Soak in IPA, RT, 10 min
* Blow dry with N_2

8. ILD formation by wet oxidation of polysilicon

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. Acid hood

* Piranha (H_2SO_4:H_2O_2::1:1) soak, 20 min
* Rinse in DI thoroughly
* Blow dry with N_2

iii. Thermal oxidation in protemp furnace tube # 4

* Load with N_2 and O_2 at 600°C, 1 min
* Ramp the temperature to 1100°C w/ N_2, 120 min
* O_2 flow at 1.5 lpm, 1100°C, 5 min
* Steam flow at 6 slpm, 1100°C, 225 min
* O_2 flow at 1.5 lpm, 1100°C, 5 min
* N_2 purge, 400°C, 100 min
* Unload w/ N_2, 400°C

A.10 Base Contact Metallization

1. Stripping oxide from source region

i. Stripping oxide by wet chemistry

   * BOE soak, 75 sec
   * Rinse in DI thoroughly
   * Blow dry with N_2

2. Lift-off lithography

   i. Standard solvent clean

      * Acetone soak, 5 min
      * Toluene soak, 5 min
      * Acetone soak, 5 min
      * Methanol soak, 5 min
      * Blow dry with N_2
      * Soft bake at 120°C [hot plate set point 130°C], 5 min

   ii. Photolithography using LOR3B, AZ1518, base contact mask (# 8) and Heidelberg MLA150

      * Puddle LOR3B
      * Spin at 2000 rpm, 45 sec, ramp 4 sec
      * Soft bake at 150°C [hot plate set point 160°C], 5 min
      * Wait for cooling down and puddle AZ1518
      * Spin at 4000 rpm, 40 sec
      * Bake at 100°C, 1 min (Set hot plate at 110°C)
      * Align with mark (# 9)in Heidelberg MLA150 and expose at dose = 235 mJ/cm^2
      * Develop in MF26A, 27 sec
      * Rinse in DI thoroughly
      * Blow dry with N_2

3. Metal deposition process

i. Pre-deposition clean process

* Load in Branson Asher on a glass slide for descum
* Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
* Run for 1 min
* Load in Jupiter II for RIE
* Set SF_6 flow = 20 sccm; Ar flow = 10 sccm, Power = 100 W
* Run for 15 sec
* Load in Branson Asher on a glass slide for descum
* Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
* Run for 1 min
* BOE dip in an acid hood
* BOE soak, 10 sec
* Rinse in DI thoroughly
* Blow dry with N_2

ii. Metal deposition in PVD1

* Load in PVD1
* Evaporate Ti (333 Å)
* Evaporate Al (1667 Å)
* Evaporate Ni (200 Å)

4. Lift-off process

i. Lift-off by solvent

* Soak in remover PG (1^{st} bath) at 80°C, long time (preferably overnight)
* Soak in remover PG (2^{nd} bath) at 80°C, 10 min
* Soak in IPA, RT, 10 min
* Blow dry with N_2

A.11 Ohmic Contact Metallization and Annealing

1. Lift-off lithography

    i. Standard solvent clean and bake

        * Acetone soak, 5 min
        * Toluene soak, 5 min
        * Acetone soak, 5 min
        * Methanol soak, 5 min
        * Blow dry with N_2
        * Soft bake at 120°C [hot plate set point 130°C], 5 min

    ii. Photolithography using LOR3B, AZ1518, source contact mask (# 9) and Heidelberg MLA150

        * Puddle LOR3B
        * Spin at 2000 rpm, 45 sec, ramp 4 sec
        * Soft bake at 150°C [hot plate set point 160°C], 5 min
        * Wait for cooling down and puddle AZ1518
        * Spin at 4000 rpm, 40 sec
        * Bake at 100°C, 1 min (Set hot plate at 110°C)
        * Align with mark (# 10)in Heidelberg MLA150 and expose at dose = 235 mJ/cm^2
        * Develop in MF26A, 22 sec
        * Rinse in DI thoroughly
        * Blow dry with N_2

2. Metal deposition process

    i. Pre-deposition clean process

        * Load in Branson Asher on a glass slide for descum

* Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
* Run for 1 min
* Load in Jupiter II for RIE
* Set SF_6 flow = 20 sccm; Ar flow = 10 sccm, Power = 100 W
* Run for 15 sec
* Load in Branson Asher on a glass slide for descum
* Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
* Run for 1 min
* BOE dip in an acid hood
* BOE soak, 10 sec
* Rinse in DI thoroughly
* Blow dry with N_2

ii. Metal deposition in PVD1

* Load in PVD1
* Evaporate Ni (1000 Å)

3. Lift-off process

i. Lift-off by solvent

* Soak in remover PG (1^{st} bath) at 80°C, long time (preferably overnight)
* Soak in remover PG (2^{nd} bath) at 80°C, 10 min
* Soak in IPA, RT, 10 min
* Blow dry with N_2

4. High temperature contact anneal

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min

* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. Rapid thermal annealing in Jipelec RTA

* Run recipe 5 for 2 min at 1000°C

A.12 ILD Opening for Gate Contact

1. Post-anneal clean

   i. Standard solvent clean

   * Acetone soak, 5 min
   * Toluene soak, 5 min
   * Acetone soak, 5 min
   * Methanol soak, 5 min
   * Blow dry with N_2

   ii. RIE in Jupiter II

2. PR pattern as oxide etch mask

   i. Pre-lithography clean with solvent

   * Acetone soak in 1^{st} bath, 5 min
   * Acetone soak in 2^{nd} bath, 5 min
   * IPA soak in 1^{st} bath, 5 min
   * IPA soak in 2^{nd} bath, 5 min
   * Blow dry with N_2
   * Soft bake at 120°C [hot plate set point 130°C], 5 min

   i. Lithography using AZ9260, gate ILD etch mask # 10
   and Heidelberg MLA150

* Wait for cooling down and puddle HMDS
* Spin at 0 rpm, 20 sec
* Spin at 4000 rpm, 40 sec, ramp 4 sec
* Soft bake at 120°C [hot plate set point 130°C], 2 min
* Wait for cooling down and puddle AZ9260
* Spin at 4000 rpm, 30 sec
* Bake at 110°C, 3 min (Set hot plate at 120°C)
* Align with mark # 8 in Heidelberg MLA150 and expose at dose = 415 mJ/cm^2
* Develop in AZ400K:DI::75 ml:225 ml for 3.5 min (1st bath) and 30 sec(2nd bath)
* Rinse in DI thoroughly
* Blow dry with N_2

3. Oxide etching

   i. RIE process in Panasonic E620

   * Mount the sample on the carrier wafer with crystal bond 555 and load
   * Parameter set: RF power = 650 W, Bias power = 50 W, CF_4 flow rate = 10 sccm, CHF_3 flow rate = 40 sccm, Pressure = 1 Pa
   * Etch time, 10 min

   ii. Wet chemistry process in BOE

   * Soak in BOE, 3 min
   * Rinse in DI thoroughly
   * Blow dry with N_2

4. Stripping photoresist

   i. Stripping by solvent

   * Soak in remover PG at 80°C, long time (preferably overnight)

* Soak in IPA, RT, 10 min
* Blow dry with N_2

A.13 Top Ohmic Metallization

1. Metal deposition process

   i. Standard solvent clean

   * Acetone soak, 5 min
   * Toluene soak, 5 min
   * Acetone soak, 5 min
   * Methanol soak, 5 min
   * Blow dry with N_2

   ii. Pre-deposition clean process

   * Load in Branson Asher on a glass slide for descum
   * Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
   * Run for 1 min
   * BOE dip in an acid hood
   * BOE soak, 10 sec
   * Rinse in DI thoroughly
   * Blow dry with N_2

   iii. Metal deposition by sputtering in PVD system

   * Load the sample
   * Set power = 350 W, Ar flow = 15 sccm and metal source = Al
   * Run for 3 hrs 30 min

2. PR pattern as top metal etch mask

   i. Pre-lithography clean with solvent

* Acetone soak in 1st bath, 5 min
* Acetone soak in 2nd bath, 5 min
* IPA soak in 1st bath, 5 min
* IPA soak in 2nd bath, 5 min
* Blow dry with N_2
* Soft bake at 120°C [hot plate set point 130°C], 5 min

ii. Lithography using AZ1518, top metal mask (# 11) and Heidelberg MLA150

* Wait for cooling down and puddle HMDS
* Spin at 0 rpm, 20 sec
* Spin at 4000 rpm, 40 sec, ramp 4 sec
* Soft bake at 120°C [hot plate set point 130°C], 2 min
* Wait for cooling down and puddle AZ1518
* Spin at 4000 rpm, 40 sec, ramp 4 sec
* Bake at 100°C, 1 min (Set hot plate at 110°C)
* Align with mark # 11D in Heidelberg MLA150 and expose at dose = 200 mJ/cm^2
* Develop in MF26A, 22 sec
* Rinse in DI thoroughly
* Blow dry with N_2

3. Wet etching of Aluminum

i. Etch in Al etch type A etchant

* Prepare the etchant solution as H_3PO_4:HNO_3:CH_3COOH:DI::400 ml:25 ml:25 ml:50 ml
* Etch for 2 min at 50°C

4. Stripping photoresist

i. Stripping by solvent

* Soak in remover PG at 80°C, long time (preferably overnight)
* Soak in IPA, RT, 10 min
* Blow dry with N_2

A.14 Waffle Process

1. Thinning substrate by RIE

   i. Standard solvent clean

   * Acetone soak, 5 min
   * Toluene soak, 5 min
   * Acetone soak, 5 min
   * Methanol soak, 5 min
   * Blow dry with N_2

   ii. Coating top side with photoresist AZ1518

   * Puddle AZ1518
   * Spin at 1000 rpm, 40 sec, ramp 4 sec
   * Soft Bake at 100°C, 1 min (Set hot plate at 110°C)
   * Hard Bake at 120°C, 20 min (Set hot plate at 130°C)

   iii. Stripping polysilicon layer from the back side

   * Soak in DI:HF:HNO_3 = 1:1:5::50 ml:50 ml:250 ml, 80 sec
   * Rinse in DI thoroughly
   * Blow dry with N_2

   iv. Stripping remaining oxide from the back side

   * Soak in BOE, 2 min 30 sec
   * Rinse in DI thoroughly
   * Blow dry with N_2

v. Stripping photoresist from the top side

* Soak in remover PG at 80°C, long time (preferably overnight)
* Soak in IPA, RT, 10 min
* Blow dry with N_2

vi. Back side RIE process in STS-AOE

* Mount the sample on a carrier wafer with crystal bond 555
* O_2 clean the chamber with a dummy wafer, 30 min
* Set RF power = 1800 W, Bias power = 70 W, SF_6 flow = 17 sccm, Pressure = 10 mT
* Load the sample and run for maximum 4 hrs
* Unload and unmount the sample on a hot plate
* Clean the remaining crystal bond in running DI and blow dry with N_2
* Repeat above steps until the target is achieved

2. Waffle etch mask by Ni electroplating

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. Coating top side with photoresist AZ9260

* Puddle AZ9260
* Spin at 4000 rpm, 30 sec, ramp 4 sec
* Soft Bake at 110°C, 3 min (Set hot plate at 120°C)

iii. Metal seed layer deposition for electroplating

* Load the sample in CHA-1

* Evaporate 25 nm Ti
* Evaporate 75 nm Au

iv. PR mask fo electroplating by photo lithography using AZ9260 and Heidelberg MLA150

* First coating: Puddle AZ9260
* Spin at 2400 rpm, 60 sec, ramp 4 sec
* Soft bake at 110°C [hot plate set point 120°C], 80 sec
* Second coating: Puddle AZ9260
* Spin at 2400 rpm, 60 sec, ramp 4 sec
* Soft bake at 110°C [hot plate set point 120°C], 180 sec
* Expose in MLA150 using waffle mask with dose = 950 mJ/cm^2
* Develop in AZ400K:DI(1:3::75 ml:225 ml), 4 min in 1st bath and 2 min in 2nd bath
* Rinse in DI thoroughly
* Blow dry with N_2

v. Post-development clean

* Load on a glass slide in Branson asher
* Set O_2 flow = 11/5, Ar flow = 110, Power = 100 W
* Run for 1 min

vi. Ni electroplating using beaker setup

* Take 750 ml Ni Sulfamate in a beaker on a hot plate
* Set temperature = 40°C, stir = 100 rpm
* Submerge the sample hanging from cathode
* Supply 80 mA current
* Run for 1 hr 15 min
* Rinse in DI thoroughly and blow dry with N_2

vii. Stripping photoresist by solvent

* Soak in remover PG at 80°C, long time (preferably overnight)
* Soak in IPA, RT, 10 min
* Blow dry with N_2

viii. Coating top side with photoresist AZ1518

* Puddle AZ1518
* Spin at 1000 rpm, 40 sec, ramp 4 sec
* Soft bake at 100°C for 1 min and hard bake at 120°C for 20 min

ix. Etching metal seed layer

* Soak in 250 ml Au etchant GE-8148, 30 sec
* Rinse in DI thoroughly
* Soak in Ti etchant DI:H_2O_2:HF::400 ml:20 ml:20 ml, 30 sec
* Rinse in DI thoroughly
* Blow dry with N_2

x. Stripping photoresist by solvent

* Soak in remover PG at 80°C, long time (preferably overnight)
* Soak in IPA, RT, 10 min
* Blow dry with N_2

3. Waffle pattern by RIE

i. RIE process in STS-AOE

* Mount the sample on a Si carrier wafer using crystal bond 555
* O_2 clean the chamber with a dummy wafer, 30 min
* Set RF power = 1800 W, Bias power = 70 W, SF_6 flow = 17 sccm, Pressure = 10 mT
* Load the sample and run for maximum 4 hrs

ii. Etch stop detection by Bruker profilometry and I-V measurement at probe station

        * Measure the step height in Bruker profilometer and quantify whether p-anode layer is reached or not
        * Measure I-V characteristics between mesa and trench bottom and identify whether p-anode layer is reached or not
    iii. Repeat processes (i.) and (ii.) until p-anode layer is detected

4. Ohmic contact metallization

    i. Pre-deposition clean process

        * Load in Jupiter II
        * Set SF_6 flow = 20 sccm; Ar flow = 10 sccm, Power = 100 W
        * Run for 15 sec
        * Load in Branson Asher on a glass slide for descum
        * Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
        * Run for 1 min
        * BOE dip in an acid hood
        * BOE soak, 10 sec
        * Rinse in DI thoroughly
        * Blow dry with N_2

    ii. Metal deposition process in PVD1

        * Load in PVD1
        * Evaporate 33 nm Ti, 167 nm Al, 100 nm Ni

5. Ohmic contact formation by laser annealing

    i. Sample mounting process for the annealing

        * Puddle the carrier wafer with AZ9260
        * Spin at 4000 rpm, 30 sec, ramp 4 sec
        * Place the sample at the center of the carrier wafer and bake at 110°C for 3 min

* Clean the PR from the field area using acetone soaked wipe and qtip

ii. Laser anneal process [Performed by Fraunhofer IISB, Germany]

* Energy density: 3.3 J/cm^2
* Scan overlap: 67%, Step overlap: 50%

iii. Sample unmounting process

* Soak in remover PG at 80°C, long time (preferably overnight)
* Soak in IPA, RT, 10 min
* Blow dry with N_2

6. Top ohmic metallization

i. Standard solvent clean

* Acetone soak, 5 min
* Toluene soak, 5 min
* Acetone soak, 5 min
* Methanol soak, 5 min
* Blow dry with N_2

ii. Coating top side with photoresist

* Puddle AZ9260
* Spin at 4000 rpm, 30 sec, ramp 4 sec
* Soft bake at 110°C, 3 min

ii. Pre-deposition clean process

* Load in Branson Asher on a glass slide for descum
* Set O_2 flow = 14/6, Ar flow = 135, Power = 100 W
* Run for 1 min
* BOE dip in an acid hood
* BOE soak, 10 sec

* Rinse in DI thoroughly
* Blow dry with N_2

iii. Metal depostion process in PVD sputtering system

* Load in PVD sputtering system
* Set the power = and source = Al
* Run for 200 min

iv. Stripping photoresist by solvent

* Soak in remover PG at 80°C, long time (preferably overnight)
* Soak in IPA, RT, 10 min
* Blow dry with N_2

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