FABRICATION AND CHARACTERIZATION OF SILICON PHOTONIC DEVICES

by

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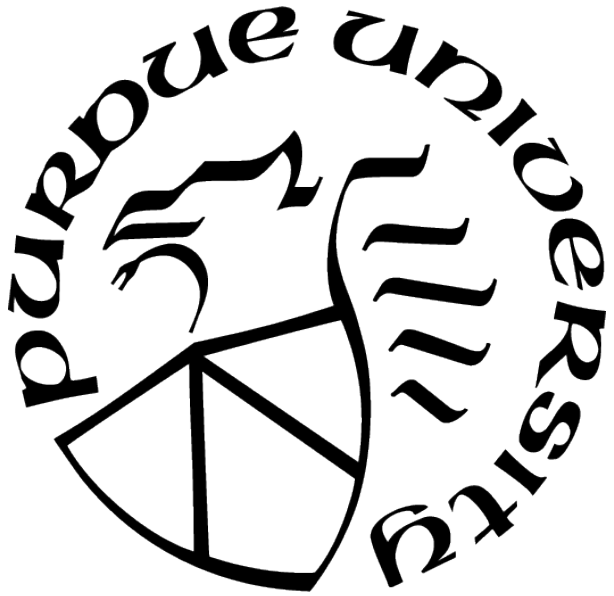

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This thesis is dedicated to my son

Izaan Abdullah,

who not only supported and inspired me

during my whole PhD life,

but also sacrificed a lot.

I love you, Son.

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LIST OF SYMBOLS

c	Velocity of Light
v_g	Group Velocity
ϵ	Electric Permeability
μ	Magnetic Permittivity
ω	Angular Frequency
λ	Wavelength of Light
β	Propagation Constant
ψ	Spectral Phase
β_2	Second Order Dispersion
D	Dispersion Coefficient
T	Transmittance
n_2	Kerr Non-linearity
f_{CEO}	Carrier Envelope Offset Frequency
κ	Coupling Coefficient
Q	Quality Factor
n_g	Group Refractive Index

ABBREVIATIONS

SOI	Silicon on Insulator
FSR	Free Spectral Range
TE	Transverse Electric
TM	Transverse Magnetic
E-skid	Extreme Skin Depth
AMM	Anisotropic MetaMaterial
TIR	Total Internal Reflection
IPA	Isopropyl Alcohol
DI water	De-Ionized water
BOE	Buffered Oxide Etch
HSQ	Hydrogen silsesquioxane
RPM	Revolution per Minute
TMAH	Tetramethylammonium hydroxide
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
MMI	Multi Mode Interference
WDM	Wavelength Division Multiplexing
PDM	Polarization Division Multiplexing
MDM	Mode Division Multiplexing
ADC	Asymmetric Directional Coupler
HSQ	Hydrogen silsesquioxane
DKS	Dissipative Kerr Soliton

ABSTRACT

Silicon photonics has become one of the leading candidates for the next generation optical communication platform. In addition to being an inexpensive material and compatible with Complementary metal–oxide–semiconductor (CMOS) manufacturing, silicon exhibits low absorption at optical telecommunication bands. However, high propagation loss and poor light confinement in narrow Si waveguides have limited high-density optical integration. In this work, we show the fabrication and characterization of a novel type of devices named E-skid devices that can reduce the skin depth and suppress the large spatial content of evanescent light. These devices use artificial anisotropic dielectric metamaterial to suppress the evanescent waves. Beside E-skid devices, we also discuss the fabrication and experimental characterization of mode filters using Silicon on Insulator that can block the fundamental TE_0 and allow the higher order modes to pass through using Multi Mode Interference. In this work, the mode is filtered using radiation, not by reflection.

Beside Silicon, Silicon Nitride has also gained much interest because of its low loss, smaller nonlinear absorption and higher Kerr effect. Silicon Nitride waveguides have widely been used for lots of applications specially the optical frequency comb generation. One special case of coherent optical frequency comb is Soliton in which case the non-linearity and dispersion cancel each other's effect and keep the pulse without distortion. In this work, we described the Silicon Nitride fabrication process and did a comparative analysis with other research groups who fabricates similar devices. We tried to improve our process by inserting a few additional steps in our fabrication process. We also investigated our process step by step and found out reasons for our low quality factor and low yield. We found a few factors that might be responsible for the low quality factor and addressed them. We fabricated real devices using our modified process and saw improvement in quality factors, yield and thermal performance of the devices.

Finally, we describe an edge polishing method for Silicon Nitride microring resonator devices, which we developed from scratch and we can polish edges down to sub-micron level.

Thus, the edges become optically flat and it allowed us to do heterogeneous integration with an Indium Phosphide chip. This paves away for some exciting opportunities like on-chip frequency comb generation.

1. INTRODUCTION

Silicon photonics has become one of the leading candidates for the next generation optical communication platform which uses Silicon as an optical medium to guide an optical mode. The fabrication cost of Silicon photonics has also been affordable due to the massive development in CMOS industry as they share the same material. From optical perspective, Silicon has the advantage of having low absorption in telecommunication C-band (1530nm-1565nm). Therefore, Silicon has been used to develop on-chip laser sources [1], optical waveguides [2], Electro-optic modulators [3], integrated photodetectors [4], on-chip Mode Division Multiplexing [5] etc. However, the demand for increasing density and miniaturization of these components has led to technological challenges in their manufacturing and operation. Also, Silicon suffers from two-photon absorption and subsequent free-carrier injection [6] which limit the nonlinear efficiency of the medium. Therefore, for nonlinear applications such as Kerr Frequency Comb generation [7], Silicon Nitride is preferred, which has a lower loss, greater thermal stability and no Two Photon Absorption (TPA) process.

The first part of this report contain works that is based on Silicon-on-Insulator (SOI) for some light confinement devices [8] and mode filters using Multi Mode Interference (MMI) which are described in Chapter 2 and 3 respectively. The rest of the chapters (chapter 4, 5 and 6) are based on Silicon Nitride devices, more specifically Silicon Nitride microring resonators that are designed for the purpose of Optical frequency comb generation. Before going into the details, we will focus on some basic terminologies first in the following section.

1.1 Light Confinement Techniques in Photonic Waveguides

1.1.1 Crosstalk

Crosstalk can be defined as the interference between the signals that are propagating on various line or channel in the same system. It is a phenomenon by which the light transmitted in one photonic waveguide or channel of a system creates an undesired effect in another waveguide or channel. It results from coupling of energy from electromagnetic fields gener-

ated by neighboring lines and is highly undesirable as it increases the loss for that line or channel.

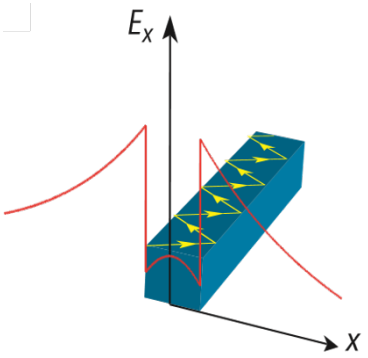
Miniaturization of photonic chips and dense integration has always been a challenge due to the fact that as the size goes down, it becomes harder to confine the light within the structure. Also, the large spatial extent of evanescent light waves during coupling results in high crosstalk and high radiation loss [9].

1.1.2 Light Confinement Techniques

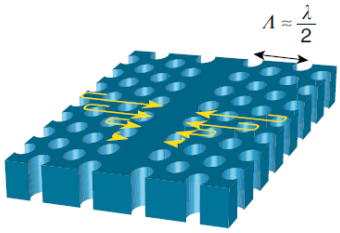
One of the ways to confine lights in photonic devices is to use plasmonic structures [10], [11]. They can strongly reduce the bending loss and crosstalk because of the sub-diffraction nature of the coupling of light [12]. But the inherent large ohmic loss of metals limits their use for photonic integration [13], [14].

All dielectric structures has been considered a potential solution to that problem and a few all dielectric structures were considered in recent years to make the miniaturization possible [15]–[17]. Fig.1.1 shows a few different classes of dielectric waveguides that were used to confine light in photonic chips.

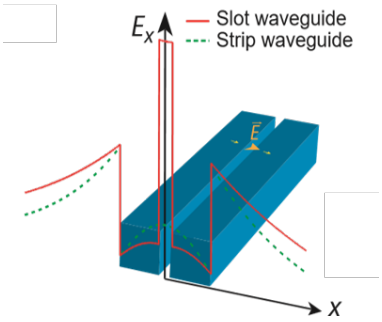
Fig 1.1a illustrates the most common type of waveguide for guiding light in SOI chip-Strip Waveguides. In this type of waveguide usually the higher index Silicon channel is surrounded by lower index Silicon Dioxide.Due to the high contrast of the refractive index between the core and the cladding, light is usually confined into the core waveguide because of the total internal reflection [9]. The problem with these kind of structures is that when we try to reduce the core size, the mode starts to increase and that creates a stumbling block in its miniaturization [18].



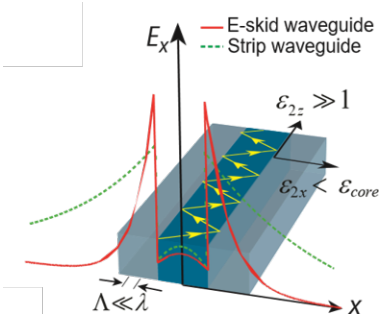
(a) Strip Waveguide



(b) Photonic Crystal Waveguide



(c) Slot Waveguide



(d) E-skid Waveguide

Figure 1.1. All Dielectric Waveguides for light confinement in SOI. The Skin Depth of E-skid waveguide is shorter compared to other waveguides. This picture is reproduced from [8].

Fig 1.1b illustrates Photonic Crystal Waveguides that can confine light inside a line defect using Bragg Reflection[19]. These waveguides can work very efficiently with sharp bends[20] overcoming the radiation loss at sharp bends. However, the integration density for these kind of waveguides are limited due to the fact that the periodicity of Bragg reflector is on the order of the wavelength. Also, these kind of waveguides cannot be perturbed by any other nearby waveguides[21].

Fig 1.1c illustrates the slot waveguides, which are an opposite arrangement compared to the strip waveguide. In this kind of waveguide, a sub-wavelength low index gap is surrounded by high index dielectric rods [22]. For this kind of arrangements, the electric field peaks inside the gap which leads to light confinement. But at the same time, it causes skin-depth expansion in the cladding, which results in crosstalk between adjacent waveguides and radiation loss at sharp bends making dense integration and miniaturization problematic.

Fig 1.1d illustrates the E-skid waveguides, which is fundamentally different from the other approaches and uses all-dielectric anisotropic metmaterials. The confinement of light in this kind of waveguides is based on the photonic skin-depth engineering of evanescent waves in the cladding. This is possible due to an additional degree of freedom in Total Internal Reflection (TIR) which is described in [18], [23]. The relaxed condition enables the control of evanescent wave decay which in turn reduces crosstalk and bending loss.

In E-skid devices, the anisotropic metamaterials is used as cladding and the dielectric waveguides are fabricated on a monolithic Silicon-On-Insulator (SOI) platform. As a consequence of decay control, the crosstalk is reduced down to -30dB in the photonic circuit [8].

1.2 Microring resonator

An optical microring resonator is a set of waveguides which consists of one or more input or output bus waveguides, through which the power is sent or received and one or more

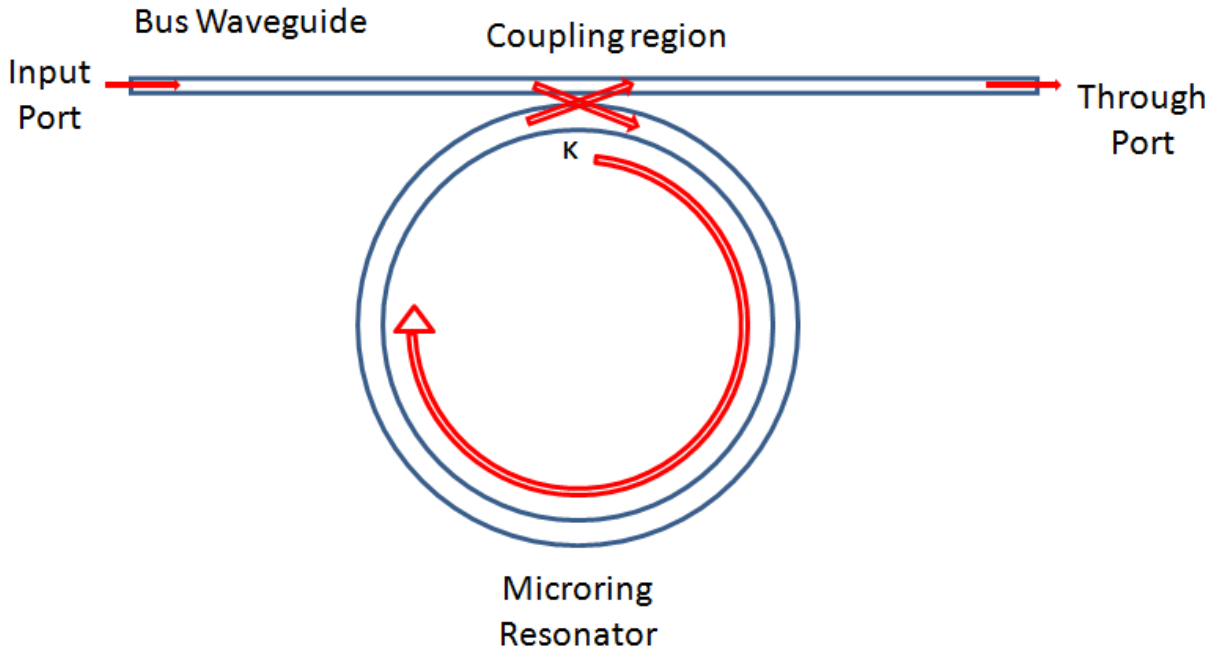
closed waveguides in which power is coupled and circulated. The closed waveguide can be of any shape, but the most common shape is a circular ring. A microring resonator usually has two ports, an input port, through which the light is sent in and a through port by which light comes out as shown in Fig 1.2a.

When there is through port only, there is only one waveguide and the input light couples inside the microring via the coupling coefficient κ, circulates around the cavity. We only have one coupling region in this case. But occasionally we have another port, which is called drop port.

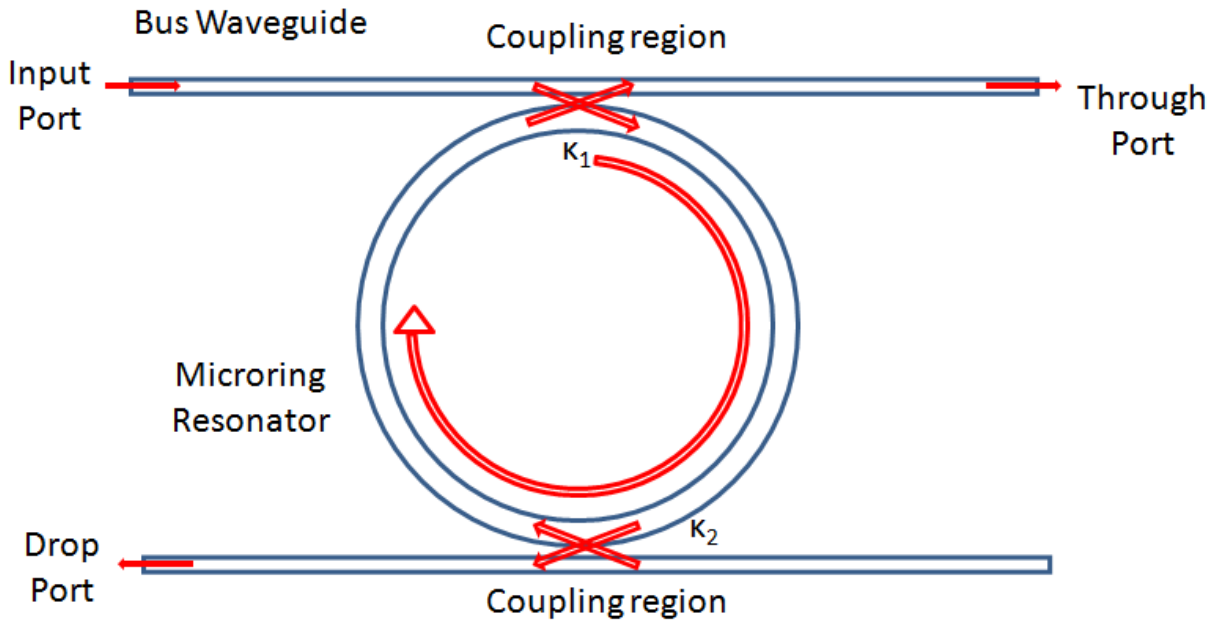
When we have drop port in design that usually couples power from the field that develops inside the microring. So a separate waveguide takes power from the ring after the ring takes power from the input bus waveguide as shown in Fig. 1.2b. In this case we have two coupling regions. The input light couples inside the microring via the coupling co-efficient κ_1 and the light is again coupled to the drop waveguide from the ring via another coupling co-efficient κ_2 and reaches the drop port.

When we send some light through the input waveguide of the microring resonator, some part of light is coupled to microring depending of the wavelength of the light and some of the design parameters of the microring, the rest of the light is transmitted to the output port via the input bus waveguide. The coupled light circulates inside the cavity by internal reflection and suffers some losses due to sidewall roughness, intrinsic absorption of waveguide material and scattering losses due to bending at the edges.

On the other hand as the light completes one round trip, it interferes with the incoming light constructively and thus the light intensity inside the microring is build up. The coupling of light critically depends on the gap between the ring and the input bus waveguide, the effective coupling length along which the coupling of light takes place and the refractive index of the medium between the two waveguides.



(a) Microring with through port only



(b) Microring with both through port and drop port

Figure 1.2. The basic structure of a microring resonator a) with through port only b) with both through and drop port

Transmission Spectrum

The transmission spectrum is obtained by plotting the transmittance for the system. Transmittance is defined as the ratio of the transmitted power to the input power. Let us consider a microring resonator without the drop port as shown in Fig. 1.2a. It has through port only and through the input port we send some light from a laser source and receive the output light from the through port. Transmission spectrum can be obtained by measuring transmittance. The transmittance for such structures can be written as [24]:

$$T = \frac{(\lambda - \lambda_0)^2 + (\frac{v_g \lambda^2}{8\pi^2 Rc})(\kappa_c^2 - \kappa_i^2)^2}{(\lambda - \lambda_0)^2 + (\frac{v_g \lambda^2}{8\pi^2 Rc})(\kappa_c^2 + \kappa_i^2)^2} \tag{1.1}$$

Where, λ_0=resonant wavelength of the microring,κ_c^2= fraction of power losses due to coupling of power to the ring from bus waveguide, κ_i^2=fraction of intrinsic power losses. A sample transmission spectrum is shown in Fig. 1.3.

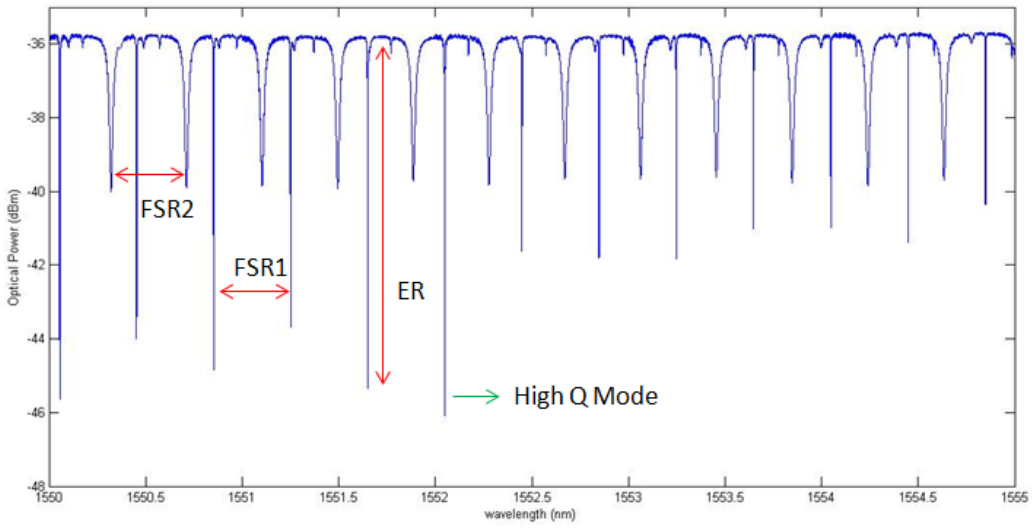


Figure 1.3. A sample Transmission Spectrum for a Microring Resonator. Each dip corresponds to a resonance frequency that the microring resonator can support

Some important terms related to Transmission Spectrum are Free Spectral range (FSR) and Extinction Ratio (ER).

Free Spectral Range (FSR)

Free Spectral Range (FSR) of an optical microresonator is defined as the spacing in frequency or wavelength between two maxima of the dropped power or minima of the through power. FSR can be obtained from transmission spectrum very easily. It is just the difference between two successive resonance frequencies or wavelengths for the same mode family.FSR for different mode families are different. If a microresonator can support multiple modes, then the fundamental mode usually has the highest FSR. Fig 1.3 shows a sample transmission spectrum and FSRs for two different mode families are termed as FSR_1 and FSR_2. Mathematically, FSR can be defined (in frequency) as [25]:

$$FSR_f = \Delta f_{FSR} = \frac{c}{n_g L} \tag{1.2}$$

Where, c= Velocity of light, n_g= Group index of the cavity material, L=Length of the cavity. FSR is also the inverse of round-trip time. If the round-trip time for the cavity is T_R, then:

$$T_R = \frac{1}{FSR_f} = \frac{n_g L}{c} \tag{1.3}$$

Extinction Ratio (ER)

Extinction ratio (ER) is fundamentally defined as the ratio of two optical signals generated by an optical source. Mathematically, we can express it as-

$$ER = \frac{P_2}{P_1} \tag{1.4}$$

Where, P_2 is the received power and P_1 is the transmitted power. Usually it is expressed in dB units, in which case we write it as:

$$ER = -10log\frac{P_2}{P_1}(dB) \tag{1.5}$$

For microring resonator, Extinction Ratio (ER) can be defined as the ratio between transmitted power and input power. It can simply be obtained from the transmission spectrum. The difference between the maximum and minimum point in a particular resonance gives us the Extinction Ratio. For example if we see Fig 1.3, the Extinction Ratio for the marked resonance is around 10.5 dB. Extinction Ratio is also important because if ER is too small, then we cannot probably use that for comb generation. Thus Extinction Ratio plays a vital role in the application of microring resonator.

Quality Factor (Q)

Quality factor or Q factor is a dimensionless parameter that is used for defining the strength of damping of an oscillator. It was initially developed for electronic circuits, but later became very commonly used for photonic cavities or resonators. Quality factors can be defined by two ways:

From oscillator point of view, Q factor is approximately defined as the ratio of the initial energy stored in the resonator to the energy lost in one radian of the cycle of oscillation [26]. Alternatively, Quality Factor can be defined as the ratio of a resonator's resonant frequency to its the full width at half-maximum (FWHM) bandwidth when subject to an oscillating driving force. High Q corresponds to a lower rate of energy loss and low damping. Usually that corresponds to low loss in microring resonators. For microring resonators, Quality factor can be defined as:

$$Q = \frac{\lambda_0}{\Delta\lambda} = \frac{\Delta f}{f_0} \tag{1.6}$$

where, λ_0 is the resonant wavelength, f_0 is the resonant frequency, $\Delta\lambda$ and Δf is the Full Width at Half Maximum (FWHM).

Dispersion

The word dispersion generally means the action or process of distributing things over a wide area. In Optics the term dispersion results in similar type of thing- spreading of the pulse. Dispersion causes different frequency components to travel at different velocities, resulting in the pulse broadening. When the pulse is broadened it actually can cause a lot of unwanted situations including distortion of data. Dispersion is a very important parameter for microring resonator. The comb generation process depends on the type of dispersion. Also, it is crucial as it limits the maximum achievable comb bandwidth [27].

In fiber optics, dispersion is usually described in terms of dispersion co-efficient (D) which can be expressed as [28]:

$$D = \frac{\partial \beta_1}{\partial \lambda} = -\frac{2\pi c \beta_2}{\lambda^2} \tag{1.7}$$

where, β_1 is the first order dispersion, which is the inverse of group velocity v_g and it can be expressed as [28]:

$$\beta_1 = \frac{\partial \beta}{\partial \omega}|_{\omega=\omega_0} = \frac{1}{v_g} \tag{1.8}$$

The term $\beta_2 = \frac{\partial^2 \beta}{\partial \omega^2}$ is called Group Velocity Dispersion (GVD). The unit of D is ps/nm-km and it actually gives the group delay difference of two optical pulses after propagating certain distance in the optical fiber at certain wavelength. Depending on the sign of D we define two distinct type of dispersion:

1) When D>0, the dispersion is called Anomalous Dispersion.

2) When D<0, the dispersion is called Normal Dispersion.

It is worth mentioning that the frequency comb generation principle is entirely different for these two type of dispersion regimes which is explained later.

1.3 Optical Frequency Comb

Optical Frequency Combs are evenly spaced periodic spectral lines, which are discrete and the spacing between individual comb lines are constant along the whole spectrum. Thus an optical frequency comb can be used as an optical ruler because if we know the comb frequency we can find any unknown frequency by beating that with the optical frequency comb. Optical frequency combs have been useful in many applications such as comb spectroscopy [29], molecular fingerprinting [30], astronomical calibration [31], arbitrary waveform generation [32] etc.

Optical frequency combs can be generated in many ways, but the most common method is using a mode-locked laser with stable frequency and repetition rate. Fig. 1.4 shows an example of mode locked frequency comb [28]:

In general, the frequencies of individual comb lines for a frequency comb can be expressed as [28]:

$$f_m = m f_{rep} + f_{CEO} \tag{1.9}$$

where, f_{rep}=$\frac{1}{T}$ is the repetition rate of the laser, T is the period of the optical pulse as shown in Fig. 1.4b and f_{CEO} is the carrier envelope offset frequency=$\frac{\delta\omega}{2\pi}$. The carrier envelope offset occurs from the phase slip due to the carrier phase velocity v_p being faster than the envelope group velocity v_g. The difference in those two velocities arise from the group velocity dispersion inside the cavity. One useful thing about microring resonator is that the FSR can be controlled very easily. Also microring resonator allow us to reduce the size and

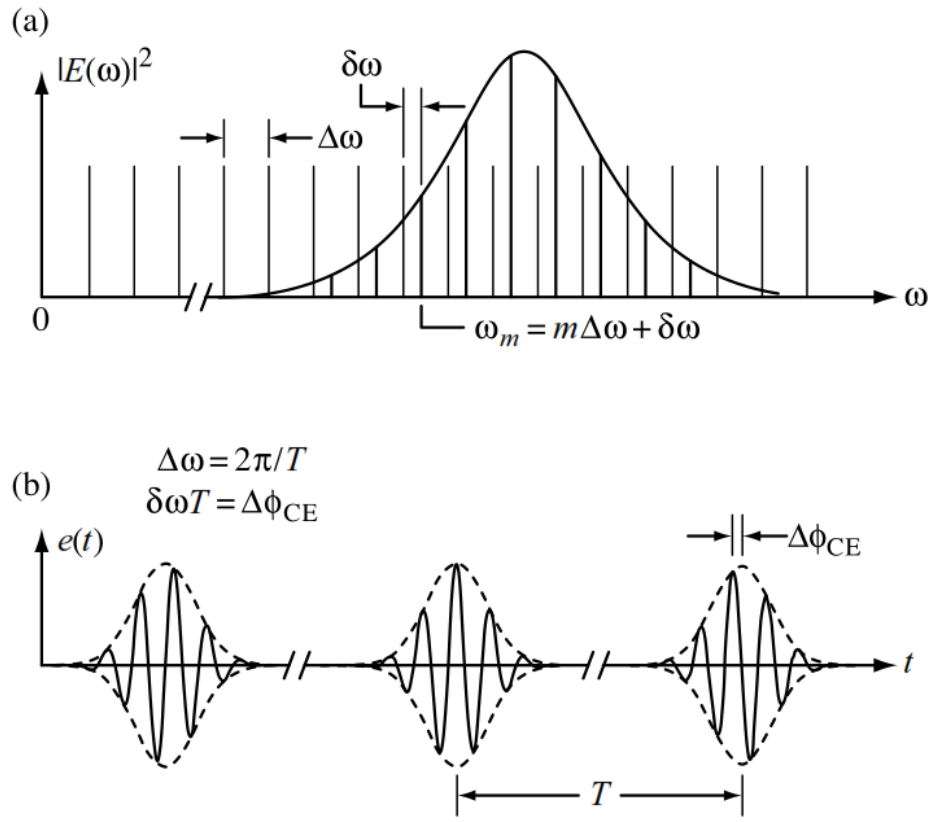
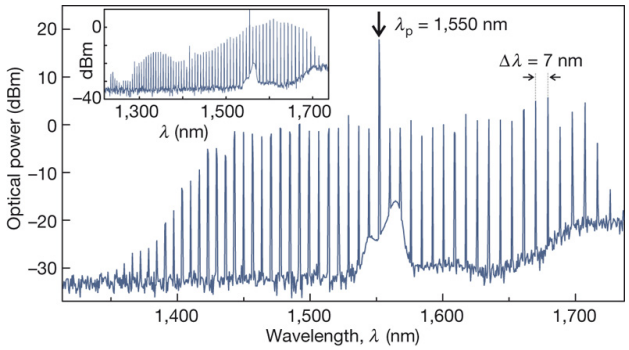


Figure 1.4. Mode-locked frequency comb a) The offset frequency $\delta\omega$ is shown b) Pulse to pulse phase shift $\Delta\phi_{CE}$ is shown. The picture is taken from [28]

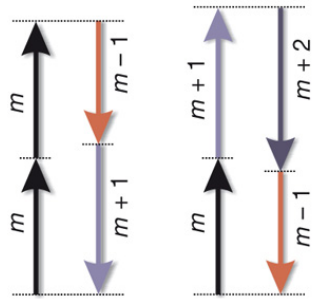
can be implemented in chip level. So, for obtaining high repetition rate combs microring resonators have become very popular recently.

The optical frequency comb in microring resonators are generated by a parametric frequency conversion which is based on the Four Wave Mixing (FWM) process. The parametric conversion must follow both the energy and the momentum conservation law. In this process two pump photons (ω_p) are absorbed at sufficient power and two sidebands are generated as [33]:

$$2\omega_p = \omega_s + \omega_{\mathrm{i}} \tag{1.10}$$



(a) A broadband Optical Frequency comb



(b) Degenerate & non-degenerate FWM

Figure 1.5. An example of Optical Frequency comb generated from microresonator via the parametric frequency conversion process. Fig a) shows the broadband frequency comb and Fig. b) shows the difference between degenerate and non-degenerate FWM process. The figure is taken from [7].

where $\omega_s = \omega_p + \Delta\omega$ and $\omega_\mathrm{i} = \omega_p - \Delta\omega$ are generated sidebands which must be equidistant to maintain energy and momentum conservation law. Now this process continues and the whole frequency comb is formed. If two pump photons generate sidebands, they are usually called degenerate FWM. When one photon from pump interacts with one photon from nearby sidebands and create two new sidebands, then it is called non-degenerate FWM. An example of frequency comb generated from microring resonator is shown in Fig 1.5.

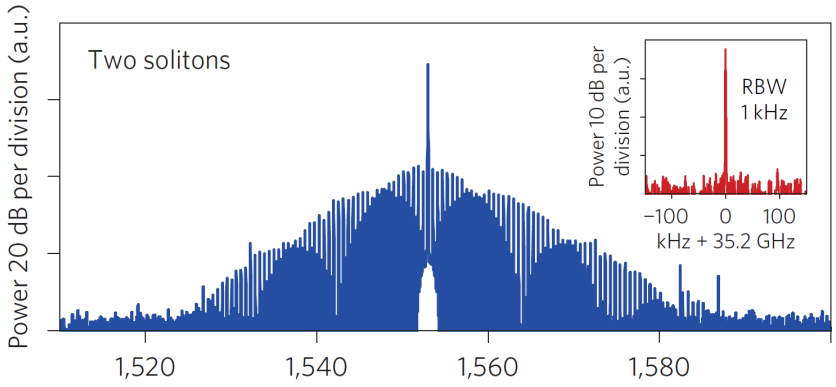
Solitons

As mentioned in the previous subsection, the comb initiation process inside the microring resonator is created by an interaction between Kerr nonlinearity and group velocity dispersion, which is called modulational instability. Anomalous dispersion regime inherently supports modulational instability, so frequency comb generation in anomalous dispersion regime has been very popular and widely investigated [7], [34]–[36]. On the other hand, Kerr frequency comb generation in normal dispersion was initially thought to be impossible because of the lack of modulational instability. Later, it has been found that the mode

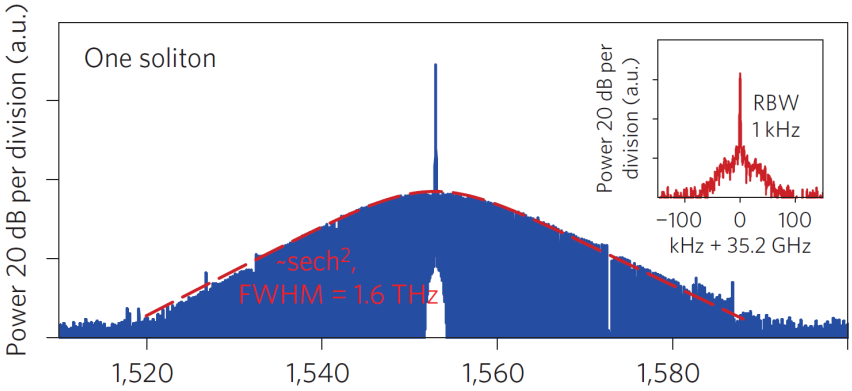
coupling between adjacent mode families can generate modulational instability in normal dispersion regime and hence Kerr frequency comb generation in normal dispersion regime is possible [37], [38]. However, the mode interaction in normal dispersion regime was based on accidental degeneracies between spatial modes and hence thermally controlled mode interaction based frequency comb generation in normal dispersion regime was demonstrated later [39].

A critical issue for most of the application of the comb generation is the requirement of high temporal coherence. In anomalous dispersion regime, coherence can be obtained by soliton mode-locking [40]. A similar kind of route but with a different terminology and physics leads to coherence in normal dispersion regime through dark-pulse mode-locking [41]. The coherence in normal dispersion regime is usually repeatable and dark-pulse number is deterministic [41]. On the other hand, anomalous dispersion regime exhibits stochastic soliton number and the soliton number in most of the cases are greater than 1 [42], [43]. In most of the applications, single soliton is preferred because it has a smooth spectra with single Free Spectral Range (FSR) and greater coherence. The frequency comb spectrum with multi (two) soliton and single soliton are shown in Fig 1.6 [40].

In general, Dissipative Kerr solitons (DKS) generation requires the balance between the loss and gain in an active media, along with the balance between nonlinearity and dispersion. Despite the similarity between the DKS formation and soliton mode-locking in femtosecond lasers, DKS does not require additional saturable absorbers to stabilize them. Also in DKS, the pump laser frequency is a part of the soliton spectrum unlike the fiber soliton which does not require a continuous pump. The external coherent pump provides a central control parameter of the soliton and in addition constitutes one of the comb lines—which has no counterpart in conventional mode-locked lasers [44].



(a) Two Soliton



(b) Single Soliton

Figure 1.6. Frequency comb generation spectrum with (a) Multiple (two) soliton (b) Single soliton. Single soliton spectrum exhibits smoother $sech^2$ profile. Figures are reproduced from [40].

1.4 Organization of the report

In chapter 2, we will discuss about E-skid devices that utilizes all dielectric metamaterial structures that reduce the decay length of evanescent light. We also discuss the fabrication details of such devices, the crosstalk and the propagation loss measurement. Low crosstalk and propagation loss make these devices suitable for miniaturization and dense integration.

In chapter 3, we will discuss the fabrication and measurement of some mode filters using Multi Mode Interference (MMI) intended for on-chip Mode Division Multiplexing (MDM). The filters can effectively filter out the fundamental TE_O mode and allow the higher TE_1 mode to pass be means of radiation.

In Chapter 4, we will discuss the fabrication process of Silicon Nitride microring resonators and all the improvements that we incorporated to the fabrication process after doing a comparative analysis with other groups. We will discuss some of our investigation into our process and some issues that might be responsible for our low Quality factors. Finally we show some characterization results of some devices that were fabricated with our modified process.

In chapter 5, we will discuss the microheater fabrication process. We will show how we explored different materials and combinations to improve our microheater performance and how we ended up successfully fabricating what was needed for one of our projects.

In Chapter 6, we will discuss about the edge polishing process that we developed from the scratch. This process make the edges of our chips optically flat which allows heterogeneous integration paving ways for on-chip frequency comb generation.

Finally in the summary chapter, we summarized all the works.

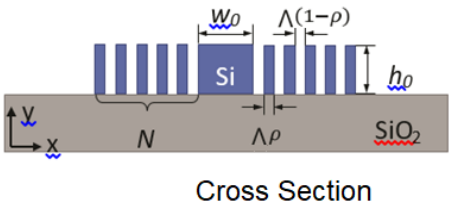
2. FABRICATION AND LOSS CHARACTERIZATION OF E-SKID DEVICES

2.1 Motivation and Goal

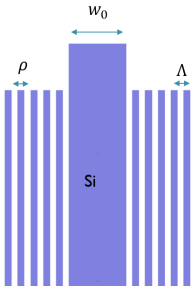
Large spatial extent of evanescent light waves generated during nanoscale light confinement has always been a major stumbling roadblock to miniaturization. In this chapter, we will discuss the fabrication and loss measurement of a very exciting and new type of devices that can improve the evanescent coupling of light [8]. The major idea of this work is the introduction of anisotropic metamaterials (AMM), which opens a new degree of freedom in total internal reflection (TIR) to reduce the decay length of evanescent waves. The devices were termed as E-skid devices because they work at the extreme skin depth condition of the Silicon. Relatively negligible propagation loss and low crosstalk of these devices makes them suitable for improved photonic integrated circuits.

2.2 Fabrication of E-skid Devices

The cross section and the top view of the E-skid devices along with design parameters are shown in Fig 2.1.

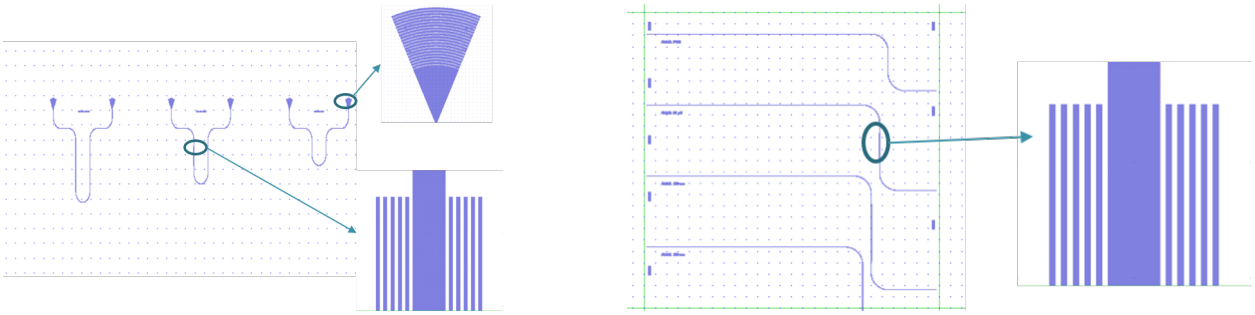


(a) Cross Section



(b) Top view

Figure 2.1. The design parameters of the E-skid devices. (a) Cross Section and (b) Top view. Here, w_0= Width of the Silicon waveguide= 450nm, h_0= Height of the Silicon waveguide= 220nm, ρ= Width of the AMM structures= 50nm, Λ= Spacing between AMM structures= 50nm, N=Number of parallel AMM structures in each side= 5. The cross section is reproduced from [8]



(a) Cross Section (b) Top view

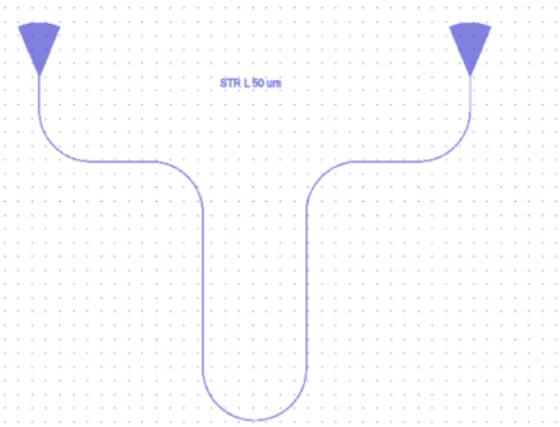
Figure 2.2. Two different layout schemes for E-skid Devices (a) Grating Coupling Scheme (b) Edge Coupling Scheme. For the final devices we proceed with grating coupling schemes because it needed less number of steps to complete the fabrication.

For the fabrication of E-skid devices, we tried both the grating coupling scheme and edge coupling scheme as shown in Fig 2.2. The lengths of AMM structure for loss measurement were same, just the coupling region and the main waveguide was different. Initially, we proceeded with the fabrication for both the layouts. But in the end, we decided to go ahead with the grating coupling scheme because it required less number of steps and less time to finish the fabrication process.

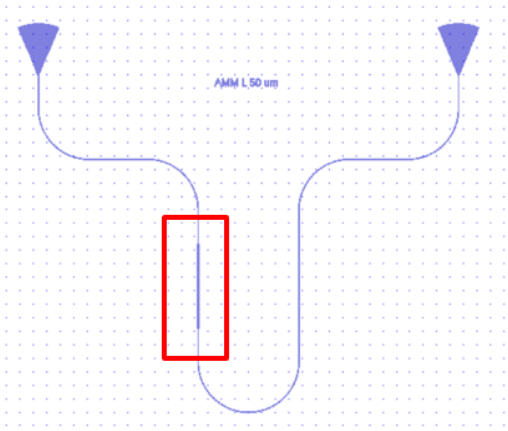
For the purpose of loss measurement, we made 3 different kind of layouts. One layout didn't have any AMM structures, which we called the reference devices (Strip waveguides) (Fig 2.3a). Another one had AMM structures in only one of the arms (Fig 2.3b) and the third one had AMM structures in both the arms (Fig 2.3c) for the grating coupler scheme. The lengths of the straight section of the e-skid and strip waveguides were varied from 0 to 1.8 mm. All the measurements were combined together to find an average value of loss for the E-skid devices, which is described in next subsection.

2.2.1 Fabrication Method

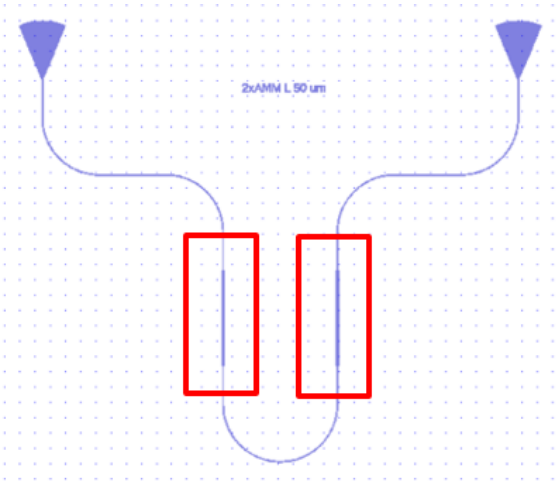
The devices were fabricated on a SOI wafer, which had a 220 nm of Silicon on top of a 2 μm Silicon Dioxide. Initially, we cleaved a small rectangular SOI piece from the large wafer, the typical size of the pieces were 50 mm $\times$ 40 mm. After cleaving, the piece was cleaned



(a) Reference Structures



(b) AMM on one arm



(c) AMM on both arms

Figure 2.3. The three different Layouts for loss measurement (a) Without any AMM structures (b) AMM structures in one arm only (c) AMM structures in both arms

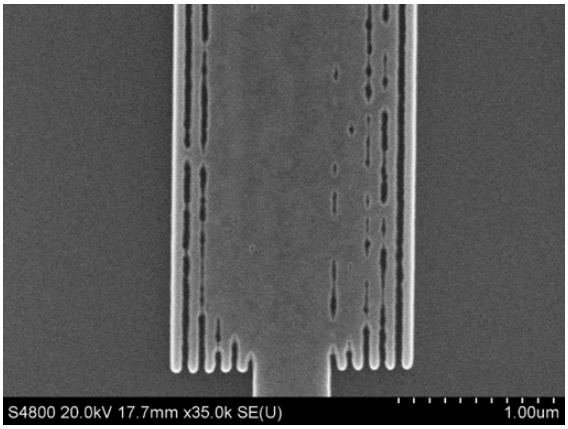
with general solvents (Toluene, Acetone, Methanol, IPA, DI water and then blow dried with Nitrogen Gun). After that, a 5s Buffered Oxide Etch (BOE) dip was done to remove native oxide. After removing native oxide, we baked the piece at 120 degree Celsius to drive away all the solvents from the piece. After that, we spun 6% HSQ on the SOI piece at 6000 rpm for 30 seconds with a ramp of 3 seconds. The soft bake is done at 120 degree Celsius for 3 minutes, after which the sample is ready for E-beam writing.

The E-beam writing was done on RAITH EBPG5200 e-beam writing machine from University of Notre Dame's Nanofabrication facility. We used a field size of 500 μm, a beam current of 1nA and a dose of 2400 $\mu C/cm^2$. After the writing was finished, the sample were developed using a 25% TMAH solution for 70 seconds. Then the sample undergoes Chlorine dry Reactive Ion Etching (RIE) in Panasonic Etching machine for about 9 minutes. Finally the sample is cleaned with solvent and ready for measurements.

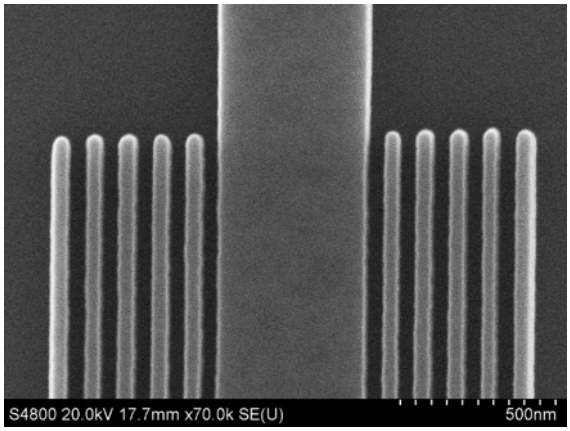
2.2.2 Fabrication Challenges

There were lots of challenges in the fabrication of E-skid devices. The first challenge we faced in this fabrication was to optimize all the process steps. We had to try different spin speeds for depositing e-beam resist on top of the wafer. We had to optimize our new baking time and temperature according to the thickness of the e-beam deposited from spins. We had to do dose test in e-beam writing. We also tried Proximity Error Correction (PEC), which takes care of the charging effect by distributing the dose according to the structure density to improve the writing instead of using a constant dose. We also found that the etching rate was proportional to the sample size. So we had to try different etching time in order to etch away all the materials that were required to remove. Fig 2.4 shows the effect of dose on structure writing.

Secondly, since the AMM structures were very small we had lots of difficulty in their stability. In our first few attempts, we observed that the structures were peeling off. It was happening because of the high surface tension of water, which we had been using to clean

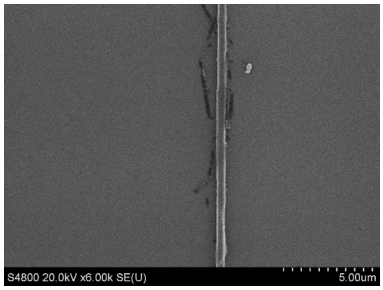


(a) Without Proper Dose

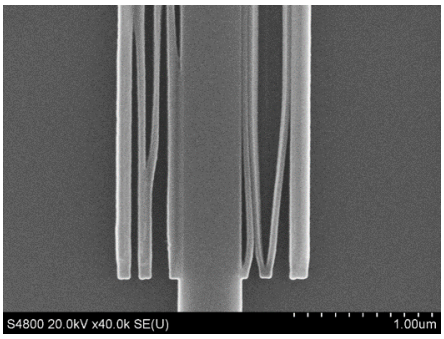


(b) With Proper Dose

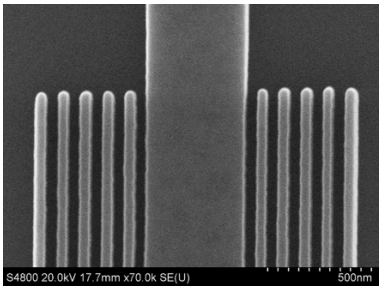
Figure 2.4. The effect of dose on structure writing. SEM image of the devices (a) With an unsuitable dose, where the structures merged together (b) With a suitable dose, where the structures are clear and distinct.



(a) Totally Broken structures



(b) Partially Broken structures



(c) No Broken Structures

Figure 2.5. The effect of high surface tension of water on AMM structures. SEM images of (a) Completely Broken AMM structures (b) Partially Broken AMM structures (c) No Broken AMM structures (used IPA instead of water)

the developer solution after development. Therefore, we stopped using water and used Iso-Propyl Alcohol (IPA) in our last step. IPA has a weaker surface tension compare to water, and it helped us to keep our structures intact.

2.3 Crosstalk measurement

To verify the low crosstalk and high density waveguides scheme with an anisotropic metamaterial (AMM) cladded waveguide , we fabricated and tested the devices. Figure 2.6a shows the layout and SEM images of a fabricated device.

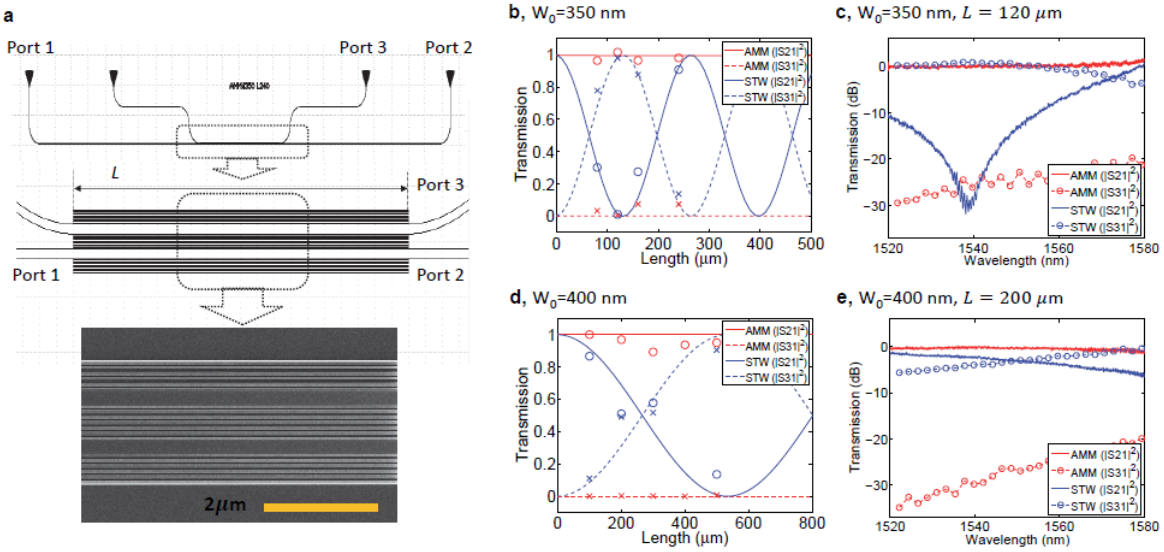


Figure 2.6. Experimental demonstrations of low crosstalk with metamaterial sidewalls. (a) Layout and SEM images of the device. (b)(d) Measured power transmissions as a function of device length, when the core widths are (b) w_0 = 350 nm and (d) w_0 = 400 nm, respectively. Red and blue are the cases with anisotropic (AMM) metamaterial claddings and standard waveguides (STW) respectively. The circles and crosses are for $|S_{21}|^2$ and $|S_{31}|^2$, respectively. The simulated transmissions are also plotted: $|S_{21}|^2$ (solid line) and $|S_{31}|^2$ (dashed line). (c),(e) Measured power transmission spectra of (c) (L = 120 μm) and (e) (L = 200 μm) respectively; red and blue are the AMM and STW respectively, and solid lines are for $|S_{21}|^2$ and dashed circles are for $|S_{31}|^2$.

The insertion loss for the fabricated device is about 6 dB/facet. To avoid an undesired coupling between coupler waveguides before the metamaterial section, we bent one of the coupler waveguides with a tapering, to impose a phase mismatch. For comparison, the same geometries are used for the standard waveguides (STW), but without the metamaterial sidewalls. The total device length L is varied among other devices, and Figure 2.6b shows the

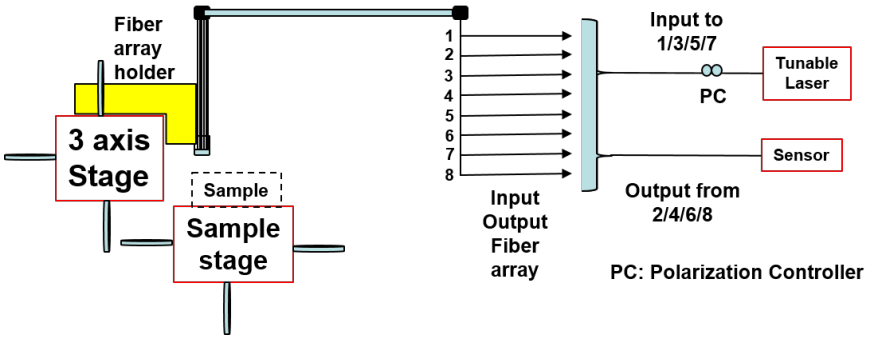
measured (circles for $|S_{21}|^2$ and crosses for $|S_{31}|^2$) and simulated (solid line for $|S_{21}|^2$ and dashed line for $|S_{31}|^2$) power transmissions as a function of L: with (red) and without (blue) metamaterial sidewalls. The w_0 and ρ are 350 nm and 0.5 respectively. The experimental results match well with the numerical results; in this length scale (< 500 μm), there is almost no crosstalk with metamaterials, while the conversion length is only about 130 μm without the metamaterials.

Figure 2.6c is the measured power transmission spectra when the device length is L = 120 μm. With metamaterials, $|S_{21}|^2$ is almost 0 dB through the measured bandwidth, while it's opposite for standard waveguides with almost complete crosstalk ($|S_{31}|^2 \sim 0$ dB). With metamaterial sidewalls, the extinction ratio between $|S_{21}|^2$ and $|S_{31}|^2$ is about 30 dB consistently. Without metamaterials, the extinction ratio varies between 0 dB and 30 dB with different wavelengths. In the standard waveguides, the rapid variation with different wavelengths is due to the short conversion length; shifting the wavelength effectively works as changing the device length. The crosstalk determines the conversion length, which limits the device bandwidth as well.

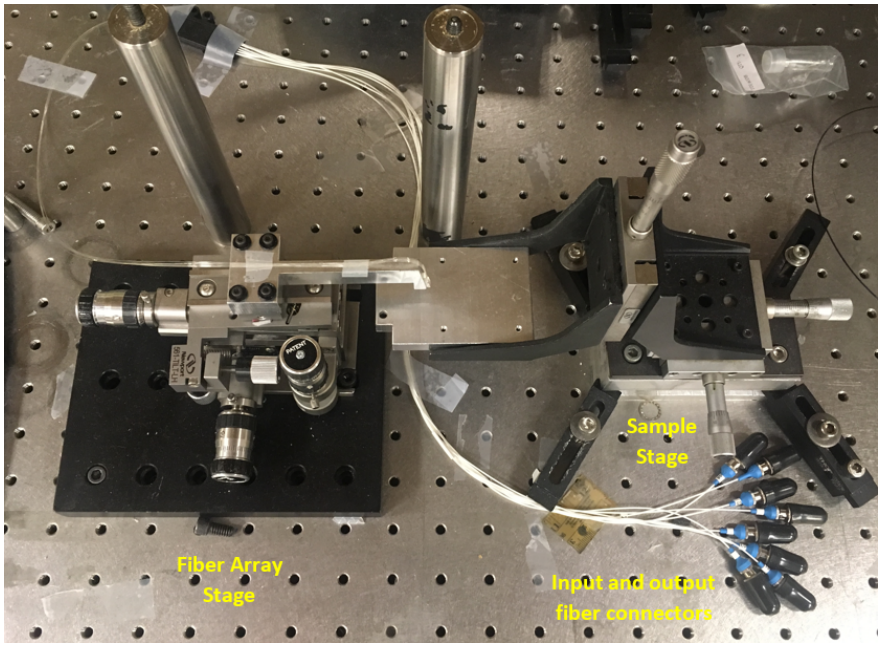
Figures 2.6d and 2.6e are the power transmissions that are similar to 2.6b and 2.6c, respectively, but with different waveguide core width $w_0 = 400$ nm. Notice that, in Figure 2.6d, the experimental and simulation results match well, and the trends, similar to those in Figure 2.6b, also can be observed, but with longer conversion length. Figure 2.6e is the transmission spectra when L = 200 μm; over the wavelength, the transmissions of standard waveguides are less sensitive than these in Figure 2.6c, due to the longer conversion length.

2.4 Loss Measurements of E-skid Devices

The loss measurement was performed using a grating coupler set up in which we used a tunable laser (Agilent 81680A) and a power sensor (HP 81632A). A schematic diagram and the major part of the real set up is shown in Fig. 2.7.



(a) Schematic Diagram



(b) Actual set up

Figure 2.7. The set up for loss measurement of e-skid waveguides (a) Schematic Diagram (b) Real set up with fiber array for coupling

The Sample lies on a stage that has very good control over 3 axes. The input-output fiber array was attached to a chuck that was mounted on top of another 3 axis stage which gives us better control for separation and alignment of the sample with the fiber array. Light goes into the chip and couples back to these fiber arrays from the grating structures from the chip. They have 250 μm separation between fibers, the same separation used in the layout. There was a polarization controller before the stage to control the polarization of the incoming laser light.

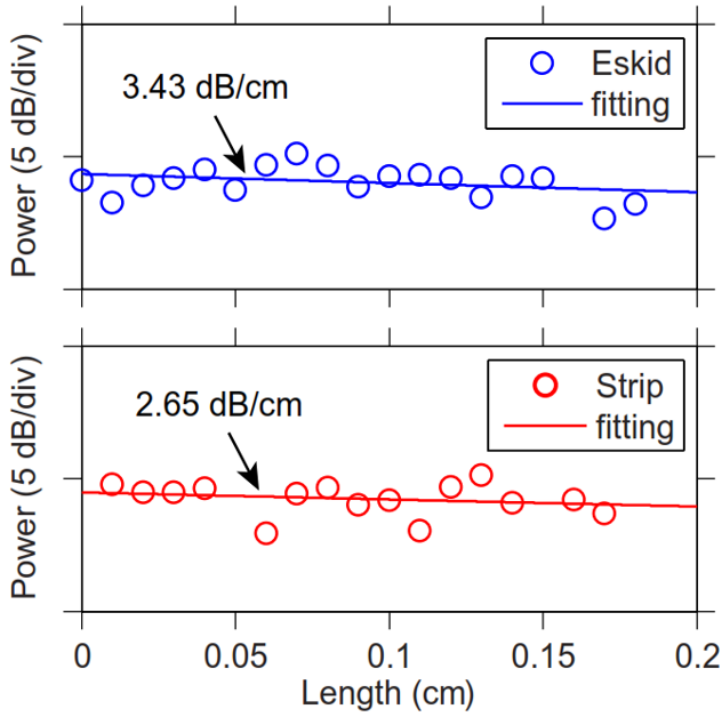


Figure 2.8. The Loss measurement of E-skid and the reference strip waveguides. The circle represents normalized transmission through E-skid (blue) and Reference strip (red) waveguides at λ=1550 nm. The propagation loss in e-skid and strip waveguide is 3.43 and 2.65 dB/cm at = 1550 nm, and the average losses for e-skid and strip waveguides for wavelengths between 1540 nm to 1560 nm are 3.67 dB/cm and 1.84 dB/cm, respectively, with a standard deviation of 1.0 dB/cm and 1.4 dB/cm, respectively. Figure reproduced from [8]

To measure the losses we scanned the laser from 1520 nm to 1600 nm and took the transmission spectrum after optimizing the coupling for each device. We first measured all the reference devices, then we measured all devices with AMM in it. From both set of data we extrapolated the loss for the AMM structures only. Fig 2.8 shows the transmission powers of e-skid (blue circles) and strip (red circles) waveguides at $\lambda_0 = 1550$ nm, for different device lengths.

Solid lines in each figure are the linear fitting curves that give the propagation losses of 2.65 dB/cm and 3.43 dB/cm to strip and e-skid waveguides, respectively. The propagation losses for strip and e-skid waveguides at different wavelengths have also been characterized. The average losses for strip and e-skid waveguides for wavelengths between 1540 nm to 1560 nm are 1.84 dB/cm and 3.67 dB/cm, respectively, with a standard deviation of 1.4 dB/cm and 1.0 dB/cm, respectively. This propagation loss of the e-skid waveguide is reasonable for compact devices, especially given that the cross-talk is improved significantly.

Finally, some performance comparison between the E-skid devices and other similar dielectric devices from literature are shown Table 2.1 [8].

Table 2.1. Performance Comparison between E-skid and other dielectric waveguides

Reference	**Cross Talk (dB)**	**Propagation Loss (dB/cm)**
Superlattice [45]	-20	>20
Adiabatic elimination [46]	-21.9	N/A
Inverse Design [47]	-22.9	>300
Dissimilar waveguides [48]	-20	N/A
Sinusoidal waveguides [49]	-26.8	>600
E-skid [8]	-30	3.67

Summary

In this part, we have described the fabrication technique of E-skid devices that opens up a new method for light confinement on chip and paves the way to miniaturization and dense integration. We discussed a few fabrication difficulties we faced on our way toward fabricating the devices and how we dealt with them. We showed different layouts for our fabrication which were intended for the loss measurement. We showed the crosstalk measurement, which showed that the devices have very low crosstalk. Finally, we showed how we measured the propagation loss and how that loss is comparable with other similar dielectric waveguides in literature.

Acknowledgement

The work was done in collaboration with Professor Zubin Jacob's group of Purdue University (USA). We are specially thankful to Saman Jahani, who developed this idea. We thank all other authors of the work [8] for their valuable contributions. We are thankful to the sponsors who sponsored this work. We want to thank Birck Nanotechnology Center of Purdue University where we performed most of the fabrication work. We also want to thank University of Notre Dame for allowing us to use their nanofabrication lab for e-beam writing and development after writing.

3. FABRICATION AND CHARACTERIZATION OF MODE FILTER DEVICES FOR ON CHIP MODE DIVISION MULTIPLEXING

3.1 Introduction

Optical multiplexing technique is a process which combines a number of optical carrier signals onto a single optical fiber. This technique is very useful for photonic devices because it enables bidirectional communications and increase the capacity. Among various multiplexing techniques, Wavelength Division Multiplexing (WDM) is the most popular process, where multiple channels with different wavelengths are combined together [50]. However, on-chip WDM has been challenging due to the fact that the accurate wavelength control is difficult for the laser sources and the device footprint for the whole process is quite large.

Another multiplexing technique, where two orthogonal polarizations are used to represent two channels are called Polarization Division Multiplexing (PDM) [51]. The limitation of PDM is that the data capacity can only be increased twice compared to the single channel. Therefore, to allow more channels another multiplexing technique has been developed which is called Mode Division Multiplexing (MDM). MDM uses orthogonal eigenmodes of a multimode waveguide as different channels and thus allows more channels [5], [52] to be employed. Various functional devices for on-chip MDM have been developed over recent years, including sharp bending [53]–[55], waveguide crossing [56], (de)multiplexers [5], [57], [58], mode converters [59], mode switches [60] and mode filters [61], [62] etc.

In this chapter, we will discuss the fabrication and measurement results of a high order mode pass filter on SOI platform which strongly blocks TE_0 mode while allows TE_1 to pass with low insertion loss. TE_0 mode is filtered by radiation instead of reflection. Experimental demonstration shows 1.5 dB insertion loss for TE_1 with 15 dB rejection of TE_0 over C band. Cascaded filter with higher insertion loss and better extinction ratio is also demonstrated.

3.2 Fabrication

For the device fabrication, We started with a rectangular piece of SOI cleaved from a large SOI wafer. The size of the piece depends on how many chips we want to make, but typically we used 50 mm by 40 mm pieces. At first we cleaned the SOI piece to remove all particle and debris by using the traditional solvent cleaning (Using Toluene, Acetone, Methanol, IPA and DI water, then blow drying with Nitrogen gun). After that the piece was baked at 120 degree for 5 minutes to remove the excess solvent from the piece. Then we spin e-beam resist, soft bake at 120 degree Celsius for 3 minutes and write the structures using RAITH VB6 e-beam machine. After e-beam writing, we develop the sample on a solution of 25% TMAH solution for 70 seconds. After that, we dry etch the Silicon and then deposit Low Temperature Oxide (LTO) on top as upper cladding. Finally, we dice the sample into small pieces and the sample becomes ready for measurements.

3.3 Measurement set up

For measuring the devices, we used an optical measurement set up that contains a tunable laser (Agilent 81680A), a polarization controller, a sample stage where the sample was put and a sensor(HP 81632A). For coupling light into the chip, a set of lensed fiber was used which were clamped to the five axis stages on both ends and can be moved by the precision micrometer screws to obtain proper coupling. The polarization controller was used to optimize the polarization during the measurements. A schematic diagram of the set up is shown in Fig 3.1.

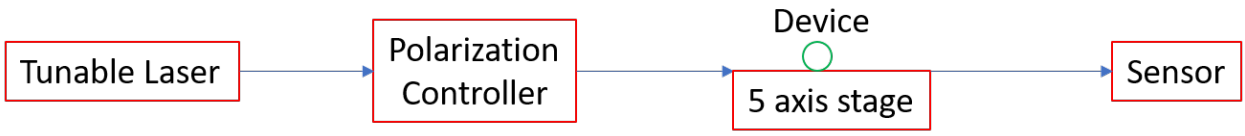


Figure 3.1. A sample set up for measuring Transmission Spectrum for the Mode filter devices. The coupling was done using two lensed fibers and they were very precisely controlled using the 5 axis stage.

For all the devices, we coupled the devices using the 5 axis stage and measured insertion losses after optimizing polarization using the polarization controller. Then we scanned the device using the tunable laser from 1520 nm to 1580 nm and recorded the sensor data.

3.4 Mode Filter Design using MMI

Mode Filters are very useful device for on-chip MDM, which helps to clean the channel. Filtering out the higher order mode is easy as they are weakly guided and can be filtered out by using adiabatic waveguide tapers. But filtering out the fundamental lower order mode is challenging as it is better guided and requires more efforts than just some tapers. A few designs are proposed to filter out the fundamental mode using photonic crystals [61] and polymer material platform [63]. But they had limitations regarding the high reflection and larger footprint along with the complex fabrication difficulties.

Here, we present a Multi Mode interference (MMI) based design of TE_0 filter, which allows TE_1 to pass. The schematic diagram of the TE_1 pass TE_0 filter is shown in Fig 3.2.

Fig 3.2a shows the design parameters of the filter. In this design, the input mode is split first using a Y junction, which splits TE_0 mode into an in-phase TE_0 pair and splits the TE_1 mode into an anti-phase TE_0 pair. Then these beams excite a MMI structure where TE_1 will refocus at the center and TE_0 is eliminated by those two outer ports equally. These designs were modeled by Dr. Min Teng and he also performed the simulations using Lumerical 3D FDTD software to verify the design. Fig 3.2b shows the resultant Electric field when a TE_0 mode is input, it splits into two in-phase TE_0 pairs and is guided out of the chip by the outer ports as predicted. Fig. 3.2 shows the effect when a TE_1 mode is the input, in which case it is split into two anti-phase TE_0 pair and after passing the MMI, they refocus at the center and guided out through the central output port. Thus this device can efficiently reject TE_0 while allowing TE_1 to pass. In this design, mode conversion between TE_0 and TE_1 is not possible because of horizontal symmetry, which is very important for MDM.

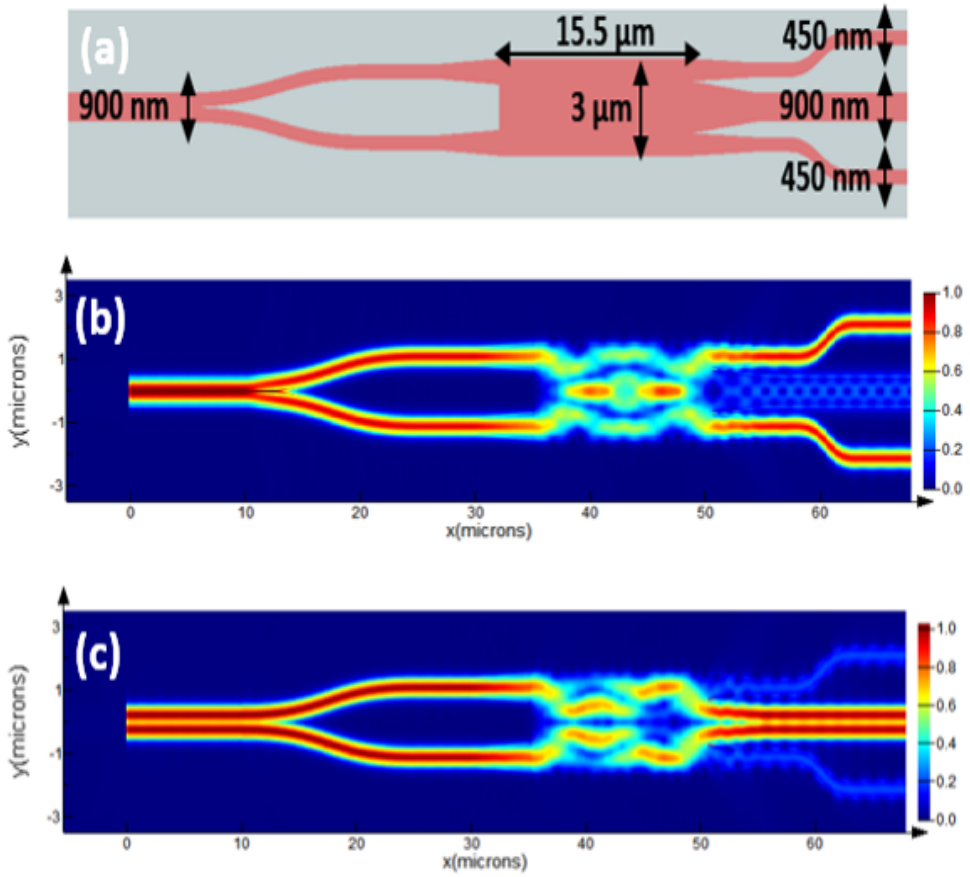
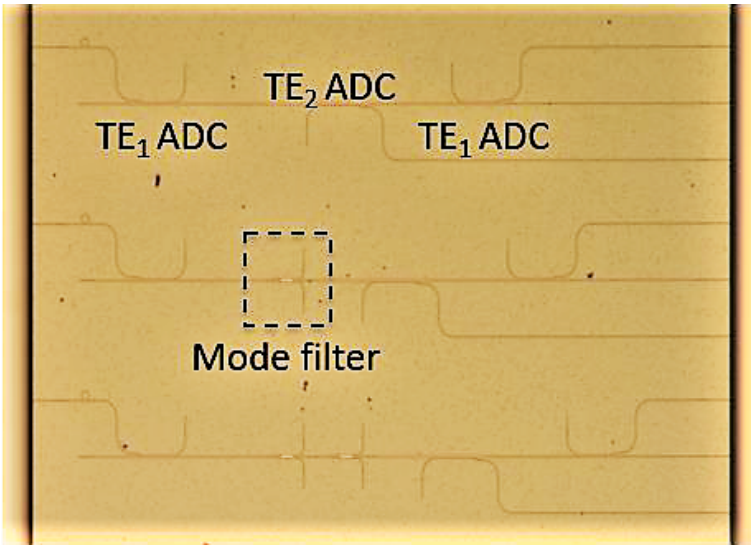


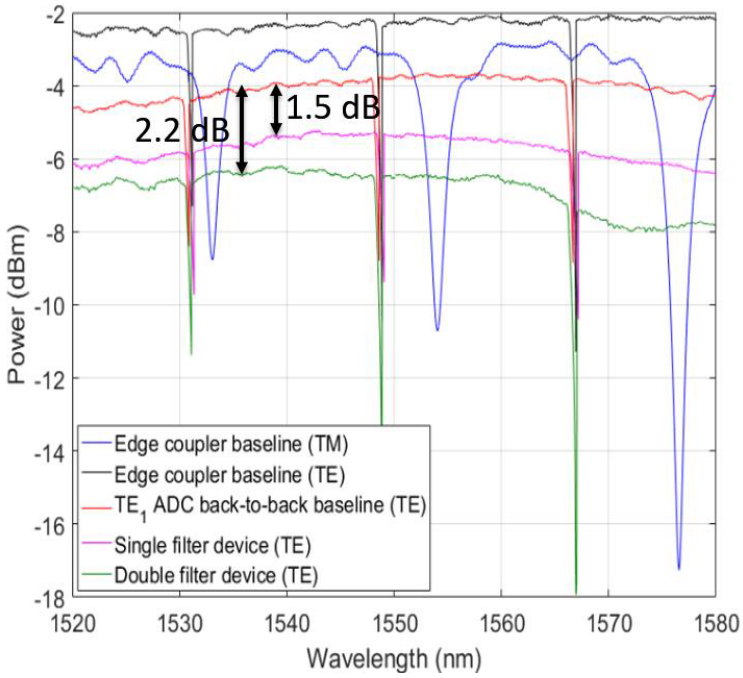
Figure 3.2. SOI TE_1 pass TE_0 filter a) Schematic diagram of the device b) FDTD simulation plot of Electric field with TE_0 input c) FDTD simulation plot of Electric field with TE_1 input. The simulation results were taken from Dr. Min Teng's PhD thesis with permission.

In order to measure the insertion loss for TE_1 mode, Asymmetric Directional Coupler (ADC) was used. To excite the TE_1 mode, one set of ADC is designed at the input and another set is designed at the output to demux different mode orders. The back to back ADC shows around 1 dB insertion loss at C band. Fig 3.3 shows different designs with ADC for loss characterization.

Fig 3.3 shows the measured power spectrum for mode filter devices with single and double filter set ups along with back to back ADCs. The baseline for ADC were measured by back to back ADC only without any filter devices. From the spectrum, we see around 1.5 dB



(a) Microscope image of the devices with ADC



(b) Measurement Spectrum

Figure 3.3. a) Microscope image of devices using ADC for loss measurement of ADC b) Measurement results of filter device with ADC for both single filter and double filter device with TE_1 input. Figure reproduced from Dr. Min Teng's thesis with permission.

insertion loss over C band and the best performance occurs around 1530nm. Also because of the broadband nature of the MMI, the filter devices are also broadband. Also with the double filter design we see around 2.2 dB insertion loss over C band.

Now, to analyze the performance of the mode filter we designed a cascaded MMI network as shown in Fig 3.4a. All the devices in the MMI network share the same input edge coupler, which makes measurements more reliable in expense of slightly noisier spectrum due to the MMI.

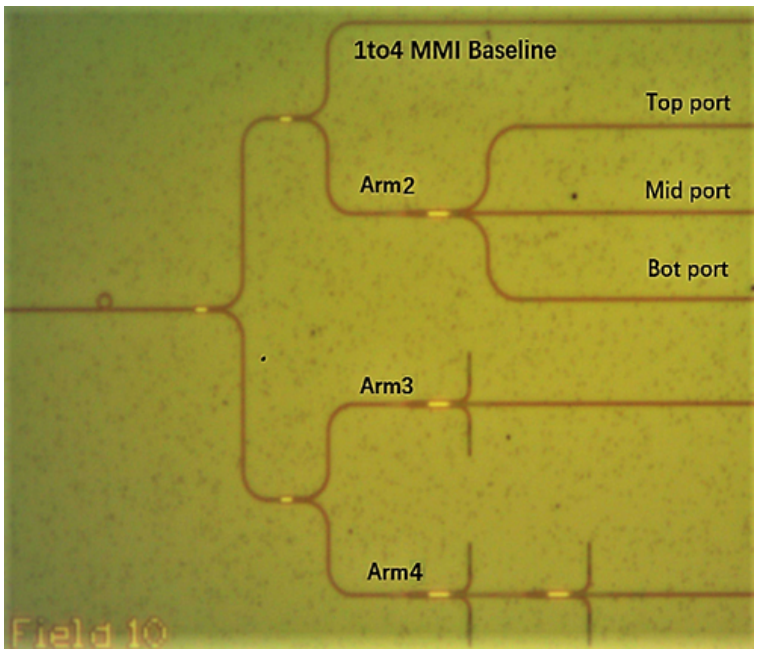
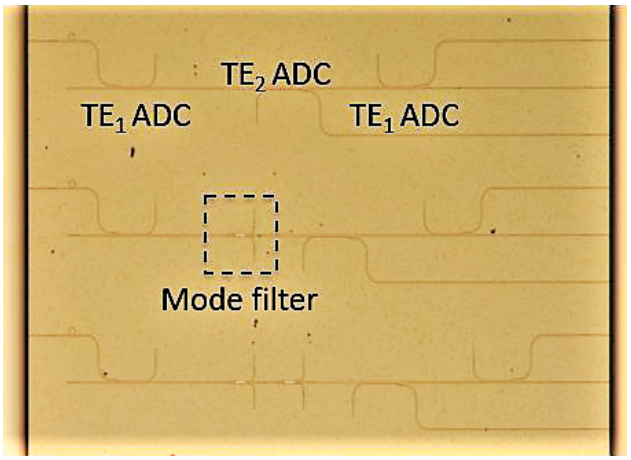
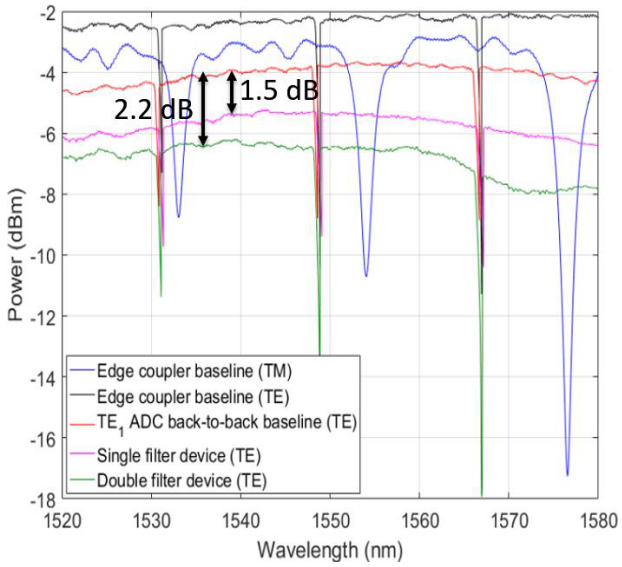


Figure 3.4. Microscopic image of the measurement scheme for a TE_0 rejection mode filter inside a cascaded MMI system. Top arm is the baseline for the MMI system. Arm 1 & Arm 2 have single & double filters respectively. Figure reproduced from Dr. Min Teng's PhD thesis with permission.

The measurement spectrum for the devices are shown in Fig 3.5a. The top arm (top red line) acts as the baseline for the MMI network. The top and the bottom port of arm 3 (purple and blue curve respectively) gives us transmission because they allow TE_0 mode. On the other hand, the middle port (green curve) shows a 15 dB rejection of TE_0 mode.



(a) Single filter with TE_0 input



(b) Single and double filter with TE_0

Figure 3.5. Measurement spectrum of a mode filter (TE_0 rejection) a) single filter b) single filter and double filter with TE_0 input. Figure is reproduced from Dr. Min Teng's PhD thesis with permission.

Figure 3.5b shows measurement results with both single and double filters. The double filter scheme gives us a rejection of 25 dB for the TE_0 mode. Table 3.1 shows the comparison between this work and others from literature.

Table 3.1. Performance Comparison between some mode filters from literature

Work	**Footprint**	**Measured Performance**
Bragg reflector based filter [61]	15 μm long on SOI platform	1.8 dB excess loss for TE_1 and 50 dB rejection for TE_0
Mode switch based filter [62]	11 mm long polymer platform	2.2 dB excess loss for TE_1 and 20 dB TE_0 rejection
MMI based filter (this work)	60μm long on SOI platform	$<$ 1.5 dB excess loss for TE_1 and 15 dB TE_0 rejection

Summary

In this chapter, the fabrication and experimental measurement of a SOI high order mode pass filter is demonstrated. The filter device shows $<$ 1.5 dB insertion loss over C band and $>$ 15 dB filtering of TE_0 mode. TE_0 power is rejected by radiation and the filter device is based on MMI suffers negligible reflection. The same principle should also work for TM polarization as well where alternative MMI dimension is needed. To our knowledge, this is the first practical experimental demonstration of high order mode pass filter on SOI platform. Such feasible filtering solution can be widely used for on-chip two-mode division multiplexing system to reduce the channel crosstalk.

Acknowledgement

We are thankful for Dr Min Teng, who designed and simulated those devices for this work. We are thankful to Yun Jo Lee and Dr. Yi Xuan for their help in fabrication. We are thankful to our sponsors for sponsoring this work, Birck Nanotechnology Center of Purdue University where we fabricated these chips and Ultrafast Optics and Fiber Communication lab of Purdue University where we characterized these devices.

4. FABRICATION OF SILICON NITRIDE MICRORING RESONATOR

4.1 Objective and Goal

In this chapter, we have discussed all the steps associated with a Silicon Nitride microring resonator fabrication. We started with an initial process that we inherited, thanks to our previous group members and collaborators. But we found that the devices fabricated with that process have some issues that needed to be addressed. We did a comparative analysis with other research groups that also fabricate Silicon Nitride microring resonators and made some changes to our process according to our findings. We also investigated our whole fabrication process step by step and found some issues that could be responsible for our low quality factors. We suggested some improvements and added steps to our whole fabrication process to improve the quality and yield of our fabrication. We made actual devices using the modified fabrication process with all the added steps and the initial characterization results show improvement in our quality factors, thermal performance and yield. All the steps and results are explained in detail in the following sections and subsections.

4.2 Fabrication of Silicon Nitride microring resonator

4.2.1 Introduction

Fabrication is a continuously evolving process and it is always improving with time. There are many steps associated with the fabrication process of Silicon Nitride microresonators. Some of the major steps are: Photolithography, Etching, Annealing, E-beam writing, Film Deposition, Metal deposition etc. Some of those steps are briefly described in appendix. In this section, we are going to discuss the efforts we put in to improve the fabrication of our Silicon Nitride microring resonators. To improve the fabrication process, we add additional steps or modify some steps of the fabrication process. The improvement of fabrication process is measured by a few parameters like Quality factor (Q-factor), Loss, thermal performance etc. There are two types of quality factors that is usually reported: one is called the intrinsic quality (Intrinsic Q) factor, which is directly related with the intrinsic loss

inside the microring resonators, such as absorption loss, bending loss, scattering loss due to top surface or sidewall roughness and existence of particle or contamination etc. The other quality factor is called the loaded quality (Loaded Q) factor, which accumulates the coupling loss along with the intrinsic loss. The higher the quality factor is, the lower is the power requirement to initiate a frequency comb [64]. Therefore, high quality factor chips are more suitable for on-chip optical frequency comb generation and many other applications.

Different type of losses in Silicon Nitride microring resonators are shown in Fig 4.1.

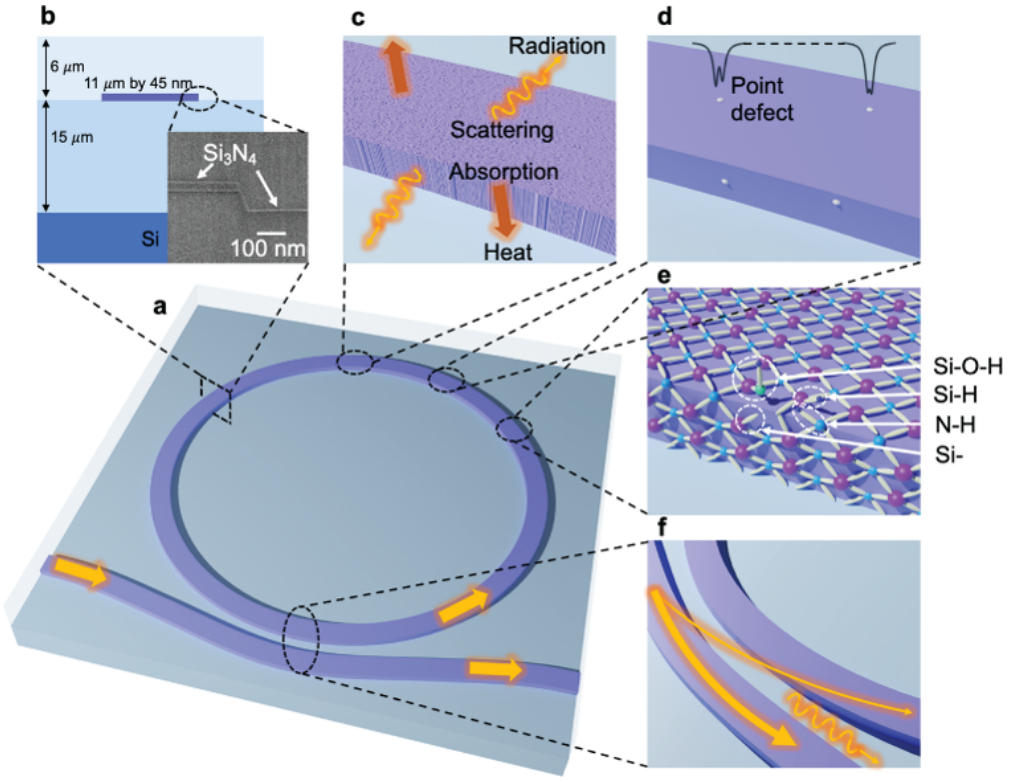
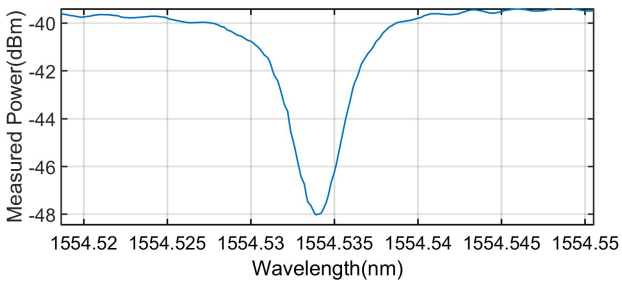
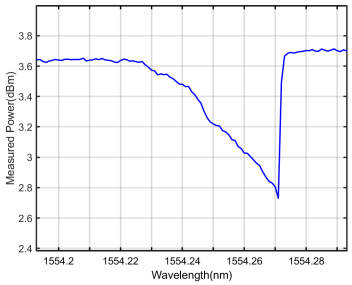


Figure 4.1. Different kind of losses in Silicon Nitride microring resonators and their origins. The picture is taken from [65]

The losses in microring resonator can be minimized by both design and fabrication improvements. For example, bending loss inside the microring resonator due to sharp bends can be minimized by designing the bend with more number of points for better definition of the curved area. Similarly, the optimization of e-beam writing during the writing can help us to reduce the bending loss. In the end, there will always be some loss, however small that is,



(a) Symmetric resonance at low power



(b) Skewed resonance at high power

Figure 4.2. Resonance skewing due to thermal self locking between the laser and the resonance.

but optimizing the design and fabrication step it is possible to minimize that loss. Similarly, the presence of particle and contamination can be a major source of scattering loss which can be reduced by careful and clean fabrication process. Also, the etching process can contribute to sidewall roughness and hence scattering loss [66]. The annealing can help us to reduce absorption loss by breaking those N-H bonds that causes absorption loss in telecommunication wavelength [67]. All these losses can be reduced by properly optimizing the fabrication steps.

Finally, the thermal performance of the devices can affect soliton generation as resonances starts to get skewed as we start injecting more power into them due to thermal self locking between the laser and the resonance [68]. An example of thermal skewing is shown in Fig 4.2. If the thermal skewing is large, it may cause difficulty in locking into the soliton step and the stability of soliton is affected. By properly optimizing the annealing, it is possible to reduce the thermal skewing and hence reduce the thermal broadening.

4.2.2 Old Fabrication steps

The fabrication of Silicon Nitride microring resonator consists of many steps and processes. Usually we start with a bare prime Silicon wafer and then start growing and patterning everything on top of it. The basic fabrication process was developed by the previous group members in our group and it was an effort that took years to develop. With time, the process steps were modified and changed according to our needs and also because of

new development in fabrication side. The basic fabrication process that we inherited can be shown in Fig. 4.3.

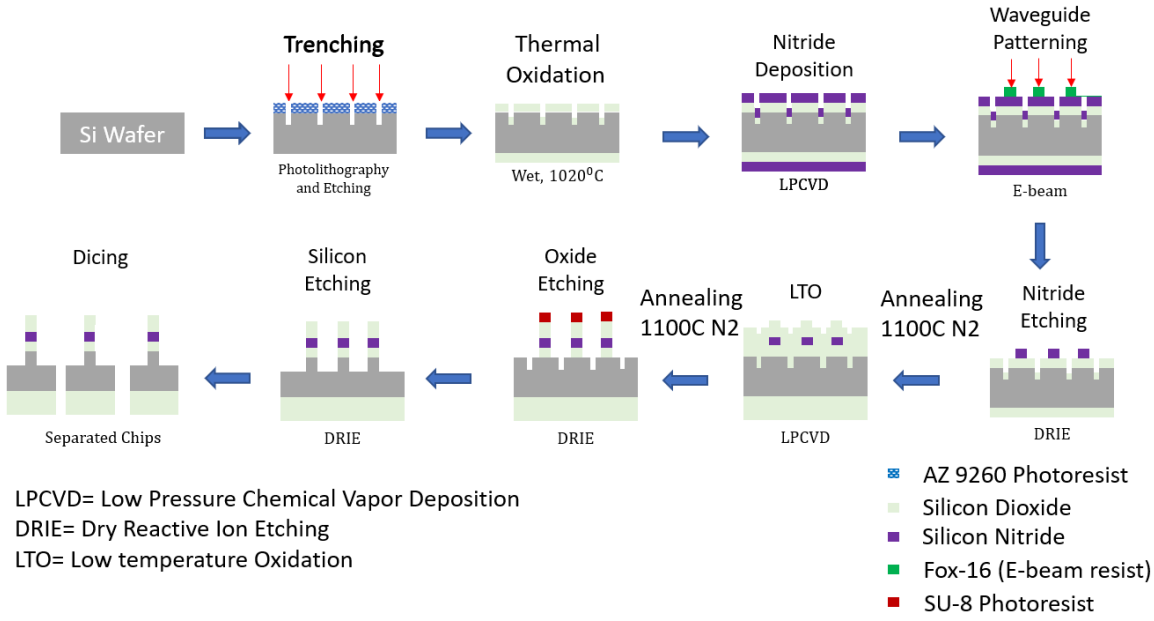


Figure 4.3. Process steps during the fabrication of Silicon Nitride microring resonators.

The process starts from a bare Silicon wafer and we start growing films on it, do necessary pattering, cleaning and annealing processes before separating the chips. The basic processes are described in Appendix. We were one of the first groups to report high quality factors in Silicon Nitride microresonators [64]. But unfortunately after that we were not able to reproduce them despite our best efforts. Also, recently we noticed that our devices do not have very good thermal performance compared to other research groups working with similar devices. Our devices showed large thermal broadening and skewing at high power which affected our soliton generation process.

4.2.3 DARPA A-Phi Project and its unique challenges

Recently, we started a new DARPA project in collaboration with Sandia National Lab. The goal of the project is to develop a fully integrated atomic-optical clock. Sandia National Lab will integrate a Ytterbium (Yb) ion trap including all the optical assembly required

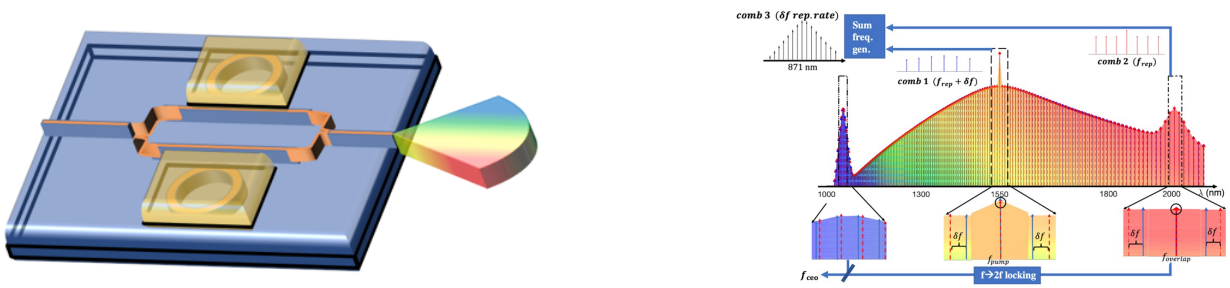


Figure 4.4. Vernier Dual comb scheme for the DARPA A-Phi project. Image courtesy: Dr. Mohammed Al Alshaykh.

for trapping and probing. OE waves will develop a 'clock' laser at 871 nm, which is based on a low-linewidth and self-injection locking technique with a whispering gallery mode resonator. For frequency-doubling, thin film Lithium Niobate (LN) waveguides will be used, which was developed by Prof. Hong Tang's group at Yale University. Our focus at Purdue is the development of an integrated Optical Frequency Comb system (based on Silicon Nitride), which is capable of coherently dividing the clock laser within the requirements of the program. In order to do that, we chose the vernier dual comb approach [69], where we need to have two microring resonators which have a slightly different FSR (20 GHz difference) and they are pumped by a single laser. If we can line up the resonances together and beat those combs together, we will get 20 GHz beat notes in the first sidebands as shown in Fig 4.4.

But this was a very challenging work from both the design and fabrication perspective for many reasons. From design perspective, we had to design in such a way that it can produce a coherent frequency comb that will be very close to the optical clock source. A lot of dispersion engineering is needed for getting broadband octave spanning frequency comb [70] with dispersive waves. From fabrication perspective, making good quality devices with very small devices (radius $\sim$ 25 μm) with narrow width (width $\sim$ 1.5 μm) is quite challenging. Also, as we started making devices, we have noticed that the dispersive waves are highly sensitive to the film thickness too. We need to hit the right thickness in order to get the dispersive waves close to the targeted region. But since our Silicon Nitride deposition process

is a stochiometric process, controlling the film desposition rate or hitting the right thickness was very challenging. From design perspective, we can tweak our designs to some extent to compensate the variation, but that was not enough to cover the thickness variation during the film deposition. The fabrication sensitivity was analyzed by our group member Cong Wang and she came up with some numbers as shown in Table 4.1.

Table 4.1. Thickness Sensitivity of the Dispersive waves

Cross section	**First Dispersive wave shift**	**Second Dispersive wave shift**	**Pump Resonance shift**	**Repetition Rate shift**	**Offset Frequency shift**
1.5 μm x 750 nm	-2.7 THz / 5 nm	+3.7 THz / 5 nm	-100 GHz / 5 nm	-60 MHz / 5 nm	85 GHz / 5 nm

From simulations, we also see that dispersive wave locations are sensitive to the thickness of the film. Thanks to Cong Wang, we found a few other things that affects the location of dispersive waves. She will discuss them in detail in her thesis. Here, in Fig 4.5 we are showing only the height sensitivity:

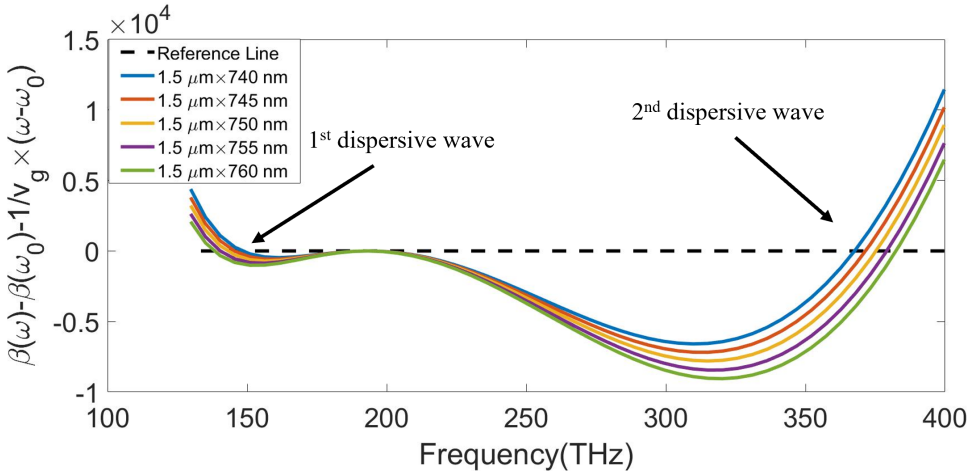
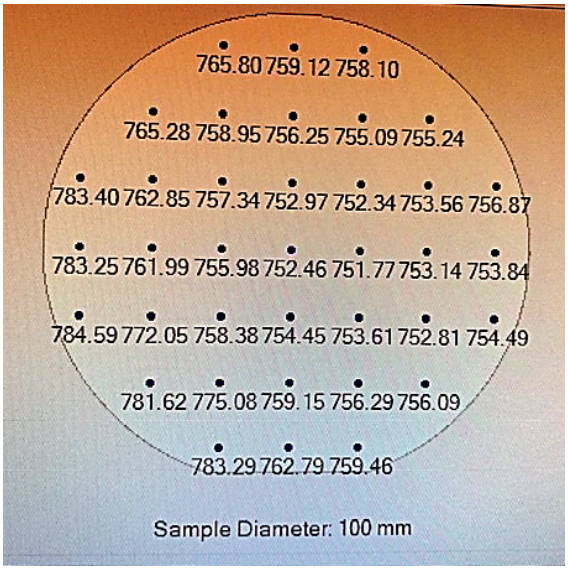
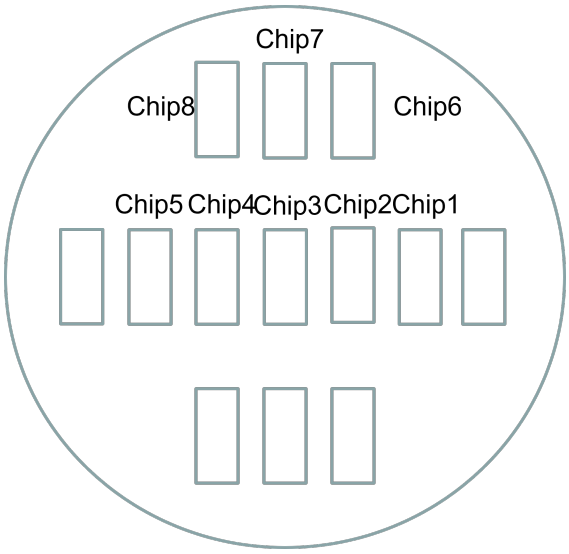


Figure 4.5. Film thickness sensitivity for dispersive wave locations. Thanks to Cong Wang for the simulation.



(a) Thickness map

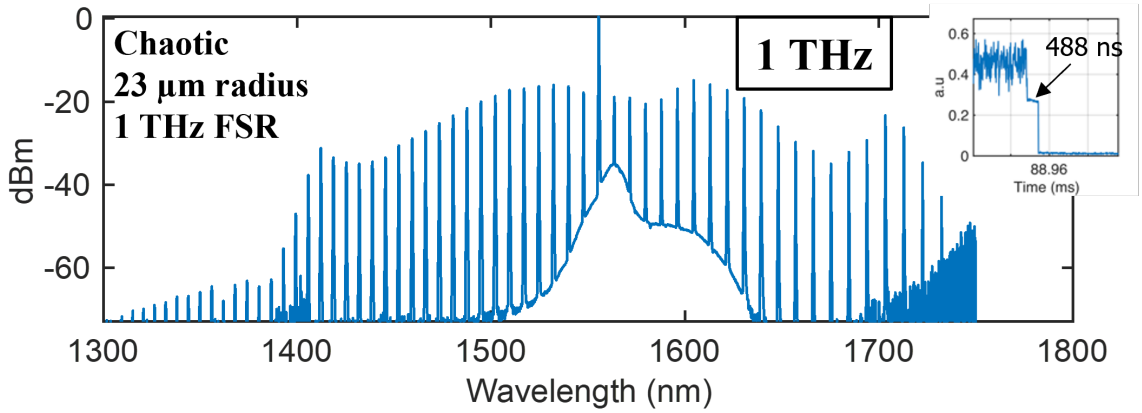


(b) Chip locations in actual wafer

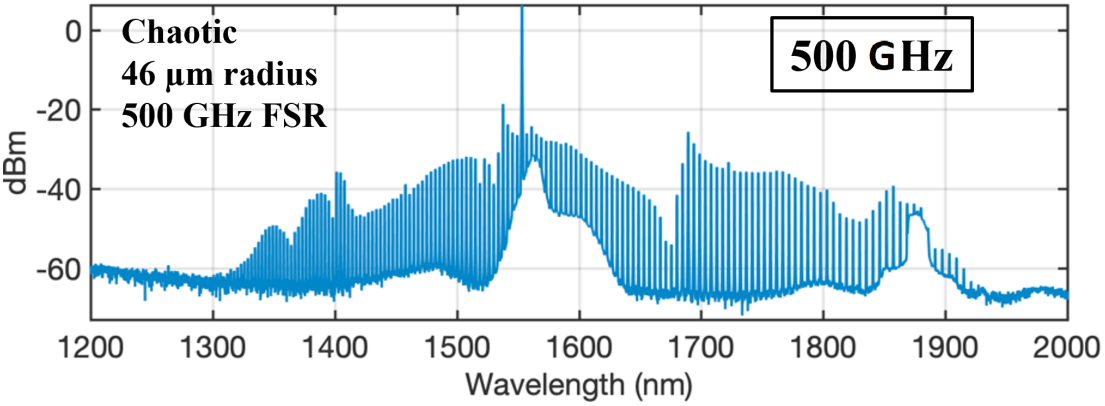
Figure 4.6. Thickness mapping for Silicon Nitride films. a) Thickness measured by Filmetrics F40 tool at different points of the wafer b) Sample chip locations in the wafer, each chip's thickness can be read from the thickness map and change the design accordingly to compensate the variation.

In order to solve that problem, we came up with the idea of thickness mapping. We used a thickness measurement tool named Filmetrics, which works similarly to ellipsometer, to measure the thickness of the Silicon Nitride film. This tool has a 10 μm aperture and a light source, and sends light to the film and reads the reflection. Finally it fits the reflected data with its database and estimate the film thickness. The measured thickness is very close to the actual values. With proper optimization we can get values close to 95 % accuracy. An example of thickness mapping is shown in Fig 4.6.

When we make designs for each chip, we read the thickness from thickness map and vary our designs around that thickness to compensate the thickness variation. For example, chip 8 in Fig 4.6b will be designed around 759 nm thickness. Similarly, Chip 3 will be designed around 752 nm thickness. Thus, we were able to overcome the thickness variation problem.



(a) Comb generation from 1 THz device



(b) Comb generation from 500 GHz device

Figure 4.7. Examples of Optical Frequency comb generation from our first few efforts in the DARPA project.

In our first few fabrications, we optimized our designs and were able to get frequency combs from two different designs that we tried. One was 1 THz design and another was 500 GHz design. But they were not octave spanning combs as shown in Fig 4.7. Those were chaotic state frequency combs and not coherent. Also, the frequency combs were not octave spanning and not broad enough for fulfilling our project goals.

Later, we were able to modify our designs, compensate the height variations and we got our first octave spanning comb as shown in Fig 4.8. But it was also in chaotic state and not coherent. Most importantly, it needed around 950 mW input fiber power in order to generate that comb, which was higher than the power budget in this project. So we needed to improve our quality factor to reduce that power and satisfy the power budget. But our devices had only a few million (1-2) quality factors, which despite our best effort, we could not improve previously. That drove us to investigate our process thoroughly and find issues which were causing the low quality factor of our devices.

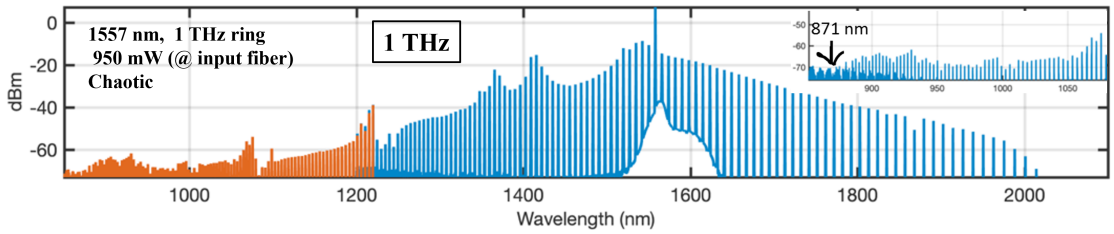


Figure 4.8. Our first octave spanning chaotic comb from 1 THz design. The required power to get the octave spanning comb was about 950 mW. Two different OSAs were used to get this data. The Orange lines are the data from standard (visible/near-IR) OSA and the blue lines are the data from long-wavelength OSA.

To investigate, we have really dug into our process and tried to check every step in our fabrication. In the next couple of sections, we will show a few investigation results that might be responsible for our low yield and low quality factors and we will suggest possible ways to improve our fabrication process. We will start with a comparative analysis with other research groups that fabricate Silicon Nitride microring resonators. We compared our process with theirs and tried to modify our fabrication process in order to improve our quality factors. We also did a step by step SEM investigation of our devices at different steps of the fabrication process and tried to find out defects or problems that could cause low quality factors for our devices. All of these issues are discussed in the following section

4.3 Comparative analysis

We started with a comparative analysis among several groups that fabricates Silicon Nitride microring resonators and tried to see what are the things that may be responsible for our degraded quality factors. It is true that every group has their own unique style of fabrication and some may be completely different due to the equipment availability. Still we wanted to see if there are any major things that we might be missing in our fabrication. The comparative analysis results can be summarized in table 4.2.

Table 4.2. Comparison between the fabrication process of different research groups that fabricates Silicon Nitride microring resonator

Begin of Table				
Purdue (Qi group)	**EPFL (Kippenberg group)**	**Chalmers (Company group)**	**Columbia (Lipson group)**	**Purdue (2014 fab)**
Use subtractive process	Use photonic damascene process	Use subtractive process	Use subtractive process	Use subtractive process
Use E-beam machine to define waveguide structure	Use DUV stepper lithography to define waveguide structure	Use E-beam machine to define waveguide structure	Use E-beam machine to define waveguide structure	Use E-beam machine to define waveguide structure
Use HSQ as e-beam resist	Use Ma-N as E-beam resist	Use Ma-N as E-beam resist	Use Ma-N as E-beam resist	Use HSQ as E-beam resist

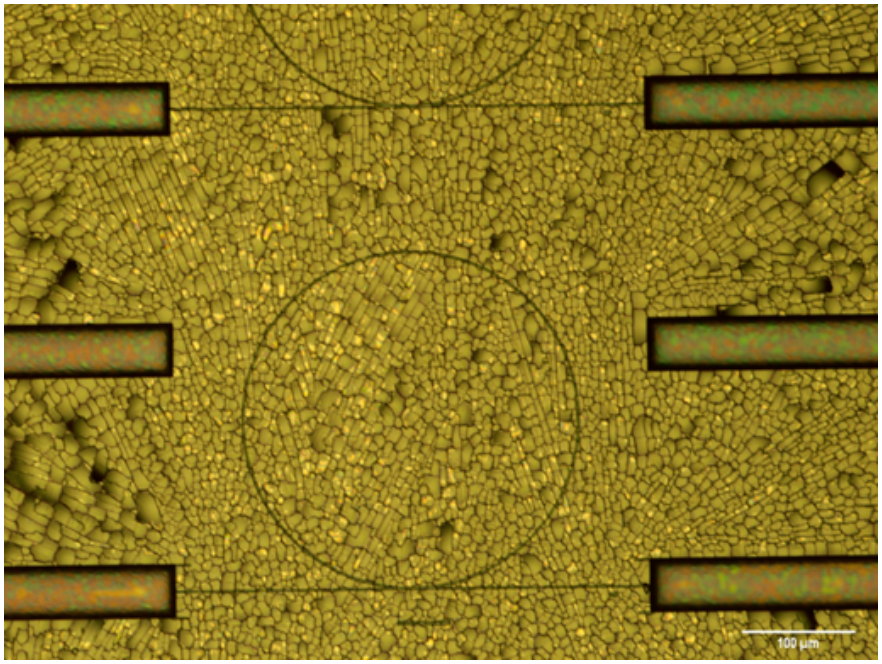
Continuation of Table 4.2				
Purdue (Qi group)	**EPFL (Kippenberg group)**	**Chalmers (Victor group)**	**Columbia (Lipson group)**	**Purdue (2014 fab)**
Do not use any hard masks during etching patterns	Use a-Si hard mask during etching patterns	Do not use any hard masks during etching patterns	Use SiO_2 hard mask during etching patters	Do not use any hard masks during etching patterns
Annealing is done at 1100°C	Annealing is done at 1200°C and 1250°C	Annealing is done at 1200°C	Annealing is done at 1200°C	Annealing is done at 1200°C
Upper cladding all LTO	Upper cladding TEOS first (500nm) and then LTO	Upper cladding TEOS first (500nm) and then PECVD	Upper cladding TEOS first (500nm) and then PECVD	Upper cladding all LTO
No CMP is used	CMP is used for planarization	No CMP is used	CMP is used for planarization	No CMP is used
Loaded Q 1-2 millions (1.5 μm wide), Intrinsic Q 2-3 millions	intrinsic Q> 23 millions, 30 millions (2021) [71]	Intrinsic Q 12.5 millions, 11.4 millions (2019) [72]	Intrinsic Q 37 millions (width 2.5 μm) (2017) [73]	intrinsic Q 17M (width 3 μm) (2016) [64]
End of Table				

There are different ways of fabricating Silicon Nitride microresonators and each group came up with their own way of fabricating the devices with their equipment and resource availability. But if we look at the table carefully, we see that there are two major steps that our fabrication process lacked compared to other groups: First, annealing step and second, upper cladding deposition step. The annealing is a very important process of the fabrication as this step ensures uniform and high Quality factor chips. Our annealing process with limited by our tool availability. In our fabrication facility we were only allowed to get up to 1100°C temperature whereas all other groups were annealing at 1200°C or above.

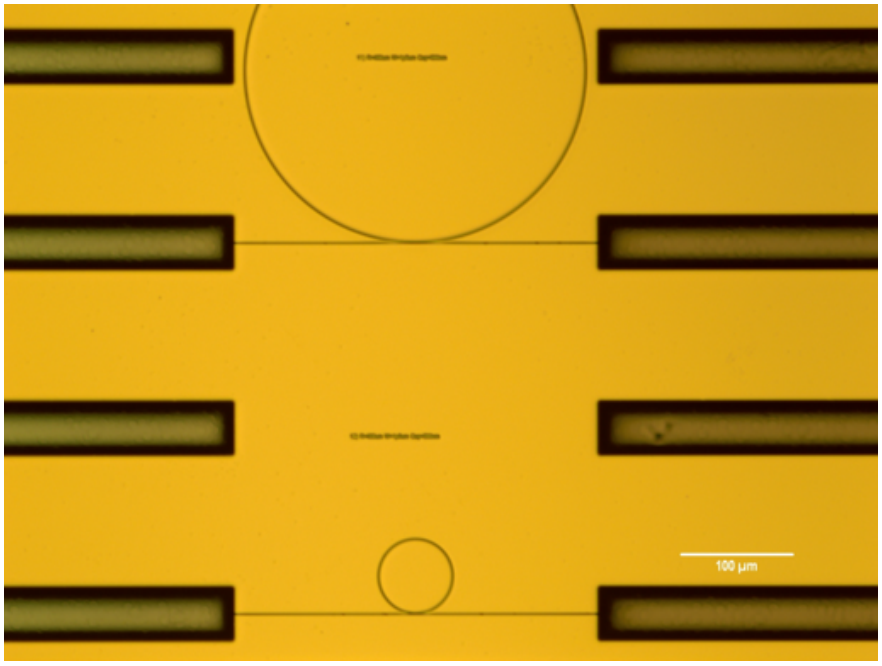
4.3.1 Efforts on improving the annealing process

Our first effort was to try to anneal our samples at higher temperature. First, we tried to work with a completed chip that has upper cladding on it (LTO). We collaborated with Professor Tang's group from Yale university as they have annealing tubes that can go 1200°C. We sent some samples there. They annealed those samples and returned them to Purdue. But unfortunately, the results were not satisfactory. There were couple of problems: First, since we have deposited a thick upper cladding (∼3 μm), heating it up couldn't drive away hydrogen across that thick oxide cladding. As a consequence, we didn't see any change in our device performance. Additionally, at 1200°C our upper cladding completely cracked and made our devices not useful. At 1150°C our upper cladding didn't crack. But there was no change in the quality factor of the devices. The microscopic picture of our samples annealed at 1200°C and 1150°C are shown in Fig. 4.9.

Another difference that we observed is that we used to deposit our entire film in a single step Silicon Nitride deposition. But since our films are quite thick (∼800 nm), it is very hard to drive out the hydrogen from the bottom part of the film. So we tried depositing our films in 2 steps and add an annealing and RCA cleaning step in between. Also, thanks to the research staffs at Birck Nanotechnology center, we were able to anneal our samples at slightly higher temperature at 1150°C.



(a) Annealed at 1200°C



(b) Annealed at 1150°C

Figure 4.9. Microscopic images of annealed samples at Yale university. The samples had $\sim$3 μm upper cladding on top. a) Sample annealed at 1200°C. The upper cladding completely cracked. b) Sample annealed at 1150°C. The upper cladding did not crack, but the device performance did not improve.

The main reason for us to add those annealing steps were twofold. Firstly, annealing breaks N-H bonds which can cause an additional absorption loss at telecommunication wavelength [67]. Appropriate annealing can make the quality factors more uniform and can potentially increase by reducing absorption loss. Secondly, thermal performance of the chip can be improved by optimizing the annealing process. Thermal performance of the chip is important for many applications. For example, thermally controlling resonance locations by microheaters [39], temporal soliton generation (soliton step length, hence the stability of soliton state) [40] etc. In our case, both were important factors for us. Our quality factor has recently been around 1-2 millions mostly and we needed to improve it to open up many possibilities, especially the on-chip applications. Similarly, our devices were showing large thermal broadening and hence anything at high power (e.g. Soliton generation) was having issues. Therefore, we made some changes to our fabrication to accommodate more annealing steps.

Improving cleaning steps: RCA cleaning

Beside annealing, we also added a number of RCA cleaning at different stages of our fabrication process. RCA cleaning was first developed by Werner Kern in 1965 while working for Radio Corporation of America (RCA), hence the name RCA cleaning [74]. It is a very popular cleaning process and widely followed in industries. RCA cleaning usually involves 3 steps:

- Step 1: (SC-1) Removal of Organic contaminants: This step not only removes any organic residue (e.g. photoresist residue), but also removes particle contamination. In this step, ammonia water ($29\%NH_4OH$), aqueous Hydrogen peroxide ($30\%H_2O_2$)and DI water is mixed at 1:1:5 ratio and the solution is heated up to 80°C. The wafers are dipped into the solution at that temperature for about 10 minutes. Then the wafers are rinsed well with DI water before doing anything further.

- Step 2: (SC-2) Removal of Metallic contaminants: This step not only removes any metallic contamination, but also any contamination from SC-1. In this step, Hydrochloric acid (HCl), aqueous Hydrogen peroxide ($30\%H_2O_2$)and DI water is mixed

at 1:1:6 ratio and the solution is heated up to 80°C. The wafers are dipped into the solution at that temperature for about 10 minutes. Then the wafers are rinsed well with DI water before doing anything further.

- Step 3: (SC-3) HF dip or Oxide strip: This is an optional step in RCA cleaning and it removes any native oxide formation on Silicon wafers during step 1 or any other process. This step is important before the film deposition. But if there is Silicon Dioxide film present on wafer, this step should not be used. In this step, 49%HF and DI water is mixed at 1:50 or 1:100 ratio and then the wafers are dipped for about 10-15 seconds. Then they are rinsed well with water.

When we work with Silicon or Silicon Nitride films, we perform all three steps. But when the film on top of our wafer is Silcon dioxide we only perform step 1 and 2. During the two step Silicon Nitride deposition, RCA cleaning has a very important contribution. It not only cleans the surface, but also removes the thin silicon Dioxide formed at the interface of those two steps [66].

Beside doing all these changes, we also improved the photolithography processes. We moved all of our masked photolithography processes to maskless ones including the trenching photolithography, edge definition photolithography as shown in Fig 4.3. Maskless lithography works on projection, hence we do not need physical mask. That saves a lot of time and money during our fabrication process. We also improved the fabrication by adding more alignment marks for alignment purposes, optimizing the settings and writings on the e-beam machine, exploring the upper cladding deposition schemes etc. Incorporating all the changes we developed this current fabrication scheme (Fig. 4.10), which we are currently using for all of our Silicon Nitride Fabrications:

4.4 Debugging Fabrication: Finding process defects

Beside modifying our previous fabrication process, we also dug through all the steps in our fabrication process in search for finding fabrication defects. We did step by step SEM investigation of our process and tried to find reasons for our low quality factors and low

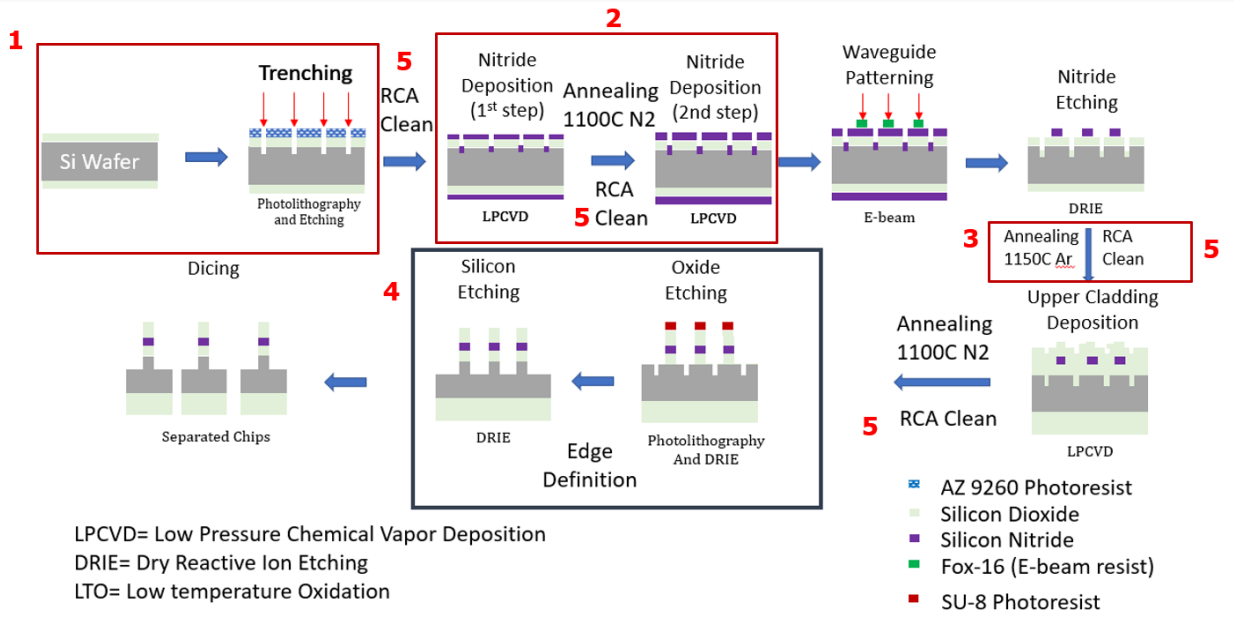
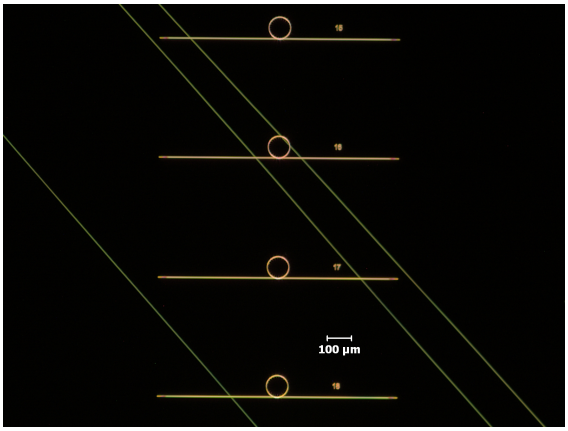


Figure 4.10. Modified process steps for the fabrication of Silicon Nitride microring resonators. 1. Modified trenching process 2. Multi step Silicon Nitride film deposition with added annealing and RCA cleaning step 3. Modified annealing step after Nitride etching and HSQ (E-beam resist) removal 4. Maskless lithography process for edge definition 5. All the RCA cleanings to reduce contamination and particles.

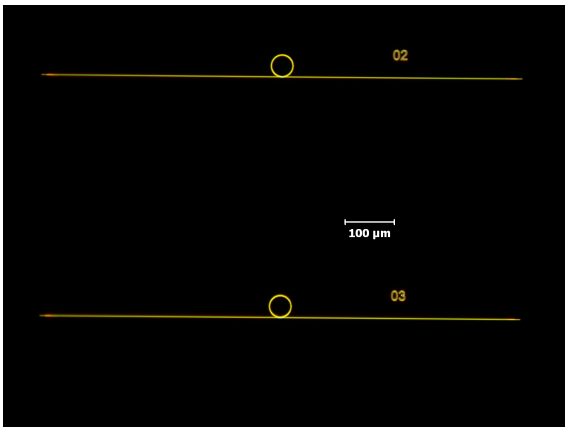
yield. We found several reasons which could be responsible for that and those are discussed in the following subsections.

4.4.1 Importance of trenches

We had been using trenched Silicon wafers previously and the trenching process was an important step in our fabrication. Trenching helps us to stop the cracking of thick Silicon Nitride films. This trenching process was done on bare Silicon wafer. But in recent times, we had been using some foundry wafers which had thick thermal oxide (bottom cladding $\sim$3.5μm) grown on it. For some wafers, we also had some Silicon Nitride film (300nm or 400nm) grown on it. So we had no way to make trenches on them. we tried to deposit rest of the Silicon Nitride on top and fabricate chips using those wafers. It has caused us several issues: Firstly, due to the absence of trenches, our Nitride films had cracks and those



(a) Devices with film cracks

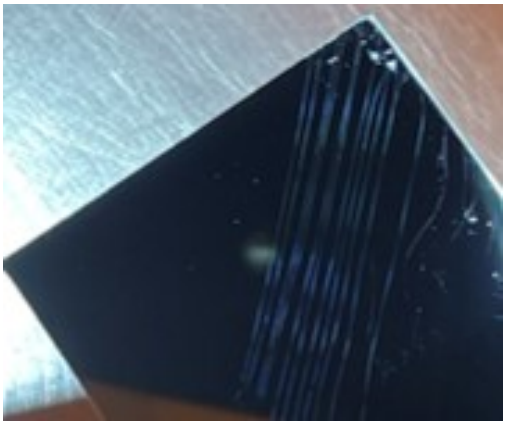


(b) Devices without film cracks

Figure 4.11. Dark field microscopic picture of the wafer after e-beam writing a) all the devices went under the film cracks, so none of them would be good b) Some good devices that didn't fall under the film cracks. This reduced our fabrication yield by a huge amount.

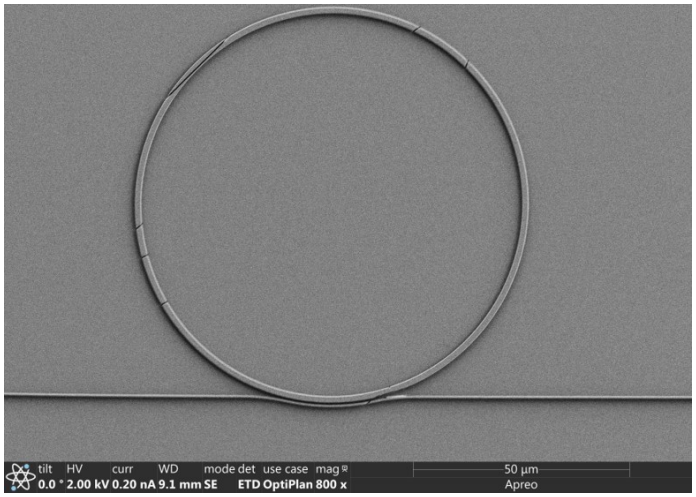
cracks were random and unpredictable. That thing alone drastically reduced our yield as any device that went through the crack are basically useless. Some example of film cracking due to the absence of trenches are shown in Fig. 4.11.

Beside the cracking of Silicon Nitride films, we found that the trenches have another very important contribution and that is stopping or reducing the crack in our e-beam resist. We use HSQ (FOx-16) as our e-beam resist and during the Nitride etching step, it acts as



(a) HSQ crack on a piece sample

(b) HSQ crack on a wafer



(c) SEM image of a device that had cracks in HSQ film

Figure 4.12. HSQ cracks a) Cracks on a piece sample b) Cracks on a wafer c) SEM images of the device fabricated that had HSQ cracks.

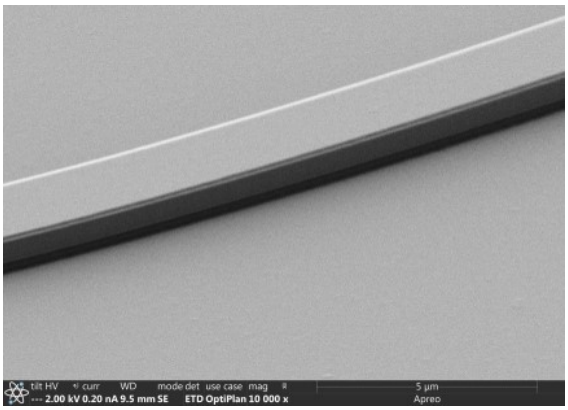
a mask. But the selectivity during the etching is low, around 1: 1.25 or less with Silicon Nitride, which means we etch about 1.25 nm of Silicon Nitride while 1 nm etch mask is gone. Therefore, our e-beam resist needs to be quite thick ($\sim$1μm) to make sure we can etch properly without any problem. When we spin such a thick layer of HSQ and bake it before e-beam writing, it causes some film shrinkage and that can crack the HSQ film as shown in Fig 4.12 (a).

Additionally, we use tweezers to handle our wafers and the points where we hold the wafers are prone to cracks in the films. Any crack formation on the film usually propagates all over to relieve the stress. Also, since we do an annealing step in our nitride deposition step, that also puts additional stress of wafer and make our wafers bend (wafer bowing) which can lead to film cracks on top. Now if there is a crack in HSQ film, during the etching the reactant can go in and etch the Silicon Nitride through that crack and that device would be ruined. This has happened to many of our devices without trenches. An example of HSQ crack and the SEM image of the fabricated device is shown in Fig. 4.12(c).

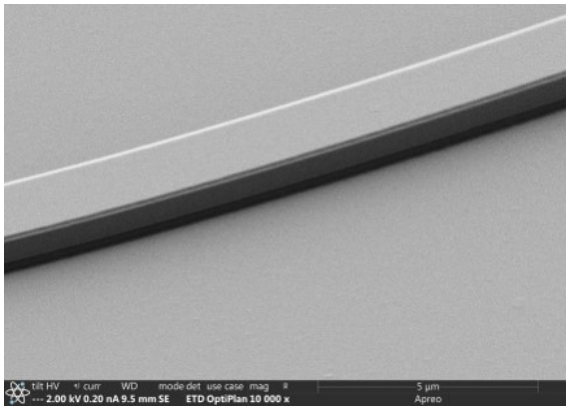
In our old fabrication flow, we used to make trenches first before sending wafers to the foundry for bottom cladding deposition using thermal oxidation. But in our recent fabrication runs, we ordered wafers from foundry with oxide film deposited on it. Therefore, we did not do any trenching process which affected our yield to a great extent. In order to improve the yield, we reintroduced the trenches. But the challenge was the bottom cladding on Silicon wafer. Thanks to the discussion with our collaborator from Chalmers University of Technology of Sweden (Professor Victor Torres Company's group), we were able to develop a process by which we could make trenches on a Silicon wafer with oxide films. We basically do the same lithography and process, just add 2 additional steps: First, the oxide etching using BOE (Buffered Oxide Etch) solution and second the RCA cleaning after finishing the trenching process. This helped us to improve our yield a lot since now we started to have wafers with very little or no cracks.

4.4.2 HSQ aging and dosage change

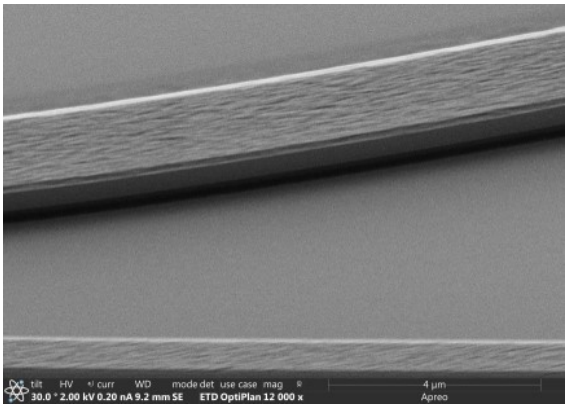
We also found that due to the aging our e-beam resist, the e-beam dosage need to be readjusted. Since it is a negative e-beam resist, it starts to link up more as it ages, so it needs less amount of dose to fabricate those structure. Traditionally, we use 2200 $\mu C/cm^2$ or 2400 $\mu C/cm^2$ dose to pattern our wafers. But after doing a dose test with an aged e-beam resist, we found that the dose has changed and we need to do a dose test every time we fabricate devices. At that time when we did the dose test, we found that any dose in between 1600



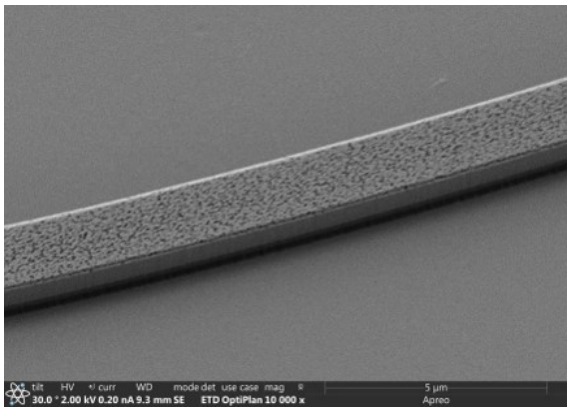
(a) Dose=1600μC/cm^2



(b) Dose=1800 μC/cm^2



(c) Dose=2200μC/cm^2



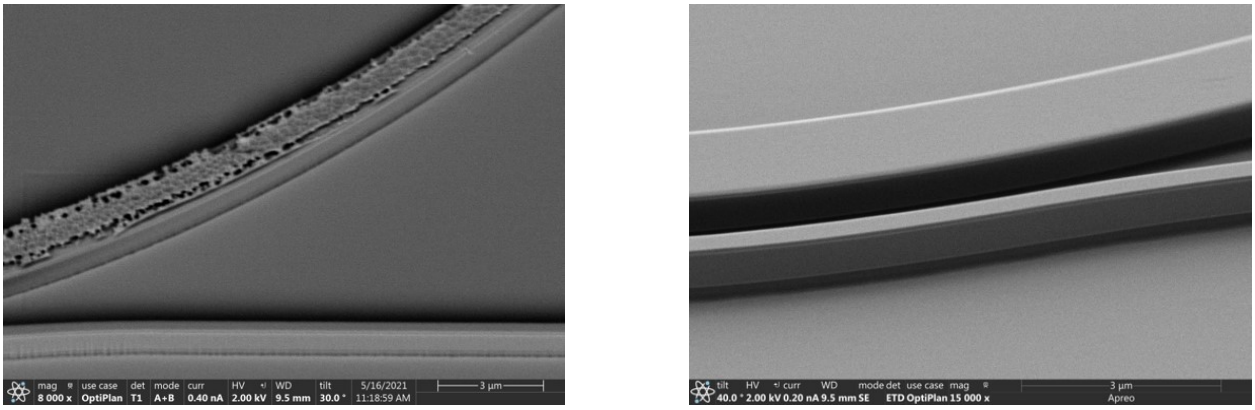
(d) Dose=2600μC/cm^2

Figure 4.13. SEM images of devices with different e-beam doses.

μC/cm^2 to 1800 μC/cm^2 works best for our devices. The SEM images of the patterned structures with different doses are shown in Fig. 4.13.

4.4.3 Removal of e-beam resist

We use HSQ (Fox-16) as our e-beam resist and usually dip into BOE solution for 8-10 seconds after nitride etching to remove the rest of the e-beam resist from our pattered devices. This step is very important and of high significance as after removing the HSQ we do high temperature annealing and upper cladding deposition. Any residue that is not removed will



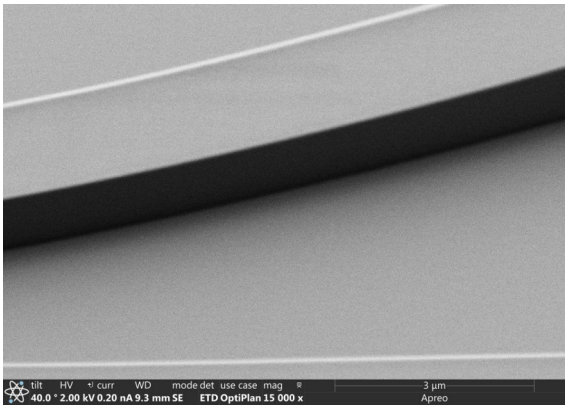
(a) Devices with HSQ residues

(b) Devices without HSQ residues

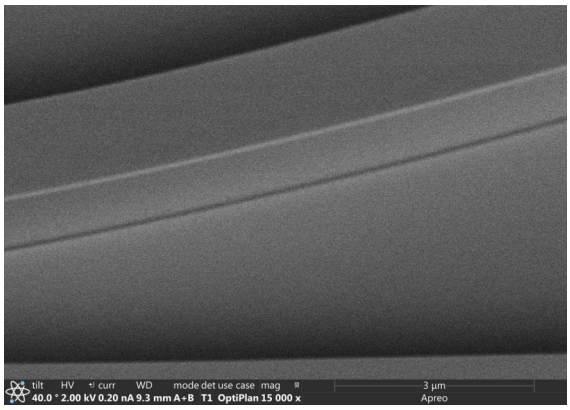
Figure 4.14. SEM images of a device that has a) HSQ residues on top of the waveguide after BOE dip b) All the HSQ residues removed from device top.

stay in contact with the waveguide and will be a reason for scattering loss during the light propagation through the waveguide. This will have a direct impact on the quality factors of our devices.

During our SEM investigation, we found out that our traditional steps to remove the e-beam resist was not sufficient. We noticed that even after we dip into BOE for 8-10 seconds, there is still some residual HSQ on top of our devices. Since our e-beam resist is quite thick and the etching selectivity is not a constant thing, the amount of HSQ that stays there are not always the same. In order to make sure that all the e-beam resists are gone, we dipped our wafer slightly longer (20 seconds in total for one and 30 seconds for another wafer) to make sure that all the residues are gone. Depending on the e-beam dose, development and nitride etching selectivity, this time may change. But it is for sure that any residue that stays on top of our waveguides will have a huge impact on the quality factor of the devices. The SEM images with improper HSQ removal and one with complete HSQ removal are shown in Fig 4.14.



(a) Top view



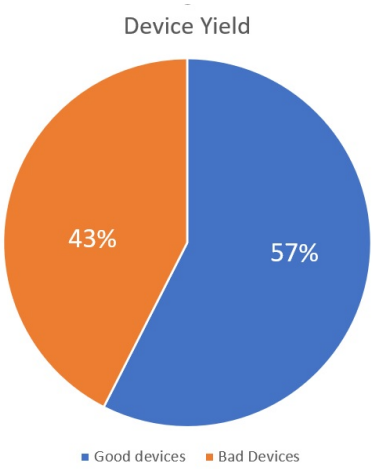
(b) Top and Sidewall view

Figure 4.15. SEM images of a) Top view of the device that shows all the residues are gone and we have a smooth top surface b) Top and sidewall view that shows we have very smooth sidewalls.

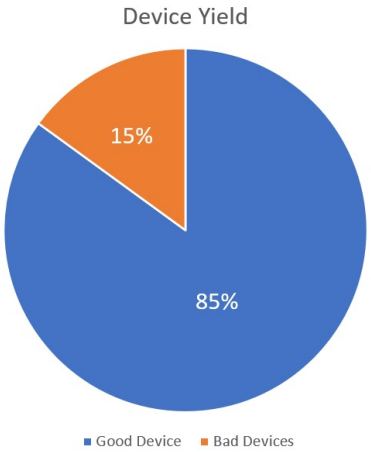
4.4.4 Implementation of changes

After finding those issues and addressing them, we fabricated a batch of chips trying to reduce those issues. Our main target was twofold: First, we wanted to check if our yield improves or not. Secondly, we wanted to check the quality factor of our chips. We checked our devices under SEM in every step of the fabrication to make sure that we did everything properly. The SEM images of the fabricated devices are shown in Fig 4.15.

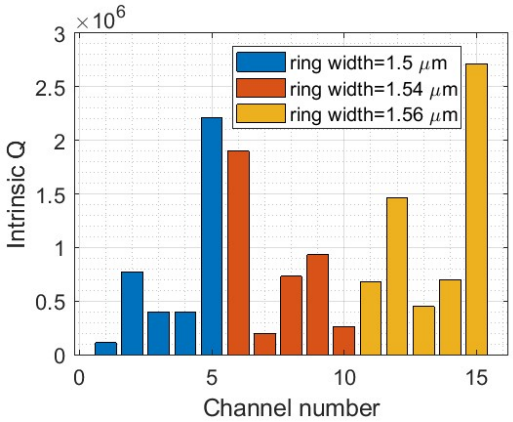
The devices were measured for those comparisons and we found a great improvement in their yield. The devices that we previously fabricated this year had only a little over 50% working devices, which was drastically improved to 85% after implementing those changes. By working devices, we mean that we can couple light into those devices, measure their transmission spectrum and see resonance dips one FSR apart as shown in Fig 1.3. The non-working devices often have etching issue and we cannot couple light into those devices. They might also suffer from film cracks or HSQ cracks (if any) in which case, they show no resonance. Also the quality factor became more uniform and improved after implementing those changes. The yield statistics is shown in Fig. 4.16



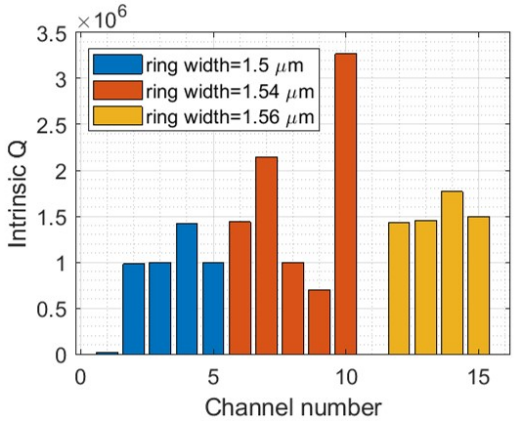
(a) Old fabrication



(b) New fabrication



(c) Old fabrication data



(d) New fabrication data

Figure 4.16. Measurement statistics between the old fabrication and modified fabrication process. a) Percentage of working devices in our earlier fabrication without those modifications b) Percentage of working devices after those modifications in process c) Quality factors of some measured devices from our earlier fabrication d) Quality factors of similar devices from our new fabrication. Image and data collection courtesy: Saleha Fatema and Cong Wang.

Those comparisons were based on similar type of devices. All devices were of comparable size (same or almost same radius, similar width etc). The data shown here are for a microring resonator with 25μm radius and about 1.5-1.6 μm width. The percentage of working device statistics was done measuring many devices. Fig. 4.16a, was constructed after measuring about 80 devices and Fig. 4.16b was constructed after measuring about 100 devices. Therefore, we can safely say that we had enough measurement done to observe the improvement in yield. Out of those devices,we tried to find devices with similar design parameters to make a comparison as shown in 4.16c and 4.16d. The data shown in those plots are the comparison between 3 microring resonators with same radius (25 μm), 3 different widths as shown by 3 different colors in the plot (values are mentioned in the legend) and 5 different gap sizes (each corresponds to a different device numbers). For devices with no resonance or no coupling are shown with 0 quality factors. For getting this statistics, we measured the transmission spectrum from 1540 nm -1560 nm and reported the best Quality factor found in this range. Also, if we see 4.16c, we only had about 27% of the chips over 1 Million intrinsic Q in our earlier fabrication. That number improved drastically to around 80% in our recent run.

Next, we tried to check for thermal performance of our devices and measured thermal broadening. We tested few devices from our old fabrication and tried to find similar devices from our new run. We measured the thermal broadening at different intracavity powers and found that our new process reduced the thermal broadening a lot as shown in Fig 4.17.

In our old fabrication process, we used to two two annealing steps (both at 1100°C for 3 hours in N_2 environment as shown in Fig 4.3. In our new fabrication process, we have three annealing steps as shown in Fig 4.10. The first annealing is at 1100°C for 3 hours in N_2 environment which is in between the Silicon Nitride film deposition. The second annealing is done after the Nitride etching and removal of HSQ step. This annealing is done at 1150°C for 3 hours in Ar environment. The last annealing is done after upper cladding deposition and it is done at 1100°C for 3 hours in N_2 environment again.

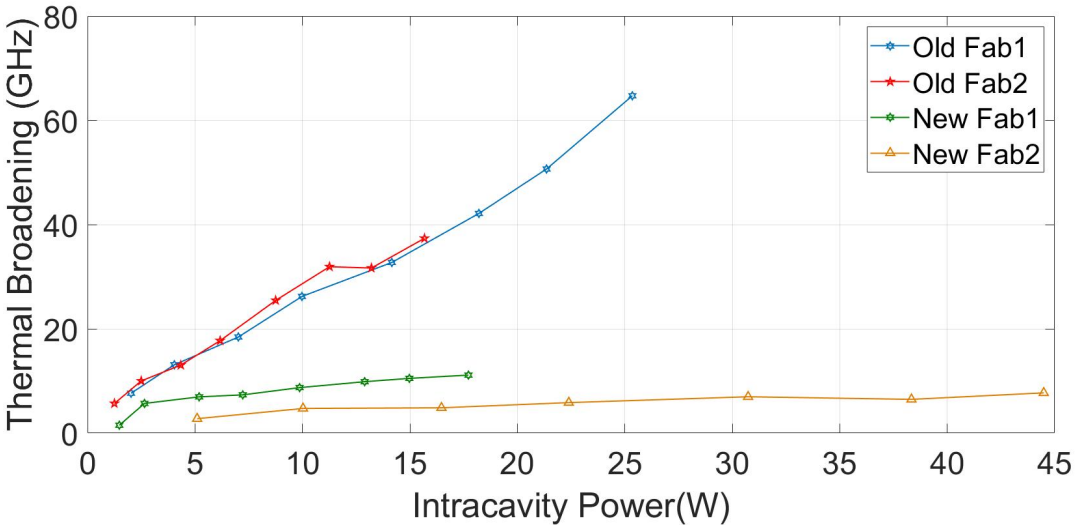
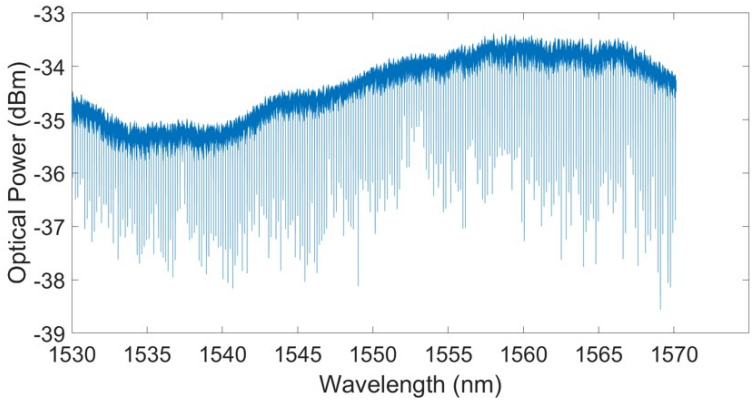


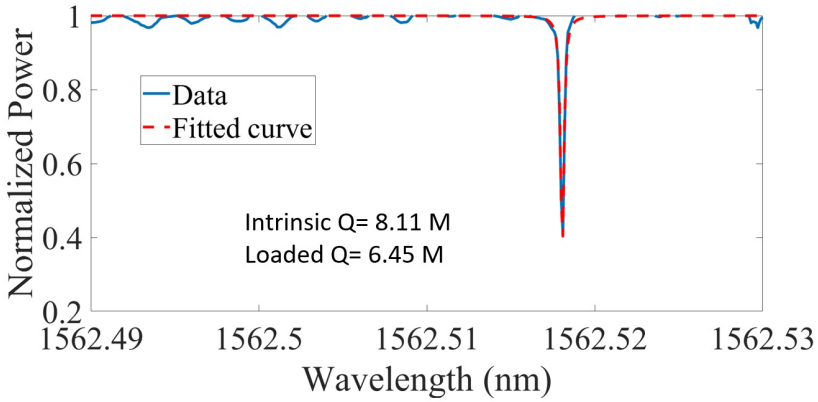
Figure 4.17. Comparison of thermal broadening between two fabrication runs. In Old fabrication run we only had two annealing steps as shown in Fig 4.3. In the new fabrication run we had three annealing steps and a few other improvements as shown in Fig 4.10.

Along with other modifications in our fabrications like modified trenching process, multi-step film deposition, all the added RCA cleaning steps, modified HSQ removal step, we think that additional annealing helped us to improve the device's thermal performance as we found from our measurements.

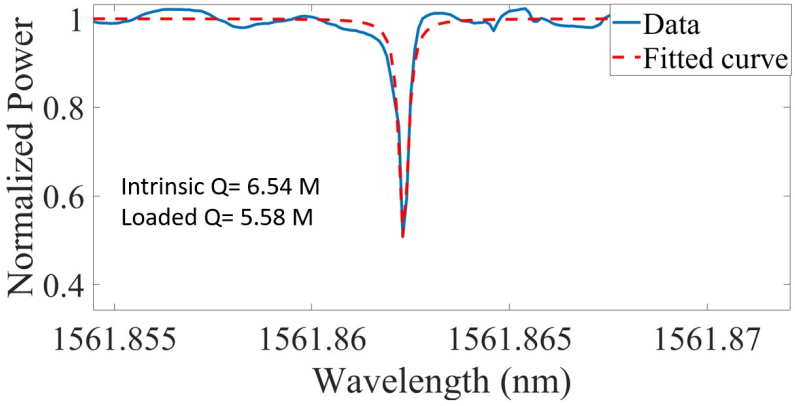
In order to test for the quality factors, we tried many types of devices and we saw a significant improvement in the quality factor of our devices. Some data is shown in the section that we just discussed. But we also got high quality factors for some other structures too. We fabricated some large structures (around 20 GHz FSR) and we found good quality factors for those devices. We want to thank Dr. Zhichao Ye and Marcello Giradi from Chalmers University of Technology at Sweden for the helpful discussion and we have tried some of the design optimization techniques that Dr. Zhichao Ye described in his PhD thesis [75]. The measurement data for one of those devices are shown in Fig. 4.18.



(a) Transmission Spectrum of the device



(b) Quality factor fitting for the resonance at 1562.5181 nm



(c) Quality factor fitting for the resonance at 1561.8623 nm

Figure 4.18. Measurement data for a large microring resonator a) The transmission spectrum of the device b) Quality factor fitting for the resonance at 1562.5181 nm. The intrinsic quality factor is about 8.11 million with a loaded Q of 6.45 million. c) Quality factor fitting for the resonance at 1561.8623 nm. The intrinsic quality factor is about 6.54 million with a loaded Q of 5.58 million.

The results shown here are for a 20 GHz FSR ring with 1.9 μm waveguide. The quality factors that were shown are the two highest quality factors that we obtained from this device. The other quality factors for many resonances lie between 4 to 5 Millions. It is worth mentioning that we found 4-5 Million Instrinsic Q for some other designs too (around 100 GHz FSR) for smaller width (around 1.5 μm). These measurements are the highest Q values that we could obtain in over last few years and certainly they open the door for many other possibilities.

Acknowledgement

We are thankful to to Birck Nanotechnology Center of Purdue University and all its staff for providing us all the fabrication opportunities. We want to specifically mention Dr. Justin Wirth, Richard Hosler, Dan Hosler, Bill Rowe and Francis Manfred's name. We appreciate all their helps and helpful discussions. We also thank Cong Wang and Saleha Fatema for helping us with optical measurements. We are thankful to Professor Tang's group from Yale university for their help in annealing. We are also thankful to Professor Victor Torres Company's group from Chalmers University of Technology at Sweden for all of their helpful discussions and suggestions. Finally we want to thank DARPA for sponsoring the project which lead to all our efforts.

5. MICROHEATER FABRICATION FOR SILICON NITRIDE MICRORING RESONATOR

In this chapter, we have discussed microheater fabrication process of Silicon Nitride microresonators. Microheaters are very useful and has recently been very popular in many engineering application. In this chapter, we have described all the steps associated with the microheater fabrication. We also showed some measurement data after doing heater characterization and made some changes to both our design and fabrication side. We also investigated the cause of some burned heaters and tried to improve both the heater performance and stability. Finally, we show some successful heater fabrication with satisfactory heater performance and better stability which was required for one of our projects.

5.1 What is a microheater?

A microheater is a thin metal resistive filament that is capable of generating heat through Joules heating. The heat production is initiated by application of sufficient voltage or current on two separate ends on the microheater, which are called heater pads. There are several materials that are used for fabricating microheaters for example Titanium [76], Platinum [77], [78], Gold (with Ti adhesion layer) [76], [79], molybdenum [80], [81], tungsten [82], [83], or polysilicon [84], [85] etc. Among them the polyslilicon heaters are limited to only 500°C due to the polysilicon electrical resistance of the heater would experience a slow uncertain change resulting from the unpredictable variation of grain boundaries above that [86]. Due to the limited availability of Molybdenum and Tungsten in our fabrication facility, our microheater fabrication was limited to Titanium, Gold and Platinum only.

Many of these microheaters are used for gas sensing, pressure sensing, flow rate sensing and other micro sensing application [76]–[78], [80]–[83] etc. But they also have significant importance in Silicon photonic devices too. Microheaters can tune the optical properties of Silicon photonic devices. This can stabilize the operating temperatures also compensate the fabrication variations. For example, for microring resonators made of Silicon Nitride, mi-

(a) Vernier scheme

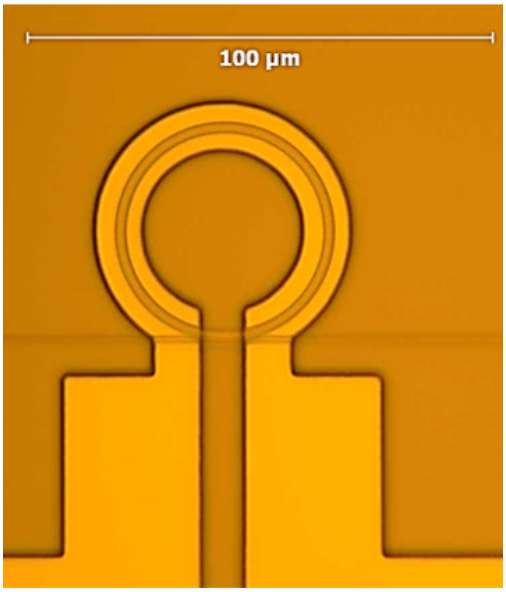
(b) 20 GHz beat note

Figure 5.1. Vernier clock scheme using two microring resonators with slightly different FSR. The figure is reproduced from [69].

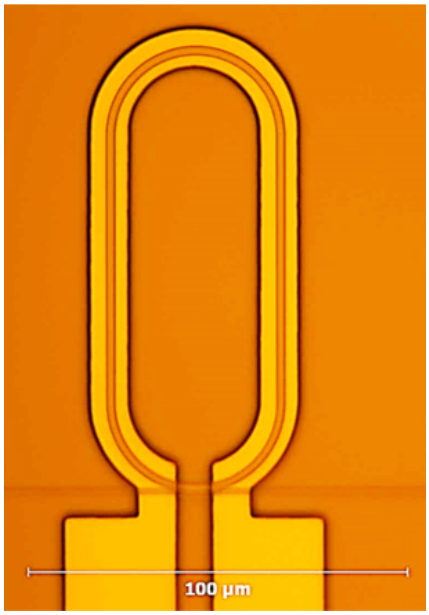
croheaters can be used to exploit the thermo-optic effect to move the resonance frequencies to a desired location (within certain range). That can lead to some exciting opportunities like controllable mode interaction to generate frequency comb in normal dispersion regime [39] or generate soliton in dual ring resonators using controllable mode interaction between those rings [87] etc.

Microheaters on microring resonators can be of different sizes and shapes depending on the requirement of the project. Usually, they need to be exactly at the top of the ring structure for efficient heating. For that reason, their shape is usually like the shape of the ring structure as shown in Fig.5.2. In order to get maximum heating, we need to cover most part of the resonator structure as shown in Fig. 5.2a and Fig. 5.2b . Again, we need to put some minimum spacing in between the heater pads in order to make sure they do not get merged together. Sometimes they may take some other forms like the zigzag structure shown in Fig. 5.2d [39]. But usually in that case, their efficiency is reduced as the heater is not covering the major part of the ring. Sometimes they can cover the half of the ring or less like Fig. 5.2c, depending on the power and thermal shift requirements.

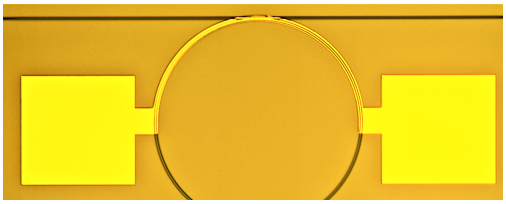
Due to the thermo-optic effect, the joule heat produced by microheater cause a change in local refractive index. That causes the resonance to move towards longer wavelengths. Applying appropriate voltage or current the resonance can be moved up to certain limit that



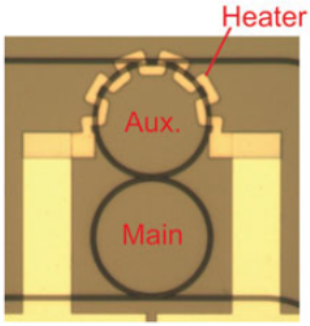
(a) Microheater on a ring (full)



(b) Microheater on a racetrack structure



(c) Microheater on a ring half



(d) Zigzag patterned microheater

Figure 5.2. Different kinds of microheaters for Silicon Nitride microresonators. a) Microheater covering most part of a full ring b) Microheater covering most part of a racetrack resonator c) Microheater covering half of a ring d) Zigzag shaped microheater on top of a dual-ring microresonator [39].

the devices can tolerate. Beyond that limit, the microheaters may break. We need to ensure that we always stay under that limit while working with microheaters.

The microheater fabrication was a very important step for one of our DARPA projects, in which we were trying to accomplish an integrated atomic clock in collaboration with Sandia National Lab. For the project, we needed to have a vernier clock with single pump, so we needed to align the resonances from both the microrings to have a beat note of 20 GHz. Also, the carrier envelope offset frequency needed to be low enough for our project, which can lie anywhere between 0 and ± FSR/2. Previously, our group member Dr. Xiaoxiao Xue showed that it is possible to shift the carrier envelope offset frequency by using microheaters on top of it [88]. Therefore, microheaters were a crucial part to accomplish the goal of the project.

5.2 Microheater Fabrication Process

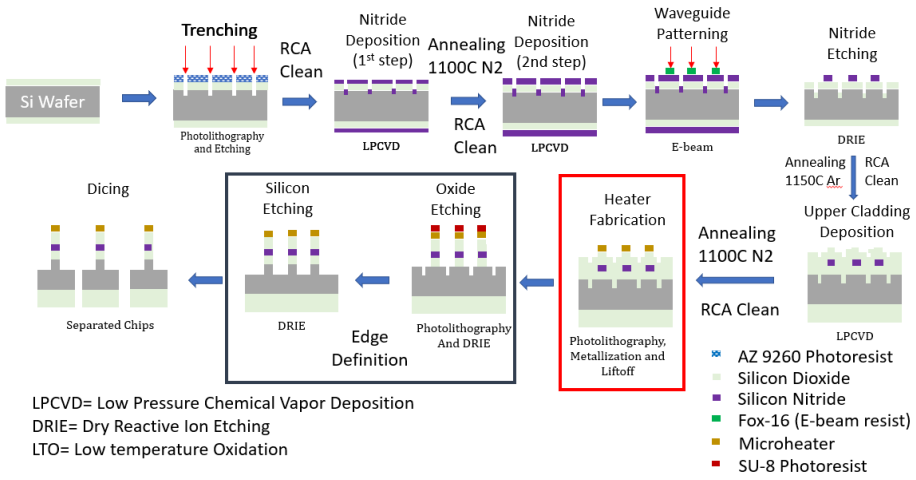


Figure 5.3. Location of heater fabrication process in the complete fabrication flow. It is usually done after the final annealing step and before the edge definition lithography step in the complete fabrication flow.

Before describing those steps, we want to show where this part lies in a complete wafer fabrication. The microheater fabrication starts after the annealing step after upper cladding deposition step in a complete wafer run as shown in Fig.5.3.

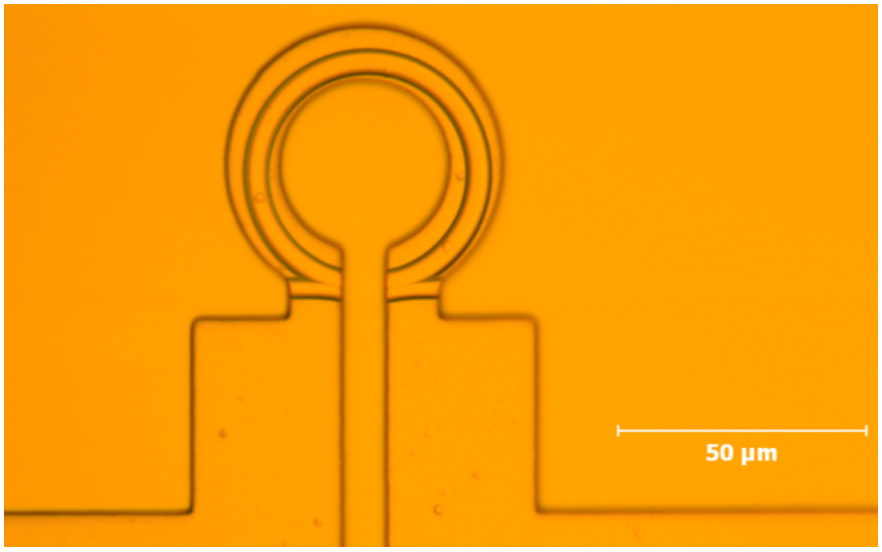
The complete microheater fabrication process can be described by 3 major fabrication steps: Photolithography, Metal deposition and Lift-off. These steps are described in the appendix with necessary details and pictures.

5.3 Challenges and Difficulties

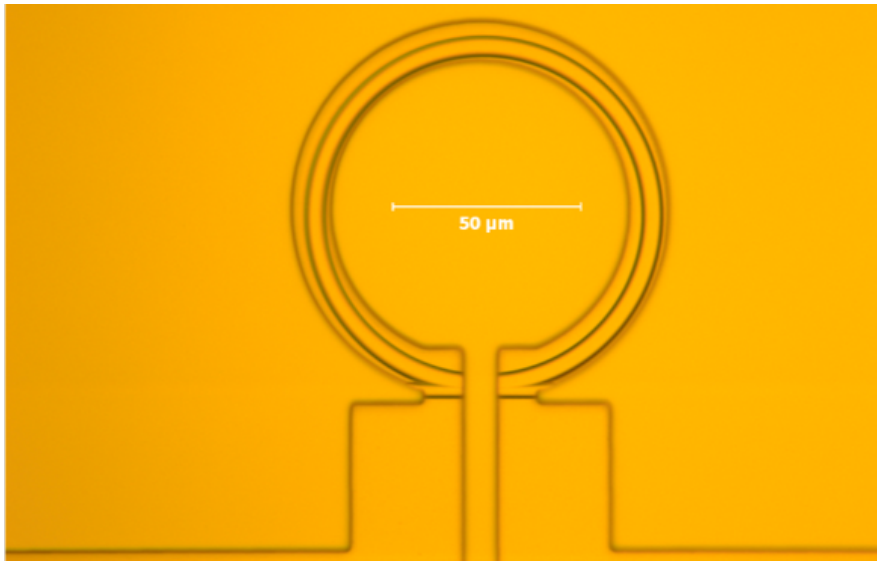
There were many difficulties in microheater fabrication. Some of them were tool related and some were design related. The first challenge was the alignment tolerance. Our microheaters had a very small margin of misalignment tolerance. Thankfully, we had heidelberg maskless lithography tool, which helped us in this case. We never used the tool before, but we were able to successfully utilize the alignment feature of the tool. During the heater fabrication process, we found several things:

- E-beam writing issue: During the microheater fabrication process, we had to align our heaters with the microring structures pattered using e-beam machine. We found that their y-axis is reversed, so we had to make changes to our microheater lithography layout to compensate that accordingly. Also, we found that during the e-beam writing we previously used single height checking virtual mark which can be a source of misalignment. We modified that and chose 4 virtual marks, which helped us to get better alignment. Fig. 5.4 shows the problem with the alignment due to the e-beam writing and Fig.5.5 show how we solved the problem.

- Beside figuring out the e-beam issue, we also tried to change the design of the microheater layout so that it can tolerate the misalignment. We increased the width of the microheater for that reason, but that did not help much. Additionally, we found out that the width has very little impact on microheater performance. As long as we cover the most part of the microring with the microheater, the impact on changing width is very small. The results of changing width is discussed later in this chapter.



(a) 1 THZ device



(b) 500 GHz device

Figure 5.4. Misalignment due to e-beam writing issue

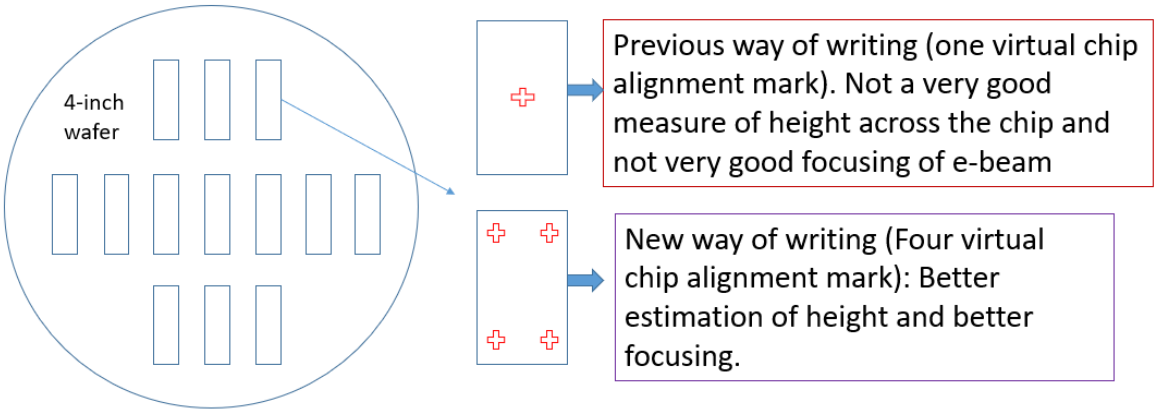
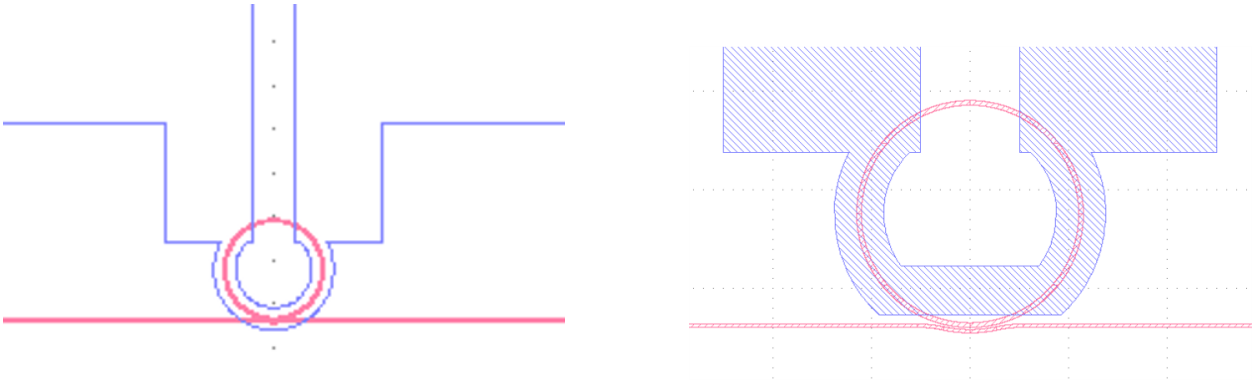


Figure 5.5. Modification of e-beam alignment marks for better alignment and writing



(a) Modified heater design 1

(b) Modified heater design 2

Figure 5.6. Modified heater designs for better stability and thermal efficiency.

- We also noticed that the heater design was not good as we had discontinuity around the coupling region area. Since there is a step around that region, this part was prone to breaking. So we decided to modify our heater designs. We tried two different designs, one covering the whole coupling region and another completely avoiding the coupling region as shown in Fig.5.6. The results of making those changes are discussed in the next section.

- Finally, in order to increase microheater stability we tried to increase the thickness of the metal. But that resulted in some problems. Firstly, we needed to do our deposition in two steps to avoid peeling off the metal during the deposition. Secondly, the liftoff

process was no longer giving us good edges and in some cases we saw no liftoff from some areas. To solve that problem, instead of using HMDS, we used Lift-Off Resist (LOR 3B). Liftoff resist are specifically used to help lift off processes. It is spun under the photoresist and not sensitive to light. But it is sensitive to the developer solution and cause an undercut during the development. That undercut ensures very little sidewall deposition and better lift-off. Fig.5.7 shows how LOR helps during the microheater fabrication by helping the liftoff process. The microheaters fabricated using LOR is shown in Fig. 5.8.

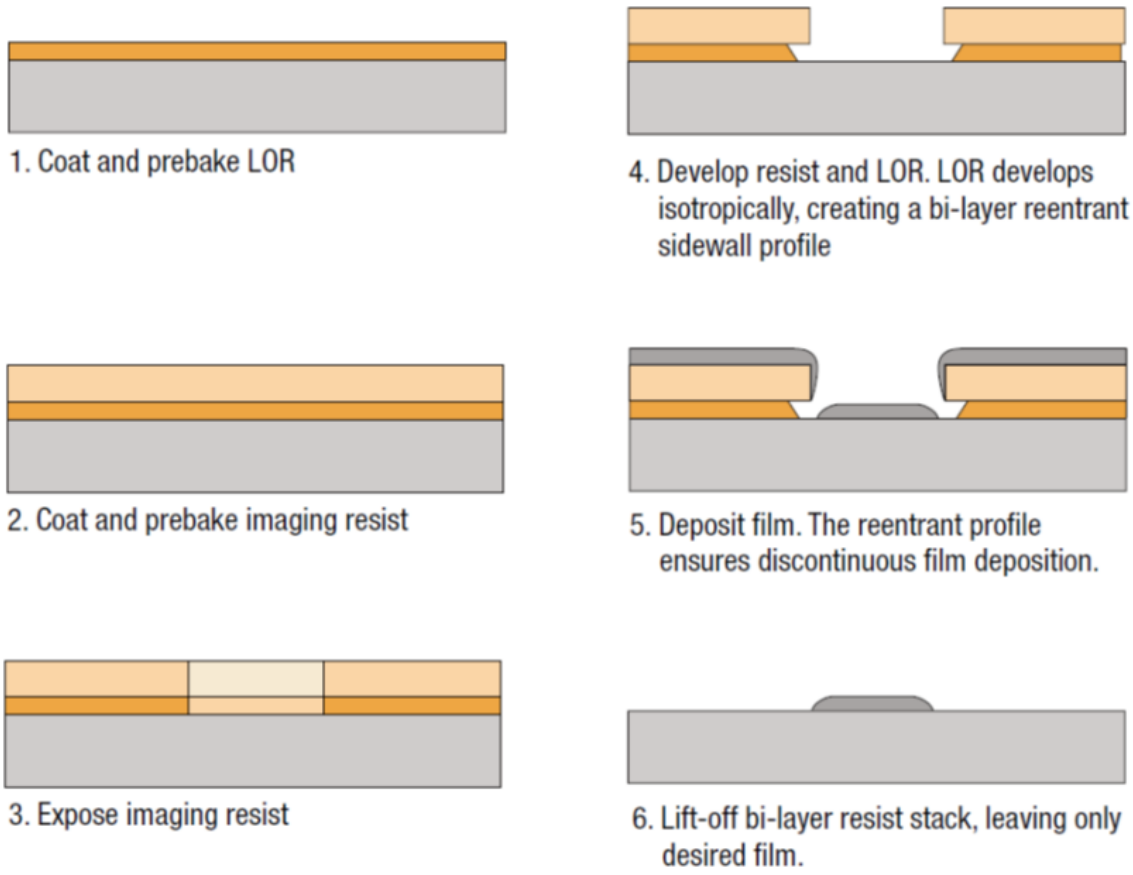


Figure 5.7. Process steps of microheater fabrication with LOR and how it helps in our liftoff process. Image courtesy: https://engineering.tufts.edu/microfab/documents/SOP_Liftoff-LOR.pdf

(a) 1 THZ device

(b) 500 GHz device

Figure 5.8. Microscopic images of micoheaters fabricated with Lift Off Resist

5.4 Characterization of microheaters

After fabricating those microheaters, we did some optical and electrical characterization of microheaters. We measured the electrical resistance using some micro-manipulator probes of heater pads. We applied voltage on both pads and tried to measure tuning efficiency. Also, we tried to check the maximum voltage we can put on the heater pads before they break. From those measurements, we also calculated the maximum thermal tuning we can do safely for our devices. We investigated the heater breaking mechanism by doing SEM and literature study. In order to increase the thermal shift capability we tried different heater materials. We fabricated microheaters with Titanium, Gold and Platinum and checked their performances. We also made changes to our designs according to the measurement results to improve our microheater performance and stability. The results of microheater characterization are described in the following subsections.

Titanium and Gold Microheaters

Our microheater fabrication started with Titanium and Gold material as we had previous experience working with those. Also because these materials are available in our fabrication facility and many researchers use them for their microheater fabrication. We tried 2 different configurations while working with these materials. In our first effort, we tried thick 300 nm Titanium (Ti) as adhesion layer with 20 nm Gold (Au) on top and used it as our microheater. During the measurements, we tried to estimate the total resistance of the microheater and also the pad resistance by using micromanipulator probes. The measured resistance ($\sim$ 20 ohms) is slightly higher than with the theoretically predicted resistance ($\sim$ 12 ohms). The main reason for the mismatch is due to the contact resistance between the probe and the microheater and some possibility of oxidation at high temperatures. As mentioned before, we can tune the resonance by applying a heater voltage, using the thermo-optic effect of Silicon Nitride. The more voltage we put in, the more heat it can generate and more shift we can get up to a certain limit, after which the microheaters will break. We tried to check the maximum resonance tuning that we can achieve before the heaters break.

We also estimated the carrier envelope offset shift due to the application of heater voltage. The carrier-envelope offset frequency (f_{CEO}) could be calculated by resonance frequency f extracted by a integer times Free Spectra Range (FSR) of the device, $f_{CEO} = f - m * FSR$. The thermal effect would shift both resonance frequency f and free spectra range FSR, which would result in the shift in offset frequency. The numbers in the table is estimated based on the simulated relationship between df/dT and df_{CEO}/dT from waveguide simulation [88]. Finally, we also estimated the electrical power requirement to shift one FSR, in which case we can line up the resonances from the vernier rings. The performance of such microheaters are described in Table. 5.1.

Table 5.1. Characterization of microheaters with 300 nm Titanium and 20 nm Gold

Parameter	**Value**
Heater width	10μm
Total heater resistance	80-180 Ω
Heater pad resistance	40-60 Ω
Maximum achievable resonance tuning	370 GHz
Estimated offset frequency shift	43 GHz
Estimated Electrical Power Requirement to shift one FSR (1 THz)	570-770 mW

The first microheater characterization was done in 1 THz microring resonators. Since the maximum achievable resonance tuning was quite small, for the next batch of characterization we used 500 GHz rings. Also to increase the thermal efficiency and reducing the contact pad resistance, we reduced the thickness of Titanium and increased the thickness of Gold. Therefore, in our second microheater fabrication, we used 20 nm Ti for adhesion layer with 300 nm Au on top and used it as our microheater. Finally, we measured all the parameters exactly the same way as we measured in our first fabrication. The characterization results of that second microheater fabrication with 20 nm Ti and 300 nm Au is shown in Table 5.2.

Table 5.2. Characterization of microheaters with 20 nm Titanium and 300 nm Gold

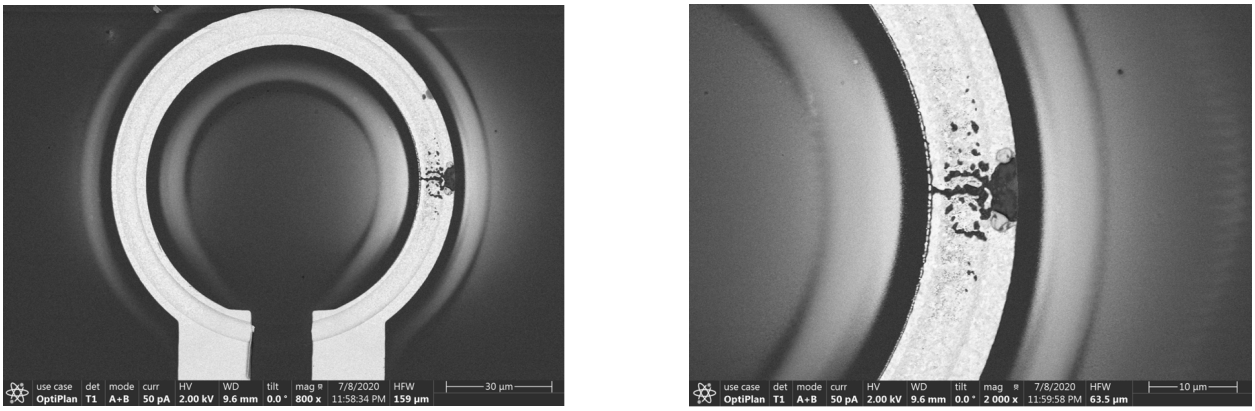
Parameter	**Value**
Heater width	10μm
Total heater resistance	7-12 Ω
Heater pad resistance	1-2 Ω
Maximum achievable resonance tuning	488 GHz
Estimated offset frequency shift	46 GHz
Estimated Electrical Power Requirement to shift one FSR (500 GHz)	500-650 mW

In that fabrication we also fabricated heaters with different width to check how much effect the width has on heater performance. We tried 2 different heater widths: 7μm heaters and 10μm heaters. We found better results for heaters with 10μm width. Their characterization data is shown in Table 5.3.

Table 5.3. Comparison of performance for microheaters with 2 different widths

Parameter	**7μm heater**	**10μm heater**
Heater width	7μm	10μm
Total heater resistance	6-14 Ω	7-12 Ω
Heater pad resistance	2-3 Ω	1-2 Ω
Maximum achievable resonance tuning	380 GHz	488 GHz
Estimated offset frequency shift	46 GHz	48 GHz
Estimated Electrical Power Requirement to shift one FSR (500 GHz)	500-650 mW	500-650 mW

At this stage, we tried to investigate the cause of our heater damage. After some literature review and SEM inspection, we came to the conclusion that the the heaters broke because of Electromigration of Gold atoms.



(a) A burned microheater (b) Zoomed-in view

Figure 5.9. SEM images of burned microheaters

Electromigration

Electromigration is a process by which the metallic ions inside a thin film are gradually moved to another location, due to the momentum transfer between electrons and diffusing metal atoms, when an external electric field is applied to it. Electromigration is very common at thin films specially at high powers, when the current density exceeds certain value called maximum current density. It was first reported many years ago by French scientist Gerardin [89]. After that it was not explored much until 1960s, when Integrated Circuits started to get popularity. The first observation of Electromigration on thin films was reported by Blech [90] in thin aluminum films on Titanium Nitride. Since then many efforts were put to avoid the irreversible damage. Several ways that we tried, by which it can be reduced, include changing materials (using metals that can withstand higher current density), changing design parameters (height and width) to reduce current densities etc. Some SEM images of our burned heaters are shown in Fig. 5.9

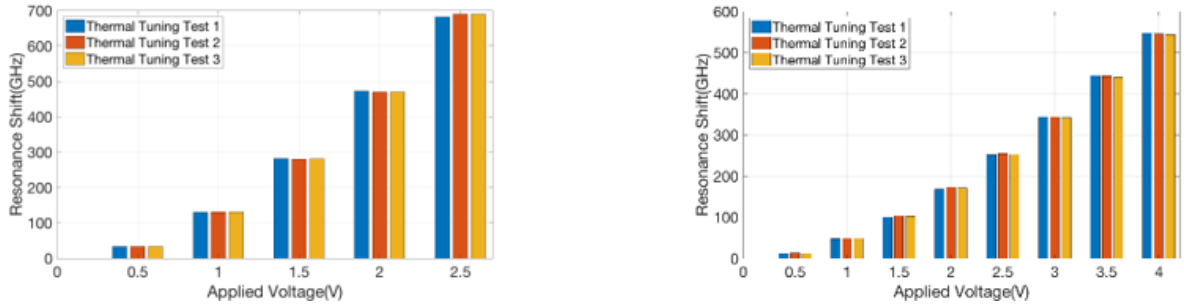
To verify, we tried to measure the current density of those Ti/Au heaters and we found that the current density before the heaters broke was about $1.6\times10^{7} A/cm^{2}$, which is pretty high for Gold to handle and that further proves that the breakage of microheaters were due to the electromigration effect.

Platinum microheaters

To check for new materials that has high current handling capability as well as availability in our fabrication facility. Platinum (Pt) was the best candidate for us as it can handle high current density ($\sim 3\times10^6 A/cm^2$) [91] and it was available in our fabrication facility. So we tried to fabricate our microheaters with Platinum with Ti as adhesive layer. Also to improve the stability of our heaters and to heat them for a long time (several hours), we decided to increase our heater thickness to 600 nm. But we had to do it in two steps (300nm deposition each time) in order to avoid the heater peeling off and better uniformity. The electrical characterization data for those microheaters are shown in Table 5.4. All the measurements were performed exactly like the same way we did for the previous microheaters. Also, We did not have any direct measurement for the microheater temperatures. However, The temperature can be estimated by resonance tuning range and simulated resonance tuning per degree C df/dT in waveguide simulation. Assuming the microheater in room temperature, the change in resistance suggests that the temperature at maximum tuning was 314°C. But more measurements and analysis are necessary for properly estimating the microheater temperatures.

Table 5.4. Characterization of microheaters made of 20nm Ti and 600nm Platinum

Parameter	**1 THz device**	**500 GHz device**
Heater width	10μm	10μm
Total heater resistance	7.3-14.6 Ω	7.6-15.4 Ω
Heater pad resistance	5-6 Ω	5-6 Ω
Maximum achievable resonance tuning	1023 GHz	1203 GHz
Estimated offset frequency shift	119 GHz	140 GHz
Estimated Electrical Power Requirement to shift one FSR	550 mW	510 mW



(a) 1 THz devices

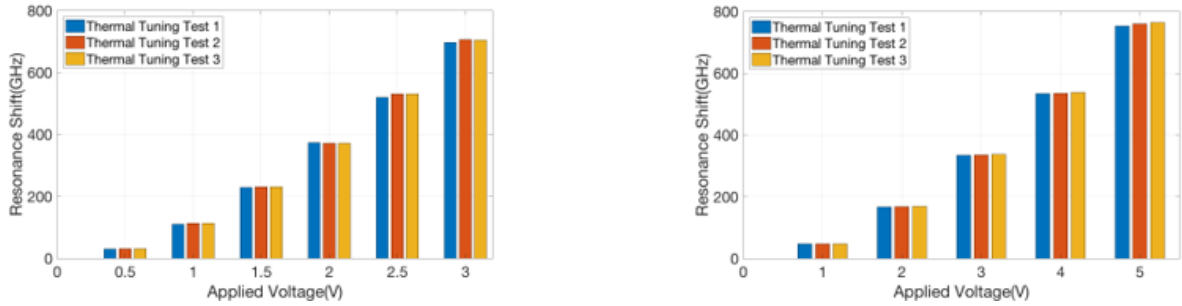
(b) 500 GHz devices

Figure 5.10. Short term (10 mins) stability test for Ti/Pt microheaters (Image courtesy: Cong Wang)

Stability check

For our project, it was important that the microheater performance was repeatable and consistent for long time heating. So after getting the desired shifts, we wanted to check how the microheaters perform when we heat them up for longer times. But before heating them up for long periods, we did some short time test as well to make sure that they pass those tests. In this part, we will discuss those results from the short and long term stability performance check for the microheaters. For 1 THz devices, reaching the maximum limit may burn the microheaters. So, we tried to reach 70% of the maximum achievable shift and let it stay there for the fixed amount of time to check if the performance degrades if we try to repeat it again. For 500 GHz devices, we were able to safely shift the resonances over one FSR. The results of short term stability were obtained by applying a voltage to the microheater for 10 mins and measuring the resonance shift. The results are shown in Fig. 5.10.

The short term stability shows consistent and repeatable results at different voltage levels. More importantly, the microheaters were stable and did not burn during the process. To further test their stability, we did some long term stability test. In this case, we put the same voltage constantly for an hour and found that the results are still repeatable. The results for one hour of constant heating are shown in Fig 5.11.



(a) 1 THz devices

(b) 500 GHz devices

Figure 5.11. Long term (1 hour) stability test for Ti/Pt microheaters (Image courtesy: Cong Wang)

Finally, we heat up the microheaters for 3 hours and checked their performances. The microheaters were able to successfully withstand that long heating. And we also got more than 1 FSR thermal tuning for both 1 THz and 500 GHz device. The estimated carrier offset frequency shift was more than 100 GHz. The measurement results are shown in table 5.5.

Table 5.5. Performance of microheaters after three hour long constant heating

Parameter	**1 THz device**	**500 GHz device**
Heater width	10μm	10μm
Total heater resistance	7.3-14.6 Ω	7.6-15.4 Ω
Heater pad resistance	5-6 Ω	5-6 Ω
Maximum resonance tuning without damage	670 GHz	730 GHz
Maximum current density	$3.05\times10^{6} A/cm^{2}$	$3\times10^{6} A/cm^{2}$

5.5 Summary

In this chapter, we have described a successful microheater fabrication process and its evolution. We have described all the process steps and show electrical and optical characterization results of our fabricated microheaters. To increase the efficiency and stability of our heaters, we changed our heater materials from Ti/Au combination to Ti/Pt combination, where Ti was used an adhesion layer. Using our fabricated microheaters we were not only

able to move one full FSR of our ring resonators (which is very important for our DARPA A-Phi project), but also were able to withstand long heating (tested upto 3 hours). We hope that this microheater fabrication will also help us to explore many things in future, such as controllable mode interaction, integrated frequency comb generation and many other applications.

Acknowledgement

We are thankful to Cong Wang for characterization part of this work. We are also thankful to Birck Nanotechnogy center and the research engineers working there for providing us all the fabrication tools and keeping them up. I want to specifically thank Dr. Justin Wirth, Dr. Joon Park and Richard Hosler for their help and useful conversations. Finally, we are thankful to Defense Advance Research Project Agency (DARPA) for sponsoring the project which led us to develop this fabrication process.

6. EDGE POLISHING PROCESS FOR SILICON NITRIDE MICRORESONATOR

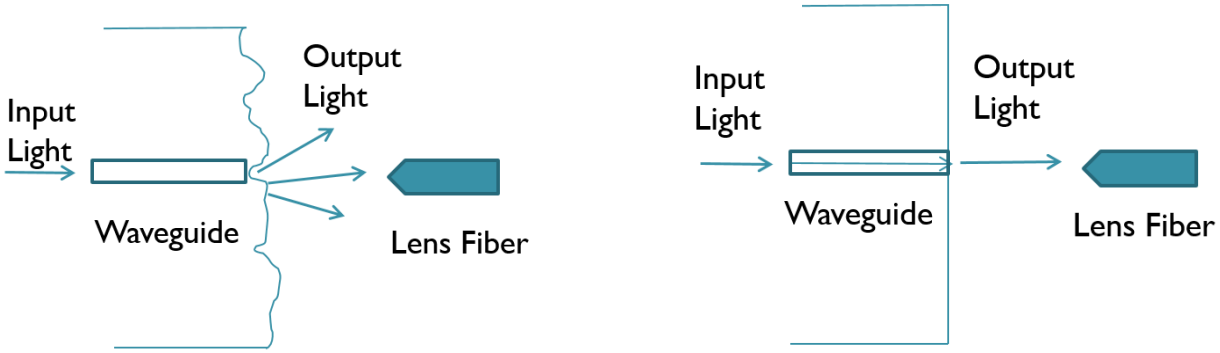
In this chapter, we have discussed an edge polishing process of Silicon Nitride microresonators, which uses mechanical polishing method and the process was developed from scratch. This polishing process was intended to make our samples ready for heterogeneous integration with an Indium Phosphide chip. Beside that, polishing makes the edges of our chips optical flat which reduces the insertion loss and it creates opportunity for a lot of interesting things e.g. on chip frequency comb generation. This process is not only of low cost, but also is reliable, have good control over the process and produced satisfactory results.

6.1 Edge Polishing Process

Polishing or grinding is a process of removing some material forcefully either by mechanical pressure and rubbing or by chemical reaction to make the surface or edge smoother. In other words, it is a process for reducing surface or edge roughness. Usually polishing requires thorough cleaning before and after the process to make sure no debris or unwanted materials remain on the desired surface.

Polishing of photonic chips can be classified into two major types: Surface polishing and edge polishing. Surface polishing is very common and has lots of developed tools and techniques to do so. It is the most common and popular polishing method in industries. The edge polishing, on the other hand, an inherently difficult process. It is not very common and requires a completely different set up and technique.

There are numerous methods for polishing, among them the most common methods are Mechanical Polishing (without using any chemicals) and Chemical Mechanical Polishing (CMP). CMP is very popular in industries because of its good control on removal rate, reliability and wide range of applications [92]. The mechanical polishing is also popular



(a) Unpolished Rough Edge (b) Polished Flat Edge]

Figure 6.1. The problem with a rough edge at the end of photonic chips (a) An unpolished rough edge where the light scatters away while coming out (b) A polished flat edge with low or no scattering

because of being less complex, can be modified easily and for being user friendly. Depending on polishing requirements, either of them can produce good results.

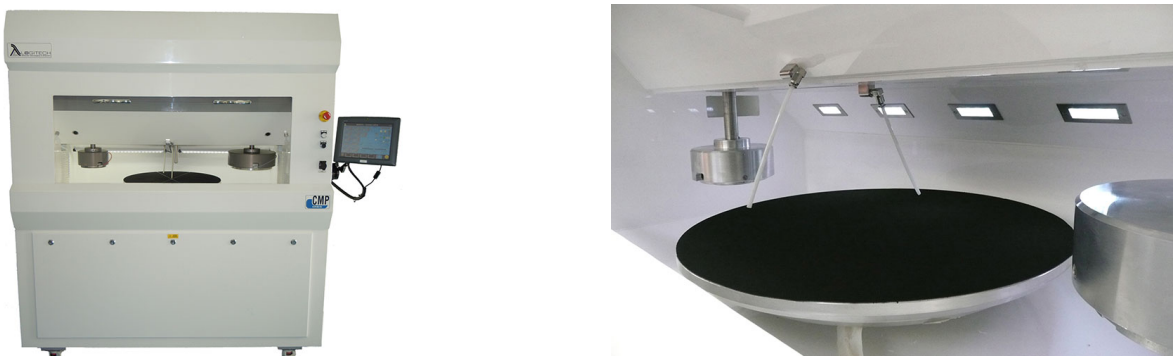
Why polishing is needed?

For photonic chips, the edges are usually formed by cleaving, chemical etching or mechanical dicing process during fabrication and neither of which gives optically flat surface. In order to get optically flat surface, edges from where light enters into or comes out of the bus waveguide of our microresonators need to be polished.

Edge polishing is important because it can reduce the scattering and helps to process different kinds of photonic integration. Polishing also can potentially reduce the insertion loss and make the chip suitable for various applications like frequency comb generation. In this work, our goal was to do heterogeneous integration with an Indium Phosphide chip.

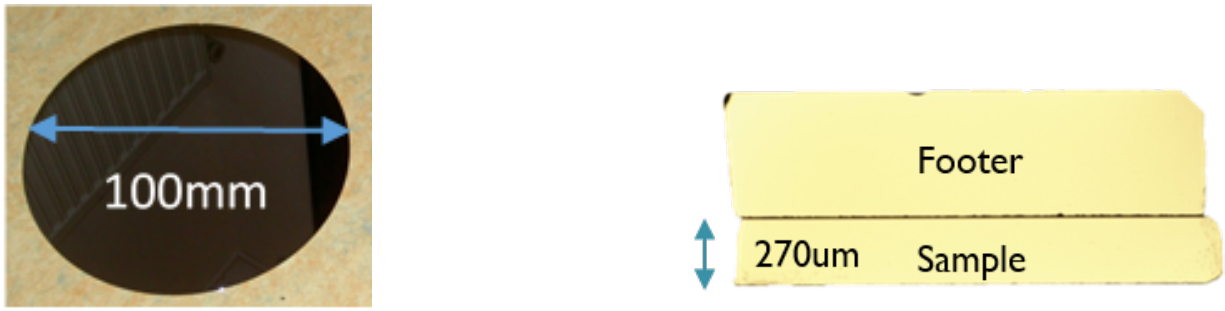
Why CMP was not used?

CMP uses a chemical slurry that etches away the materials along with the mechanical pressure induced grinding. This process needs costly materials including the machine itself, the pads, the sample holder and the slurry needed for different kind of polishing. Mechani-



(a) A CMP Machine (b) Polishing Pad and holder of CMP

Figure 6.2. Logitech Orbis Chemical Mechanical Polisher (a) The CMP machine (b) The Polishing pad and holder inside the CMP machine. The photos are taken from https://logitech.uk.com/product/orbis-cmp-solution/



(a) A Polished Surface (b) A Polished Edge

Figure 6.3. The difference between surface polishing and edge polishing. (a) A Polished surface, which has a large polishing area (b) A polished edge, which has a smaller area to polish

cal polishing on the other hand does not require slurry and depending on the material that need to be polished, different kind of polishing pads are available commercially. The major difference between the CMP and the mechanical polishing is the use slurry or the chemical that etch away some additional material to make the process faster. On the other hand, mechanical polishing method is very flexible. It can be customized according to the requirements and the user can choose own materials to develop a process.

Despite CMP being the more popular method of polishing, it was not chosen for several reasons. Firstly, because we did not have a CMP facility available nearby. The use of near-

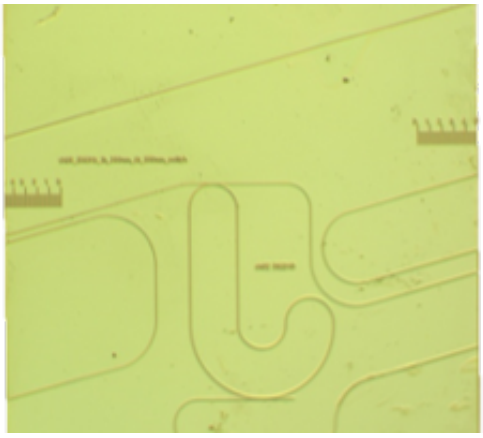
est CMP machine needed frequent transportation and that was not feasible considering the enormous amount of time needed to develop the recipe. In addition, buying all those pads and chemicals along with the equipment was beyond our financial budget. Thirdly, doing edge polishing using CMP is inherently difficult because of the small edge surface that the user has to deal with. In addition, mounting a chip on the polishing holder is very difficult and customized polishing holders may be needed which must be compatible with the machine.

Therefore, a cheaper alternative polishing method was chosen which uses just the mechanical polishing method without any chemical slurry and a customized sample holder was designed to hold those samples. For mechanical polishing, no machine was used; polishing was done by loading the sample of sample holder and then grinding it on polishing paper by hand. Finally, this process is very fast and can produce reasonably good results.

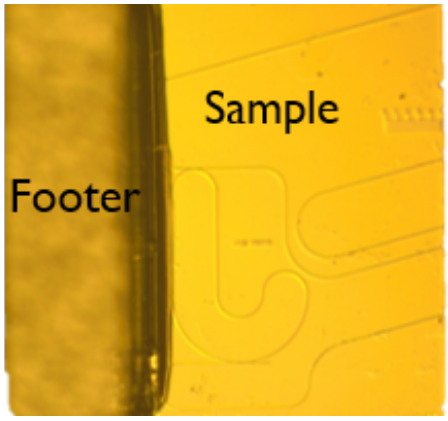
6.2 Overview and Difficulties

The edge polishing process was developed from scratch. The first challenge was to overcome the small surface area issue. It was addressed by adding an additional piece of Silicon on top of the sample, which we termed as footer. The footer was initially introduced to help the heterogeneous integration process, but it also helped the polishing process by increasing the polishing surface area and protecting the edge. The footer was attached to the sample using a chemical epoxy EPO-TEK OG198-54 from Epoxy technology, which requires UV curing and provides excellent attachment. Fig 6.4 shows a sample with and without footer.

The second and harder difficulty was designing a sample holder that can hold the sample perpendicularly during edge polishing. The traditional sample holders cannot hold the sample for edge polishing. Therefore, a new sample holder needed to be designed with some specific features for edge polishing. A few iterations were needed to come up with an improved design. For proper attachment to the sample holder, we used crystal bond and align the sample carefully to the sample holder to ensure uniform polishing.



(a) Without footer (Top View)



(b) With footer (Top view)

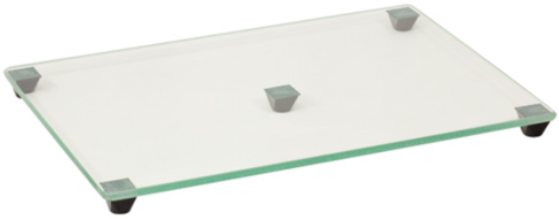
(c) With footer (Side view)

Figure 6.4. Importance of Footer (Small Silicon chuck on top of the sample)

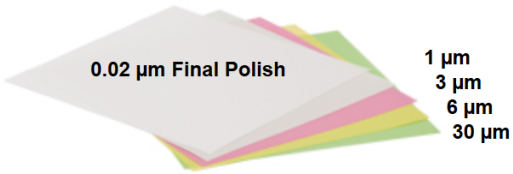
(a) Customized Sample Holder

(b) Crystal Bond 509

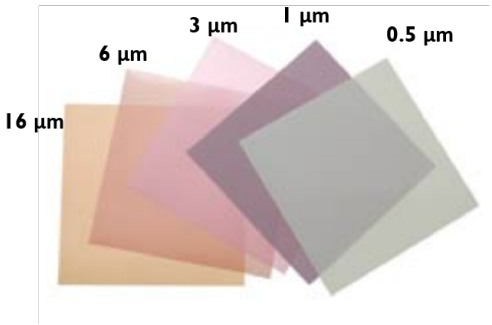
(c) EPO-TEK OG198-54



(d) Glass Plate



(e) Grit papers from ThorLabs Inc.



(f) Grit Papers from TedPella Inc.

Figure 6.5. Chemicals and materials used for the edge polishing process

The polishing was done on diamond polishing grit papers commercially available from TedPella Inc. and ThorLabs Inc. Different grit sizes were chosen from the vendors and starting from the largest grit of 30 μm, the samples were polished down to 20 nm grits. For stability and uniformity a plain glass plate was used. DI water was used as a lubricant and to remove away all the debris generated from the polishing process. All the chemicals and materials that were used for the polishing process are shown in Fig. 6.5.

6.3 The Steps of the Edge Polishing Process

The whole polishing process can be summarized by the following flow chart (Fig. 6.6).

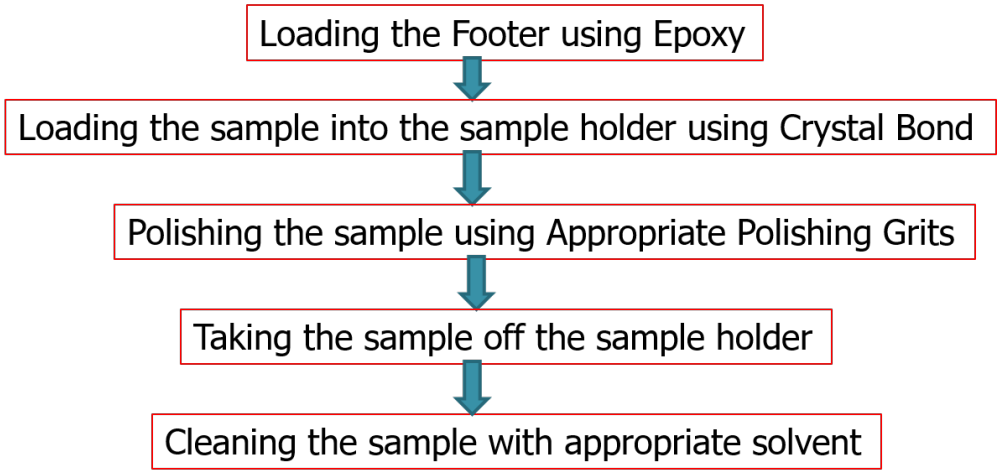


Figure 6.6. All the major steps of the edge polishing process

The first step of the polishing process is placing the footer on top of the sample to protect the polishing edge and provide better mechanical stability while polishing the samples. We first choose the proper edge. Then we spread epoxy near that edge using an optical fiber tip. After that, we place the footer there, align it to the sample edge by pushing both the sample and the footer together against the sample holder. Once the alignment looks good, we cure the epoxy exposing to UV ray first and then heating the sample on hotplate at 130 degree for about an hour. The details of the process is discussed in Appendix.

Next step is to load the sample on sample holder. We heat up the sample holder first to apply crystalbond. We put the dummy samples into the groove first and then glue the main sample to the Silicon pieces using the crystalbond. After that, we let the sample holder cool down a little by putting it into a bowl of DI water. then we check the alignment using a small glass plate. If everything is good, it goes to the polishing, otherwise everything is repeated again. The details of this step is described in Appendix.

In the next step, we polished the samples on diamond grit papers of different grit sizes starting from 30μm. Then we went down to 16μm, 6μm, 3μm, 1μm, 500 nm and 20 nm grit papers. The amount of pressure and speed were important during the polishing process. During the polishing process, we followed a zigzag pattern for better uniformity. We used a glass plate to hold the diamond grit papers which acted as a base during the whole process. To remove debris created during the polishing process, we used DI water as lubricant. After polishing, we cleaned the samples using DI water and then blow dry with nitrogen. Finally, we observed them under the microscope. The impact of the polishing is shown in Fig. 6.7, where the polished edge was observed under the microscope after each grit paper. We can see the gradual improvement after each grit paper.

After the polishing is complete and the edge looks good, the sample is taken off the sample holder by heating up the sample and melting the crystalbond. Finally, we clean the sample using crystalbond 509 remover solution. We perform ultrasonic cleaning for 3-5 minutes first. Then, we clean the sample using cloronox solution for a few seconds. Finally, we rinse the sample with DI water and blow dry using a nitrogen gun. The details of these steps are described in Appendix B.

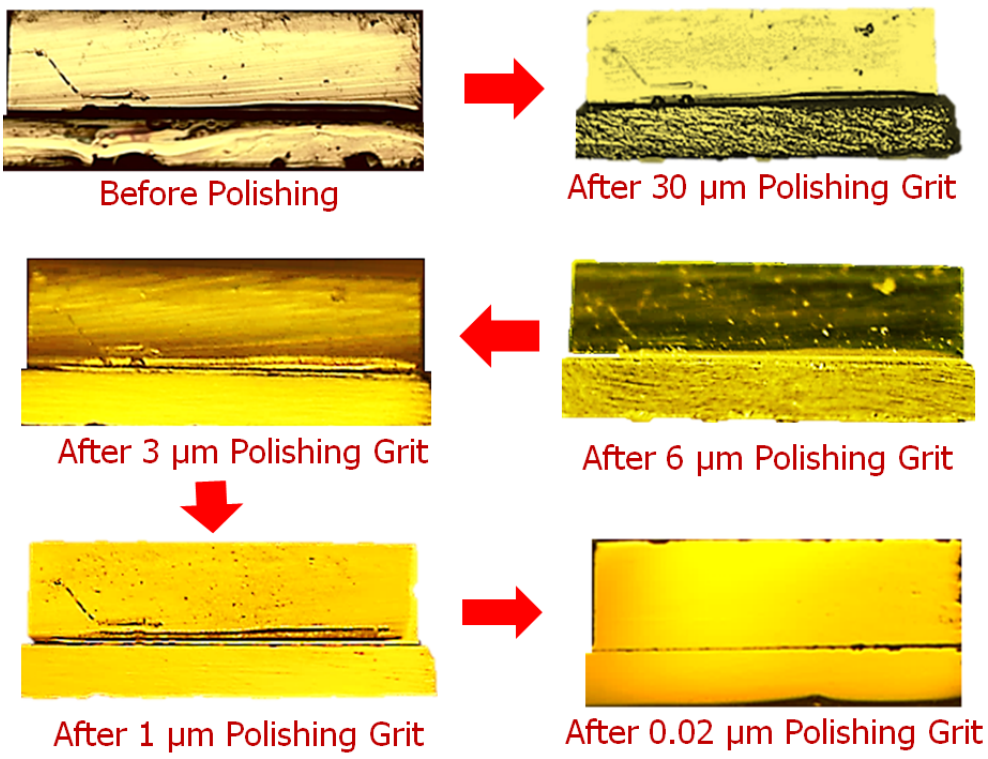


Figure 6.7. The effect of polishing on the edge. Starting from 30 μm grit and going down to 20nm grit. Gradual improvement is noticeable as grit size goes from coarse grits to finer grits

6.4 Results

6.4.1 SEM images

After finishing the polishing process, some of the samples were observed under the SEM. The edges looked very good and smooth. Some SEM pictures of the polished chips are shown in Fig. 6.8.

6.4.2 Measurement results

After finishing the polishing, we measured different things in order to check the optical performance of the polished devices. One of the important things to measure after polishing was the insertion loss measurement. In order to measure insertion losses, we have used lensed fiber setup for coupling light in and out of the chip. We have used a 5-axis stages which has

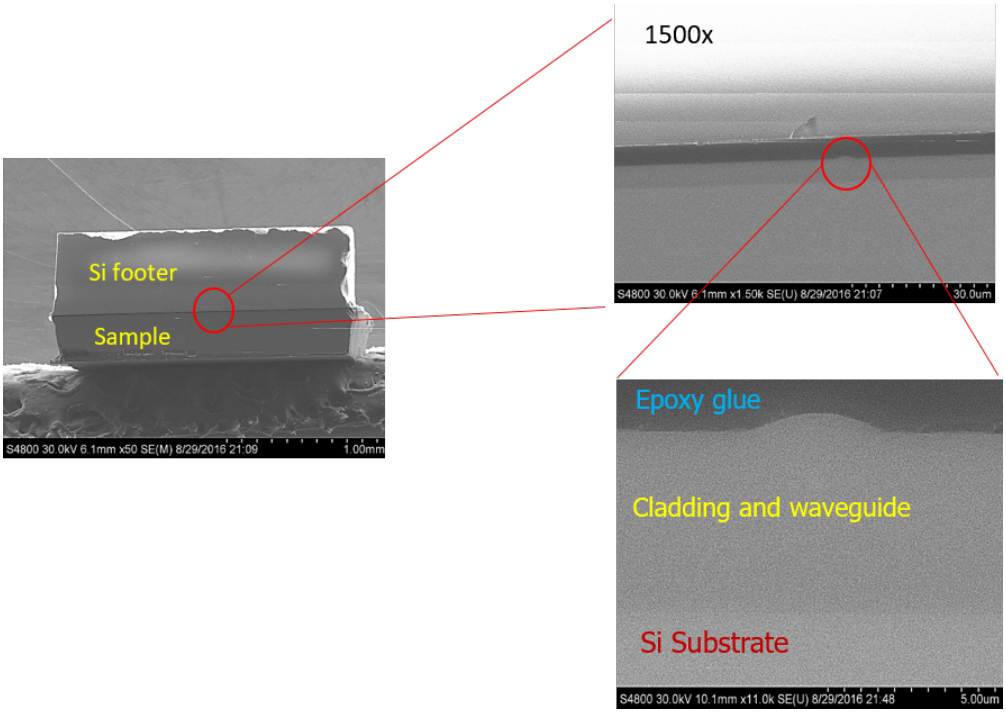


Figure 6.8. The SEM images of the polished chips

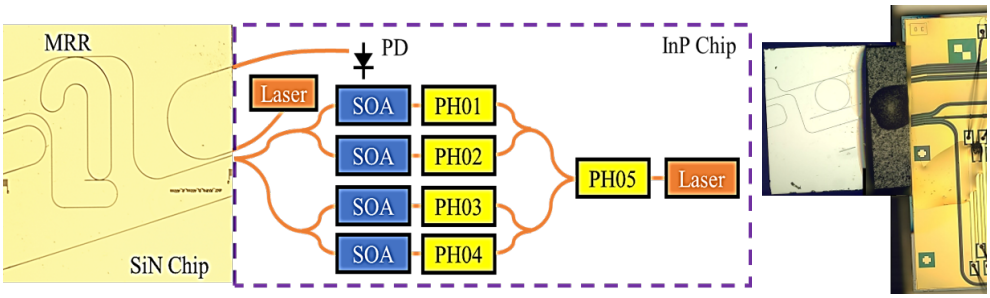
precision micrometer screws to hold and move the lens fibers close to the chip to couple the light. A tunable laser was used to send light into the chip and a detector was used to sense the power coupled out of the chip through the lens fiber. It is worth mentioning that in our fabrication process, we tried to optimize the process so that the edges of our chips after etching is almost vertical. Thus the insertion loss before polishing is not that high. Our main purpose here was to prepare the sample for heterogeneous integration. So we needed to make sure that the after polishing, the loss was still low and within reasonable limit. The measurement results of some chips before and after polishing is shown below in table 6.1:

6.4.3 The Heterogeneous Integration

After screening the devices, we sent some chips to Infinera Inc. for heterogeneous integration with an Indium Phosphide chip. The schematic diagram for the integrated chips are shown in Fig 6.9. The heterogeneous integration was done by placing the chips side by side, align them using the alignment loops as shown in Fig 6.9a and placing index matching glue

Table 6.1. Insertion Loss measurement results before and after polishing process

Chip label	Cross Section of the sample (μm×nm)	Insertion Loss before polishing (dB)	Insertion Loss after polishing (dB)
D18	2×770	8.8	5.8
D20	2×770	6.7	5.9
D29	2×770	5.8	6.4
D30	2×770	6.8	6.9
D34	2×770	7.1	6.2
F24	2×580	6.5	5.4
F26	2×580	9.5	6.6
M12	2×770	7.2	5.1



(a) schematic view (b) Real assembly

Figure 6.9. The heterogeneous integration of SiN-InP chip a) Schematic view of the integration b) Real assembly. This figure is taken from [93]

in between them.

After successful integration, we tested the bonded assembly using the on-chip laser on InP chip. The insertion loss of the bonded system was small (around 6 dB) and we were able to measure the transmission spectrum for a very small range. The measured data is shown in Fig. 6.10. The measured results showed consistency with the expected 50GHz FSR and showed multiple mode families. This figure is taken from [93].

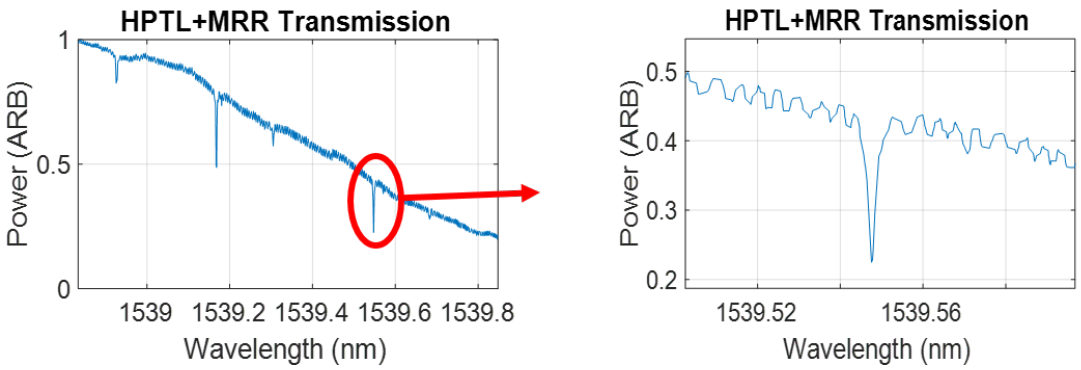


Figure 6.10. The short transmission spectrum of the bonded assembly [93]

6.5 Summary

In this chapter, we have shown a cheap yet effective edge polishing method using hand held mechanical polishing. With limited resources and expertise, we developed this process from scratch and the results were satisfactory. The polished chips looked good under the microscope and the SEM. The measurement results were satisfactory and consistent. Another way to measure the success was the successful heterogeneous integration of the polished chips with InP chips by Infinera Inc. The bonded chips with low insertion loss were successfully tuned for a small range and showed good potential for on-chip frequency comb generation.

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7. CONCLUSION

In this report, we have discussed the fabrication and optical characterization of different kinds of photonic devices based on Silicon and Silicon Nitride platform.

We started with the fabrication and loss characterization of a novel device named E-skid as proposed in [8] which shows a new way of light confinement in photonic devices. The introduction of all dielectric anisotropic metamaterials allows the reduction of decay length of the evanescent wave. We discussed some challenges in the fabrication based on SOI and how we overcame the issues. We also showed that the introduction of those metamaterial structures add only a very small amount of losses which is negligible making this design suitable for a lot of applications. The crosstalk measurement for such devices show very low crosstalk among neighboring channels. Thus it paves way to miniaturization and dense integration of photonic devices.

Then we discussed about the fabrication and characterization of higher order mode filter designs using MMI. The devices were fabricated using SOI platform. The mode filters can effectively allow TE_1 to pass with low insertion loss while blocking TE_0 mode. Experimental demonstration shows 1.5 dB insertion loss for TE_1 with 15 dB rejection of TE_0 over C band. Cascaded filter with higher insertion loss and better extinction ratio is also demonstrated.

We showed the silicon nitride fabrication process and all the steps associated with it. In order to improve our process, we did a comparative study with other research groups that also fabricate similar devices. We added some new steps to our fabrication for improving the performance of our devices. We also investigated the reason for our low quality factor devices and identified some reasons for that. We fabricated some devices addressing those issues and saw an improvement in both the quality factor and yield of our fabrication. Finally, we showed an exciting alternative to traditional LTO to deposit SiO_2 on top of wafer as upper cladding. The RTP processing of HSQ was developed along with the edge bead removal process that allowed the films to withstand thermal stress. Multiple layers

of HSQ can be stacked to make a thicker film, however there is a thickness limit beyond which that is not possible. But it is possible to fill up the rest of the upper cladding with LTO or PECVD. Also we have seen very good refractive index matching with SiO_2 after the process verified by ellipsometry measurement. We fabricated devices using this as our immediate contact to the waveguide and saw satisfactory results that shows promise for the future.

We also discussed the microheater fabrication process on top of our silicon nitride waveguides. We explored different matrials to find the correct one to have the sufficient ability to shift resonances. We also checked the stability of those microheaters and investigated the reason of their breakage at high voltage. We also cheked the stability of the microheaters by doing and short and long time measurements.

Finally, we described an edge polishing process of Silicon Nitride resonator which was built from scratch. This process is of low cost, have fast turnout and pretty much repeatable and reliable. The edge polishing process effectively prepared our samples for a successful heterogeneous integration with InP chips. The heterogeneously integrated chips showed low insertion loss and we were able to tune it to obtain some transmission spectrum which shows great potential for on-chip frequency comb generation.

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A. BASIC FABRICATION PROCESS STEPS

A.1 Deposition

In fabrication, deposition is a process that grows, coats, or otherwise transfers a material onto the wafer using some tools/techniques. The most common deposition techniques that we follow are intended to deposit film at different stages of our fabrication. Usually they are performed in horizontal furnaces at a low pressure chamber and that process is called Low Pressure Chemical Vapor Deposition (LPCVD). LPCVD is a very popular deposition method that is used to produce high quality, high-performance, solid materials, typically under vacuum. Reduced pressures tend to reduce unwanted gas-phase reactions and improve film uniformity across the wafer. This process is often used in the semiconductor industry to produce thin films. In our fabrication process, we usually deposit Silicon Dioxide by using thermal oxidation and Low Temperature Oxidation process. We also deposit stoichiometric thin Silicon Nitride film using those horizontal furnaces. These horizontal furnaces are useful for high temperature annealing too, which is a heat treatment that alters the physical and sometimes chemical properties of a material to increase its ductility and reduce its hardness, making it more workable. An example of a horizontal furnace, name protemp horizontal furnace is shown in Fig. A.1a.

For metal deposition, we use thermal evaporation, a popular kind of Physical Vapor Deposition technique, to deposit desired metals on top of our wafer. It also uses vacuum technology for applying coatings of pure materials to the surface of various objects. The coatings, also called films, are usually in the thickness range of angstroms to microns and can be a single material, or can be multiple materials in a layered structure. An example of a thermal evaporator tool is shown in Fig. A.1b.

A.2 Photolithography

Photolithography is a process of transferring any pattern to wafer surface. It is usually done by using a mask, called photomask, which effectively transfers the pattern through a

(a) Horizontal furnaces for LPCVD

(b) Thermal evaporator for metal deposition

Figure A.1. Different deposition tools (a) Horizontal furnaces for LPCVD of thin films (b) Thermal evaporator for metal deposition

photo sensitive material called Photoresist (PR). A series of chemical treatments then either engraves the exposure pattern into the material or enables deposition of a new material in the desired pattern upon the material underneath the photoresist. There are several steps that needs to be done to do the photolithography and they include cleaning, pre-baking, spinning the photoresist, soft-baking, exposure and development etc. The steps associated with photolithography are shown in Fig. A.2.

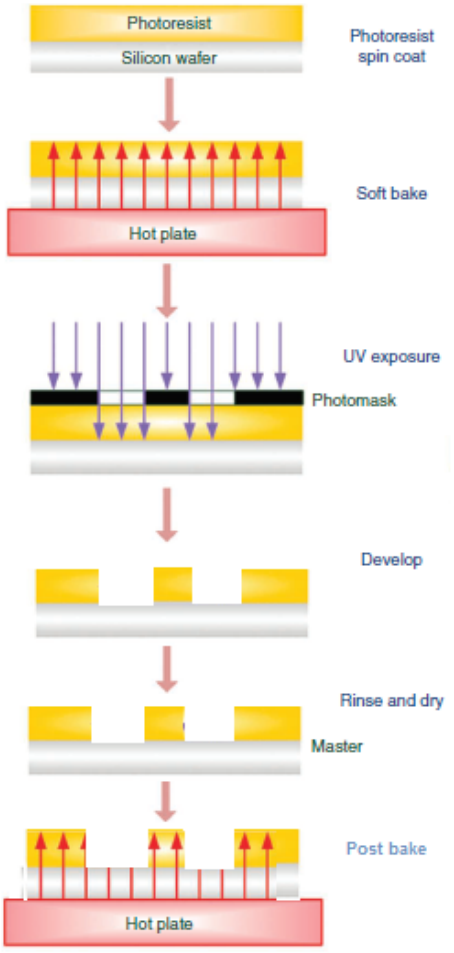


Figure A.2. Different steps of the photolithography process.

Cleaning is an essential step to remove any particle or debris from wafer surface. We typically use solvent cleaning method that includes Acetone, Methanol, Isopropanol and De-Ionized water. But sometimes acid cleaning needs to be done if we cannot remove all

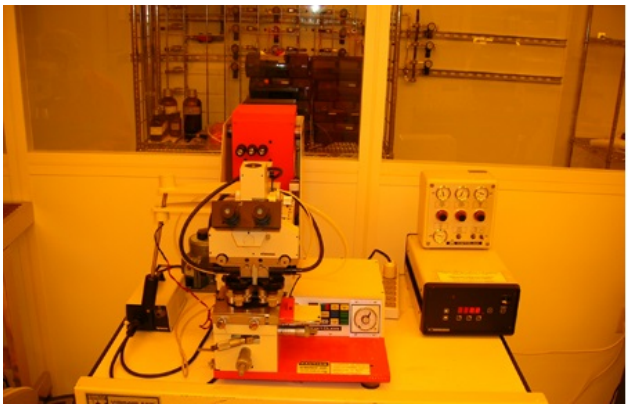
particles by solvent cleaning or if the wafer is very dirty. The pre-bake is to remove all the solvent molecule before spinning to remove any moisture from wafer surface. the spinning is done in a spinner and the spin-curve is followed to deposit a certain thickness of a particular photoresist (PR). Soft-baking is done on hotplates to drive out excess solvent after spinning and to improve adhesion with the surface of the wafer. The exposure is the most critical step of photolithography in which the PR either melts (Negative PR) or gets hardened (Positive PR) when it is exposed to the UV-ray. Thus the pattern of the mask is transferred to the wafer surface. Finally the development removes all the unwanted part of the photoresist after exposure.

A.3 Etching

Etching is a process to chemically remove some part or layer from the surface of a wafer. It is a very important process and we have to do it several times during the fabrication process. During the etching process, some selective part of the wafer is protected from the etchant by a "masking" material which resists etching. In most of the cases, the masking material is a photoresist which is patterned by using photolithography.

There are two distinct type of etching method, one is called west chemical etching and the other is dry plasma based etching. We use the later, which is also called Reactive ion etching (RIE). We use different kind of gas mixtures to etch different kind of materials. For example, to etch Silicon we use Chlorine (Cl_2) or Tetrafluoromethane (CF_4) gas along with Sulfur hexafluoride (SF_6) and for etching Silicon Nitride and Silicon Dioxide, we use trifluoromethane (CHF_3) gas along with Sulfur hexafluoride (SF_6) etc. Some of the etching tools that we use are shown in Fig. A.4.

(a) Spin coater system



(b) SUSS Mjb3 aligner

(c) SUSS MA6 aligner

Figure A.3. Different tools used in the photolithography process (a) Spin coater by which a wafer surface is coated with photoresist (b) SUSS mjb3 optical aligner system, by which sample or wafer is aligned and exposed (c) SUSS MA6 optical aligner, an improved version of mjb3, but performs the same task of alignment and exposure.

(a) STS ASE Etcher

(b) Panasonic E620 Etcher

Figure A.4. Different tools for performing etching process. (a) STS ASE Silicon etcher (b) Panasonic E620 etcher

A.4 Electron-Beam (E-beam) Lithography

Electron beam or E-beam lithography is a process of transferring a pattern to wafer similar to photolithography except the fact that in this case, the pattern is transferred by exposing the wafer to high voltage e-beam instead of UV rays and special e-beam resist is used instead of photoresist. It is a direct writing technique and it uses an accelerated beam of electrons to pattern features with resolution down to sub-10nm. This lithography process is maskless. It has high resolution and low throughput. It is used to create very small structures in the resist that can subsequently be transferred to the substrate material by etching or depositing other materials after development.

An Electron beam lithography system uses hardware similar to a scanning electron microscope (SEM) to guide a nanometer sized focused beam of electrons to form a latent image in a layer of resist. The result of this exposure is to render the resist either more soluble (positive resist) or less soluble (negative resist) in an appropriate developer solution. The resulting pattern is then transferred via etching or by depositing other materials.

Electron beam lithography tools have a certain maximum area that it can write for a fixed stage position know as Write Field. Typically, they range from a few 10s of µms to 1-2 mms. If the pattern to be exposed is more than the size of the write field, the electron beam is blanked, the stage moves by a distance of 1 write field and the writing continues. To avoid discontinuities or overlaps between write fields (known as field stitching errors), an electron beam lithography system has a laser interferometry stage position system that allows stitching of fields with nanometer scale precision. Fig. A.5 shows an example of stitching error while writing.

During the writing process, electron scatters within the resist and the from the substrate resulting in undesired exposures of the resist in regions adjacent to the primary incident beam. This effect is known as the "Proximity Effect" in electron beam lithography. Due to proximity effects, corners in the desired patterns are rounded, gap spacings and linewidths

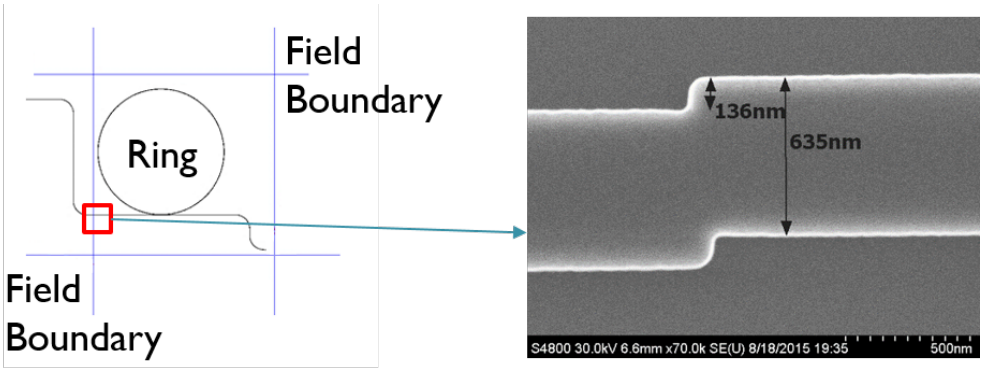


Figure A.5. An example of stitching error while writing a waveguide that crosses two field lines between adjacent fields in the e-beam system.

are modified, and certain features may even merge together or disappear completely. This can be corrected using Proximity Error Correction (PEC) technique available in some developed E-beam machines. Instead of using the constant dose, which refers to number of electrons per unit area of exposure, PEC distributes the dose among various regions of the structure to correct the errors.

B. EDGE POLISHING PROCESS

The details of the edge polishing process for Silicon Nitride Microresonators is discussed here. The process include the following steps:

1. Footer Loading process
2. Sample Loading process
3. Polishing the sample
4. Taking off the sample from sample holder
5. Cleaning the sample

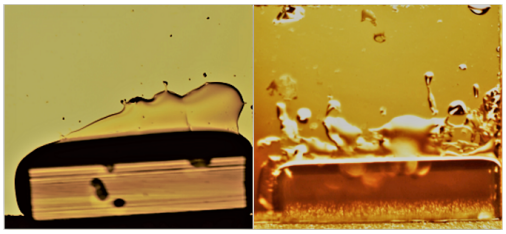
All the steps were discussed in brief in chapter 6. Here the details of each step are discussed.

B.1 Loading the Footer using Epoxy

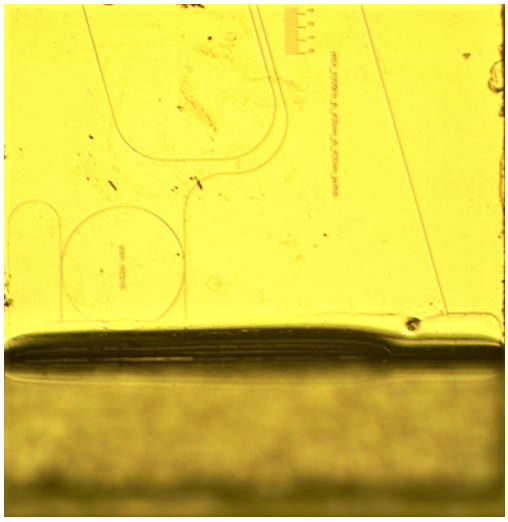
The first step of the polishing process is placing the footer on top of the sample to protect the polishing edge and provide better mechanical stability while polishing the samples. This process may seem pretty easy, but the truth is it is a very complicated process. There are several reasons behind that statement.

Firstly, because the footer alignment is very important for polishing. If the footer is misaligned, that may have an impact while polishing. So it is important to make sure that the footer is exactly or very close to parallel to the edge that needs to be polished. To make better alignment, the sample holder was used as a reference.Both the sample and the footer was pushed against it to make them parallel.

Secondly, The footer itself is a very small chuck of silicon (2mm x 0.5 mm x 0.5 mm). Handling such small piece with tweezer was very difficult. The vacuum suction pumps were tried , but again with such small area, the vacuum cannot work strongly. So proper care was necessary to hold the footer and to place it on top of the sample.



(a) Bad epoxy control



(b) Good Epoxy control

Figure B.1. (a) Bad Epoxy control, epoxy spread over the sample (b) Good epoxy control with good alignment

Finally, the epoxy control was also important. Too much epoxy on top of the sample will cover everything and the footer will slide on top as shown in figure B.1. So epoxy was controlled close to the polishing edge using an optical fiber tip.

For loading the footer, the first step is to choose the proper edge that needs to be polished. It is important to note that the handing of the sample is very important in this stage because it is very easy to damage the edges while handling the sample in this stage. Then using the optical fiber tip epoxy is spread on the sample near that edge where footer would be located. Then the footer is placed there using a tweezer and initial alignment is done by bare eyes using the tweezer. the final alignment check is done by pushing both the sample and the footer together against the sample holder and adjusting the footer location using the tweezer. Once the alignment looks good, UV ray is used for initial curing of the epoxy. Final curing is done by putting the sample on hotplate at 130 degree for about an hour. The whole footer loading process can be summarized by the flow chart shown in Fig B.2.

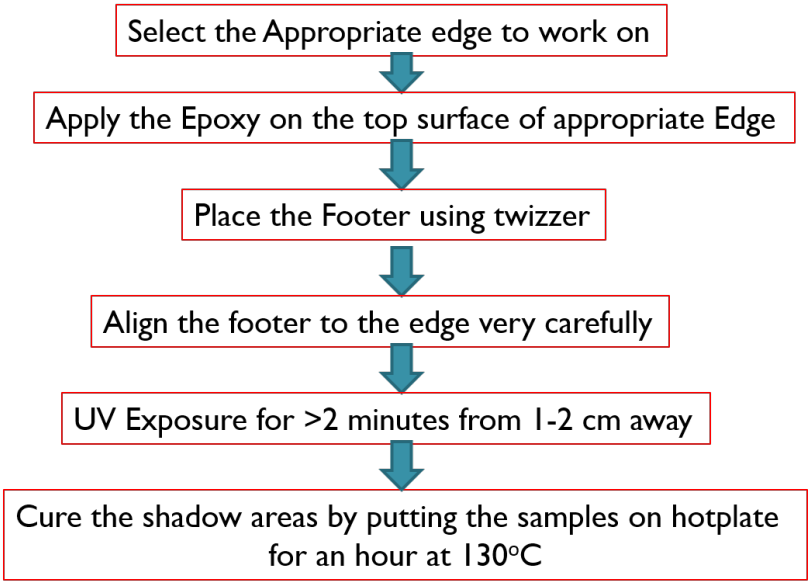


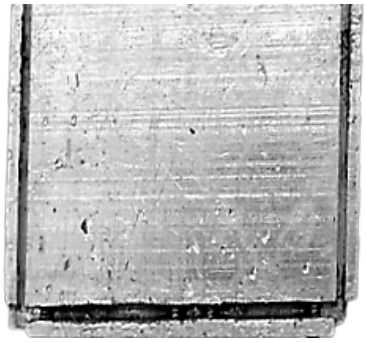
Figure B.2. The flowchart of footer loading process for Polishing the sample

B.2 Loading the Sample on Sample Holder

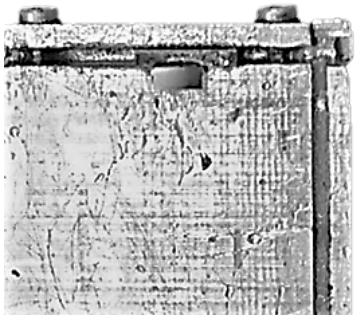
This is the most critical and the longest among all the steps of the polishing process. The quality of polishing depends how well the sample is loaded on the sample holder. The initial sample holder was designed with a rectangular block and the initial plan was to hold the sample around that holder using crystal bond. Nevertheless, the samples fell off easily during the polishing process causing catastrophic damages. Then the modified holder was designed with some grooves all around. The samples can go inside the groove, which can be adjusted by some screws to hold the sample during the polishing process. However, that also had some problems since the screws were not very good ways to hold the sample. Without sufficient pressure, the samples would move during the process. With stronger pressure, the sample may break. So the crystalbond was used to glue the sample into the grooves and prevent these issues.

Since the sample goes inside the groove, the pressure during the polishing process was causing damaged to the opposite edge and therefore the polishing was not successful.

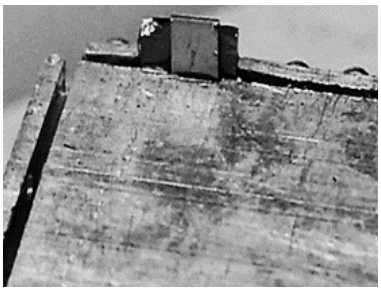
(a) Customized Sample Holder



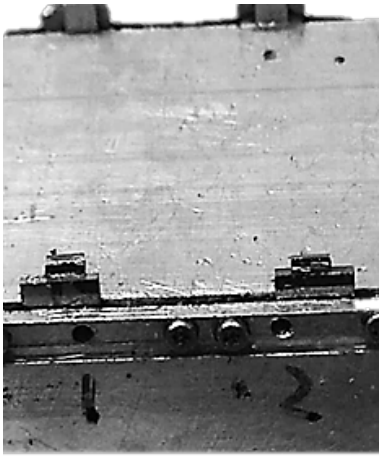
(b) The groove on sample holder



(c) The sample on the groove



(d) Use of sacrificial Si pieces



(e) Final arrangement

(f) Alignment check

Figure B.3. Sample holder and sample loading process

Finally, the idea of using sacrificial Silicon samples, which are of the same size as the sample, came up which effectively solved these issues. Now, the sacrificial Silicon sample goes into the groove and the sample is attached to the extended part of it that comes out of the groove using crystalbond. Also for keeping the same uniform height during the polishing process, three other dummy samples were inserted into the groove so that the system gets some kind of balance. For alignment purpose, a small glass plate was used to make sure all samples are of the same height.

To load the sample, first the sample holder is put on a hotplate around 250 degree Celsius. Then the sacrificial Silicon samples go into the groove. The dummy samples are loaded first and then the main sample is glued to the Silicon pieces using the crystalbond. The initial alignment check is done by bare eyes. Then the sample holder is submerged into water to cool down a little. The sample holder is then taken out to check the final alignment using a small glass plate. If everything is good, it goes to the polishing. If the alignment is not right, everything is repeated again until the alignment seems fine. It is worth mentioning that the alignment does not necessarily have to be perfect, but the better alignment ensures better polishing. The whole process can be summarized by the following flowchart shown in Fig. B.4

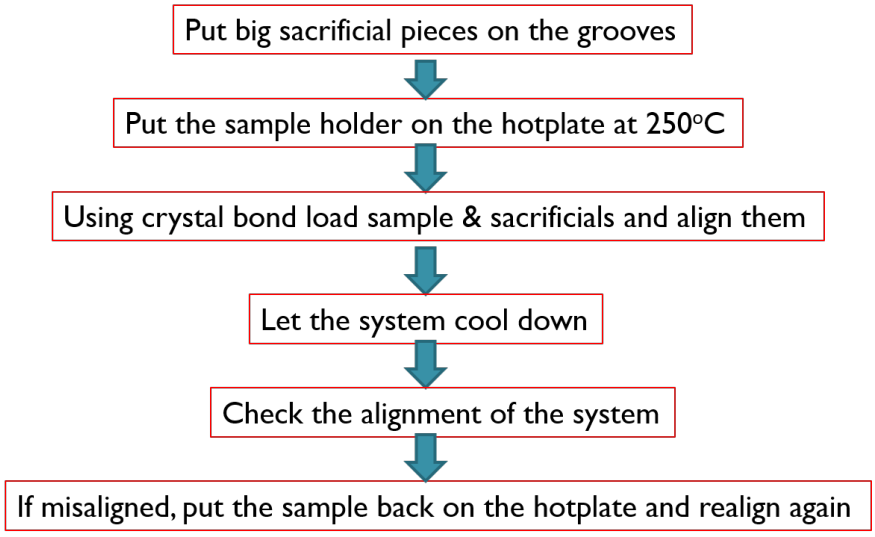


Figure B.4. The flowchart of all the steps during sample loading process

B.3 Polishing the Sample

The actual polishing was done on diamond grit papers starting from a large grit size and going down to finer and finer grits. The polishing grits were obtained from TedPella Inc. and ThorLabs Inc. The largest grit used in this process was 30μm. Then 16μm, 6μm, 3μm, 1μm, 500 nm and 20 nm grit papers were used. The amount of pressure and speed were important during the polishing process. Since circular motion was not possible, a zigzag pattern was followed during the polishing process for better uniformity. The polished surfaces were observed under the microscope after each grit paper to optimize the whole process. However, the actual polishing time was actually very small, ranging from a few seconds to tens of seconds in each grit paper.

The actual polishing time varied from sample to sample, but usually the whole polishing process is finished within 5 minutes. In fact, the initial preparation for polishing usually takes more time. But once everything was set for polishing, it was a very quick process to polish the samples. To hold the diamond grit papers, a glass plate was used and the grit papers were taped on top the glass plate before polishing.

During the polishing process, a very important thing is the use of lubricant to remove debris created from the polishing process and make polishing process uniform. In this case, DI water was used as lubricant. After polishing in each grit paper, the sample was rinsed with DI water and blow dried by nitrogen gun before moving to the next grit paper.The impact of the polishing is shown in Fig. B.5, where the polished edge was observed under the microscope after each grit paper. The gradual improvement is clearly observed as the sample moved from coarse to finer grits.

B.4 Taking the Sample off the Sample Holder

Despite being the easiest step of the polishing process, proper care is necessary in this step. After the polishing is complete and the edge looks good, the sample is taken off the sample holder. To do so, the first thing that is necessary is to melt the crystalbond by

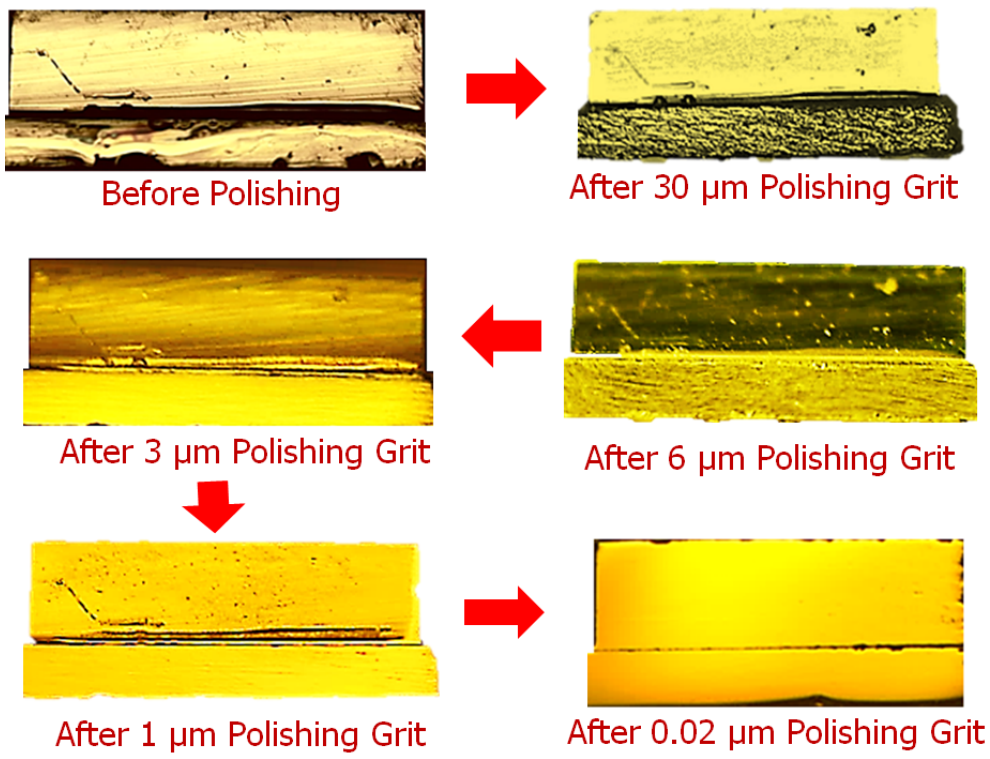


Figure B.5. The effect of polishing on the edge. Starting from 30 μm grit and going down to 20nm grit. Gradual improvement is noticeable as grit size goes from coarse grits to finer grits

which the sample was attached. A hotplate is used to do so and the sample is placed there at appropriate temperature (anything above 200 degree Celsius is fine). After a few minutes when the crystalbond starts to melt, the sample is carefully taken out from the sample holder. After that the sample holder and the sample is submerged in a bowl of DI water so that they can cool down. After a few minutes they are taken out of the water and blow dried with nitrogen gun.

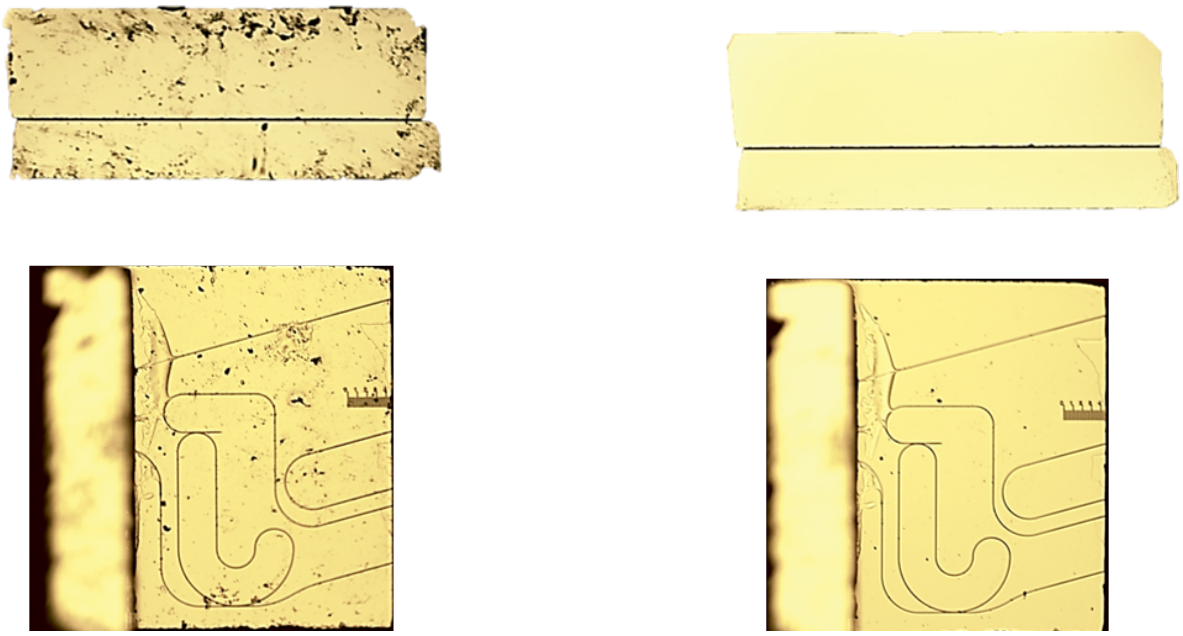
Several precautions are necessary in this step: Firstly, the sample holder usually is hot and there is a chance of burning if the user touches it. So proper thermal insulation or care is necessary to handle it. Secondly, the sample must be handled very carefully since touching edges using the tweezer can damage the sample. In addition, the samples were very small, so there is always chances of dropping the sample. In order to avoid them, a reverse

cup tweezer was used, which gave better handling option and hold the sample strongly to withstand those.

B.5 Cleaning the Sample with Appropriate Solvent

This is the last step of the polishing process and it is important too because the sample gets very dirty during the polishing process. The debris created from the polishing process and crystalbond residues are not removed by the lubricant properly, which can cause some problems. Sometimes they can go to the edge and cover the waveguides through which light propagates, which is very bad. Also, they sometime cover the entire top surface making it difficult to do any alignments later. Therefore, it is necessary to remove them after the polishing process.

To clean the sample, the first step is using crystalbond 509 remover. This is obtained from the company from which the crystalbond was ordered and it was a very effective way to remove crystalbond residues from the top and edge of the sample. Since there was no metal on the sample, ultrasonic cleaning was performed for 3-5 minutes. After that, the sample was cleaned using cloronox solution for a few seconds. Finally, the sample was rinsed with DI water and blow dried using a nitrogen gun. After performing these steps, a visual inspection was done. In case the sample still had some crystalbond residues, the same process was repeated until most of the crystalbond is gone. Finally, the sample is blow dried well with a nitrogen gun and stored in a separate carrier box with protected films for further testing and investigation. The effect of cleaning the sample is shown in Fig B.6:



(a) Before cleaning (b) After cleaning

Figure B.6. Sample cleaning after the polishing process

C. MICROHEATER FABRICATION PROCESS

The complete microheater fabrication process can be described by 3 major fabrication steps: Photolithography, Metal deposition and Lift-off as shown in Fig.C.1. These steps are described in the following subsections with necessary details and pictures.

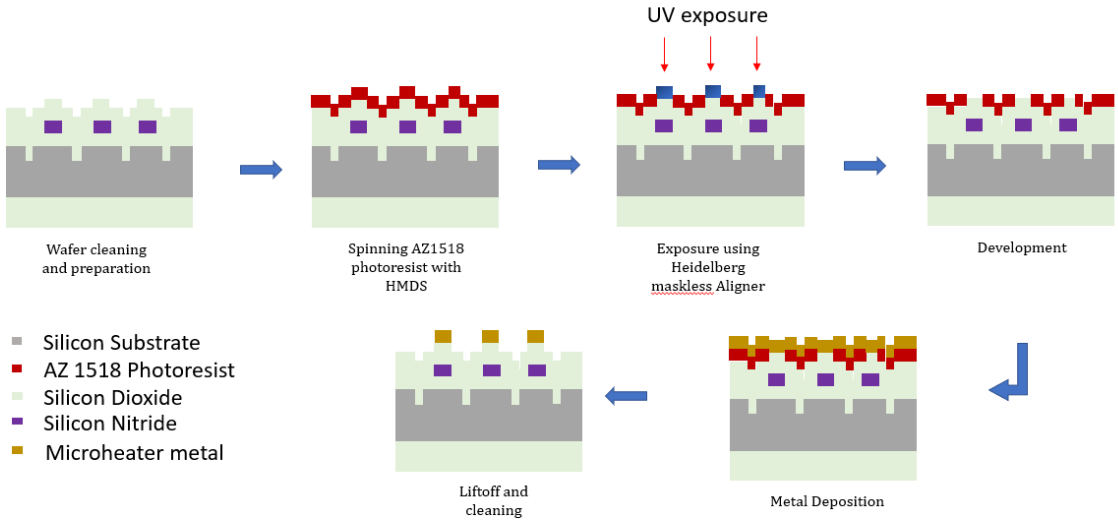


Figure C.1. Photolithography steps in microheater fabrication

C.1 Microheater photolithography

Photolithography is the first step in microheater fabrication. In Birck nanotechnology center at Purdue University, we have two different ways of performing this step. We can do it with traditional photolithography process with physical masks and contact aligners or we can do it with a maskless lithography process tool named Heidelberg MLA150. We chose the latter for several reasons.

Firstly, the microheater fabrication process is not a fixed layout process. In every heater fabrication, due to the design changes, we have to fabricate microheaters with different sizes and shapes. With traditional photolithography process, it is expensive and time consuming

(a) SUSS MA6

(b) Heidelberg Maskless MLA150

Figure C.2. The photolithography tools available for microheater fabrication: a) Traditional photolithography tool SUSS MA6 b) Heidelberg Maskless Aligner MLA150.

process to make physical masks every single time to do that lithography. Also sometimes we had to order masks from outside vendors and that can cause delay in our whole fabrication process. Since maskless photolithography is based on projection and direct writing, it is quick and any design changes can be quickly addressed by changing design files for writing.

Besides, the alignment process in maskless lithography system is very good and it can be done quite easily without large alignment error. Heidelberg uses some cross shaped alignment marks for alignment and those marks can be etched or written on wafer level and can be detected quite easily by Heidelberg's system. On the other hand, in traditional lithography process, we need to do alignments by eye and judgement through a microscope. Therefore, Heidelberg can go down to a few hundreds nm of alignment error in comparison to several micron alignment error from traditional photolithography tools. Since microheater lithography requires good alignment, Heidelberg was the best choice for us.

C.2 Photolithograpy steps

The photolithography steps during the microheater fabrication are described below:

- Wafer cleaning and preparation: We start the heater lithography process by doing some traditional cleaning process. These cleaning steps includes RCA cleaning (without HF dip step, as we have Silicon Dioxide upper cladding), Piranha cleaning and/or solvent cleaning consisting of soaking into Acetone, Methanol and IPA solutions. After cleaning the wafer it is important to rinse it with DI water and blow dry with Nitrogen gun.

- Pre-baking to remove solvent: After cleaning the wafer we put the wafer on hotplate at 180°C for 5-10 minutes to drive away the solvents from wafer surface for better adhesion of the photoresist.

- Spinning HMDS and photoresist: After baking the wafer sufficiently we move to the spinning step. It consists of 2 steps: the first step includes the spinning of an adhesive

Figure C.3. After Heidelberg lithography and good alignment of heater layout with respect of our ring resonators.

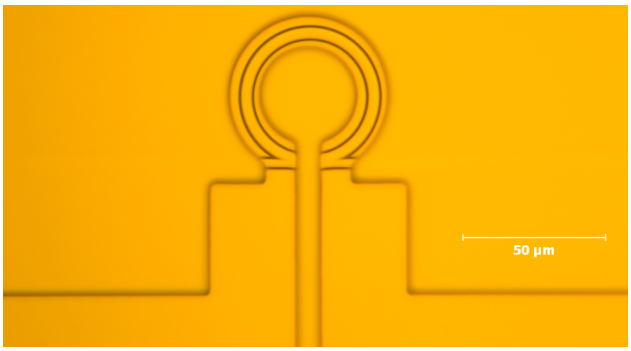
chemical name HMDS (Hexamethyldisilazane) and then the photoresist (AZ1518). Both HMDS and AZ1518 were spun at 4000 rpm for 60s with a ramp of 1000 rpm/s.

- Soft baking: After spinning, the wafer is baked at 120°C for 3 minutes.
- Exposure: The exposure is performed using Heidelberg MLA150 maskless aligner tool after loading the wafer and doing necessary alignments. 300 mJ/cm^2 dose were chosen for exposure after doing an initial dosetest.
- Development: After exposure, the wafer was developed in MF-26 solution for 35-40 seconds and then rinsed with water and blew dry with nitrogen gun. Finally the wafer was inspected under the microscope to check alignment.

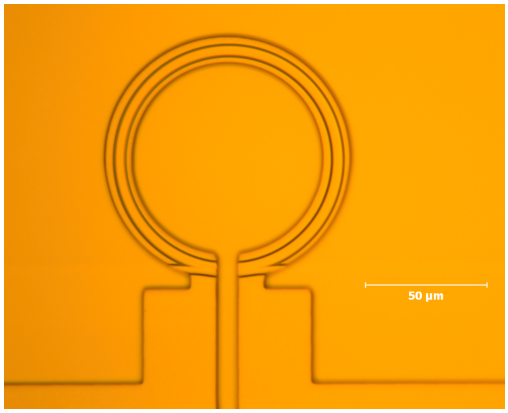
Some examples of how it looks like after photolithography steps are shown in Fig C.3.

C.3 Metal Deposition

The metal deposition was done using E-beam evaporators. There are several e-beam evaporators at Birck Nanotechnology center of Purdue University namely CHA e-beam evaporator, Lesker e-beam evaporators, Leybold e-beam evaporator etc.



(a) 1 THz Device



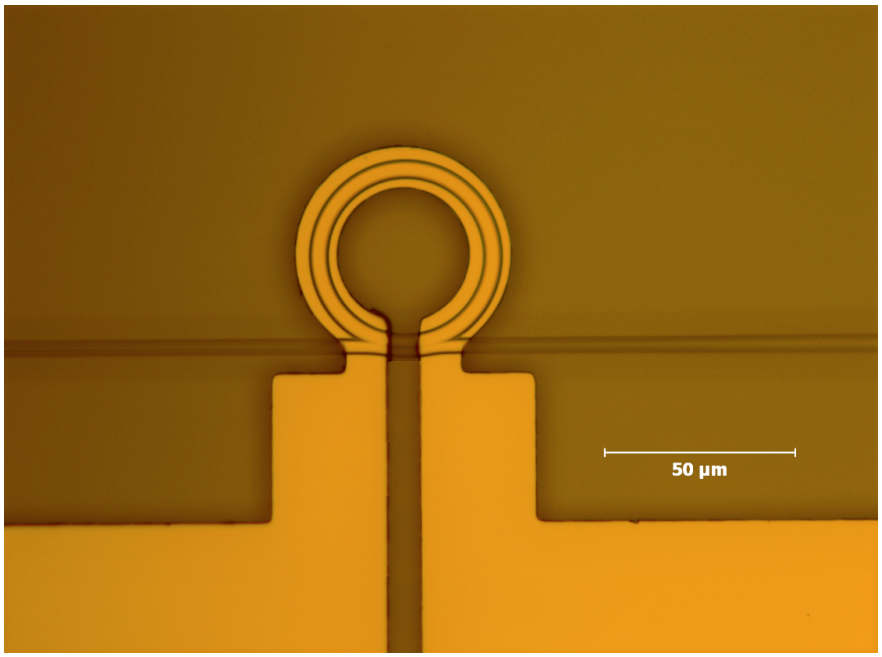
(b) 500 GHz device

Figure C.4. Microscopic images of the devices after metal deposition

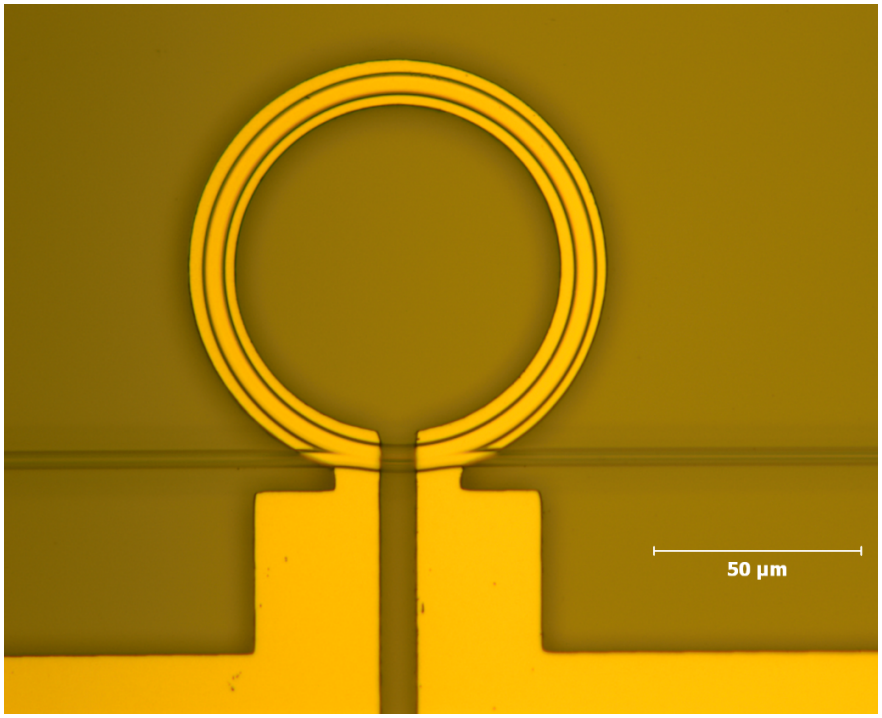
Since we were depositing metals on top of oxide, we needed another thin metal layer for better adhesion. Titanium worked really well for all of them. We didn't have any problem when we were depositing Titatnium only as heater, but for Gold and Platinum we needed a thin Ti layer (20-50nm). The deposition was done at a slow rate of 2A°/sec. We tried different heater designs for better heater efficiency and stability. When the heater thickness was over 500nm, we divided it into two step deposition. Some examples of how it looks like after metal deposition step is shown in fig. C.4.

C.4 Liftoff

After metal deposition, we put our wafer in remover PG solution overnight (6-8 hours) at 80°C hotplate covering the entire beaker with aluminum foil. The remover PG solution reacts with the photoresist and liftoff all the metals in contact with it. After taking out the wafer, we rinse it with IPA solution and put it into a new fresh solution of remover PG. Finally, we rinse again with IPA, rinse with DI water and finally blow dry with a nitrogen gun. Some examples of how it looks like after metal deposition step is shown in fig. C.5.



(a) 1 THz Device



(b) 500 GHz device

Figure C.5. Microscopic images of the devices after liftoff process

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