TWO-DIMENSIONAL NANO-TRANSISTORS FOR STEEP-SLOPE DEVICES AND HARDWARE SECURITY

by

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献给我挚爱的父母

To my beloved parents

吴英彪和姚润芬

Yingbiao Wu & Runfen Yao

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I_D	drain current
I_{ON}	ON-state current
I_{OFF}	OFF-state current
V_G, V_{GS}	gate voltage
V_D, V_{DS}	drain voltage
$\mathrm{V_{DD}}$	supply voltage
GND	ground
V_{th}	threshold voltage
E_g	bandgap
E_F	Fermi level
E_C	conduction band minimum
E_V	valence band maximum
m^*	effective mass
m_0	free electron mass
λ	screening length
t_{ox}	oxide thickness
t_{body}	body thickness
C_q	quantum capacitance
W	channel width
L_g, L_{ch}	gate/channel length
Φ_{SB}	Schottky-barrier height

ABBREVIATIONS

MOSFET	metal-oxide-semiconductor field-effect transistor
SB-FET	Schottky-barrier field-effect ttransistor
TFET	tunneling field-effect transistor
NC-FET	negative capacitance field-effect transistor
CMOS	complementary metal-oxide semiconductor
IC	integrated circuit
SS	subthreshold swing, or inverse subthreshold slope
BP	black phosphorus
TMD	transition metal dichalcogenides
1D	one-dimensional
2D	two-dimensional
MoS_2	molybdenum disulfide
WSe_2	tungsten diselenide
WS_2	tungsten disulfide
CNT	carbon nanotube
SiO_2	silicon dioxide
HfO_2	hafnium oxide
Al_2O_3	aluminum oxide
Al	aluminum
Au	gold
Cr	chromium
Ni	nickel
Ti	titanium
Si	silicon
mV/dec	milivolts per decade
eV	electron volt
μA/μm	micro ampere per micrometer
ALD	atomic layer deposition

SEM	scanning electron microscopy
TEM	transmission electron microscopy
STEM	scanning transmission electron microscopy
FIB	focused ion beam
AFM	atomic force microscopy
DIBT	drain-induced barrier thinning
BTBT	band-to-band tunneling
NDR	negative differential resistance
EOT	equivalent oxide thickness
WKB	Wentzel-Kramer-Brillouin
TG	top-gate
BG	back-gate, or bottom-gate
DG	double-gate
ADG	asymmetric double-gate

ABSTRACT

Since the discovery of graphene, two-dimensional (2D) materials have attracted broad interests for transistor applications due to their atomically thin nature. This thesis studies nano-transistors based on 2D materials for several novel applications, including tunneling transistors for low-power electronics and reconfigurable transistors for hardware security.

The first part of the thesis focuses on tunneling field-effect transistors (TFETs). Since the current injection in a conventional MOSFET depends on thermionic injection over a gate-controlled barrier, the subthreshold swing (SS) of MOSFET is fundamentally limited to 60 mV/dec at room temperature, hindering the supply voltage scaling of integrated circuits (ICs). Utilizing band-to-band tunneling (BTBT) as current injection mechanism, TFETs overcome the SS limit by filtering out the Fermi tail in the source and achieve steep-slope switching. However, existing demonstrations of TFETs are plagued by low on-currents and degraded SS, largely due to the large tunneling distances caused by non-scaled body thicknesses, making 2D materials a promising candidate as channel materials for TFETs. In this thesis, we demonstrate a prototype TFET based on black phosphorus (BP) adopting electrostatic doping that is tuned by multiple top-gates, which allows the device to be reconfigured into multiple operation modes. The band-to-band tunneling mechanism is further confirmed by source-doping-dependent and temperature-dependent measurements, and the performance improvement of BP TFETs with further body and oxide thicknesses scaling is projected by atomistic simulation. In addition, a vertical BP TFET with a large tunneling area is also demonstrated, and negative differential resistance (NDR) is observed in the device.

The second part of the thesis focuses on reconfigurable nano-transistors with tunable p- and n-type operations and the implementation of hardware security based on such transistors. Polymorphic gate has been proposed as a hardware security primitive to protect the intellectual property of ICs from reverse engineering, and its operation requires transistors that can be reconfigured between p-type and n-type. However, a traditional CMOS transistor relies on substitutional doping, and thus its polarity cannot be altered after the fabrication. By contrast, 2D nano-transistors can attain both electron and hole injections. In this thesis,

we review the Schottky-barrier injection in 2D transistors and demonstrate the feasibility of achieving complementary p-type and n-type transistors using BP as channel material by adopting metal contacts with different work functions. In this design, however, the discrepancy in the p-FET and n-FET device structures makes it unsuitable for reconfigurable transistors. Therefore, we continue to modify the device design to enable reconfigurable p-type and n-type operations in the same BP transistor. Finally, a NAND/NOR polymorphic gate is experimentally demonstrated based on the reconfigurable BP transistors, showing the feasibility of using 2D materials to enable hardware security.

In the last part, we demonstrate an artificial sub-60 mV/dec switching in a metal-insulator-metal-insulator-semiconductor (MIMIS) transistor. Negative capacitance FETs (NC-FETs) have attracted wide interest as promising candidates for steep-slope devices. However, the detailed mechanisms of the observed steep-slope switching are under intense debate. We show that sub-60 mV/dec switching can be observed in a WS_2 transistor with an MIMIS structure – without any ferroelectric component. Using a resistor-capacitor (RC) network model, we show that the observed steep-slope switching can be attributed to the internal gate voltage response to the chosen varying gate voltage scan rates. Our results indicate that the measurement-related artefacts can lead to observation of sub-60 mV/dec switching and that experimentalists need to critically assess their measurement setups.

1. INTRODUCTION

Over the past decades, the continuous scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs), widely known as Moore's Law [1], has been the driving force of the ubiquitous application of integrated circuits (ICs). However, in recent years, several issues, including short-channel effects and slowing down of supply voltage (V_{DD}) scaling, are hindering the continuation of Moore' Law, and the industry and research community are seeking more innovative solutions to these issues. Among these solutions, introducing novel nano-materials, such as two-dimensional (2D) materials, is of particular interest.

Since the debut of graphene in 2004 [2], 2D materials have remained a hot topic in the research community. Notably, after the demonstration of single layer MoS_2 transistors in 2011 [3], 2D semiconducting materials, such as transition metal dichalcogenides (TMDs) [3]–[6], black phosphorus [7]–[9] and silicene [10], have been extensively studied for transistor applications, since they have the potential to become the ultimate solution to the scaling problem, thanks to their atomically thin nature. While significant efforts have been spent in applying 2D materials in traditional MOSFET to continue the scaling trend, which is known as *More Moore*, there also have been efforts in seeking novel applications leveraging the unique properties of the new materials, known as *More than Moore*, or *Beyond-CMOS*. In this thesis, we study two-dimensional material-based nano-transistors for such novel applications, including low-power tunneling field-effect transistors (TFETs) and reconfigurable transistors for hardware security.

1.1 Two-dimensional semiconducting materials

Since the discovery of graphene, the idea of using graphene as channel material in transistor applications has attracted extensive studies, due to its atomically thin body thickness and ultra-high electron mobility ($\sim$ 15000 $cm^2/V \cdot s$) [11]. However, since graphene is a gapless semi-metal, the on-off ratios of graphene field-effect transistors (FETs) are typically less than 100, which limits its application in digital integrated circuits (ICs). Therefore, 2D semiconducting materials with bandgaps, such as transition metal dichalcogenides (TMDs) and black phosphorus (BP), are more attractive for transistor applications. Fig. 1.1 shows

the atomic structures of two representative 2D materials, molybdenum disulfide [MoS_2, Fig. 1.1(a)] and BP [Fig. 1.1(b)]. These 2D materials are composed of stacks of atomic layers that are held together by van der Waals force, and each layer is less than 1 nm thick. The atomically thin body thicknesses make 2D semiconductors attractive for applications in ultra-scaled transistors and continuing Moore's Law.

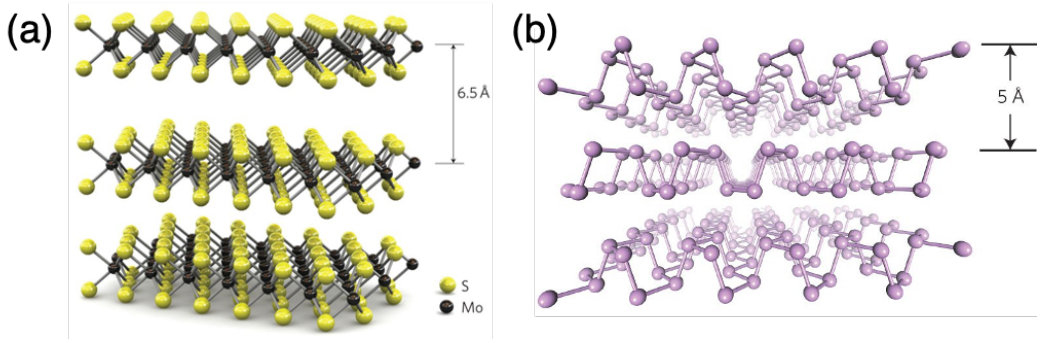


Figure 1.1. Illustration of atomic structure of 2D materials. (a) Molybdenum disulfide (MoS_2). (b) Black phosphorus (BP). Reprinted with permission from B. Radisavljevic *et al.*, "Single-layer MoS_2 transistors", *Nature Nanotechnology* **6**, 147-150 (2011) & L. Li *et al.* "Black phosphorus field-effect transistors", *Nature Nanotechnology* **9**, 372-377 (2014). Copyright (2011 & 2014) Springer Nature.

Compared with replacing Si with 2D materials to allow aggressive scaling of MOSFETs and continue Moore's Law, it is more appealing to study novel transistor applications based on the unique properties of 2D materials as a complement to conventional Si CMOS transistors. In the next few sections, we continue to discuss the rationale of incorporating 2D materials in nano-transistors to enable such novel applications, including tunneling field-effect transistors for low-power devices and reconfigurable transistors for hardware security.

1.2 Tunneling field-effect transistors

Over the past decades, integrated circuits are seeing more and more applications due to the continuous improvement of performance and reduction of cost, both of which are enabled by Moore's Law. The driving force behind Moore's Law is the the continuous scaling of MOSFETs, following the Dennard scaling [12], or constant-field scaling. Dennard

scaling states that for each new process node of MOSFETs, the gate length and width, power supply voltage V_{DD} and gate oxide thickness t_{ox} scale by 0.7×. Such scaling rule ensures that the power density of a chip is kept constant for each generation. However, in recent years, Dennard scaling has stopped functioning as a result of the slowing down of V_{DD} scaling, which is due to a fundamental limit of conventional MOSFET, and the power consumption of ICs has becomes a major issue ever since. To understand the issue, we need to study the operation principle of a MOSFET.

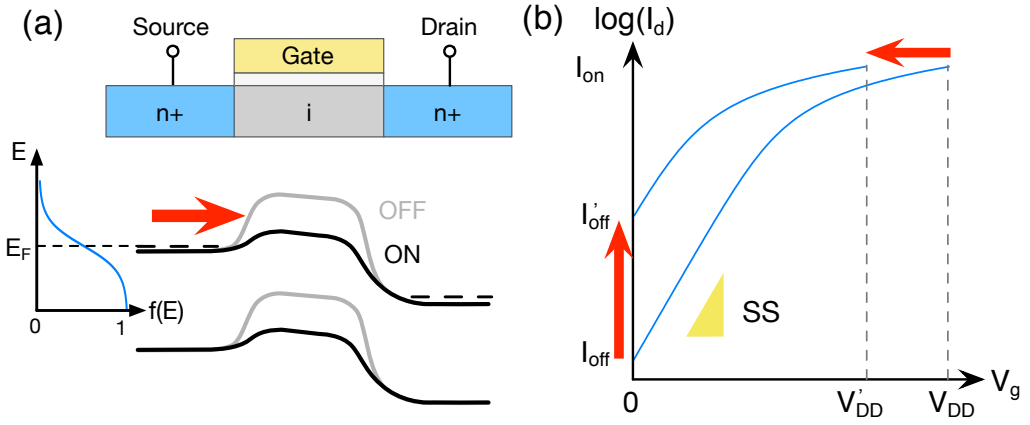


Figure 1.2. (a) Schematic and band diagram of a MOSFET, showing the thermionic emission. (b) The impact of minimum SS on V_{DD} scaling and off-state current.

Fig. 1.2 shows the schematic and the band diagram of an n-type MOSFET. Since the current injection in a conventional MOSFET is governed by thermionic emission over a barrier, the subthreshold swing (SS), *i.e.*, the amount of gate voltage required to change the current by one order of magnitude, is fundamentally limited to at least $\ln(10) \times k_B T/q$, which is ∼60 mV/dec at room temperature [13]–[16]. Because the limitation of SS, further decreasing V_{DD} while maintaining the same on-state current (in order not to affect the clock frequency, or equivalently, the speed of the circuit) would result in an exponential increase of off-state current, as shown in Fig. 1.2(b). Since a large-scale digital IC require low leakage currents of its component devices in order not to burn itself, such exponential increase is intolerable. As a result, Dennard scaling has ended and V_{DD} scaling has nearly stopped since ∼2003 [17], and the heat dissipation has become the main limiting factor of the increase of

clock speed and performance of digital circuits. Such issue has been termed as "Boltzmann tyranny", named after the Boltzmann distribution of electrons (or the Boltzmann constant k_B in the formula $\ln(10) \times k_B T/q$)[1]. Therefore, steep-slope devices that overcome the SS limit are highly sought after.

Tunneling field-effect transistors (TFETs) are proposed by J. Appenzeller *et al.* as a steep-slope device in 2004 [13], and in the same paper, a CNT TFET was demonstrated to exhibit a subthreshold swing of 40 mV/dec at 300 K.[2] TFET typically adopts a gated p-i-n structure (or n-i-p for p-type TFET), as shown in Fig. 1.3(a). The injection mechanism of a TFET is band-to-band tunneling (BTBT), instead of thermionic emission in conventional MOSFETs. The key for steep switching in TFETs is that the high energy part of the electron, or the Fermi tail, in the source is filtered out by the tunneling window, indicated by the green shade in Fig. 1.3(b), and thus the injected electrons into the channel are effectively "cooled down" by the band-pass filter [14], allowing an SS below 60 mV/dec. Fig. 1.3(b) shows a comparison of the transfer characteristics of a MOSFET and a TFET. In the ideal case, although the ON-current of a TFET may be lower than a MOSFET at large V_{DD} values due to the finite transmission of BTBT, after scaling to a lower supply voltage V'_{DD}, the ON-current of the TFET can be higher than the MOSFET due to a steeper SS.

In reality, however, most experimental TFETs exhibit low I_{on} values, as illustrated by the dashed red line in Fig. 1.3(b). Even though sub-60 mV/dec may be observed in the transfer characteristics, the corresponding current levels are too low for any practical applications. The reason behind the low currents is mainly due to a small transmission associated with the band-to-band tunneling through the barrier, which can be calculated based on the Wentzel–Kramer–Brillouin (WKB) approximation [27], [28]:

$$T_{BTBT}^{WKB} = \exp\left(\frac{-4\lambda\sqrt{2m^* E_g^3}}{3\hbar(\Delta\Phi + E_g)}\right) \tag{1.1}$$

[1]↑In reality, Fermi-Dirac distribution should be used, yet Maxwell-Boltzmann distribution is a good approximation for the "tail" in the Fermi-Dirac distribution, which is responsible for the off-current in a MOSFET.
[2]↑Before this work, several papers [18]–[26] already proposed the gated p-i-n structure, as some review articles of TFETs pointed out. However, it is worth mentioning that *none* of these early works mentioned the possibility of achieving sub-60 mV/dec operation using the structure – as a matter of fact, most of them were merely intended to propose a gated version of Esaki diode for a tunable NDR.

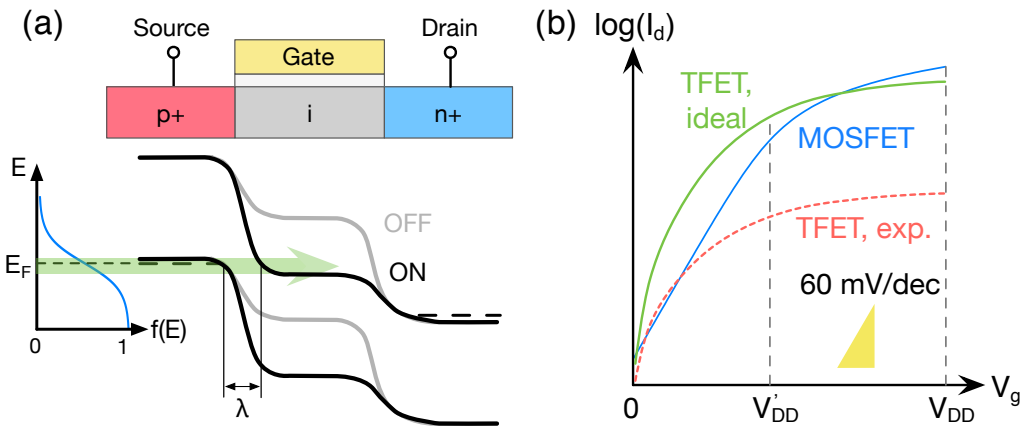


Figure 1.3. (a) Schematic and band diagram of a TFET, showing the band-to-band tunneling current injection path. (b) A comparison of MOSFET and TFET transfer characteristics.

The detailed analysis of the equation will be discussed in Chapter 2 of the thesis. Here, we are only focusing on the screening length λ. The tunneling probability has an exponential dependence on λ, which is in turn proportional to the square root of gate oxide thickness and body thickness, *i.e.*, $\lambda \sim \sqrt{t_{ox} t_{body}}$. Therefore, it is essential to decrease body thickness t_{body} in order to achieve a small λ and a large T_{BTBT}, which in turn leads a high on-current. Due to the atomically thin nature, 2D materials are a natural solution to the scaling problem in TFETs. In this thesis, we discuss the progress on demonstrating a prototype TFET with black phosphorus, an emerging 2D material, as channel material.

1.3 Reconfigurable nano-transistors for hardware security

Hardware security has become a critical design consideration in modern IC industry besides the traditional metrics, such as performance, power consumption and cost. To prevent IP piracy, polymorphic gate [29] has been proposed as one of the hardware security measures that leverage emerging transistor technologies. As an example, Fig. 1.4 shows a NAND/NOR polymorphic gate built with nano-transistors that can be reconfigured between p-FET and n-FET operation modes. By swapping V_{DD} and GND, the pull-up network and the pull-down network can be interchanged, and thus the functionality of the circuit can be transformed between a NAND gate and a NOR gate. Without a prior knowledge to the cir-

cuit design, an extraction of the circuit layout via reverse engineering is unable to distinguish the intended functionality of the circuit. If N of such polymorphic gates are incorporated in an IC design, there are 2^N combinations of possible functions in total, rendering the attacks extremely difficult with brute-force attacks. Such exponential increase ensures the security of the IC design from hardware level.

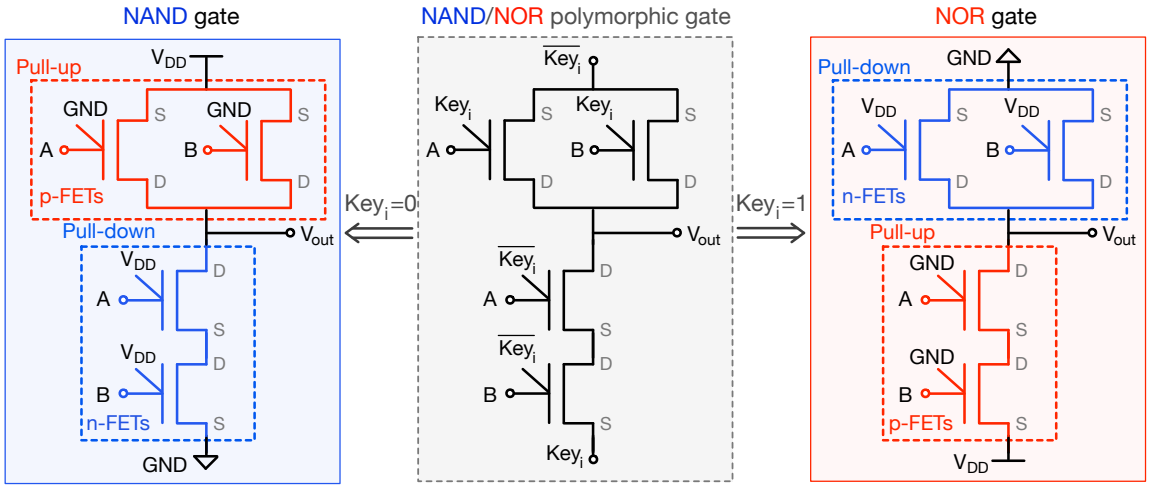


Figure 1.4. Schematic of a NAND/NOR polymorphic gate built with reconfigurable nano-transistors. Adapted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

However, such implementation of the polymorphic gate cannot realized with traditional CMOS transistors, since the operation of CMOS transistors requires p-type or n-type substitutional doping in the source/drain regions for p-FETs and n-FETs, respectively, and as a result it is prohibitive to alter the polarity of a device post-fabrication. By contrast, 2D nano-transistors usually adopt doping-less structures and the current injection is governed by Schottky-barrier injection, of which the carrier type can be tuned by electrostatic doping [5], [8], [30]–[32]. Therefore, it is possible to achieve both electron and hole injection with good electrostatic gating and transparent enough Schottky barriers, both of which are attainable via proper device design. As an example, well-designed black phosphorus transistors exhibit ambipolar characteristics, as shown in Fig. 1.5. By applying a positive or negative gate voltage, either electron or hole can be allowed to be injected into the channel, and thus both p-

and n-branches can be observed in the device. Such operation requires a combination of the unique properties of BP, such as a moderate bandgap and near mid-gap Fermi level pinning from the metal-BP interface [8], [30], as well as an elaborate design of device structure, such as the correct selection of contact metal and a tight gate control ensured by the thin high-κ dielectric and a double-gate structure. Details of the implementation will be discussed in the thesis.

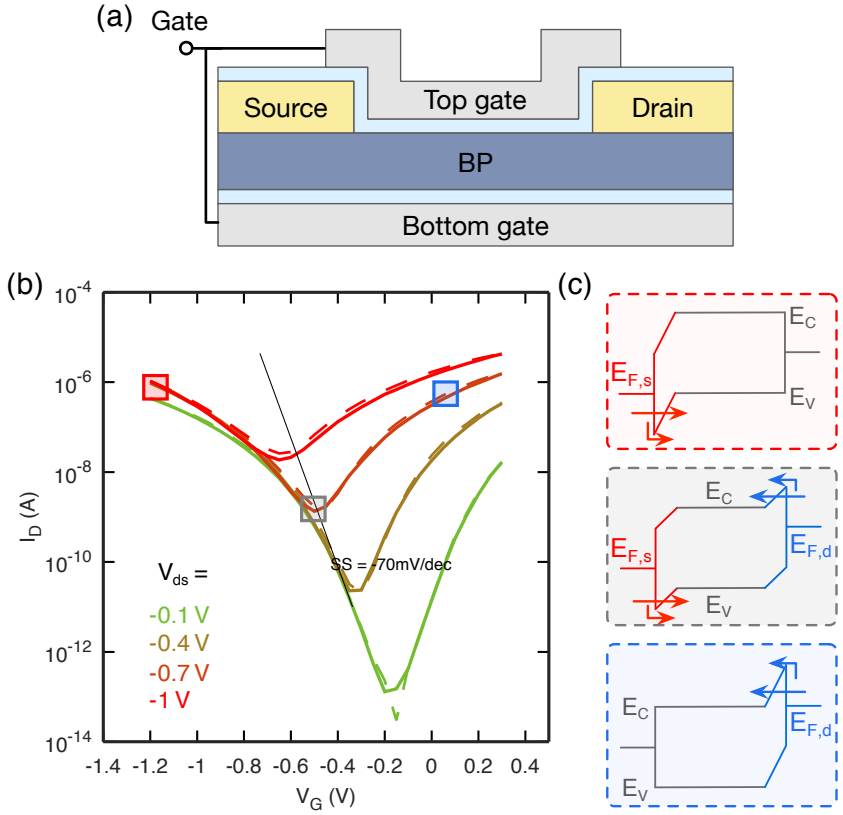


Figure 1.5. An exemplary ambipolar BP transistor. (a) Schematic of an ambipolar BP transistor. (b) Transfer characteristics of the ambipolar BP transistor. Ambipolar characteristics are observed in the device. (c) Band diagrams of the BP ambipolar transistor corresponding to different gate voltages, showing the electron and hole injections. Adapted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

Having discussed the merits of the ambipolar BP transistors, an issue can also be identified from the characteristics shown in Fig. 1.5(b). As drain voltage V_d increases (or decreases

for negative V_d values in a p-FET), the ambipolar injection from the drain is enhanced, leading to an increase in the off-state current. As discussed before, the merit of CMOS transistor is the low off-state current, which allows the integration of millions of devices without burning the chip. Therefore, the degradation of off-state current needs to be solved, and the solution will be discussed in details in the thesis.

1.4 Organization

The organization of the thesis is as follows:

- Chapter 2 discusses BP tunneling field-effect transistors. Starting with a discussion of the unique properties that make BP an ideal candidate as channel materials for TFETs, we continue to demonstrate a prototype BP TFET, in which the electrostatic doping allows for reconfigurable operations between n-type and p-type conduction, as well as between MOSFET and TFET modes. Next, source-doping-dependent and temperature-dependent measurements confirm the band-to-band tunneling mechanism in the device. Finally, atomistic simulation is performed to project the performance improvement of BP TFETs by continue scaling down the body and oxide thicknesses.

- Chapter 3 discusses vertical BP TFETs. We demonstrate a much larger tunneling current in the vertical structure compared with the lateral structure in Chapter 2, due to a larger tunneling area from the vertical overlapping region, and negative differential resistance (NDR) is observed in the vertical device. The vertical BP TFET also exhibits reconfigurable operations, similar to the lateral BP TFET in Chapter 2.

- Chapter 4 discusses achieving CMOS-like devices with 2D materials. We start by reviewing Schottky-barrier injection, the current injection mechanism in 2D nanotransistors. Next, we discuss how to achieve unipolar n-type and p-type characteristics in BP Schottky-barrier FETs via contact work function engineering and optimization of device structure – an asymmetric double-gate structure. Finally, a high performance inverter is demonstrated by connecting the properly designed unipolar n-FET and p-FET.

- Chapter 5 discusses 2D nano-transistors with reconfigurable polarities and their applications in hardware security. We start with an overview of realizing hardware security using polymorphic gate, which requires the use of transistors with reconfigurable polarities. Next, we discuss the necessity of using a small bandgap material such as BP for reconfigurable transistors, and based on the existing results in Chapter 4, we continue to engineer the device structure to achieve reconfigurable operations between unipolar p-type and n-type modes as well as immunity from off-current degradation caused by ambipolar drain injection, and a high performance inverter is demonstrated with the reconfigurable BP FETs. Finally, a hardware security primitive – a NAND/NOR polymorphic gate is demonstrated experimentally, and the robustness of the polymorphic gate against power supply variations is tested using Monte Carlo simulations.

- Chapter 6 discusses artificial sub-60 mV/dec switching in a metal-insulator-metal-insulator-semiconductor (MIMIS) transistor. We show that in a WS_2 transistor with an MIMIS structure, which is similar to a negative capacitance FET (NC-FET) yet without any ferroelectric component, sub-60 mV/dec switching can be observed. Using a resistor-capacitor (RC) network model, we show that the observed steep-slope switching can be attributed to the internal gate voltage response to the chosen varying gate voltage scan rates. Our results indicate that the measurement-related artefacts can lead to observation of sub-60 mV/dec switching and that experimentalists need to critically assess their measurement setups.

2. BLACK PHOSPHORUS TUNNELING FIELD-EFFECT TRANSISTORS

Band-to-band tunneling field-effect transistors (TFETs) have emerged as promising candidates for low-power integration circuits beyond conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) and have been demonstrated to overcome the thermionic limit, that results intrinsically in subthreshold swings of at least 60 mV/dec at room temperature. In this chapter we demonstrate complementary TFETs based on few-layer black phosphorus, in which multiple top gates create electrostatic doping in the source and drain regions. By electrically tuning the doping types and levels in the source and drain regions, the device can be reconfigured to allow for TFET or MOSFET operation and can be tuned to be n-type or p-type. Owing to proper choice of materials and careful engineering of device structures, record high current densities have been achieved in 2D TFETs. Full band atomistic quantum transport simulations of the fabricated devices agree quantitatively with the I–V measurements which gives credibility to the promising simulation results of ultra-scaled phosphorene TFETs. Using atomistic simulations, we project substantial improvements in the performance of the fabricated TFETs when channel thicknesses and oxide thicknesses are scaled down.

2.1 Introduction

In recent years, two-dimensional (2D) semiconducting materials have attracted attention as channel material for next-generation transistors [4], [5], [7], [8], [33]–[38], as the ultra-thin body allows for ideal electrostatic control of the channel potential, addressing problems in conventional devices related to channel length scaling [8], [39]. However, regardless of the actual channel material, in conventional MOSFETs the current flowing below threshold is always determined by thermionic emission over the gate controlled barrier between source and drain, which fundamentally limits the subthreshold swing (SS) to about 60 mV/dec at

room temperature. Among other things, this hinders scaling down the supply voltage and prevents further, urgently needed, reduction in power dissipation. Therefore, apart from new materials for transistor applications in general, novel devices based on alternative switching mechanisms are required to break the thermal limit and to achieve ultra-low-power device operation. Band-to-band tunneling (BTBT) field-effect transistors (TFETs) [13]–[16], [40]–[43] have been proposed and demonstrated as promising candidates for achieving steep-slope devices. Combining this concept with using 2D materials as the active channel in TFETs allows benefitting from the ultra-thin body thickness aspect of 2D, which leads to short tunneling distances. Small tunneling distances in turn result in both high ON-state currents (I_{ON}) and steep SS values [43]–[47].

Various research articles on building TFETs using 2D materials have been published over the last years. Most of this work focused on 2D vertical heterojunctions, such as molybdenum disulfide (MoS_2)/tungsten diselenide (WSe_2) [42], tin diselenide ($SnSe_2$)/BP [48] and $SnSe_2$/WSe_2 [49]. Some [45], [50], [51] studied homojunction TFETs based on WSe_2, a 2D material intensively evaluated for TFET applications [45], [46]. However all these tunneling devices suffer from low current levels. To evaluating the on-current I_{ON} for TFETs, it is instructive to take a look at the transmission probability T, that describes charge transport through the BTBT barrier, based on the Wentzel–Kramer–Brillouin (WKB) approximation [27], [28]:

$$T_{WKB} = \exp\left(\frac{-4\lambda\sqrt{2m^* E_g^3}}{3\hbar(\Delta\Phi + E_g)}\right) \tag{2.1}$$

where E_g is the bandgap, m^* is the effective mass, $\lambda = \sqrt{(\epsilon_{body}/\epsilon_{ox})t_{ox}t_{body}}$ is the screening length, which describes the spatial extent of the tunneling junction, in which t_{ox} and t_{body} are oxide thickness and body thickness respectively, ϵ_{ox} and ϵ_{body} are dielectric constants of oxide and body, respectively, and $\Delta\Phi$ is the energy window of BTBT, *i.e.*, the energy difference between the conduction band edge in the n-type region and the valence band edge in the p-type region. In order to achieve a high transmission probability, E_g and m^* need to be minimized by choosing a suitable material and λ needs to be reduced by improving the electrostatics in the device. TFETs built from WSe_2 exhibit thus unavoidably

low I_{ON}–values, since the large bandgap [52] (1.0 eV to 1.5 eV) and high effective masses [45] (electron effective mass $m_e^* = 0.34\ m_0$, hole effective mass $m_h^* = 0.44\ m_0$) of WSe_2 give rise to a low transmission probability. On the other hand, black phosphorus (BP) as channel material [7], [8], [38], [53]–[57] is characterized by a tunable small bandgap [8], [58], [59] (0.3 eV to 2 eV) and low effective mass [58] (0.15 m_0) and can thus be expected to be a better material choice for high on-current TFET applications [43], [60], [61]. Based on few-layer BP, here we report experimental results on complementary lateral TFET, with BTB tunneling occurring at electrostatically [50], [62], [63] defined p/n (or n/p) homojunctions that can be controlled by means of multiple gates. We call this device a Reconfigurable-Electrostatically-Doped Tunneling Field-Effect Transistor (BP RED-TFET). It is worth noticing that such electrostatically-doped TFETs based on BP and reconfigurable operations have been demonstrated before [61]. In this chapter, we report both n-type and p-type operations in BP TFETs for the first time. In addition, we demonstrate record-high current drive densities and improved room-temperature subthreshold slopes, through an optimized device structure. One of the challenges with 2D materials is a lack of doping scheme. In traditional semiconductors, doping can be introduced by diffusion or ion implantation. In this work, we have overcome this challenge by adopting the multiple-gate design to achieve the p/i/n doping profile as required by a TFET. Although the multiple-gate design complicates the device structure and also makes the circuit design more challenging, for a prototype device it allows more flexible design due to tunable parameters, such as doping concentrations and types in different regions, and ultimately electrostatic doping has the potential to outperform chemical doping [43], [64].

2.2 Device structure and operation principle

Fig. 2.1(a) and 2.1(b) show the schematic and a scanning electron microscopy (SEM) image (false-colored for clarity) of a BP RED-TFET. A few-layer BP flake is located on top of Au source/drain contacts, and two top-gates overlapping with the source and drain electrodes, G1 and G2, can be used to induce the desired electrostatic doping in the source and drain portions (next to the contact electrodes) of the BP, while the middle top-gate

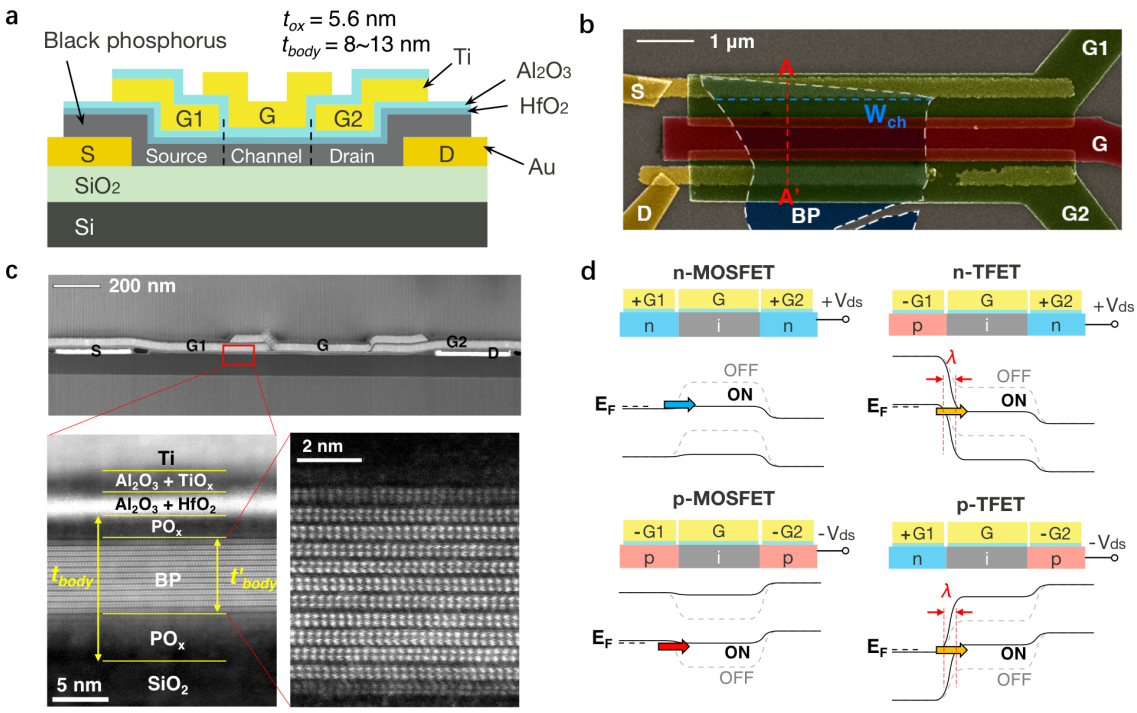


Figure 2.1. Black phosphorus RED-TFET. (a) Schematic of the BP RED-TFET. (b) Representative false-colored SEM image of the BP RED-TFET. Scale bar: 1 μm. (c) Representative cross-section HAADF-STEM image of the BP RED-TFET along A-A' in (b), showing the triple top-gate structure, the interface of BP and gate oxide, and crystal structure of BP. Notice that due to oxide formation on both sides of BP, the real body thickness t'_{body} is smaller than the nominal body thickness t_{body}. (d) Schematic illustration of the bands through the BP channel when reconfiguring the RED-TFET in the four operation modes, enabled by electrostatic doping as controlled by V_{g1} and V_{g2}. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

G controls the channel region. The silicon back-gate is kept floating in all measurements. Devices employed in this study have varying flake thicknesses as measured by AFM between 8 nm and 13 nm. Fig. 2.1(c) shows a representational cross-section high-angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) image of the BP RED-TFET cross-section cut along the A-A' line depicted in Fig. 2.1(b). The triple-gate structure of the device is clearly visible in the low-magnification image; the high-magnification details (images below) show the interface of BP with the gate oxide and the crystalline structure of

BP. Note that there are amorphous-like layers both on the top and on the bottom of the BP layer, presumably PO_x. These unexpected layers not only reduce the thickness of the active BP layer as discussed in the simulation section but also change the actual electrostatics and gate dielectric film thicknesses (see Section 2.7.1). Owing to the electrostatic doping approach implemented here, the doping profile along the source/channel/drain regions is electrically tunable, as shown in Fig. 2.1(d), which enables reconfiguring the device to different operation modes: (1) n-type TFET with a p/i/n profile; (2) n-type MOSFET with an n/i/n profile; (3) p-type TFET with an n/i/p profile and (4) p-type MOSFET with a p/i/p profile.

Depending on the operation mode, the device is characterized by different carrier injection mechanisms. As shown in Fig. 2.1(d), in the n-type (or p-type) MOSFET mode, by applying a positive (or negative) gate bias V_G to the middle gate G, the bands in the "i" channel region are moved downwards (or upwards) to allow electrons (or holes) to be thermally injected from the source into the channel, turning the device from OFF to ON. On the other hand, in the n-type (or p-type) TFET mode, applying a positive (or negative) V_G opens up a band-to-band tunneling window at the source-to-channel junction [Fig. 2.1(d)], turning the device from OFF to ON.

Similar triple-gate structures and reconfigurable operation have been reported in other articles [50], [61], [62]. However, not all four operation modes were achieved in these devices, and the reported current drive in the TFET mode is relatively small. In our devices, we have in particular optimized the contacts to enable both electron and hole injection, which allows to access all four possible operation modes. The key lies in utilizing the top gates G1 and G2 to include gating of BP in the source and drain contact regions. Note that our BP films are located on top of the source and drain contact. We have also carefully engineered the gate structure to reduce oxide thickness and spacer thickness between the gates. Therefore, in the TFET modes, the thin gate dielectric thickness (t_{ox}) and a thin body thickness (t_{body}) together enable ideal electrostatics and ensure the abruptness of the tunneling junction through a small λ-value, enabling us to achieve the lowest room-temperature SS and highest I_{ON} at $V_{ds} = 0.8$ V to date in 2D homojunction TFETs.

2.3 Electrical characterization

Fig. 2.2(a) shows the transfer (I_d – V_g) characteristics of a BP RED-TFET as a function of V_{g1} in n-type configuration, *i.e.* for positive V_{ds} and V_{g2} (V_{ds} = 0.8 V, V_{g2} = 0.8 V). To illustrate the reconfigurability of our devices, first, a positive bias is applied to G1 (V_{g1} = 1.1 V), resulting in an effective n-doping of both, the source and the drain region – the device thus exhibits an n/i/n doping profile across the BP flake – and operates in the n-type MOSFET mode. When V_{g1} decreases progressively until $V_{g1} = -0.3$ V, the n-doping level in the source region becomes lower and electron injection from the source metal contact into the source region is gradually suppressed, as shown in the band diagram in Fig. 2.2(b), resulting in steadily decreasing current levels as indicated by the solid black arrow in Fig. 2.2(a).

Next, when the G1 voltage is further decreased beyond $V_{g1} = -0.3$ V, the doping in the source region becomes p-type. Under these conditions, current levels start increasing again, indicated by the dashed gray arrow in Fig. 2.2(a). This at a first glance surprising non-monotonic trend occurs, since when the source doping is made effectively p-type, the device changes from a conventional n-type MOSFET with an n/i/n doping profile to an n-type TFET with a p/i/n doping profile and a BTBT window at the source-to-channel junction is opened, as shown in Fig. 2.2(b). As V_{g1} is further decreased, the source region becomes even more substantially p-doped, and the BTBT window is enlarged, resulting in further increased current levels, as illustrated by the dashed gray arrow in Fig. 2.2(a). This non-monotonic trend of current level change with V_{g1}, or equivalently source doping level, is an unambiguous evidence for our claim of BTB tunneling in the device. Moreover, reconfigurable operation of our BP RED-TFET from the MOSFET mode to the TFET mode by tuning the source doping is demonstrated in this way.

Similarly, transfer characteristics of a BP RED-TFET as a function of V_{g1} in p-type configuration, *i.e.* for negative V_{ds} and V_{g2} ($V_{ds} = -0.8$ V, $V_{g2} = -1.2$ V) are shown in Fig. 2.2(c). When the source doping is changed from p-type to n-type by sweeping the G1 bias from $V_{g1} = -1.5$ V to V_{g1} = 0.9 V, one observes a similar non-monotonic trend of current level change as in Fig. 2.2(a) and reconfiguration from the p-type MOSFET mode to the

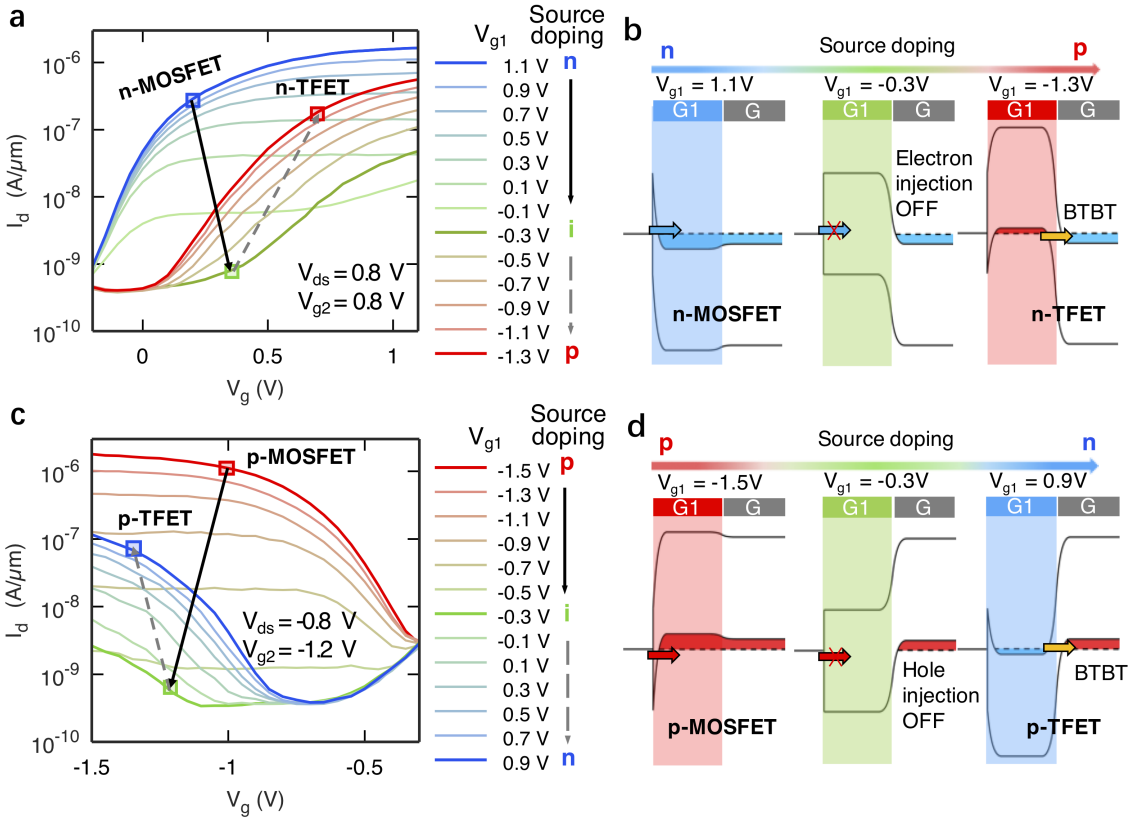


Figure 2.2. Transfer characteristics and reconfiguration of the BP RED-TFET. (a, c) Transfer characteristics of the BP RED-TFET in (a) n-type and (c) p-type configurations under different source doping conditions, showing the transition from the MOSFET mode to the TFET mode. (b, d) Band diagrams of the RED-TFET in (b) n-type and (d) p-type configurations corresponding to different source doping conditions in (a, c) respectively. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

p-type TFET mode. The band diagrams of our BP RED-TFET changing from the p-type MOSFET mode to the p-type TFET mode are shown in Fig. 2.2(d).

The output characteristics (I_d – V_{ds}) of the BP RED-TFET configured in (a) the p-type and n-type MOSFET mode and (b) the p-type and n-type TFET mode are displayed in Fig. 2.3. Output saturation is observed for all four operation modes, indicating a good electrostatic control of the channel by the gate. Note that in the TFET modes, I_d increases nonlinearly with V_{ds} for small V_{ds} [Fig. 2.3(b)]. While non-linear output characteristics are

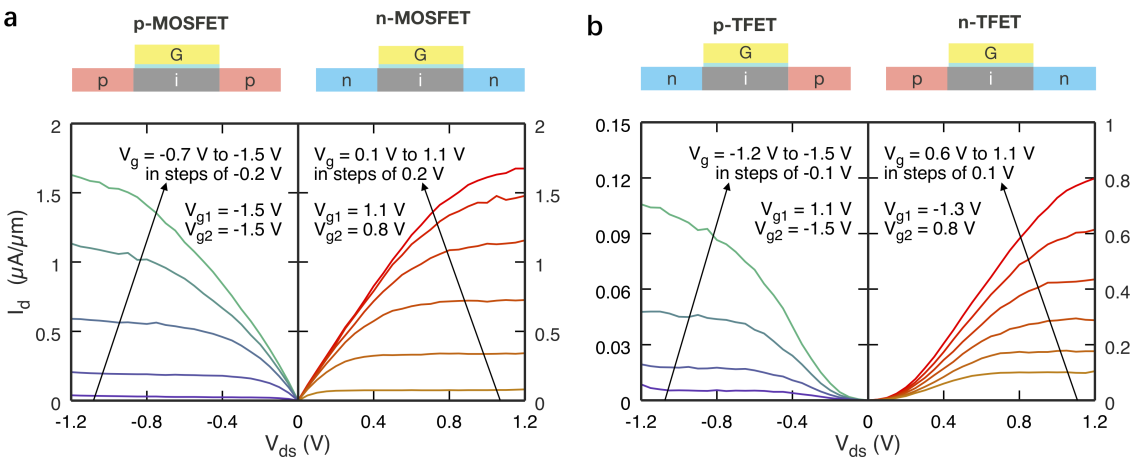


Figure 2.3. Output characteristics of the BP RED-TFET. (a) Output characteristics of the BP RED-TFET in the p-type and n-type MOSFET mode. The saturation behavior indicates a good gate control on the channel. (b) Output characteristics of the BP RED-TFET in the p-type and n-type TFET mode. Non-linear output onsets are observed due to drain-induced-barrier thinning (DIBT) effect. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

often seen as a sign for Schottky-barrier contacts, this explanation does not apply in our case. In fact, if the non-linearity would indeed be caused by the contacts, the device operating in the MOSFET modes with the same source doping configurations would also exhibit non-linearity in the output characteristics, which is clearly not the case in Fig. 2.3(a). Instead, the observed non-linear increase in I_d originates from drain-induced-barrier-thinning (DIBT) of the BTBT barrier [15], which is a consequence of the relatively large quantum capacitance of the black phosphorus channel. Therefore, it is exclusive to TFETs and not observed in MOSFETs where BTB tunneling barriers are absent. Note that in a 1D carbon nanotube device with low quantum capacitance, DIBT can be suppressed in the quantum capacitance limit [65] and linear output characteristics can be recovered [15].

2.4 Temperature-dependent measurement

Transfer characteristics of the BP RED-TFET in n-type configuration at different temperatures are shown in Fig. 2.4(a). It is apparent that lowering the temperature results in

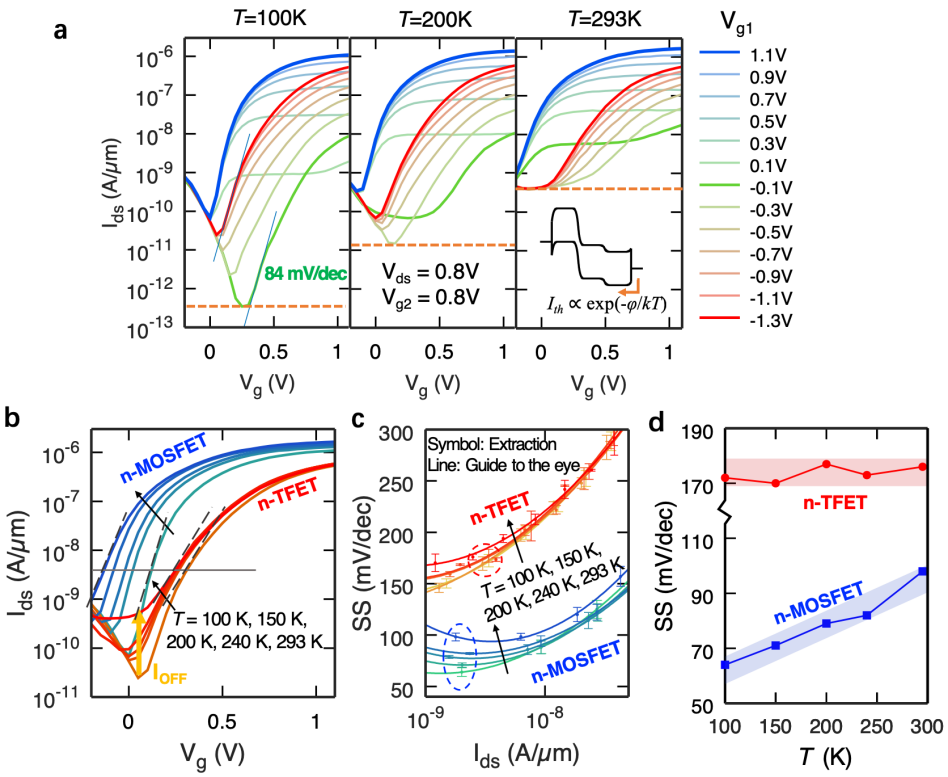


Figure 2.4. Temperature-dependent measurements. (a) Comparison of transfer characteristics of the BP RED-TFET at 100 K, 200 K and 293 K, showing increasing OFF-current levels at elevated temperatures. Dashed orange lines indicate thermionic current and trap-assisted current cut-off limits. The inset shows a band diagram explaining the impact of thermionic injection from the drain at higher temperatures. (b) Comparison of transfer characteristics of the BP RED-TFET in the n-type MOSFET mode and the n-type TFET mode at different temperatures. In the n-TFET mode, the transfer characteristics show a weaker temperature dependence compared with the operation in the n-MOSFET mode, except for a rise in the minimum OFF current level due to thermal injection. (c) Comparison of experimental subthreshold swing (SS) values versus drain current I_d in the n-type MOSFET mode and the n-type TFET mode at different temperatures. In the n-TFET mode, SS shows weaker temperature dependence. (d) Comparison of experimental SS values versus temperature for the n-type MOSFET mode and the n-type TFET mode. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

reduced OFF current levels, due to suppressed thermionic injection from the drain [see inset of Fig. 2.4(a)] and suppressed trap-assisted transport [61]. Fig. 2.4(b) shows a comparison of temperature-dependent $I_d - V_g$ characteristics for a device operating in the n-type MOSFET mode and in the n-type TFET mode. The device shows distinctly different temperature-dependences when operating in these two modes due to different injection mechanisms. In the MOSFET mode, the carriers are thermally injected into the channel, therefore $I_d - V_g$ has a strong dependence on temperature. By contrast, the carrier injection mechanism is BTB tunneling in the TFET mode, and $I_d - V_g$ displays a much weaker dependence on temperature [13], as shown in Fig. 2.4(b). Note that the increasing minimum OFF current with temperature in case of the TFET is due to an increase in thermionic injection at higher temperatures over the drain barrier biased at positive V_{g2}–values. Fig. 2.4(c) shows SS–values versus drain current I_d in the n-type MOSFET mode and the n-type TFET mode at different temperatures, where the latter clearly shows a weaker temperature dependence. Fig. 2.4(d) compares SS–values versus temperature for the same device operating in the MOSFET mode and in the TFET mode. SS–values are extracted near a constant current of 5 nA [as shown in circles in Fig. 2.4(c)], in order to avoid the impact of the temperature-dependent thermionic current cut-off [dashed orange lines in Fig. 2.4(a)] on the SS-extraction. As expected, SS–values increase with temperature in case of the MOSFET mode while remaining constant in the TFET mode.

Also note that the minimum SS-value at room temperature for band-to-band tunneling is 178 mV/dec, well above 60 mV/dec. This is in part due to the choices of flake thickness and gate dielectrics as discussed below but also related to the fact that the steepest slopes in case of TFETs occur at the lowest current levels. In fact, when analyzing the green curve at $V_{g1} = -0.1$ V at 100 K, a minimum SS-value of 84 mV/dec is extracted.

2.5 Performance benchmark and projections

Previous studies on building TFETs using 2D materials [42], [48], [49] mainly focused on vertical heterostructures. This is in part due to the difficulty in achieving chemical doping in 2D materials [6] (which is resolved here using electrostatic doping), while in heterostructures,

the band alignment between different 2D materials can be leveraged to construct a tunneling p-n junction. Lateral homojunction TFETs, which are the focus of this study and prior work [61], have better scaling potential compared with vertical heterojunction TFETs. In this context, Fig. 2.5 shows a comparison of the area scaling of a vertical and a lateral TFET. Since the tunneling area in a vertical TFET is proportional to the channel length L, the normalized ON-current will decrease proportionally when scaling down the channel length, as shown in Fig. 2.5(a). Moreover, the accessible steep slope regime of the subthreshold characteristics will also decrease after scaling. This means achieving steep slopes alone, without high ON-currents, is of little practical value. On the other hand, lateral TFETs do not suffer from the same scaling dilemma.

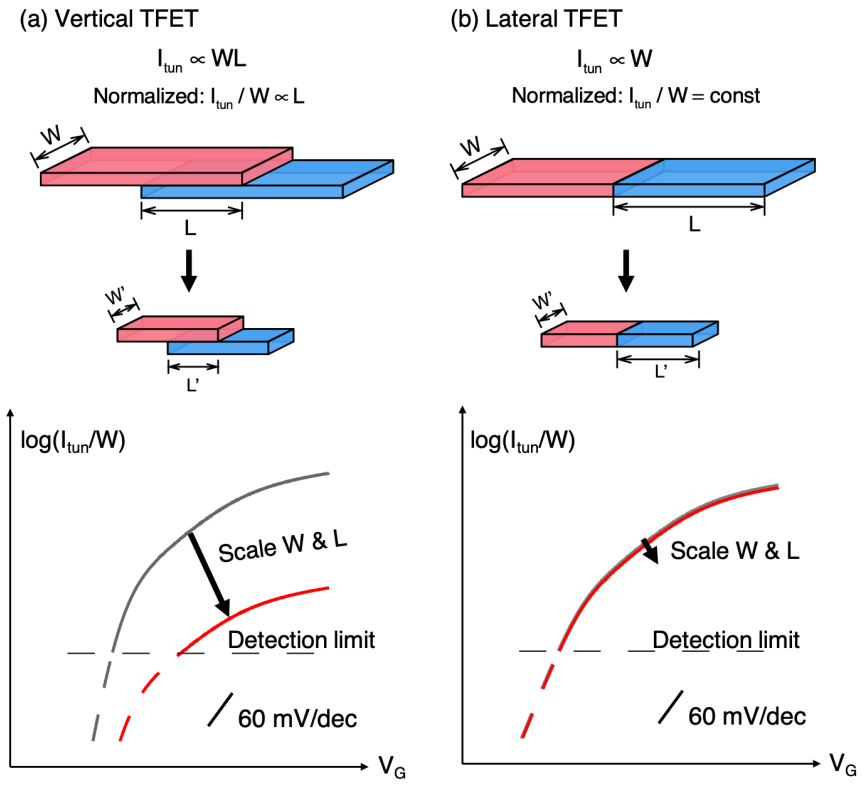
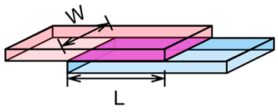
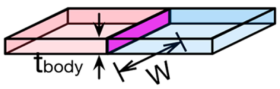


Figure 2.5. Comparison of scaling for (a) a vertical TFET and (b) a lateral TFET. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

Table 2.1 shows a comparison of 2D TFETs from previous publications and our work. As evident, BP TFETs as discussed here are achieving the highest tunneling current densities 2×10^4 A/cm^2, a critical step in the development of TFETs. From the table, one can readily see that all vertical TFETs exhibit rather low tunneling current densities of ~ 10 A/cm^2 – three orders of magnitude lower than reported here – which is compensated by employing a large tunneling area of $\sim$10 μm$\times$10 μm in the prototype device demonstrations. Scaling down the channel length into the sub-micron regime, the ON-current will drop by orders of magnitude and become too low for practical applications. While previous vertical heterojunction 2D TFETs are important proof-of-concept demonstrations for steep-slope devices, they fundamentally lack the scaling potential as required for modern ICs. In contrast, the ON-current of a lateral device will not be affected by channel length scaling, as shown in Fig. 2.5(b), which means that lateral TFETs are more promising candidates for scaled devices than vertical TFETs.

Table 2.1. A comparison of 2D TFETs. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

Structure	Ref.	Material	I_{ON}	Area	Current density	Minimum SS @300K	ON/ OFF	Reconfi gurable
Vertical heterojunction 	[18]	MoS_2/ WSe_2	5 nA (V_{DS}=-1.5 V)	~2 µm×4 µm	0.06 A/cm^2	130 mV/dec	10^4	Yes
	[25]	BP/ $SnSe_2$	10 µA (V_{DS}=-1 V)	~9 µm×8 µm	13 A/cm^2	--[1]	--[1]	No
	[26]	WSe_2/ $SnSe_2$	4 µA (V_{DS}=-1 V)	~140 µm^2	3 A/cm^2	164 mV/dec	10^6	Yes
Lateral homojunction 	[27]	WSe_2	1.2 nA/µm (V_{DS}=-0.5 V)	3 nm×1 µm	40 A/cm^2	366 mV/dec	10^2	Yes
	[40]	BP	0.2 µA/µm (V_{DS}=-2 V)	~5 nm×1 µm	4×10^3 A/cm^2	595 mV/dec	10^2	Yes
	Our work	**BP**	**0.6 µA/µm (V_{DS}=0.8 V)**	**3 nm×1 µm**	**2×10^4 A/cm^2**	**170 mV/dec**	**10^3**	**Yes**

[1] Tunneling diode

The tunneling area is defined by $W \times L$ in a vertical heterojunction, and $W \times t_{body}$ in a lateral homojunction, where W and L are channel width and channel length, respectively. Since the tunneling area is independent of L in a lateral homojunction, this device layout exhibits better scaling potential.

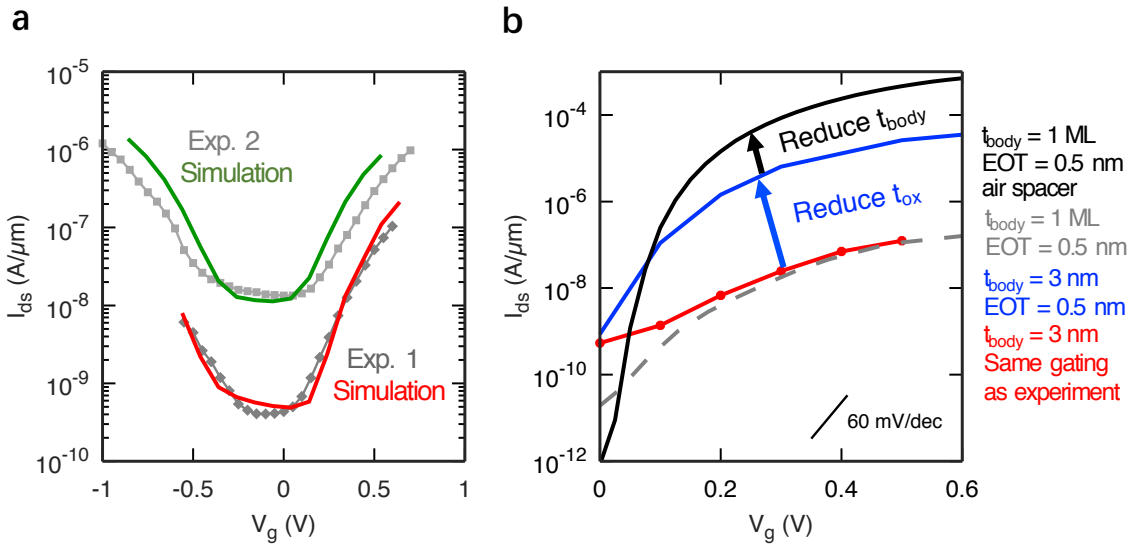


Figure 2.6. Projections for BP TFET performance. (a) Atomistic simulations, solid lines, of $I_d - V_g$ for two exemplary BP TFETs, showing good agreement with experimental data (gray dots). Exp. 1 refers to measurements performed on a device as shown in Fig. 2.1 with a nominal 8.3 nm body and with gate G1 and G2 having configurations (−1.3 V, 0.8 V). The simulation has been performed with a smaller BP thickness of 3 nm and a thicker oxide to account for the oxidation. Exp. 2 is a measurement of an earlier prototype device with a thicker BP flake of 12.8 nm that has been simulated with 7 nm to account for the oxidation. (b) Simulation of the fabricated BP TFET shown in red. Improving the electrostatics by using HfO_2 with an EOT = 0.5 nm is expected to significantly improve steepness and current levels as shown in blue. Further improvements can be achieved by scaling down the channel into a mono-layer (ML) BP and incorporating air spacer as shown in black. Notice that due to the larger bandgap of ML BP, the current levels are lower without proper electrostatics enabled by an air spacer, as shown by the gray dashed line. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

In order to boost the performance of BP TFETs further, channel body and oxide thicknesses need to be aggressively scaled down [46]. As one can see from equation (2.1), the performance of a TFET not only depends on material parameters such as E_g and m^*, but in particular also on the screening length λ, which in turn depends on t_{ox} and t_{body}. In order to make quantitative projections about the potential performance improvement of 2D BP TFETs with scaled down t_{ox} and t_{body}, self-consistent atomistic simulations are first

performed using the NEMO5 toolsets [66], [67] to match the experimental data obtained in this study. Fig. 2.6(a) shows a comparison of simulated I_d – V_g and measured TFET characteristics, showing good agreement between simulation and experimental data. Note that to achieve this matching we made use of our findings from Fig. 2.1(c). To describe the experimental results (Exp. 1) for a device with a nominal thickness of $t_{body} = 8.3$ nm and $t_{ox} = 5.6$ nm properly, $t'_{body} = 3$ nm and $t'_{ox} = 7.5$ nm were assumed in the simulations to account for formation of the above mentioned PO_x layers, where t'_{body} and t'_{ox} denotes the real body thickness and real oxide thickness, respectively, after considering formation of PO_x layers. Under these assumptions, both, the inverse subthreshold slope as well as the actual current levels are properly reproduced [see Fig. 2.6(a)]. Moreover, when performing a similar comparison for a device from a slightly thicker BP flake, a $t'_{body} = 7$ nm and a $t'_{ox} = 8.1$ nm in the simulation nicely match the experimental results for the nominal values of $t_{body} = 12.8$ nm and a $t_{ox} = 6.2$ nm [Exp. 2 in Fig. 2.6(a)]. All simulations are performed with transport direction along the armchair direction of BP.

With this calibration in place, we are in a position to carry out projections based on simulations for aggressively scaled BP TFETs. Fig. 2.6(b) shows simulated I_d – V_g of a BP TFET when scaling down the oxide to an equivalent oxide thickness (EOT) of 0.5 nm while keeping the same channel thickness of $t'_{body} = 3$ nm (blue line). This approach results in significant improvements in the steepness of the subthreshold region and ON-current levels. Moreover, further scaling down the channel thickness to a single mono-layer (black line) and etching the spacers between separate gates to achieve better electrostatic conditions [64] result in $I_{ON} = 800$ μA/μm and SS = 12 mV/dec values, clearly highlighting the potential of BP TFETs in future applications. It is worth noticing that mono-layer BP exhibits a much larger bandgap than few-layer [8], [58] ($\sim$2 eV compared with $\sim$0.3 eV). Therefore, scaling down the channel thickness to a single mono-layer without introducing air-spacer results in a lower current level (gray dashed line), and the employment of the novel air-spacer structure amplifies the electric field in the tunnel junction [64], compensating for the increase in bandgap and as a result boosting the ON-current to 800 μA/μm (black line).

2.6 Conclusion

In conclusion, we have demonstrated reconfigurable complementary BP TFETs. The TFETs exhibit ON-currents of up to 0.6 μA/μm and subthreshold swings of 170 mV/dec at room temperature for V_{ds} = 0.8 V in n-type configuration and ON-currents of up to 0.14 μA/μm and subthreshold swings of 174 mV/dec at room temperature for V_{ds} = −0.8 V in p-type configuration. Record high tunneling current densities of 2×10^4 A/cm^2 have been achieved in the TFETs through proper choice of material and optimization of device structure. Our devices can be reconfigured to behave as an n/p-type TFET and as an n/p-type MOSFET owing to electrostatic doping control of three separate top gates. Atomistic simulations predict that the performance of BP TFETs can be further improved towards I_{ON} = 800 μA/μm and SS = 12 mV/dec with scaled down channel and oxide thicknesses. Our BP RED-TFET provides a guide for energy-efficient tunneling devices based on 2D materials.

2.7 Appendix

2.7.1 Thickness determination of BP

It is well known that BP readily oxidizes and forms PO_x upon exposure to air by reacting with oxygen and water [68]–[70]. In addition to air exposure during the device fabrication process, the BP surface was also exposed to a water rich environment at elevated temperatures (200 °C) during the ALD gate oxide deposition. Since the electrically active BP layer thickness is a critical parameter for the tunneling currents in our devices, it is important to determine the thicknesses of the oxidized layers and the thickness of the remaining crystalline BP layer in the total BP flake thickness.

Fig. 2.7(a) shows an AFM image and line scan of a t_{body} = 8.3 nm thick BP flake as the active channel in one of the BP RED-TFETs with a nominal t_{ox} = 5.6 nm thick Al_2O_3/HfO_2 gate dielectric stack as described in the manuscript. Fig. 2.7(b) shows a comparison of the experimentally measured I_d – V_g curve of this device and a set of simulations with different flake thicknesses. In our simulations, we have considered both the reduction of the body

thickness and the increase of the oxide thickness as a result of oxidation, and we assume the resulting PO_x layers on the top and on the bottom side of BP are of the same thickness (note that only the PO_x layer on the top contributes to the gate dielectric thickness t'_{ox}). The dielectric constants of the oxides used in the simulation are 8 for Al_2O_3, 16 for HfO_2 and 5.4 for PO_x. The chemical composition of the PO_x layer formed on black phosphorus is assumed to be P_2O_5 (Ref. 3) and the dielectric constant is estimated from phosphate glass [71], in which P_2O_5 acts as glass former. As apparent from Fig. 2.7(b), a body thickness of $t'_{body} = 3$ nm and a $t'_{ox} = 8.3$ nm ($t_{ox} = 5.6$ nm, plus additional 2.7 nm of PO_x layer) results in the best match between experiment and simulation.

To verify our assumption of a substantial reduction in BP body thickness and corresponding increase of dielectric layer thickness through the formation of PO_x, a careful TEM analysis on another BP RED-TFET that went through the same fabrication process was performed. The BP flake thickness in this device is determined to be $t_{body} = 12.8$ nm from AFM measurements, as shown in Fig. 2.7(c). Fig. 2.7(d) shows an HAADF-STEM image of the BP RED-TFET. Fig. 2.7(e) shows higher magnification HAADF-STEM images of the "G1-S" and "G1" regions, as depicted by the red and green boxes in Fig. 2.7(d). The thicknesses of the BP crystalline layer and PO_x layers are labeled in the images, which are determined using the method described below.

Fig. 2.7(f) shows an electron energy loss spectrum (EELS) in the "G1-S" region, which is the sum of all the background subtracted spectra acquired along the A-B line depicted in Fig. 2.7(e), showing the P-L, O-K and Ti-L edges. Fig. 2.7(g) shows the intensity profiles of the HAADF image (HAADFI) and EELS P-L, O-K and Ti-L edges along the A-B line in Fig. 2.7(e). Combining the HAADF intensity profile and EELS line scan, one can determine the thicknesses of the top PO_x layer and the BP crystalline layer in the "G1-S" region to be 1.4 nm and 6.9 nm respectively. The total flake thickness is 13 nm, which agrees reasonably well with the AFM measurement. Using the same method, we can measure the thicknesses of the top PO_x layer and the BP crystalline layer in the "G1" region to be 1.9 nm and 6.7 nm respectively, with the total flake thickness being 12.2 nm. The discrepancy between the extraction in the G1-S and G1 region occurs reasonable considering the variations when

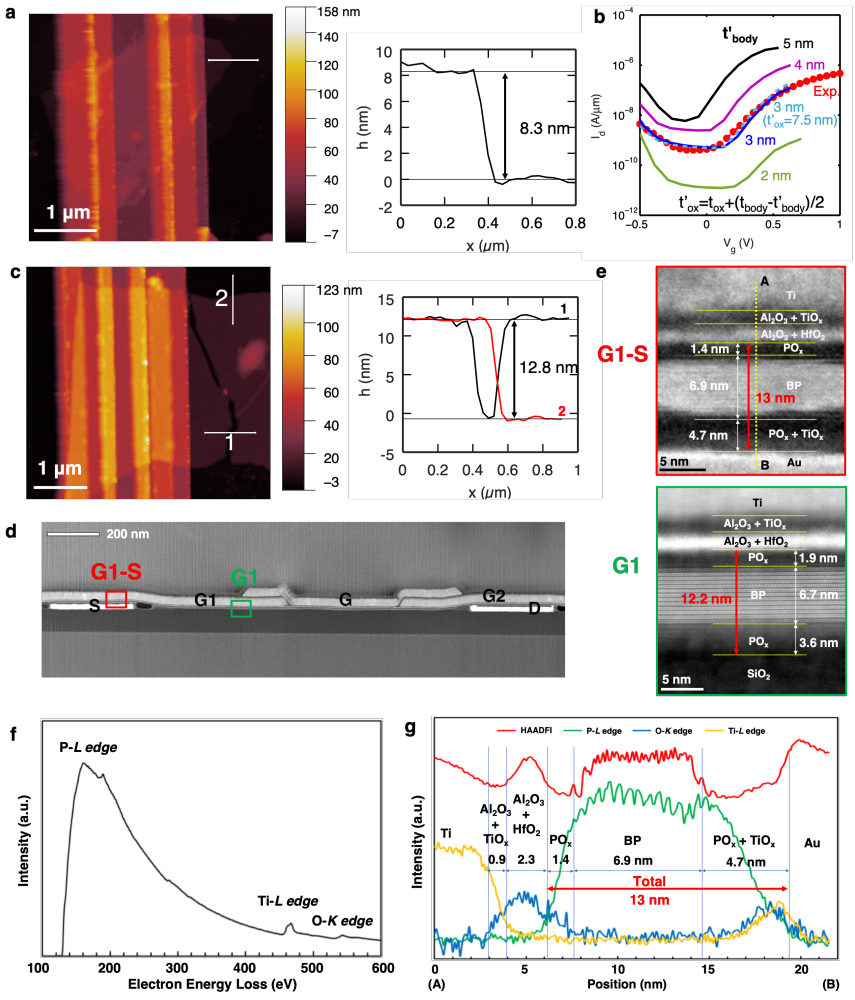


Figure 2.7. Thickness determination of BP. (a) AFM image and line scan of the BP flake used in the electrical characterization (t_{body} = 8.3 nm). (b) Comparison of measured I_d – V_g curve of BP TFET (dots) and simulated I_d – V_g curves for different body thicknesses t'_{body} (lines). The simulation with t'_{body} = 3 nm matches best with the experiment. (c) AFM image and line scan of the BP flake used in the TEM analysis (t_{body} = 12.8 nm). (d) HAADF-STEM image showing the cross-section of the BP RED-TFET. (e) Higher magnification HAADF-STEM images from the regions defined by the red and green boxes in (d). (f) Background subtracted EELS spectra, showing the sum of all the spectra acquired along A-B line shown in (e). (g) Intensity profiles of HAADF image and EELS P-L, O-K and Ti-L edges along A-B line in (e), showing the thicknesses of crystalline BP and PO_x layers and total flake thickness. Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

preparing the sample for cross-section TEM and the uncertainty in determining the position of the interface between PO_x and SiO_2.

In conclusion, from the TEM analysis, we have found that in a $t_{body} = 12.8$ nm thick BP flake, the thickness of the BP crystalline layer is reduced to $t'_{body} = 6.9$ nm. This means that in the $t_{body} = 8.3$ nm thick BP flake, the BP crystalline layer thickness should be about $t'_{body} = 2.4$ nm [~ 8.3 nm $-$ (12.8 nm $-$ 6.9 nm)]. Considering the uncertainty in the thickness measurements and device-to-device variations, $t'_{body} = 3$ nm is a good approximation for the simulation framework employed in Fig. 2.7(b). Note that to account for the thickness of the PO_x layer ($\sim$1.9 nm from the TEM analysis), the effective dielectric thickness of the Al_2O_3/HfO_2 plus PO_x gate dielectric stack is corrected to be $t'_{ox} = 7.5$ nm ($\sim$ 5.6 nm + 1.9 nm) which is decomposed in the atomistic simulation into the various oxide layers.

2.7.2 Effects of BP orientation and transport direction on BTBT

BP exhibits anisotropic effective masses along different transport directions [58]. DFT calculations [58] show that in monolayer BP, the carrier effective masses are 0.15 m_0 (holes) and 0.17 m_0 (electrons) in the armchair direction, and 6.35 m_0 (holes) and 1.12 m_0 (electrons) in the zigzag direction. On the other hand, in bulk BP, the values are 0.14 m_0 (holes) and 0.15 m_0 (electrons) in the armchair direction, and 0.71 m_0 (holes) and 1.15 m_0 (electrons) in the zigzag direction.

As we have discussed before, the BTBT tunneling current is exponentially dependent on the effective mass. Therefore, the current level of a BP TFET depends on the transport direction. It has been experimentally demonstrated in Ref. [61] that the anisotropy of band-to-band tunneling in armchair direction and zigzag direction in BP can be up to 10^4. Here, we have investigated the effects of BP orientation on BTBT by both i) simulation and ii) a statistical study of experimental device currents.

Fig. 2.8(a) shows the analytic modeling approach for the orientation-dependent BTBT current in BP TFETs. We have calculated a tunneling direction dependent transmission $T(\theta)$ based on the direction dependent tunneling distance $\lambda/\cos(\theta)$ and effective mass $m^*(\theta)$, and integrate over the full range of transport directions to obtain the total BTBT current I_{ON}.

Considering the effective masses anisotropy in BP, the tunneling direction dependent effective mass $m^*(\theta)$ is estimated by assuming an elliptical iso-energy surface in k-space. Fig. 2.8(b) shows the results of the model. The dependence of ON-current on the orientation of the BP device shows a strong non-linear behavior. However, while the possible range of I_{max}/I between transport in the armchair and in the zigzag direction can be as much as $\sim 10^3$, the ON-current differs only by less than 50% when the transport direction is within 30° of the armchair direction.

Fig. 2.8(c) shows atomistic simulations of $I_d - V_g$ curves for a BP TFET along different transport directions. The thickness of BP in the simulation is assumed to be that of a single mono-layer and the gate oxide is HfO_2 with an EOT = 0.5 nm with the spacer between separate gates etched away. This simulation has not been performed for the larger flake thicknesses since a reduced symmetry in the structure along the transverse direction significantly increases the computational cost, which makes it unfeasible to perform simulations with thicker cross-sections. This point can however be addressed by the analytic modeling approach shown in Fig. 2.8(a). The atomistic simulation results match well with the analytical model, as shown by the red dots and line in Fig. 2.8(b).

We have further investigated the effects of orientation on the ON-currents in BP TFET through a statistical study of our experimental data. In the experiments, the orientation of BP is not controlled deliberately; therefore, one can assume the orientation of BP to be randomly distributed between 0° to 90°. Fig. 2.8(d) shows the statistical distribution of ON-currents of experimental BP TFETs, normalized by the "expected" ON-current values. The "expected" ON-current values are estimated from the body thickness of the BP flake, assuming that transport is along the armchair direction. Note that since these devices share the same triple-gate structure, the main factors affecting ON-currents are the bandgap and the screening length λ, which can be deduced from the body thickness of the individual devices. In Fig. 2.8(d) we assign an error bar of 5× to the expected ON-current, considering the uncertainty in body thickness estimation. One can see that the distribution matches approximately with the orientation-dependent trend from our analytic model shown in Fig. 2.8(b). The device investigated in the previous section, indicated by the blue bar, falls into the category of less than 50% deviation from the armchair direction, *i.e.*, the transport di-

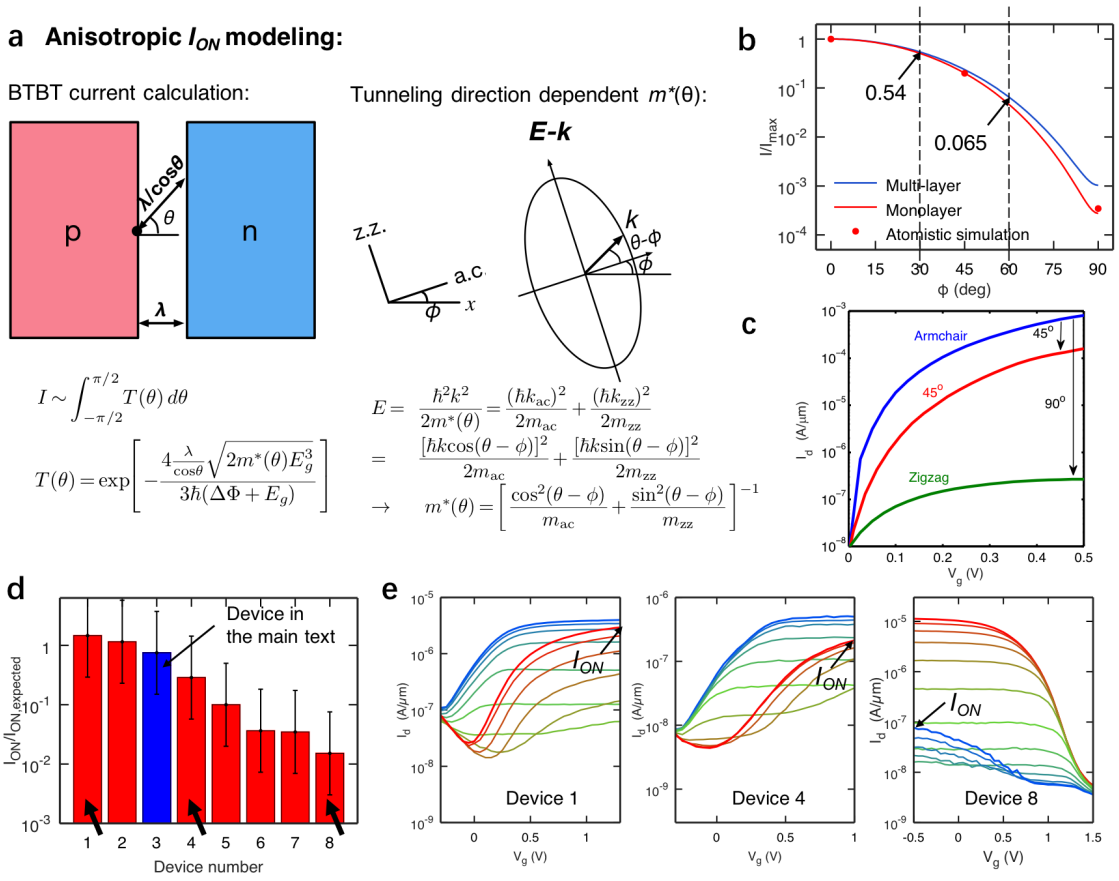


Figure 2.8. Effects of BP orientation and transport direction on BTBT. (a) Brief description of modeling approach of orientation-dependent BTBT current in BP TFETs. (b). Orientation-dependent I_{ON} of multi-layer and mono-layer BP TFETs from the model. The results match with atomistic simulation. (c) Atomistic simulation of effects of BP orientation on BTBT in a mono-layer TFET with EOT=0.5 nm. (d) Statistics of I_{ON} of experimental devices, normalized by expected I_{ON}. (e) Exemplary device characteristics from the statistics in (d). Reprinted with permission from P. Wu *et al.*, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377–385 (2019). Copyright (2019) American Chemical Society.

rection is expected to be within 30° of the armchair direction. However, the eight devices explored by us cover indeed the expected range of ON-currents for differently oriented BP TFETs. In order to control the orientation of BP more precisely, one could envision determining the orientation of BP using angle-dependent Raman spectroscopy prior to device fabrication and alignment of the channel in the armchair direction [61].

Fig. 2.8(e) shows exemplary device characteristics of the devices indicated by the black arrows from the statistical study shown in Fig. 2.8(d). It is worth mentioning that in Device 8, the BTBT branch is already barely observable, since the thermal current cut-off limit at room-temperature is only less than one order of magnitude lower. This implies that a device with $I_{ON}/I_{ON,expected}$ below 10^{-2} may yield a BTBT branch that is not observable at all, which is likely the reason why lower currents as predicted by Fig. 2.8(b) were not observed in Fig. 2.8(d).

2.7.3 Methods

Device fabrication and electrical characterization

Ti/Au (10 nm/20 nm) contacts were deposited onto a silicon substrate with 90 nm of silicon dioxide (SiO_2) on top and patterned using e-beam lithography and lift-off process. BP flakes were exfoliated onto the Au contacts from bulk crystals, purchased from Smart Elements (purity 99.998 %), using mechanical exfoliation with standard dicing tape purchased from Semiconductor Equipment Corp. The exfoliation is performed in ambient atmosphere; however, care was taken to minimize the time that BP flakes were exposed to the air (less than 30 min). A thin layer of Al was e-beam evaporated on top of BP, which formed a 1.3 nm thick aluminum oxide upon exposure to air and acted as seeding layer for the subsequent ALD process. A bilayer dielectric stack composed of 0.8 nm of HfO_2 and 2.2 nm of Al_2O_3 was deposited by a thermal ALD process at 200 °C to form gate dielectrics for G1 and G2. Next, G1 and G2 were defined by subsequent e-beam lithography and e-beam evaporation of 40 nm Ti. The sample is annealed in forming gas for 3 hours at 300 °C to improve the quality of the gate dielectric. To achieve proper isolation between gates G1/G2 and G, while maintaining relatively thin dielectric thicknesses for gate G, the Al_2O_3 between the G1 and G2 regions was removed by wet etching, with G1 and G2 metals as masks and HfO_2 as etch stop layer. A second ALD process was performed to deposit another 3.5 nm Al_2O_3 layer as gate dielectric for G, as well as to ensure isolation between G1/G2 and G. The total oxide thickness for gate G is 5.6 nm. The device fabrication is finalized by depositing 40 nm Ti to form gate G. Room-temperature and low-temperature electrical characterization of the

device was performed in a LakeShore FWPX Cryogenic Probe Station at a vacuum level below 10^{-5} Torr using an Agilent 4156C Parameter Analyzer.

Atomistic simulation

The atomistic quantum transport simulation results have been obtained from a self-consistent solution of the 3D-Poisson equation and by employing the Non-Equilibrium Green's Functions (NEGF) method using the Nanoelectronics modeling tool NEMO5 [66], [67]. The Poisson equation provides the potential for the NEGF method and takes the free charge in return. The tight-binding Hamiltonian of phosphorene used in NEGF calculations employs a 10 bands sp3d5s* 2nd nearest neighbor model. More details on the Poisson equation with anisotropic dielectric tensor and NEGF equations can be found in our previous works [43], [44].

Transmission electron microscopy (TEM) characterization

An FEI Nova NanoLab 600 DualBeam (SEM/FIB) was employed to prepare cross-sectional TEM samples. Carbon was deposited on top of the device to protect the surface. To reduce Ga-ions damage, in the final step of preparation the TEM samples were thinned with 2 kV Ga-ions using a low beam current of 29 pA and a zero-degree incident angle. An FEI Titan 80-300 probe-corrected scanning transmission electron microscope (STEM) equipped with monochromator and GIF Tridiem electron energy loss spectrometer (EELS) system was employed to acquire atomic-resolution high-angle annular dark field (HAADF) images and EELS based spectrum-images. HAADF images were acquired with the detector semi-angular collection range of 35 - 195 mrad. The spectrum-images were acquired with a condenser aperture convergence semi-angle of 13 mrad and a spectrometer entrance aperture collection semi-angle of 14 mrad.

3. BLACK PHOSPHORUS VERTICAL TUNNELING FIELD-EFFECT TRANSISTORS

Tunneling field-effect transistors (TFETs) have been proposed as energy-efficient switches for low-power integrated circuits. In this chapter, we present the first reconfigurable black phosphorus vertical tunneling field-effect transistor (TFET). The device exhibits record high ON-current (I_{ON}) among all 2D TFETs of 15.2 μA/μm at $V_{DS} = -1$ V and a subthreshold swing (SS) of 187 mV/dec at $V_{DS} = -0.3$ V. By tuning the electrostatic doping with multiple gates, the device can be reconfigured to operate in the TFET mode or MOSFET mode and can be tuned to behave like an n-type or p-type FET. Moreover, negative differential resistance (NDR) is observed in the forward bias of the TFET at room temperature, providing unambiguous evidence of band-to-band tunneling in our devices.

3.1 Introduction

Tunneling field-effect transistors (TFETs) have been studied as promising candidates to achieve sub-60 mV/dec subthreshold swing (SS) switching for ultra-low power applications [13], [16], [41]. Meanwhile, two-dimensional (2D) materials have attracted attention recently, since the ultra-thin body allows for strong gate control of the channel electrostatics, which is critical for high performance TFETs. Although the hunt for the ideal 2D material for TFET applications is still ongoing, among various 2D materials, black phosphorus (BP) has been proposed and demonstrated to be a promising channel material for high ON-current TFETs due to its tunable small bandgap and low effective mass [9], [43], [60], [61]. In this chapter, we demonstrate the first TFET based on a black phosphorus vertical homojunction with a record-high ON-current among all 2D TFETs of $I_{ON} = 15.2$ μA/μm at $V_{DS} = -1$ V. Moreover, negative differential resistance (NDR) in the forward bias of the TFET is observed at room temperature, which together with a clear non-monotonic trend of current versus side

gate voltage V_{G1} provides unambiguous evidence of tunneling dominated transport in these novel devices.

3.2 Device structure

A schematic of our BP vertical TFET is shown in Fig. 3.1(a). By applying opposite bias polarities on the local bottom gate G1 and the top-gate TG, a tunneling p/n or n/p junction can be created, enabling a vertical band-to-band tunneling (BTBT) path in the overlap region between G1 and TG. Such operation has been described as electron-hole bilayer TFET (EHBTFET) in previous studies [72], [73].

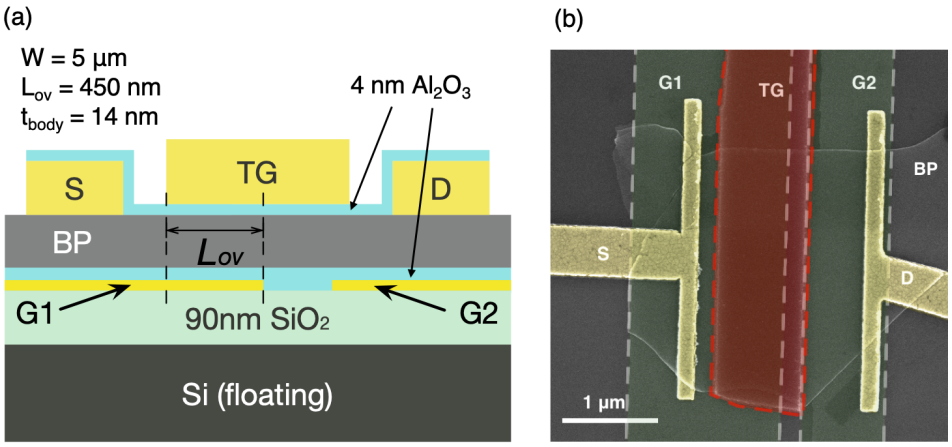


Figure 3.1. (a) Schematic of the black phosphorus vertical TFET. (b) Representative false-colored SEM image of a BP vertical TFET. Reprinted with permission from P. Wu, J. Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor with Record High ON-Currents," *IEEE Electron Device Letters* **40**, 6, 981-984 (2019). Copyright (2019) IEEE.

The process flow for device fabrication is as follows. 2 nm thick Ti metal lines were deposited onto a silicon substrate with 90 nm SiO_2 on top and patterned into electrodes for local bottom gates G1 and G2 using e-beam lithography and lift-off process. 4 nm Al_2O_3 was deposited by atomic layer deposition (ALD) at 200 °C to form the dielectric for G1 and G2. BP flakes were exfoliated onto the local bottom gates from bulk crystals. The thickness of BP (t_{body}) is 14 nm. 1.5 nm/40 nm Ti/Au was deposited and patterned as source/drain contacts. The Ti/Au metal contact enables ambipolar charge injection into the BP channel

[9]. 0.8 nm Al was evaporated on top of BP and naturally oxidized in air to form a seeding layer for the subsequent ALD process. A second ALD process was used to deposit 4 nm Al_2O_3 on top to act as a dielectric for the top-gate TG. Finally, 40 nm Ti was deposited and patterned to form the TG electrode. The device was annealed in forming gas at 300 °C for 3 hours to improve the dielectrics' and contacts' quality. Fig. 3.1(b) shows a representative SEM image of a BP vertical TFET, depicting the BP channel, source/drain contacts and three gates. The device performance shows negligible changes after storage in a nitrogen box for 7 months.

3.3 Device characteristics

Owing to electrostatic doping controlled by G1, TG and G2, the device can be reconfigured to different operation modes: (1) a p-type MOSFET with a p/i/p doping profile; (2) a p-type TFET with an n/i/p doping profile; (3) an n-type MOSFET with an n/i/n doping profile; (4) an n-type TFET with a p/i/n doping profile. Similar reconfigurable operations have been demonstrated in previous works [9], [60], [61]. However, here, the reconfigurability is demonstrated for the first time in a vertical tunneling device, and record-high tunneling currents are experimentally achieved.

We have characterized the device in all different operation modes with different gate biasing conditions as shown in figures 3.2 through 3.5. All measurements were conducted at room-temperature, with the source contact grounded. All currents are normalized to the device width of $W = 5$ μm.

3.3.1 Device operation in p-type configurations

Fig. 3.2(a-b) show the transfer characteristics $I_D - V_{TG}$ of the BP vertical TFET in p-type configuration ($V_{DS} = -0.3$ V/-1 V, $V_{G2} = -2.1$ V) as a function of V_{G1}. We start with a negative G1 bias $V_{G1} = -2.1$ V. Under these conditions, as shown in the schematic and band diagram in Fig. 3.2(c), the device exhibits p-doping across the channel and operates in the p-type MOSFET mode.

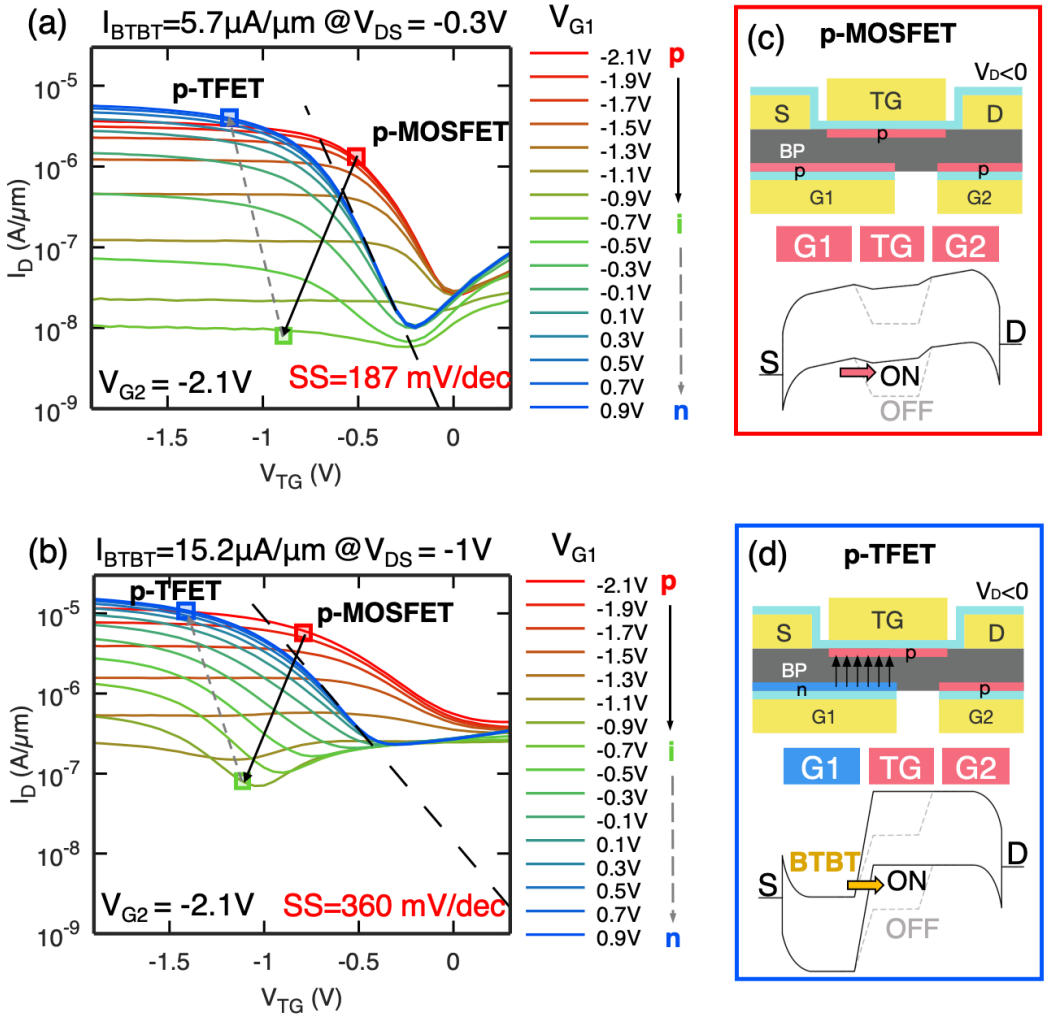


Figure 3.2. (a-b) Transfer characteristics of a BP vertical TFET in the p-type configuration at (a) $V_{DS} = -0.3$ V. (b) $V_{DS} = -1$ V. (c-d) Device schematics and band diagrams in the (c) p-MOSFET mode. (d) p-TFET mode. Reprinted with permission from P. Wu, J. Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor with Record High ON-Currents," *IEEE Electron Device Letters* **40**, 6, 981-984 (2019). Copyright (2019) IEEE.

When V_{G1} increases progressively from -2.1 V to -0.5 V, the effective p-doping induced by G1 becomes weaker and hole injection from the source contact is gradually suppressed, resulting in decreasing current levels, indicated by the solid black arrows in Fig. 3.2(a) and Fig. 3.2(b). Next, when V_{G1} further increases beyond $V_{G1} = -0.5$ V, the effective doping induced by G1 becomes n-type, and the current levels increase again, indicated by the dashed gray arrow in Fig. 3.2(a) and Fig. 3.2(b). This non-monotonic trend that was mentioned in section I is a result of the fact that the n-type doping induced by G1 opens a vertical BTBT path from the n-doped region on the bottom side of BP to the p-doped region on the top side. This in turn makes the device operation change from a p-type MOSFET to a p-type TFET, as shown in the schematic and band diagram in Fig. 3.2(d). As V_{G1} increases further, the n-doping induced by G1 becomes even stronger, and the BTBT window is enlarged, resulting in further increasing current levels. This non-monotonic trend of current level change with V_{G1} is an unambiguous evidence of BTBT in the device. While not shown here, it has been discussed in the context of lateral reconfigurable BP TFETs [9], [61] that the above non-monotonic behavior and an SS that is independent of temperature in the TFET mode but depends linearly on temperature in the MOSFET mode occur hand in hand.

In the p-TFET mode, the device exhibits record high ON-current levels of $I_{ON} = 15.2$ μA/μm at $V_{DS} = -1$ V among all published 2D TFETs. When normalized by the overlap area between G1 and TG, current densities of around 3.4×10^3 A/cm^2 can be extracted, a value that is about two orders of magnitude larger than any previously reported current drive in vertical TFETs [42], [48], [49]. It is worth noting that the ON-current in the p-TFET mode is even higher than the ON-current in the p-MOSFET mode (11.6 μA/μm at $V_{DS} = -1$ V). This phenomenon indicates that electron injection from the source in case of the p-TFET is more efficient than hole injection in this device and hints at that in general contact resistances may still be the limiting factor for the current drive capability of the TFET device.

Fig. 3.3 shows output characteristics of a BP vertical TFET in the (a) p-MOSFET mode and (b) p-TFET mode. Negative differential resistance (NDR) is clearly observed in the forward bias (positive V_{DS} for p-TFET) in the p-type TFET mode at room-temperature, and not in the p-MOSFET mode as expected, providing further evidence for tunneling as

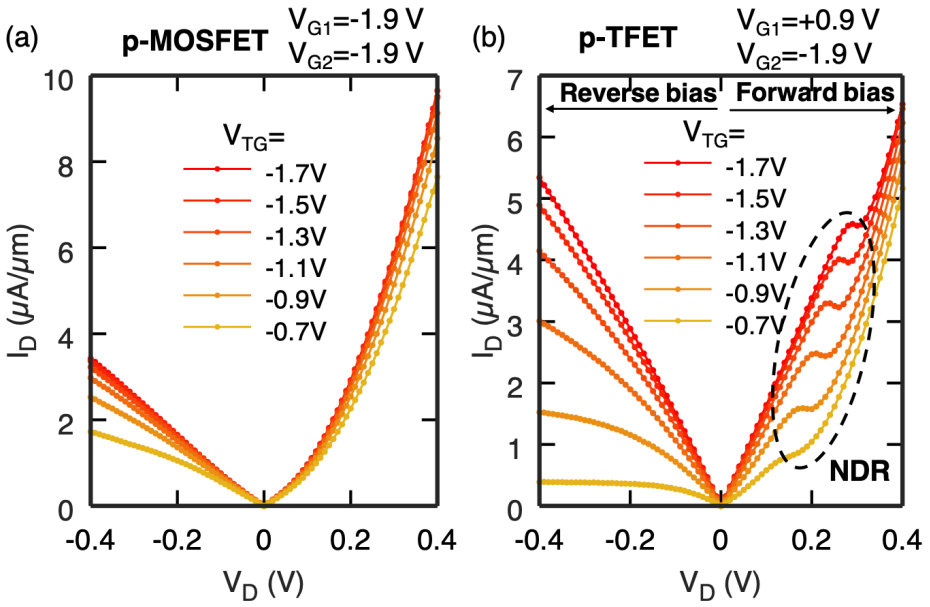


Figure 3.3. Output characteristics of a BP vertical TFET in the (a) p-MOSFET mode (b) p-TFET mode. NDR is observed at room temperature in forward bias direction in the p-TFET mode, but not in the p-MOSFET mode as expected. Reprinted with permission from P. Wu, J. Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor with Record High ON-Currents," *IEEE Electron Device Letters* **40**, 6, 981-984 (2019). Copyright (2019) IEEE.

the dominant mechanism in our TFET devices. NDR in the p-TFET mode is hysteresis free and observable when scanning V_D from 0 upwards or from 0.4 V down to 0.

3.3.2 Device operation in n-type configurations

Fig. 3.4(a-b) show the transfer $I_D - V_{TG}$ characteristics of the device in n-type configuration (V_{DS} = 0.3 V and 1 V, V_{G2} = 0.5 V and 0.8 V) as a function of V_{G1}. Similar to the p-type configuration, the current levels show a non-monotonic change when V_{G1} gradually decreases. In this case the device changes from an n-type MOSFET to an n-type TFET, as shown in the schematics and band diagrams in Fig. 3.4(c-d).

Fig. 3.5 shows the output characteristics of the device in the (a) n-MOSFET mode and (b) n-TFET mode. A trend towards NDR is observed in the forward bias (negative V_{DS} for

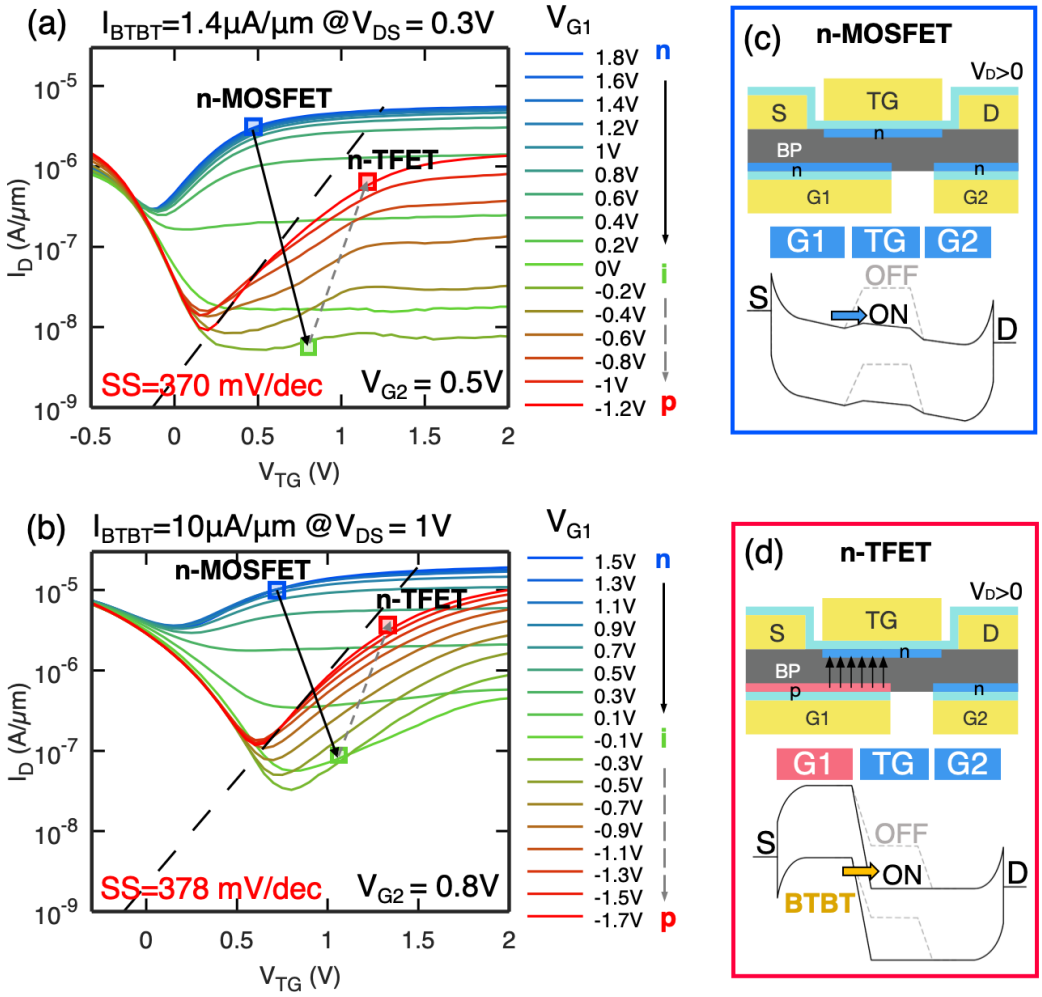


Figure 3.4. (a-b) Transfer characteristics of a BP vertical TFET in the n-type configuration at (a) $V_{DS} = 0.3$ V. (b) $V_{DS} = 1$ V. (c-d) Device schematics and band diagrams in the (c) n-MOSFET mode. (d) n-TFET mode. Reprinted with permission from P. Wu, J. Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor with Record High ON-Currents," *IEEE Electron Device Letters* **40**, 6, 981-984 (2019). Copyright (2019) IEEE.

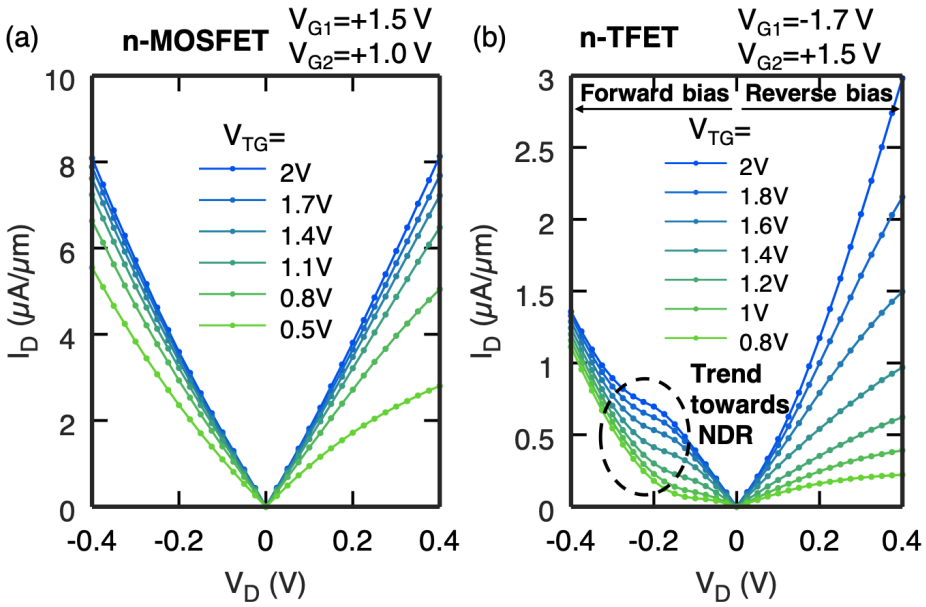


Figure 3.5. Output characteristics of a BP vertical TFET in the (a) n-MOSFET mode (b) n-TFET mode. Trends towards NDR are observed at room temperature in forward bias direction in the n-TFET mode, but not in the n-MOSFET mode as expected. Reprinted with permission from P. Wu, J. Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor with Record High ON-Currents," *IEEE Electron Device Letters* **40**, 6, 981-984 (2019). Copyright (2019) IEEE.

n-TFET) in the n-type TFET mode at room-temperature, and not in the n-MOSFET mode as expected.

3.4 Comparison with previous works on 2D TFETs

Table 3.1 shows a comparison of our vertical BP TFET with recent work on 2D TFETs in the literature. Compared with previously reported vertical TFET characteristics [42], [48], [49], the current density in our device is more than two orders of magnitude higher. While in comparison with BP lateral TFETs [9], [61], the tunneling current densities in our BP vertical TFETs are lower, the ON-current of our device is more than one order of magnitude higher than for BP lateral TFETs due to a larger tunneling area.

We note that SS of the presented device in the TFET mode is 187 mV/dec, still well above the sub-60 mV/dec target, and that the ON/OFF current ratio of 10^2 is lower than

Table 3.1. Comparison with other 2D TFETs. Reprinted with permission from P. Wu, J. Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor with Record High ON-Currents," *IEEE Electron Device Letters* **40**, 6, 981-984 (2019). Copyright (2019) IEEE.

Struct.	Ref.	Material	I_{ON}	ON/ OFF	Current density	SS_{min} @300K	NDR
Vertical	[42]	MoS_2/ WSe_2	5 nA	10^4	0.06 A/cm^2	130 mV/dec	Yes (150K)
	[48]	BP/ $SnSe_2$	10 μA	–[1]	13 A/cm^2	–[1]	Yes (300K)
	[49]	WSe_2/ $SnSe_2$	4 μA	10^6	3 A/cm^2	164 mV/dec	Yes (77K)
	This work	**BP**	**15.2 μA/μm**	**10^2**	**3.4×10^3 A/cm^2**	**187 mV/dec**	**Yes (293K)**
Lateral	[61]	BP	0.2 μA/μm	10^2	4×10^3 A/cm^2	595 mV/dec	No
	[9]	BP	0.6 μA/μm	10^3	2×10^4 A/cm^2	170 mV/dec	No

[1] Tunneling diode

previously reported for some devices. To reduce SS, a common approach is to reduce the tunneling distance λ by scaling down t_{body} and t_{ox}. However, scaling down t_{body} from multi-layer to mono-layer, the band gap of BP increases from ∼0.3 eV to ∼2.0 eV, which is not desirable for high ON-currents. Besides, in a BP vertical TFET, the channel thickness should be above a certain limit to create an electron-hole bilayer [72]. Therefore, rather than scaling t_{body}, an alternative approach has been proposed in [74], in which a 3-layer BP and 1-layer BP is combined as the channel material in a lateral TFET. In this design, the 3-layer BP with a low bandgap of ∼0.57 eV is used as a tunneling junction to enable a high ON-current of 1280 μA/μm, while the 1-layer BP with a larger bandgap is connected in series and enables a low OFF-current of 10^{-4} μA/μm and a steep SS of 10 mV/dec. Such thickness-engineered design of combining a thick layer and thin layer of BP could also be adopted in the vertical TFET to achieve high ON-currents while simultaneously reducing the OFF-current and SS. A selective etching in the G2 region can be adopted to introduce a thin BP region with a

larger bandgap in the channel to reduce OFF-current, while the vertical tunneling in the G1-TG overlapping region with thick BP and a smaller bandgap is not affected.

3.5 Conclusion

We have demonstrated the first reconfigurable BP vertical TFET with ON-currents of 15.2 μA/μm at $V_{DS} = -1$ V, that outperform existing current levels in 2D TFETs. SS-values of 187 mV/dec at $V_{DS} = -0.3$ V are achieved. Moreover, clear reconfigurability of the devices is demonstrated by tuning the electrostatic doping controlled by multiple gates and room-temperature NDR is observed at forward biases for devices operating in the p-TFET mode. The novel device presented here shows promising performance specs that pave the way towards building high performance TFETs from novel 2D materials.

4. TOWARDS CMOS-LIKE DEVICES FROM TWO-DIMENSIONAL MATERIALS

In this chapter we explain in detail the critical aspects of Schottky barrier (SB) field-effect transistors (FETs) for circuit implementations. In particular, we focus on two-dimensional (2D) channel materials such as black phosphorus. After an initial tutorial about the operation of SB-FETs, we discuss various scaling approaches and how proper unipolar device characteristics from 2D layered materials can be obtained. Various transistor layouts described in the literature are evaluated in terms of the achieved device performance specs, and the most advanced experimental approach is presented that combines proper scaling, source/drain work function engineering, and gating. This chapter closes by highlighting the performance of an inverter obtained from properly designed BP-based n-type and p-type transistors.

4.1 Introduction

Complementary metal-oxide semiconductor (CMOS) devices have been the work-horses of the information technology (IT) industry over the last few decades. What makes the CMOS so successful is its complementary nature that n-type and p-type transistors can be made from silicon alike. An n-type field-effect transistor (FET) is characterized by operating in its on-state under positive drain voltages (V_{ds}) and gate voltages (V_{gs}) beyond its threshold voltage V_{th-n}. For $V_{gs} < V_{th-n}$, the device is in its off-state. The situation is mirrored in terms of voltage polarities for a p-type FET. Combining both types of FETs allows for power efficient circuits. For example, in an inverter that consists of an n-FET and a p-FET in series between ground and the supply voltage V_{DD} with a common input to the two gates, energy is

only dissipated during the actual switching process that defines the output to be low or high [75]. Thus, mimicking this device behavior in novel channel materials is highly desirable.

Scaling silicon transistors over the last decade has, in particular, focused on making devices smaller while preserving the electrostatics through the use of thin silicon fins. However, silicon fins with ultrathin bodies (t_{body}) below ~3 nm show a strong degradation of their mobility, which makes the smaller t_{body} more significant due to increased scattering at the Si/SiO_2 interfaces [76], [77]. Ultimately, it is desirable to achieve body thicknesses in the subnanometer range without the introduction of excess scattering in the semiconductor.

After the groundbreaking work by Novoselov et al. in 2004 [2] on few-layer graphene, a semimetal, the scientific community started searching for other two-dimensional (2D) crystals as the ultimate implementation of an ultrathin body channel, with the declared goal to identify semiconducting materials for electronic applications. In 2011, Radisavljevic et al [3]. reported on the first single layer MoS_2 transistors with a bandgap around 1.8 eV, followed by the demonstrations of FETs from black phosphorus (BP) in 2014 [7], [78]. While these devices in fact exhibit body thicknesses below 1 nm, their mobility was found to be in the range of tens to hundreds of $cm^2/V \cdot s$ [7], [78]–[82], making them attractive for ultimately scaled transistor applications as an extension of the above mentioned work on silicon FinFETs.

However, creating the desired n-type and p-type FETs from the same 2D channel material that exhibit the above described unipolar transport properties, *i.e.*, only electrons (holes) are involved in current transport in the case of an n-FET (p-FET), has been proven difficult. This lies in part in the fact that substitutional doping to create an n/p/n or p/n/n profile along the channel, as in the case of silicon devices, is hard to achieve due to the small number of atoms involved in forming the device channel. As a result, most of the prototype devices on 2D channels are using metal electrodes (instead of doped semiconductors) as source and drain contacts. The resulting devices are so-called Schottky barrier (SB) field-effect transistors, where gating includes the source and drain contact regions. Ambipolar transport is typically observed since for positive gate voltages, electrons are involved in current transport, while for negative V_{gs}, hole transport occurs through the valence band [83].

4.2 Basic operation of Schottky-barrier field-effect transistors

In order to address this undesirable situation, it is important to understand some details about the operation of Schottky barrier field-effect transistors (SB-FETs). Fig. 4.1 illustrates in simple terms how device characteristics depend on a number of critical parameters as the Schottky barrier heights Φ_{SB-p}, Φ_{SB-n}, and the geometric screening length λ. For all graphs, it was assumed that the conduction band edge E_C and valence band edge E_V respond 1:1 to the gate voltage V_{gs} in the off-state of the device. This implies, in particular, that an ideal inverse subthreshold slope (SS) of 60 mV/dec at room temperature is achievable when carrier injection (electrons or holes) into the channel is mediated by thermal emission (I_{th}) over band edge E_C or E_V.

Let us first focus on the green curve in Fig. 4.1 that plots the logarithmic current from source to drain as a function of gate voltage. The device is in its on-state when $V_{gs} < V_{th-p}$ for hole transport and $V_{gs} > V_{th-n}$ for electron transport. The corresponding image band structures for the voltages marked (1) and (3) are shown next to the device characteristics with E_{Fs} and E_{Fd} denoting the Fermi level in the metal source and drain, respectively. For voltages in between V_{th-p} and V_{th-n}, the device is in its off-state with three distinct slopes. Between V_{th-p} and the flat band voltage V_{FB} [marked (2) in Fig. 4.1], device characteristics are determined by thermal assisted tunneling I_{tunnel} through the Schottky barrier Φ_{SB-p}. This is the case since for an ultrathin body device, the characteristic tunneling distance is given by the so-called geometric screening length $\lambda = \sqrt{(\epsilon_{body}/\epsilon_{ox})t_{ox}t_{body}}$ that can become very small for small t_{body} values. Here, ϵ_{body} and ϵ_{ox} are the dielectric constants and t_{body} and t_{ox} the thicknesses of the channel material and the gate dielectric, respectively. The SS value in this region depends on the actual value of λ and varies between 60 mV/dec for $\lambda = 0$ (dark blue curve) and SS $= \infty$ for $\lambda = \infty$ (orange curve). The orange marked triangle on the left of Fig. 4.1 indicates the range of allowed inverse subthreshold slopes. Once flat band voltage is reached, only thermal emission is allowed (I_{th}) until a minimum current is reached at V_{min}. At this point, the thermally injected hole current through the valence band becomes equal to the thermally assisted electron tunneling current through Φ_{SB-n} into the conduction band. Finally, for $V_{min} < V_{gs} < V_{th-n}$, tunneling of electrons through the

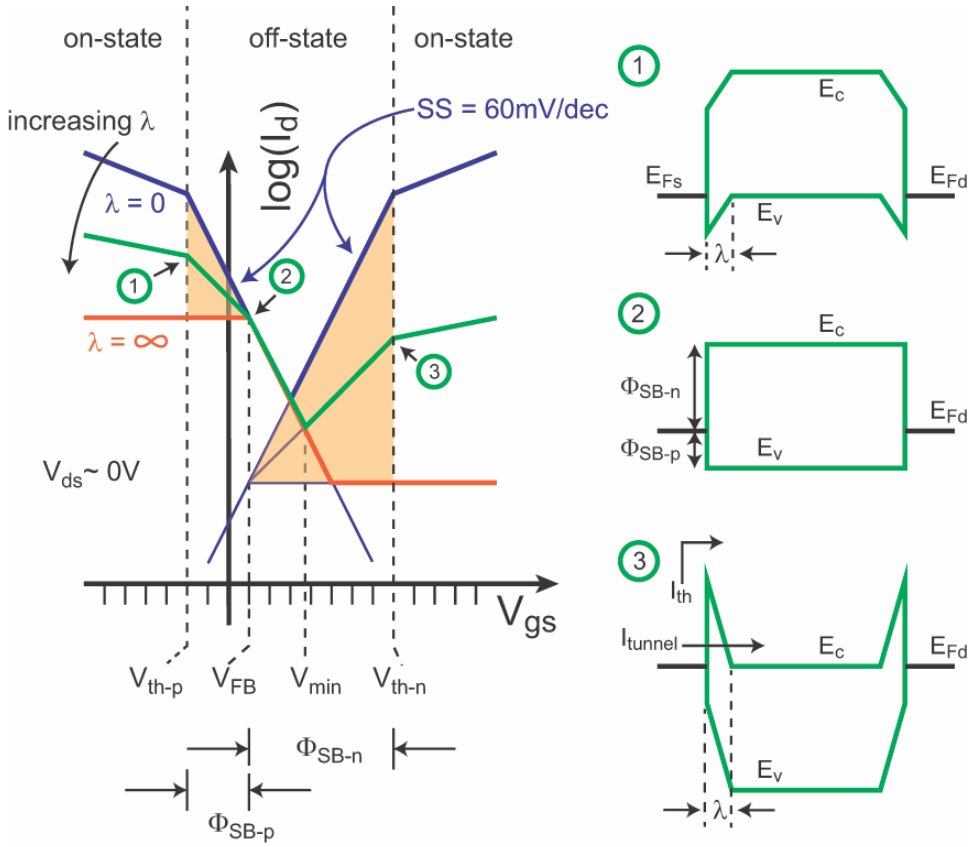


Figure 4.1. The construction of device characteristics at small voltages V_{ds} for different λ-values. The blue curve corresponds to $\lambda = 0$, while the orange curve would result for $\lambda = \infty$. (1) through (3) denote particular gate voltages with the respective band bending schematically shown on the right. Reprinted from P. Wu, J. Appenzeller, "Towards CMOS like devices from two-dimensional channel materials," *APL Materials* 13, 377–385 (2019), under a Creative Commons Attribution (CC BY) license.

Schottky barrier Φ_{SB-n} dominates in the device, defining SS within the range marked by the orange triangle on the right of the graph, depending as before on the exact value of λ. Note that the entire discussion above focused on the device off-state, which is why scattering in the channel that dominates in the on-state was not part of our consideration.

The goal to achieve one type of carrier injection *only* is thus intimately related to the question of how to suppress Schottky barrier injection of holes for an n-FET and injection of electrons for a p-FET. As stated above, *e.g.*, p-FET operation in CMOS requires negative gate and drain voltage polarities. Since the lateral electric field in the channel is positive

from source to drain for negative drain voltages, this implies that electron injection between $V_{min} < V_{gs} < V_{th-n}$ occurs from the drain side. For an n-FET, the undesirable hole injection also occurs from the drain, since operation is under positive drain voltages. This observation is key to designing devices that show unipolar characteristics, *i.e.*, only electron currents for n-FETs and hole currents for p-FETs.

Many approaches have tried to suppress either electron or hole carrier transport to recover unipolar device characteristics. Often this is done at the expense of on-current performance by using thick oxides [84]. For devices as shown in Fig. 4.1 with a Schottky barrier height that is substantially smaller (Φ_{SB-p} or $\Phi_{SB-n} < E_g/4$) for one carrier type than the other, increasing λ by using thick oxides indeed improves the on/off current ratio $I(V_{th-n-or-p})/I(V_{min})$ — compare, *e.g.*, the green and the blue characteristics. However, only n-FETs or p-FETs can be realized in this way for a given choice of metal source/drain electrodes that define Φ_{SB-p} and Φ_{SB-n}. Moreover, the thicker gate oxide that translates into a larger screening length λ harms the on-state current, since injection from the source beyond threshold is occurring by tunneling through a thicker barrier. Another approach is to leave the drain side of the device ungated [84], [85]. While this indeed suppresses drain injection, it results in highly nonlinear output characteristics $I_d - V_{ds}$ for low drain voltages. Carriers injected from the source cannot leave the channel on the drain side due to the thick tunneling barrier that is a result of an absent gating of the drain. An improved version of this design incorporates an additional gate at the drain side, which is tied to the drain electrode so that the drain injection is suppressed at zero gate-to-drain voltage V_{gd} [86]. However, in this feedback-gate design, the injection from the source is still affected by the additional gate at low V_{ds}, causing nonlinear output characteristics.

All of the above discussion is in general independent of the actual choice of channel material. The material properties become relevant only in that (i) the gate voltage range from V_{th-p} to V_{th-n} depends on the actual bandgap, (ii) the Schottky barrier heights depend on the combination of chosen metal source/drain electrodes and semiconducting channel, and (iii) the on-state current level itself, of course, depends on the achievable carrier concentration (determined by the density of states—DOS) and mobility of the chosen channel material.

4.3 Towards unipolar p- and n-type Schottky-barrier FETs

Different from the above described approaches, a device layout was presented at the Device Research Conference (DRC) 2018 [87] that combines (a) linear output characteristics ($I_d - V_{ds}$) with (b) high on-state currents and (c) unipolar transfer characteristics. To achieve this goal, a device with an asymmetric double gate (ADG) on top and underneath a black phosphorus flake had been built using source/drain metals with a preferred line-up closer to the valence band edge (p-FET) or conduction band edge (n-FET)—for details, see the next section. The key design feature is that while the respective oxides of the two gate stacks had both aggressively been scaled to an equivalent oxide thickness (EOT) of ∼3 nm, one of the two gates only partially covers the device channel and does not gate the drain region of the SB-FET. In addition, the choice of source/drain metal allows for the preferred injection of one carrier type. The impact of this type of gate layout in comparison with a fully double gated (DG) device structure is graphically illustrated in Fig. 4.2. Increasing the effective value of λ by removing one of the two gates entirely would change the device characteristics qualitatively from the set of green to the set of red curves as shown in Fig. 4.2(a). Different from Fig. 4.1, Fig. 4.2 also illustrates the drain voltage dependence. A negative drain voltage of $V_{ds} = -0.1$ V in comparison with a negative V_{ds}-value close to zero volts results in a shift of the electron branch (right side of device characteristics) toward negative gate voltages by exactly the amount of the applied drain voltage under the conditions assumed for this model. This is the case since the threshold voltage for electron injection from the drain has been altered by applying V_{ds} as is the flat band voltage on the drain side. Correspondingly, $V_{FB-d2}(V_{ds} = -0.1\ \text{V}) = V_{FB-d1}(V_{ds} \sim -0\text{V}) - 0.1$ V and $V_{th-n-d2}(V_{ds} = -0.1\ \text{V}) = V_{th-n-d1}(V_{ds} \sim -0\text{V}) - 0.1$ V. If, on the other hand, λ is kept small by using a double gate in the source region, while λ is made somewhat larger in the drain region by removing the impact of one of the two gates, on-currents of this particular p-FET are almost preserved, while the electron current from the drain is strongly suppressed. Fig. 4.2(b) illustrates how the double gated (DG) p-FET (green) compares with the new

asymmetric double gated (ADG) p-FET design presented here.[1] Applying the same scheme to a device with low work function source/drain metal contacts consequently results in an n-FET. Fig. 4.2(c) summarizes the outcome of this approach and illustrates how the same channel material displays the desired (almost) unipolar complementary (*i.e.*, n-type and p-type) device characteristics. Figs. 4.2(d) and 4.2(e) show the comparison of band diagrams of a p-type DG FET and a p-type ADG FET in the on-state and off-state, respectively. At the source side, the two types of FETs have the same λ and the on-currents remain almost unaffected. However, when a positive V_{gs} is applied to turn the devices off, a larger λ' in the ADG FET suppresses the electron injection from the drain, resulting in a smaller off-state current, as shown in Fig. 4.2(b). The operation of an n-type ADG FET can be understood in a similar fashion.

4.4 Experimental implementation

Following the above presented idea, this section discusses in detail the experimental implementation of unipolar p-type and n-type SB-FETs. Among various 2D materials, black phosphorus (BP) was chosen as a channel material due to its high mobility and moderate bandgap [7], [8]. The relatively small bandgap of BP enables both electron and hole injection in SB-FETs and facilitates the implementations of both p-type and n-type transistors, as neither of the Schottky barrier heights Φ_{SB-p} and Φ_{SB-n} is too large to block carrier injection. Therefore, BP transistors usually exhibit ambipolar characteristics, and complementary BP SB-FETs and circuits have been demonstrated in Ref. [88]. However, although BP SB-FETs are "blessed" with easier access to both the p-type and n-type branches and thus allow for implementation of complementary transistors, they are also "cursed" with significant ambipolar behavior and thus low I_{ON}/I_{OFF} ratios. In the following, the problem posed by ambipolar branches is further illustrated using a more concrete example of a complementary BP double-gate (DG) FET. Next, the ADG-FET design is introduced to resolve this issue to achieve unipolar characteristics as well as high I_{ON}/I_{OFF} ratios.

[1]↑Note that on a linear scale currents for the DG FET and ADG are not identical for small drain voltages since the drain barrier still effects current transport when scattering is present in the channel.

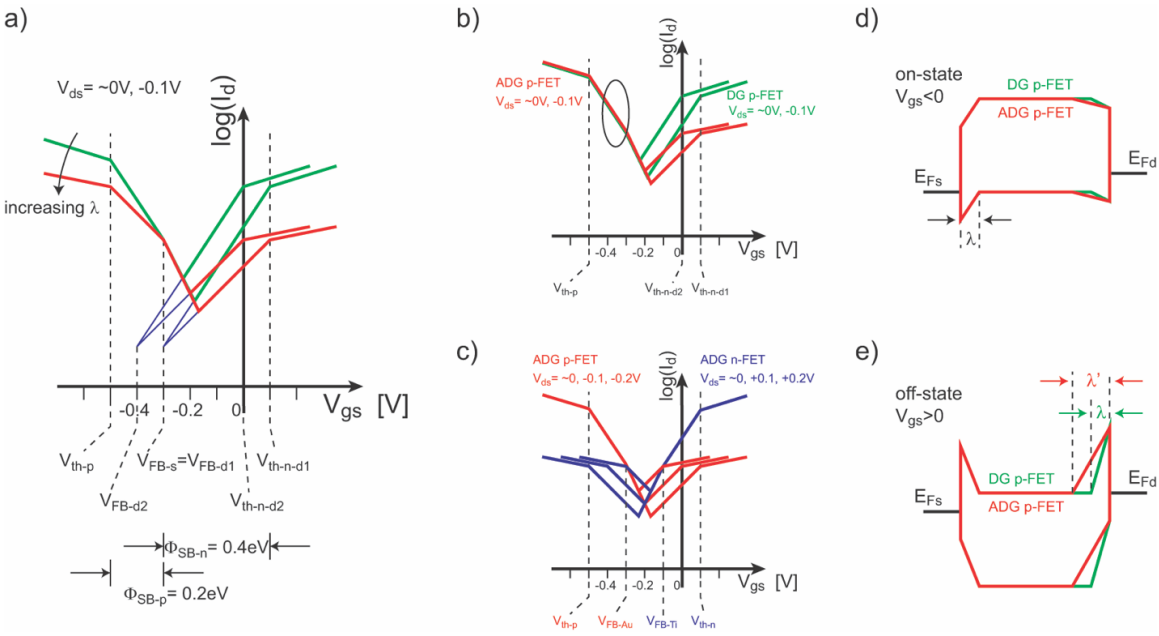


Figure 4.2. (a) Construction of ambipolar device characteristics as in Fig. 4.1, but for two drain voltages, showing a shift of the electron branch for negative drain voltages. Green vs red captures a uniform change of λ, *e.g.*, by changing from a double gated to a single gated structure. (b) Improvement of device characteristics from the asymmetric double gate design by suppressing the electron injection from the drain without sacrificing on-state performance. (c) The expected outcome for a properly designed n-type and p-type ADG FET exhibiting the desired unipolar device characteristics. (d) Band diagrams of a p-type DG FET and a p-type ADG FET in the on-state. (e) Band diagrams of a p-type DG FET and a p-type ADG FET in the off-state. Reprinted from P. Wu, J. Appenzeller, "Towards CMOS like devices from two-dimensional channel materials," *APL Materials* 13, 377–385 (2019), under a Creative Commons Attribution (CC BY) license.

Fig. 4.3(a) shows the device structure of a BP DG-FET. A BP flake was transferred onto the bottom gate (BG), composed of 2 nm Ti as gate metal and 0.8 nm Al seeding layer plus 4 nm Al_2O_3 grown by atomic layer deposition (ALD) as gate dielectric. Then, 40 nm Ti or 1.5 nm/40 nm Cr/Au were evaporated and patterned as source/drain metal contacts for the n-FET and the p-FET, respectively. Another 0.8 nm Al seeding layer and 4 nm ALD-grown Al_2O_3 were deposited on top of BP as top-gate (TG) dielectric, followed by evaporation and patterning of 40 nm Ti as TG metal. The BG and TG are electrically connected to form

a double-gate structure (the gate voltage V_{gs} is applied to both TG and BG). Fig. 4.3(b) shows a representative false-colored SEM image of a BP DG-FET.

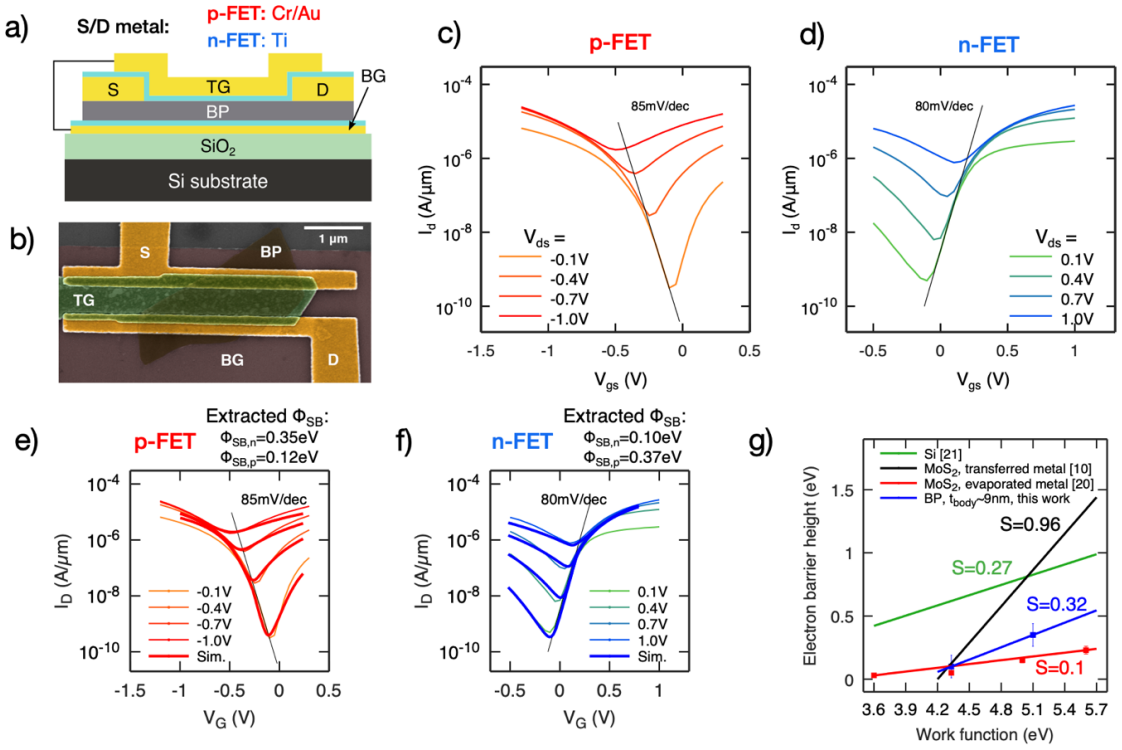


Figure 4.3. (a) Device structure of a BP DG-FET. (b) False-colored SEM image of a BP DG-FET. (c) Transfer characteristics of a BP DG p-FET. (d) Transfer characteristics of a BP DG n-FET. (e) Experimental and simulated characteristics of a p-type BP FET and the extracted barrier heights. (f) Experimental and simulated characteristics of an n-type BP FET and extracted barrier heights. (g) Schottky barrier heights vs metal work function in various metal-semiconductor systems. The data for Si and MoS_2 are derived from Refs. [81], [4], and [89]. Reprinted from P. Wu, J. Appenzeller, "Towards CMOS like devices from two-dimensional channel materials," *APL Materials* 13, 377–385 (2019), under a Creative Commons Attribution (CC BY) license.

As described in the last section, source/drain metal contacts with different work functions are employed to tune the Schottky barrier heights Φ_{SB-p} and Φ_{SB-n} in favor of one particular type of carrier injection from the source, *i.e.*, a low work function metal like Ti favors electron injection in an n-FET, while a high work function metal such as Cr/Au favors hole injection in a p-FET. Figs. 4.3(c) and 4.3(d) show the transfer characteristics of a p-type BP DG-FET and an n-type BP DG-FET, respectively. It is apparent from the high respective on-

current levels that the metal work function engineering is effective and that complementary operation is achieved for the same gating scheme in BP FETs. In addition, thanks to the strong gate control from the double-gate structure, both the p-FET and the n-FET show steep SS values of 85 mV/dec and 80 mV/dec, respectively. Figs. 4.3(e) and 4.3(f) show fits of transfer characteristics obtained for the p-type BP DG-FET and the n-type BP DG-FET employing the Schottky barrier model from Ref. [8] to extract the respective Schottky barrier heights. The extracted Schottky barrier heights are Φ_{SB-p} = 0.12 eV and Φ_{SB-n} = 0.35 eV for Cr/Au contacts, and Φ_{SB-p} = 0.37 eV and Φ_{SB-n} = 0.1 eV for Ti contacts, respectively. Fig. 4.3(g) shows the Schottky barrier heights for electrons vs metal work function in various semiconductors, including MoS_2 [4], [81], Si [89] and BP. Due to metal-induced gap states, the Schottky barrier heights of metal-semiconductor junctions do not follow the ideal Schottky-Mott rule, which predicts the Schottky barrier height for electrons to increase linearly with the metal work function exhibiting a slope of 1. Instead, an effect referred to as Fermi-level pinning arises [81], [89], causing the Schottky barrier heights to increase with metal work function with a slope much smaller than 1, as shown by the green line (Si, S = 0.27) and the red line (MoS_2, S = 0.1) in Fig. 4.3(g). A recent discovery shows that by transferring metal contacts onto MoS_2 instead of direct metal evaporation, an excellent metal-semiconductor interface quality can be achieved and the gap states can be eliminated, approaching the Schottky-Mott limit (S = 1) [81], as shown by the black line (S = 0.96) in Fig. 4.3(g). Fig. 4.3(g) also shows the data extracted from Figs. 3(e) and 3(f) assuming a Ti work function value of WF = 4.33 eV and a Cr/Au value of WF = 5.1 eV. Note that we assumed here that the 1.5 nm thin Cr adhesion layer does not change the work function of the Cr/Au stack to be different from Au. From our data, two important conclusions can be drawn (1) Fermi level pinning is indeed present in our metal-BP junctions, as apparent from the blue line (S = 0.32) in Fig. 4.3(g), and (2) despite the Fermi level pinning, work function engineering of the metal contacts is sufficiently effective to enable low barriers for electron injection (Ti, Φ_{SB-n} = 0.1 eV) and hole injection (Cr/Au, Φ_{SB-p} = 0.12 eV) in n-type and p-type BP FETs, respectively.

While we have in this way achieved complementary BP FETs using contact work function engineering, the still existing ambipolar branches caused by drain injection are severe for both

FETs and result in low I_{ON}/I_{OFF} ratio, especially at high drain biases [compare Fig. 4.2(a)]. Transistors with high I_{ON}/I_{OFF} ratios are essential to achieve low static power consumption and a full output swing for CMOS circuits, which requires modification of the above device layout. The solution lies in designing an asymmetric double gate (ADG) FET structure.

We have demonstrated complementary BP ADG-FETs with nearly unipolar characteristics and high I_{ON}/I_{OFF} ratios during the Device Research Conference (DRC) in 2018 [87]. Fig. 4.4(a) presents the device structure of a BP ADG-FET, in comparison with a DG-FET. In the ADG-FET, the BG is placed overlapping with only the source contact and part of the BP channel. The drain side of the FET remains ungated by the bottom gate, while the TG covers the entire channel. The process flow of fabricating an ADG-FET is similar to that of a DG-FET, with the only difference being that the drain electrode is placed outside of the BG region. Fig. 4.4(b) shows a false-colored SEM image of a BP ADG-FET. By introducing the underlap of BG with respect to the drain in the ADG-FET, the impact of BG is eliminated on the drain side of the device, and thus the effective value of λ is made larger for the drain injection than for the source injection. As discussed in the last section and shown in Fig. 4.2(b), this approach is expected to suppress the drain injection while preserving the source injection, resulting in higher I_{ON}/I_{OFF} ratios and almost unipolar characteristics.

The experimental outcome of the ADG-FET approach is shown by the transfer characteristics of a p-type and an n-type BP ADG-FET in Fig. 4.4(c). The ambipolar branches are substantially suppressed as expected from our analysis, and almost unipolar p-type and n-type FETs are achieved, with significantly improved I_{ON}/I_{OFF} ratios if compared to the BP DG-FETs. Moreover, the p-type and n-type BP ADG-FETs exhibit steep SS values of 78 mV/dec and 88 mV/dec, respectively, underlining the strong gate control of the double-gate structure. Fig. 4.4(d) shows the output characteristics of the p-type and n-type BP ADG-FETs. Both types of ADG-FETs show rather linear output characteristics at low V_{ds} values, as the drain side of the device is still gated by the TG, which is an improvement over the highly nonlinear output characteristics of the device structure in Refs. [84] and [85], where the drain side is ungated. Moreover, both types of FETs exhibit high ON-current values of $\sim$100 μA/μm at $|V_{ds}| = 1.2$ V, owing to the proper engineering of the source/drain contact metal work functions, which impact the Schottky barrier heights Φ_{SB-p} and Φ_{SB-n} for hole

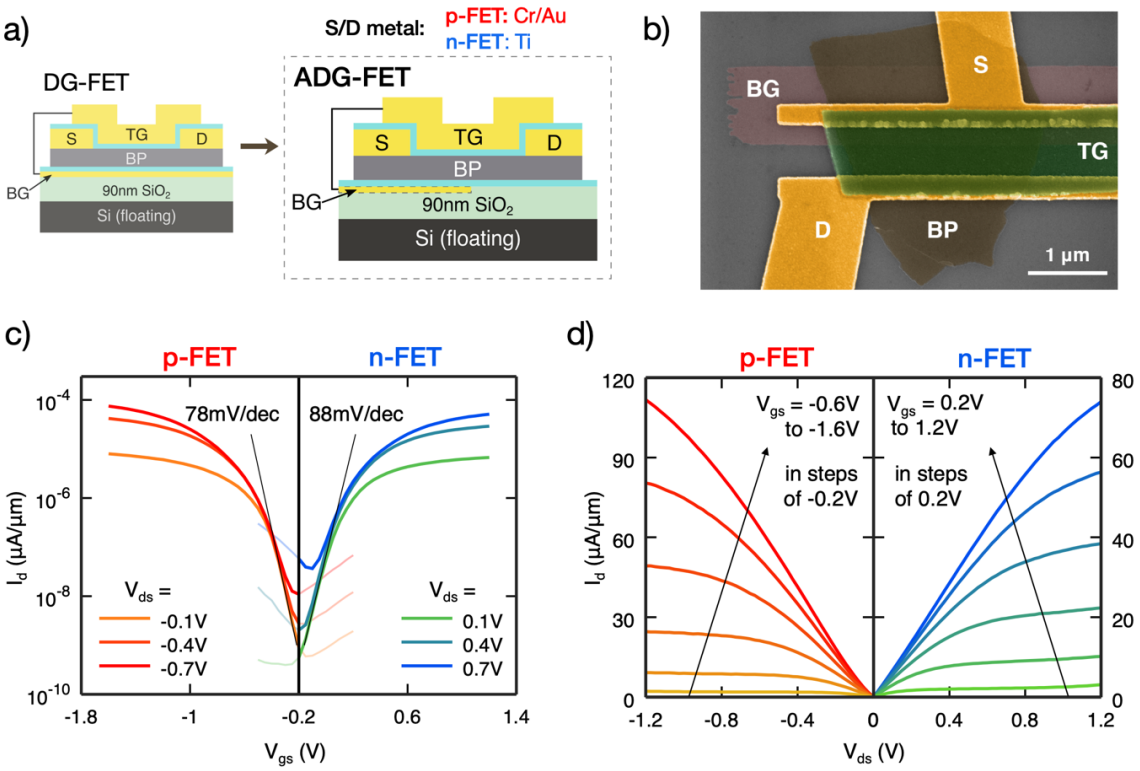


Figure 4.4. (a) Device structure of a BP ADG-FET, in comparison with a BP DG-FET. (b) False-colored SEM image of a BP ADG-FET. (c) Transfer characteristics of a p-type and an n-type BP ADG-FET. (d) Output characteristics of a p-type and an n-type BP ADG-FET. Reprinted with permission from P. Wu, J. Appenzeller, *IEEE Device Research Conference* (IEEE, 2018). Copyright 2018 IEEE.

and electron injections as described above. Also note that current saturation is observed for both types of ADG-FETs in the output characteristics as expected for properly designed scaled devices with both gate and drain voltages in the ∼1 V range.

4.5 Circuit demonstration

Based on the complementary BP ADG-FETs discussed in the last section we next demonstrate a simple CMOS circuit — an inverter [87]. Figs. 4.5(a) and 4.5(b) display the schematic and a false-colored SEM image of an inverter built from a p-type BP ADG-FET and an n-type BP ADG-FET in which the p-FET and the n-FET are fabricated on the same BP flake.

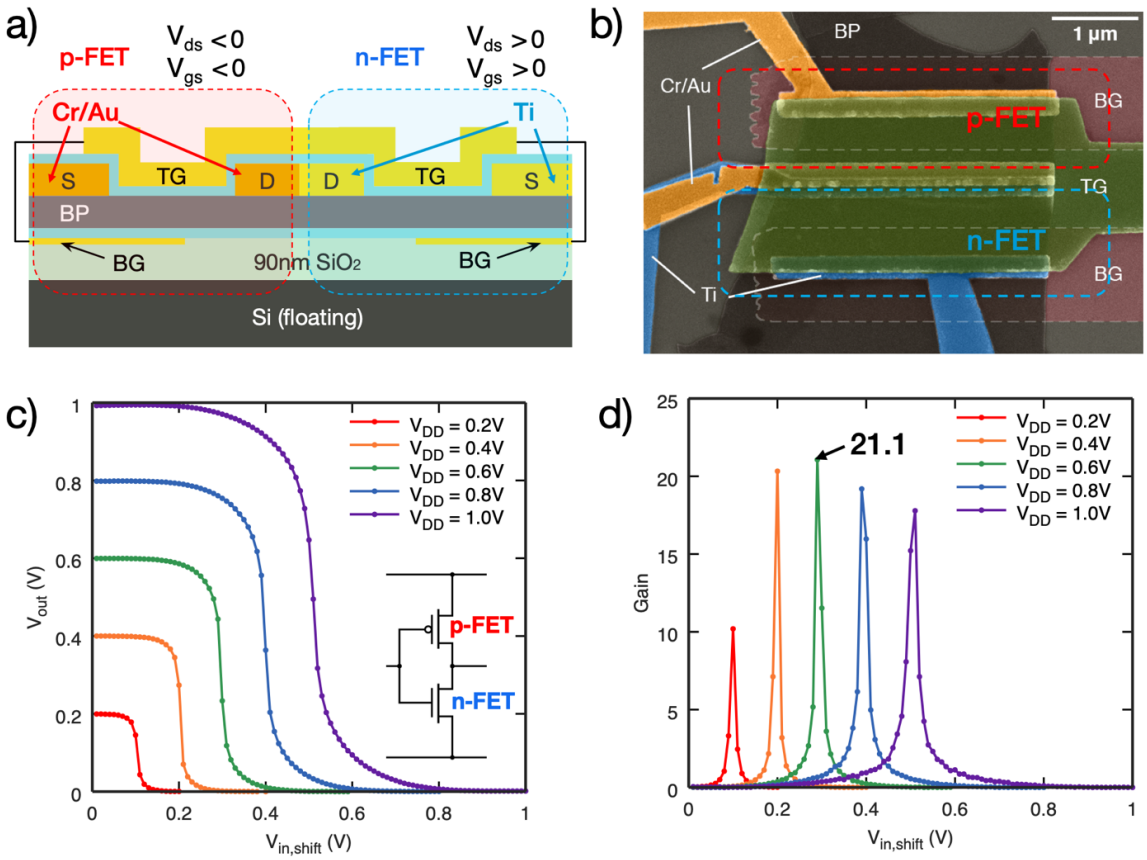


Figure 4.5. (a) Structure of a BP inverter built from complementary BP ADG-FETs. (b) False-colored SEM image of the BP inverter. (c) Voltage transfer characteristics of the BP inverter at different supply voltages V_{DD}. Inset: circuit diagram of the inverter. (d) Gain of the BP inverter at different supply voltages V_{DD}. Reprinted with permission from P. Wu, J. Appenzeller, *IEEE Device Research Conference* (IEEE, 2018). Copyright 2018 IEEE.

As evident from the voltage transfer characteristics [Fig. 4.5(c)] and gain [Fig. 4.5(d)] of the inverter at different supply voltages V_{DD}, excellent performance specs have been achieved, thanks to the high performance of the individual BP FETs as shown in Figs. 4.4(c) and 4.4(d) in the last section. A number of aspects are worth noting: First, the inverter is fully operational even at V_{DD} values as low as 0.2 V, since the individual p-FET and n-FET have steep subthreshold slopes and the input voltage range required to turn on and off the devices is small. Second, a full output swing from V_{DD} to 0 is obtained, since unipolar characteristics were successfully achieved by suppressing the drain injection by employing the above described ADG-FETs. The key is that both the n-FET and the p-

FET can be turned off effectively when the input is 0 or V_{DD}. Finally, the inverter exhibits a very high gain of 21.1 at V_{DD} = 0.6 V, and even at the lowest supply voltage of V_{DD} = 0.2 V, a peak gain of 10.2 is still retained. This high gain of the inverter is a result of the relatively high output resistances of the BP ADG-FETs in their respective saturation regions [75], as depicted in Fig. 4.4(d).

It is worth noting that since the transfer characteristics of the p-FET and the n-FET are symmetrical with respect to a nonzero gate voltage, *i.e.*, $V_{gs} = -0.2$ V, as shown in Fig. 4.4(c), the input voltage has been shifted in Figs. 4.5(c) and 4.5(d) by 0.2 V, *i.e.*, $V_{in,shift} = V_{in} + 0.2$ V to compensate for the mismatch of threshold voltages of the p-FET and the n-FET. This problem can be resolved by various threshold voltage tuning schemes to shift the voltage back to zero, such as gate metal work function tuning and interface dipole engineering [90].

4.6 Conclusion

In this chapter, we have demonstrated some recent efforts of demonstrating CMOS-like devices using 2D materials. Starting from a review of the operation principle of Schottky barrier field-effect transistors, ambipolar current injection in transistors made from 2D channels has been carefully discussed. A recently demonstrated device structure, *i.e.*, an ADG-FET has been presented to suppress ambipolar device characteristics effectively and has been implemented in n-type and p-type black phosphorus FETs and a CMOS inverter circuit. Our work may provide guidance to the design of future generations of 2D materials' based devices and logic circuits.

5. TWO-DIMENSIONAL TRANSISTORS WITH RECONFIGURABLE POLARITIES FOR HARDWARE SECURITY

Security is a critical aspect in modern circuit design, but research into hardware security at the device level is rare as it requires modification of existing technology nodes. With the increasing challenges facing the semiconductor industry, interest in out-of-the-box security solutions has though grown, even if this implies introducing novel materials such as two-dimensional (2D) layered semiconductors. In this chapter, we show that high-performance, low-voltage 2D black phosphorus field-effect transistors (FETs) that have reconfigurable polarities are suitable for hardware security applications. The transistors can be dynamically switched between p-FET and n-FET operation through electrostatic gating, and achieve on-off ratios of 10^5 and subthreshold swings of 72 mV/decade at room temperature. Using the transistors, we create inverters that exhibit gains of 33.3 and are fully functional at V_{DD}=0.2 V. We also create a security primitive circuit with polymorphic NAND/NOR obfuscation functionality with sub-1V operation voltages; the robustness of the polymorphic gate against power supply variations is tested using Monte Carlo simulations.

5.1 Introduction

Two-dimensional (2D) materials, such as transition metal dichalcogenides (TMDs) [4], [5], [34] and black phosphorus (BP) [7]–[9], [38], [62], are of interest as channel material for transistors [37], [91], [92], since their atomic thickness could allow scaled devices to be created that extend Moore's Law beyond the capabilities of silicon [1], [93], [94]. However, research in the field typically focuses on demonstrating operations that are also achievable with traditional transistors, and efforts to try to leverage the unique properties of 2D materials, such as ambipolarity, to deliver new functionalities are rather.

In a complementary metal-oxide-semiconductor (CMOS) digital logic circuit, the functionality of each building block is implemented by a pull-up network composed of p-type field-effect transistors (FETs), and a pull-down network composed of n-type FETs [75]. The connections of the two networks follow De Morgan's Law [75] so that the two networks will turn on and off alternatively, connecting the output node to either V_{DD} or ground. However, since the polarities of traditional Si CMOS transistors rely on substitutional doping of the source/drain and channel regions, it is not possible to modify their n-type or p-type character post-fabrication. Thus, a hypothetical adversary could easily retrieve the layout of an integrated circuit (IC) chip through various reverse engineering techniques, such as transmission electron microscopy (TEM) [95] and X-ray imaging [96], [97], and thus decipher the functionality of the chip.

In contrast, transistors based on 2D semiconductors typically rely on carrier injection through Schottky barriers at source/drain metal-semiconductor interfaces [8], [30], [89], [91], [93] and are inherently ambipolar: that is, both electron and hole injection is possible and can be tuned via gating[1]. Therefore, through a proper choice of material properties and careful engineering of the device structures, transistors with reconfigurable polarities can be realized using 2D materials [31], [98]–[101], making identification of the functional properties of the circuit more difficult. In this chapter, we show how the ambipolarity and general properties of transistors based on 2D materials makes them ideal for use in hardware-based security applications. In particular, we fabricate high-performance black phosphorus (BP) FETs with reconfigurable polarities and demonstrate their application in secure circuits.

5.2 Polymorphic gates for logic locking and IC camouflaging

By using reconfigurable transistors, hardware security can be achieved in integrated circuits (Fig. 5.1). In the proposed secure circuit layout, the standard cell circuits are implemented using polymorphic logic gates [29], [102]–[104]. Polymorphic gates exhibit bi-fold functionality when all p-FETs become n-FETs and all n-FETs become p-FETs as selected by a key bit. This is achieved by reversing the role of the V_{DD} and GND rails. (The green

[1]↑Note that low-dimensional systems in general allow for effective carrier injection due to their ultra-thin body that translates into a small geometric screening length [83]

boxes in Fig. 5.1 illustrate a NAND/NOR polymorphic gate as an example, where the roles of two pull-up and two pull-down transistors are reversed by changing the polarity of V_{DD} and GND.) Even if a hypothetical adversary were able to map out the entire layout of the chip, without the correct key the functionality of the chip would still be hidden as the individual functionalities of the cell circuits are still unknown (grey box, Fig. 5.1). The entire chip will also only be functional if all the correct key bits are provided during run-time to set the logic gates into their correct functions. These approaches illustrate two hardware security techniques that can be achieved with polymorphic gates, *i.e.*, logic locking and IC camouflaging [103], [104].

The goal of logic locking is to "modify the behaviour of ICs in such a way that they do not produce expected outputs unless they are properly activated using a new primary input, the secret key" [105]. A common technique for locking the functionality of a circuit consists of inserting XOR gates or multiplexers in strategic nodes of a circuit [106], [107]. These gates have one of their inputs as a key bit, which has to be a certain value ('0' or '1') in order for the circuit to work correctly. Logic locking with polymorphic gates is enabled by the key bit that grants one of the two possible functionalities to the logic gate. To enable logic locking with an acceptable security level, a number of standard cells in a circuit are replaced by their equivalent polymorphic gates. Quantitatively, in terms of transistor count overhead, polymorphic gate-based logic locking does not incur additional overhead to a circuit. In contrast, alternative techniques [106], [107] require at least $8N$ additional transistors to be implemented, where N is the number of bits of the key used.

IC camouflaging is defined as "a layout-level technique that hampers imaging-based reverse engineering by using, in one embodiment, functionally different standard cells that look alike" [108]. Previous works have exploited obfuscation cells to achieve IC camouflaging. Obfuscation cells are made possible by techniques such as the use of dummy contacts [109] and dopant polarity [110], [111] that enable distinct functions within the same cell structure. The obfuscation cells are placed in a layout along with regular standard cells. IC camouflaging with polymorphic gates relies on the fact that the same physical cell layout can provide two distinct functionalities that cannot be guessed by looking at the layout. When using polymorphic gates, IC camouflaging can be achieved without using additional gates as

a single gate can assume different functions [104]. In comparison, "Obfusgates" [111] uses many obfuscation cells placed alongside regular standard cells to achieve equivalent security, and as a case study, the obfuscation of AES S-Box circuit (which consists of look-up tables) using 2-input NAND "Obfusgates" demands 154% of the number of original gates in the circuit [111].

Both logic locking and IC camouflaging can be achieved with polymorphic gates without using additional transistors in the circuit. However, realization of polymorphic gates relies on access to reconfigurable FETs which can be dynamically tuned into p-type or n-type during run-time (purple box, Fig. 5.1).

5.3 Schottky-barrier FETs for reconfigurable operation

Since the reconfigurability of a 2D transistor relies on the Schottky-barrier injection, it is informative to study the operation of a Schottky-barrier FET (SB-FET) to find the optimal device structure and material properties to realize such reconfigurable 2D FETs. Fig. 5.2(a) shows a typical structure of a SB-FET with 2D channel and the impact of bandgap E_g on the device performance. In a SB-FET, the on-current levels of p- and n-branch depend on the corresponding Schottky barrier heights, $\Phi_{SB,p}$ and $\Phi_{SB,n}$. To ensure symmetric current levels between two branches as required in a reconfigurable FET, it is desirable to have a mid-gap Fermi level line-up at the metal-semiconductor contact, *i.e.*, $\Phi_{SB,p} \sim \Phi_{SB,n} \sim E_g/2$. Since the current injection is dominated by tunneling through Schottky-barriers [I_{tunnel}, as illustrated by the band diagrams in Fig. 5.2(a)] the on-current I_{on} can be related to the barrier heights, and thus bandgap E_g, using Wentzel–Kramer–Brillouin (WKB) approximation [27]:

$$I_{ON} \sim \exp\left(-\frac{4\lambda\sqrt{2m^*\Phi_{SB}}}{3\hbar}\right) \approx \exp\left(-\frac{4\lambda\sqrt{2m^*(E_g/2)}}{3\hbar}\right)$$

where m^* is the effective mass of holes (electrons) for the p (n) branch, respectively, and λ is the geometric screening length [30]. Therefore, a channel material with a small bandgap E_g and small effective masses m^* is desirable for a reconfigurable SB-FET to achieve higher I_{on}.

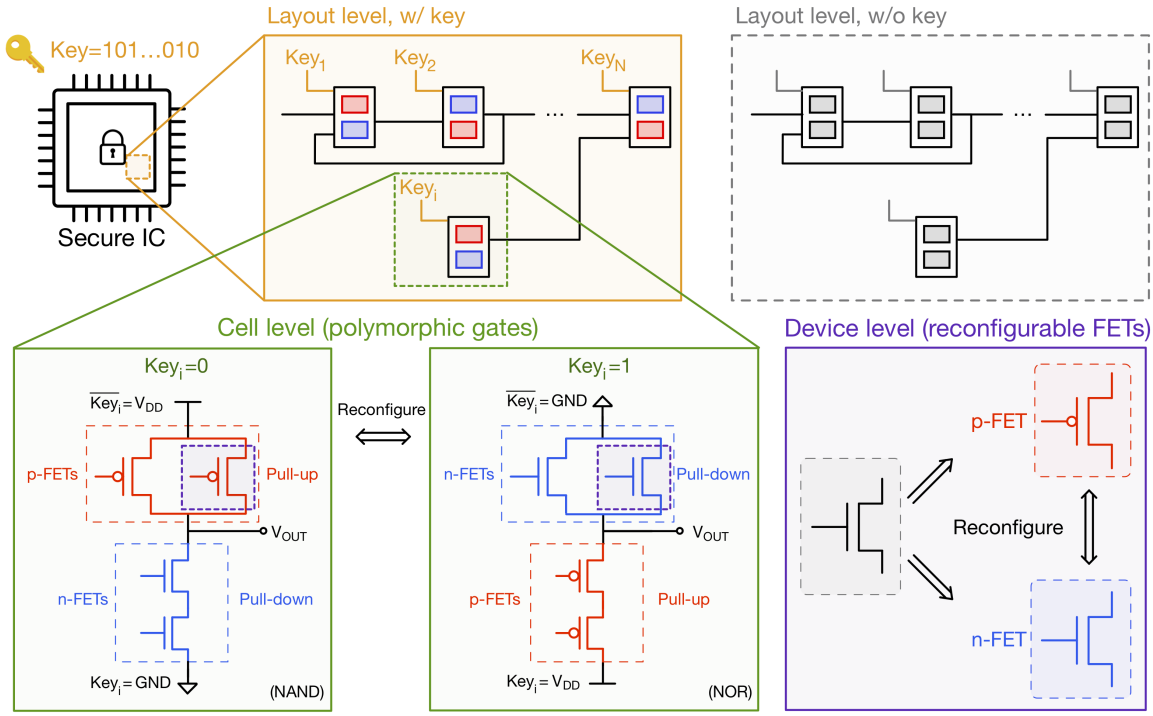


Figure 5.1. Schematic of a secure chip enabled by reconfigurable FETs. The standard cells of the secure chip are implemented using polymorphic gates, and the functionality of each cell is bi-fold when all p-FETs become n-FETs and all n-FETs become p-FETs, as selected by a key bit (green box). Without the correct key, the chip will not be functional (logic locking), nor can an outside attacker decipher the functionality of the chip through reverse engineering (IC camouflaging). To implement such secure chips, transistors with reconfigurable p-type and n-type polarities are required (purple box). Credit: padlock icon, © Evil Icons 2020; key icon, © 2017 ThemeIsle. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

Apart from higher I_{on}, another reason for using a small bandgap material is to achieve low-voltage operation. As illustrated in the $I_d - V_g$ characteristics and the corresponding band diagrams in Fig. 5.2(a), even if we assume a perfect gate control and an ideal one-to-one band movement with the gate voltage, the threshold voltages of the p- and n-branches, $V_{th,p}$ and $V_{th,n}$, are spaced by E_g/q. In previous attempts to achieve reconfigurable SB-FETs, materials with relatively large bandgap, such as Si nanowires [112]–[114] ($E_g \sim 1.1$ eV), WSe_2 [101] ($E_g \sim 1.8$ eV) and $MoTe_2$ [98], [100], [115] ($E_g \sim 1.1$ eV) were employed as channel

materials. Therefore, even with the best oxide possible, V_{th} cannot be scaled down to less than $E_g/2q$, which hinders reduction of the operation voltage of the device. In traditional CMOS devices, this issue can be resolved by employing gate metals with different work functions for the p-FETs and n-FETs, namely, a high work function metal for the p-FETs and a low work function metal for the n-FETs [116]. However, this approach is not allowable for reconfigurable FETs, since the p-FETs and n-FETs are interchangeable in the proposed secure circuit setup and must share the same device structure and thus the same gate metal. Therefore, the only option to scale down V_{th} is through adopting channel materials with a small E_g.

On the other hand, choosing a material with a "too small bandgap" is also prohibitive. While the previous discussion only considered the injection from the source, one also needs to consider drain injection and the corresponding ambipolar current branch and its impact on the off-state current I_{off}, as illustrated in Fig. 5.2(b). As an example, next the reconfigurable FET in the n-FET mode is analyzed. Note that the argument for the p-FET mode is similar when considering the proper reversal of gate and drain voltage polarity.

As illustrated by the $I_d - V_g$ characteristics and the corresponding band diagrams in Fig. 5.2(b), in the off-state of the n-FET mode ($V_g = 0, V_{ds} > 0$), the hole injection from drain is enabled because the gate is negative relative to the drain, *i.e.*, $V_{gd} = V_g - V_d < 0$. Since the ambipolar drain injection is modulated by V_{gd}, the p-branch shifts to the right by V_{ds} compared to the case when V_{ds} is near zero and shows very similar n-branch behavior at a somewhat higher on-current level, causing an increased I_{off} and reduced on-off current ratio, as shown in Fig. 5.2(b). This situation is alleviated by a large bandgap, since the p- and n-branches are spaced further apart (by an amount of E_g/q, assuming a perfect gate control) such that after shifting to the right by an amount of V_{ds}, the ambipolar branch does not affect the off-state current as much.

5.4 Reconfigurable black phosphorus FETs

From the above discussion it is clear that satisfying on- and off-current requirements simultaneously is not achievable – materials with a small bandgap are more desirable for

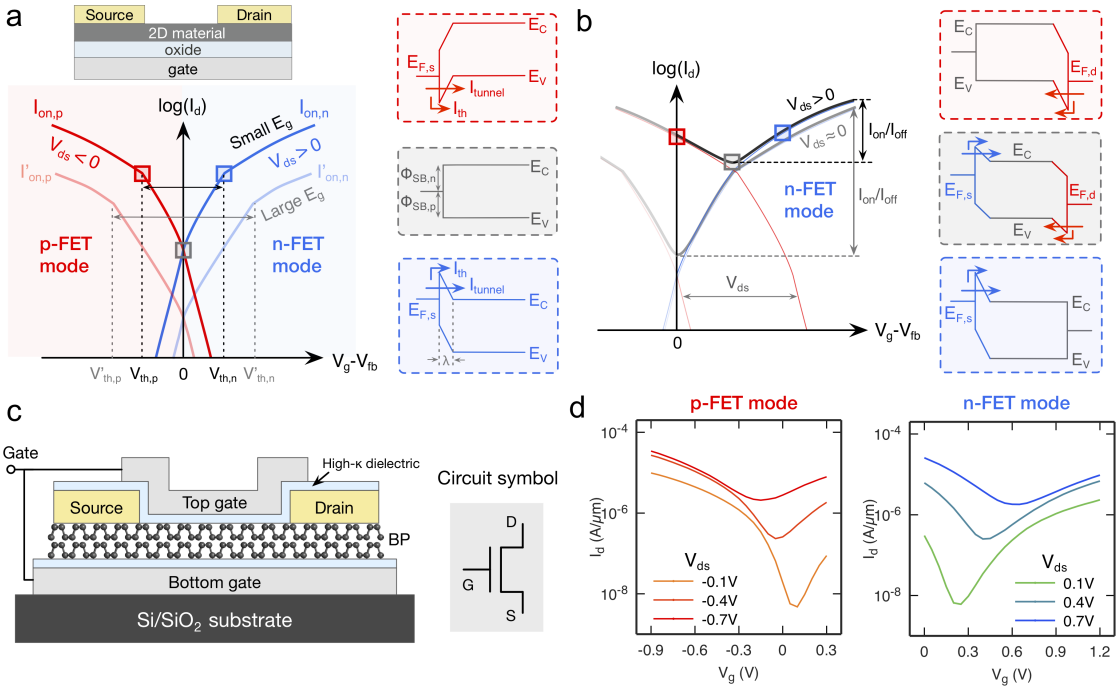


Figure 5.2. Design consideration for reconfigurable Schottky-barrier FET. (a) Schematic of a Schottky-barrier FET with 2D channel and the impact of bandgap on the device performance of a reconfigurable SB-FET with mid-gap Schottky barriers. (b) Impact of drain injection on the on-off ratio of a SB-FET in the n-FET mode. (c) Device structure of a double-gate BP SB-FET. (d) Transfer characteristics of the BP SB-FET in the p-FET and n-FET modes. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

higher on-state currents and lower operation voltages, yet the on-off ratio will be deteriorated. To illustrate the severity of the problem, black phosphorus (BP) SB-FETs, as shown in Fig. 5.2(c) were fabricated. BP has been studied intensively for transistor applications [7], [9], [38] due to its small bandgap [8], [58], [117] (0.3 eV to 2 eV, depending on thickness) and low effective mass [58] (0.15 m_0), all of which are desirable for reconfigurable FETs. The thicknesses of BP channels in this study range from 5 nm to 16 nm, and the corresponding E_g values range from 0.35 eV to 0.7 eV. In our experiment Cr/Au metal stacks were chosen as source/drain contacts to BP due to this stack's mid-gap Fermi level line-up enabling both electron and hole injections [9], [30]. A tight gate control of the channel is ensured through

a double-gate structure formed by a bottom gate (BG) and a top gate (TG), which are electrically connected as the gate (G) terminal, as well as a thin high-κ gate dielectrics (see Methods). Fig. 5.2(d) shows transfer characteristics of a representative BP SB-FET in the p-FET and n-FET modes. Clearly, both hole and electron branches can be enabled in the p-FET and n-FET modes, respectively, due to the near mid-gap Fermi level alignment of Cr/Au contacts combined with an observed doping effect due to the Al_2O_3 dielectric film (see Section 5.9.1). Low-voltage operation is achieved due to the small bandgap of BP that – together with the strong gate control resulting from the double-gate structure and the thin gate dielectrics – results in small V_{th} values of the BP SB-FET. Also clearly visible, however, is the strong deterioration of the on-off current ratio at large V_{ds} for both p-FET and n-FET modes as expected. Though the on-off current ratio degradation in ambipolar Schottky-barrier transistors has also been identified in previous work [118]–[120], it becomes even more important for reconfigurable transistors, since a mid-gap Fermi level line-up is required and shifting the Fermi level closer to the conduction band for n-FETs or valence band for p-FETs does not provide a solution.

To address this severe problem, we propose here a novel device structure to achieve a high on-off current ratio in a reconfigurable FET with a small bandgap material without changing the design between an n-FET and a p-FET. [2]

Fig. 5.3(a) shows the schematic of the proposed structure of a reconfigurable BP transistor. Compared to the structure shown in Fig. 5.2(c), a polarity gate (PG) overlapping with the drain electrode is introduced in the new structure to suppress the undesired ambipolar current branch from drain injection, while allowing the desired current branch from source injection to pass, thus setting the device into a particular polarity. Fig. 5.3(b) shows a false-colored scanning electron microscopy (SEM) image of a reconfigurable BP FET. Fig. 5.3(c) shows the transfer characteristics of a reconfigurable BP transistor in the p-FET mode and the n-FET mode. Note that the two sets of curves are obtained from the same device in different operation modes. The device exhibits steep subthreshold swings (SS) of 75 mV

[2]↑Different from Ref. [30], here we are using the same source/drain metal contact stacks and have added a polarity gate that ensures suppression of the undesired branch. Note that a device structure with reconfigurable operation and improved on-off current ratios has been previously demonstrated [62], but did not give rise to the same quality of gate control nor allowed for the scaled voltage operation achieved here.

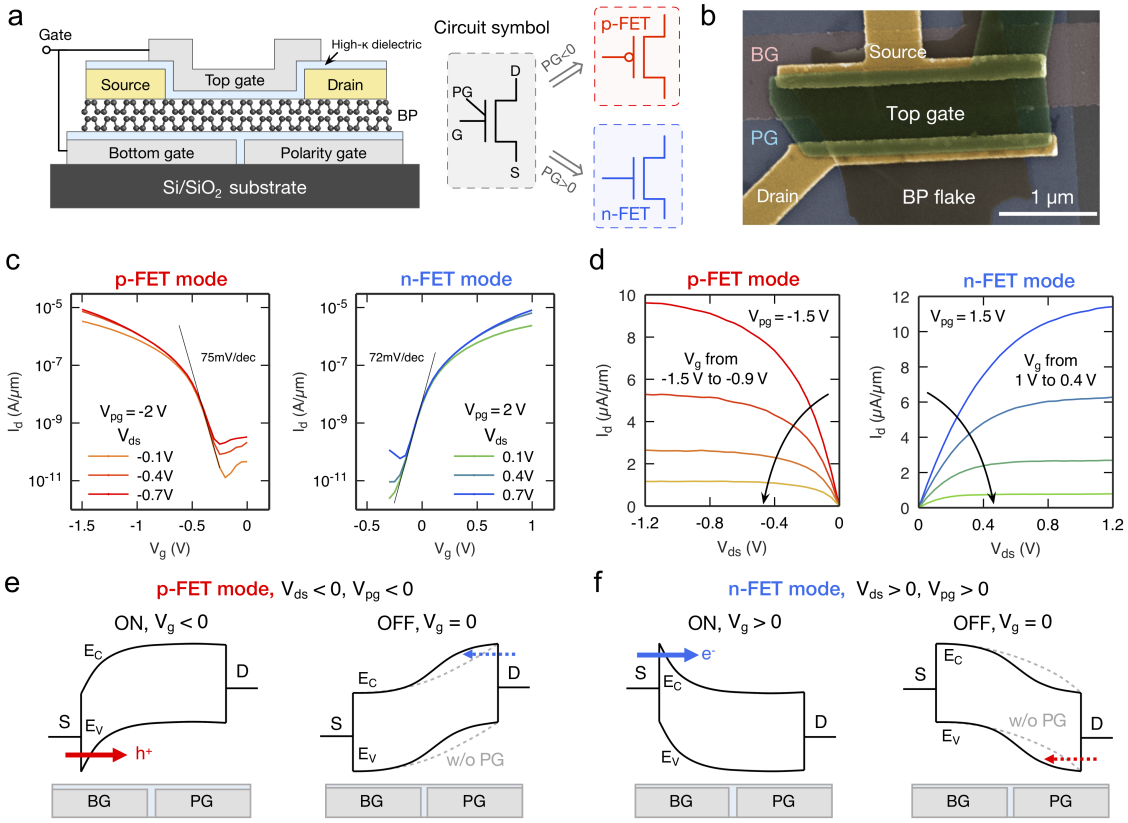


Figure 5.3. Black phosphorus transistors with reconfigurable polarities. (a) Schematic of the reconfigurable BP transistor with polarity gate. (b) Scanning electron microscopy image of a reconfigurable BP transistor (BG and PG stand for bottom gate and polarity gate, respectively). (c) Transfer characteristics of a reconfigurable BP transistor in the p-FET mode and n-FET mode. (d) Output characteristics of the transistor in the p-FET mode and n-FET mode. (e-f) Energy band diagrams of the transistor in the on-state and off-state of the (e) p-FET mode and (f) n-FET mode. The dashed lines illustrate the energy bands and corresponding drain injection current paths without polarity gate, which lead to higher I_{off}. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

per decade and 72 mV per decade in the p-FET and n-FET modes, respectively, and a high on-off current ratio of 10^5 in each operation mode at $V_{ds} = \pm 0.7$V, underlining the strong gate control and successful suppressing of the undesired ambipolar current injection. The on-current levels are around 10 μA/μm at low drain and gate voltages of $V_{ds} = \pm 0.7$V and

$V_g - V_{fb} = \pm 1.2$V, which are reasonably high considering the long channel length of $\sim$1 μm of the prototype devices. Moreover, the p-type and n-type characteristics are highly symmetrical, which is essential to circuit demonstrations using complementary p-FETs and n-FETs. Fig. 5.3(d) shows the output characteristics of the reconfigurable BP transistor in the p-FET mode and the n-FET mode. The transistor shows symmetrical output characteristics in the p-FET and n-FET modes, and exhibits output saturations in both operation modes.

To help understanding the function of the polarity gate, the energy band diagrams of the reconfigurable FET in the p-FET and n-FET operation modes are illustrated in Fig. 5.3(e) and 5.3(f), respectively. To simplify the following discussion, the flat-band voltage V_{fb} is assumed to be zero. In the p-FET mode, when $V_g < 0$, hole injection from the source is enabled and the device is turned on; when $V_g = 0$, the BP near the source side is at flat-band and the hole injection is turned off, while on the drain side, the electron injection is suppressed by a negative polarity gate voltage V_{pg}, and the device is in its off-state. Without the polarity gate, an electron injection path from drain will be turned on as the gate voltage is positive relative to the drain ($V_g = 0, V_d < 0$), as indicated by the blue dashed line in Fig. 5.3(e), causing a deteriorated on-off current ratio, which has been shown in Fig. 5.2(d).

In the n-FET mode, the situation is similar: When $V_g > 0$, electron injection from the source is enabled and the device is turned on; when $V_g = 0$, electron injection from the source is turned off while the ambipolar hole injection from the drain is suppressed by the polarity gate, as indicated by the red dashed line in Fig. 5.3(f), and the device is turned off. Note that for larger polarity gate biases (more positive for n-FET mode and more negative for p-FET mode), the OFF-state current may be deteriorated due to band-to-band tunnelling effects (see Section 5.9.1).

5.5 Complementary logic inverter based on reconfigurable BP FETs

Next, we demonstrate a complementary logic inverter based on our reconfigurable BP transistors as shown in Fig. 5.4(a). The inverter is composed of two reconfigurable BP transistors – the top transistor has its polarity gate connected to ground and operates in

the p-FET mode ($V_{ds} < 0, V_{pg,s} = -V_{\mathrm{DD}}$) while the bottom transistor has its polarity gate connected to V_{DD} and operates in the n-FET mode ($V_{ds} > 0, V_{pg,s} = V_{\mathrm{DD}}$). Fig. 5.4(b) shows the voltage transfer characteristics V_{out} – V_{in} of the inverter under different supply voltages from V_{DD} = 0.2 V up to V_{DD} = 1 V. The inverter exhibits a full output swing from V_{DD} to 0 at all supply voltages due to a successful suppression of off-state currents, and shows highly symmetrical characteristics, thanks to the symmetrical characteristics of the reconfigurable BP transistors in the p-FET mode and in the n-FET mode. Owing to the steep SS of the transistors, the inverter is fully operational even at V_{DD} down to 0.2 V. It is worth noticing that the input voltage has been shifted for all curves by 0.27 V, *i.e.*, $V_{in,shift} = V_{in} - V_{fb} = V_{in} + 0.27\mathrm{V}$, to compensate for a non-zero flat-band voltage $V_{fb} = -0.27$ V, that is clearly visible in the transfer characteristics shown in Fig. 5.3(c). This slight offset is only pronounced when the input voltages are scaled down to sub-1 V range as in this work, as opposed to the large input voltage range in previous works [37], [88], where this offset is hardly noticeable. The offset could be entirely eliminated in the future by careful tuning of the gate metal work function [116] or by introducing dipoles at the dielectric interface [90], both of which are beyond the scope of this work. Fig. 5.4(c) shows the gain of the inverter as a function of input voltage under different supply voltages. The highest gain of 33.3 is achieved at V_{DD} = 1 V, and a gain of 6.4 is still retained at V_{DD} = 0.2 V.

5.6 Demonstration of polymorphic gates

Next, we demonstrate a hardware security primitive – a NAND/NOR polymorphic gate circuit based on the reconfigurable BP transistors. Fig. 5.5(a) illustrates the circuit connections for the NAND/NOR polymorphic gate and the corresponding biasing conditions for NAND and NOR configurations. When the key bit is set to 0, the top two transistors, which are connected in parallel and having their sources connected to V_{DD} and PGs connected to GND, operate in the p-FET mode and function as the pull-up network, while the bottom two transistors, connected in series and having their PGs connected to V_{DD}, operate in the n-FET mode and function as the pull-down network, thus the polymorphic gate operates in the NAND mode. When the key bit is set to 1, the V_{DD} and GND rails, the p-FETs and

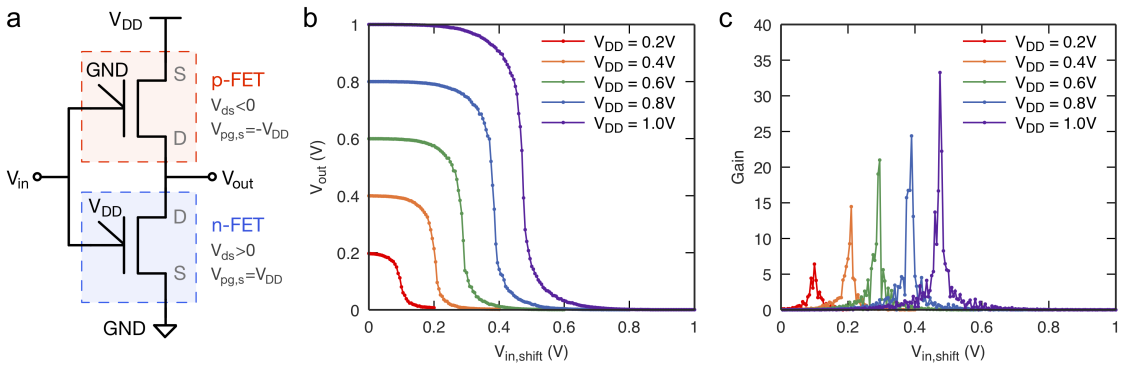


Figure 5.4. Inverter characteristics. (a) Schematic of an inverter formed by connecting two reconfigurable BP transistors together on chip, with one in the p-FET mode and the other in the n-FET mode. (b) Voltage transfer characteristics V_{out} – V_{in} of the inverter under different supply voltages V_{DD}. Note that the input voltage has been shifted by 0.27 V, *i.e.*, $V_{in,shift} = V_{in}+0.27$ V, to compensate for the non-zero V_{fb}. (c) Gain of the inverter under different supply voltages V_{DD}. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

n-FETs, as well as the pull-up and pull-down networks are interchanged, changing the functionality of the circuit to a NOR gate. Fig. 5.5(b) shows the experimental output voltages of the NAND/NOR polymorphic gate, normalized by V_{DD}, as a function of inputs A and B under different supply voltages from 0.4 V to 1 V. Reconfigurability of the polymorphic gate from NAND to NOR operation for the key bit changing from 0 to 1 is observed under low supply voltages from 0.4 V to 1 V, thanks to the reconfigurability and low-voltage operations of the composing four BP-FETs that have been wired in this experiment on chip.

In addition, we have performed circuit simulations of an XOR/XNOR polymorphic gate [Fig. 5.5(c)] using a look-up table-based Verilog-A model built from our experimental measurements (see Sections 5.9.3 and 5.9.4 for more details on device modeling). Note that the XOR/XNOR layout achieves perfect symmetry, compared with the NAND/NOR layout, which may be especially beneficial to applications in the cryptography domain where a large number of XOR functions are required to mask plaintexts with stream ciphers. Examining the simulated waveforms [Fig. 5.5(d)], one can see that the design can support two distinct

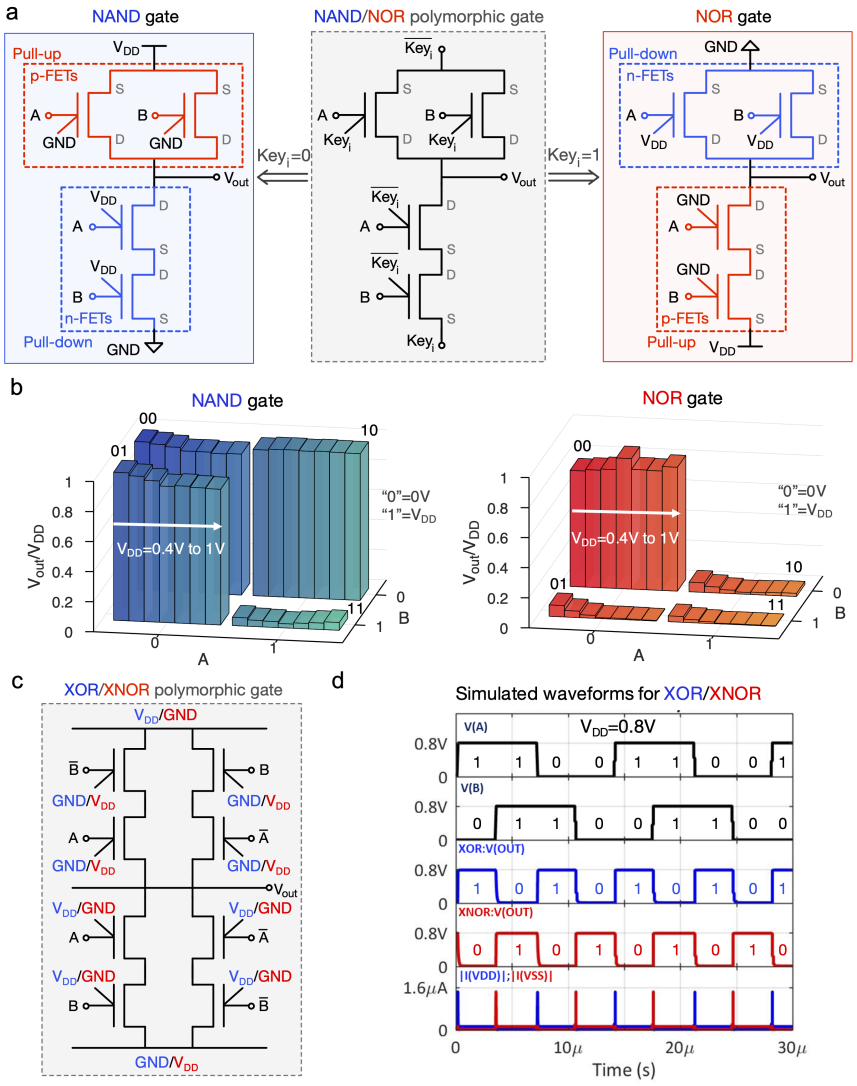


Figure 5.5. Demonstration of NAND/NOR and XOR/XNOR polymorphic gates. (a) Schematic of a NAND/NOR polymorphic gate leveraging the tunable polarities of the reconfigurable BP transistors. (b) Measured output voltages of the NAND/NOR polymorphic gate in the NAND and NOR configurations as a function of inputs A and B under different supply voltages V_{DD} from 0.4 V to 1 V, showing the reconfigurability of the polymorphic gate and low-voltage operations. (c) Schematic of an XOR/XNOR polymorphic gate. (d) Simulated waveforms of the XOR/XNOR polymorphic gate based on experimental data. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

functions, XOR and XNOR, by interchanging the V_{DD} and GND rails. Furthermore, the currents on the power supply rails in an XOR/XNOR polymorphic gate are more symmetrical than in a NAND/NOR polymorphic gate (Fig. 5.13), indicating that the former may provide better resilience to power-analysis-based side channel attacks [121].

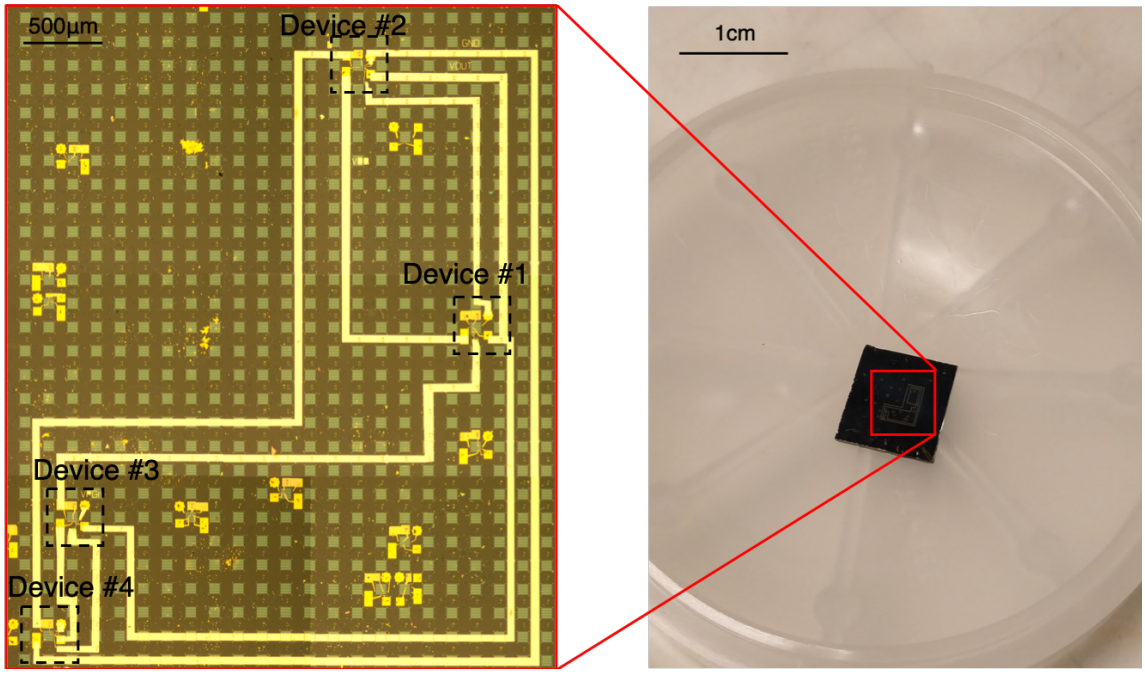


Figure 5.6. Optical image and photograph of the NAND/NOR polymorphic gate on a single chip, showing the connections between four individual reconfigurable BP devices. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

Fig. 5.6 shows a photograph of the NAND/NOR polymorphic gate on a single chip and a zoomed-in optical microscopic image showing the connections between four individual reconfigurable BP devices. At the current stage, we rely on individual exfoliated BP flakes to fabricate the devices and then connect them together to form a circuit; however, once the large-area growth of BP [122], [123] becomes more mature, monolithic integration of the circuit is possible. Note that a recent report [124] has demonstrated large-area growth of tellurium (Te), a low-dimensional material with similar electrical properties as BP [125], and exploring Te as channel material for reconfigurable FETs may be interesting for future work.

5.7 Robustness of the polymorphic gates

Finally, we assess the robustness of the polymorphic gates against power supply variations. Since the polarity gates and the power rails are interconnected, fluctuations in V_{DD} and V_{SS} are expected to affect V_{pg-s} and V_{pg-d} of the BP-FETs, which may be expected to impact the functionality of the polymorphic gates. (Note that here the notation for the "GND" rail has been replaced by "V_{SS}" as the voltage may deviate from zero.) To investigate the robustness issue, we have performed Monte Carlo simulations to verify the functionality of the NAND/NOR and XOR/XNOR polymorphic gates under power supply variations (see Section 5.9.6). The results depicted in Fig. 5.7 indicate that NAND/NOR and XOR/XNOR polymorphic gates are robust against power supply variations, as either mode in each gate can produce outputs that are distinguishable between two possible logic states, *i.e.*, logic '0' outputs are in the [-0.35 0.35] V interval, while logic '1' outputs are in the [0.45 1.15] V interval.

5.8 Conclusion

In summary, we have reported reconfigurable transistors based on BP that can be switched between p-FET and n-FET modes. Due to careful engineering of the device structure, the BP transistors exhibit on-state currents of 10 μA/μm, a steep SS of 72 mV/dec and an on-off ratio of 10^5, with highly symmetrical operation in the p-FET and n-FET modes. A high-performance complementary inverter is demonstrated based on the reconfigurable BP FET and achieved a gain of 33.3 and a lowest supply voltage of 0.2 V. A hardware security primitive, NAND/NOR polymorphic gate, was also demonstrated based on the reconfigurable BP FETs, and achieved sub-1V operation – a critical milestone for integrating 2D FETs into secure circuits. Finally, the robustness of NAND/NOR and XOR/XNOR polymorphic gates to power supply variations was verified using Monte Carlo simulations.

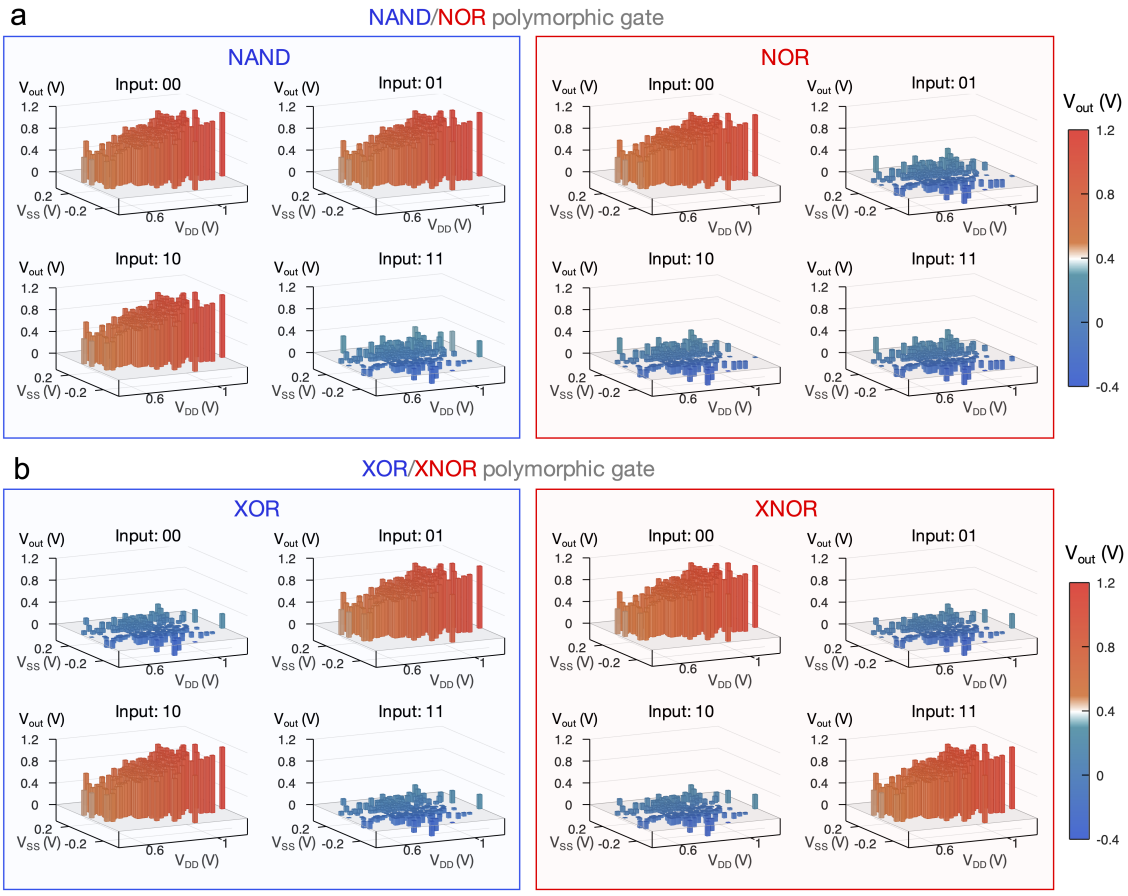


Figure 5.7. Robustness of the NAND/NOR and XOR/XNOR polymorphic gates to power supply variations. (a) Simulation results for the NAND/NOR polymorphic gate. (b) Simulation results for the XOR/XNOR polymorphic gate. Monte Carlo simulations using a table-based Verilog-A model were performed to assess the operation of the polymorphic gates under power supply variations. Simulation results for 500 runs (250 for each one of the two modes) for each polymorphic gate attest that the gates perform the intended function even in face of non-ideal power supply conditions. In the simulations, V_{DD} and V_{SS} were sampled with a Gaussian distribution, where $\mu(V_{DD})$=0.8 V and $\mu(V_{SS})$=0 V, σ=100 mV. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

5.9 Appendix

5.9.1 Doping effect of ALD Al_2O_3 on BP

BP transistors typically show p-type characteristics due to Fermi-level line-up of the metal contact closer to the valence band [7], [8]. However, a mid-gap alignment is preferred for reconfigurable transistors. We have resolved this issue by depositing Al_2O_3 on top of BP to induce n-doping effect, which also serves as top-gate dielectric. The n-doping effects induced by ALD Al_2O_3 and HfO_2 dielectrics have been reported on various material systems, including BP [9], [32], [126], MoS_2 [127], carbon nanotubes [128], [129] and tellurium [130]. Fig. 5.8 shows the transfer characteristics of a BP SB-FET before and after Al_2O_3 capping. The device shows predominately p-type characteristics, as the intrinsic Fermi level alignment of Cr/Au contact is closer to the valence band of BP. After 4 nm ALD Al_2O_3 capping and top-gate fabrication, the device shows ambipolar characteristics with symmetrical p- and n-branches, indicating a mid-gap Fermi level alignment after the treatment. Notably, the hysteresis in the transfer characteristics is greatly reduced after Al_2O_3 capping.

Apart from our experimental observations, there have also been various publications showing that the Fermi-level line up between metal and channel material in a Schottky-barrier FET can indeed be affected by a capping layer on the channel [128], [131]. The detailed mechanism of how an ALD capping layer on the channel modifies the contact properties is still under exploration.

5.9.2 Effect of BP body thickness on the device performance

Previous studies have shown that the bandgap of BP and Fermi level line-up of metal-BP contacts depend on the BP body thickness [8]. Therefore, the device performance of a BP SB-FET is also impacted by the BP body thickness. Fig. 5.9 shows the effect of BP body thickness on the device performance of BP SB-FETs. In Device A with t_{body} = 5.6 nm, the ambipolar p- and n-branches are highly symmetrical, indicating a mid-gap Fermi-level alignment of the metal contacts. However, when t_{body} is increased to 11 nm and 15 nm in Device B and Device C, respectively, even though the n-branches are still quite visible

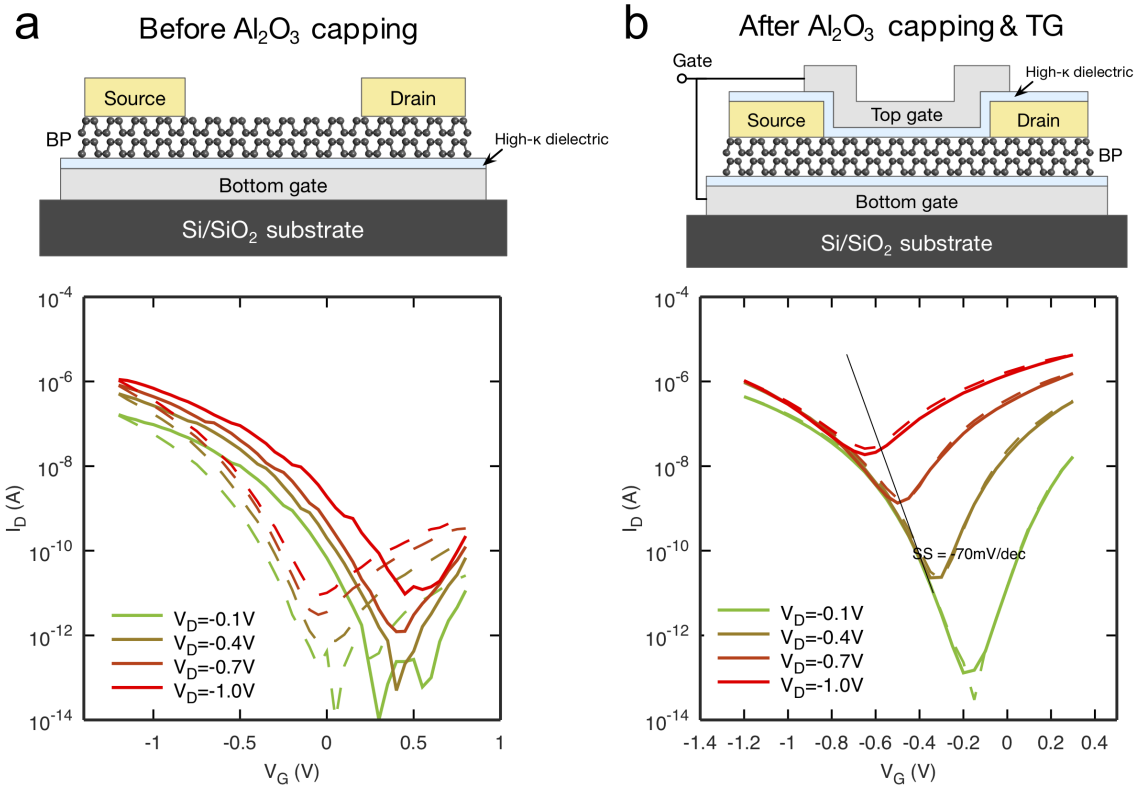


Figure 5.8. Doping effect of ALD Al_2O_3. (a) Transfer characteristics of a BP SB-FET before Al_2O_3 capping. (b) Transfer characteristics of the same device after Al_2O_3 and top-gate fabrication. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

(thanks to the n-doping effect discussed in the previous section), the p-branches become more dominant, indicating the Fermi-level alignment of the metal contact becomes closer to the valence band in the case of thicker BP bodies. Also notice that the on-off current ratios of the BP SB-FETs become smaller with thicker body thicknesses, which indicates a decreasing bandgap with thicker BP thickness, in accordance with previous reports [8].

Since the Fermi level line-up of the metal-BP contact depends on the BP body thickness, the performance of reconfigurable BP FETs also depends on the body thickness, as shown in Fig. 5.10. In Device A with $t_{body} = 7$ nm (the device described in Section 5.4 and Fig. 5.3), the p-FET and n-FET modes exhibit highly symmetrical operations, due to mid-gap Fermi

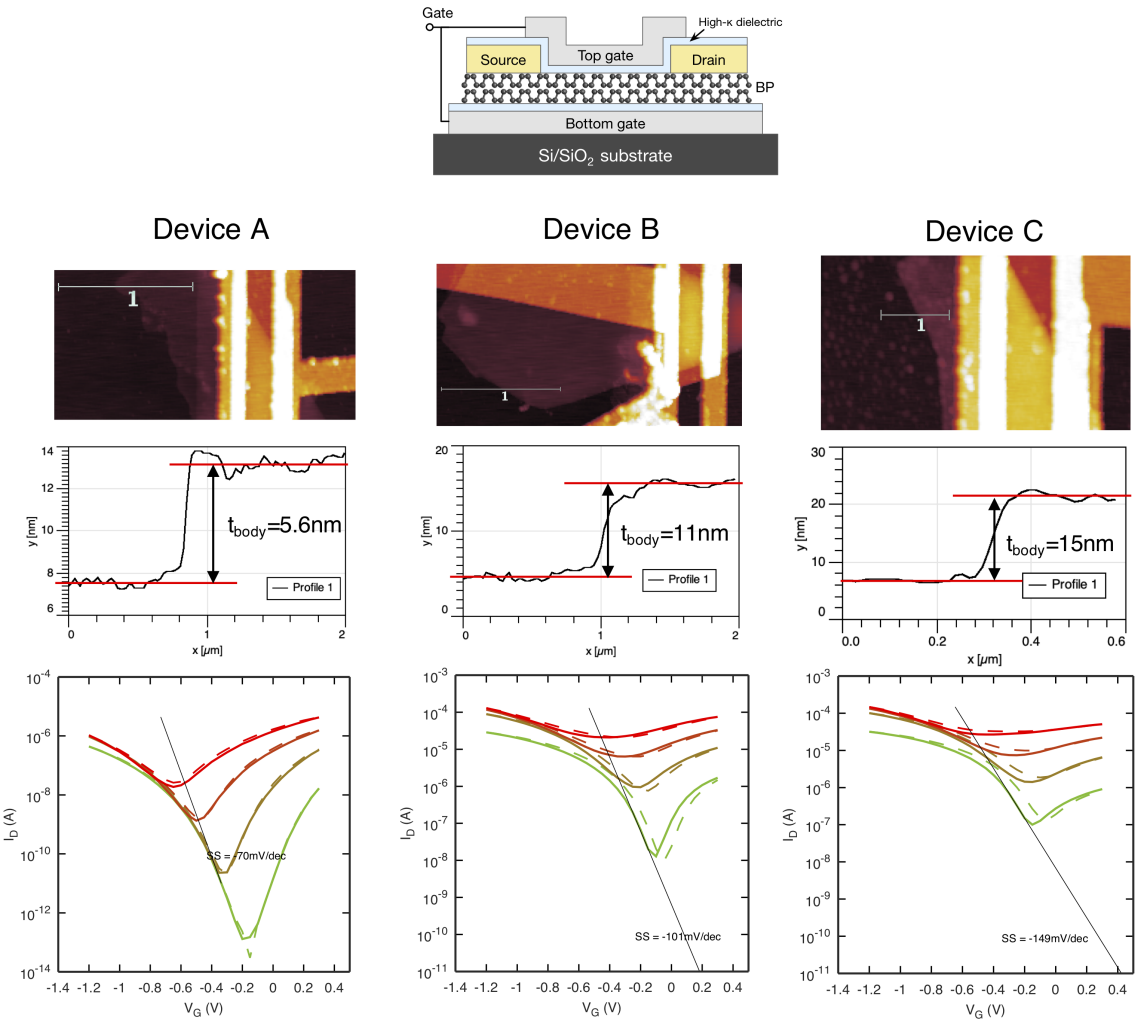


Figure 5.9. Effect of BP body thickness on BP SB-FETs performance. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

level alignment of the metal contact. However, in Device B with t_{body} = 16 nm, since the Fermi level is pinned closer to the valence band, the p-FET mode shows a higher on-current than the n-FET mode. Also notice that the off-current in the n-FET mode is higher, since the Fermi level is now closer to the valence band and the hole injection from the drain is more difficult to turn off.

In summary, BP with body thicknesses in the range of 5 nm to 7 nm are optimal to achieve symmetrical p-FET and n-FET modes and high on-off ratios. However, since our

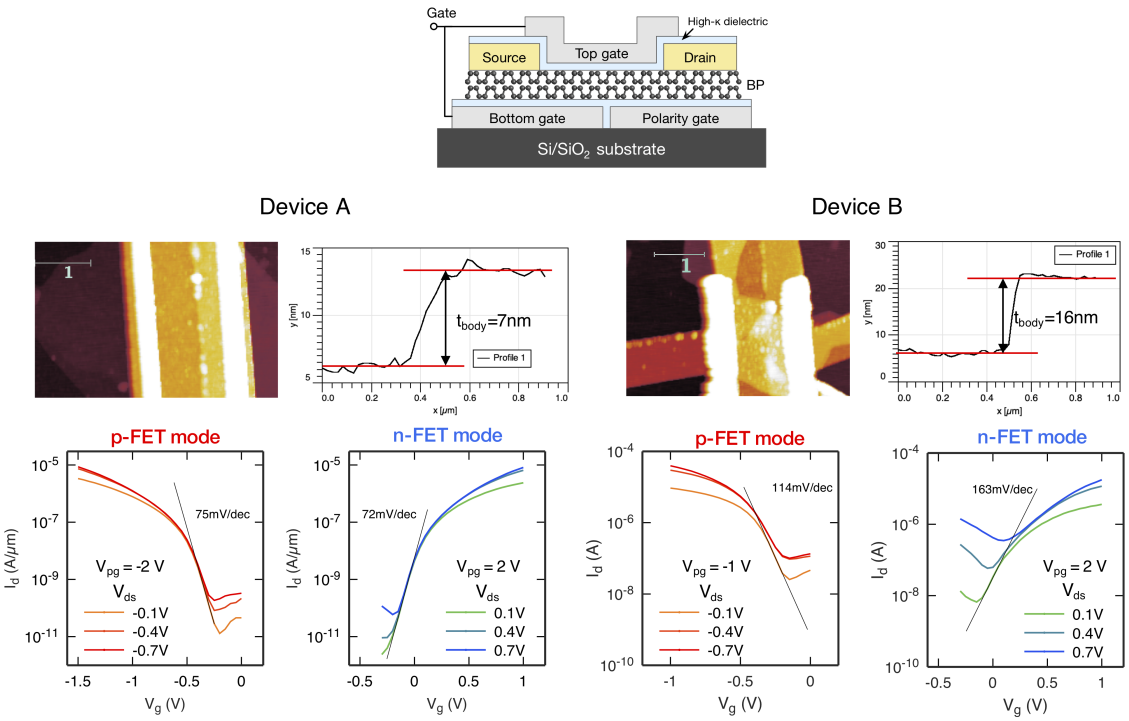


Figure 5.10. Effect of BP body thickness on reconfigurable BP FETs performance. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

device fabrication involves exfoliation of BP flakes from bulk crystals, flakes with thickness in this range are rare to find (most of the flakes are >10 nm thick). Even though we succeeded in finding two flakes with optimal thicknesses in one batch to fabricate two FETs and an inverter (shown in Fig. 5.4), finding 4 flakes with optimal thicknesses in one batch is more challenging and our efforts remained unsuccessful. Therefore, we built the NAND/NOR polymorphic gate from four reconfigurable BP FETs with flake thicknesses larger than 10 nm as a prototype (Device B in Fig. 5.10 is a representative one of the four devices). The lower on-off current ratios in these four transistors, due to non-optimal body thicknesses, are the main reasons for the output voltages not reaching V_{DD} and 0. In the future, with large-area growth of BP [122], [123] or material with similar properties, such as tellurium [124], [125], becoming more mature, one can expect a better control of the body thickness

in the desired range, and the circuit performance can be further improved, as evident from our inverter demonstration.

5.9.3 Device modeling of reconfigurable BP FETs for circuit simulation

To perform circuit simulation of polymorphic gates built with the reconfigurable BP transistors, we have developed a look-up table-based Verilog-A model that is based on our experimental device measurements. The voltage scan ranges for the experimental measurement are shown in Fig. 5.11. The measurement results with different combinations of V_d, V_g and V_{pg} form a three-dimensional tensor and are used as the look-up table for the Verilog-A model, and interpolation is used for voltages that are not included in the table.

	n-FET mode	p-FET mode
V_d	[0:0.05V:1V]	[0:-0.05V:-1V]
V_g	[0:0.05V:1V]	[0:-0.05V:-1V]
V_{pg}	[0:0.1V:1V]	[0:-0.1V:-1V]

Figure 5.11. Voltage scan ranges for experimental measurement, in the format of "[start:step:end]". Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

Note that the below measurements were performed on a different device than the reconfigurable BP FET shown in the main text. A subset of the measurement results is shown in Fig. 5.12. The device used for modeling shows slightly worse symmetry between the p-FET mode and the n-FET mode than the device in the main text, as well as worse on-off current ratio and SS in the n-FET mode, as one can see by comparing Fig. 5.3 and Fig. 5.12. Nevertheless, the device also exhibits reconfigurable operation between n-FET and p-FET modes and decent on-off current ratios of 10^3, and can be used for circuit simulation of polymorphic gates.

In addition, the effects of polarity gate bias on the device transfer characteristics are shown in Fig. 5.12. One can see that with larger V_{pg} (more positive for the n-FET mode and

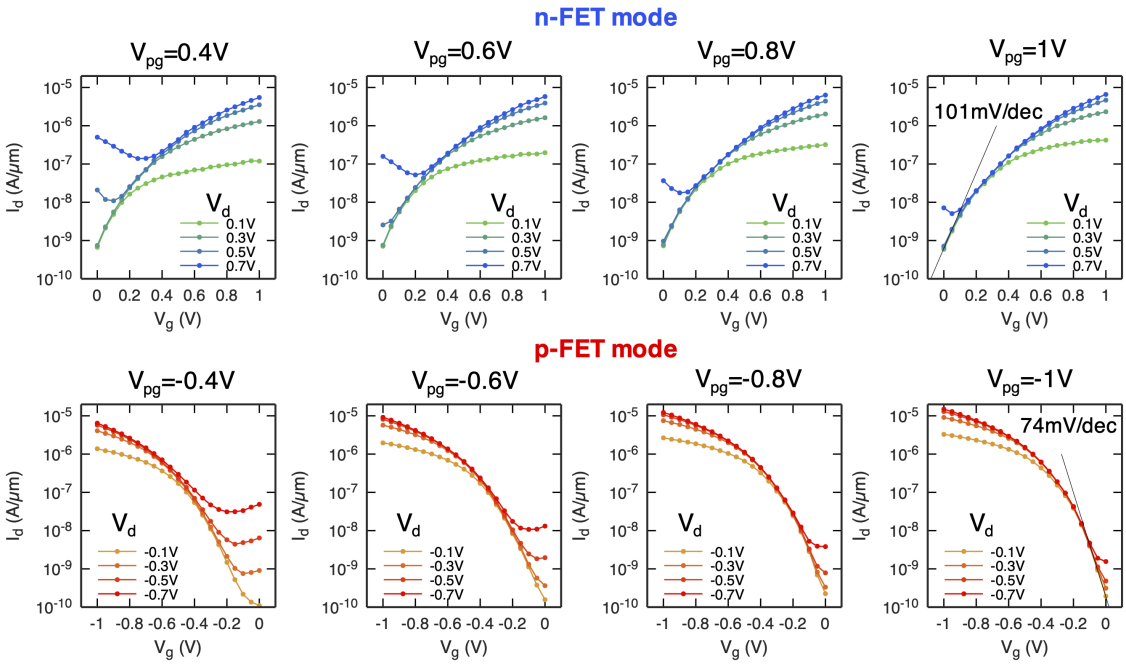


Figure 5.12. Measurement results of the reconfigurable BP FET used for modeling. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

more negative for the p-FET mode), the off-state current decreases and on-off current ratio increases, which agrees with our analysis in Figs. 5.3(e) and 5.3(f) and the Section 5.9.5.

5.9.4 Circuit simulation of a NAND/NOR polymorphic gate

Using the Verilog-A device model developed in Section 5.9.3, we have also simulated a NAND/NOR polymorphic gate. Fig. 5.13 shows the simulated waveforms for the NAND/NOR polymorphic gate. The circuit can achieve NAND or NOR functionality when assigning the V_{DD} and V_{SS} rails as indicated by the blue and red labels, respectively. In addition, by inspecting the current profiles on the voltage supply rails, one can see that the spikes on the current profiles are not symmetrical for NAND and NOR configurations, indicating the risk of using power-analysis-based side-channel attacks to determine the functionality of the circuit. By contrast, the XOR/XNOR polymorphic gate, shown in Fig. 5.5(d), exhibits

symmetrical current profiles in the XOR and XNOR configurations, and is thus less prone to power-analysis attacks.

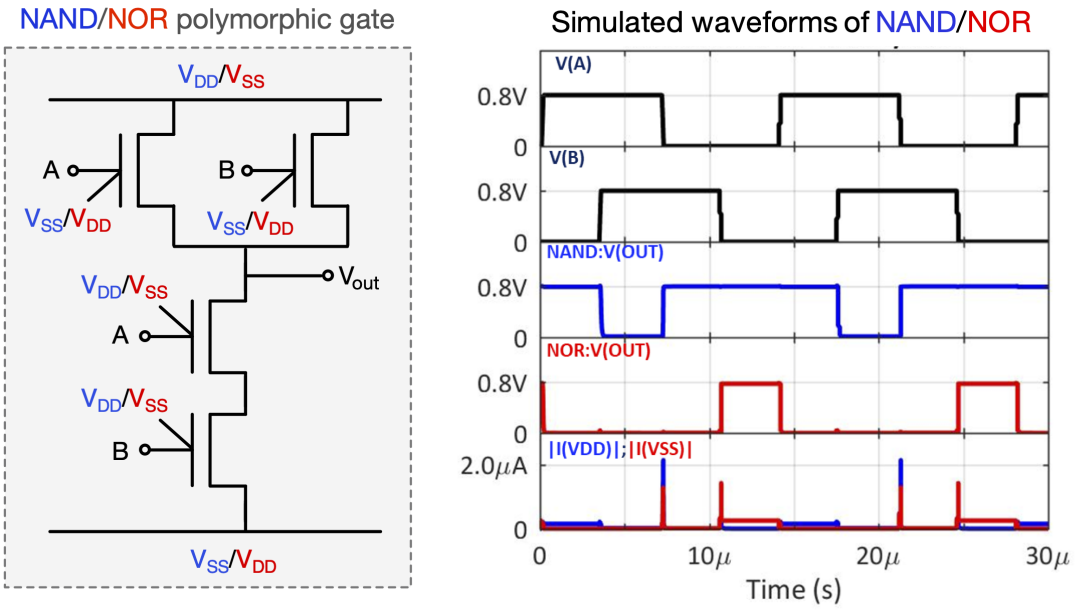


Figure 5.13. Simulated waveforms of NAND/NOR polymorphic gate. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

5.9.5 The effect of band-to-band tunneling on the off-state current of the reconfigurable BP FETs

Previous works [62], [132] have pointed out that band-to-band tunneling (BTBT) might be the limiting factor for the OFF-state current in a BP transistor. However, we argue that due to (1) our different device structure (2) a different scan range of gate voltages, the off-state current in our device is indeed limited by ambipolar injection from the drain side, rather than BTBT.

In Fig. 5.14, we compare our device structure with the device structure in Ref. [62] and the corresponding band diagrams in the OFF-state of the p-FET modes. Since we are looking into injection from the drain side, the gate (drain gate/polarity gate) voltage relative to the drain should be studied. As shown in Fig. 5.14(a), a BTBT path is created that limits the

OFF-state current, as indicated by the grey arrow in the triple-gated structure in Ref. [62], since the channel region and drain region are electrostatically doped to n-type and p-type, respectively, due to the positive gate voltage and negative drain gate voltage ($V_{g-d} = 1$ V, $V_{dg-d} = -7$ V).

In comparison, in our device structure, region 2 is controlled by both gate G (top gate, to be more specific) and polarity gate PG. Since G and PG have opposite polarities relative to drain ($V_{pg-d} = -1.3$ V, $V_{g-d} = 0.7$ V), the negative PG voltage "cancels out" (at least partially) the n-doping effect induced by G. Therefore, the n-doping in region 2 is weaker than in the channel region in the triple-gated structure. In addition, since a relatively small voltage is applied on PG ($V_{pg-d} = -1.3$ V, compared with $V_{dg-d} = -7$ V in Ref. [62]), the p-doping concentration in region 3 is also weaker than in the drain region in the triple-gated structure. Adding up these effects, we can see that both the n-doped region and the p-doped region have weaker doping levels in our device structure than in the triple-gated structure. Therefore, BTBT is suppressed in our device structure, as shown in the band diagram in Fig. 5.14(b).

Also note that in Fig. 5.14(b), we are plotting band diagrams for two possible injection paths, A and B, in which path-A is where BTBT might occur but electron injection is suppressed by the p-doped region 3 which is under PG control, and path-B is the direct injection path from the drain to region 2. The latter is under the control of both G and PG, and electron injection is more likely to occur. Since our main concern is electron injection from the drain rather than BTBT as we have analyzed, we are plotting the band diagram for path-B in Fig. 5.3(e).

More importantly, apart from this qualitative analysis, we have also measured the device characteristics under different polarity gate voltages to further consolidate our analysis. If the OFF-state current would be limited by BTBT, the OFF-state current would increase when a more negative polarity gate voltage is applied in the p-FET mode because of the increased p-doping in the drain region and the larger BTBT window, as shown in Fig. 5.14(a). However, as shown in Fig. 5.15 (also in Fig. 5.12), the OFF-state current decreases for more negative V_{pg} in the p-FET mode (or more positive V_{pg} in the n-FET mode), indicating that the OFF-

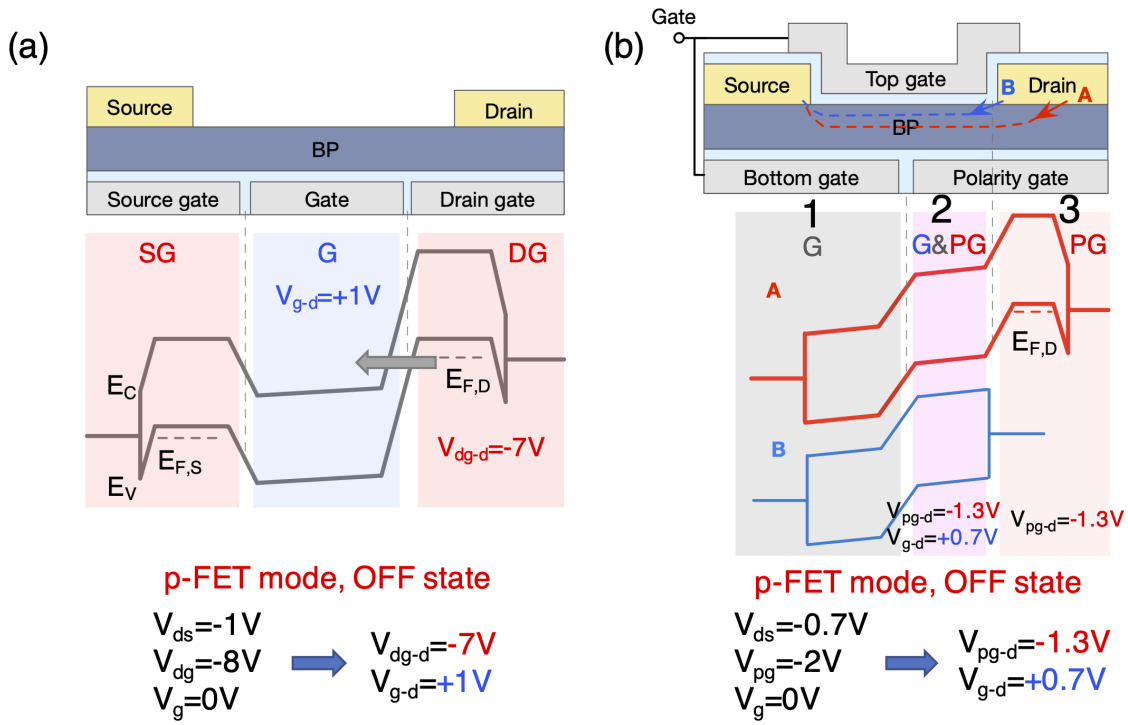


Figure 5.14. Device schematics and band diagrams of two reconfigurable FET structures in the OFF-state of p-FET mode. (a) Triple-gated structure in Ref. [62]. (b) Device structure in our work. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

state current is indeed limited by electron injection from the drain side in the p-FET mode and hole injection from the drain side in the n-FET mode, rather than BTBT.

From the V_{pg}-dependent I-V curves, we can see that the OFF-state current is still limited by injection from the drain, rather than BTBT, at least within the V_{pg} range we have scanned. However, for too large polarity gate bias, we believe that there is a possibility that a BTBT path might be turned on, as shown in Fig. 5.14(a).

5.9.6 Monte Carlo simulation for robustness of polymorphic gates

We leverage the Verilog-A table-based model for BP-FETs to perform Monte Carlo simulations in HSPICE. The goal of the Monte Carlo simulations is to assess the robustness of

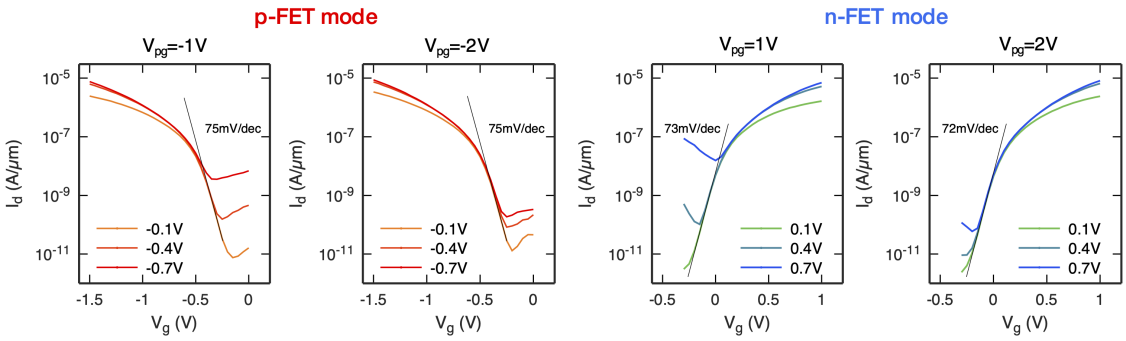
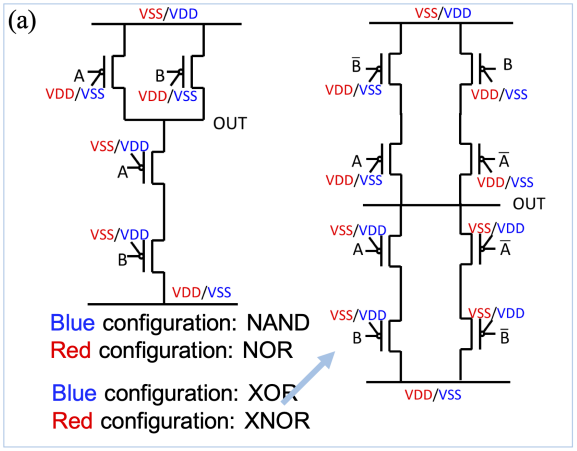


Figure 5.15. Transfer characteristic of the reconfigurable BP FET in the p-FET mode and the n-FET mode under different polarity gate voltages. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

the NAND/NOR and XOR/XNOR polymorphic gates [Fig. 5.16(a)] against power supply variations. A list of the signals applied at the inputs of these gates, as well as the supply rails, is provided in Fig. 5.16(b). We sampled V_{DD} and V_{SS} with a Gaussian distribution, where $\mu(V_{DD})$=0.8 V and $\mu(V_{SS})$=0 V, σ=100 mV. Furthermore, four logic inputs (A and B) patterns were tested for each gate, *i.e.*, '00', '01', '10', '11'. We set logical values '1' and '0' to be 0.8 V and 0.0 V, respectively, which correspond to $\mu(V_{DD})$ and $\mu(V_{SS})$, respectively. That is, no voltage variations were considered for the logic inputs.

Monte Carlo simulations of the NAND/NOR polymorphic gate consisted of 500 runs (*i.e.*, 250 for NAND function and 250 for NOR function). Similarly, Monte Carlo simulations of the XOR/XNOR polymorphic gate employed a total of 500 runs (250 for each one of the XOR and XNOR functions). As it can be seen in the histogram of Fig. 5.16(c), the parameters chosen for our Monte Carlo simulation allow for the widest range of V_{DD} and V_{SS} that do not result in an overlap between V_{DD} and V_{SS}. Considering the $\mu(V_{DD})$, $\mu(V_{SS})$, and σ adopted in our simulations, we expect 99.7% (3σ) of the voltage supply samples produced by the Gaussian distribution to fall in the $V_{DD} = [0.5\ 1.1]$ V and $V_{SS} = [-0.3\ 0.3]$ V intervals.

The effects of voltage supply variation in the logical outputs of the polymorphic NAND/NOR and XOR/XNOR gates are depicted in Fig. 5.7. Our simulation results indicate that polymorphic NAND/NOR and XOR/XNOR gates are robust against power supply variations,



(b)

Signal	Type	Value (s)	Variation?
A	Logic Input	0.8V (logic '1') 0.0V (logic '0')	No
$\bar{A}$	Logic Input	0.8V (logic '1') 0.0V (logic '0')	No
B	Logic Input	0.8V (logic '1') 0.0V (logic '0')	No
$\bar{B}$	Logic Input	0.8V (logic '1') 0.0V (logic '0')	No
VDD	Supply	$\mu \pm \sigma$ = 0.8V ±0.1V	Yes
VSS	Supply	$\mu \pm \sigma$ = 0.0V ±0.1V	Yes

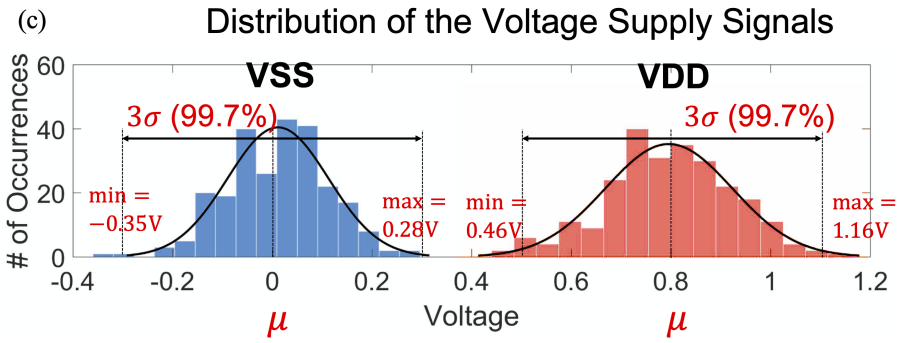


Figure 5.16. Setup of Monte Carlo Simulations. We assess the operation of the polymorphic NAND/NOR and XOR/XNOR gates under power supply variations. V_{DD} and V_{SS} were sampled with a Gaussian distribution, where μ (V_{DD})=0.8 V and μ(V_{SS})=0 V, σ=100 mV. Four logic inputs (A and B) patterns were tested for each gate, *i.e.*, '00', '01', '10', '11', without voltage variations. Considering the $\mu(V_{DD})$, $\mu(V_{SS})$, and σ adopted in our simulations, there is no overlap between V_{DD} and V_{SS}. Furthermore, 99.7% (3σ) of the voltage supply samples produced by the Gaussian distribution fall in the V_{DD} = [0.5 1.1] V and V_{SS} =[-0.3 0.3] V ranges. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

as either mode in each gate can produce outputs that are distinguishable between the two possible logic states, *i.e.*, logic '0' outputs are in the [−0.35 0.35] V interval, while logic '1' outputs are in the [0.45 1.15] V interval.

5.9.7 Methods

Bottom gates and polarity gates fabrication

Polarity gate (PG) electrodes (2 nm Ti) were deposited using e-beam evaporation onto a silicon substrate with 90 nm of silicon dioxide on top and patterned using standard e-beam lithography and lift-off process. Next, an isolation layer of 6 nm Al_2O_3 and bottom gate (BG) electrodes (2 nm Ti) were deposited using atomic layer deposition (ALD) and e-beam evaporation, respectively, and were patterned using e-beam lithography and lift-off process in the same step. Finally, 7 nm of HfO_2 was deposited on top of the gate metals as dielectric for both BG and PG using another ALD process.

Device fabrication

BP flakes were exfoliated onto the substrate with BG and PG structures from bulk crystals (purchased from Smart Elements, purity 99.998%). The exfoliation was performed in ambient environment; however, care was taken to minimize the exposure time in air (<30 min). Cr/Au (1 nm/40 nm) electrodes were deposited and patterned by e-beam evaporation and e-beam lithography as source/drain contacts. A thin layer of Al was evaporated on top of BP, which formed a 1.3 nm thick aluminum oxide upon exposure in air and acted as seeding layer for ALD process on BP. Next, 4 nm of Al_2O_3 top gate (TG) dielectric was deposited employing an ALD process on top of BP. The device fabrication was finalized by depositing a TG electrode (40 nm Ti) and another metallization step to connect the TG and BG electrodes. After all fabrication steps, the sample was annealed in a forming gas environment for 3 hours at 300 °C to improve the quality of the dielectric. For the inverter and NAND/NOR polymorphic gate circuits, an additional lithography and metallization step was performed to deposit and define the metal wires connecting the electrodes of individual devices on chip. A more detailed process flow is shown in Fig. 5.17.

The description for each step is given below:

(1) Start with 90 nm SiO_2/Si substrate;

(2) Define and deposit 2 nm Ti as polarity gate (PG);

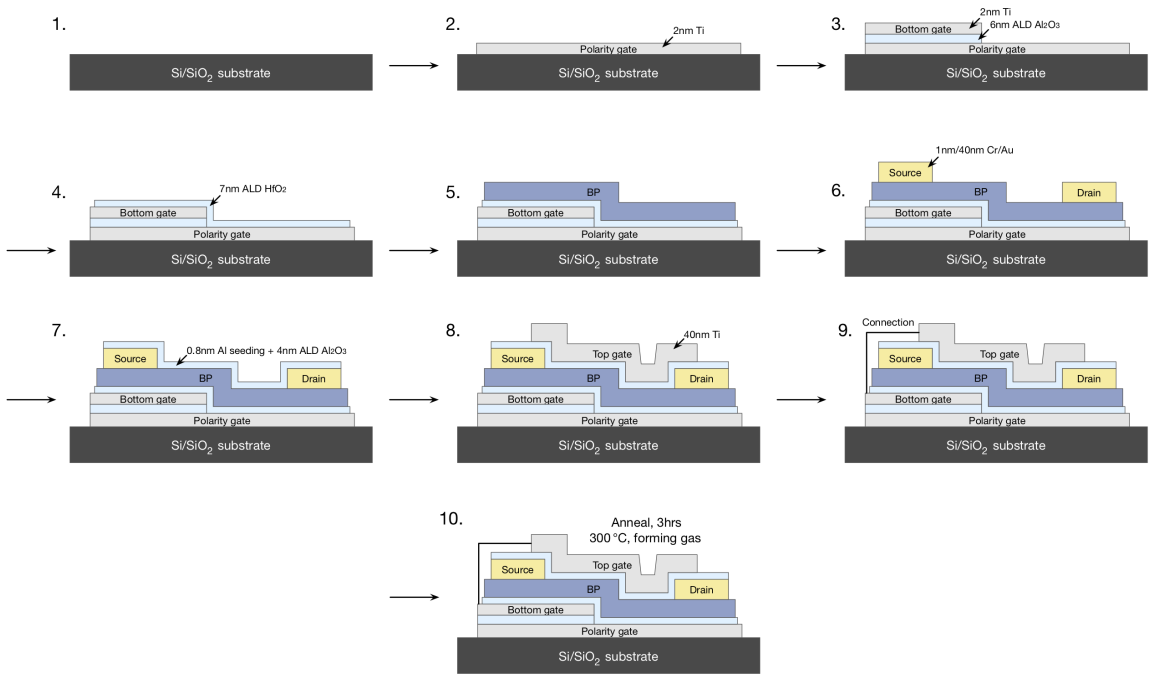


Figure 5.17. Process flow of device fabrication. Reprinted with permission from P. Wu, D. Reis, X. S. Hu, J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021). Copyright (2021) Springer Nature.

(3) Define and deposit 6 nm ALD Al_2O_3 and 2 nm Ti as isolation layer and bottom gate (BG);

(4) Deposit 7 nm ALD HfO_2 as gate dielectric for PG and BG;

(5) Exfoliate BP flakes;

(6) Define and deposit 1 nm/40 nm Cr/Au as source/drain contacts;

(7) Deposit 0.8 nm Al seeding layer and 4 nm ALD Al_2O_3 as top gate dielectric;

(8) Define and deposit 40 nm Ti as top gate (TG);

(9) Define and deposit 40 nm Ti as metal wire connecting BG and TG (Al_2O_3 is etched before metal deposition);

(10) Anneal in forming gas environment for 3 hours at 300 °C.

Device characterization

The electrical characterization of the devices and circuits was performed in a LakeShore FWPX Probe Station at a vacuum level below 10^{-5} Torr using an Agilent 4156C Parameter Analyzer. All measurements were performed at room temperature.

Device modeling and circuit simulation

The circuit simulation in this work is based on a look-up table-based Verilog-A model built from experimental measurements of a reconfigurable BP FET. More details of the experimental device, modeling and simulation are described in Sections 5.9.3, 5.9.4 and 5.9.6.

6. ARTIFICIAL SUB-60 MV/DEC SWITCHING IN A METAL-INSULATOR-METAL-INSULATOR-SEMICONDUCTOR TRANSISTOR WITHOUT FERROELECTRIC COMPONENT

Most of the material in this chapter has been reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* 15, 5158-5164 (2021). Copyright (2021) American Chemical Society.

Negative capacitance field-effect transistors (NC-FETs) have attracted wide interest as promising candidates for steep-slope devices, and sub-60 millivolts/decade (mV/dec) switching has been demonstrated in NC-FETs with various device structures and material systems. However, the detailed mechanisms of the observed steep-slope switching in some of these experiments are under intense debate. Here we show that sub-60 mV/dec switching can be observed in a WS_2 transistor with a metal-insulator-metal-insulator-semiconductor (MIMIS) structure – without any ferroelectric component. This structure resembles an NC-FET with internal gate, except that the ferroelectric layer is replaced by a leaky dielectric layer. Through simulations of the charging dynamics during the device characterization using a resistor-capacitor (RC) network model, we show that the observed steep-slope switching in our "ferroelectric-free" transistors can be attributed to the internal gate voltage response to the chosen varying gate voltage scan rates. We further show that a constant gate voltage scan rate can also lead to transient sub-60 mV/dec switching in an MIMIS structure with voltage dependent internal gate capacitance. Our results indicate that the observation of sub-60 mV/dec switching alone is not sufficient evidence for the successful demonstration of a true steep-slope switching device and that experimentalists need to critically assess their measurement setups to avoid measurement-related artefacts.

6.1 Introduction

Negative capacitance field-effect transistors (NC-FETs) have been proposed as devices that could break the 60 mV/dec subthreshold swing (SS) limit of metal-oxide-semiconductor field-effect transistors (MOSFETs) at room temperature and achieve low-power switching [133]–[136]. The proposed NC-FET structure includes a ferroelectric (FE) capacitor in se-

ries with a normal dielectric (DE) capacitor to stabilize the negative capacitance region in the ferroelectric material, leading to an internal voltage amplification and sub-60 mV/dec switching. Since then, sub-60 mV/dec operations have been reported in NC-FETs from various material systems and device structures [137]–[142]. However, the origin of the observed steep-slope switching is still under intense debate. Different from the original proposal, alternative mechanisms for the observed steep slope switching have been proposed and the validity of a stabilizing negative capacitance (NC) region of FE materials has been challenged [143]–[145]. For example, some papers relate the observed steep switching to transient effects such as internal potential jumps [146], [147] or differential voltage amplification caused by polarization switching of FE material [148]–[154], instead of a quasi-static NC effect represented as the "S"-shaped curve in the polarization–electric field (P–E) relation of FE materials [133], [155], [156]. Other explanations include domain nucleation and growth in multi-domain FE materials [147], [157], [158]. Yet due to the complexity of both the ferroelectric physics and the experimental systems, there has not been a single consolidated theory that can convincingly explain all the experimental findings. Therefore, a model system exhibiting similar device characteristics yet with simplified physics is highly sought after.

In this chapter, we experimentally demonstrate a two-dimensional tungsten disulfide (WS_2) transistor in a metal-insulator-metal-insulator-semiconductor (MIMIS) device structure, in which sub-60 mV/dec switching is observed. The device structure is similar to an NC-FET with internal metal gate, or equivalently a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure [Fig. 6.1(a)], except that the ferroelectric (FE) layer is replaced by a leaky dielectric (DE) layer [Fig. 6.1(b)]. In previous publications, negative capacitance FETs with leaky FE layers have been studied [159], [160]. However, to the best of our knowledge, there have been no discussions on the impact of leaky insulators in devices built with only DE layers and no FE layers. Also it has been reported that a lossy dielectric can be misinterpreted as ferroelectric due to measurement artefacts [161], yet there have been no discussions on the implications of such artefacts for electrical devices.

In the MIMIS device, we show that several key phenomena observed in NC-FETs can be reproduced [Figs. 6.1(c) & 6.1(d)]: (i) sub-60 mV/dec switching, (ii) anti-clockwise hysteresis, and (iii) internal voltage amplification. By replacing the FE layer with a DE

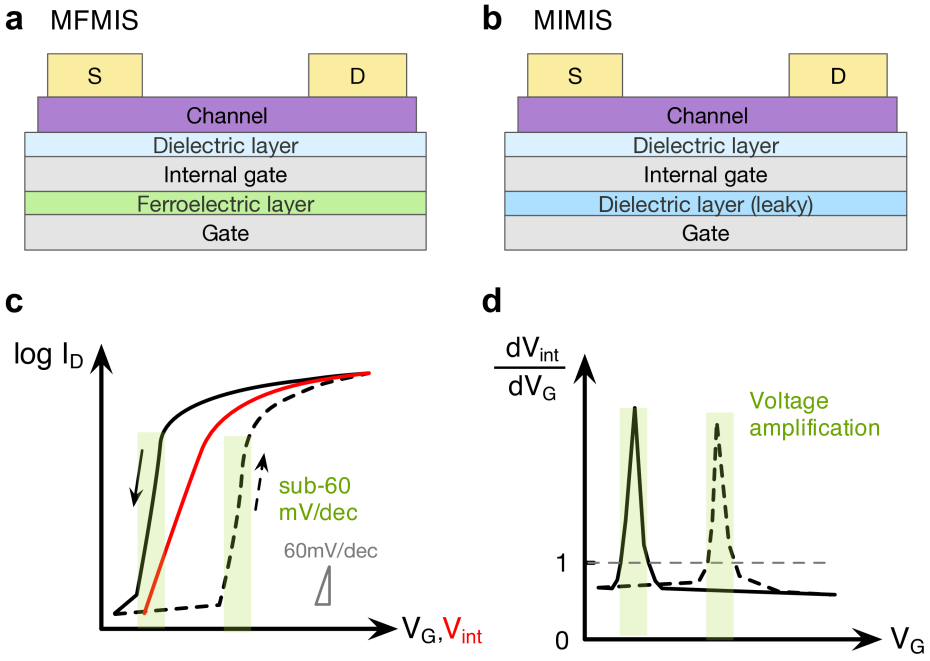


Figure 6.1. Steep switching behavior in MFMIS and MIMIS structure. (a) Schematic of a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure. (b) Schematic of a metal-insulator-metal-insulator-semiconductor (MIMIS) structure with a leaky dielectric layer between gate and internal gate. (c) Illustration of the transfer characteristics of a steep switching MFMIS or MIMIS device. (d) Illustration of internal voltage amplification of a steep switching MFMIS or MIMIS device. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

layer, we are able to avoid the controversial discussion about polarization switching in the ferroelectric and can focus entirely on the charging dynamics inside the system, which is built with well-understood basic circuit components such as resistors (R) and capacitors (C). Using a simple RC network model, we are able to simulate the charging dynamics in the MIMIS device. Distinct device features i) through iii) from above can be readily explained as a result of the varying gate voltage scan rates due to auto-ranging of the current measurement, which could be a common issue in the characterization of steep-slope transistors. We further show that a sub-60 mV/dec switching can still be observed with a

constant gate scan rate if the internal gate capacitance is voltage-dependent, highlighting the universality of the effect.

6.2 Experimental demonstration of sub-60 mV/dec switching in an MIMIS device

Fig. 6.2(a) shows a schematic of the MIMIS device. The internal FET is composed of an 8-nm-thick WS_2 channel with Ni source/drain metal contacts on top of a local bottom gate structure with 7-nm-thick HfO_2 gate dielectric grown by atomic layer deposition (ALD) and Ti gate metal as "Internal gate" electrode, which is separated from the "Gate" electrode by a low-quality, leaky AlO_x dielectric film grown by natural oxidation of a thin Al layer (see Methods). The leakage current through the leaky AlO_x dielectric film in a capacitor with an area of $\sim$1 μm^2 is on the order of 1$\sim$100 pA at $\pm$0.5 V [Fig. 6.2(b)]. Note that due to the low growth temperatures of the HfO_2 and AlO_x dielectric films, these layers are expected to be amorphous, which precludes any ferroelectricity.

Fig. 6.2(c) shows the I_D – V_{int} transfer characteristics of the internal WS_2 FET. All device characterization in this study was performed using an Agilent 4156C semiconductor parameter analyzer in a LakeShore FWPX probe station at a vacuum level below 10^{-5} Torr at room temperature. Due to the ultra-thin body of the WS_2 channel and high quality of the ALD-grown HfO_2 dielectric [162], an SS-value of 61 mV/dec is achieved in the WS_2 internal FET, close to the 60 mV/dec room-temperature limit. Also note that the hysteresis in the I_D – V_{int} characteristics of the WS_2 internal FET is negligible [inset of Fig. 6.2(c)] due to the high quality of the HfO_2 dielectric and low defect density at the semiconductor-oxide interface. The near-ideal SS-value and hysteresis-free characteristics of the WS_2 internal FET are independent of the measurement setup details, such as scan rates and hold time, as shown in the Section 6.7.4.

Next, we characterize the I_D – V_G transfer characteristics of the WS_2 MIMIS device. As shown in Fig. 6.2(d), an anti-clockwise hysteresis is observed in the I_D – V_G characteristics, and sub-60 mV/dec switching behaviors are observed in both sweep directions, indicated by the green and orange shaded regions, respectively. The observed characteristics resemble previous reported two-dimensional (2D) NC-FETs with MFMIS device structures [138]–[140],

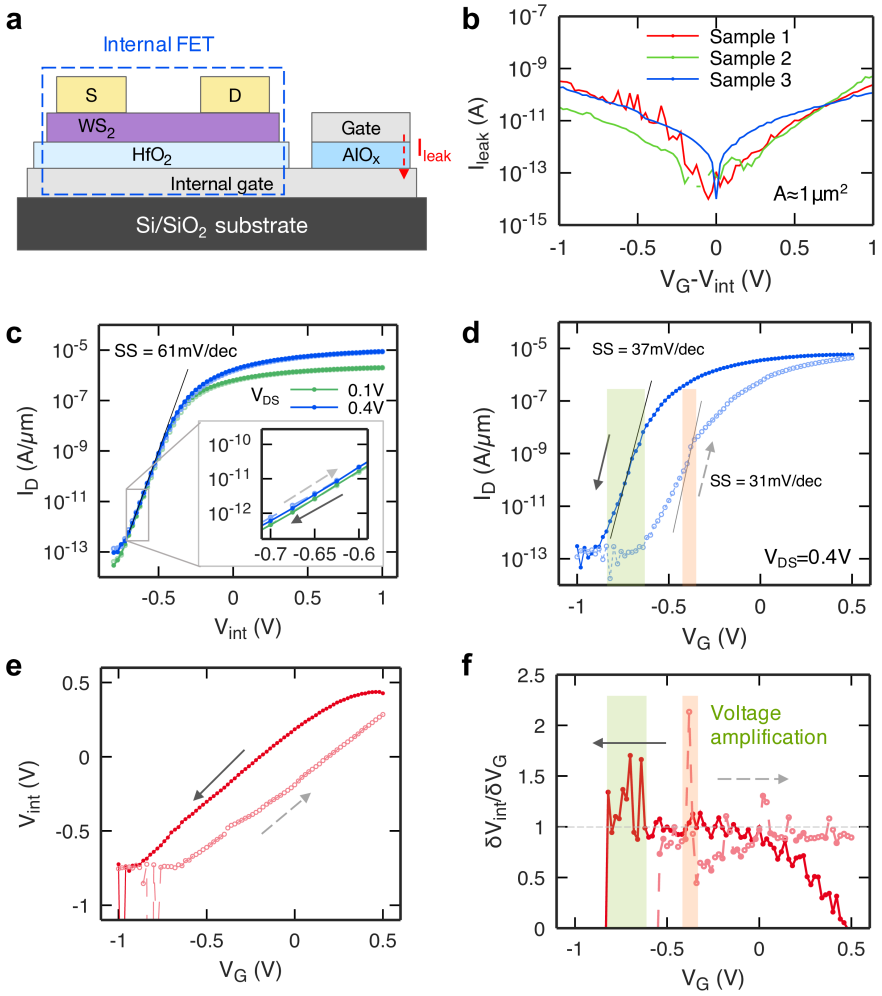


Figure 6.2. Experimental demonstration of sub-60 mV/dec switching in a MIMIS device. (a) Schematic of the MIMIS transistor structure with WS_2 channel. (b) Leakage current I_{leak} through the leaky AlO_x dielectric. (c) I_D – V_{int} characteristics of WS_2 FET using the internal gate electrode, showing near-ideal 60 mV/dec switching. Inset: enlarged view of the subthreshold I_D – V_{int} characteristics, showing negligible hysteresis. (d) I_D – V_G characteristics of the WS_2 MIMIS FET using the electrode labeled "gate", showing sub-60 mV/dec switching and anti-clockwise hysteresis. (e) Extracted V_{int} – V_G from the I_D – V_G scan. (f) Extracted internal voltage gain $\delta V_{int}/\delta V_G$ – V_G from the I_D – V_G scan, showing internal voltage amplifications. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

even though there is no ferroelectric component in our MIMIS device. Since the I_D – V_{int} characteristics of the internal WS_2 FET are essentially hysteresis-free, we can derive a one-to-one mapping between I_D and V_{int} at a given drain voltage and extract V_{int} [Fig. 6.2(e)] and the internal voltage gain $\delta V_{int}/\delta V_G$ [Fig. 6.2(f)] during the I_D – V_G scan. One can see that internal voltage amplifications ($\delta V_{int}/\delta V_G > 1$) can be observed in both sweeping directions in the I_D – V_G scan. Note that although direct measurement methods of the internal gate voltage V_{int} during the I_D – V_G scan exist, previous studies [146], [147] have pointed out that a voltage measurement system with input impedance much larger than the leakage resistances of the capacitors is required to accurately measure these voltages, which is not available in our measurement system. Therefore, we have adopted the strategy of indirectly extracting V_{int} from the measured I_D.

6.3 Modeling of the charging dynamics in the MIMIS device

To understand the mechanism behind the observed sub-60 mV/dec switching behaviour and internal voltage amplification in the WS_2 MIMIS device, we have performed circuit simulations of the charging dynamics during the I_D – V_G scan based on an equivalent circuit model shown in Fig. 6.3(a). In the equivalent circuit, we are considering the quantum capacitance of the WS_2 channel C_q, the oxide capacitance of HfO_2 dielectric C_{ox}, the parasitic capacitance of the internal gate to the substrate C_p, and the capacitance of the AlO_x dielectric between gate and the internal gate C_{int-G}. The leakage current in the AlO_x capacitor is modelled as a linear resistor R to simplify the discussion, although the leakage current is non-linear with voltage. Since the parasitic capacitance of the internal gate to substrate C_p is much larger than C_{ox} and C_q (see Section 6.7.1), it is reasonable to consider only C_p and ignore C_{ox} and C_q in the simulation of the V_{int} response. The parameters used in the simulation are (Section 6.7.1):

$C_p = 9.59 \times 10^{-13}$ F, $C_{int-G} = 7.75 \times 10^{-15}$ F, $R = 6 \times 10^{11}$ Ω.

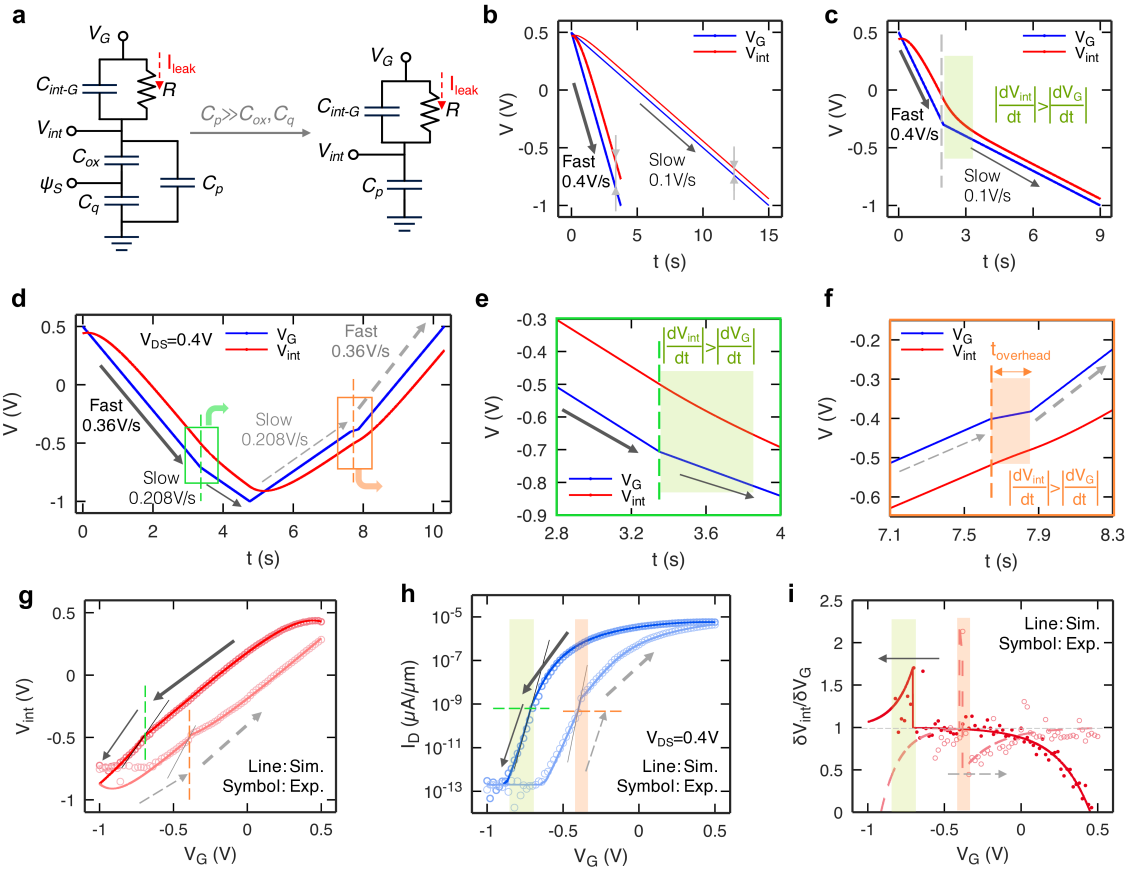


Figure 6.3. Simulation of the charging dynamics in the I_D – V_G scan of the MIMIS device. (a) Circuit model of the MIMIS device. (b) Simulated V_{int} response to different V_G scan rates. (c) Simulated V_{int} response to V_G scan with varying scan rates, showing different transient voltage amplification during transition from fast scan to slow scan. (d) Simulated V_G scan and V_{int} response during the I_D – V_G scan of the WS_2 MIMIS FET. (e) Enlarged views of the V_G scan and (f) V_{int} response, showing different transient voltage amplification during transitions of scan rates. (g) Simulated V_{int} – V_G during the I_D – V_G scan. (h) Simulated I_D – V_G characteristics of the MIMIS device. (i) Simulated internal voltage gain $\delta V_{int}/\delta V_G$ – V_G during the I_D – V_G scan. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

Next, we calculate the V_{int} response to a given V_G scan. From Kirchhoff's Current Law (KCL) at the V_{int} node, we have:

$$I_{leak} = \frac{V_G - V_{\text{int}}}{R} = \frac{d}{dt}[C_p V_{\text{int}} - C_{\text{int}-G}(V_G - V_{\text{int}})] \tag{6.1}$$

$$\frac{dV_{\text{int}}}{dt} = \frac{V_G - V_{\text{int}}}{R(C_p + C_{\text{int}-G})} + \frac{C_{\text{int}-G}}{C_p + C_{\text{int}-G}} \frac{dV_G}{dt} \tag{6.2}$$

Let $dV_{\text{int}}/dt = dV_G/dt$, we have the steady state response:

$$V_G - V_{\text{int}} = RC_p \frac{dV_G}{dt} \tag{6.3}$$

As indicated by Eq. 6.3, the difference between V_{int} and V_G at steady state is proportional to the RC time constant (which is 0.58 s for the parameters chosen here) and the V_G sweep rate (dV_G/dt), which agrees with the simulated V_{int} responses to different V_G scan rates in Fig. 6.3(b). Now if we think about a varying the V_G sweep rate ["fast" to "slow", Fig. 6.3(c)], there is a transition period [green shaded area in Fig. 6.3(c)] during which the difference between V_{int} and V_G changes from one steady state to another, and in this transition period we have $|dV_{\text{int}}/dt| > |dV_G/dt|$, which indicates a differential internal voltage amplification ($\delta V_{int}/\delta V_G > 1$).

From the above analysis, it is clear that in the RC circuit model, differential internal voltage amplification occurs when the gate sweep rate is changed from "fast" to "slow". Next, we identify such events in the experimental I_D – V_G measurement of the WS_2 MIMIS device. When measuring the transfer characteristics of a transistor, since the current range may span more than 7 orders of magnitude [as shown in Figs. 6.2(c) & 6.2(d)], auto ranging is typically adopted by the semiconductor parameter analyzer [163], and it is common to use slower scan rates for smaller current ranges to allow for longer integration times to reduce errors. On the other hand, faster scan rates are used for larger current ranges to increase measurement speed. In our measurement setup (see Methods), a "fast" scan rate of 0.36 V/s is adopted when the current level is above 1 nA (~0.6 nA/μm in the I_D – V_G curve,

normalized by channel width $W = 1.7$ μm), and a "slow" scan rate of 0.208 V/s is adopted when the current level is below 1 nA (Section 6.7.2 and Section 6.4).

Based on the findings, we reconstruct the V_G input as a function of time during the I_D – V_G scan of the WS_2 MIMIS device at V_{DS} =0.4 V and simulate the V_{int} response based on Eq. 6.2, as shown in Fig. 6.3(d). In the real measurement, the V_G input is a staircase function of time t, instead of a linear function used in the simulation (Section 6.4). Yet due to the small step size (0.02 V), the difference is negligible. An initial condition $V_{int}(t = 0) = 0.43$ V is determined from the first datapoint in the measured V_{int} – V_G shown in Fig. 6.2(e). We monitor V_{int} and the respective I_D in the simulation and change the V_G sweep rate correspondingly when the current level reaches values above or below 1 nA to mimic the experimental setup. In the forward scan direction (0.5 V to −1 V) of the V_G sweep, we observe a differential internal voltage amplification when the V_G sweep rate changes from "fast" to "slow", indicated by the green shaded area in Fig. 6.3(e), which is in accordance with our previous analysis. In the backward scan direction (−1 V to 0.5 V), however, the scan rate change from "slow" to "fast" and should not result in the observed sub-60 mV/dec switching and differential voltage amplification shown in Figs. 6.2(d) & 6.2(f). The reason for the observed phenomenon, *i.e.*, again voltage amplification in the experiment, is that an overhead time $t_{overhead} \approx 0.22$ s is associated with the change of current measurement range, as indicated by the orange shaded area in Fig. 6.3(f). During the overhead time, V_G increases only by the scan step size $V_{step} = 0.02$ V, resulting in an equivalent scan rate of 0.091 V/s. Since dV_{int}/dt remains almost unchanged (Eq. 6.2) while dV_G/dt slows down significantly during the overhead time, a transient differential internal voltage amplification $|dV_{int}/dt| > |dV_G/dt|$ occurs. We have performed additional measurements while recording the waveform of V_G to confirm the overhead time, as shown in Section 6.4. Figs. 6.3(g) & 6.3(h) show the simulated internal gate voltage V_{int} and drain current I_D as a function of V_G, which shows good agreement with the experimental data. The experimentally observed characteristics, such as anti-clockwise hysteresis and sub-60 mV/dec switching in both sweeping directions, are reproduced in the simulation. The transition points of scan rates are indicated by the green and orange lines in the figures. Fig. 6.3(i) shows the simulated internal voltage gain $\delta V_{int}/\delta V_G$ as a function of V_G, which shows

good agreement with the experimental data not only qualitatively, but also quantitatively in terms of amplitudes of the internal voltage amplifications and the corresponding V_G positions. This clearly shows that our simple model captures the essential characteristics of the charging dynamics of the I_D – V_G measurement. Note that from Eq. 6.3, we can see that the voltage difference between V_{int} and V_G in the steady state is given by $RC_P \cdot (dV_G/dt)$, which is equal to 0.21 V and 0.12 V for "slow" and "fast" scan rates, respectively, and both are smaller than the voltage scan window of 1.5 V. If the RC time constant is too small, V_{int} would follow V_G completely; if the RC time constant is too large, V_{int} would not reach steady state within the voltage scan window. Therefore, the RC time constant needs to be comparable to the timescale of the V_G scan in order to see the described effects. As an example, the measurement of an MIMIS FET with larger AlO_x layer leakage resistance is shown in Section 6.7.6.

6.4 Direct measurement of the waveform of gate voltage

To verify our model, we perform a direct measurement of the waveform of gate voltage during I_D – V_G characterization. Fig. 6.4(a) shows the schematic of measurement setup for measuring the waveforms of test signals. A parameter analyzer (Agilent 4156C, denoted as "parameter analyzer #1") was used to generate the voltage signals to the device under test (DUT) and measure the currents, using source-measurement units (SMUs) 1, 2 and 3 for source, drain and gate (or internal gate, if measuring the internal FET), respectively. In order to measure the waveform of the gate voltage without disturbing the measurement of the actual DUT, we used an additional SMU 4 in the synchronous sweep measurement mode, which effectively "copies" the voltage output from SMU 3, *i.e.*, the gate voltage, and used an additional parameter analyzer (Agilent 4156C, denoted as "parameter analyzer #2") in sampling measurement mode to record the waveform of the "copied" gate voltage from parameter analyzer #1.

Next, we measure the device transfer characteristics and record the waveforms of the gate voltage during the measurement. Note that we have performed these measurements on a different device from the same batch as the device described in Section 6.2. Fig. 6.4(b) shows

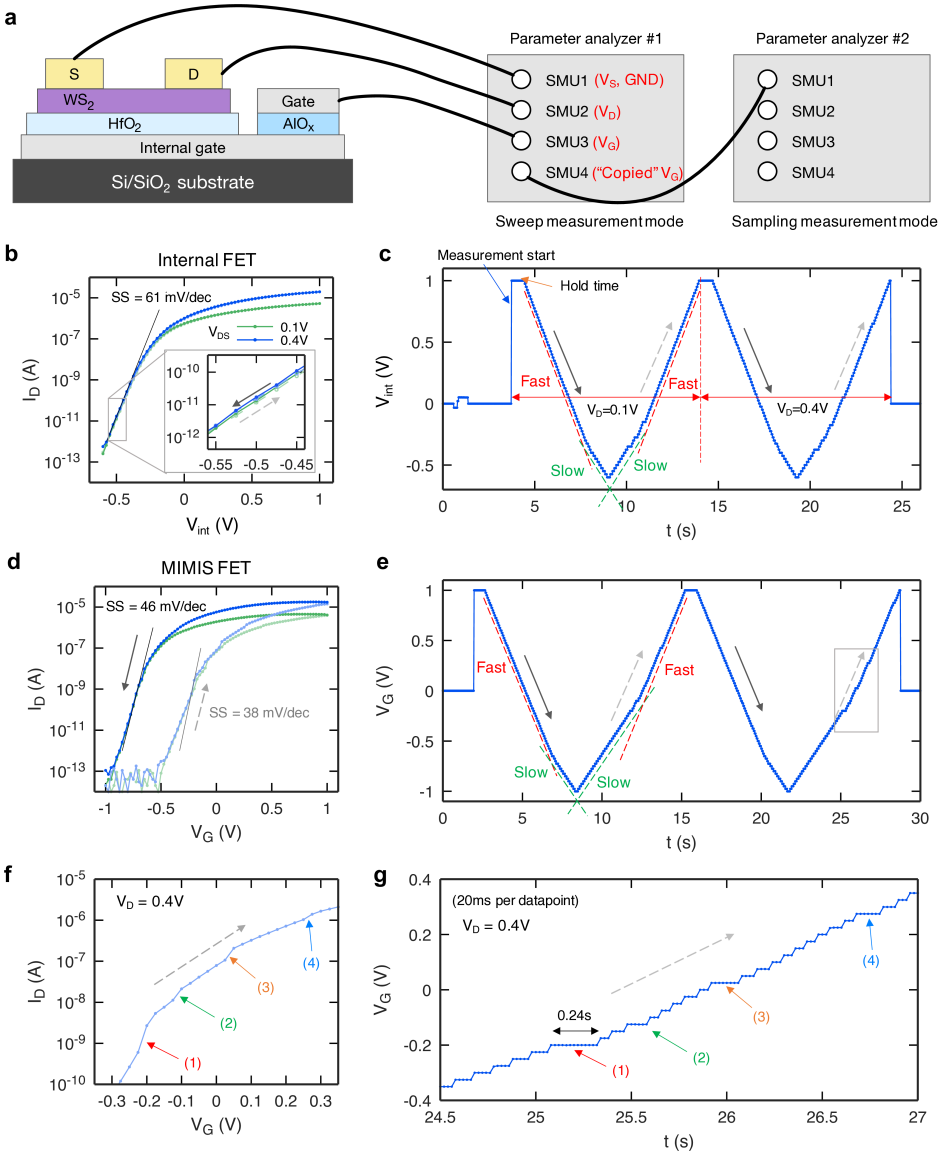


Figure 6.4. Measurement of waveforms of gate voltage. (a) Schematic of measurement setup for measuring testing signals using the sampling measurement of the parameter analyzer. (b) I_D – V_{int} characteristics of the internal FET. (c) Measured waveform of V_{int} as a function of time. (d) I_D – V_G characteristics of the MIMIS FET. (e) Measured waveform of V_G as a function of time. (f) Enlarged view of I_D – V_G characteristics of the MIMIS FET in the backward scan direction at $V_D = 0.4$ V. (g) Enlarged view of measured waveform of V_G as a function of time. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

the measured I_D – V_{int} characteristics of the internal FET. The internal FET exhibits an SS-value of 61 mV/dec and negligible hysteresis. Fig. 6.4(c) shows the measured waveform of V_{int} as a function of time during the I_D – V_{int} measurement, from which one can observe the bidirectional sweeps of V_{int} at two different drain voltages and two distinctive scan rates, "fast" and "slow".

Fig. 6.4(d) shows the measured I_D – V_G characteristics of the MIMIS FET, from which one can observe an anticlockwise hysteresis and sub-60 mV/dec switching in both sweep directions. Fig. 6.4(e) shows the measured waveform of V_G as a function of time during the I_D – V_G measurement. In the forward scan direction (1 V to −1 V), one can observe a transition from "fast" scan rate to "slow" scan rate at $V_G = -0.7$ V, exactly the gate voltage at which the sub-60 mV/dec switching is observed. In the backward scan direction (−1 V to 1 V), with the directly measured waveform of V_G, one can see that there exist several plateau regions due to overhead times associated with measurement range changes. From the enlarged views of the I_D – V_G characteristics and measured V_G waveform shown in Fig. 6.4(f) and 4g, respectively, it becomes very apparent that there are four "kinks" in the I_D – V_G characteristics and four corresponding plateau regions in the V_G waveform, which are associated with the measurement range changes at 10^{-9} A, 10^{-8} A, 10^{-7} A and 10^{-6} A, respectively. Note that the overhead time at $V_G = -0.2$ V [labeled as "(1)"] is about 0.24 s, which is associated with the measurement range change at 10^{-9} A, where the transition from "slow" to "fast" scan rate occurs, and the value is in agreement with $t_{overhead} = 0.22$ s that was used in the simulation in Section 6.3.

6.5 Simulation of sub-60 mV/dec switching with constant V_G scan rate

We have simulated the characteristics of the WS_2 MIMIS device with varying V_G scan rates and have shown that transient sub-60 mV/dec switching can be observed due to internal voltage amplifications when the scan rate is changing. However, one may argue that while varying scan rates are common when characterizing transistors, a constant scan rate is achievable with proper configuration of measurement setups and thus the effects discussed in the previous section can be avoided (Section 6.7.5). To show that such effects are rather

universal and do not just apply to a particular scenario, we simulate the case of a constant V_G scan rate and show that sub-60 mV/dec switching can still be observed.

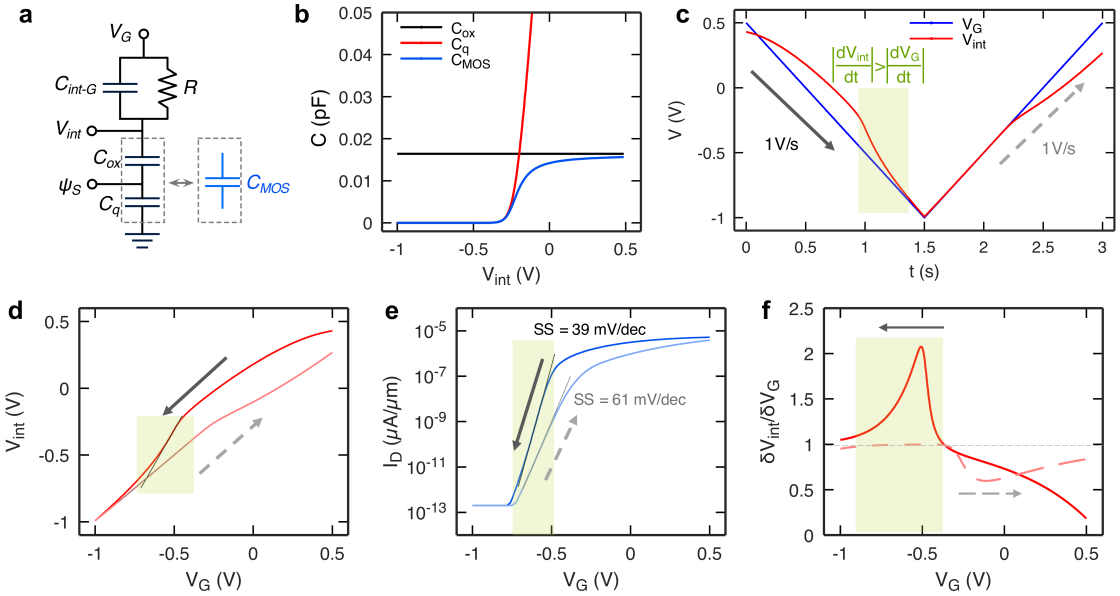


Figure 6.5. Simulation of charging dynamics of $I_D - V_G$ scan with a constant scan rate of an MIMIS device with voltage-dependent internal gate capacitance. (a) Circuit model of an MIMIS device without parasitic capacitance. Note that the internal gate capacitance CMOS is voltage dependent. (b) V_{int} dependence of oxide capacitance C_{ox}, quantum capacitance C_q and total internal gate capacitance CMOS. (c) Simulated V_{int} response to the V_G scan with a constant scan rate. (d) Simulated $V_{int} - V_G$ during the $I_D - V_G$ scan. (e) Simulated $I_D - V_G$ characteristics, showing sub-60 mV/dec switching in one scan direction. (f) Simulated internal voltage gain $\delta V_{int}/\delta V_G - V_G$ during the $I_D - V_G$ scan. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

In the previous section, the circuit under discussion had a constant RC time constant due to a large, constant parasitic capacitance C_p, and in combination with a time-varying V_G scan rate, sub-60 mV/dec switching can be observed. One can envision that with a constant V_G scan rate, yet in combination with a varying RC time "constant", similar effects could also be achieved. It is well-known that the gate capacitance of a MOSFET is voltage-dependent

[27], and for the 2D WS_2 transistor in this study, CMOS can be represented by the series of oxide capacitance C_{ox} and quantum capacitance [164], [165] C_q, which can be expressed by:

$$C_q = q^2 DOS_{2D} f(E_C) A_{device} = q^2 \frac{g_C m_e^*}{\pi\hbar^2} \frac{1}{1+\exp\left[(E_C - E_F)/k_B T\right]} A_{device} \tag{6.4}$$

where g_C is conduction band valley degeneracy, m_e^* is electron effective mass. From Eq. 6.4, we can see that C_q is dependent on the relative position of conduction band edge E_C and Fermi level E_F, which can be tuned with gate voltage, and by removing the parasitic capacitance from the circuit, we can achieve a voltage-dependent internal gate capacitance CMOS for the internal FET [Fig. 6.5(a)]. The elimination of parasitic capacitance C_p could be achieved by switching to an insulating substrate (see Section 6.7.1), such as sapphire, yet this would bring significant experimental challenges, such as identifying WS_2 flakes, compared with our current setup using a Si substrate with 90 nm SiO_2 on top. Fig. 6.5(b) shows the simulated C_{ox}, C_q and CMOS as a function of V_{int} (see Section 6.7.3). One can see that when V_{int} is negative and the internal WS_2 FET is in its off-state, C_q is nearly zero as the Fermi level E_F in WS_2 is in the bandgap, and thus CMOS is almost zero; when V_{int} increases and the internal WS_2 FET is turned on, C_q quickly increases and exceeds C_{ox} as the Fermi level E_F approaches the conduction band edge E_C, and thus CMOS approaches C_{ox}.

Next, we simulate the V_{int} response with a constant V_G scan rate and voltage-dependent CMOS, for which Eq. 6.1 and Eq. 6.2 are modified as follows:

$$\begin{aligned} I_{leak} &= \frac{V_G - V_{int}}{R} = \frac{d}{dt}[Q_{ch}(V_{int}) - C_{int-G} \times (V_G - V_{int})] \\ &= \frac{\partial Q_{ch}}{\partial V_{int}} \frac{dV_{int}}{dt} - C_{int-G} \frac{d(V_G - V_{int})}{dt} \\ &= [C_{MOS}(V_{int}) + C_{int-G}] \frac{dV_{int}}{dt} - C_{int-G} \frac{dV_G}{dt} \end{aligned} \tag{6.5}$$

$$\frac{dV_{int}}{dt} = \frac{V_G - V_{int}}{R[C_{MOS}(V_{int}) + C_{int-G}]} + \frac{C_{int-G}}{C_{MOS}(V_{int}) + C_{int-G}} \frac{dV_G}{dt} \tag{6.6}$$

From Eq. 6.6, we simulate the V_{int} response to the V_G scan with a constant scan rate of 1 V/s, as shown in Fig. 6.5(c). We have also changed the parameter $R = 2\times10^{13}$ Ω to compensate for the removal of a large capacitance C_p to keep the RC time constant approximately the same ($RC_{ox} = 0.32$ s). A differential internal voltage amplification $|dV_{int}/dt| > |dV_G/dt|$ (green shaded area) is observed in the forward scan direction (0.5 V to −1 V), but not in the backward scan direction (−1 V to 0.5 V). Fig. 6.5(d) shows the simulated V_{int} as a function of V_G. Assuming the same I_D – V_{int} as in Fig. 6.2(c), I_D – V_G characteristics can be simulated [Fig. 6.5(e)], in which a sub-60 mV/dec switching is observed in the forward scan direction. Fig. 6.5(f) shows the simulated internal voltage gain $\delta V_{int}/\delta V_G$ as a function of V_G, in which the differential internal voltage amplification is clearly illustrated by the green shaded area.

6.6 Conclusion

In previous demonstrations of NC-FETs, observing sub-60 mV/dec switching has been deemed as a mark of success for steep-slope switching devices. However, the results in this work show that by putting a leaky capacitor in series with the gate of an FET, which is clearly not a solution to steep-slope switching devices, sub-60 mV/dec switching can also be observed. Such effects originate from transient voltage amplifications over a small voltage window ($\delta V_{int}/\delta V_G > 1$), instead of persistent voltage amplifications over the entire voltage scan range ($\Delta V_{int}/\Delta V_G > 1$) that is required for a real demonstration of low-voltage switching. The transient voltage amplification may occur during transitions between current measurement ranges, where changes in the voltage scan rates are typical, and even for a constant scan rate, an abrupt change of internal gate capacitance near threshold voltage V_{th} may lead to similar effects. Since the effects are caused by the charging dynamics in a non-ideal measurement setup, which is likely to be utilized in the characterization of NC-FETs by many, it is imperative to reassess the measurement setups in the previous reported sub-60 mV/dec switching NC-FETs with internal metal gates, to rule out such measurement-related artefacts and verify the existence of real voltage amplification predicted by the quasi-static NC theory.

6.7 Appendix

6.7.1 Determination of capacitance and resistance components in the RC network model

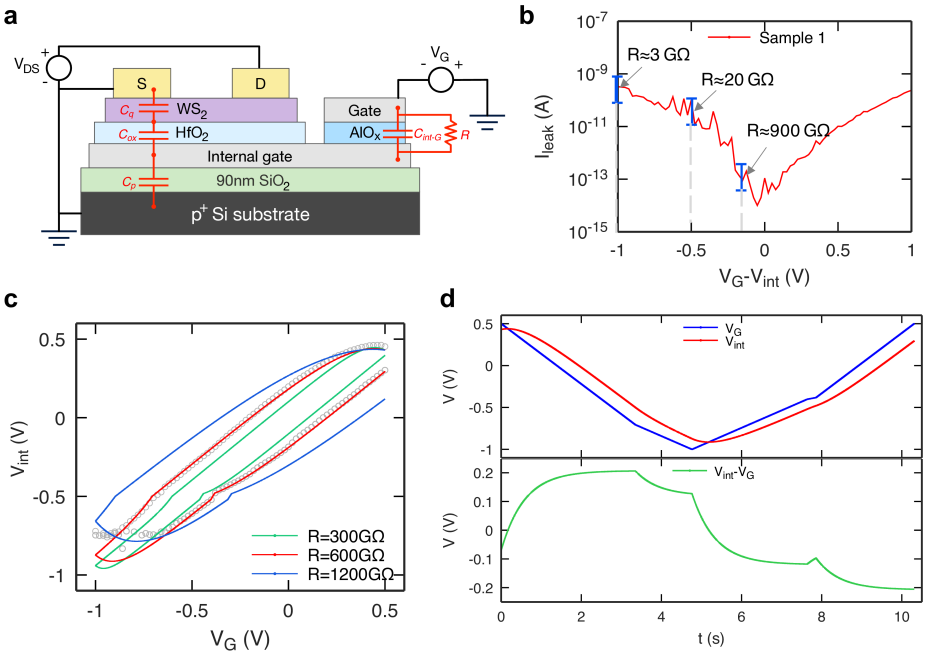


Figure 6.6. Determination of capacitance and resistance in the RC network model. (a), Schematic of capacitance and resistance components in the WS_2 MIMIS FET. (b) Leakage current I_{leak} in the AlO_x capacitor versus V_G-V_{int}, showing non-linear characteristics and different R values at different V_{diff}. (c) Simulated V_{int} – V_G for different R values. Line: simulation. Symbol: experiment. (d) Simulated V_G, V_{int} and V_{int}-V_G versus time t. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

Fig. 6.6(a) shows a schematic of the capacitance and resistance components in the WS_2 MIMIS device. The overlapping area of internal gate and gate is $A_{int-G} = 1\ \mu m^2$ and the area

of the contact pad for the internal gate is $A_{pad} = 50\ \mu\text{m} \times 50\ \mu\text{m} = 2500\ \mu\text{m}^2$, respectively. The device area of the WS_2 FET is $A_{device} = 1\ \mu\text{m}^2$. The capacitances can be calculated:

$$C_{int-G} = \frac{\epsilon_{AlO_x}\epsilon_0 A_{int-G}}{t_{AlO_x}} = \frac{7 \times 8.854 \times 10^{-12} \times 1 \times (10^{-6})^2}{8 \times 10^{-9}} = 7.75 \times 10^{-15}\ \text{F} \tag{6.7}$$

$$C_p = \frac{\epsilon_{SiO_2}\epsilon_0 A_{pad}}{t_{SiO_2}} = \frac{3.9 \times 8.854 \times 10^{-12} \times 50 \times (10^{-6})^2}{90 \times 10^{-9}} = 9.59 \times 10^{-13}\ \text{F} \tag{6.8}$$

$$C_{ox} = \frac{\epsilon_{HfO_2}\epsilon_0 A_{device}}{t_{HfO_2}} = \frac{13 \times 8.854 \times 10^{-12} \times 1 \times (10^{-6})^2}{7 \times 10^{-9}} = 1.64 \times 10^{-14}\ \text{F} \tag{6.9}$$

The calculation of C_q can be found in Section 6.7.3, yet since it's in series with C_{ox}, the total capacitance CMOS is smaller than C_{ox}. Note that C_p is ~60 times larger than C_{ox} for 90 nm SiO_2. Therefore, we can ignore CMOS when simulating the V_{int} response. As we illustrated in Fig. 6.5, if C_p could be eliminated, the effect of the voltage-dependent CMOS would become relevant and can lead to a steep switching even for a measurement with a constant scan rate. Yet with Si/SiO_2 substrates, it is challenging to achieve thicker than ~500 nm SiO_2 using typical thermal oxidation methods, which would only reduce C_p to ~1/6 of its current value, and C_p would still be 10× larger than C_{ox}. Therefore, C_p could not be eliminated by using a substrate with thicker SiO_2 dielectric. One possible solution is to switch to an insulating substrate, such as sapphire, yet this would make identifying flakes almost impossible.

Next, the resistance value for R is determined. Fig. 6.6(b) shows the leakage current I_{leak} in the AlO_x capacitor as a function of voltage difference $V_{diff} = V_G - V_{int}$, which clearly exhibits a non-linear behavior and different R values can be extracted at different V_{diff}-values. In addition, due to inaccuracies and noises in the measurement, there is a significant uncertainty associated with the extracted R value, especially when the current is small. Therefore, we have adopted an indirect method of extracting R by fitting the measured V_{int} – V_G curve, as shown in Fig. 6.6(c). As shown in Eq. 6.3, different R values lead to different $V_G - V_{int}$ values and thus different hysteresis voltage values in the bidirectional V_G scan. As

clearly shown in Fig. 6.6(c), $R = 600$ GΩ gives the best fit to the experimental data, while other values either underestimate or overestimate the hysteresis voltage. The good fitting also indicates that using a fixed value for R is a good approximation despite the non-linear I_{leak} – V_{diff} characteristics. Fig. 6.6(d) shows the simulated V_{int}-V_G as a function of time using the parameter $R = 600$ GΩ. The voltage difference is below 0.21 V during the V_G voltage scan, and from the I_{leak} – V_{diff} characteristics in Fig. 6.6(b), we can roughly estimate $R \approx 900$ GΩ at $V_G - V_{int} = -0.2$ V, which is in acceptable agreement with the extracted R = 600 GΩ.

6.7.2 Extraction of scan rates from experiment

Fig. 6.7(a) shows a single frame from a video of a researcher performing an I_D – V_G scan of the WS_2 MIMIS FET on the Agilent 4156C parameter analyzer. The measured I_D – V_G characteristics are shown in Fig. 6.7(b). Note that the measurement was performed ∼3 months after the initial measurement [Fig. 6.2(d)], and the characteristics have drifted slightly compared to the initial characterization. In particular, the hysteresis voltage had become larger, which indicates an increase in the resistance R of the AlO_x capacitor according to our analysis from the previous section. However, the main features, such as sub-60 mV/dec switching and anti-clockwise hysteresis, are still retained in the new measurement. We speculate that the resistance increase may be related to a decrease in oxygen vacancies while the AlO_x film is exposed to air. It has been shown in Refs. [166]–[169] that aluminum forms a natural oxide layer that acts as a decent gate dielectric after sufficiently long air exposure. Yet in our device, we limit the air exposure time of Al to ∼15 minutes before capping it with another metal layer. As a result, the AlO_x film may be sub-stoichiometric and likely contains oxygen vacancies, which contribute to the leaky behavior. It has also been reported in Ref. [166] that after AlO_x dielectric breaks down, it can "self-heal" upon further oxidation in air, which is in line with our speculation.

From the video, we extract the gate voltage V_G as a function of time t for $V_{DS} = 0.4$ V, as shown by the red dots in Fig. 6.7(c). It is clear that two distinct scan rates of 0.36 V/s ("fast") and 0.208 V/s ("slow") can be extracted from the measured V_G – t curve, which

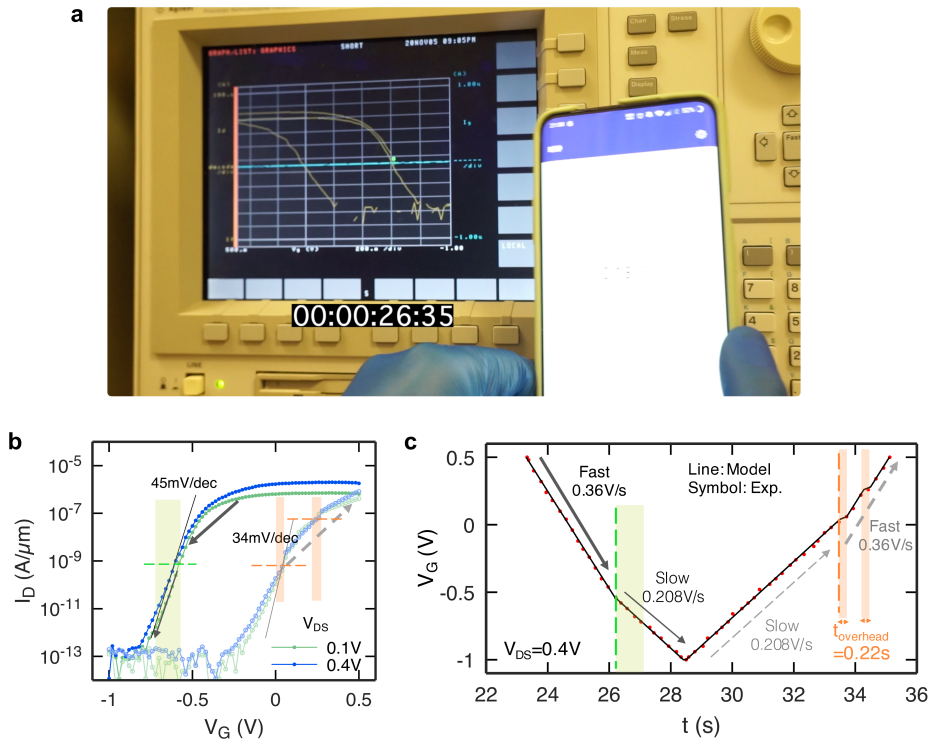


Figure 6.7. Extraction of scan rates from experiment. (a) A single frame from the video of performing an I_D – V_G scan on the WS_2 MIMIS FET. (b) Measured I_D – V_G characteristics. (c) V_G as a function of time, showing two scan rates at different current levels and overhead time in the backward scan direction. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

correspond to I_D above and below 1 nA (0.6 nA/μm), respectively. The values for the "fast" and "slow" scans are applied in the simulation for the V_{int} response in Section 6.3. In the forward scan direction (0.5 V to −1 V), sub-60 mV/dec switching is observed when the scan rate transitions from "fast" to "slow" at I_D = 1 nA (green shaded area). In the backward scan (−1 V to 0.5 V), two sub-60 mV/dec switching events are observed, one at I_D = 1 nA and another at I_D = 100 nA, which correspond to the overhead time associated with two measurement range changes, as shown by the orange shaded areas in Fig. 6.7(c). Interestingly, the second sub-60 mV/dec event at I_D = 100 nA was not observed in the initial measurement. The cause for the difference is still under investigation, which we speculate

might be from some minor changes in the settings of the parameter analyzer in the initial measurement and the new measurement, despite our effort of making them the same.

6.7.3 Calculation of quantum capacitance C_q

Fig. 6.8(a) shows the schematic of the capacitance model for the WS_2 internal FET. The quantum capacitance C_q of 2D WS_2 channel is given by:

$$C_q = \frac{\partial Q_{ch}}{\partial \psi_S} = q^2 DOS_{2D} f(E_C) A_{device} = q^2 \frac{g_C m_e^*}{\pi \hbar^2} \frac{1}{1 + \exp\left[(E_C - E_F)/k_B T\right]} A_{device} \tag{6.10}$$

Eq. 6.10 describes the dependence of C_q on the relative position of E_C and Fermi level E_F, or equivalently the surface potential ψ_S. In order to calculate the V_{int} dependence of C_q, we need to determine the relation of ψ_S and V_{int}, which is given by:

$$\frac{d\psi_S}{dV_{int}} = \frac{C_{ox}}{C_{ox} + C_q} \tag{6.11}$$

$$\psi_S = \frac{\Phi_{SB,n} + E_F - E_C}{q} \tag{6.12}$$

Note that we have chosen flat-band condition as the zero point for the potential ψ_S, *i.e.*, $\psi_S = 0$ when $V_{int} = V_{FB}$. For multilayer WS_2 in this study, we have:

$$g_C = 6, m_e^* = 0.22 m_0$$

The only missing parameters are the flat-band voltage V_{FB} and electron Schottky barrier height $\Phi_{SB,n}$. We extract these parameters by fitting experimental $I_D - V_{int}$ data with a Landauer model [8], [83], as shown in Fig. 6.8(b). Using the Landauer model, we extract the parameters:

$V_{FB} = -0.46$ V, $\Phi_{SB,n} = 0.33$ eV, and the screening length for Schottky barrier injection $\lambda = 2.6$ nm. Notice that above V_{th} (the extraction of its value will be discussed next), the simulated curve from Landauer model starts to deviate from experimental data. This is

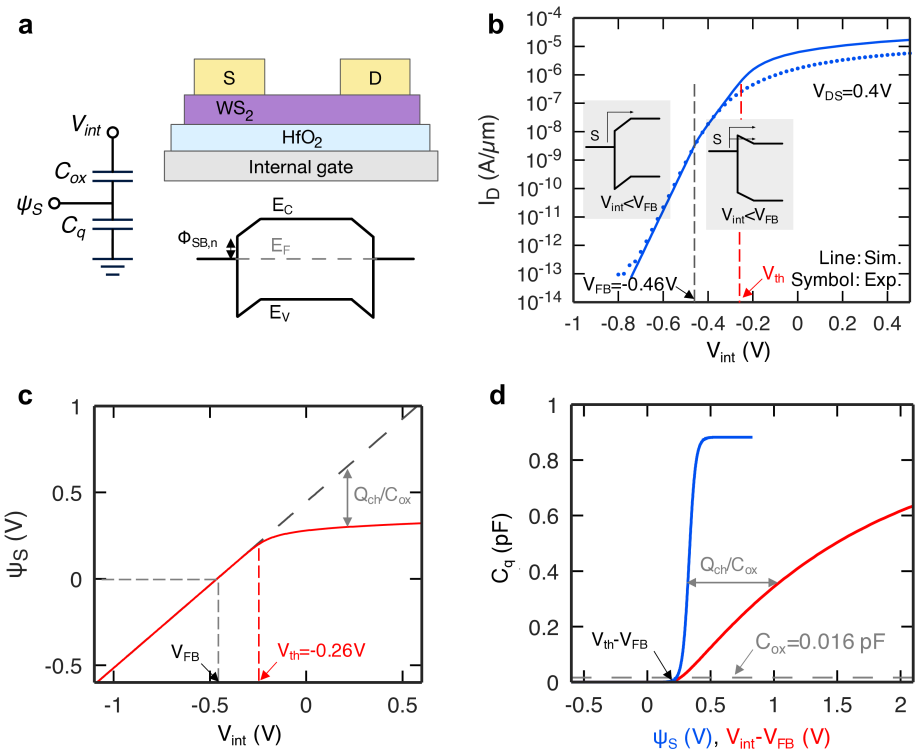


Figure 6.8. Calculation of quantum capacitance C_q. (a) Schematic of capacitance model of internal WS_2 FET and the band diagram. (b) Extraction of V_{FB} and $\Phi_{SB,n}$ using Landauer model. (c) Surface potential ψ_s as a function of internal gate voltage V_{int}. (d) Quantum capacitance as a function of ψ_s and $V_{int} - V_{FB}$. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

because the Landauer approach is based on a ballistic transport picture, while above V_{th}, electrons start to populate the channel and a diffusive picture should be adopted for the long channel device ($L \approx 0.6$ μm) in this study. However, the fitting for the data below V_{th}, where scattering can be ignored, is already sufficient to extract the critical parameters and we did not try to simulate the on-state of the device quantitatively.

Having determined the values of V_{FB} and $\Phi_{SB,n}$, we calculate ψ_S as a function of V_{int} based on Eqs. 6.11 & 6.12, as shown in Fig. 6.8(c). One can see that ψ_S is following V_{int} one-to-one below $V_{th} = -0.26$ V. Above V_{th}, channel charges Q_{ch} become significant and ψ_S starts to saturate and deviate from the one-to-one relation.

Finally, we calculate C_q as a function of ψ_S based on Eq. 6.10, as shown by the blue line in Fig. 6.8(d). One would expect C_q to show up as a step function of ψ_S at T = 0 K, yet at finite temperatures, the transition becomes more gradual due to thermal broadening. By applying the ψ_S – V_{int} relation shown in Fig. 6.8(c), we can determine C_q as a function of V_{int}, as shown by the red line in Fig. 6.8(d). Note that $C_{q,max} \gg C_{ox}$, which indicates CMOS, the series capacitance of C_{ox} and C_q, will quickly saturate to C_{ox} once V_{int} is above V_{th}, as shown in Fig. 6.5(b).

6.7.4 Measurement of internal FET with different scan rates and hold time

We have measured the internal FET with different scan rates and hole time t_{hold} to highlight that the near ideal SS and small hysteresis are independent to measurement setup. Figs. 6.9(a) and 6.9(b) show the measured I_D – V_{int} characteristics of the internal FET and waveform of V_{int} during the measurement with t_{delay} = 0 s and t_{hold} = 0.5 s. A near ideal slope of 61 mV/dec and negligible hysteresis are observed in the I_D – V_{int} characteristics. The resulting scan rates are 0.39 V/s ("fast") and 0.236 V/s ("slow") for current levels above and below 10^{-9} A, respectively. Note that the values are different from 0.36 V/s ("fast") and 0.208 V/s ("slow") that were used in Section 6.3, since a different voltage step size (0.025 V, instead of 0.02 V in Section 6.2) were used here unintentionally. Figs. 6.9(c) and 6.9(d) show the measured I_D – V_{int} characteristics of the internal FET and waveform of V_{int} during the measurement with t_{delay} = 0.5 s and t_{hold} = 5 s. A near ideal slope of 60 mV/dec and negligible hysteresis are observed in the I_D – V_{int} characteristics, despite the much slower scan rate of 0.044 V/s. Note that the I_D – V_{int} characteristics are shifted by about −0.1 V in Fig. 6.9(c) compared with Fig. 6.9(a), possibly due to trapped charges induced by repeated measurements. Also note that a few outlier points in the backward scan direction at V_D = 0.4 V in Fig. 6.9(c) are a result of an unstable contact between the probe tips and the metal pads for source/drain electrodes, which we found to be occurring in prolonged measurements (> 100 s), possibly due to vibrations loosening the contact.

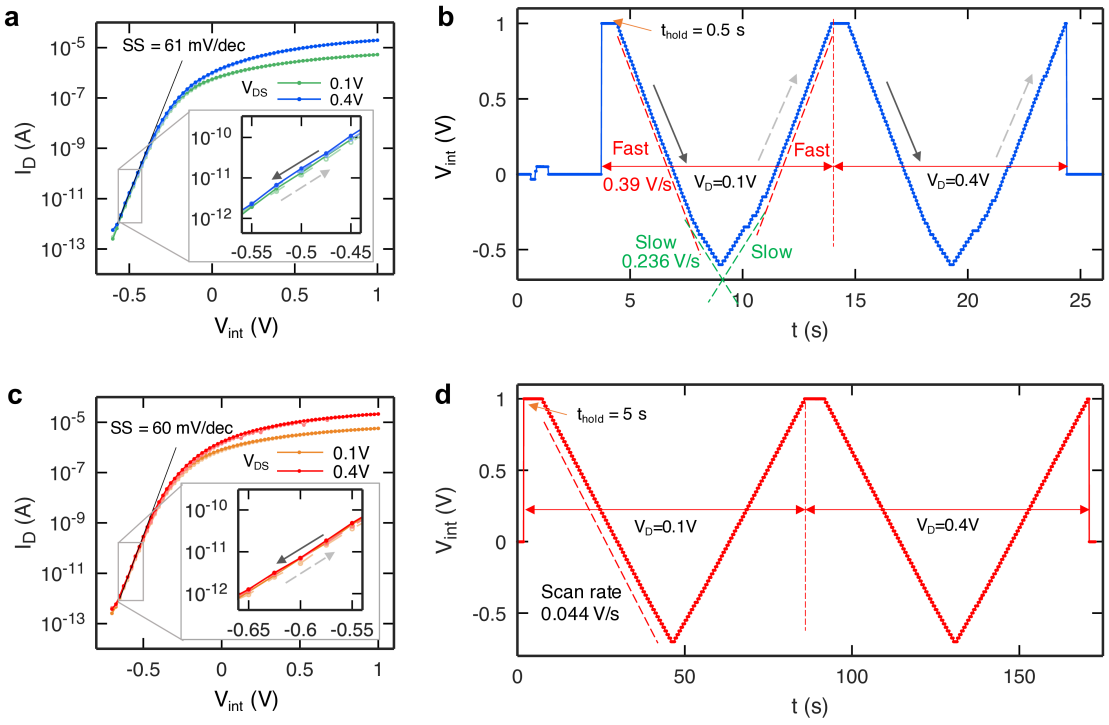


Figure 6.9. Measurement of internal FET with different scan rates. (a) I_D – V_{int} characteristics of the internal FET with t_{delay} = 0 s and t_{hold} = 0.5 s. (b) Measured waveform of V_{int} as a function of time with t_{delay} = 0 s and t_{hold} = 0.5 s. (c) I_D – V_{int} characteristics of the internal FET with t_{delay} = 0.5 s and t_{hold} = 5 s. (d) Measured waveform of V_{int} as a function of time with t_{delay} = 0.5 s and t_{hold} = 5 s. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

6.7.5 Measurement of MIMIS FET with constant gate voltage scan rate

In Section 6.3, we have attributed the sub-60 mV/dec switching in the MIMIS FET to varying scan rates of gate voltage V_G. Since the capacitance in the RC circuit model is dominated by the constant parasitic capacitance C_p, we expect no steep switching behavior for a constant V_G scan rate. Here, we characterize the MIMIS FET with a constant V_G scan rate to verify our theory.

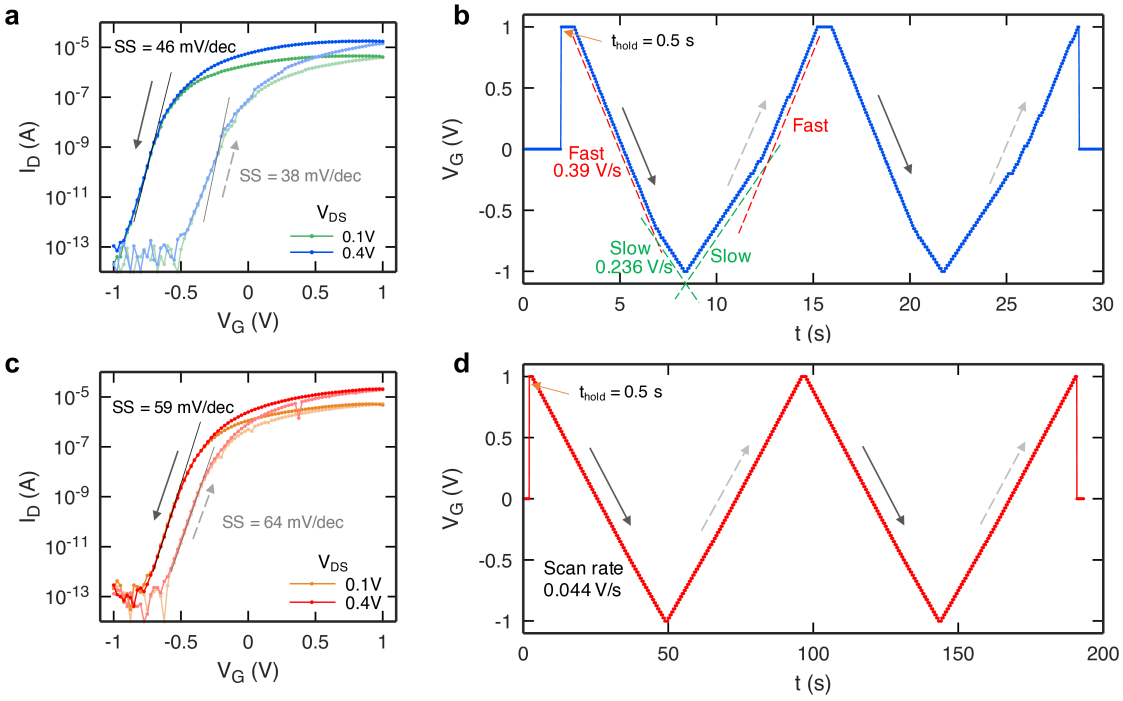


Figure 6.10. Measurement of MIMIS FET with different scan rates. (a) I_D – V_G characteristics of the MIMIS FET with t_{delay} = 0 s and t_{hold} = 0.5 s. (b) Measured waveform of V_G as a function of time with t_{delay} = 0 s and t_{hold} = 0.5 s. (c) I_D – V_G characteristics of the MIMIS FET with t_{delay} = 0.5 s and t_{hold} = 0.5 s. (d) Measured waveform of V_G as a function of time with t_{delay} = 0.5 s and t_{hold} = 0.5 s. A constant scan rate is obtained. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

Figs. 6.10(a) and 6.10(b) show the measured I_D – V_G characteristics of the MIMIS FET and waveform of V_G during the measurement with t_{delay} = 0 s and t_{hold} = 0.5 s, which leads to varying scan rates of 0.39 V/s ("fast") and 0.236 V/s ("slow") for current levels above and below 10^{-9} A, respectively. As we have analyzed in Section 6.3 and Section 6.4, in the forward scan direction (1 V to −1 V), one can observe sub-60 mV/dec switching at $V_G = -0.7$ V, at which the scan rate changes from "fast" to "slow", and in the backward scan direction (−1 V to 1 V), steep switching can be observed when the auto-ranging of the parameter analyzer changes the measurement range, which leads to an overhead time.

Figs. 6.10(c) and 6.10(d) show the measured I_D – V_G characteristics of the MIMIS FET and waveform of V_G during the measurement with t_{delay} = 0.5 s and t_{hold} = 0.5 s, which leads to a constant scan rate of 0.044 V/s. As expected, no steep switching behaviors are observed in the transfer characteristics. Please note that this is an expected behavior due to a large, constant parasitic capacitance C_p being dominant in the RC network model, and as we illustrated in Fig. 6.5, if C_p could be eliminated, a steep switching behavior could still be observed even with a constant scan rate. As we have mentioned in Section 6.7.4, the outlier points in Fig. 6.10(c) are a result of unstable contact between the probe tips and the metal pads for source/drain electrodes, which we found to be occurring for prolonged measurements (> 100 s), possibly due to vibrations loosening the contact. Also note that a finite hysteresis still exists even for a constant scan rate in Fig. 6.10(c), which is a result of the leaky dielectric, yet the hysteresis is much smaller due to a slower scan rate, which is in agreement with our calculation in Eq. 6.3.

6.7.6 Measurement of MIMIS FET with larger AlO_x layer leakage resistance

Fig. 6.11(a) shows the leakage currents of the AlO_x capacitors as a function of applied voltage in two different samples, where Sample 1 denotes the device in Section 6.2 and Sample 4 denotes another device in the same batch that happens to have much lower leakage current. One can see that in this device, the leakage current is below the noise floor of the measurement (10^{-13} A) when the applied voltage $V_{diff} = V_G - V_{int}$ is below ±1 V. Fig. 6.11(b) shows the I_D – V_{int} characteristics of the internal FET in Sample 4, in which near ideal SS and hysteresis-free characteristics are observed. Fig. 6.11(c) shows the I_D – V_G characteristics of the MIMIS FET in Sample 4 with different voltage scan ranges. When the scan range is 1 V to −1.2 V, the device cannot be turned off, which is distinctively different from the MIMIS FET in Sample 1, shown in Fig. 6.2(b). When the scan range is extended to 1 V to −1.4 V, the OFF-current can reach a lower value of below 1 nA. Finally, when the scan range is extended to 1 V to −1.6 V, the device is able to turn off completely, and steep-slope switching are again observed in both scan directions. The I_D – V_G characteristics of the MIMIS FET with different voltage scan ranges are compiled in a single plot in Fig.

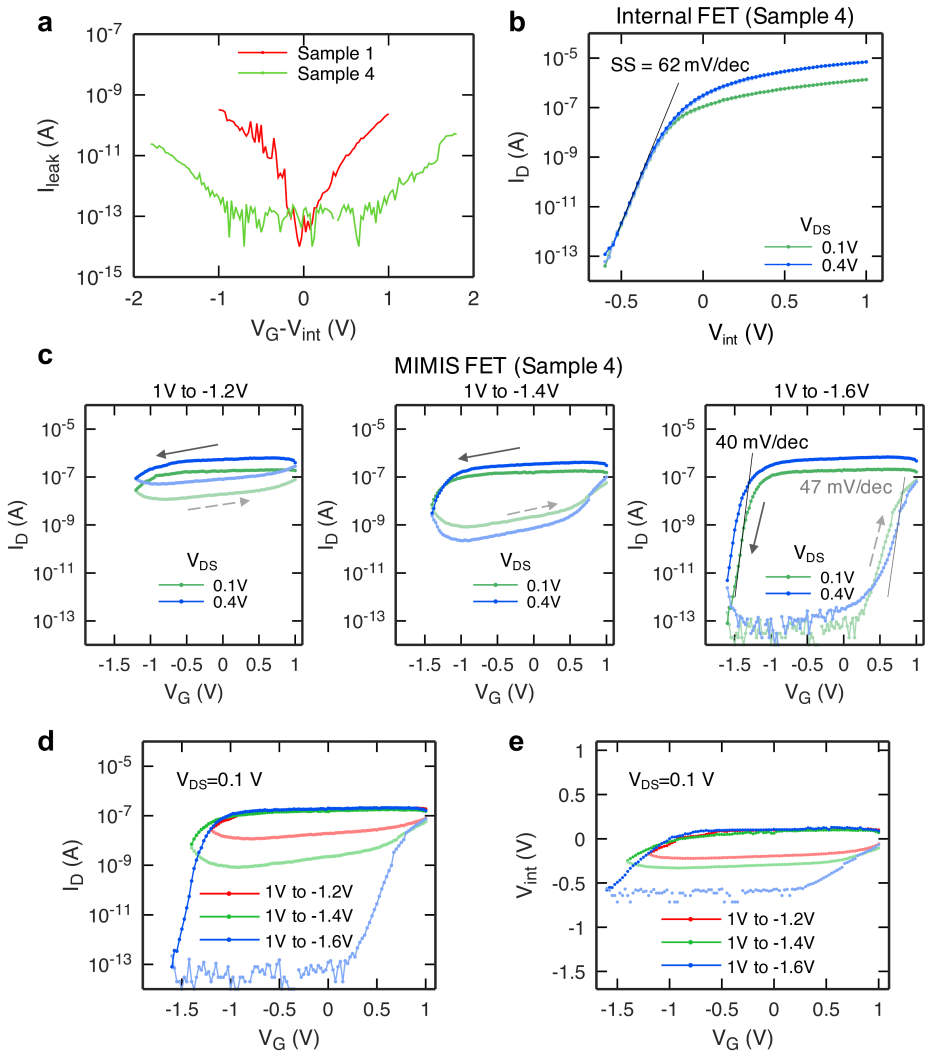


Figure 6.11. Measurement of MIMIS FET with large AlO_x layer leakage resistance. (a) I_{leak} – V_{diff} characteristics of the AlO_x capacitors in two different samples. (b) I_D – V_{int} characteristics of the internal FET. (c) I_D – V_G characteristics of the MIMIS FET with different voltage scan ranges. (d) A compilation of I_D – V_G characteristics of the MIMIS FET with different voltage scan ranges. (e) Extracted V_{int} as a function of V_G during I_D – V_G measurement with different voltage scan ranges. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

6.11(d), and combined with I_D – V_{int} characteristics, we derive the V_{int} – V_G relations under different V_G scan ranges, as shown in Fig. 6.11(e). From the V_{int} – V_G plot, we can see that in the forward scan direction, V_{int} remains almost unchanged at 0 V until V_G reaches below −1 V, after which I_{leak} starts to show up, allowing V_{int} to follow V_G while maintaining the voltage difference. The scan in the backward scan direction shows a similar behavior, although with $V_{diff} = V_G - V_{int}$ changing its polarity. The V_G scan window needs to be large enough to allow V_{diff}, and thus I_{leak}, to be large enough in order to see the complete switching. Interestingly, this plot in some way resembles the minor and major P – E loop scans in ferroelectric materials.

Another way to understand this observation is already discussed in Section 6.3: "the RC time constant needs to be comparable to the timescale of the V_G scan in order to see the described effects." Note that the leaky AlO_x film is a highly nonlinear resistor, which indicates that even if R is too large under small V_{diff}, under larger V_{diff}, R may become smaller and fall into the range in which the RC constant is comparable to the sweep time. In this interpretation, the V_G scan window also needs to be large enough to allow a large enough V_{diff} to make the RC time constant "compatible" with the sweep time.

6.7.7 Characterization of the thin Ti layer as internal gate electrode

In our device, a thin Ti layer was used as internal gate electrode. The reason for using a thin Ti layer is that it is well known that the evaporation process for depositing the AlO_x layer has a poor step coverage, and we intentionally used a thin Ti layer to avoid an excessive leakage current at the side wall, as depicted in Fig. 6.12(a).

To address a possible concern about the resistance of the thin Ti layer being too large, we have characterized the conductivity of the thin Ti layer with a nominal thickness of 2 nm, same as in our device, using a transfer length method (TLM) structure as shown in Fig. 6.12(b). A 3-μm-wide Ti stripe with 2 nm nominal thickness was deposited using e-beam evaporation and patterned using e-beam lithography and liftoff process, followed by patterning and deposition of 40 nm thick Ni contacts. Note that the Ti layer was exposed to air for ∼24 hours before patterning and depositing the Ni metal leads, which is much

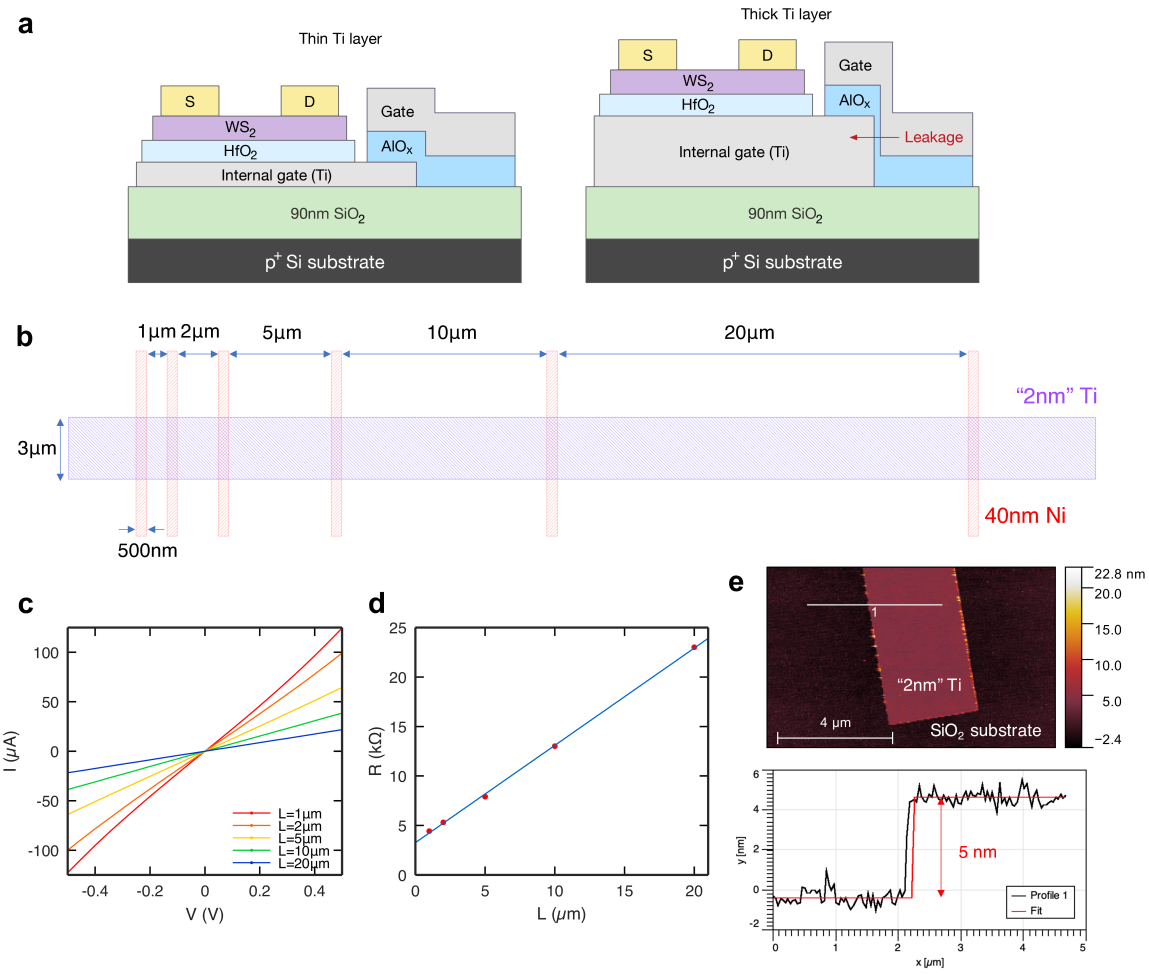


Figure 6.12. Characterization of thin Ti layer as internal gate electrode. (a) Schematic of step coverage of evaporated AlO_x with thin and thick Ti layers. (b) Schematic of the TLM structure. (c) $I - V$ characteristics of the Ti stripes with different lengths. (d) TLM measurement results. (e) AFM scan of the Ti layer. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

longer than the typical air exposure time for the Ti gate layer in our device. Therefore, any possible oxidation of Ti from air exposure is already taken into consideration in our test. Fig. 6.12(c) shows the $I - V$ characteristics of Ti stripes with different lengths. The linear $I - V$ characteristics indicates Ohmic contacts. Fig. 6.12(d) shows the TLM measurement results, from which we can extract a contact resistance of $2R_C = 3.26$ kΩ and a sheet resistance of

$R_{sheet} = 2.95$ kΩ/sq. Note that the resistance of the leaky AlO_x layer is ∼600 GΩ, which is more than seven orders of magnitude higher than the resistance of the Ti layer. Therefore, the voltage drop within the internal gate electrode can be ignored.

In addition, we have performed AFM scans on the "2 nm" Ti layer, as shown in Fig. 6.12(e), from which we found that the actual thickness of the Ti layer is 5 nm. This could be attributed to the crystal monitor in our evaporator not being well-calibrated for depositing thin films at a low evaporation rate (0.5 Å/s). A thickness change after Ti oxidizes in air could be another reason.

6.7.8 Gate leakage current during $I_D - V_G$ scan

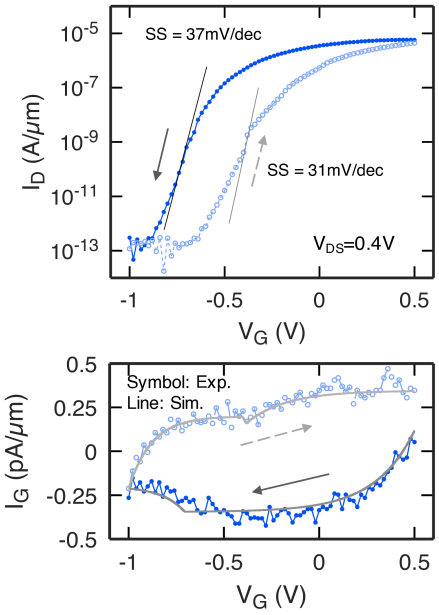


Figure 6.13. Measured and simulated $I_G - V_G$ during $I_D - V_G$ scan. Reprinted with permission from P. Wu, J. Appenzeller, "Artificial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor without Ferroelectric Component," *ACS Nano* **15**, 5158-5164 (2021). Copyright (2021) American Chemical Society.

Fig. 6.13 shows the gate leakage current I_G as a function of V_G during $I_D - V_G$ scan. We have also plotted the simulated $I_G - V_G$ curve from the RC network simulation in the figure, which shows very good agreement with the experiment. From the figure, we can see that

the points at which the leakage current changes polarity coincide with the points at which $V_G - V_{int}$ changes polarity, as predicted in the simulation shown in Fig. 6.6(d).

6.7.9 Methods

Device fabrication

Internal gate electrodes (5 nm Ti) were deposited using e-beam evaporation onto a silicon substrate with 90 nm of silicon dioxide on top and patterned using standard e-beam lithography and lift-off process. 7 nm of HfO_2 was deposited using atomic layer deposition (ALD) on top of the internal gate metal as dielectric for the internal WS_2 FET. The HfO_2 film was grown using a low-temperature (90 °C) ALD process and patterned using e-beam lithography and lift-off to expose part of the internal gate metal. Few-layer WS_2 flakes were exfoliated onto the local bottom gate structure from bulk crystals (purchased from HQGraphene). Ni (40 nm) electrodes were deposited and patterned by e-beam evaporation and e-beam lithography as source/drain contacts for the WS_2 FET. A thin aluminium film was deposited on the exposed internal gate metal using e-beam evaporation and oxidized in air for 15 minutes to form the leaky AlO_x dielectric. To make sure the Al is fully oxidized, the evaporation-oxidization was done in two steps (evaporation-oxidation-evaporation-oxidation) with 2 nm Al in each deposition, instead of 4 nm in a single deposition step. Finally, the gate metal (40 nm Ti) was deposited using e-beam evaporation and patterned using e-beam lithography and lift-off process.

Device characterization

The electrical characterization was performed in a LakeShore FWPX Probe Station at a vacuum level below 10^{-5} Torr using an Agilent 4156C Parameter Analyzer. All measurements were performed at room temperature. The sweep measurement in the parameter analyzer has the following settings:

Primary sweep (VAR1): V_G, start voltage: 0.5 V, end voltage: -1 V, step voltage: 0.02 V, double sweep: enabled, compliance: 1e-7 A

Subordinate sweep (VAR2): V_D, start voltage: 0.1 V, step voltage: 0.3 V, no. of steps: 2, compliance: 1e-1 A

Measurement ranging mode: auto ranging, integration time: SHORT, hold time: 0.5 s, delay time: 0 s

7. SUMMARY

Since the discovery of two-dimensional materials, their applications in transistors have been extensively studied. The unique properties of 2D materials enable novel applications that are beyond the scope of conventional CMOS transistors. In this thesis, we have discussed the applications of 2D materials in steep-slope tunneling FETs for low-power electronics and reconfigurable transistors for hardware security.

For tunneling FETs, the atomically thin nature of 2D materials allows aggressive scaling down of channel thickness for a small tunneling distance in order to achieve a large I_{on} and steep SS. In particular, black phosphorus is an ideal 2D material for TFET applications due to its moderate bandgap and small effective mass. In this thesis, for the first time, we have demonstrated a prototype BP TFET, and the multi-gate structure and electrostatic doping enable reconfigurable operations between MOSFET and TFET modes. Furthermore, we discuss the improvement of performance, including I_{on} and SS, by further scaling down t_{body} and t_{ox} in the BP TFET.

For reconfigurable transistors, Schottky-barrier tunneling in 2D nano-transistors enables ambipolar conduction, namely, allowing both hole injection and electron injection into the channel. However, the ambipolarity causes degraded on-off ratios at large V_{ds} values due to injection from the drain side. In this thesis, we discuss the strategies to suppress the drain injection currents and achieve unipolar conduction and large on-off ratios in reconfigurable BP transistors that can switch between p-FET and n-FET modes. Based on such reconfigurable transistors, we demonstrate a security primitive circuit, a polymorphic gate that can switch between NAND and NOR functionalities, showing the potential of integrating 2D materials for hardware security applications.

In addition, through studying the charging dynamics during the characterization of an MIMIS device, we show that an artificial sub-60 mV/dec switching can be observed due to transient effects. Therefore, researchers working on steep-slope devices such as NC-FETs need to pay particular attention to their measurement setups to avoid such artifacts.

REFERENCES

[1] A. D. Franklin, "Nanomaterials in transistors: From high-performance to thin-film applications," *Science*, vol. 349, no. 6249, aab2750–aab2750, 2015, ISSN: 0036-8075. DOI: 10.1126/science.aab2750.

[2] K. S. Novoselov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004, ISSN: 0036-8075. DOI: 10.1126/science.1102896.

[3] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnology*, vol. 6, no. 3, pp. 147–150, 2011, ISSN: 1748-3387. DOI: 10.1038/nnano.2010.279.

[4] S. Das, H. Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High performance multilayer MoS_2 transistors with scandium contacts," *Nano Letters*, vol. 13, no. 1, pp. 100–105, 2013, ISSN: 15306984. DOI: 10.1021/nl303583v.

[5] S. Das and J. Appenzeller, "WSe_2 field effect transistors with enhanced ambipolar characteristics," *Applied Physics Letters*, vol. 103, no. 10, p. 103 501, 2013, ISSN: 0003-6951. DOI: 10.1063/1.4820408.

[6] G. R. Bhimanapati, Z. Lin, V. Meunier, Y. Jung, J. Cha, S. Das, D. Xiao, Y. Son, M. S. Strano, V. R. Cooper, L. Liang, S. G. Louie, E. Ringe, W. Zhou, S. S. Kim, R. R. Naik, B. G. Sumpter, H. Terrones, F. Xia, Y. Wang, J. Zhu, D. Akinwande, N. Alem, J. A. Schuller, R. E. Schaak, M. Terrones, and J. A. Robinson, "Recent Advances in Two-Dimensional Materials beyond Graphene," *ACS Nano*, vol. 9, no. 12, pp. 11 509–11 539, 2015, ISSN: 1936-0851. DOI: 10.1021/acsnano.5b05556.

[7] L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, and Y. Zhang, "Black phosphorus field-effect transistors," *Nature Nanotechnology*, vol. 9, no. 5, pp. 372–377, 2014, ISSN: 1748-3387. DOI: 10.1038/nnano.2014.35.

[8] A. V. Penumatcha, R. B. Salazar, and J. Appenzeller, "Analysing black phosphorus transistors using an analytic Schottky barrier MOSFET model," *Nature Communications*, vol. 6, p. 8948, 2015, ISSN: 2041-1723. DOI: 10.1038/ncomms9948.

[9] P. Wu, T. Ameen, H. Zhang, L. L. A. Bendersky, H. Ilatikhameneh, G. Klimeck, R. Rahman, A. A. V. Davydov, and J. Appenzeller, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano*, vol. 13, no. 1, pp. 377–385, 2019, ISSN: 1936086X. DOI: 10.1021/acsnano.8b06441.

[10] L. Tao, E. Cinquanta, D. Chiappe, C. Grazianetti, M. Fanciulli, M. Dubey, A. Molle, and D. Akinwande, "Silicene field-effect transistors operating at room temperature," *Nature Nanotechnology*, vol. 10, no. 3, pp. 227–231, 2015, ISSN: 1748-3387. DOI: 10.1038/nnano.2014.325.

[11] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Materials*, vol. 6, no. 3, pp. 183–191, 2007, ISSN: 1476-1122. DOI: 10.1038/nmat1849.

[12] R. Dennard, F. Gaensslen, H.-N. Yu, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974, ISSN: 0018-9200. DOI: 10.1109/JSSC.1974.1050511.

[13] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Physical Review Letters*, vol. 93, no. 19, pp. 1–4, 2004, ISSN: 00319007. DOI: 10.1103/PhysRevLett.93.196805.

[14] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011, ISSN: 0028-0836. DOI: 10.1038/nature10679.

[15] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *physica status solidi (a)*, vol. 205, no. 4, pp. 679–694, 2008, ISSN: 18626300. DOI: 10.1002/pssa.200723528.

[16] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, 2010, ISSN: 0018-9219. DOI: 10.1109/JPROC.2010.2070470.

[17] I. Young, *Transistors Keep Moore's Law Alive*, 2018. [Online]. Available: https://www.eetimes.com/transistors-keep-moores-law-alive/ (visited on 12/12/2018).

[18] L. L. Chang and L. Esaki, "Tunnel triode—a tunneling base transistor," *Applied Physics Letters*, vol. 31, no. 10, pp. 687–689, 1977, ISSN: 0003-6951. DOI: 10.1063/1.89505.

[19] J. Quinn, G. Kawamoto, and B. McCombe, "Subband spectroscopy by surface channel tunneling," *Surface Science*, vol. 73, pp. 190–196, 1978, ISSN: 00396028. DOI: 10.1016/0039-6028(78)90489-2.

[20] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, "A new three-terminal tunnel device," *IEEE Electron Device Letters*, vol. 8, no. 8, pp. 347–349, 1987, ISSN: 0741-3106. DOI: 10.1109/EDL.1987.26655.

[21] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai, "A band to band tunneling MOS device (B_2T-MOSFET)-a kind of 'Si quantum device'," in *Technical Digest., International Electron Devices Meeting*, IEEE, 1988, pp. 402–405. DOI: 10.1109/IEDM.1988.32841.

[22] T. Baba, "Proposal for Surface Tunnel Transistors," *Japanese Journal of Applied Physics*, vol. 31, no. Part 2, No. 4B, pp. L455–L457, 1992, ISSN: 0021-4922. DOI: 10.1143/JJAP.31.L455.

[23] W. M. Reddick and G. A. J. Amaratunga, "Silicon surface tunnel transistor," *Applied Physics Letters*, vol. 67, no. 4, pp. 494–496, 1995, ISSN: 0003-6951. DOI: 10.1063/1.114547.

[24] J. Koga and A. Toriumi, "Negative differential conductance at room temperature in three-terminal silicon surface junction tunneling device," *Applied Physics Letters*, vol. 70, no. 16, pp. 2138–2140, 1997, ISSN: 0003-6951. DOI: 10.1063/1.118970.

[25] W. Hansch, C. Fink, J. Schulze, and I. Eisele, "A vertical MOS-gated Esaki tunneling transistor in silicon," *Thin Solid Films*, vol. 369, no. 1-2, pp. 387–389, 2000, ISSN: 00406090. DOI: 10.1016/S0040-6090(00)00896-8.

[26] C. Aydin, A. Zaslavsky, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, "Lateral interband tunneling transistor in silicon-on-insulator," *Applied Physics Letters*, vol. 84, no. 10, pp. 1780–1782, 2004, ISSN: 0003-6951. DOI: 10.1063/1.1668321.

[27] S. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2006, ISBN: 9780470068328. DOI: 10.1002/0470068329.

[28] J. Knoch, S. Mantl, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," *Solid-State Electronics*, vol. 51, no. 4, pp. 572–578, 2007, ISSN: 00381101. DOI: 10.1016/j.sse.2007.02.001.

[29] Y. Bi, X. S. Hu, Y. Jin, M. Niemier, K. Shamsi, and X. Yin, "Enhancing Hardware Security with Emerging Transistor Technologies," in *Proceedings of the 26th edition on Great Lakes Symposium on VLSI - GLSVLSI '16*, vol. 18-20-May-, New York, New York, USA: ACM Press, 2016, pp. 305–310, ISBN: 9781450342742. DOI: 10.1145/2902961.2903041.

[30] P. Wu and J. Appenzeller, "Toward CMOS like devices from two-dimensional channel materials," *APL Materials*, vol. 7, no. 10, p. 100 701, 2019, ISSN: 2166-532X. DOI: 10.1063/1.5115147.

[31] Y. Ren, X. Yang, L. Zhou, J. Y. Mao, S. T. Han, and Y. Zhou, "Recent Advances in Ambipolar Transistors for Functional Applications," *Advanced Functional Materials*, vol. 29, no. 40, pp. 1–65, 2019, ISSN: 16163028. DOI: 10.1002/adfm.201902105.

[32] N. Haratipour and S. J. Koester, "Ambipolar Black Phosphorus MOSFETs With Record n-Channel Transconductance," *IEEE Electron Device Letters*, vol. 37, no. 1, pp. 103–106, 2016, ISSN: 0741-3106. DOI: 10.1109/LED.2015.2499209.

[33] V. Podzorov, M. E. Gershenson, C. Kloc, R. Zeis, and E. Bucher, "High-mobility field-effect transistors based on transition metal dichalcogenides," *Applied Physics Letters*, vol. 84, no. 17, pp. 3301–3303, 2004, ISSN: 0003-6951. DOI: 10.1063/1.1723695.

[34] K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, and A. K. Geim, "Two-dimensional atomic crystals," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 102, no. 30, pp. 10 451–10 453, 2005, ISSN: 00278424. DOI: 10.1073/pnas.0502848102.

[35] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically thin MoS_2: A new direct-gap semiconductor," *Physical Review Letters*, vol. 105, no. 13, p. 136 805, 2010, ISSN: 0031-9007. DOI: 10.1103/PhysRevLett.105.136805.

[36] H. Liu and P. D. Ye, "MoS_2 Dual-Gate MOSFET With Atomic-Layer-Deposited Al_2O_3 as Top-Gate Dielectric," *IEEE Electron Device Letters*, vol. 33, no. 4, pp. 546–548, 2012, ISSN: 0741-3106. DOI: 10.1109/LED.2012.2184520.

[37] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, and T. Palacios, "Integrated Circuits Based on Bilayer MoS_2 Transistors," *Nano Letters*, vol. 12, no. 9, pp. 4674–4680, 2012, ISSN: 1530-6984. DOI: 10.1021/nl302015v.

[38] H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, and P. D. Ye, "Phosphorene: An unexplored 2D semiconductor with a high hole mobility," *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, 2014, ISSN: 1936086X. DOI: 10.1021/nn501226z.

[39] Yang-Kyu Choi, K. Asano, N. Lindert, V. Subramanian, Tsu-Jae King, J. Bokor, and Chenming Hu, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron era," *IEEE Electron Device Letters*, vol. 21, no. 5, pp. 254–255, 2000, ISSN: 0741-3106. DOI: 10.1109/55.841313.

[40] J. Appenzeller, Y.-M. Lin, J. Knoch, Z. Chen, and P. Avouris, "Comparing Carbon Nanotube Transistors—The Ideal Choice: A Novel Tunneling Device Design," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2568–2576, 2005, ISSN: 0018-9383. DOI: 10.1109/TED.2005.859654.

[41] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and I_{on} = 10 μA/μm for I_{off} = 1 nA/μm at V_{ds} = 0.3 V," in *2016 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2016, pp. 19.1.1–19.1.4, ISBN: 978-1-5090-3902-9. DOI: 10.1109/IEDM.2016.7838450.

[42] T. Roy, M. Tosun, X. Cao, H. Fang, D.-H. Lien, P. Zhao, Y.-Z. Chen, Y.-L. Chueh, J. Guo, and A. Javey, "Dual-Gated MoS_2/WSe_2 van der Waals Tunnel Diodes and Transistors," *ACS Nano*, vol. 9, no. 2, pp. 2071–2079, 2015, ISSN: 1936-0851. DOI: 10.1021/nn507278b.

[43] T. A. Ameen, H. Ilatikhameneh, G. Klimeck, and R. Rahman, "Few-layer Phosphorene: An Ideal 2D Material For Tunnel Transistors," *Scientific Reports*, vol. 6, no. 1, p. 28 515, 2016, ISSN: 2045-2322. DOI: 10.1038/srep28515.

[44] H. Ilatikhameneh, T. Ameen, B. Novakovic, Y. Tan, G. Klimeck, and R. Rahman, "Saving Moore's Law Down To 1 nm Channels With Anisotropic Effective Mass," *Scientific Reports*, vol. 6, no. 1, p. 31 501, 2016, ISSN: 2045-2322. DOI: 10.1038/srep31501.

[45] S. Das, A. Prakash, R. Salazar, and J. Appenzeller, "Toward low-power electronics: Tunneling phenomena in transition metal dichalcogenides," *ACS Nano*, vol. 8, no. 2, pp. 1681–1689, 2014, ISSN: 1936-0851. DOI: 10.1021/nn406603h.

[46] H. Ilatikhameneh, Y. Tan, B. Novakovic, G. Klimeck, R. Rahman, and J. Appenzeller, "Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 1, pp. 12–18, 2015, ISSN: 2329-9231. DOI: 10.1109/JXCDC.2015.2423096.

[47] H. Ilatikhameneh, R. B. Salazar, G. Klimeck, R. Rahman, and J. Appenzeller, "From Fowler–Nordheim to Nonequilibrium Green's Function Modeling of Tunneling," *IEEE Transactions on Electron Devices*, vol. 63, no. 7, pp. 2871–2878, 2016, ISSN: 0018-9383. DOI: 10.1109/TED.2016.2565582.

[48] R. Yan, S. Fathipour, Y. Han, B. Song, S. Xiao, M. Li, N. Ma, V. Protasenko, D. A. Muller, D. Jena, and H. G. Xing, "Esaki Diodes in van der Waals Heterojunctions with Broken-Gap Energy Band Alignment," *Nano Letters*, vol. 15, no. 9, pp. 5791–5798, 2015, ISSN: 15306992. DOI: 10.1021/acs.nanolett.5b01792.

[49] T. Roy, M. Tosun, M. Hettick, G. H. Ahn, C. Hu, and A. Javey, "2D-2D tunneling field-effect transistors using $WSe_2/SnSe_2$ heterostructures," *Applied Physics Letters*, vol. 108, no. 8, p. 083 111, 2016, ISSN: 0003-6951. DOI: 10.1063/1.4942647.

[50] M. R. Müller, R. Salazar, S. Fathipour, H. Xu, K. Kallis, U. Künzelmann, A. Seabaugh, J. Appenzeller, and J. Knoch, "Gate-Controlled WSe_2 Transistors Using a Buried Triple-Gate Structure," *Nanoscale Research Letters*, vol. 11, no. 1, p. 512, 2016, ISSN: 1931-7573. DOI: 10.1186/s11671-016-1728-7.

[51] A. Seabaugh, S. Fathipour, W. Li, H. Lu, J. H. Park, A. C. Kummel, D. Jena, S. K. Fullerton-Shirey, and P. Fay, "Steep subthreshold swing tunnel FETs: GaN/InN/GaN and transition metal dichalcogenide channels," in *2015 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2015, pp. 35.6.1–35.6.4, ISBN: 978-1-4673-9894-7. DOI: 10.1109/IEDM.2015.7409835.

[52] A. Prakash and J. Appenzeller, "Bandgap Extraction and Device Analysis of Ionic Liquid Gated WSe_2 Schottky Barrier Transistors," *ACS Nano*, vol. 11, no. 2, pp. 1626–1632, 2017, ISSN: 1936-0851. DOI: 10.1021/acsnano.6b07360.

[53] X. Chen, Y. Wu, Z. Wu, Y. Han, S. Xu, L. Wang, W. Ye, T. Han, Y. He, Y. Cai, and N. Wang, "High-quality sandwiched black phosphorus heterostructure and its quantum oscillations," *Nature Communications*, vol. 6, p. 7315, 2015, ISSN: 20411723. DOI: 10.1038/ncomms8315.

[54] R. A. Doganov, E. C. T. O'Farrell, S. P. Koenig, Y. Yeo, A. Ziletti, A. Carvalho, D. K. Campbell, D. F. Coker, K. Watanabe, T. Taniguchi, A. H. C. Neto, and B. Özyilmaz, "Transport properties of pristine few-layer black phosphorus by van der Waals passivation in an inert atmosphere," *Nature Communications*, vol. 6, p. 6647, 2015, ISSN: 2041-1723. DOI: 10.1038/ncomms7647.

[55] G. Long, D. Maryenko, J. Shen, S. Xu, J. Hou, Z. Wu, W. K. Wong, T. Han, J. Lin, Y. Cai, R. Lortz, and N. Wang, "Achieving Ultrahigh Carrier Mobility in Two-Dimensional Hole Gas of Black Phosphorus," *Nano Letters*, vol. 16, no. 12, pp. 7768–7773, 2016, ISSN: 1530-6984. DOI: 10.1021/acs.nanolett.6b03951.

[56] Y. Cao, A. Mishchenko, G. L. Yu, E. Khestanova, A. P. Rooney, E. Prestat, A. V. Kretinin, P. Blake, M. B. Shalom, C. Woods, J. Chapman, G. Balakrishnan, I. V. Grigorieva, K. S. Novoselov, B. A. Piot, M. Potemski, K. Watanabe, T. Taniguchi, S. J. Haigh, A. K. Geim, and R. V. Gorbachev, "Quality Heterostructures from Two-Dimensional Crystals Unstable in Air by Their Assembly in Inert Atmosphere," *Nano Letters*, vol. 15, no. 8, pp. 4914–4921, 2015, ISSN: 1530-6984. DOI: 10.1021/acs.nanolett.5b00648.

[57] D. J. Perello, S. H. Chae, S. Song, and Y. H. Lee, "High-performance n-type black phosphorus transistors with type control via thickness and contact-metal engineering," *Nature Communications*, vol. 6, p. 7809, 2015, ISSN: 2041-1723. DOI: 10.1038/ncomms8809.

[58] J. Qiao, X. Kong, Z.-X. Hu, F. Yang, and W. Ji, "High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus," *Nature Communications*, vol. 5, p. 4475, 2014, ISSN: 2041-1723. DOI: 10.1038/ncomms5475.

[59] V. Tran, R. Soklaski, Y. Liang, and L. Yang, "Layer-controlled band gap and anisotropic excitons in few-layer black phosphorus," *Physical Review B*, vol. 89, no. 23, p. 235 319, 2014, ISSN: 1098-0121. DOI: 10.1103/PhysRevB.89.235319.

[60] P. Wu, A. Prakash, and J. Appenzeller, "First demonstration of band-to-band tunneling in black phosphorus," in *2017 75th Annual Device Research Conference (DRC)*, IEEE, 2017, pp. 1–2, ISBN: 978-1-5090-6328-4. DOI: 10.1109/DRC.2017.7999394.

[61] M. C. Robbins and S. J. Koester, "Crystal-oriented black phosphorus TFETs with strong band-to-band-tunneling anisotropy and subthreshold slope nearing the thermionic limit," in *2017 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2017, pp. 15.7.1–15.7.4, ISBN: 978-1-5386-3559-9. DOI: 10.1109/IEDM.2017.8268399.

[62] M. C. Robbins and S. J. Koester, "Black phosphorus p- and n-MOSFETs with electrostatically doped contacts," *IEEE Electron Device Letters*, vol. 38, no. 2, pp. 285–288, 2017, ISSN: 07413106. DOI: 10.1109/LED.2016.2638818.

[63] M. Buscema, D. J. Groenendijk, G. A. Steele, H. S. van der Zant, and A. Castellanos-Gomez, "Photovoltaic effect in few-layer black phosphorus PN junctions defined by local electrostatic gating," *Nature Communications*, vol. 5, p. 4651, 2014, ISSN: 2041-1723. DOI: 10.1038/ncomms5651.

[64] H. Ilatikhameneh, T. A. Ameen, G. Klimeck, J. Appenzeller, and R. Rahman, "Dielectric Engineered Tunnel Field-Effect Transistor," *IEEE Electron Device Letters*, vol. 36, no. 10, pp. 1097–1100, 2015, ISSN: 0741-3106. DOI: 10.1109/LED.2015.2474147.

[65] J. Knoch, W. Riess, and J. Appenzeller, "Outperforming the Conventional Scaling Rules in the Quantum-Capacitance Limit," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 372–374, 2008, ISSN: 0741-3106. DOI: 10.1109/LED.2008.917816.

[66] S. Steiger, M. Povolotskyi, H.-H. Park, T. Kubis, and G. Klimeck, "NEMO5: A Parallel Multiscale Nanoelectronics Modeling Tool," *IEEE Transactions on Nanotechnology*, vol. 10, no. 6, pp. 1464–1474, 2011, ISSN: 1536-125X. DOI: 10.1109/TNANO.2011.2166164.

[67] J. E. Fonseca, T. Kubis, M. Povolotskyi, B. Novakovic, A. Ajoy, G. Hegde, H. Ilatikhameneh, Z. Jiang, P. Sengupta, Y. Tan, and G. Klimeck, "Efficient and realistic device modeling from atomic detail to the nanoscale," *Journal of Computational Electronics*, vol. 12, no. 4, pp. 592–600, 2013, ISSN: 1569-8025. DOI: 10.1007/s10825-013-0509-0.

[68] J. D. Wood, S. A. Wells, D. Jariwala, K. S. Chen, E. Cho, V. K. Sangwan, X. Liu, L. J. Lauhon, T. J. Marks, and M. C. Hersam, "Surface chemistry of black phosphorus under a controlled oxidative environment," *Nanotechnology*, vol. 27, no. 43, p. 434 002, 2016, ISSN: 0957-4484. DOI: 10.1088/0957-4484/27/43/434002.

[69] J. D. Wood, S. A. Wells, D. Jariwala, K. S. Chen, E. Cho, V. K. Sangwan, X. Liu, L. J. Lauhon, T. J. Marks, and M. C. Hersam, "Effective Passivation of Exfoliated Black Phosphorus Transistors against Ambient Degradation," *Nano Letters*, vol. 14, no. 12, pp. 6964–6970, 2014, ISSN: 1530-6984. DOI: 10.1021/nl5032293.

[70] M. T. Edmonds, A. Tadich, A. Carvalho, A. Ziletti, K. M. O'Donnell, S. P. Koenig, D. F. Coker, B. Özyilmaz, A. H. C. Neto, and M. S. Fuhrer, "Creating a Stable Oxide at the Surface of Black Phosphorus," *ACS Applied Materials & Interfaces*, vol. 7, no. 27, pp. 14 557–14 562, 2015, ISSN: 1944-8244. DOI: 10.1021/acsami.5b01297.

[71] H. A. A. Sidek, I. T. Collier, R. N. Hampton, G. A. Saunders, and B. Bridge, "Electrical conductivity and dielectric constant of samarium phosphate glasses," *Philosophical Magazine B*, vol. 59, no. 2, pp. 221–232, 1989, ISSN: 1364-2812. DOI: 10.1080/13642818908220173.

[72] L. Lattanzio, L. De Michielis, and A. M. Ionescu, "The electron–hole bilayer tunnel FET," *Solid-State Electronics*, vol. 74, pp. 85–90, 2012, ISSN: 00381101. DOI: 10.1016/j.sse.2012.04.016.

[73] J. L. Padilla, C. Alper, F. Gámiz, and A. M. Ionescu, "Assessment of field-induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field-effect transistor," *Applied Physics Letters*, vol. 105, no. 8, p. 082 108, 2014, ISSN: 0003-6951. DOI: 10.1063/1.4894088.

[74] F. W. Chen, H. Ilatikhameneh, T. A. Ameen, G. Klimeck, and R. Rahman, "Thickness Engineered Tunnel Field-Effect Transistors Based on Phosphorene," *IEEE Electron Device Letters*, vol. 38, no. 1, pp. 130–133, 2017, ISSN: 0741-3106. DOI: 10.1109/LED.2016.2627538.

[75] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits (2nd Edition)," *Book*, 2003.

[76] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. I. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5 nm," in *Technical Digest - International Electron Devices Meeting*, 2002. DOI: 10.1109/iedm.2002.1175776.

[77] S. Reggiani, E. Gnani, A. Gnudi, M. Rudan, and G. Baccarani, "Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2204–2212, 2007, ISSN: 0018-9383. DOI: 10.1109/TED.2007.902899.

[78] Y. Du, H. Liu, Y. Deng, and P. D. Ye, "Device perspective for black phosphorus field-effect transistors: Contact resistance, ambipolar behavior, and scaling," *ACS Nano*, vol. 8, no. 10, pp. 10 035–10 042, 2014, ISSN: 1936086X. DOI: 10.1021/nn502553m.

[79] Y. Jung, M. S. Choi, A. Nipane, A. Borah, B. Kim, A. Zangiabadi, T. Taniguchi, K. Watanabe, W. J. Yoo, J. Hone, and J. T. Teherani, "Transferred via contacts as a platform for ideal two-dimensional transistors," *Nature Electronics*, vol. 2, no. 5, pp. 187–194, 2019, ISSN: 25201131. DOI: 10.1038/s41928-019-0245-y.

[80] D. Liu, X. Chen, Y. Yan, Z. Zhang, Z. Jin, K. Yi, C. Zhang, Y. Zheng, Y. Wang, J. Yang, X. Xu, J. Chen, Y. Lu, D. Wei, A. T. S. Wee, and D. Wei, "Conformal hexagonal-boron nitride dielectric interface for tungsten diselenide devices with improved mobility and thermal dissipation," *Nature Communications*, vol. 10, pp. 1–11, 2019, ISSN: 20411723. DOI: 10.1038/s41467-019-09016-0.

[81] Y. Liu, J. Guo, E. Zhu, L. Liao, S.-J. Lee, M. Ding, I. Shakir, V. Gambin, Y. Huang, and X. Duan, "Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions," *Nature*, vol. 557, no. 7707, pp. 696–700, 2018, ISSN: 0028-0836. DOI: 10.1038/s41586-018-0129-8.

[82] G. Long, D. Maryenko, J. Shen, S. Xu, J. Hou, Z. Wu, W. K. Wong, T. Han, J. Lin, Y. Cai, R. Lortz, and N. Wang, "Achieving ultrahigh carrier mobility in two-dimensional hole gas of black phosphorus," *Nano Letters*, vol. 16, no. 12, pp. 7768–7773, 2016, ISSN: 1530-6984. DOI: 10.1021/acs.nanolett.6b03951.

[83] J. Appenzeller, F. Zhang, S. Das, and J. Knoch, "Transition metal dichalcogenide schottky barrier transistors: A device analysis and material comparison," in *2D Materials for Nanoelectronics*, 2016, ISBN: 9781498704182. DOI: 10.1201/b19623-11.

[84] S. Heinze, J. Tersoff, and P. Avouris, "Electrostatic engineering of nanotube transistors for improved performance," *Applied Physics Letters*, vol. 83, no. 24, pp. 5038–5040, 2003, ISSN: 0003-6951. DOI: 10.1063/1.1632531.

[85] Y.-M. Lin, J. Appenzeller, and P. Avouris, "Ambipolar-to-unipolar conversion of carbon nanotube transistors by gate structure engineering," *Nano Letters*, vol. 4, no. 5, pp. 947–950, 2004, ISSN: 1530-6984. DOI: 10.1021/nl049745j.

[86] C. Qiu, Z. Zhang, D. Zhong, J. Si, Y. Yang, and L. M. Peng, "Carbon nanotube feedback-gate field-effect transistor: Suppressing current leakage and increasing on/off ratio," *ACS Nano*, vol. 9, no. 1, pp. 969–977, 2015, ISSN: 1936086X. DOI: 10.1021/nn506806b.

[87] P. Wu and J. Appenzeller, "High performance complementary black phosphorus FETs and inverter circuits operating at record-low V_{DD} down to 0.2V," in *Device Research Conference - Conference Digest, DRC*, 2018, ISBN: 9781538630280. DOI: 10.1109/DRC.2018.8442224.

[88] Y. Liu and K. W. Ang, "Monolithically integrated flexible black phosphorus complementary inverter circuits," *ACS Nano*, vol. 11, no. 7, pp. 7416–7423, 2017, ISSN: 1936086X. DOI: 10.1021/acsnano.7b03703.

[89] A. M. Cowley and S. M. Sze, "Surface states and barrier height of metal-semiconductor systems," *Journal of Applied Physics*, vol. 36, no. 10, pp. 3212–3220, 1965, ISSN: 00218979. DOI: 10.1063/1.1702952.

[90] P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, M. A. Quevedo-Lopez, H. C. Wen, H. Alshareef, K. Choi, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker, H. R. Harris, P. Majhi, R. Choi, P. Lysaght, B. H. Lee, H. H. Tseng, R. Jammy, T. S. Böscke, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, "Dipole model explaining high-k/metal gate field effect transistor threshold voltage tuning," *Applied Physics Letters*, vol. 92, no. 9, pp. 2–5, 2008, ISSN: 00036951. DOI: 10.1063/1.2890056.

[91] D. S. Schulman, A. J. Arnold, and S. Das, "Contact engineering for 2D materials and devices," *Chemical Society Reviews*, vol. 47, no. 9, pp. 3037–3058, 2018, ISSN: 0306-0012. DOI: 10.1039/C7CS00828G.

[92] A. Prakash, H. Ilatikhameneh, P. Wu, and J. Appenzeller, "Understanding contact gating in Schottky barrier transistors from 2D channels," *Scientific Reports*, vol. 7, no. 1, p. 12 596, 2017, ISSN: 2045-2322. DOI: 10.1038/s41598-017-12816-3. arXiv: 1707.01459.

[93] G. Moore, "Cramming More Components Onto Integrated Circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, 1998, ISSN: 0018-9219. DOI: 10.1109/JPROC.1998.658762.

[94] T. Skotnicki, J. Hutchby, T. King, H.-S. Wong, and F. Boeuf, "The end of CMOS scaling," *IEEE Circuits and Devices Magazine*, vol. 21, no. 1, pp. 16–26, 2005, ISSN: 8755-3996. DOI: 10.1109/MCD.2005.1388765.

[95] G. Servanton, L. Clement, K. Lepinay, F. Lorut, R. Pantel, A. Pofelski, and N. Bicais, "Advanced TEM Characterization for the Development of 28-14nm nodes based on fully-depleted Silicon-on-Insulator Technology," *Journal of Physics: Conference Series*, vol. 471, no. 1, p. 012 026, 2013, ISSN: 1742-6588. DOI: 10.1088/1742-6596/471/1/012026.

[96] M. Holler, M. Odstrcil, M. Guizar-Sicairos, M. Lebugle, E. Müller, S. Finizio, G. Tinti, C. David, J. Zusman, W. Unglaub, O. Bunk, J. Raabe, A. F. J. Levi, and G. Aeppli, "Three-dimensional imaging of integrated circuits with macro- to nanoscale zoom," *Nature Electronics*, vol. 2, no. 10, pp. 464–470, 2019, ISSN: 2520-1131. DOI: 10.1038/s41928-019-0309-z.

[97] M. Holler, M. Guizar-Sicairos, E. H. Tsai, R. Dinapoli, E. Müller, O. Bunk, J. Raabe, and G. Aeppli, "High-resolution non-destructive three-dimensional imaging of integrated circuits," *Nature*, vol. 543, no. 7645, pp. 402–406, 2017, ISSN: 14764687. DOI: 10.1038/nature21698.

[98] S. Nakaharai, M. Yamamoto, K. Ueno, Y. F. Lin, S. L. Li, and K. Tsukagoshi, "Electrostatically Reversible Polarity of Ambipolar α-$MoTe_2$ Transistors," *ACS Nano*, vol. 9, no. 6, pp. 5976–5983, 2015, ISSN: 1936086X. DOI: 10.1021/acsnano.5b00736.

[99] W. J. Yu, U. J. Kim, B. R. Kang, I. H. Lee, E. H. Lee, and Y. H. Lee, "Adaptive logic circuits with doping-free ambipolar carbon nanotube transistors," *Nano Letters*, vol. 9, no. 4, pp. 1401–1405, 2009, ISSN: 15306984. DOI: 10.1021/nl803066v.

[100] Y. F. Lin, Y. Xu, S. T. Wang, S. L. Li, M. Yamamoto, A. Aparecido-Ferreira, W. Li, H. Sun, S. Nakaharai, W. B. Jian, K. Ueno, and K. Tsukagoshi, "Ambipolar $MoTe_2$ transistors and their applications in logic circuits," *Advanced Materials*, vol. 26, no. 20, pp. 3263–3269, 2014, ISSN: 15214095. DOI: 10.1002/adma.201305845.

[101] G. V. Resta, Y. Balaji, D. Lin, I. P. Radu, F. Catthoor, P. E. Gaillardon, and G. De Micheli, "Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors," *ACS Nano*, vol. 12, no. 7, pp. 7039–7047, 2018, ISSN: 1936086X. DOI: 10.1021/acsnano.8b02739.

[102] J. Rajendran, R. Karri, J. B. Wendt, M. Potkonjak, N. Mcdonald, G. S. Rose, and B. Wysocki, "Nano meets security: Exploring nanoelectronic devices for security applications," *Proceedings of the IEEE*, vol. 103, no. 5, pp. 829–849, 2015, ISSN: 00189219. DOI: 10.1109/JPROC.2014.2387353.

[103] S. Patnaik, N. Rangarajan, J. Knechtel, O. Sinanoglu, and S. Rakheja, "Advancing hardware security using polymorphic and stochastic spin-hall effect devices," in *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, IEEE, 2018, pp. 97–102, ISBN: 978-3-9819263-0-9. DOI: 10.23919/DATE.2018.8341986. eprint: 1806.00790.

[104] Y. Bi, K. Shamsi, J.-S. Yuan, P.-E. Gaillardon, G. D. Micheli, X. Yin, X. S. Hu, M. Niemier, and Y. Jin, "Emerging Technology-Based Design of Primitives for Hardware Security," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 13, no. 1, pp. 1–19, 2016, ISSN: 1550-4832. DOI: 10.1145/2816818.

[105] S. Dupuis and M.-L. Flottes, "Logic Locking: A Survey of Proposed Methods and Evaluation Metrics," *Journal of Electronic Testing*, vol. 35, no. 3, pp. 273–291, 2019, ISSN: 0923-8174. DOI: 10.1007/s10836-019-05800-4.

[106] J. A. Roy, F. Koushanfar, and I. L. Markov, "EPIC: Ending Piracy of Integrated Circuits," in *2008 Design, Automation and Test in Europe*, IEEE, 2008, pp. 1069–1074, ISBN: 978-3-9810801-3-1. DOI: 10.1109/DATE.2008.4484823.

[107] S. M. Plaza and I. L. Markov, "Solving the Third-Shift Problem in IC Piracy With Test-Aware Logic Locking," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 6, pp. 961–971, 2015, ISSN: 0278-0070. DOI: 10.1109/TCAD.2015.2404876.

[108] J. Rajendran, O. Sinanoglu, and R. Karri, "VLSI testing based security metric for IC camouflaging," in *2013 IEEE International Test Conference (ITC)*, IEEE, 2013, pp. 1–4, ISBN: 978-1-4799-0859-2. DOI: 10.1109/TEST.2013.6651879.

[109] J. Rajendran, M. Sam, O. Sinanoglu, and R. Karri, "Security analysis of integrated circuit camouflaging," in *Proceedings of the 2013 ACM SIGSAC conference on Computer & communications security - CCS '13*, New York, New York, USA: ACM Press, 2013, pp. 709–720, ISBN: 9781450324779. DOI: 10.1145/2508859.2516656. [Online]. Available: http://dl.acm.org/citation.cfm?doid=2508859.2516656.

[110] M. Shiozaki, R. Hori, and T. Fujino, "Diffusion Programmable Device: The device to prevent reverse engineering.," *IACR Cryptology ePrint Archive*, 2014.

[111] S. Malik, G. T. Becker, C. Paar, and W. P. Burleson, "Development of a Layout-Level Hardware Obfuscation Tool," in *2015 IEEE Computer Society Annual Symposium on VLSI*, IEEE, 2015, pp. 204–209, ISBN: 978-1-4799-8719-1. DOI: 10.1109/ISVLSI.2015.118.

[112] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable silicon nanowire transistors," *Nano Letters*, vol. 12, no. 1, pp. 119–124, 2012, ISSN: 15306984. DOI: 10.1021/nl203094h.

[113] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, and W. M. Weber, "Dually active silicon nanowire transistors and circuits with equal electron and hole transport," *Nano Letters*, vol. 13, no. 9, pp. 4176–4181, 2013, ISSN: 15306984. DOI: 10.1021/nl401826u.

[114] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P. E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," *Technical Digest - International Electron Devices Meeting, IEDM*, pp. 8.4.1–8.4.4, 2012, ISSN: 01631918. DOI: 10.1109/IEDM.2012.6479004.

[115] S. Larentis, B. Fallahazad, H. C. Movva, K. Kim, A. Rai, T. Taniguchi, K. Watanabe, S. K. Banerjee, and E. Tutuc, "Reconfigurable Complementary Monolayer $MoTe_2$ Field-Effect Transistors for Integrated Circuits," *ACS Nano*, vol. 11, no. 5, pp. 4832–4839, 2017, ISSN: 1936086X. DOI: 10.1021/acsnano.7b01306.

[116] R. Bao, K. Watanabe, J. Zhang, J. Guo, H. Zhou, P. Jamison, M. Wang, N. Loubet, V. Ba, M. Sankarapandian, J. Li, A. R. Hubbard, D. Dechene, D. Guo, B. Haran, H. Bu, and M. Khare, "Multiple-V_t Solutions in Nanosheet Technology for High Performance and Low Power Applications," *2019 IEEE International Electron Devices Meeting (IEDM)*, pp. 234–237, 2019.

[117] Y. Cai, G. Zhang, and Y.-W. Zhang, "Layer-dependent Band Alignment and Work Function of Few-Layer Phosphorene," *Scientific Reports*, vol. 4, no. 1, p. 6677, 2015, ISSN: 2045-2322. DOI: 10.1038/srep06677.

[118] N. Haratipour, S. Namgung, S.-H. Oh, and S. J. Koester, "Fundamental Limits on the Subthreshold Slope in Schottky Source/Drain Black Phosphorus Field-Effect Transistors," *ACS Nano*, vol. 10, no. 3, pp. 3791–3800, 2016, ISSN: 1936-0851. DOI: 10.1021/acsnano.6b00482.

[119] N. Haratipour, S. Namgung, R. Grassi, T. Low, S.-H. Oh, and S. J. Koester, "High-Performance Black Phosphorus MOSFETs Using Crystal Orientation Control and Contact Engineering," *IEEE Electron Device Letters*, vol. 38, no. 5, pp. 685–688, 2017, ISSN: 0741-3106. DOI: 10.1109/LED.2017.2679117. [Online]. Available: http://ieeexplore.ieee.org/document/7873224/.

[120] S. Das, M. Demarteau, and A. Roelofs, "Ambipolar Phosphorene Field Effect Transistor," *ACS Nano*, vol. 8, no. 11, pp. 11 730–11 738, 2014, ISSN: 1936-0851. DOI: 10.1021/nn505868h.

[121] P. Kocher, J. Jaffe, and B. Jun, "Differential Power Analysis," in *Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics)*, 1999, pp. 388–397, ISBN: 3540663479.

[122] C. Li, Y. Wu, B. Deng, Y. Xie, Q. Guo, S. Yuan, X. Chen, M. Bhuiyan, Z. Wu, K. Watanabe, T. Taniguchi, H. Wang, J. J. Cha, M. Snure, Y. Fei, and F. Xia, "Synthesis of Crystalline Black Phosphorus Thin Film on Sapphire," *Advanced Materials*, vol. 30, no. 6, p. 1 703 748, 2018, ISSN: 09359648. DOI: 10.1002/adma.201703748.

[123] Y. Xu, X. Shi, Y. Zhang, H. Zhang, Q. Zhang, Z. Huang, X. Xu, J. Guo, H. Zhang, L. Sun, Z. Zeng, A. Pan, and K. Zhang, "Epitaxial nucleation and lateral growth of high-crystalline black phosphorus films on silicon," *Nature Communications*, vol. 11, p. 1330, 2020, ISSN: 2041-1723. DOI: 10.1038/s41467-020-14902-z.

[124] C. Zhao, C. Tan, D.-H. Lien, X. Song, M. Amani, M. Hettick, H. Y. Y. Nyein, Z. Yuan, L. Li, M. C. Scott, and A. Javey, "Evaporated tellurium thin films for p-type field-effect transistors and circuits," *Nature Nanotechnology*, vol. 15, no. 1, pp. 53–58, 2020, ISSN: 1748-3387. DOI: 10.1038/s41565-019-0585-9.

[125] Y. Wang, G. Qiu, R. Wang, S. Huang, Q. Wang, Y. Liu, Y. Du, W. A. Goddard, M. J. Kim, X. Xu, P. D. Ye, and W. Wu, "Field-effect transistors made from solution-grown two-dimensional tellurene," *Nature Electronics*, vol. 1, no. 4, pp. 228–236, 2018, ISSN: 2520-1131. DOI: 10.1038/s41928-018-0058-4.

[126] H. Liu, A. T. Neal, M. Si, Y. Du, and P. D. Ye, "The Effect of Dielectric Capping on Few-Layer Phosphorene Transistors: Tuning the Schottky Barrier Heights," *IEEE Electron Device Letters*, vol. 35, no. 7, pp. 795–797, 2014, ISSN: 0741-3106. DOI: 10.1109/LED.2014.2323951.

[127] C. J. McClellan, E. Yalon, K. K. H. Smithe, S. V. Suryavanshi, and E. Pop, "Effective n-type doping of monolayer MoS_2 by AlO_x," in *2017 75th Annual Device Research Conference (DRC)*, IEEE, 2017, pp. 1–2, ISBN: 978-1-5090-6328-4. DOI: 10.1109/DRC.2017.7999392.

[128] C. Lau, T. Srimani, M. D. Bishop, G. Hills, and M. M. Shulaker, "Tunable n-Type Doping of Carbon Nanotubes through Engineered Atomic Layer Deposition HfO_x Films," *ACS Nano*, vol. 12, no. 11, pp. 10 924–10 931, 2018, ISSN: 1936-0851. DOI: 10.1021/acsnano.8b04208.

[129] J. Zhang, C. Wang, Y. Fu, Y. Che, and C. Zhou, "Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from p-Type to n-Type Using Atomic Layer Deposition of High-κ Oxide and Its Application in CMOS Logic Circuits," *ACS Nano*, vol. 5, no. 4, pp. 3284–3292, 2011, ISSN: 1936-0851. DOI: 10.1021/nn2004298.

[130] G. Qiu, M. Si, Y. Wang, X. Lyu, W. Wu, and P. D. Ye, "High-Performance Few-Layer Tellurium CMOS Devices Enabled by Atomic Layer Deposited Dielectric Doping Technique," in *2018 76th Device Research Conference (DRC)*, IEEE, 2018, pp. 1–2, ISBN: 978-1-5386-3027-3. DOI: 10.1109/DRC.2018.8442253.

[131] A. Alharbi and D. Shahrjerdi, "Analyzing the Effect of High-k Dielectric-Mediated Doping on Contact Resistance in Top-Gated Monolayer MoS 2 Transistors," *IEEE Transactions on Electron Devices*, vol. 65, no. 10, pp. 4084–4092, 2018, ISSN: 0018-9383. DOI: 10.1109/TED.2018.2866772.

[132] M. C. Robbins, N. Haratipour, and S. J. Koester, "Band-to-band tunneling limited ambipolar current in black phosphorus MOSFETs," in *2017 75th Annual Device Research Conference (DRC)*, IEEE, 2017, pp. 1–2, ISBN: 978-1-5090-6328-4. DOI: 10.1109/DRC.2017.7999417.

[133] S. Salahuddin and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices," *Nano Letters*, vol. 8, no. 2, pp. 405–410, 2008, ISSN: 1530-6984. DOI: 10.1021/nl071804g.

[134] M. Kobayashi, "A perspective on steep-subthreshold-slope negative-capacitance field-effect transistor," *Applied Physics Express*, vol. 11, no. 11, p. 110 101, 2018, ISSN: 1882-0778. DOI: 10.7567/APEX.11.110101.

[135] "Rethinking negative capacitance research," *Nature Electronics*, vol. 3, no. 9, pp. 503–503, 2020, ISSN: 2520-1131. DOI: 10.1038/s41928-020-00483-8.

[136] M. Hoffmann, S. Slesazeck, U. Schroeder, and T. Mikolajick, "What's next for negative capacitance electronics?" *Nature Electronics*, vol. 3, no. 9, pp. 504–506, 2020, ISSN: 2520-1131. DOI: 10.1038/s41928-020-00474-9.

[137] A. Rusu, G. A. Salvatore, D. Jimenez, and A. M. Ionescu, "Metal-Ferroelectric-Metal-Oxide-Semiconductor Field Effect Transistor with Sub-60mV/decade Subthreshold Swing and Internal Voltage Amplification," in *2010 International Electron Devices Meeting*, IEEE, 2010, pp. 16.3.1–16.3.4, ISBN: 978-1-4424-7418-5. DOI: 10.1109/IEDM.2010.5703374.

[138] F. A. McGuire, Y.-C. Lin, K. Price, G. B. Rayner, S. Khandelwal, S. Salahuddin, and A. D. Franklin, "Sustained Sub-60 mV/decade Switching via the Negative Capacitance Effect in MoS_2 Transistors," *Nano Letters*, vol. 17, no. 8, pp. 4801–4806, 2017, ISSN: 1530-6984. DOI: 10.1021/acs.nanolett.7b01584.

[139] M. Si, C. Jiang, C.-J. Su, Y.-T. Tang, L. Yang, W. Chung, M. A. Alam, and P. D. Ye, "Sub-60 mV/dec ferroelectric HZO MoS_2 negative capacitance field-effect transistor with internal metal gate: The role of parasitic capacitance," in *2017 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2017, pp. 23.5.1–23.5.4, ISBN: 978-1-5386-3559-9. DOI: 10.1109/IEDM.2017.8268447.

[140] M. Si, C. Jiang, W. Chung, Y. Du, M. A. Alam, and P. D. Ye, "Steep-Slope WSe_2 Negative Capacitance Field-Effect Transistor," *Nano Letters*, vol. 18, no. 6, pp. 3682–3687, 2018, ISSN: 1530-6984. DOI: 10.1021/acs.nanolett.8b00816.

[141] A. Saeidi, A. S. Verhulst, I. Stolichnov, A. Alian, H. Iwai, N. Collaert, and A. M. Ionescu, "Near Hysteresis-Free Negative Capacitance InGaAs Tunnel FETs with Enhanced Digital and Analog Figures of Merit below $V_{DD} = 400$mV," in *2018 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2018, pp. 13.4.1–13.4.4, ISBN: 978-1-7281-1987-8. DOI: 10.1109/IEDM.2018.8614583.

[142] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J. Liu, J. Shi, H. J. Kim, R. Sporer, C. Serrao, A. Busquet, P. Polakowski, J. Muller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, "14nm Ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *2017 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2017, pp. 15.1.1–15.1.4, ISBN: 978-1-5386-3559-9. DOI: 10.1109/IEDM.2017.8268393.

[143] W. Cao and K. Banerjee, "Is negative capacitance FET a steep-slope logic switch?" *Nature Communications*, vol. 11, p. 196, 2020, ISSN: 2041-1723. DOI: 10.1038/s41467-019-13797-9.

[144] Z. Liu, M. A. Bhuiyan, and T. P. Ma, "A Critical Examination of 'Quasi-Static Negative Capacitance' (QSNC) theory," in *2018 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2018, pp. 31.2.1–31.2.4, ISBN: 978-1-7281-1987-8. DOI: 10.1109/IEDM.2018.8614614.

[145] J. A. Kittl, B. Obradovic, D. Reddy, T. Rakshit, R. M. Hatcher, and M. S. Rodder, "On the validity and applicability of models of negative capacitance and implications for MOS applications," *Applied Physics Letters*, vol. 113, no. 4, p. 042 904, 2018, ISSN: 0003-6951. DOI: 10.1063/1.5036984. arXiv: 1805.01145.

[146] X. Li and A. Toriumi, "Direct relationship between sub-60 mV/dec subthreshold swing and internal potential instability in MOSFET externally connected to ferroelectric capacitor," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2019, ISBN: 9781728119878. DOI: 10.1109/IEDM.2018.8614703.

[147] X. Li and A. Toriumi, "Stepwise internal potential jumps caused by multiple-domain polarization flips in metal/ferroelectric/metal/paraelectric/metal stack," *Nature Communications*, vol. 11, p. 1895, 2020, ISSN: 2041-1723. DOI: 10.1038/s41467-020-15753-4.

[148] Q. Han, P. Aleksa, T. C. U. Tromm, J. Schubert, S. Mantl, and Q.-T. Zhao, "Transient negative capacitance and charge trapping in FDSOI MOSFETs with ferroelectric $HfYO_X$," *Solid-State Electronics*, vol. 159, pp. 71–76, 2019, ISSN: 00381101. DOI: 10.1016/j.sse.2019.03.037.

[149] S.-C. Chang, U. E. Avci, D. E. Nikonov, S. Manipatruni, and I. A. Young, "Physical Origin of Transient Negative Capacitance in a Ferroelectric Capacitor," *Physical Review Applied*, vol. 9, no. 1, p. 014 010, 2018, ISSN: 2331-7019. DOI: 10.1103/PhysRevApplied.9.014010. arXiv: 1709.03255.

[150] A. K. Saha, S. Datta, and S. K. Gupta, "NEGATIVE CAPACITANCE IN RESISTOR-FERROELECTRIC AND FERROELECTRIC-DIELECTRIC NETWORKS: APPARENT OR INTRINSIC?" *Journal of Applied Physics*, vol. 123, no. 10, p. 105 102, 2018, ISSN: 0021-8979. DOI: 10.1063/1.5016152.

[151] H. Wang, M. Yang, Q. Huang, K. Zhu, Y. Zhao, Z. Liang, C. Chen, Z. Wang, Y. Zhong, X. Zhang, and R. Huang, "New Insights into the Physical Origin of Negative Capacitance and Hysteresis in NCFETs," in *2018 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2018, pp. 31.1.1–31.1.4, ISBN: 978-1-7281-1987-8. DOI: 10.1109/IEDM.2018.8614504.

[152] C. Jin, T. Saraya, T. Hiramoto, and M. Kobayashi, "Transient Negative Capacitance as Cause of Reverse Drain-induced Barrier Lowering and Negative Differential Resistance in Ferroelectric FETs," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2019, ISBN: 9784863487178. DOI: 10.23919/VLSIT.2019.8776583.

[153] C. Jin, K. Jang, T. Saraya, T. Hiramoto, and M. Kobayashi, "Experimental Study on the Role of Polarization Switching in Subthreshold Characteristics of HfO_2-based Ferroelectric and Anti-ferroelectric FET," in *2018 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2018, pp. 31.5.1–31.5.4, ISBN: 978-1-7281-1987-8. DOI: 10.1109/IEDM.2018.8614486.

[154] B. Obradovic, T. Rakshit, R. Hatcher, J. A. Kittl, and M. S. Rodder, "Modeling Transient Negative Capacitance in Steep-Slope FeFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 5157–5164, 2018, ISSN: 0018-9383. DOI: 10.1109/TED.2018.2868479. arXiv: 1809.02053.

[155] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, "Negative capacitance in a ferroelectric capacitor," *Nature Materials*, vol. 14, no. 2, pp. 182–186, 2015, ISSN: 1476-1122. DOI: 10.1038/nmat4148.

[156] M. Hoffmann, F. P. G. Fengler, M. Herzig, T. Mittmann, B. Max, U. Schroeder, R. Negrea, P. Lucian, S. Slesazeck, and T. Mikolajick, "Unveiling the double-well energy landscape in a ferroelectric layer," *Nature*, vol. 565, no. 7740, pp. 464–467, 2019, ISSN: 0028-0836. DOI: 10.1038/s41586-018-0854-z.

[157] Y. J. Kim, H. W. Park, S. D. Hyun, H. J. Kim, K. D. Kim, Y. H. Lee, T. Moon, Y. B. Lee, M. H. Park, and C. S. Hwang, "Voltage Drop in a Ferroelectric Single Layer Capacitor by Retarded Domain Nucleation," *Nano Letters*, vol. 17, no. 12, pp. 7796–7802, 2017, ISSN: 1530-6984. DOI: 10.1021/acs.nanolett.7b04008.

[158] S. J. Song, Y. J. Kim, M. H. Park, Y. H. Lee, H. J. Kim, T. Moon, K. Do Kim, J.-H. Choi, Z. Chen, A. Jiang, and C. S. Hwang, "Alternative interpretations for decreasing voltage with increasing charge in ferroelectric capacitors," *Scientific Reports*, vol. 6, no. 1, p. 20 825, 2016, ISSN: 2045-2322. DOI: 10.1038/srep20825.

[159] A. I. Khan, U. Radhakrishna, K. Chatterjee, S. Salahuddin, and D. A. Antoniadis, "Negative Capacitance Behavior in a Leaky Ferroelectric," *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4416–4422, 2016, ISSN: 0018-9383. DOI: 10.1109/TED.2016.2612656.

[160] A. I. Khan, U. Radhakrishna, S. Salahuddin, and D. Antoniadis, "Work Function Engineering for Performance Improvement in Leaky Negative Capacitance FETs," *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1335–1338, 2017, ISSN: 0741-3106. DOI: 10.1109/LED.2017.2733382.

[161] J. F. Scott, "Ferroelectrics go bananas," *Journal of Physics: Condensed Matter*, vol. 20, no. 2, p. 021 001, 2008, ISSN: 0953-8984. DOI: 10.1088/0953-8984/20/02/021001.

[162] C.-S. Pang, P. Wu, J. Appenzeller, and Z. Chen, "Sub-1nm EOT WS_2-FET with $I_{DS} > 600\mu A/\mu m$ at $V_{DS} = 1V$ and SS $< 70mV/dec$ at $L_G = 40$ nm," in *2020 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2020, pp. 3.4.1–3.4.4, ISBN: 978-1-7281-8888-1. DOI: 10.1109/IEDM13553.2020.9372049.

[163] Agilent Technologies, *Agilent 4155C/4156C Semiconductor Parameter Analyzer, User's Guide Vol. 2, Measurement & Analysis*. 2003.

[164] D. L. John, L. C. Castro, and D. L. Pulfrey, "Quantum capacitance in nanoscale device modeling," *Journal of Applied Physics*, vol. 96, no. 9, pp. 5180–5184, 2004, ISSN: 0021-8979. DOI: 10.1063/1.1803614.

[165] N. Ma and D. Jena, "Carrier statistics and quantum capacitance effects on mobility extraction in two-dimensional crystal semiconductor field-effect transistors," *2D Materials*, vol. 2, no. 1, p. 015 003, 2015, ISSN: 2053-1583. DOI: 10.1088/2053-1583/2/1/015003.

[166] C.-C. Lu, Y.-C. Lin, C.-H. Yeh, J.-C. Huang, and P.-W. Chiu, "High Mobility Flexible Graphene Field-Effect Transistors with Self-Healing Gate Dielectrics," *ACS Nano*, vol. 6, no. 5, pp. 4469–4474, 2012, ISSN: 1936-0851. DOI: 10.1021/nn301199j.

[167] C.-H. Yeh, Y.-W. Lain, Y.-C. Chiu, C.-H. Liao, D. R. Moyano, S. S. H. Hsu, and P.-W. Chiu, "Gigahertz Flexible Graphene Transistors for Microwave Integrated Circuits," *ACS Nano*, vol. 8, no. 8, pp. 7663–7670, 2014, ISSN: 1936-0851. DOI: 10.1021/nn5036087.

[168] C. D. English, K. K. H. Smithe, R. L. Xu, and E. Pop, "Approaching ballistic transport in monolayer MoS_2 transistors with self-aligned 10 nm top gates," in *2016 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2016, pp. 5.6.1–5.6.4, ISBN: 978-1-5090-3902-9. DOI: 10.1109/IEDM.2016.7838355.

[169] E. Guerriero, P. Pedrinazzi, A. Mansouri, O. Habibpour, M. Winters, N. Rorsman, A. Behnam, E. A. Carrion, A. Pesquera, A. Centeno, A. Zurutuza, E. Pop, H. Zirath, and R. Sordan, "High-Gain Graphene Transistors with a Thin AlO_x Top-Gate Oxide," *Scientific Reports*, vol. 7, no. 1, p. 2419, 2017, ISSN: 2045-2322. DOI: 10.1038/s41598-017-02541-2.

VITA

Peng Wu was born in Cangzhou, Hebei, China in 1993. He received his bachelor's degree of Microelectronics from Tsinghua University in 2015. His undergraduate research focused on simulation and modeling of tunneling FETs, under the guidance of Prof. Zhiping Yu and Prof. Jinyu Zhang. He continued to pursue his PhD degree in Electrical and Computer Engineering at Purdue University in 2015, under the supervision of Prof. Joerg Appenzeller. During his PhD study, he investigated nano-transistors based on two-dimensional materials, including black phosphorus and transition metal dichalcogenides, for low-power steep-slope transistors and reconfigurable transistor applications.

PUBLICATIONS

Journal papers

[1] **Peng Wu**, Joerg Appenzeller, "Artifcial Sub-60 Millivolts/Decade Switching in a Metal-Insulator-Metal-Insulator-Semiconductor Transistor Without a Ferroelectric Component," *ACS Nano* **15**, 5158–5164 (2021).

[2] **Peng Wu**, Dayane Reis, Xiaobo Sharon Hu, Joerg Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics* **4**, 45-53 (2021).

[3] **Peng Wu**, Joerg Appenzeller, "Toward CMOS like devices from two-dimensional channel materials," *APL Materials* **7**, 100701 (2019). *(Editor's Pick)*

[4] **Peng Wu**, Joerg Appenzeller, "Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor With Record High ON-Currents," *IEEE Electron Device Letters* **40**, 981-984 (2019).

[5] **Peng Wu**, Tarek Ameen, Huairuo Zhang, Leonid A. Bendersky, Hesameddin Ilatikhameneh, Gerhard Klimeck, Rajib Rahman, Albert V. Davydov, Joerg Appenzeller, "Complementary Black Phosphorus Tunneling Field-Effect Transistors," *ACS Nano* **13**, 377-385 (2018).

[6] Chin-Sheng Pang, **Peng Wu**, Joerg Appenzeller, Zhihong Chen, "Thickness-Dependent Study of High-Performance WS_2-FETs With Ultrascaled Channel Lengths", *IEEE Transactions on Electron Devices* **68** (4), 2123-2129 (2021).

[7] Chin-Cheng Chiang, Vaibhav Ostwal, **Peng Wu**, Chin-Sheng Pang, Feng Zhang, Zhihong Chen, Joerg Appenzeller, "Memory Applications from 2D Materials,"*Applied Physics Reviews* **8**, 021306 (2021).

[8] Bernhard Stampfer, Feng Zhang, Yury Yuryevich Illarionov, Theresia Knobloch, **Peng Wu**, Michael Waltl, Alexander Grill, Joerg Appenzeller, Tibor Grasser, "Characterization of Single Defects in Ultrascaled MoS_2 Field-Effect Transistors," *ACS Nano* **12**, 5368-5375 (2018).

[9] Abhijith Prakash, Hesameddin Ilatikhameneh, **Peng Wu**, Joerg Appenzeller, "Understanding contact gating in Schottky barrier transistors from 2D channels," *Scientific Reports* **7**, 12596 (2017).

Conference papers

[1] Chin-Sheng Pang, **Peng Wu**, Joerg Appenzeller, Zhihong Chen, "Sub-1nm EOT WS_2-FET with $I_{DS} > 600$ μA/μm at $V_{DS} = 1$V and SS < 70mV/dec at $L_G = 40$nm," *66th IEEE International Electron Devices Meeting (IEDM)*, 2020.

[2] **Peng Wu**, Ruiping Zhou, Chin-Sheng Pang, Xiangkai Liu, Zhihong Chen, Joerg Appenzeller, "Contact Resistance Model for WSe_2 Schottky-Barrier FET," *78th Device Research Conference (DRC)*, 2020.

[3] **Peng Wu**, Joerg Appenzeller, "High Performance Complementary Black Phosphorus FETs and Inverter Circuits Operating at Record-Low V_{DD} down to 0.2V," *76th Device Research Conference (DRC)*, 2018.

[4] **Peng Wu**, Abhijith Prakash, Joerg Appenzeller, "First demonstration of band-to-band tunneling in black phosphorus," *75th Device Research Conference (DRC)*, 2017.