ELECTRO-THERMAL AND RADIATION RELIABILITY OF POWER TRANSISTORS: SILICON TO WIDE BANDGAP SEMICONDUCTORS

by

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This thesis is dedicated to the loving memory of my father, Nirmal Mahajan

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ABSTRACT

We are in the midst of a technological revolution (popularly known as *Industrie 4.0* or 4^{th} Industrial Revolution) where our cars are being equipped with hundreds of sensors that make them safer, homes are becoming smarter, industry yields are at an all-time high, and internet-of-things is a reality. This was largely possible due to the developments in communication, electronics, motor controls, robotics, cyber security, software, efficient power distribution, etc. One of the major propellants of the 4^{th} Industrial revolution is the ever-expanding applications of power electronics devices. All electrical energy will be provided, handled, and consumed through power electronics devices in the near future. Therefore, the reliability of power electronics devices will be instrumental in driving future technological advances.

A myriad of devices is categorized as power electronics devices, and in the heart of those devices are the transistors. Although Silicon-based transistors still dominate the power electronics market, a paradigm shift towards wide bandgap semiconductors, such as silicon carbide (SiC), gallium nitride (GaN), gallium oxide (β-Ga_2O_3),etc., is underway. However, realizing the full potential of these devices demands unconventional design, layout, and reliability.

In this thesis, we try to establish a generalized model of reliability for power and logic transistors. We start by defining a comprehensive, substrate-, self-heating-, and reliability-aware safe operating area (SOA) that analytically establishes the optimum and self-consistent trade-off among breakdown voltage, power consumption, operating frequency, heat dissipation, and reliability before actual device fabrication. Then we take a deeper look into the reliability of individual transistors (a β-Ga_2O_3 transistor and a Silicon-based LDMOS), to test the predictions by the safe operating area, using both experiments and simulations. In the β-Ga_2O_3 transistor, we studied its implementation in a DC-DC voltage converter and concluded that the self-heating is a performance bottleneck and suggested approaches to alleviate it. For the LDMOS transistor, we investigated the hot carrier degradation (HCD) using experiments and simulations. We established that the HCD degradation kinetics is universal, and physics is the same as a classical transistor, despite a complicated geometry.

Finally, we studied the correlation between HCD and radiation in LDMOS used in space shuttles, airplanes, etc., to determine its lifetime.

We have holistically analyzed the reliability of power transistors by extending the theories of logic transistors in this thesis. Therefore, this thesis takes us a step closer to a generalized reliability model for power transistors by developing a comprehensive and predictive model for the safe operating area, encompassing all sources of stresses (e.g., electrical, thermal, and radiation) it experiences during operation.

1. INTRODUCTION

1.1 Background

The 4th industrial revolution refers to the digitization of manufacturing and production processes in factories using robots, smart machinery, internet-of-things, and artificial intelligence to maximize the yield. This is built upon the 3rd industrial revolution, which started with the advent of transistors in the 1950s and transformed the electronics industry. Although conceptualized a few decades earlier, the first working transistor was invented by John Bardeen, Walter Brattain, and William Shockley at Bell Labs in 1947. However, the most widely used transistor, the MOSFET, was demonstrated in 1959 by Mohamed Atalla (a Purdue University alumni) and Dawon Kahng [1]. Since then, MOSFET has been the ubiquitous building block for modern electronics. The evolution of transistors, however, followed two contrasting different routes over the last few decades: (a) Low power transistors or 'Logic' transistors: scaling down the dimensions to accommodate more transistors in a single chip to enhance speed, power, and functionality; (b) High power transistors or simply 'Power' transistors: increasing the capacity of the transistors to handle high power. Although high and low power transistors are used together in an electronic device, the applied biases and operating regimes are incongruous. Consequently, the reliability mechanisms and concerns of logic and power transistors are not the same.

Hot carrier degradation (HCD) and radiation-induced degradation are among the common reliability issues in both logic and power transistors. The focus of this thesis to develop a generalized reliability model which can describe the reliability phenomena (HCD and radiation-induced degradation) in both logic and power transistors. HCD is the phenomenon where energetic electrons traveling from the source to the drain gain enough energy ($>$ 1.5 eV) to break the passivated Si-H and Si-O bonds in the Silicon/oxide interface. Since the drain bias of power transistors is high, HCD is a prominent reliability concern. Historically, radiation-induced defects were a concern for electronics used in high radiation environments (e.g., military and space applications). However, with the heralding of projects like Google Loon, Amazon Prime Air (Drone Delivery), etc., and increasing sensitivity of the chips due to bit flips and single event effects, studies of the impact of radiation on power transistor

lifetime are becoming increasingly important. It is of immense interest to study the impact of radiation on the traditional reliability mechanisms as well. In the end, all these degradation mechanism (i.e. HCD, radiation-induced degradation) collectively determine the safe operating area (SOA) of a transistor.

This introductory chapter[1] will discuss the trends of logic and power transistor scaling, basic principles and types of power transistors, the sources, and the effects of HCD and reliability-induced degradations. The current status and an in-depth analysis of these reliability mechanisms will be discussed in the subsequent chapters.

1.2 Logic Transistor Scaling

Nowadays, the computational speed of personal electronics devices is in the gigahertz range and the storage capacity in the terabytes range. This has been possible due to aggressive scaling of the transistors, such that currently, a single chip comprises more than a billion transistors. Historically, transistor count in a chip has increased exponentially, keeping pace with the Moore's law [5]. To pack more and more transistors in a single chip, the dimensions are scaled down such that the power density remains constant, and proportional to the area while scaling both the voltage and current. This law is popularly known as the Dennard scaling law [6]. The chip manufacturers followed Dennard's scaling law until the 1990's by scaling the doping densities, voltages, dielectric thickness, while scaling down the other device dimensions. By the mid-1990s, the power dissipation started to increase as chip manufacturers ran out of options to further scale the parameters (such as the dielectric). This led to innovations like high-k/metal gate architectures to keep up the increasing demand of computational speed. While this led to a solution, for a few generations of transistors, the power dissipation was increasingly becoming a bottleneck until multicore processors were adopted in mid 2000s [7]. While this multicore approach helped manage the power dissipation, the frequency of operation became limited. Besides, the dielectric is already approaching its physical limit ($\sim$1 nm), and the transistor architecture is no longer planar. However, the numbers of transistors in a processor are still increasing to this day, as is evident from Fig

[1] ↑Some of the content of this chapter is based on Ref. [2], [3]

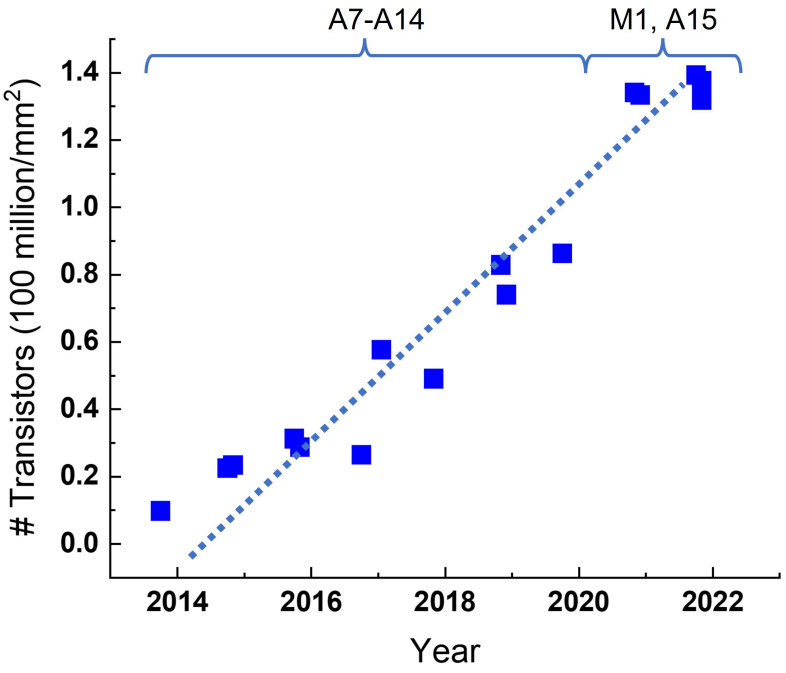


Figure 1.1. Number of transistors in Apple processors: A series (A8 to A15 Bionic) and M series (M1, M1 Pro and M1 Max). This plot has been constructed from the data available in [4]

1.1, which shows that the number of transistors in Apple processors. This trend has been possible due to constant improvement of fabrication processes, efficient thermal management, and innovative device architectures. Recent innovations like RibbonFET (Intel), Forksheet FET (IMEC), Multi-bridge channel FET (Samsung), Gate-All-Around (GAA) FET (IBM), etc., promises to keep the trend of increasing transistors in a processor, ongoing.

1.2.1 Self-Heating in Logic Transistors

As Dennard scaling in the early 1990s reduced the supply voltage, $V_D \rightarrow E_g \sim 1$V, the self-heating made the lattice temperature (T_L) of the channel higher than that of the substrate (T_S), such that $T_L > T_S$. The self-heating had already hindered the integration potential of two previous devices technologies (e.g., vacuum tubes and bipolar transistors), and was becoming an important performance metric. Briefly, $T_L = T_A + (P \times \theta_{th})$ where P is the

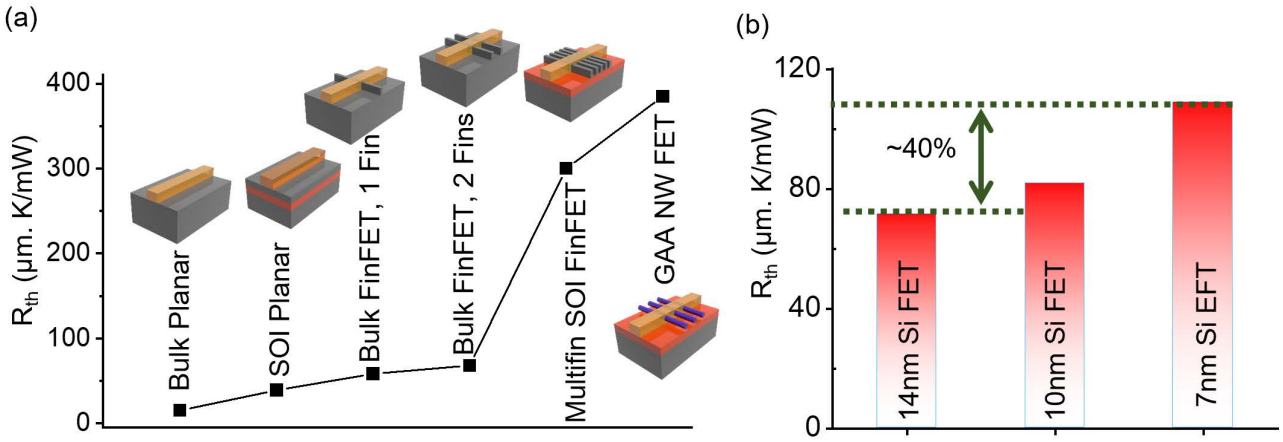


Figure 1.2. (a) Thermal resistance of bulk, SOI planar and FinFETs with various configurations and GAA nanowire FETs [Replotted from [2]]. (b) Thermal resistance of a 14nm, 10 nm and 7nm bulk Si FinFET [Replotted from[8]].

power dissipated by a transistor with area A and thermal resistance θ_{th}. Dennard scaling requires $P = P_0 \times A$, where P_0 is the power density of a transistor. Keyes calculated the elementary result that thermal resistance depends on effective thermal conductivity, λ, and transistor-substrate shape-factor, α, such that i.e. $\theta_{th}= \alpha/(\lambda \times\sqrt{A})$. This gives [2] ,[3]:

$$T_L = T_A + P_0\sqrt{A}\alpha/\lambda \tag{1.1}$$

While for a planar transistor technology, α and λ are constants, effective λ reduces significantly in non-planar technologies like FinFET. This led to a dramatic increase in T_L [9]. This is illustrated in Fig 1.2. While FinFET helped manage the short-channel effects through improved electrostatic control, the channel is now surrounded by low-thermal conductivity oxides, which leads to a corresponding increase in the θ_{th} and T_L. Careful modeling in [8] shows that θ_{th} increase by more than 40% when fin width is reduced from 14nm to 7nm technology, as shown in Fig 1.2 (b).

While a precise calculation of T_L due to self-heating is difficult, several attempts has been made to quantify it since 1970s to quantify it. Sesnic and Craig reported T_L due to self-heating in MOSFETs at cryogenic temperatures (4.2 K) in 1972 [10]. Mautry and Trager reported T_L due to self-heating in sub-μm MOSFETS using dynamic drain current measure-

ments with a time-resolution of 3 ns, in 1989 [11]. Eventually, multiple techniques such as four-terminal gate resistance [12], pulsed I-V [13], AC output conductance [14], etc., have been used to measure average channel temperature. Among them, thermoreflectance is one of the most sophisticated techniques, which uses sub-micrometer illumination sources (∼400-800 nm) offering a higher resolution compared to other methods and also enabling mapping of transient heating and cooling kinetics with 50-ns resolutions [15]. Thermoreflectance was used to measure average channel temperature in junction-less transistors (β-Ga_2O_3), [16], InGaAs GAA FETs [17], extremely thin SOI (ETSOI) [18], etc., which not only provided an accurate T_L due to self-heating, but also a closer look into the kinetics of reliability mechanisms, like HCD.

1.2.2 Hot Carrier Degradation in Logic Transistors: Correlation with Self-Heating

During MOSFET operation, the carriers get accelerated due to applied gate (V_G) and drain voltage (V_D). Some of these carriers, generated during impact ionization at high fields, become energetic (hot) enough to dissociate the passivated Si-H bonds in the semiconductor/oxide interface when injected into the gate, as shown in Fig 1.3 (a). This phenomenon is known as hot carrier degradation (HCD) and has been observed since the early days of MOSFETs [2]. HCD in a classical MOSFET peaked when $V_G \sim V_D/2$. This is because, at $V_G \sim V_D/2$, barrier height is low enough to inject a significant amount of electrons in the channel, and at the same time, the vertical field at the gate/drain edge is high enough to cause injection into the gate.

The rate of bond dissociation due to HCD is given by [2]:

$$\frac{dN_{it}\left(E_B,x,t\right)}{dt} = \sum_{E_B,x} k_f\left(E_B,T_{\mathrm{e}},T_L\right)\left[\left(N_0\left(E_B,x\right) - N_{it}\left(E_B,x,t\right)\right)\right] \tag{1.2}$$

where, T_L is the lattice temperature, T_{e} is the electron temperature, $N_0(E,x)$ is the initial number of unbroken bonds with binding energy, E_B, located at a distance x from the source, $N_{it}\ (E,x,t)$, is a fraction of these bonds broken as a function of time t. The rate of bond dissociation depends on how hot the carriers (electrons) are. As shown in Fig. 1.3 (b), close

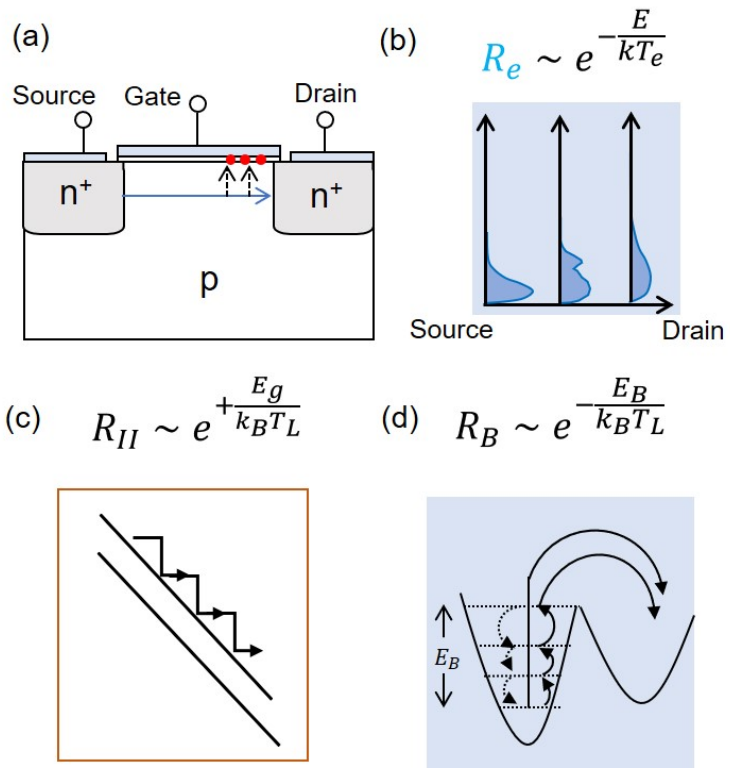


Figure 1.3. (a) A schematic representing HCD in MOSFET. (b) A schematic of the evolution of carrier distribution, from Boltzmann to heated Boltzmann distribution, as the electrons travel from the source to the drain. (c) A schematic showing negative temperature coefficient of HCD, due to reduction in impact ionization. (d) A schematic showing multiple-particle process due to increased interfacial bond vibration, leading to positive temperature coefficient.

to the source, the electrons possess relatively low energy and are Boltzmann distributed. As the electrons move towards the drain, under the influence of the electric field, the energy of the electrons increase [19]. As a result, the distribution may show a ballistic peak or a heated Maxwellian profile near the drain region, which increases the T_e and hence the degradation (R_e). The dependence of T_L is, however, complicated.

An increase in T_L led to increased lattice vibrations which siphoned off the electron energy to reduce T_e. As a consequence, this process reduced impact ionization (shown in Fig. 1.3 (c)), which would reduce HCD and increase device lifetime. This means that historically, HCD had a negative temperature coefficient (R_{II}). One of the most successful models which explained all these characteristics is the "Lucky Electron Model", where the degradation can

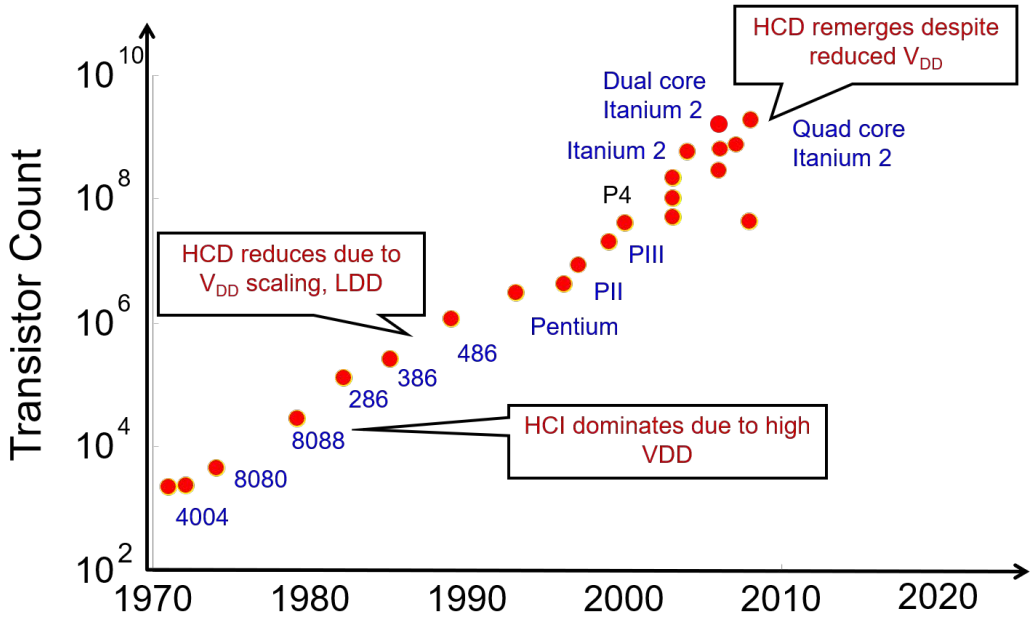


Figure 1.4. Hot Carrier Degradation trends in Intel microprocessors [20].

be described as a power law ($\Delta = At^n$) [21]. However, as device dimensions scaled-down, HCD became increasingly complicated. As T_L increased the lattice vibrations, a few low energy carriers came together to surmount the energy barrier, E_B, in ultra-scaled devices, as shown in Fig. 1.3 (d). This resulted in a positive temperature coefficient for HCD (R_B). This positive temperature activation led to the resurgence of HCD, as shown in Fig 1.4 [20].

HCD was first discovered in bipolar junction transistors (BJT), and the negative temperature coefficient was well understood [22]. It was a dominant degradation mechanism in the mid-1980s when the supply voltages were high. Innovations like lightly-doped drain (LDD) structures helped keep HCD manageable until the early 2000s [23]. As the devices were scaled down further, the reliability became more complicated. Ultra-scaled devices like FinFETs uses high-k dielectrics, which have low λ, thus increasing self-heating, which exacerbated HCD further [8]. This is evident in Fig 1.5, where the threshold voltage (ΔV_{th}) and on-current (ΔI_{on}) degrades more in multi-fin structures. Although it was expected that increasing the fin number would proportionately increase the current, it was found that, both the ΔV_{th} [24] and ΔI_{on} [25] were degraded due to mutual self-heating from nearby fins.

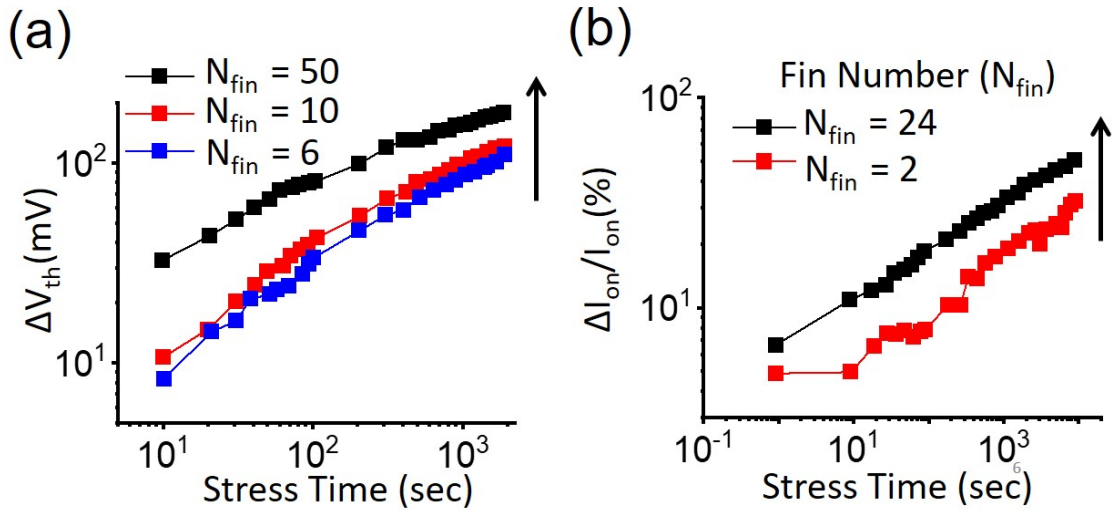


Figure 1.5. (a) Threshold voltage degradation due to fin number variation is reported in [24], and replotted here. (b) On-curent degradation due to fin number variation is reported in [25], and replotted here.

Detailed finite element simulations [26] have confirmed that the fins located in the middle are the worst affected ones.

While 'scaling down' was the trend in logic transistors, 'scaling up' was the trend for power transistors since its inception in the 1950s. Although the temperature activation of HCD in power transistors is positive, the kinetics appear to be different than classical MOSFETs because of varied geometry, oxide thickness, and operating voltage.

1.3 Power Transistors

As innovations in microprocessors made computation faster, innovations in power transistors increased the power handling capacity and switching frequency. Nowadays, the power electronics industry exceeds billions of dollars and has widespread application in the personal electronics, motor controls, photovoltaics, military, energy transmission,and transportation sectors. Based on the voltage rating, the applications can be categorized as either low, medium, or high voltages applications, as shown in Fig. 1.6. Just like the microprocessors, power transistors have an exciting history, which will be discussed next.

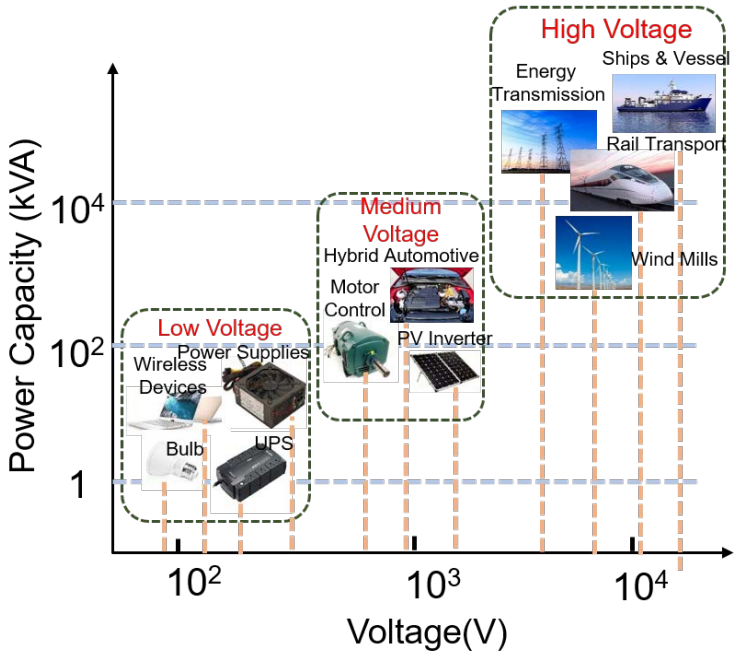


Figure 1.6. A few of the many power electronics applications.

1.3.1 Brief History of Power Transistors

After the invention of the transistors, there was a demand to increase the power handling capacity of these devices. BJTs, and not MOSFETs, were initially touted as the future of high power devices because of their high current (∼100s of amperes), voltage (>500V) handling capacity, and mature technology in the 1970s [27]. However, the current gain of BJTs was low when it was operated at high voltages, and the safe operating area was poor due to several failure modes. While approaches like the Darlington configuration were proposed as a solution, high power dissipation became an issue because it led to degradation in efficiency [27].

Meanwhile, the MOSFET technology was undergoing tremendous advances, and International Rectifier Corporation (ICR) introduced power MOSFETs in the 1970s. MOSFETs possess high input impedances and fast switching speeds (>100 kHz), and therefore an ideal candidate for future power electronic devices. While the voltage rating was low, because of high on-resistance at high breakdown voltage, MOSFETs became the *de facto* choice for power switches. Other technologies, such as Insulated Gate Bipolar Transistor (IGBT) [28]

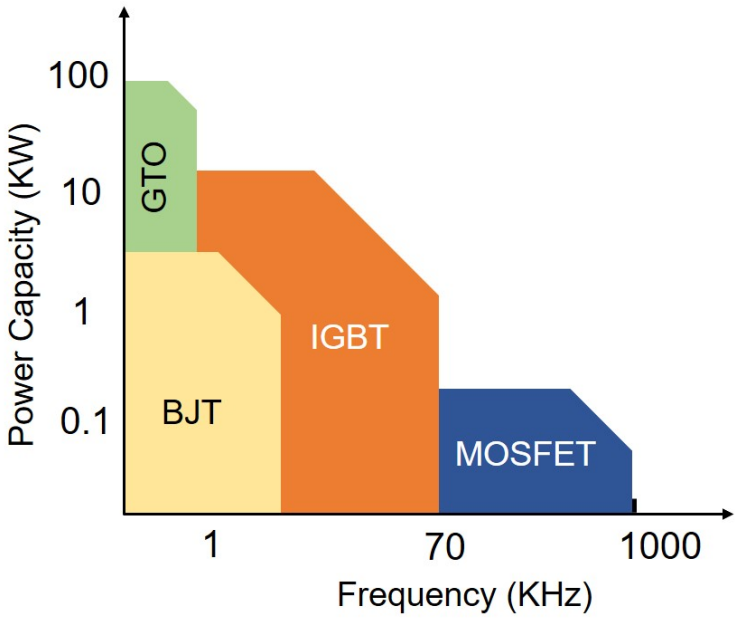


Figure 1.7. Different power devices and their power and frequency ratings. Adapted from [27]

and gate turn-off thyristor (GTO) [29], were later developed to function in the high voltage regime, as shown in Fig 1.7.

The MOSFET power transistors received a boost with the demonstration of double diffused structure in 1967 [30]. Laterally double diffused MOS (LDMOS) was reported in 1969 [31] by the Electrotechnical Laboratory (ETL) (now the National Institute of Advanced Industrial Science and Technology) in Japan. Then Hitachi produced the LDMOS from 1977-1983 for audio power amplifiers. After that, many manufacturers started producing LDMOS for various applications like personal electronics, LTE networks, radar, medical technology, etc. By the 2010s, the breakdown voltage of LDMOS exceeded several kVs, and advancements were still being made worldwide. The brief history of LDMOS is schematically represented in Fig 1.8.

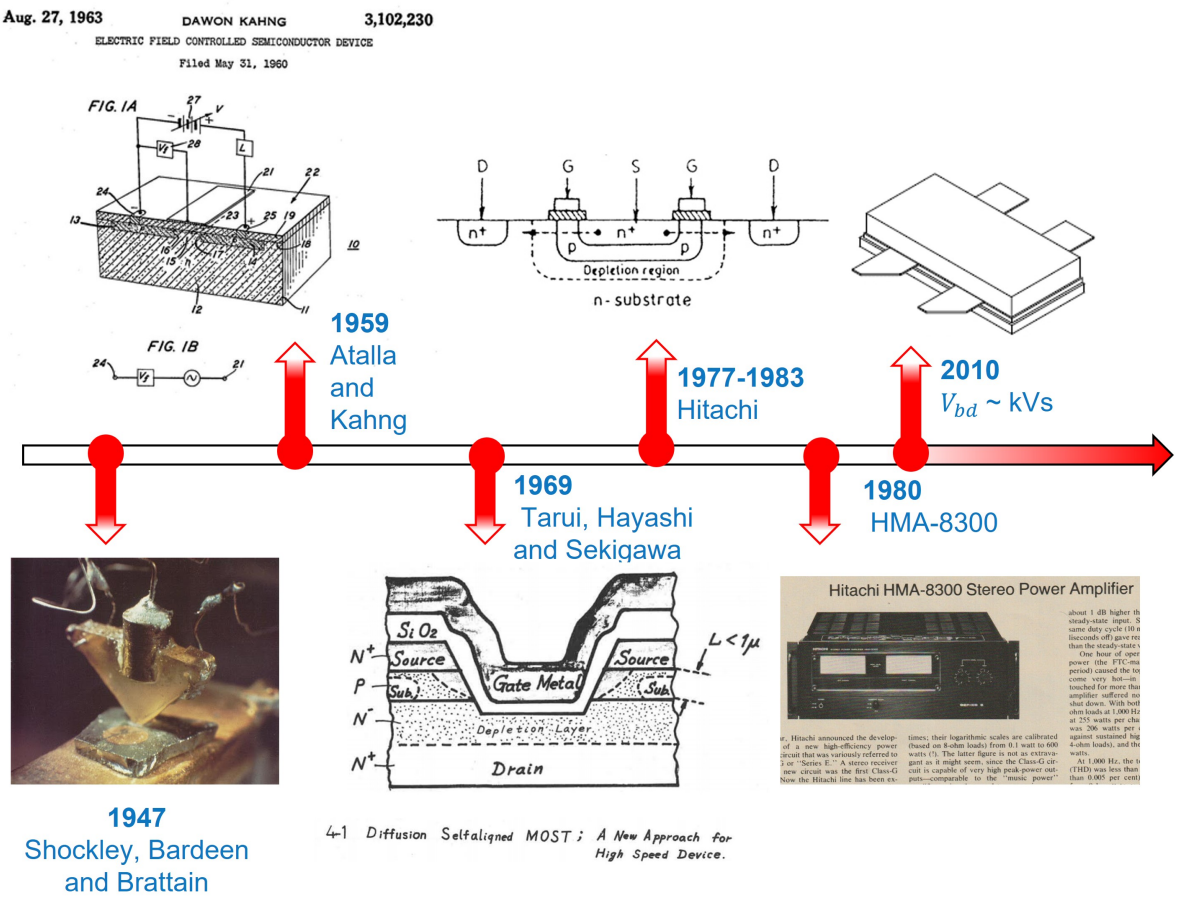


Figure 1.8. Different power devices and their power and frequency ratings [Image Source: Google Images].

1.3.2 Basic Principle of an LDMOS Transistor

The basic principle behind the LDMOS or any other high voltage MOSFET is to reduce the surface electric field to increase the breakdown voltage. The Poisson's equation is given as:

$$\frac{\partial^2 V}{\partial x^2} = -\frac{\partial E}{\partial x} = -\frac{q\rho}{\epsilon} \tag{1.3}$$

where q is the charge, ρ is space charge density, V is potential, and E is the electric field. The aim is to reduce the electric field following Eq. 1.3 [32]. As a first step, to reduce the channel electric field, a more extended channel is designed. In the following step, the drain diffusion area (n^+ region) can be increased to relax the space charge distribution and increase

the breakdown voltage [32]. The breakdown voltage can be increased by reducing the drain diffusion doping, which further relaxes the space charge distribution. However, decreasing drain diffusion doping will have adverse effects in inversion, leading to a lower current. Therefore, a lower doped 'drift' region is introduced between the channel and the drain. With optimum doping and thickness of the drift region, the depletion layer can be extended further than that for the one-dimensional lateral diode. This allows for bulk breakdown rather than junction breakdown. This approach of increasing the breakdown voltage was

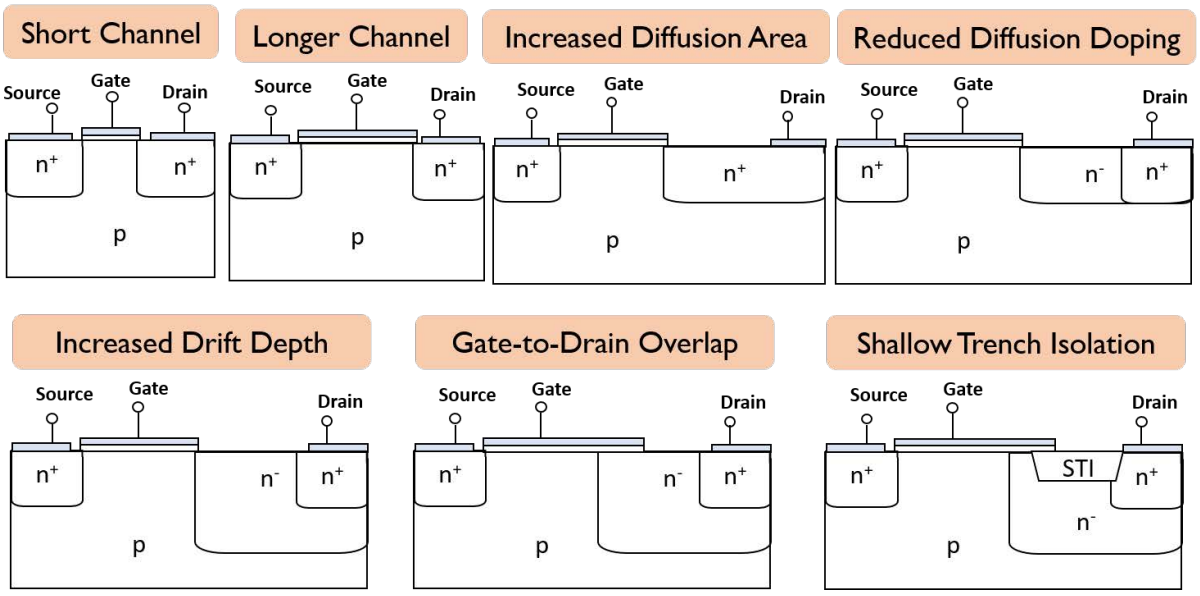


Figure 1.9. A schematic representation of design schema from low to high voltage transistors, following the Poisson's equation, Eq.1.3. This figure is redrawn from Ref. [32]

proposed by Appels and Veas in 1979 [33] and is known as the REduced SURface Field effect or simply the 'RESURF' effect. However, high on-resistance in the drift region, associated with the structure, degraded the device performance. Thus, the drift depth was increased instead of increasing the length and doping of the drift region. The type of configuration, known as the Drain Extended MOS (DeMOS) or LDMOS transistors. All these steps are schematically shown in Fig. 1.9. The gate-to-drain overlap and shallow trench isolation (STI) were introduced to increase the transistors' reliability [34].

1.3.3 Hot Carrier Degradation in LDMOS: Correlation with Self-Heating

Based on the applications, the applied biases on the LDMOS can be very high, which can accelerate the electrons greatly, thus making HCD a primary degradation mode in an LDMOS. The LDMOS contains a low doped drift region to sustain higher voltages, complicating the hot carrier degradation mechanism. First of all, it has been shown in many studies that, unlike the classical MOSFETs, the peak of HCD in LDMOS doesn't correspond to $V_G \sim V_D/2$ or to the peak of the substrate current (I_B), which is usually used as a proxy for gate current (I_G) [35]. In fact, in most of the current LDMOS, source and body are tied together, making the independent monitoring of I_B impossible. Secondly, the degradation

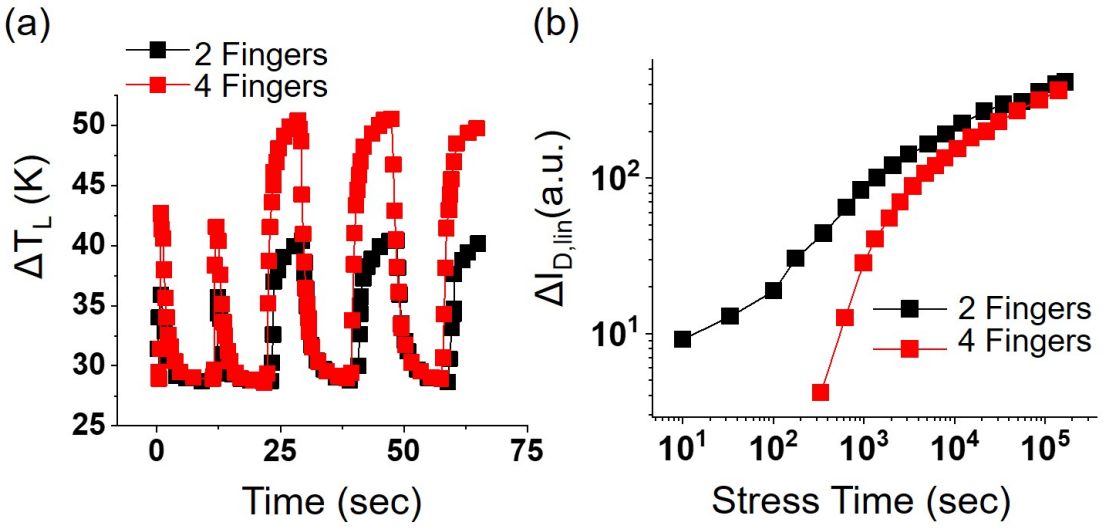


Figure 1.10. (a) Temperature rise in a 2-finger vs. 4-finger LDMOS. b) Linear drain current degradation in a 2-finger vs. 4-finger, as reported in [36].

doesn't precisely follow the power-law ($\Delta = At^n$) [37] and appears to have more than one time exponent, which points to complicated degradation kinetics. A previous study has attributed this anomalous degradation to oxide trap generation (N_{ot}) and interface traps (N_{it}), however, admitting that this phenomenon needs further investigation [38].

Unlike the ultra-scaled MOSFETs, an LDMOS has a planar geometry and is often used as a standalone device in a circuit, thereby avoiding the drawbacks of mutual self-heating. However, in some applications where gate resistance is critical or the layout requirements

are stringent, multi-finger LDMOS may be used, where self-heating plays a significant role. As shown in Fig 1.10 a 4-finger device has higher self-heating and consequently lower $\Delta I_{D,lin}$ due to positive temperature coefficient of HCD [36].

1.3.4 Wide Bandgap Semiconductor Based Power Transistors

For the first few decades since the invention of the transistor, the semiconductor industry was limited to using Silicon, Germanium and conventional III-V materials, with bandgap less than 2.3 eV [39]. Although the advantages of using III-V materials were obvious (higher mobility, direct bandgap), the development of other wide bandgap materials was difficult at that time. U.S. Department of Defense Office of Naval Research initiated research to develop crystal quality of SiC (bandgap: 3.25 eV) in the 1970s, and GaN (bandgap: 3.4 eV), a few years later [40]. In 1982, B.J. Baliga, at General Electric, derived a relation between the on-

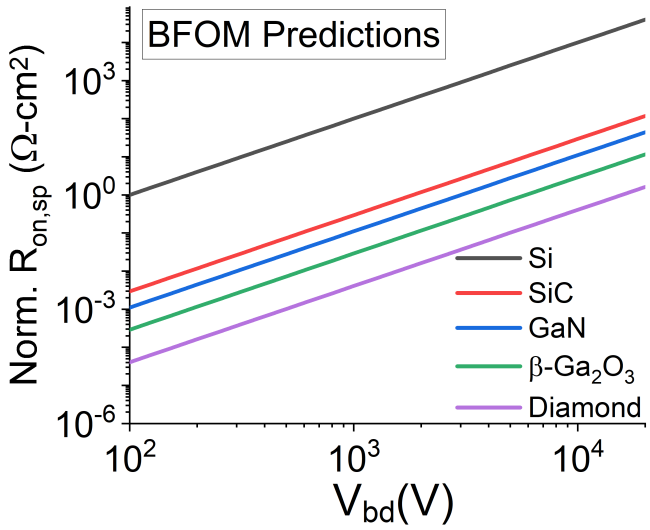


Figure 1.11. The predictions by the Baliga Figure of Merit (BFOM) [41], for wide bandgap semiconductors.

resistance of the drift region, and breakdown voltage, using basic semiconductor properties of the material, which is known as the Baliga Figure of Merit (BFOM) [41]. The relation is given as:

$$\frac{V_{bd}^2}{R_{on,sp}} = \frac{\varepsilon \mu_n E_C^3}{4} \tag{1.4}$$

where $R_{on,sp}$ is the specific on-resistance, V_{bd} is the breakdown voltage, ε is the dielectric constant, μ_n is the electron mobility, E_C is the critical electric field. This metric suggested that wide bandgap materials (materials with higher E_C) would have a higher breakdown and hence perform better than Silicon for unipolar power devices. A plot of BFOM for various wide bandgap materials is shown in Fig. 1.11. According to this plot, a power device made up of GaN will have an almost 1000 times smaller area than Silicon for the same breakdown voltage. This had huge implications and could pave the way for smaller, faster, and greener electronics. However, the development of wideband gap electronics was still at a nascent stage and not yet adopted widely.

All these changed in the early 1990s, with seminal breakthroughs in optoelectronics by Isamu Akasaki, Hiroshi Amano, Shuji Nakamura (2014 Nobel Prize in Physics, blue LED) [39], and many others in this field. This stemmed a worldwide interest, and the research in physics, chemistry, and fabrication of wide bandgap materials received a huge boost, from which the power electronics industry benefited immensely. Starting from SiC Schottky diodes, which were first commercialized by Infineon in 2001, almost all of the Silicon technology have their wide bandgap counterparts, and commercialized by various companies. Currently, GaN and SiC are mature technologies, having applications in automotive, consumer, telecommunication, and energy sectors, with global market values projected to be around billions of dollars in the next few years. With the success of GaN and SiC, the power electronics industry and research groups began to explore other materials to further improve the performance. Among them, β-Ga_2O_3 (bandgap $\sim$ 4.5 eV) and Diamond (bandgap $\sim$ 5.5 eV) are already demonstrating significant potential. However, these technologies are still at an initial stage of development, as GaN and SiC were in the 1980s, with room for understanding and orders of magnitude improvement in performance.

The immense interest behind β-Ga_2O_3 is due to its high BFOM value, and true to its prediction, $\sim$4.5 eV bandgap leads to a breakdown field of 9 MV/cm [42]–[46]. Studies on β-Ga_2O_3 have already established good controllability of doping using Si or Sn [47]–[49] . The

biggest advantage of β-Ga_2O_3 is the availability of large, high-quality native substrates, which can be grown following industry-standard techniques like Czochralski [50], vertical Bridgman [51], etc. Apart from demonstrating impressive diode and transistor characteristics [52],[53] β-Ga_2O_3 applications include high-temperature signal processing [54], solar-blind deep ultraviolet photodetectors [55], etc. However, β-Ga_2O_3 suffers from two major drawbacks which hinder its advances severely: (a) p-type doping is complex, making CMOS implementation extremely challenging [56]; (b) poor thermal conductivity (0.1-0.3 W/cmK) [57], leading to high self-heating and poor electrical performance. Currently, multiple research groups around the world are dedicated to research aiming at alleviating these issues. Compared to lateral devices, vertical devices, allow for superior current drives and field termination. The breakdown voltage of vertical devices scales with the drift layer thickness instead of gate-to-drain separation in lateral MOSFETs. In addition, the peak electric fields lie in the bulk region, rather than at the surface, which also gets rid of the reliability issues caused by the interface states [58]. Tremendous advancement has been achieved in vertical device fabrication in the last decade. Several groups have introduced MOCVD techniques to precise doping controls and breakdown voltages [59]–[63]. Despite these advantages, lateral devices are preferred because of their compatibility of integration with commercial-off-the-shelf devices and smart technologies.

Diamond is another material that possesses impressive inherent properties and is presently being researched worldwide for next-generation power devices. Diamond has some of the highest thermal conductivity (20 W/mK), electron mobility ($\sim$2000 cm^2/Vs), breakdown field (>10 MV/cm), saturation velocity ($\sim$2.5 $\times 10^7$ cm/s) among all known materials [54]. Already power devices made with remarkable performances were demonstrated on Diamond (Schottky diodes with >10 kV breakdown voltage [64], BJTs with >500 A/cm^2 current and >500 V breakdown voltage [65], etc.). The major drawbacks for Diamond are: (a) Lack of low-cost large area substrates; (b) Deep doping levels (0.3 eV for Boron [66] and 0.57 eV for Phosphorous [67]). However, progress has been made towards efficient doping [68] and the realization of single-crystal substrates using CVD [69].

Besides β-Ga_2O_3 and Diamond, the wide bandgap materials which are of enormous interest for power electronics are BN [70], AlGaN/AlN [71], $MgGa_2O_4$ [72], etc. Meanwhile

BFOM, while foreshadowed the use of the wide bandgap materials for power electronics initially, fails to predict the performance of materials like β-Ga_2O_3 and Diamond accurately, w.r.t Silicon. This is because BFOM (or other traditional FOMs) doesn't consider the crucial parameters like self-heating, incomplete-ionization, reliability, etc. synergistically. As more materials are being explored, it is becoming crucial to predict wide bandgap materials' performance before device fabrication. This necessitates the development of a holistic evaluation performance metric for all materials. The safe operating area (SOA) could be one such metric.

1.4 Safe Operating Area

SOA is defined by a collection of performance metric, which dictates the safe operating conditions of a power transistor. SOA is an indicator of device robustness and can either be calculated or measured for a device. Measured SOA presented in commercial device datasheets are usually derated (up to 35%) to guarantee that SOA will hold for different applications. Figure 1.12 shows a typical SOA of a transistor in forward bias. Four major limitation lines of an SOA are [73]: (a) on-resistance (R_{on}); (b) maximum Current (I_{max}); (c) maximum power (P_{max}); and (d) breakdown voltage (V_{bd}). Let's take a detailed look into the four parameters:

(a) R_{on} **Limitation**: The on-resistance of the device limits the maximum current that flows through the device. Or in other words, this line gives the maximum on-resistance at the maximum allowed junction temperature. R_{on} limitation line has a positive slope of 1, because all points on this line represent the same resistance (Ohm's Law).

(b) I_{on} **Limitation**: In a typical SOA, current ratings are not measured but calculated based on the intended operation. As a result, a typical data-sheet contains several current ratings like the package limit, silicon limit, continuous drain current limit, pulsed drain current limit, etc. While the package limit of current is dictated by the actual physical limitation of the package, the silicon limit defines the maximum allowable current the Silicon die can handle at a predefined case temperature. The silicon limit assumes an ideal heat sink and that the case-to-ambient thermal impedance is zero. The continuous drain current

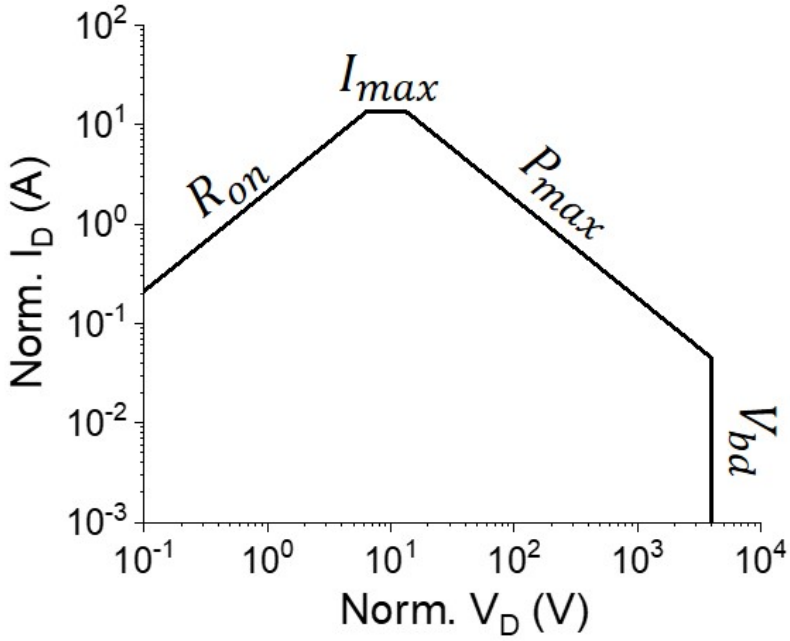


Figure 1.12. A typical Safe Operating Area (SOA) plot for a power transistor.

limit, on the other hand, is a function of the junction-to-ambient thermal impedance of the device and is much lower than the silicon limit.

The pulsed drain current limitation is the amount of current the device can handle for a certain duty cycle. Here the transient thermal impedance is used, instead of the steady-state thermal impedance, as with the other current limits. Obtaining transient thermal impedance is complicated, but in a nutshell, the expression of transient thermal impedance is the steady-state thermal impedance multiplied by a normalization factor, which is a function of pulse duration and duty cycle [74].

(c) P_{max} **Limitation**: This line gives the maximum allowable power for the device, at a maximum junction temperature. P_{max} limitation line has a slope of -1, because all points on this line represent the same power.

(d) V_{bd} **Limitation**: It is simply the breakdown voltage of the device. Factors like self-heating, impact ionization, reliability, etc. will affect the limits of SOA. Hence, obtaining an SOA for wide bandgap materials currently being assessed as potential power electronics

materials will be significantly helpful. The radiation reliability of the power transistors will be studied next.

1.5 Radiation

Power transistors form the basic building blocks of power management integrated circuits (PMICs), which perform multiple functions like battery charging, DC/DC conversion, voltage scaling, etc [75]. Integrated circuits used in drones, planes, and space shuttles are among the numerous applications of PMICs. Let us take the example of lunar landing missions

Table 1.1. Average Radiation Dose by Lunar Landing Missions.This data is replotted from [76]

Mission	Total Duration	Lunar Surface Duration	Av. Radiation Dose
Apollo 11	08 days, 03 hours, 13 mins	21 hrs, 38 mins	0.18 rad
Apollo 12	10 days, 04 hours, 31 mins	31 hrs, 31 mins	0.58 rad
Apollo 14	09 days, 00 hours, 01 mins	33 hrs, 31 mins	1.14 rad
Apollo 15	10 days, 01 hour, 11 mins	66 hrs, 54 mins	0.30 rad
Apollo 16	11 days, 01 hour, 51 mins	71 hrs, 02 mins	0.51 rad
Apollo 17	12 days, 13 hours, 51 mins	74 hrs, 59 mins	0.55 rad

(Apollo 11, 12, 14, 15, 16 and 17) where 12 astronauts walked on the moon. Table 1.1 summarizes the average radiation doses experienced by these missions. Although the radiation doses given by Table 1.1 seem low, it can significantly increase during solar maximum and due to prolonged exposure (such as in case of International Space Station). These increased radiation dose may induce defects in the power transistors and alter the predicted lifetime.

This following sections discusses a brief overview of the type and sources of radiation and the impact of radiation on a MOSFET.

1.5.1 Ionizing and Non-ionizing Radiation

Radiation is broadly defined as energy in the form of electromagnetic waves. A common example of radiation is sunlight, which helps sustain life on earth. Based on its energy (or wavelength), radiation can be categorized as either ionizing or non-ionizing. Ionizing

radiation has enough energy to knock off tightly bound electrons from atoms in the material [77]. Exposure to ionizing radiation can have devastating effects on human, animal, and plant life. One such example is the nuclear accident in Chernobyl Nuclear Power Plant, Ukraine on April 1986. 100s of people, including firefighters and first responders, during the accident, and later 1000s of people around Chernobyl, were found to have been exposed to high doses of gamma radiation, originating from the decay of radioactive isotopes of uranium or plutonium, with many suffering health-related issues.

On the other hand, non-ionizing radiation doesn't have enough energy to knock off the electron but can cause them to vibrate and generate heat. A typical example of non-ionizing radiation is that of microwaves used for heating our food. Fig. 1.13 shows the electromagnetic spectrum, categorized as ionizing and non-ionizing radiation. X-rays and gamma rays, which have very high energy (small wavelength), are classified as ionizing radiation. Visible light,

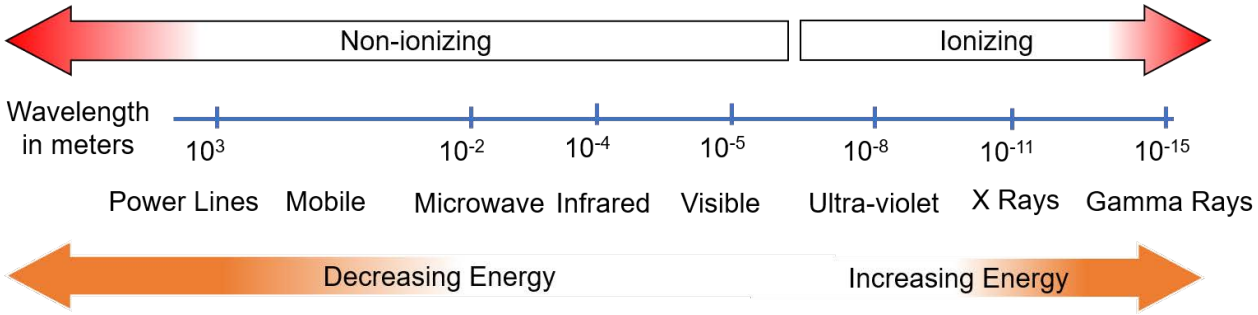


Figure 1.13. A schematic of the regions of the electromagnetic spectrum, categorized as ionizing and non-ionizing radiation.

microwaves, infrared, etc. are on the left part of the spectrum and classified as non-ionizing radiation. In this thesis, the impact of ionizing radiation on power devices will be analyzed.

1.5.2 Ionizing Radiation Sources

Broadly speaking, the ionizing radiation sources can be classified as: extra-terrestrial and terrestrial. Let us discuss these radiation sources briefly.

(a) **Extra-terrestrial sources**: These sources can be assigned as either cosmic rays or solar flares. Cosmic rays originate from sources beyond our solar system and can have energies exceeding 10^{20}eV. A majority of these cosmic rays, about $5/6^{\text{th}}$ of them consists

of protons, while $1/6^{\text{th}}$ of them consist of α particles and about 1% consists of heavy ions. The earth's magnetosphere, which extends thousands of miles into space depending on the earth's internal magnetic field, solar wind, and the magnetic field of other planets, trap a significant portion of these particles by magnetic and electric forces, which are much stronger than gravitational forces. This forms the inner (radius: 1200-6500 km) and the outer (radius: 13000-40000 km) Van Allen radiation belts. The inner belt contains high-energy electrons (a few MeV) and protons ($\sim$600 MeV), while the outer belt contains relatively low-energy electrons and protons (0.1 to 5 MeV) [78]. The portion of the cosmic rays that the magnetosphere cannot capture may reach the earth's crust and cause damages. Solar flares

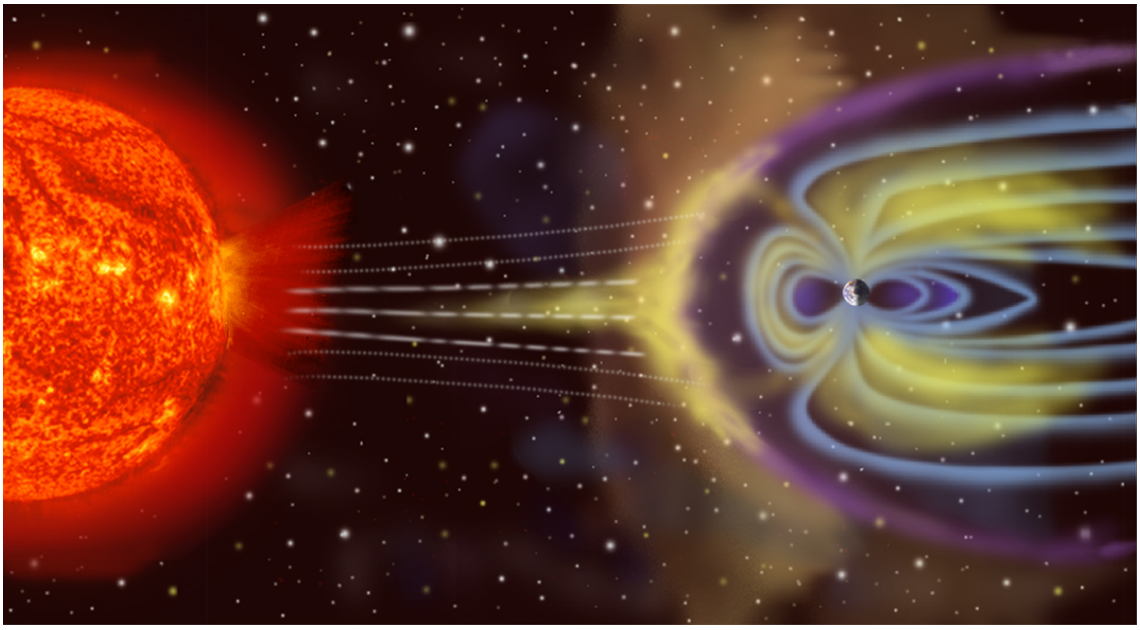


Figure 1.14. An Artist's rendition of Earth's magnetosphere. Image Source: [79]

originate from the Sun due to its composition and complicated rotation. Sun is a sphere of hot plasma comprising of very highly charged particles resulting from continuous nuclear fission. The magnetic field lines of the Sun periodically stretch out rather than looping back, resulting in a burst of plasma known as the 'solar flares', which sometimes cause geomagnetic storms. Solar flares follow roughly an 11-year cycle [80]. Most of the particles (>90%) generated during solar flares are protons (up to 500 MeV) [81]. A significant portion

of the particles due to solar flares are captured by the Van Allen radiation belts. Fig. 1.14, shows a representation of solar flares interacting with earth's magnetosphere.

(b) **Terrestrial sources**: The terrestrial sources can be further classified as cosmic ray neutrons and alpha particles from packaging materials. Despite the presence of Van Allen radiation belts, a large portion of the cosmic rays enters the earth's atmosphere, although less than 1% reaches sea level. Upon entering the earth's atmosphere, the cosmic rays (most of which are protons) are converted into secondary particles like neutrons, muons, pions, etc. [82]. While muons are pions doesn't cause much damage, some high-energy neutrons can knock off atoms from the lattice of matter, causing permanent damage. The neutrons can also react with Boron, forming an alpha particle accompanied by gamma rays.

Another terrestrial ionizing radiation source is the radioactivity of elements present in materials used for packaging. The radioactive atoms are unstable because of excess neutron or proton, resulting in radioactive decay. The decay continues in steps until the nuclear forces are balanced. This results in the emission of either neutron or proton particles or even alpha, beta, or gamma rays. Such radiation caused soft errors in DRAM chips in the 1970s by discharging some of the capacitors used to store data bits [83], [84].

1.5.3 Impact of Radiation on Transistors

Although radiation can have many different effects on the transistors [85]–[89], only Total Ionizing Dose or TID is studied in this thesis. A device may be exposed to radiation for a prolonged time. The cumulative effects of such exposure may lead to parametric degradation and possible functional differences in transistors. This phenomenon is referred to as the TID [90].

In TID, the most sensitive part of a transistor is the oxide. When a high energy radiation hits the device, electron-hole pairs are generated. A portion of the generated electron and holes quickly recombined. The remaining electrons are promptly swept out, whereas the holes surviving the recombination are left in the oxide. This is because the velocity of electrons in the oxide is orders of magnitude higher than the holes. As holes start hopping towards the Si/SiO_2 interface due to the electric field, H^+ is generated, which can travel to

the interface and create N_{it}. Some of the holes also get trapped in the oxide, and generating oxide defects (N_{ot}). This process is schematically represented in Fig 1.15 [91]. While N_{it} will lead to mobility degradation and low on-current, N_{ot} will mostly contribute towards threshold voltage shifts. The positive charge of the holes, will reduce the threshold voltage.

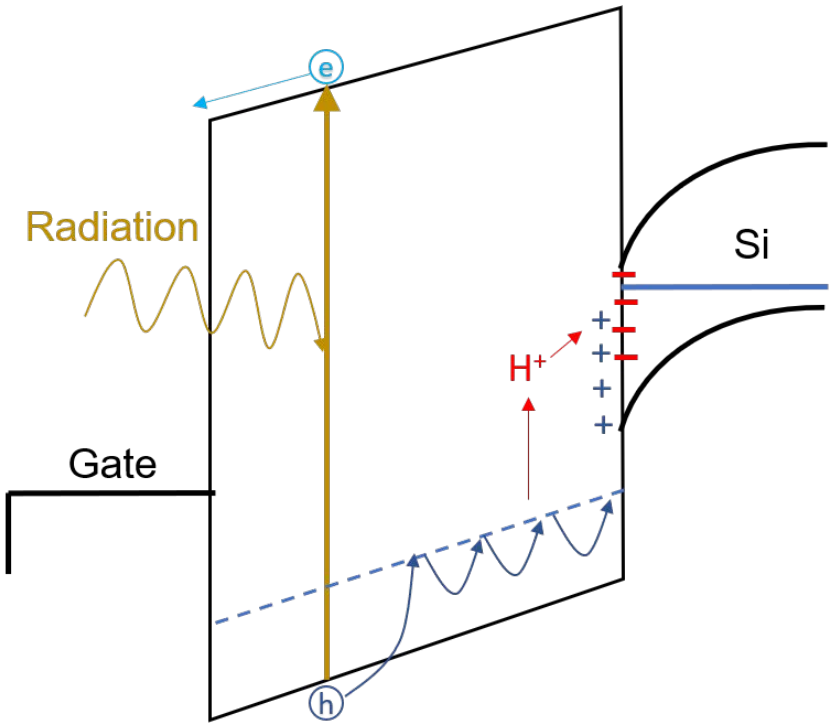


Figure 1.15. Mechanism of Total Ionizing Dose (TID) in a transistor with a thick oxide. The schematic is replotted from [91]

The relationship is given by [92]:

$$\Delta V_{th} = -\frac{Q_i}{C_{ox}} - \frac{1}{\epsilon_{ox}} \int_0^{x_0} x \cdot \rho_{ox}(x) dx \tag{1.5}$$

where Q_i is the interface charge, ρ_{ox} is the oxide charge density, x_0 is the oxide thickness. For thick oxide, such the ones in power transistors, the shift in threshold voltage, can be approximated as:

$$\Delta V_{th} \propto x_0^2 \tag{1.6}$$

Eq. 1.6 suggests that the effect of TID will be insignificant for modern logic transistors, where the oxide thickness is reduced to a couple of nanometers. However, TID will play a major role in the performance of power devices with thick oxides if they are exposed to radiation. The effects of TID will be studied in detail.

1.6 Reliability Concerns of a Power Electronic System

A schematic of a power electronics system is shown in Fig. 1.16. It usually comprises of power transistors, logic ICs, capacitors, inductors, diodes, resistors, etc., enclosed in a suitable package. The package provides mechanical integrity to the system, while also providing interconnection between components, means of heat removal, and protection from chemical (water, ions, etc.) and physical (e.g., ionization) measures during handling and operation.

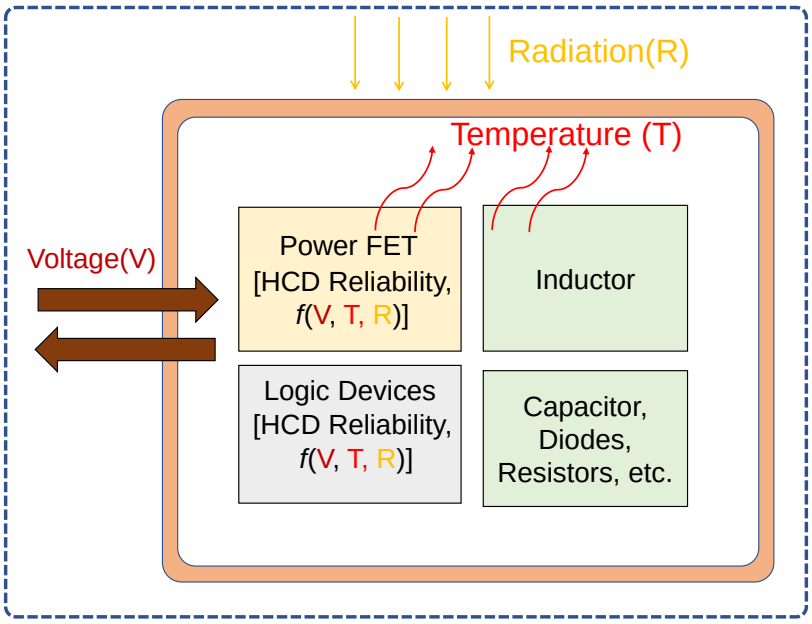


Figure 1.16. Schematic of a general power electronic system.

As described in the previous sections, the power and logic transistors in the power electronics system undergo electrical degradation due to applied bias and radiation. In addition, the inductor, capacitor, and diode may experience several reliability issues depending on the operations and environmental factors. A few reliability issues are discussed here:

(a). **Inductors**: Depending on the structure, inductors can be categorized as Common Mode Choke Coil (CMCC) and Surface Mount Power Choke Coil. While CMCC is used for noise reduction in power lines, surface mount inductors are used in power conversion circuits (e.g. Boost converter). Some of the common failure modes of such inductors are due to mechanical stress, vibration, excessive electric current during operation, damage of insulation coating, etc, leading to parametric degradation. Surface oxidation and rusting may also occur, which cause a drastic change in the magnetic properties of the core.

(b). **Capacitors**: One of the most common failure modes in a capacitor is that of dielectric breakdown. The dielectric materials can become brittle with the operation, leading to eventual failure. High voltage transients and high local temperatures can accelerate this process. High local temperatures can also lead to an 'open' condition, where the ends are not connected. In addition, electrical and environmental factors can 'short' conditions, by external bridging, delamination of adjacent layers, cracking, etc.

(c). **Diodes**: Like capacitors, although diodes can fail by short and open circuit conditions, failure by a short circuit is most common in power applications. A repeated operation can lead to an increase in resistance of the semiconductor, and it can further lead to a change in breakdown voltage, reverse leakage current, forward bias voltage, etc. In addition, environmental factors can also lead to several reliability issues.

We acknowledge that several modes of degradation (electrical, mechanical, and environmental) can affect the performance of a power electronics system. In this thesis, however, we will be focusing on the electrical (HCD) and radiation (TID) reliability of power transistors only. Incorporating the electro-thermal reliability in designing the SOA of power transistors and then coupling it with radiation reliability, is the first step towards the broad objective of developing a general, all-inclusive reliability framework for all components in a power electronics system.

1.7 Thesis Organization

This thesis is organized as follows:

In Chapter 2, we propose an analytical SOA that can predict the performance of wide bandgap semiconductors before actual device fabrication by considering all the major shortcomings of the existing performance metrics in the literature.

In Chapter 3, we analyze the electrothermal reliability of β-Ga_2O_3 transistors. We test the performance of β-Ga_2O_3 transistors in power electronic circuits in order to establish a comprehensive device-circuit model to test the predictions by the SOA further.

In Chapter 4, we put a traditional power transistor, an LDMOS, into the test. With combined experiments and analytical modeling, we establish the fact that the HCD is universal, be it a power transistor or a classical transistor.

In Chapter 5, we dive deeper into the HCD of LDMOS using numerical simulations. Using TCAD, we predict the HCD degradation for a variety of LDMOS structures and delineate the limitations of the TCAD models.

In Chapter 6, we investigate the impact of radiation on LDMOS devices. We study the correlation among the generation of trapped holes, interface defects, due to radiation and that of HCD.

Finally, Chapter 7 summarizes the thesis and discusses future work.

2. SAFE OPERATING AREA OF WIDE BANDGAP SEMICONDUCTORS

2.1 Introduction

In order to holistically analyze the reliability of power electronics, we need to define a metric, which can encompass all sources of variations. Therefore, in this chapter[1] we define a Safe Operating Area (SOA) for power transistors. An experimentally measured SOA diagram of a packaged and fully processed device ultimately defines the potential and guides the development of power electronics devices. The SOA of a MOSFET refers to voltage and current limits within which the device can be safely operated. Fig. 2.1 shows the

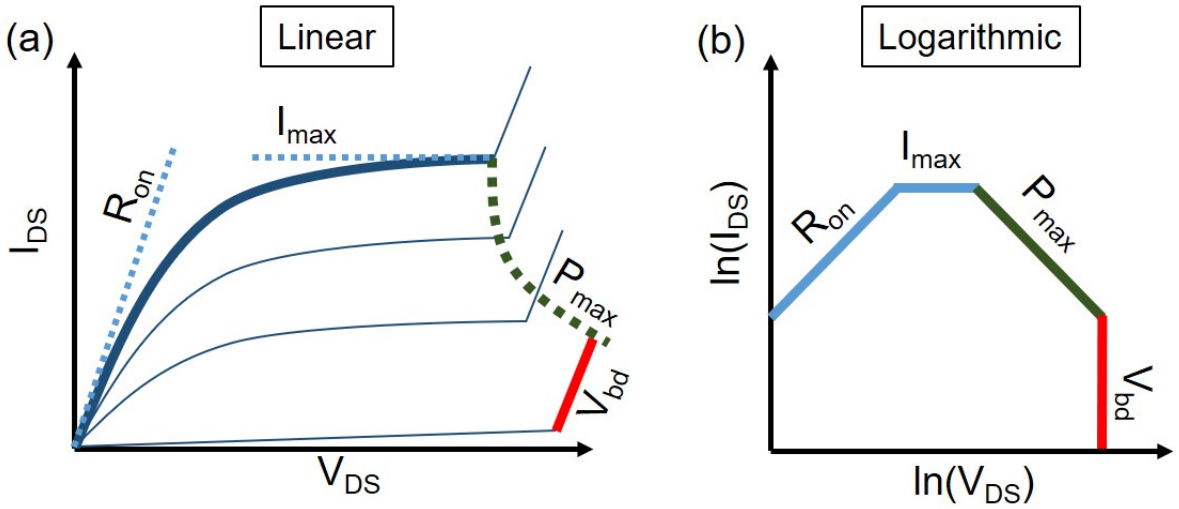


Figure 2.1. A typical Safe Operating Area (SOA) plot for a MOSFET in (a) linear scale, and (a) logarithmic scale.

output characteristics of a typical MOSFET. The important parameters of a MOSFET (on-resistance (R_{on}), breakdown voltage (V_{bd}), maximum current (I_{max}), and maximum power (P_{max})), can be easily calculated from the output characteristics. While the slope gives the R_{on}, the I_{max} can be determined easily at a given V_{GS}. The P_{max} can be obtained by setting a limit to the junction temperature. The V_{bd} can be easily obtained by applying high V_{DS} at zero V_{GS}. There parameters can be plotted in logarithmic scale to obtain the well-

[1] ↑Most of the content of this chapter is based on Ref. [93]

recognized SOA, usually provided in commercial device datasheets. The SOA deviates from its ideal form due to its thermal and reliability constraints. In addition, several factors must be considered in order to construct a realistic SOA, such as ambient temperature (T_{amb}), switching frequency (f), duty cycle (D), thermal resistance (θ_{th}), etc. For example, operating at a higher ambient temperature leads to a lower I_{max}, a lower P_{max} in which a device can operate, and reduces the V_{bd} limits, thus leading to a decrease in the SOA. In addition, one must also carefully consider the temperature-related boundary conditions. For example, it may take several seconds while attaining a steady-state between the device junction and the package, and several minutes to achieve a steady-state between the device junction and the ambient. However, the power devices are sometimes used in applications where the applied pulses are in microsecond or millisecond regimes. Therefore, one must consider a transient thermal impedance instead of a steady-state thermal impedance to achieve a reliable SOA.

Despite its importance, it is difficult to reliably calculate the extrinsic SOA of emerging WBG semiconductors because of: (a) immature process technology, (b) unknown material parameters, and (b) lack of fully packaged devices. Therefore, in practice, several simple, easy-to-calculate, material-specific FOMs are used to define and compare the device potential of emerging technologies. For example, Baliga FOM (BFOM) [41] establishes a trade-off between V_{bd} and specific on-resistance ($R_{on,sp}$), provided that self-heating is non-existent. Other popular FOMs defined by Keyes [94], Johnson [95], Huang [96], Shenai [97], etc., variously emphasize self-heating, chip-area, operating frequency, charging time, etc., all in an effort to estimate the quantities of interest. Unfortunately, it is well known that these traditional FOMs often lead to confusing and inconsistent results regarding the performance potential of various emerging technologies [97]. These FOMs have been criticized for being no more than a "marketing tool" [97], leading to the random ordering of different materials depending on the choice of FOM, as shown in Fig. 2.2. For example, BFOM suggests β-Ga_2O_3 to be a promising material for power electronics with an excellent V_{bd} to $R_{on,sp}$ ratio [54], [98]. Yet, self-consistent simulations find the potential of β-Ga_2O_3 to be compromised by self-heating associated with its poor thermal conductivity (λ) [16], [99], [100]. There is a rise in temperature due to self-heating, with increasing power in a device. The self-heating of β-Ga_2O_3 transistors depends on the substrate it is fabricated on (Fig. 2.3), yet the traditional

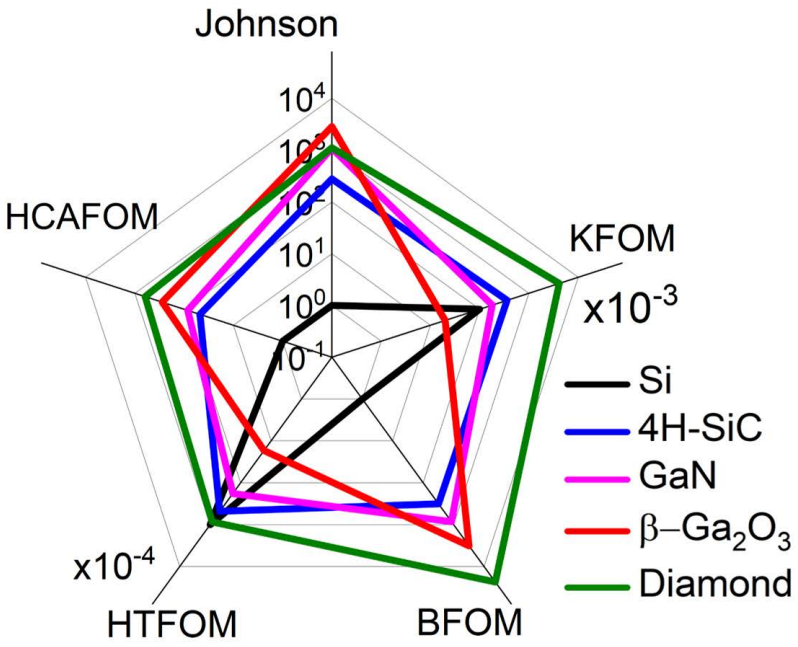


Figure 2.2. Radar Chart showing FOM values of different FOMs: Johnson FOM (JFOM), BFOM, Huang's Chip Area FOM (HCAFOM), Keyes FOM (KFOM) and Huang's Thermal FOM (HTFOM). The FOMs values are scaled to that of silicon. A constant factor scaling of KFOM and HTFOM allows a balanced display of various FOMs.

FOMs do not explicitly account for transistor substrates! Self-heating in LDMOS and GaN devices associated with relatively thick substrates is also evident. Therefore, in practice, technology development generally reverts to detailed and time-consuming material-device-circuit-system simulations or empirically measured parameters based on early-stage products to assess performance [100]–[103]. While resorting to this kind of end-to-end analysis is essential for device optimization, the approach might limit the ability to make the right decisions at an early stage of technology development, especially when the transport and thermal models of newly emerging wide bandgap (WBG) semiconductors, available in TCAD tools, are yet to be vetted against high temperature and high voltage data.

In this chapter, we show that recent progress in analytical modeling of the electro-thermal transient response of transistors with multi-layer substrates [18], [104], [105] as well as the development of generalized multi-hotspot reliability theories of power transistors [3], [93], [106], [107] allows us to construct an intrinsic SOA (i-SOA) that balances the multi-dimensional

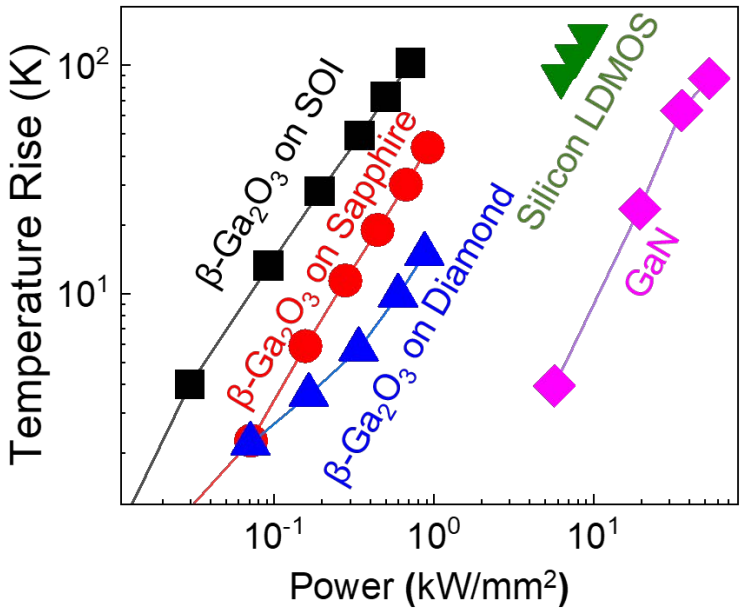


Figure 2.3. Self-heating of β-Ga_2O_3 transistors, depending on the substrate. Data from a GaN transistor and a silicon-based LDMOS is also plotted for reference.

trade-off among V_{bd}, $R_{on,sp}$, f, substrate-aware self-heating, and reliability. For calculation of i-SOA, it is assumed that the material is perfect (i.e., no defects like threading dislocation are present) and that packaging thermal resistance is negligible. Although the i-SOA obtained is not a substitute for industry-relevant SOA based on end-to-end modeling and careful qualification of packaged devices, it can be used to guard-band vast amount of experimental data reported in the recent literature and to assess the technology potential of WBG semiconductors at the early stage of development and identify the probable bottlenecks.

The chapter is arranged as follows. In section. 2.2, we derive the limits of i-SOA analytically. We rederive the trade-off between $R_{on,sp}$ and V_{bd} by including the effect of self-heating and explore its implications. We also derive the expressions for I_{max} and P_{max}. We evaluate the maximum current for WBG semiconductors based on intrinsic material properties. In Sec. 2.3, we obtain the substrate-aware i-SOA for different WBG semiconductors and systematically compare them with corresponding experimental data. Finally, Sec. 2.4 highlights the importance of self-consistent inclusion of transistor degradation, and we calculate

the reliability-aware i-SOA. We conclude the chapter by discussing the implications of the reliability-aware i-SOA for different WBG materials in Sec. 2.5.

2.2 Limits of 'Intrinsic' Safe Operating Area

2.2.1 Generalized On-Resistance

Initially proposed by Adler and Westbrook [108], the power electronics FOMs have traditionally focused on reducing $R_{on,sp}$, for a given V_{bd}. BFOM established a closed-form analytical formula relating R_{on} and V_{bd}. However, it needs to be generalized in order to include non-ideal effects, which become prominent during device operation. The next subsection will derive a generalized formula relating R_{on} and V_{bd}. Assuming a unipolar vertical power device with a drift region of width W, and doping N_D, the $R_{on,sp}$ is given as [41]:

$$R_{on,sp} = \frac{W}{q\mu_n N_D} \tag{2.1}$$

Assuming that the Poisson's equation leads to a triangular electric field distribution in the drift region, we can write:

$$V_{bd} = \frac{E_C W}{2} \tag{2.2}$$

From [41], for uniformly doped drift regions, the smallest on-resistance can be achieved when drift region depletion layer punch-through occurs simultaneously with avalanche breakdown, i.e.,

$$W = \sqrt{\frac{2\varepsilon V_{bd}}{qN_D}} \tag{2.3}$$

Using Eqns. 2.1, 2.2 and 2.3, BFOM for a vertical device is given by [41]:

$$BFOM = \frac{V_{bd}^2}{R_{on,sp}} = \frac{\varepsilon \mu_n E_C^3}{4} \tag{2.4}$$

For a lateral device, for example, the LDMOS, the breakdown voltage is given as:

$$V_{bd} \sim E_C L \tag{2.5}$$

where L is the lateral length of the drift region. The $R_{on,sp}$ for the LDMOS is given as:

$$R_{on,sp} = \left(\frac{\rho L}{WT}\right) WL = \frac{L^2}{q\mu_n N_D T} \tag{2.6}$$

where ρ is the resistivity, T is the lateral thickness, and N_D is doping of the drift region of LDMOS, and W is the width of the LDMOS. Therefore, BFOM for lateral devices can be written as [109]:

$$BFOM_{\text{lateral}} = \frac{V_{bd}^2}{R_{on,sp}} = V_{bd}^2 \left(\frac{q\mu_n N_D T}{L^2}\right) = \varepsilon \mu_n E_C^3 \tag{2.7}$$

From Eqs. 2.4 and 2.7, it is evident that BFOM expression for vertical and lateral devices are very similar. So, the generalized version of $R_{on,sp}$, that will be derived here will be appliable for both vertical and lateral power transistors. The approach is to take all the individual terms in Eq. 2.4 and include the non-idealities of device operation before putting them back together.

The electron mobility, μ_n, in Eq. 2.4 depends on temperature and doping. This dependence not only stems from the ambient temperature but from self-heating associated with the operating conditions. The generalized expression is given by [110]:

$$\mu_n\left(T_{on}\right) = \frac{\mu_0}{1 + \left(\frac{N_D \xi(T_{on})}{N_{\text{ref}}}\right)^{\beta}} \left(\frac{T_{on}}{300}\right)^{-\gamma} \tag{2.8}$$

where T_{on} is the temperature at on-state, N_{ref} is the reference doping concentration of the material, μ_0 is the intrinsic mobility at T=300 K, β,$\gamma > 0$ are empirical exponents and $\xi(T_{on})$ is the ionization ratio of the dopants, calculated from the occupation probability function as (assuming n-type doping):

$$\xi\left(T_{on}\right) = \frac{-1 + \sqrt{1 + 4g_D \frac{N_D}{N_C} \exp\left(\frac{\Delta E_D}{kT_{on}}\right)}}{2g_D \frac{N_D}{N_C} \exp\left(\frac{\Delta E_D}{kT_{on}}\right)} \tag{2.9}$$

Here, ΔE_D is doping activation energy, g_D is the degeneracy factor, N_C is effective density of state in the conduction band. The optimum doping concentration, N_D and V_{bd} are determined at off-state, at the temperature T_{off}, so that,

$$N_D \xi\left(T_{off}\right) = \frac{\varepsilon E_C^2}{2qV_{bd}} \tag{2.10}$$

where the critical electric field, given by the empirical relation, E_C=$E_{C0}(1+\beta^* T_{off})$, increases with the temperature. The coefficient β^* accounts for the decreased impact ionization rate at higher temperatures. Finally, the on-resistance at a temperature T_{on}, is given by:

$$R_{on,sp}\left(T_{on}\right) = \frac{L_D}{q\mu_n\left(T_{on}\right) N_D \xi\left(T_{on}\right)} \tag{2.11}$$

Putting everything together we get:

$$R_{on,sp}\left(T_{on}\right) = \frac{4V_{bd}^2}{\varepsilon\mu_0 E_C^3}\left[1+\left(\frac{N_D\xi\left(T_{on}\right)}{N_{ref}}\right)^{\beta}\right]\left(\frac{T_{on}}{300}\right)^{\gamma}\frac{\xi\left(T_{off}\right)}{\xi\left(T_{on}\right)} \tag{2.12}$$

This is the generalized expression for $R_{on,sp}$. We will see below that Eq. 2.12 establishes a novel and essential temperature-dependent generalization of $R_{on,sp}$, and thus Eq. 2.4. The material parameters and device dimensions used in the calculations can be found in Appendix. A. Unlike the traditional FOMs, $R_{on,sp}(T_{on})$ in Eq. 2.12 analytically accounts for excess self-heating through its impact on mobility, dopant ionization ratio, and impact ionization rate. Previously, one needed to solve multiple equations numerically to include these effects [111]. The idealized bulk parameters in Eq. 2.12 are easily obtained from online databases (e.g., Ioffe Institute's semiconductor repository [112], first principle calculation [113]–[115], bulk measurements [16], [116], [117], and TCAD simulations [100], [118]–[120].

Counter-balancing the roles of self-heating in $R_{on,sp}$ and V_{bd}

For typical switching speeds ($f > 1$ kHz), T_{on}∼T_{off} because the thermal time constant of the whole system is large enough to avoid significant cooling during the on-to-off transition. For fully ionized materials with ΔE_D∼ kT_A, Eq. 2.12 predicts $\xi(T_{off})/\xi(T_{on})$∼1, so that

self-heating increases $R_{on,sp}(T_{on})$ through mobility degradation. However, for materials (e.g. Diamond) with deep dopants (i.e.,$\Delta E_D \gg kT_A$), the self-heating ionizes more dopants, so that $\xi(T_{off}) > \xi(T_{on})$. By Eq. 2.7, $R_{on,sp}(T_{on})$ is determined by the balance between reduced mobility and increased doping. Similarly, the self-heating-supported reduction of impact ionization rate, increases the critical field and V_{bd}.

Fig. 2.4(a) shows that self-heating reduces the performance potential of Si because of mobility degradation. Remarkably, this is not the case for Diamond, as shown in Fig. 2.4(b). When the power dissipation (P) increases from 0 kW/mm^2 (T = 300 K) to 8 kW/mm^2 (T $\sim$ 525 K), the increased ionization overcomes mobility degradation, leading to improved $R_{on,sp}$ [111]. Diamond benefits from self-heating because of its higher ionization energy

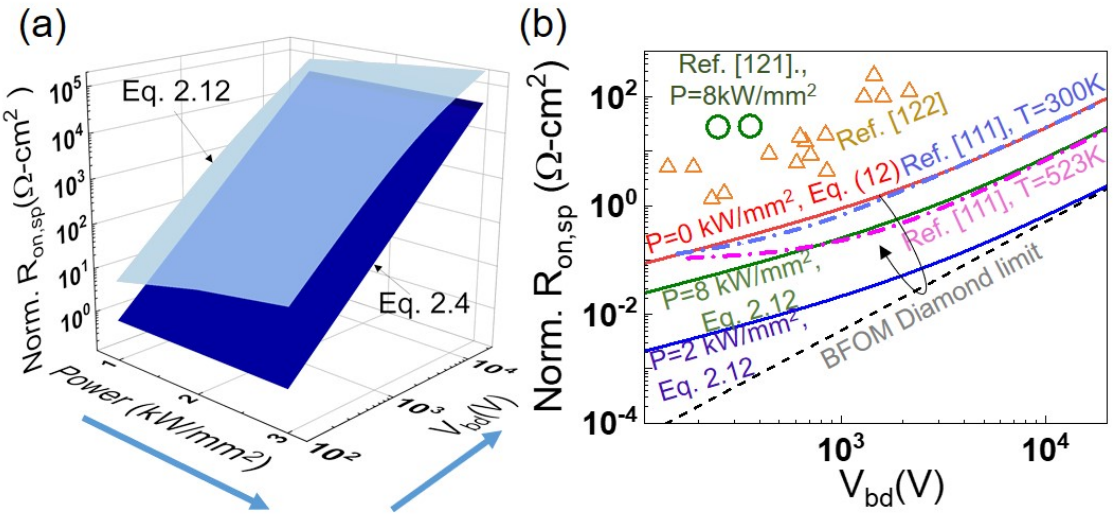


Figure 2.4. (a) While Eq. 2.4 is constant w.r.t. power, $R_{on,sp}$ (T_{on}) (for different power, P) varies depending on the degree of self-heating. As input power increases in a silicon device, self-heating increases as reflected in the curved contour in $R_{on,sp}(T_{on})$. The blue arrows indicate the direction of increasing values (b) $R_{on,sp}(T_{on})$ vs. V_{bd} for Diamond. The solid lines show $R_{on,sp}$ (T_{on}) [Eq. 2.12] for different applied power. BFOM for Diamond is given as the black dotted line. At T=300 K and 523 K, Eq. 2.12 matches the numerical results from [111], shown as dashed-dotted lines. The black arrow shows the turn-around for Diamond. Data from [121] and [122] are plotted as well for reference.

which is otherwise determined by its larger bandgap and its lower dielectric constant (e.g., Boron is an acceptor level with E_A = 0.37 eV [123]). The increasing conductivity with

P reduces $R_{on,sp}(T_{on})$. Note that Ref. [111] reaches similar conclusions through numerical simulations at increased ambient temperature; however, our work emphasizes the role of self-heating in achieving similar performance gain even at typical ambient temperature. However, increasing P beyond a critical value may lead to a reduction in $R_{on,sp}(T_{on})$ because of increased mobility degradation that eventually counterbalances the beneficial effects of self-heating (and reduces the gap between the experimental data shown by symbols and the corresponding performance limit). In short, Fig. 2.4 demonstrates the counterintuitive role of operating conditions in shaping the ultimate performance of power devices and the ability of $R_{on,sp}(T_{on})$ to capture the trend. Finally, Fig. 2.5 compares BFOM*(modified BFOM including self-heating, incomplete ionization, temperature and doping dependence of mobility.) for different materials at different power density. Eq. 2.12 predicts that standalone β-Ga_2O_3 is neither as good as predicted by BFOM, nor as bad as predicted by KFOM. Ad-

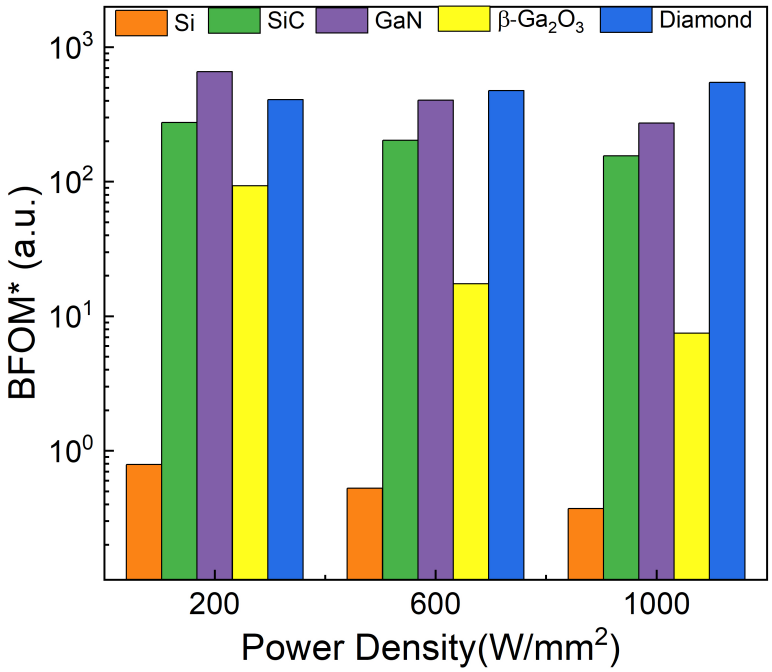


Figure 2.5. BFOM* calculated for different WBG materials at different power density.

ditionally, SiC and GaN have comparable performance. For the given $R_{on,sp}(T_{on})$, material performance degrades due to higher self-heating, except Diamond, which benefits from high self-heating. It is to be noted that Fig. 2.5 is calculated to show relative performance of

different materials at different power density. In practice, some of the power densities may not be achievable, due to severe self-heating.

Substrate-Aware $R_{on,sp}$

According to Eq. 2.12, the performance of materials such as β-Ga_2O_3, with high E_C, but with low thermal conductivity, may suffer due to self-heating. Therefore, an ultra-thin layer of β-Ga_2O_3 must be placed on top of a high thermal conductivity substrate (e.g., sapphire [16], Diamond [124], AlN [125]) for efficient heat spreading. While a lot of improvements are

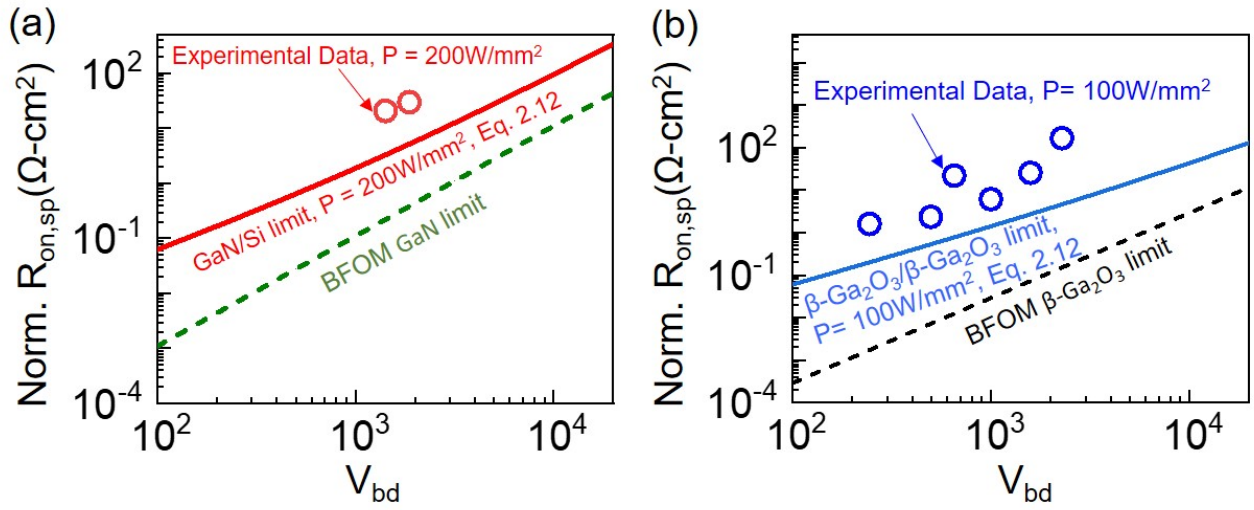


Figure 2.6. $R_{on,sp}(T_{on})$ (Eq. 2.12) predicted for bilayer GaN and β-Ga_2O_3 structures at $P = 1$ kW/mm^2 in comparison to the experimental data on bilayer structures. As an example, (a) GaN-on-Silicon [Data taken from [126]] and (b) β-Ga_2O_3-on-β-Ga_2O_3 device have been shown here. Data taken from [127].

required in the fabrication techniques of β-Ga_2O_3 FETs to emerge as the high performing power electronics substrate as originally promised, bilayer β-Ga_2O_3 devices should be compared against $R_{on,sp}(T_{on})$ expression (Eq. 2.12) to achieve realistic performance prediction of the technology. θ_{th} of the bilayer structures can be estimated using the simple formula provided in Appendix B, of this thesis.

Fig. 2.6 shows the comparison between the experimental data of a GaN-on-Si device [126] and a β-Ga_2O_3-on-β-Ga_2O_3 device [127]. In both cases, the generalized $R_{on,sp}$ (Eq. 2.12) anticipates the experimental trends better than BFOM and suggests that the devices may already be performing close to their intrinsic limits, further indicating that BFOM represents an overly optimistic metric for nontraditional WBG materials.

In practice, the rise of the junction temperature is limited by packaging and other considerations, suggesting an upper limit of power (P_{max}) and current (I_{max}) that can be sustained by a technology. We will discuss this limiting current performance in the next section.

2.2.2 Generalized I_{max}

Since the device mobility degrades with increasing temperature, the device junction temperature is required to be well below the maximum junction temperature ($T_{j,max}$) to maintain proper functionality. For a given θ_{th}, the maximum allowable power, P_{max} (P_{max}=$\Delta T_{max}/\theta_{th}$), can be used to determine the maximum allowable current, I_{max} (P_{max}=$I_{max}^2 \times R_{on}$).

Using some simple substitutions and using Eq. 2.12, we can write the maximum allowable current as:

$$\frac{I_{max}}{W} \propto \sqrt{\frac{\varepsilon \mu_n E_C \lambda_{sub} S \Delta T_{\max}}{\frac{\xi\left(T_{off}\right)}{\xi(T_{on})}\left(\frac{T_{on}}{300}\right)^{\gamma}}} \tag{2.13}$$

where W is the width of the device, λ_{sub} is the thermal conductivity of the substrate, and S is the shape factor [131], which is the technology, geometry, and material-dependent non-ideal factor. The generalization of I_{max} (Eq. 2.13) provides a limit that explicitly accounts for the first time, the effect of temperature-dependent mobility, shape factor, and incomplete ionization. As shown in Fig 2.7, the generalization of I_{max} can predict the current values in experiments [128]–[130].

2.2.3 Generalized P_{max}

The substrate- and self-heating -aware expressions obtained in the previous sections can now be used for obtaining the i-SOA of a power device. Since frequency dependence is an

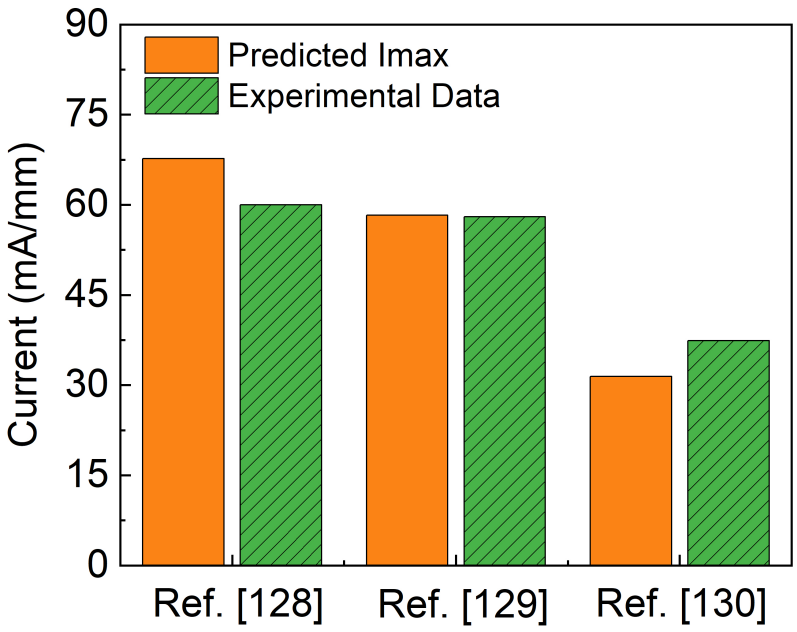


Figure 2.7. Comparison of maximum current predicted by Eq. 2.13 with that of experimental data from Refs. [128]–[130].

essential consideration for power transistors, the effect of transient thermal resistance (Z) needs to be considered. At T_{amb}= 300 K, by setting $T_{j,max}$= 450 K, P_{max} can be determined using the following relation:

$$P_{max} = \frac{T_{j,max} - T_{amb}}{\theta_{th} \times Z_m\left(t_{on}\right)} = I_D \times V_D \tag{2.14}$$

where $Z_m(t_{on})$<1, is the normalized transient thermal impedance, t_{on} is the pulse duration (t_{on}=D ζ, where ζ is the period, and D is the duty cycle). It is extremely important to calculate the transient thermal response of the chip accurately to determine the i-SOA. The junction temperature can be approximated by the superposition of the heating and cooling responses of the chip. For a train of repetitive pulses, the power pulses can be averaged,

and the temperature calculated at the end of nth or $(n+1)th$ pulse after the average power pulse. The expression is given by [74]:

$$Z_1 = D + (1 - D)Z_0(DT) \tag{2.15}$$

where D is the duty cycle, Z_0 is the transient thermal impedance measured experimentally. For a single pulse, $\mathrm{Z}_0\left(t_{on}\right) = 1 - \mathrm{e}^{-\frac{t_{on}}{\tau_{th}}}$, with $\tau_{th}(\equiv\theta_{th} \times C_{th})$ and T is the period. Another approach is to calculate the temperature at the end of the average power pulse (before steady-state conditions), where the average power is modified by a transient thermal resistance factor, given as [74]:

$$Z_2 = D + (1 - D)Z_0(D + 1)T + Z_0(DT) - Z_0T \tag{2.16}$$

While both Eqs. 2.15 and 2.16 provide a reasonable estimation of transient thermal response, they were derived using the superposition principle, since it defies a solution otherwise. Here, we will derive a closed-form analytical relation to obtain the transient thermal response of a packaged chip and compare it with those obtained using the superposition principle. We know from [104] that,

$$T^{pk}_{j,max} - T_{amb} = \Delta T^{pk}_L \tag{2.17}$$

and

$$P_{pk} = P_{max} \tag{2.18}$$

Also,

$$\Delta T^{pk}_L = P_{avg}\theta_{th} + H\left(P^{pk} - P_{avg}\right) = P^{pk}\theta_{th}\left[D + (1 - D)H_0\right] \tag{2.19}$$

Therefore, we can write:

$$Z = \frac{\Delta T^{pk}_L}{\theta_{th}P_{\max}} = \frac{\Delta T^{pk}_L}{\theta_{th}P^{pk}} = D + (1 - D)H_0 \tag{2.20}$$

where $H_0 = \left(1 - \mathrm{e}^{\left(-\frac{D\zeta}{\tau_{th}}\right)}\right)\left(\frac{1-\mathrm{e}^{\left(-\frac{(1-D)\zeta}{\tau_{th}}\right)}}{1-\mathrm{e}^{\left(-\frac{\zeta}{\tau_{th}}\right)}}\right) = CZ_0$. For a single-time-constant system, H_0 in [104] is exact, a correction term, C, is needed, i.e.,

$$C = \frac{H_0}{Z_0(t)} = \frac{1 - \mathrm{e}^{\left(-\frac{(1-D)\zeta}{\tau_{th}}\right)}}{1 - \mathrm{e}^{\left(-\frac{\zeta}{\tau_{th}}\right)}} \tag{2.21}$$

From [105], for a packaged device, if $\tau_{th,1} \gg \tau_{th,2} \gg ... \tau_{th,n}$, ΔT of successive stages can be added, so that $\Delta T(t) = \sum_i \Delta T_i \left(1 - \exp\left(-\frac{t}{\tau_{th,i}}\right)\right)$. Now dividing both sides with the dissipated power, P, we get:

$$\frac{\Delta T(t)}{P} = \sum_i \frac{\Delta T_i}{P} Z_{0,i}\left(t_{on}\right) \Rightarrow Z_0\left(t_{on}\right) = \sum_i \frac{\theta_{th,i}}{\theta_{th,tot}} Z_{0,i}\left(t_{on}\right) \tag{2.22}$$

where $Z_0\ \left(t_{on}\right)$ is the average of all individual stage $Z_{0,i}\ \left(t_{on}\right)$, and $\theta_{th,tot}$ is the summation of all θ_{th} of the packaged chip.

Therefore, a multi-stage transient thermal resistance (Eq. 2.22) including the correction factor $C(D, \zeta)$ (Eq. 2.21) and duty cycle D (Eq. 2.20) can be expressed as:

$$Z_m\left(t_{on}\right) = D + (1 - D) \sum_i \frac{\theta_{th,i}}{\theta_{th,tot}} C_i(D, \zeta) Z_{0,i}\left(t_{on}\right). \tag{2.23}$$

Eq. 2.23 is the first closed-form analytical expression for arbitrary complex package structure subjected to pulses of arbitrary duty cycle that considerably simplifies the calculation of i-SOA. Fig. 2.8 shows the derived analytical closed-form solution of transient thermal response, Z_m (Eq. 2.23) matches the responses predicted by Z_1 (Eq. 2.15) and Z_2 (Eq. 2.16) very well.

2.3 Calculating the *i*-SOA

In Eq. 2.23, index i stands for a certain stage of RC circuit ($i = 1$ is the chip itself), Z_0 is the transient thermal impedance for a single pulse expressed as $[1 - \mathrm{e}^{\frac{-t_{on}}{\tau_{th}}}]$, where τ_{th} can

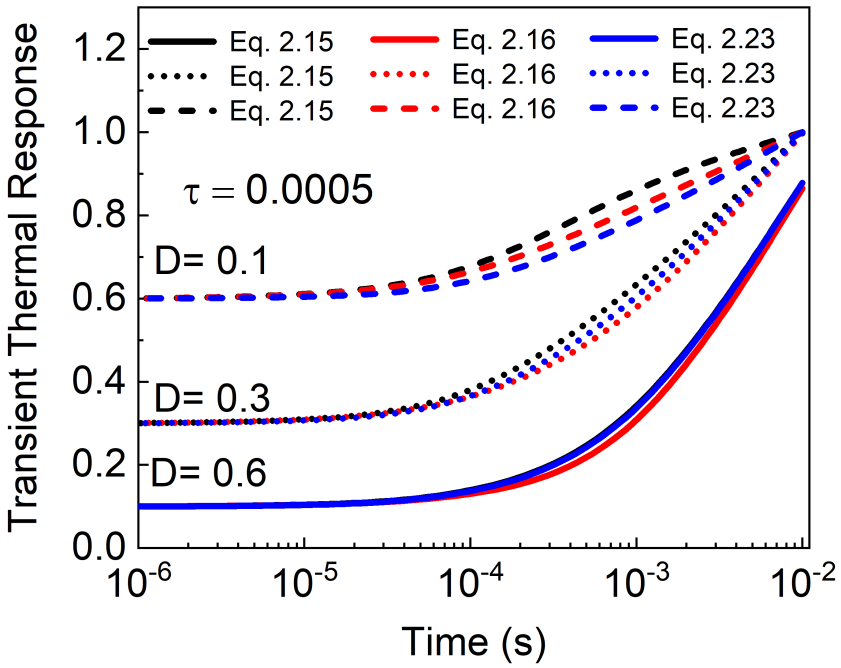


Figure 2.8. Comparison of expressions for transient thermal responses of a packaged chip derived using superposition principle (Z_1(Eq. 2.15) and Z_2(Eq. 2.16)) and the closed form analytical solution derived in this chapter (Z_m (Eq. 2.23). For the comparison, the thermal time constant, τ (τ_{th}) was taken as 0.0005, which is a typical value for microchips. Although the curves are obtained for three values of duty cycles ($D = 0.1$, 0.3 and 0.6), matching of Z_3 with Z_1 and Z_2 has been confirmed at other values of duty cycles and thermal time constants as well.

be calculated by the parameters given in Appendix A. Knowing $Z_m(t_{on})$, the current limit can be found from the following expression:

$$I_{\max} = \sqrt{\frac{T_{j,\max} - T_{amb}}{\theta_{th} Z_m\left(t_{on}\right) \times R_{on}}} \tag{2.24}$$

Using the derived equations (Eqs. 2.12, 2.14, 2.24), the i-SOA for different bulk WBG materials (Fig. 2.9) and bilayer structure (Fig. 2.10, β-Ga_2O_3 as an example) can be calculated analytically by assuming t_{on}=10 ms and D= 0.5 for a standalone device ($i = 1$).

Using the same procedure, the performance and i-SOA of other device systems (e.g., GaN-on-Si, GaN-on-SiC, etc.) can be easily evaluated. In Fig. 2.9 some of the materials (except

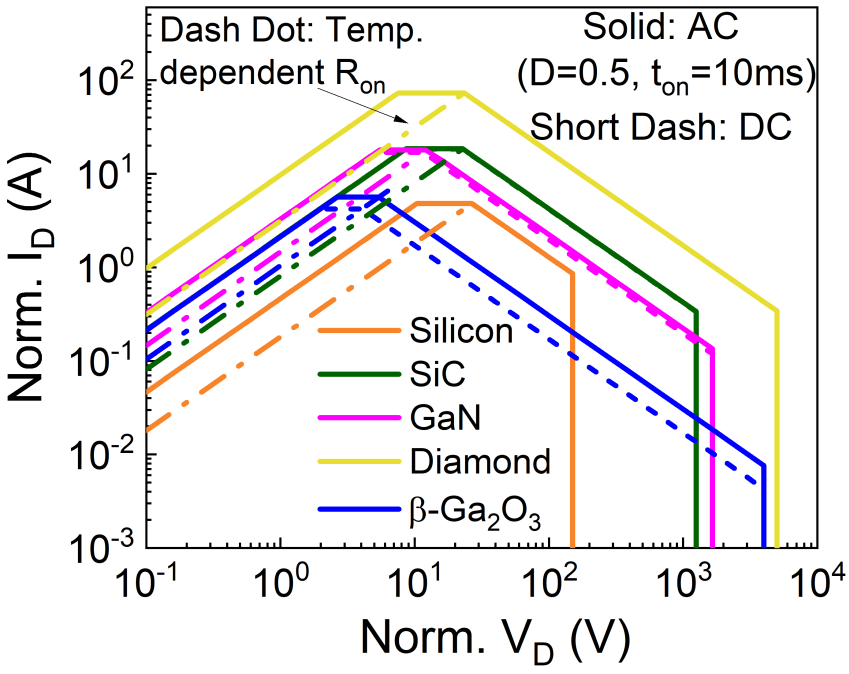


Figure 2.9. *i*-SOA predicted for various bulk WBG materials

GaN and β-Ga_2O_3) show a similar DC and AC response because of a low time constant. It is evident that device self-heating plays an important role in determining performance. Because of larger θ_{th}, β-Ga_2O_3 gains more *i*-SOA in AC operations, compared to DC condition. We reach similar conclusions for other WBG materials as well. In Fig. 2.10 materials with larger λ_{sub} have larger *i*-SOA, as expected. Thus, the *i*-SOA obtained here gives a holistic device-circuit-system perspective of WBG semiconductor performance.

2.4 Reliability-Aware *i*-SOA

Several previous works emphasize the importance of defining a reliability-aware generalization of the SOA [132], [133]. The reliability-aware SOA is defined in various ways, *viz.*, voltage-dependent HCD stress SOA [134], thermal SOA [135], catastrophic failure SOA [136], etc. Although achievable for extensively studied devices (such as silicon LDMOS), these SOAs are difficult to be determined for emerging WBG materials. Therefore, we propose a reliability-aware *i*-SOA that can be analytically obtained for a very well-researched

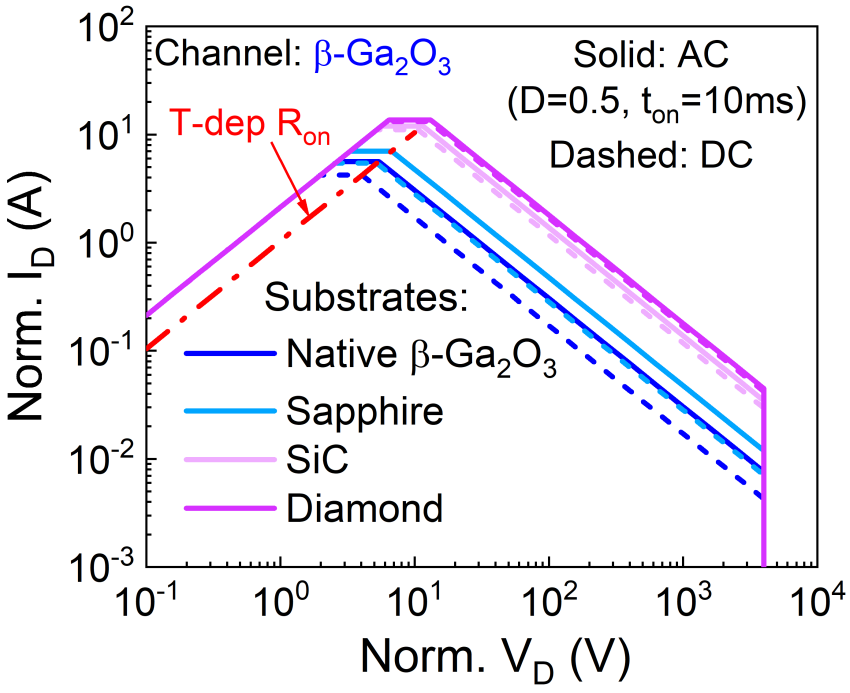


Figure 2.10. i-SOA predicted for bilayer substrates. β-Ga_2O_3 on various substrates (native β-Ga_2O_3, Sapphire, SiC, Diamond) are shown here as an example.

device like silicon LDMOS and state-of-the-art emerging WBG material-based devices like Diamond and β-Ga_2O_3.

We note that $R_{on,sp}$ degrades over stress time (t) as bulk and interface traps are generated during device operation. These traps scatter electrons and reduce mobility. The exact form of the mobility degradation depends on specific material; however, it can be simply expressed in the phenomenological Sun-Plummer form [137]:

$$\mu_n(T_{on}, t) = \frac{\mu_n(T_{on}, t = 0)}{1 + \alpha \Delta N_{it}(t)} \tag{2.25}$$

and time evolution of $\Delta N_{it}(t) \sim f(t/\tau)$ depends on the voltage- and temperature-dependent scaling factor, τ [2]. The precise functional form (e.g., power-law, exponential, sigmoid,

etc.) of N_{it} generation depends on the material of choice. The reliability factor appears as a multiplicative derating factor [138]–[140] in Eq. 2.12 for $R_{on,sp}$:

$$R^*_{on,sp}(T_{on},t) = R_{on,sp} \times T_f \times R_f(t) \tag{2.26}$$

$$T_f = \left[1 + \left(\frac{N_D \xi\left(T_{on}\right)}{N_{ref}}\right)^{\beta}\right] \left(\frac{T_{on}}{300}\right)^{\gamma} \frac{\xi\left(T_{off}\right)}{\xi\left(T_{on}\right)} \tag{2.27}$$

$$R_f(t) = (1 + \alpha \Delta N_{it}(t)) \tag{2.28}$$

The reliability of power transistors depends on various degradation mechanisms (e.g., HCD [107], BTI [141], the inverse piezoelectric effect [142], etc.) with temperature and voltage-dependent degradation rates. The localized generation of N_{it} in a multi-hotspot power transistor is phenomenologically written as [106], [143]:

$$\Delta N_{it} = \frac{At^n}{1 + Bt^n} \tag{2.29}$$

where the coefficients A and B may have positive or negative temperature coefficients and power-law or exponential voltage acceleration factors.

For an illustrative example, the role of trap-induced degradation is analyzed with TCAD simulations on silicon LDMOS (Fig. 2.11 (a)) [144]. The LDMOS has been electrically stressed to analyze the Hot Carrier Degradation (HCD), as shown in Fig 2.11(b). In Si transistors, it is well known that $\Delta N_{it}(t)$ reduces at higher temperature [140] (Figs. 2.11(c) and (d)) due to reduction of impact ionization rate due to increased phonon scattering. By including reliability aspects connected to $\Delta N_{it}(t)$ in the $R_{on,sp}$ expression, one can project device performance over the prolonged operation. This is shown in Fig. 2.11(e), where $R^*_{on,sp}(T_{on},t)$ for silicon LDMOS is calculated with $\Delta N_{it}(t)$ after certain stress time. As expected, $R^*_{on,sp}(T_{on},t)$ increases due to stress but, at the same time, self-heating reduces $\Delta N_{it}(t)$ (at a fixed stress time) in this case. This is shown by the dotted (solid) line that represents the impact of $\Delta N_{it}(t)$ on $R_{on,sp}(T_{on},t)$ without (with) thermal effects. The in-

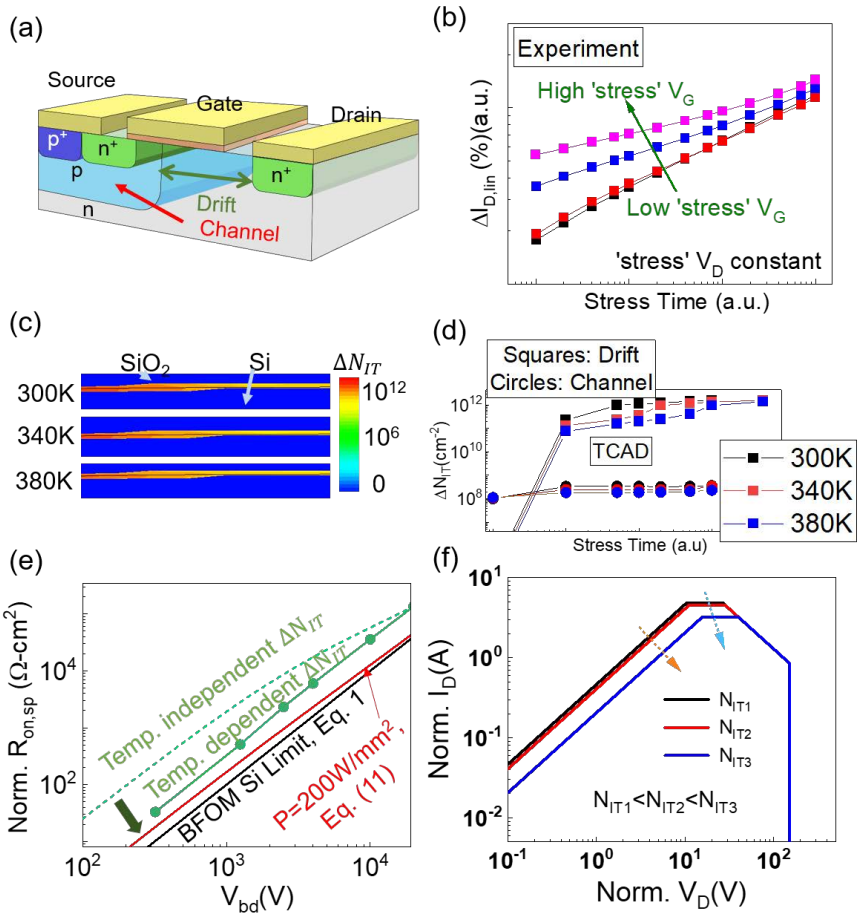


Figure 2.11. (a) Schematic of the Si LDMOS used in the study. (b) TCAD calibration of the temperature dependent HCD characteristics of the LDMOS. (c) The 2D plots showing the Si/SiO_2 interface and trap generation in the interface, in a Si LDMOS. (d) ΔN_{it} with increasing stress time at different temperatures. (e) Reliability-aware $R_{on,sp}$ or $R^*_{on,sp}$ predicted for silicon power devices (LDMOS) (f) Reliability-aware i-SOA predicted for LDMOS device at different interface trap concentrations.

creasing self-heating reduces HC-induced $\Delta N_{it}(t)$, with a small improvement in $R^*_{on,sp}(T_{on}, t)$. I_{max} accounts for $\Delta N_{it}(t)$ through $R_{on,sp}(T_{on}, t)$ and the newly calculated I_{max} can be used to obtain a Reliability-aware i-SOA (Fig. 2.11(f)). As the stress time increases, $N_{it}(t)$ increases, thus decreasing the mobility (captured using Eq. 2.17), leading to increased $R_{on,sp}$, decreased I_{max}, and closure of i-SOA. Following similar approaches, i-SOA can be obtained for other WBG semiconductors as well, provided their stress-dependent N_{it} is known either by TCAD simulations or experiments.

2.5 Summary

In this chapter, we have presented an analytical model (Eqs. 2.15, 2.16, 2.24) to calculate the i-SOA for modern power electronic devices that accounts for the self-heating effect and trap-induced degradation and compared the results with a broad range of experimental data published in the recent literature related to emerging WBG materials, such as β-Ga_2O_3. We have demonstrated that starting with the generalization of BFOM, we can get the device i-SOA by carefully considering the self-heating effects through substrate-aware θ_{th}, temperature-dependent mobility, incomplete ionization, and trap generation rate. To account for the substrate-aware SH, accurate modeling of θ_{th} is essential, which has been achieved using robust but straightforward θ_{th} formula (Appendix B). These generalizations allow calculating more realistic intrinsic device i-SOA, which was previously possible only through end-to-end modeling based on device-specific parameters and careful measurement of packaged devices. The key conclusions of this chapter are:

(a). The temperature- and reliability-aware i-SOA reveals that intrinsically Diamond is the best possible candidate at high temperature (here $T_{j,max}$= 450 K) among the WBG materials surveyed here. The i-SOA provides the new insight that Diamond would benefit from self-heating, and its performance would increase with increasing P, but only until all its dopants are fully ionized, after which the temperature-dependent mobility degradation dictates the performance limit.

(b). Similarly, from the perspective of i-SOA, GaN and SiC have comparable performance, with V_{bd} in the kV range. In practice, the material quality may further limit the empirical SOA for these materials.

(c). Moreover, with proper thermal management (high thermal conductivity substrates, cooling, etc.), i-SOA suggests that β-Ga_2O_3 FETs may be able to deliver performance comparable to GaN and SiC.

(d). In practice, nonideal effects, such as threading dislocations, interfacial thermal resistance, the choice of substrate, etc. may make the extrinsic SOA somewhat (or substantially) different.

One major factor, which is missing in our *i*-SOA is the cost of the devices. Historically, the cost has been the primary driver of the semiconductor market, and it will indisputably have a tremendous impact on the choice of wide bandgap semiconductors for power electronics in the near future. For example, in a SiC power device, 60% of the cost is that of the wafer itself. This is in sharp contrast to Silicon power devices, where the wafer cost has been less than 20% of the whole device since the early 1980s [97]. Thus along with performance and reliability, the price of the wafer will play a significant role.

Table 2.1. Average cost of wafers.This data is replotted from [145] and [146]

Material	**Available Wafer Size**	**Av. Cost (Euro/cm^2)**
Bulk GaN	2", 3"	100
SiC	4", 6"	10
Sapphire	upto 8"	1
β-Ga_2O_3	upto 4"	1
Silicon	Any	0.1

As seen from table 2.1, β-Ga_2O_3 has an incredible advantage in this aspect, compared to GaN or SiC. The development of melt-growth methods of β-Ga_2O_3 (Czochralski(CZ) [147]–[149], edge-defined film-fed growth (EFG) [150], floating zone (FZ) [151]–[153], and vertical Bridgman (VBN) [154]) , have shown enormous potential in this facet, compared to SiC and GaN. The growth of single crystal, high-quality and large-size wafers, which is in line with the production technologies of Silicon and Sapphire, has been successfully achieved and continuously improved [155]. The doping of wafers has shown tremendous controllability. In addition, there has been significant progress made in thin-film growth techniques, such as MOCVD, MBE. CVD, etc. This is very important because epitaxial β-Ga_2O_3 has been extensively used for high-performance MOSFET and diodes. At the current pace, substantial progress in the wafer growth, and fabrication techniques, will be made in the near future, and the cost of β-Ga_2O_3 devices will come down substantially. In the past few years, there has also been significant progress made in thermal management, which substantially improved the performance of β-Ga_2O_3 devices. There is an excellent possibility that such advantages may outweigh the disadvantages of β-Ga_2O_3. To consider cost appropriately along with

i-SOA, we can introduce a metric such as *i*-SOA per unit price, which will be updated regularly, as the technology matures.

Regardless, based on application-specific requirements on power dissipation and reliability, the *i*-SOA provides a unifying conceptual framework to assess the early-stage experimental data and to define the accurate merits and fundamental bottlenecks of emerging WBG technologies for specific power electronics applications long before the devices are ready to be packaged and tested.

3. ELECTRO-THERMAL PERFORMANCE LIMIT OF β-Ga_2O_3 FIELD EFFECT TRANSISTORS

3.1 Introduction

β-Ga_2O_3 is often mentioned as the low-cost and high-performance next-generation channel material for power transistors. This is because of its wide bandgap (∼4.5 eV), which leads to an impressive breakdown voltage (∼9 MV/cm), and the large-scale availability of native substrates. In the previous chapter, we have analytically demonstrated that despite the advantages, the self-heating limits the performance of the β-Ga_2O_3 field effect transistors (FETs). In this chapter[1], we will take a detailed look into β-Ga_2O_3 transistors and holistically evaluate the performance from a device-circuit-system perspective using experiments and simulation, to test the predictions of i-SOA, while suggesting approaches to improve it.

In the early 2010s, β-Ga_2O_3 received a tremendous attention from the power electronics community because it outperforms a GaN FET in Baliga's figure of merit (FOM) [41] by 400% and Huang's chip area manufacturing FOM [96] by 330%. A plot showing the characteristics of β-Ga_2O_3 and other materials for power electronics is shown in Fig. 3.1. The impressive experimental demonstrations include: a kV-class Schottky barrier diode [53], D-mode FETs with high breakdown [52], etc. It also has the potential for low power loss during high frequency switching in the GHz regime [101].

However, there is a persistent concern that the self-heating associated with the low-thermal conductivity β-Ga_2O_3 (=10–25 W/mK) [54], as shown in Fig. 3.1, may compromise its electrical performance and prevent its widespread adoption. In fact, β-Ga_2O_3 is far inferior to GaN in terms of electrothermal metrics: by 900% in terms of Keyes figure of merit [94] and by 2300% in terms of Huang's thermal FOM [96]. This challenge of self-heating is well known, and one of the solutions includes using substrates with high thermal conductivity [e.g., sapphire [16], diamond [124], and silicon carbide (SiC) [157]] to reduce self-heating and improve on-current. An integrated device-circuit-package simulation is therefore necessary to see if this strategy would actually help β-Ga_2O_3 achieve performance comparable to GaN and SiC. Device-circuit-package models provide a critical interface between the performance

[1]↑Most of the content of this chapter is based on Ref. [100], [101], and [156]

of the device and the ultimate system performance, which will be discussed in the next section.

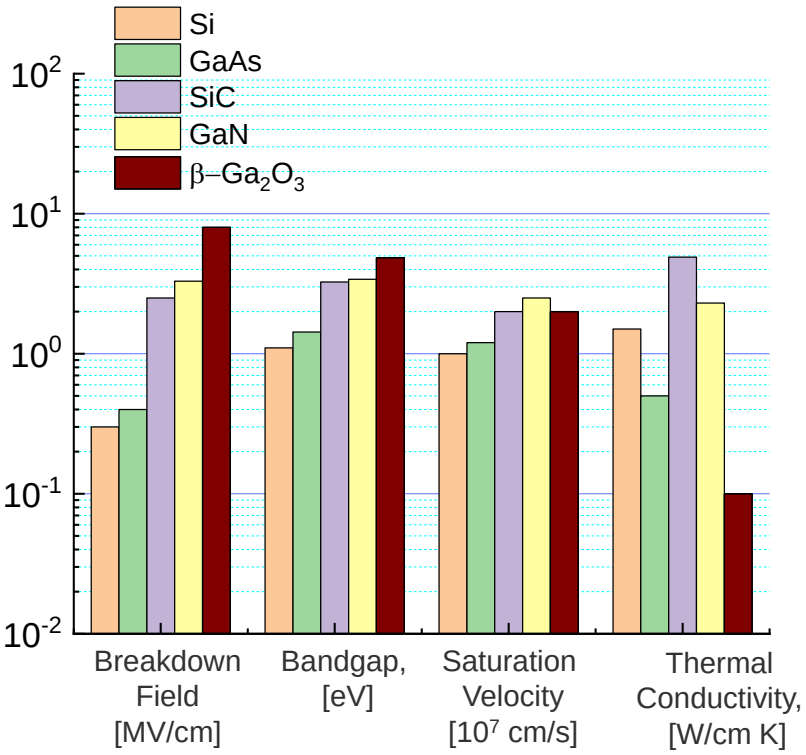


Figure 3.1. Properties of wide bandgap semiconductors used in power electronics

3.2 Electrothermal Modeling

Experimentally calibrated, self-consistent device and circuit simulations by technology computer-aided design (TCAD) and HSPICE models allow one to predict system performances under a variety of operating conditions accurately, identify performance bottlenecks, and suggest routes to application-specific optimization. However, it has been a challenge to model β-Ga_2O_3 FETs accurately. Existing TCAD models [158] calculate $I_D - V_G$ characteristics with effective parameters, but the failure to include SHE makes the model ineffective in predicting FET response on substrates with various thermal conductivity, λ. A recent model does account for SHE and predicts channel thickness-dependent, thermal resistance θ_{th}; however, it has not been calibrated extensively with experimental data [159]. Most

importantly, neither type of model predict device-circuit-package implications of a device design. We will start with device modeling (TCAD), then proceed to circuit simulations (HSPICE), and then evaluate the package performance (COMSOL).

3.2.1 Device Modeling (TCAD)

In this chapter, we develop a self-consistent TCAD model calibrated with experimental data which can predict the output and transfer characteristics of β-Ga_2O_3 FETs, including self-heating effects. We have developed the TCAD model using the commercial device simulator Sentaurus from Synopsis [160].

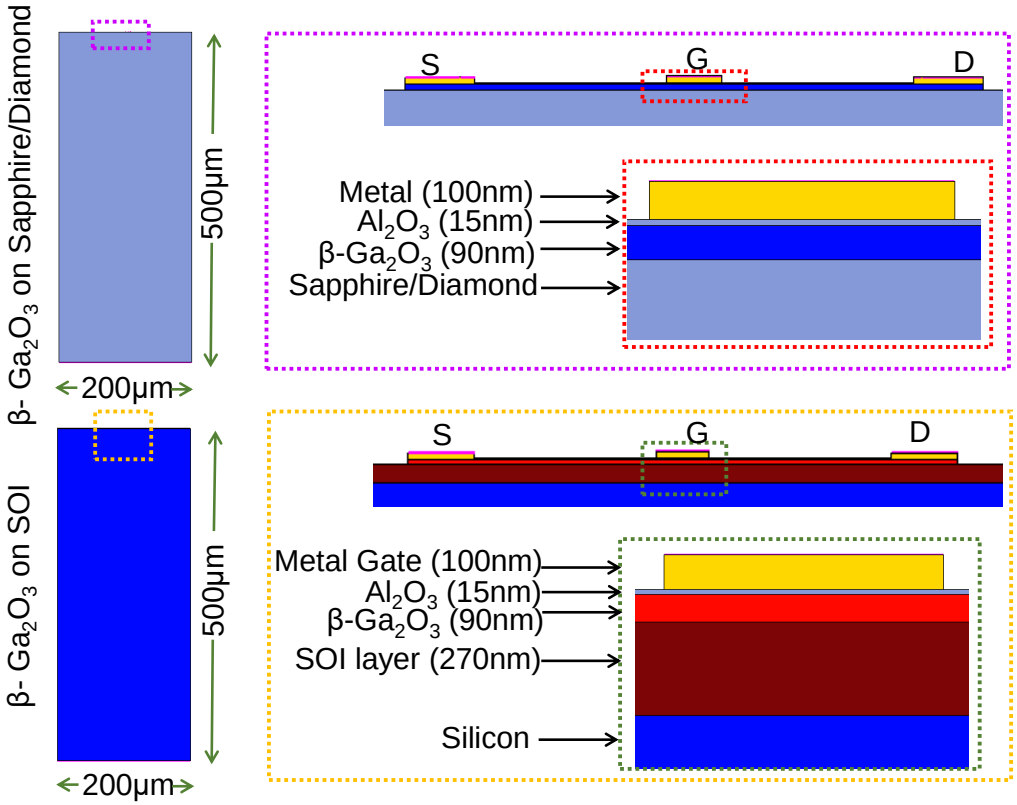


Figure 3.2. Device structures in Synopsis TCAD Simulator. The dimensions of the device are taken from fabricated devices in Refs. [16] and [124]. The substrate was considered to be n-doped with concentration of $2.7 \times 10^{18}/\text{cm}^3$. The electron mobilities were determined by fitting and it was found to be 49, 36 and 23 cm^2/V-s in case of Diamond, Sapphire and SOI substrates respectively.

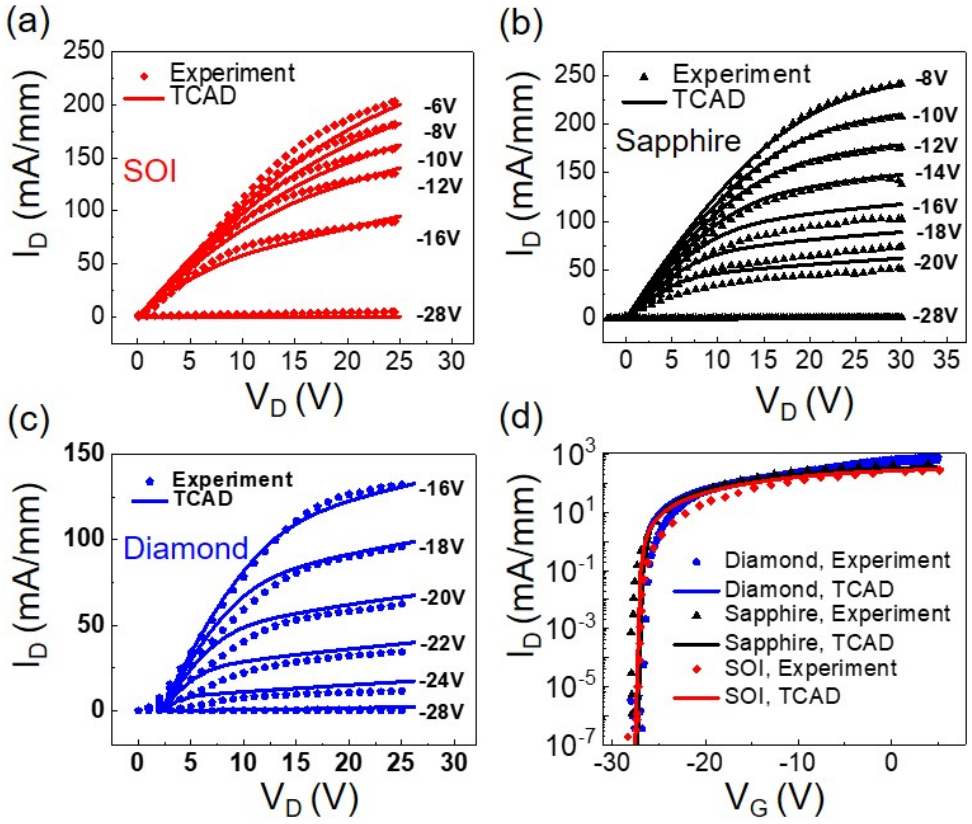


Figure 3.3. Output characteristics obtained from experiments [16], [124], and TCAD and for (a) SOI (b) Sapphire (c) Diamond. (d) Transfer characteristics of β-Ga_2O_3 FETs on the three substrates and TCAD outputs. The TCAD model reproduces the experimental data accurately.

This electro-thermal simulator self-consistently solves for position-resolved electron and hole concentrations and the lattice temperature. For electrical simulation, a key challenge is the temperature dependence of mobility associated with the complex band structure of β-Ga_2O_3. Note that the $Ga-O$ bond is strongly ionic, which gives rise to strong Frölich interaction and low optical phonon energies [161]. This specific mobility model does not exist in classical device simulators, but we adopted the analytical power-law mobility model with empirical fitting parameters to approximate the mobility between 300 and 500 K [39]. Other device parameters (e.g. doping density : $2.7 \times 10^{18}/\text{cm}^3$) are summarized in the caption of Fig. 3.2. Thermal modeling of a power transistor poses additional challenges.

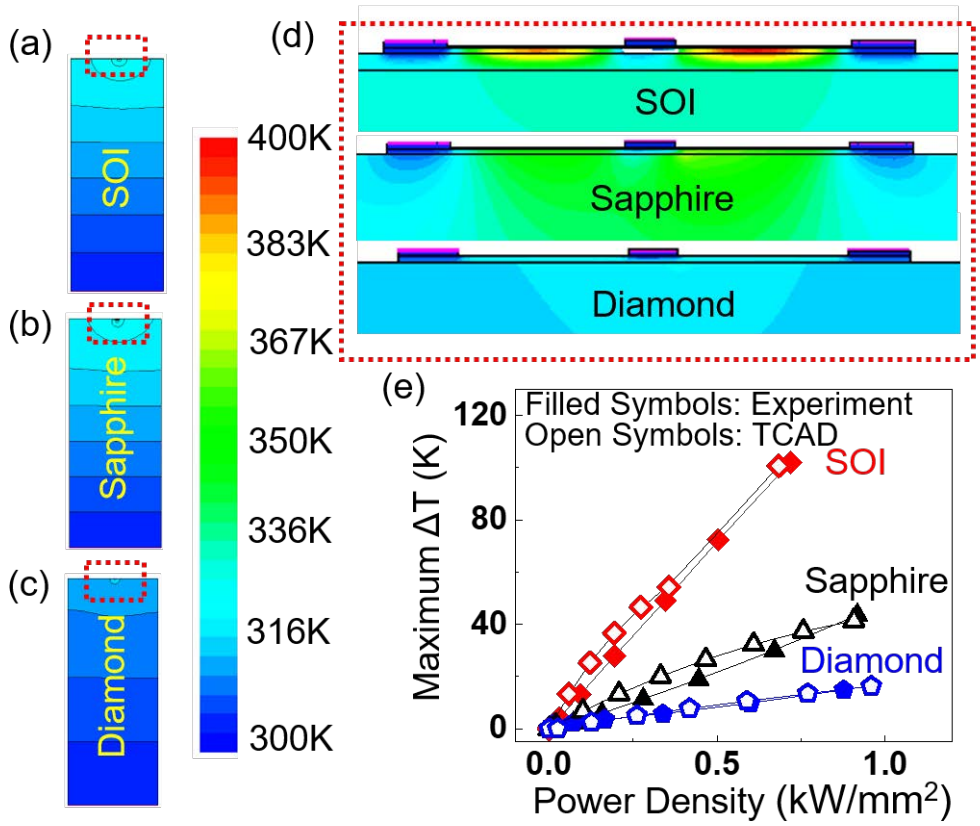


Figure 3.4. Output characteristics obtained from experiments [16], [124], and TCAD and for (a) SOI (b) Sapphire (c) Diamond. (d) Transfer characteristics of β-Ga_2O_3 FETs on the three substrates and TCAD outputs. The TCAD model reproduces the experimental data accurately.

While electrical transport is confined to the thin β-Ga_2O_3 layer, the self-heating of the channel is defined by the λ and the dimensions of both the channel and the substrate. To calibrate against experimental data [16] and [124], we considered that the β-Ga_2O_3 device rests on a substrate 500 μm thick and 200 μm wide (increasing the width further does not affect the results). Fig. 3.2 shows the multi-layer device stack necessary for the accurate thermal modeling of the transistors, with layer thicknesses varying from few nanometers to hundreds of micrometers. The source, gate, drain, and substrate contacts act as heat sinks.

The coupled electro-thermal model was used to calculate this depletion-mode transistor's output and transfer characteristics. The results were validated against experimental data from β-Ga_2O_3 FETs with three different substrates (Diamond, Sapphire, and Silicon on Insu-

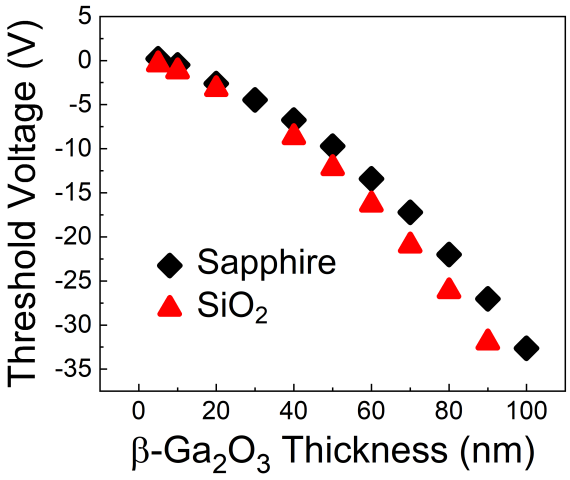


Figure 3.5. The threshold voltage dependence on channel thickness. The standard D-mode FETs must be pinched-off to be turned off, therefore thinner epitaxial layer is required to fully deplete the channel at 0 V.

lator (SOI)), as shown Fig. 3.3. The multiple-substrate validation ensures that the thermal model and the electron-hole transport models are independently calibrated. The deviation between experimental data and the model prediction in the linear region is explained by the fact that the idealized device considered in the simulation does not account for the series resistance. Indeed, contact engineering to reduce specific on-resistance remains an important research topic for β-Ga_2O_3 transistors [162]. In the context of this chapter, the maximum self-heating is defined by the saturation characteristics, which is well described by device simulation.

For additional and independent validation of the thermal model, we compared the junction temperature predicted by the TCAD model to the position-resolved surface temperature from the thermoreflectance (TR) measurement. The comparison is meaningful because most of the heat generation within the FET occurs in the thin channel lying very close to the surface. Fig. 3.4 shows that the junction temperature rise (ΔT), when plotted with power (P=V_{DS} $\times$ I_D) normalized by area, replicates the experimental data accurately. The temperature profiles (V_{GS} = -8 V,V_{DS} = 30 V) of the β-Ga_2O_3 FETs on three substrates show the dramatic position-resolved temperature rise when the transistor operates with a low λ substrate, SOI. The temperatures recorded using TR measurement are slightly lower than

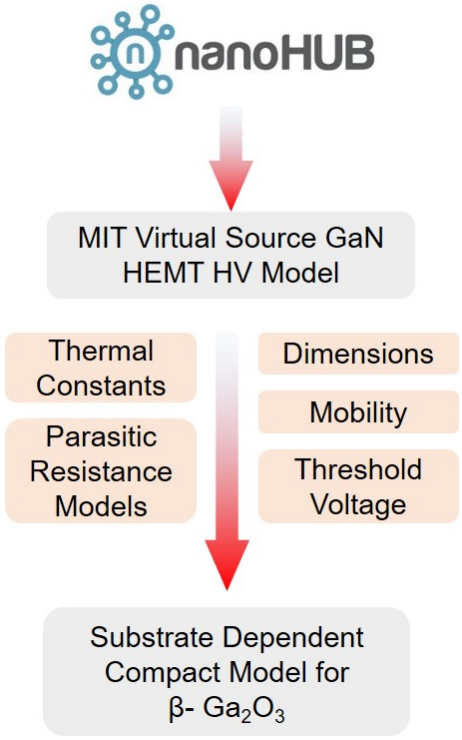
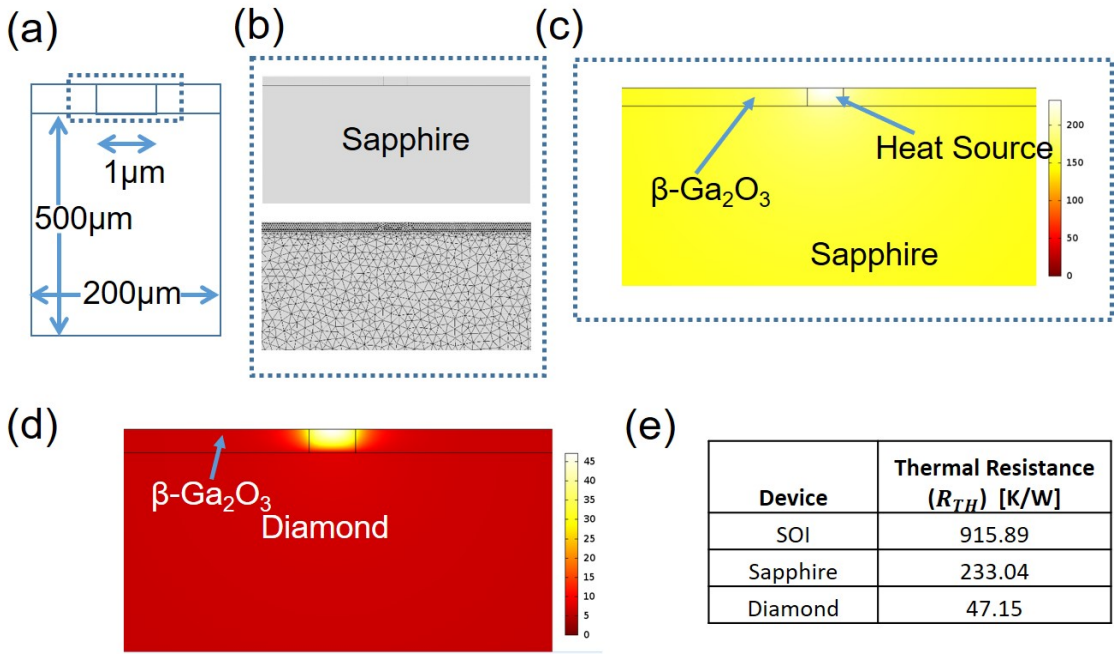


Figure 3.6. A flow chart for the construction of the β-Ga_2O_3 compact model for circuit simulation.

those of TCAD simulation, possibly because we did not account for the convective loss from the surface of the transistor.

Since this calibration device is a D-mode FET, significant negative voltage ($\sim$ -28 V) must be applied to turn the transistor off. D-mode FETs are undesirable because they require a complex gate drive circuit for fail-safe operation [158]. Fortunately, the threshold voltage can be tuned by varying β-Ga_2O_3 thickness, as shown in Fig. 3.5. A sub-20 nm film may be necessary to create a traditional E-mode transistor.

Given the well-calibrated 3D electro-thermal TCAD model for β-Ga_2O_3 transistors, we now need to determine the performance of various circuits based on this transistor technology. Towards the goal of quantifying the efficiency loss due to self-heating, we will first need to develop a compact electro-thermal model which is discussed next.



Device	Thermal Resistance (R_{TH}) [K/W]
SOI	915.89
Sapphire	233.04
Diamond	47.15

Figure 3.7. (a) Simulation structure in COMSOL (not to scale). (b) A magnified image of the device and meshing. The temperature (thermal resistance) plots obtained for (c) Sapphire (d) Diamond. The peak values are tabulated in (e).

3.2.2 Circuit Simulations (HSPICE)

A β-Ga_2O_3 compact model was developed by adapting and generalizing the MIT Virtual Source GaNFET-HV SPICE Model [102] for the relevant device physics, parameters, and dimensions. The mobility values obtained from TCAD was used for the corresponding device structures. In particular, unlike classical transistors, the compact model includes two self-consistent sub-circuits for electrical and thermal responses. A flow chart representing this is shown in Fig. 3.6.

We evaluated the thermal resistance for β-Ga_2O_3 in all three substrates, *viz.* Diamond, Sapphire and SOI, by solving the Fourier equation for heat-conduction by using the COMSOL Multiphysics software. For COMSOL simulation, the β-Ga_2O_3 channel has a width of 8 μm, and most of the power dissipation occurs close to the drain (i.e., the heat source is approximately 1 μm). For silicon-on-insulator structure, a 270 nm thick oxide is sandwiched

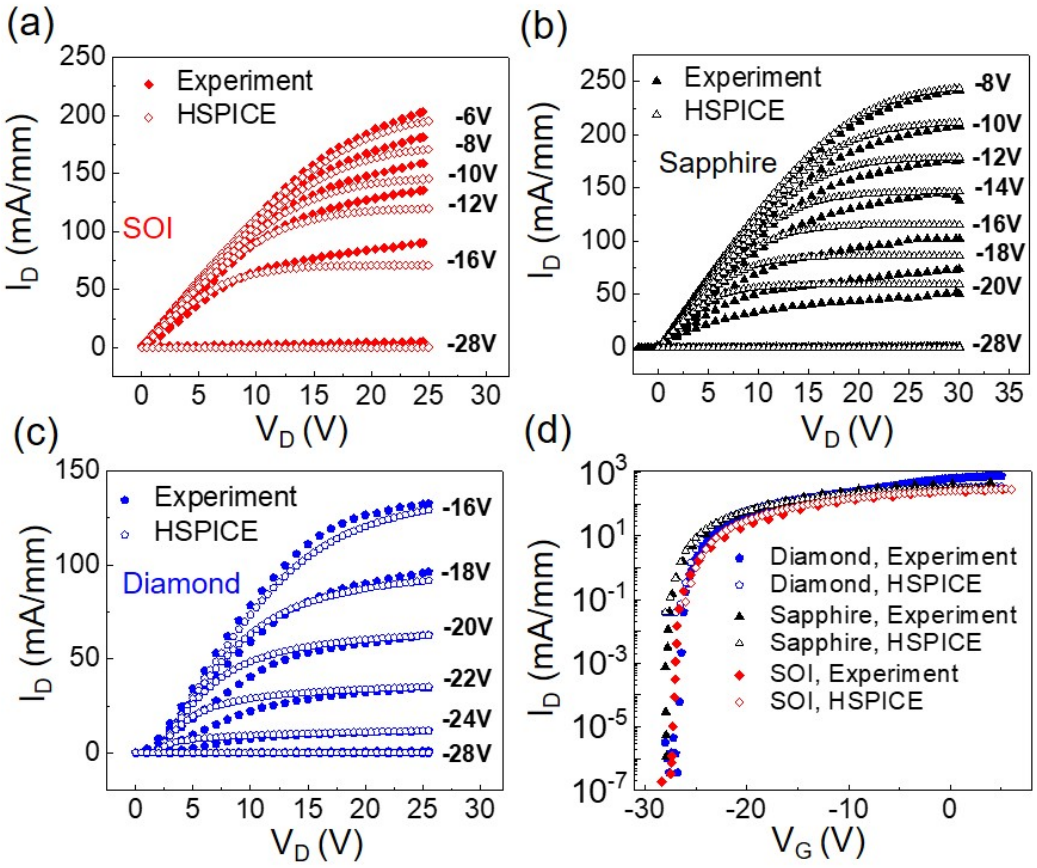


Figure 3.8. Output characteristics obtained from experiments,[16], [124], and HSPICE compact model for (a) SOI (b) Sapphire (c) Diamond. (d) Transfer characteristics of β-Ga_2O_3 FETs on the three substrates and TCAD outputs. The TCAD model reproduces the experimental data accurately.).

between the β-Ga_2O_3 and the silicon layers. These film thicknesses are typical of commercial substrates used in the experiments.

The thermal resistance is obtained with the following boundary conditions: The bottom surface is set to ΔT= 0 K (heat sink) and all other sides are thermally insulated. The structure is assumed to be ideal with no interfacial thermal boundary resistances. The use of a zero-flux condition at the top surface is a reasonable approximation because the convection heat flux is negligible. With $P = 1\ W$ at the heat source, we solve the Fourier Equation for heat transfer ($q = \lambda \times \Delta T$) to find the temperature at the heat source, T_m, and to calculate $\theta_{th} = P(T_m - 0) = T_m$ (since $P = 1\ W$). The simulation results are shown in Fig.

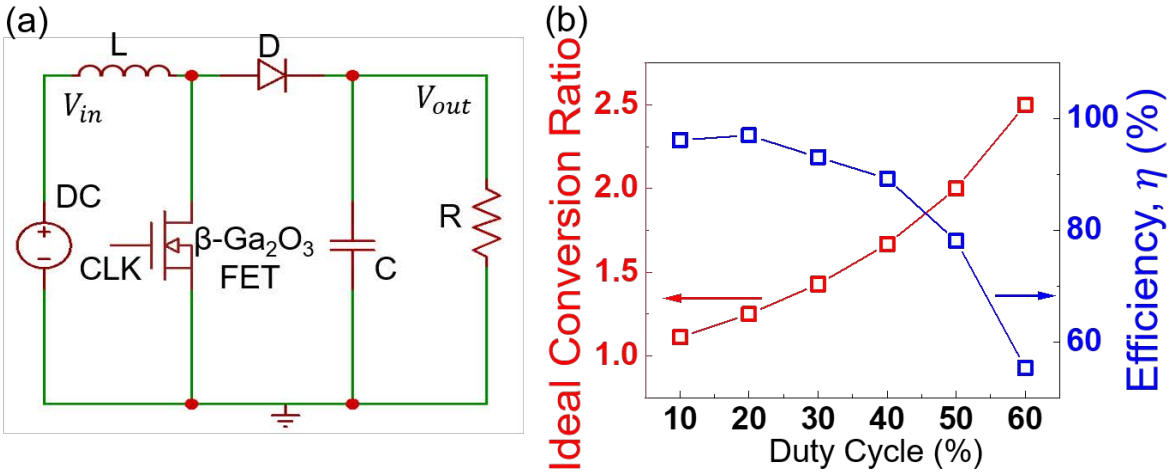


Figure 3.9. The boost converter circuit used in our analysis. Circuit parameters: Inductor, L = 3000 μH, FET= β-Ga_2O_3 on SOI/Sapphire/Diamond, Capacitance, C= 50 μF, D = Diode, Load resistance, R= 2000 Ω, V_{in} = Input Voltage, V_{out} = Output Voltage. For the diode, SBR3U100LP with forward voltage drop, V_F = 0.79 V and total capacitance, C_T = 800 pF, has been used. (b) Ideal conversion ratio and efficiency vs. duty cycle of the boost converter circuit.

3.7. The thermal capacitance was obtained from device dimensions and further refined with experimental transfer and output characteristics during calibration. The compact model reproduces the experimental data well, as seen from Fig. 3.8. This well-calibrated electro-thermal HSPICE compact model can now be used to analyze the circuit performance of β-Ga_2O_3 FETs.

To quantify the implications of self-heating associated with a β-Ga_2O_3 technology, we chose to analyze the performance of a boost converter circuit, see Fig. 3.9. The boost converter circuit is widely used as a DC/DC converter in power electronic systems, and finds applications in sensors, portable speakers, USB chargers, etc. It is important to realize that the FET dimensions necessary for use in the boost converter circuit are much larger than the devices used for model calibration. Therefore, the thermal parameters (θ_{th} ,C_{th}) of the new device geometry was recalculated from the COMSOL simulator. Finally, we used a FET with threshold voltage, V_{th} = -4 V, (corresponding to β-Ga_2O_3 layer thickness of 20 nm [101]) for all the simulations. We do realize that in practice enhancement-mode FETs

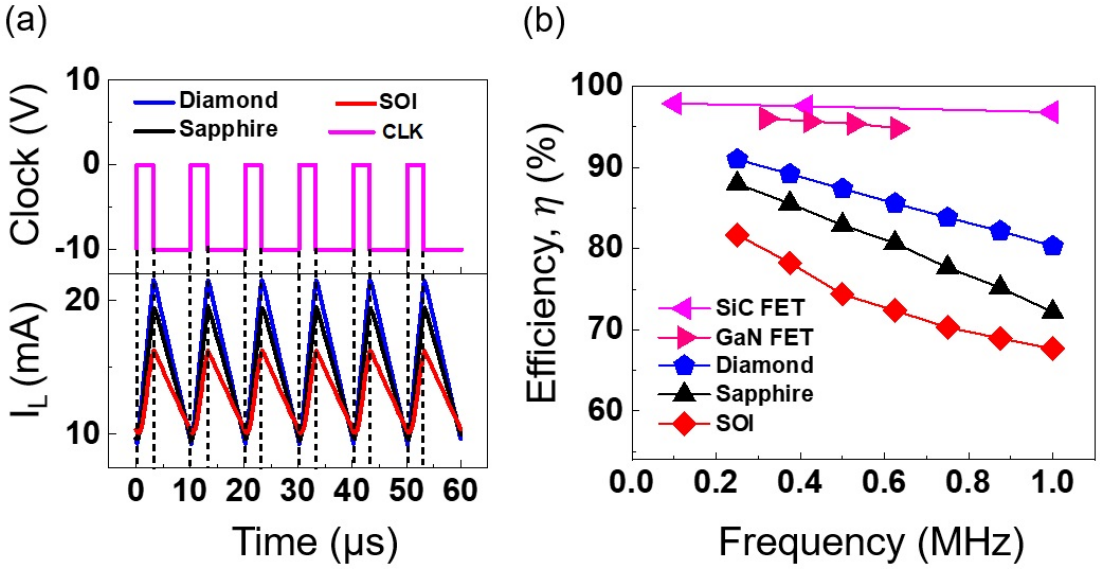
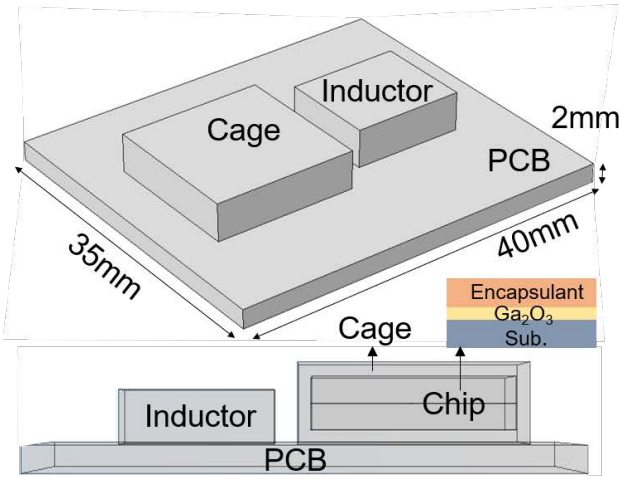


Figure 3.10. (a) Inductor current (I_L) of the boost converter circuit. The clock input is with 30% duty cycle and the driving voltage is from 0 to -10 V. (b) Efficiency of the circuit with a SiC FET [163], GaN FET [164], β-Ga_2O_3 FET on Diamond (500 μm) , Sapphire (500 μm), and SOI (270nm/500 μm). The mobility in case of β-Ga_2O_3 FET on hBN (50nm)/ Si (100 μm) is assumed to be three times to that of β-Ga_2O_3 FET on Diamond (500 μm) to account for improved heat conduction..

are preferred because depletion mode FETs with negative threshold voltage (V_{th}) require a complex gate drive circuit for fail-safe operation [158]. Developing the existing technology further to support enhancement mode operation with sufficient drive current will be an important topic of research.

For a fair comparison of performances among the β-Ga_2O_3 FET on three substrates, we need to determine the best possible operating conditions for the boost converter. Since the β-Ga_2O_3 FET needs to be turned off and on periodically, we chose our driving clock to have a lower limit of -10 V and the higher limit of 0 V, keeping the chosen V_{th} well within the operating voltage limits and giving the FETs a reasonably good operating range. To determine the duty cycle for the operations, we investigate the conversion ratio (V_{out}/V_{in}) and efficiency ($\eta = P_{out}/P_{in}$) subjected to various duty cycles (%). In order to have both high enough efficiency and conversion ratio, a duty cycle of 30% was chosen for all the simulations. Other circuit parameters are summarized in the caption of Fig. 3.9.



	κ (W/K-m)		κ (W/K-m)
Sapphire	40	Ga_2O_3	10
Silicon	80	h-BN	400
Encapsulant	1	Inductor	100
PCB	0.5	Cage	385

Top	cage	Convection ($h = 500$)
	No cage	Convection ($h = 5$)
Side		Insulated
Bottom		Fixed temperature (300K)

Figure 3.11. (a) System level simulation schematic of β-Ga_2O_3 FET on various substrates. 'Cage' refers a 'thermal Faraday Cage' which allows heat flux shielding. (b) The table summarizes the material properties, and boundary conditions for FEM simulations.

The efficiency of the boost converter is influenced directly by the output current, which is in turn determined by the degree of self-heating in the device. From Fig 3.10(b), we find that the β-Ga_2O_3 FET on SOI has an efficiency of 81.6% at 250 kHz, which decreases rapidly at higher frequencies. The SOI substrate has very severe heating, which results in lower inductor current (I_L) as shown Fig. 3.10 (a), and eventually very low efficiency. The FETs on Sapphire and Diamond have lower self-heating and, therefore, higher efficiency (89% and 91% respectively at 250 kHz) but cannot match the efficiencies of a GaN FET [164] or a SiC FET [163] (>95%) boost converters. Therefore, although theoretically β-Ga_2O_3 have low parasitic capacitances for the same on-resistance and a much lower switching loss compared to a SiC or a GaN FET, β-Ga_2O_3 FETs suffers from severe self-heating which makes the technology inferior to its competitors even though expensive bulk substrates (e.g. Sapphire [[16]], Diamond [124], etc.) are used. To determine the overall system efficiency of power transistors, one must account for SHE in packaging modules to get system-level reliability, which is discussed next.

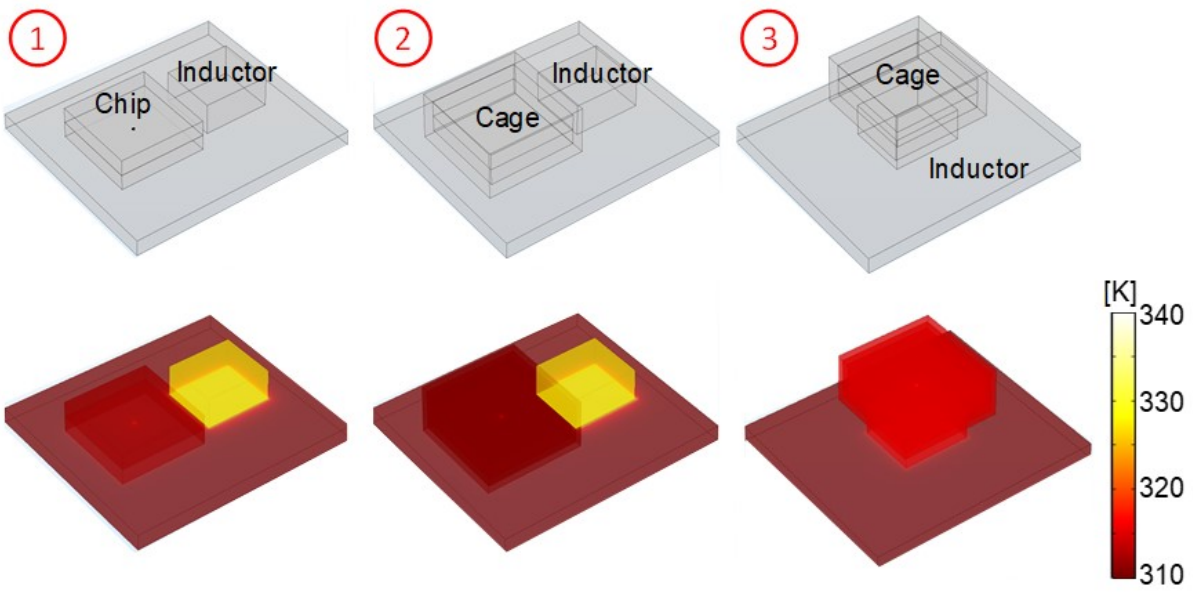


Figure 3.12. Temperature distribution comparison among different packaging configuration. Inductor temperature of vertical stack shows a considerable reduction in mutual heating effect through the use of a thermal Faraday cage.

3.2.3 Package Simulations (COMSOL)

The θ_{th} of a packaged device (including encapsulant, PCB, etc.) must be derived from the COMSOL FEM analysis (see Fig. 3.11). For the simulation, we assumed that the mode of heat transfer from the device or other components to the ambient is by convection [2]. We assumed there is no heat sink on top of the inductor ($h = 5$). The Faraday Cage is made up to a highly thermally conductive material copper, and that there is a heat sink on top of the cage ($h = 500$).

The bottom of the chip (PCB, encapsulant, FET, inductor, and other electronic components) is set at 300 K. We assumed two configurations where the cage is on top of the chip and without and another configuration where the chip with cage is on top of the inductor. We compare a classical side-by-side inductor-transistor packaging with the novel thermal "Faraday-cage" packaging (Fig. 3.12) to reduce inductor-IC mutual heating. In the classical configuration, Faraday caging does not reduce the temperature significantly. However, Faraday caging reduces inductor temperature, T_{ind}, significantly in the reduced-footprint,

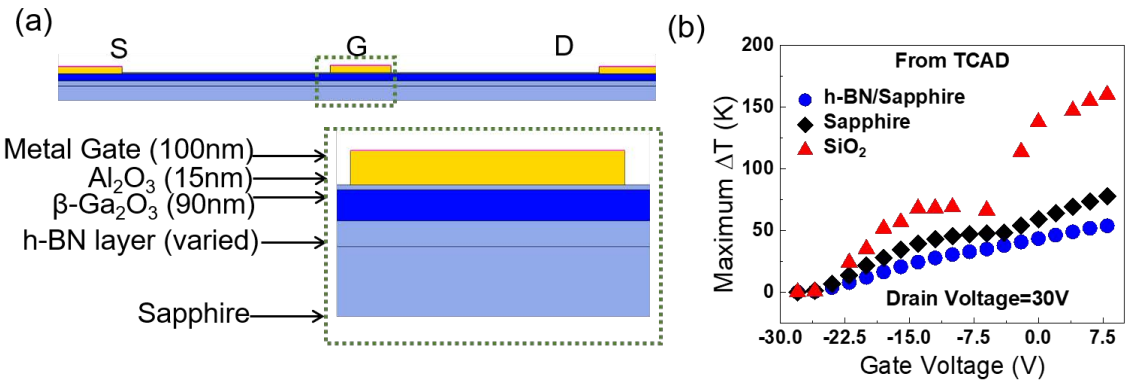


Figure 3.13. (a) Proposed h-BN based FET. (b) Maximum ΔT rise for h-BN/Sapphire is almost half as that of Sapphire, and almost $1/6^{\text{th}}$ of that of SiO_2 (V_{DS} =30V) .

stacked inductor-transistor configuration. The 3rd configuration was determined to be best among the three in terms of area and heat dissipated and therefore could serve as a solution to packaging issues of power electronics operating at very high voltage and temperature conditions. However, the intrinsic issue of high device self-heating remains.

3.3 Approaches to Improve the Performance

The simulations confirm that self-heating limits the β-Ga_2O_3 FET efficiency; hence approaches such as thermal shunts are needed for improved performance. We introduce a hexagonal boron nitride (h-BN) based thermal shunt for β-Ga_2O_3 transistor. h-BN is an emerging WBG material ($E_g \sim 6$ eV) with sp^2 hybridized Boron and Nitrogen atoms arranged in graphite-like layers. It has very high λ (bulk: 400 W/mK [165]) and has been previously used as dielectric layers [166] in electronics. h-BN growth on a Sapphire substrate has already been achieved [167] and can be an excellent choice for β-Ga_2O_3 FETs. In this section, we will evaluate the performance of the hBN-β-Ga_2O_3 transistor, the boost converter circuit with a hBN-β-Ga_2O_3 transistor as a switch, and the faraday cage.

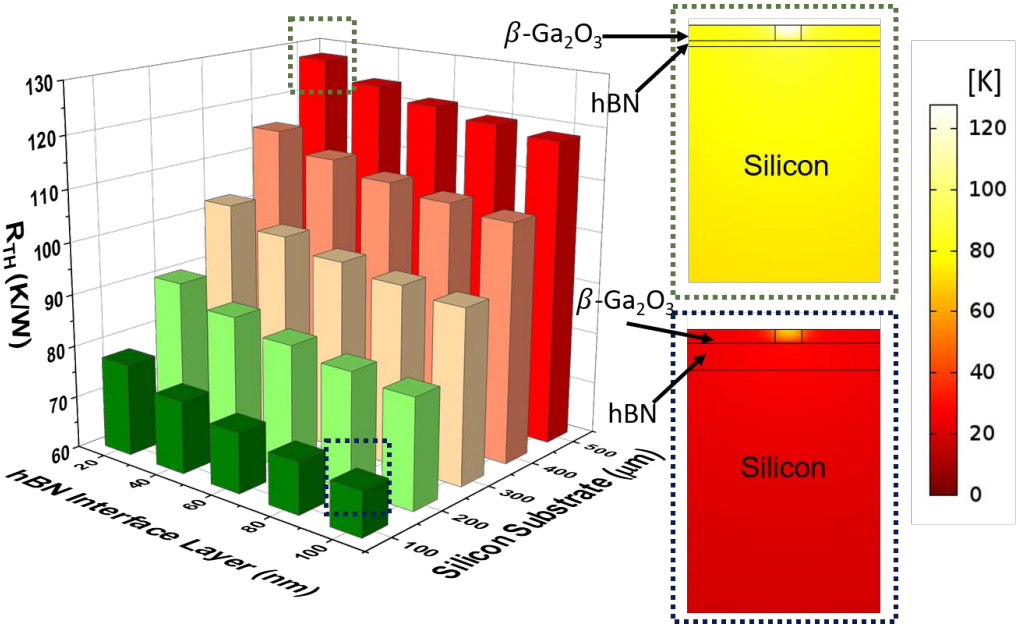


Figure 3.14. A β-Ga_2O_3/hBN/Si FET with various substrate (Silicon) thickness and interface layer (hBN) thickness. The plots on the right shows the temperature profile of FET at the respective Silicon and hBN layer thickness.

3.3.1 Device Modeling (TCAD)

Fig. 3.13 (a) shows the schematic of the proposed hBN/Sapphire FET. Fig. 3.13 (b) show that the ΔT (and corresponding θ_{th}) decreases considerably for the proposed transistor. This is because the heat generated in the β-Ga_2O_3 transistor, can now be dissipated through the hBN. A thicker shunt allows more efficient heat removal.

One of the advantages of using hBN as a thermal shunt is that Silicon can be used instead of Sapphire. The band offset provided by hBN (High electron barrier, ΔE_c=1.7 - 2 eV, calculated using electron affinity (χ) of β-Ga_2O_3 $\sim$ 4 eV [168], hBN = 2 - 2.3 eV [169], and the bandgap of β-Ga_2O_3 $\sim$ 4.5 eV [170] and hBN $\sim$ 6 eV [171]) is large enough to prevent current 'spill-off' and facilitates the usage of Silicon as the substrate. This approach will significantly reduce the cost of the process as Silicon is much cheaper than SOI, Sapphire or Diamond. Moreover, the fabrication technology of Silicon is very mature, and therefore, additional wafer processing/engineer can be easily employed to facilitate heat removal. One of such techniques is 'wafer thinning'. Combined with a thick thermal shunt and a thin

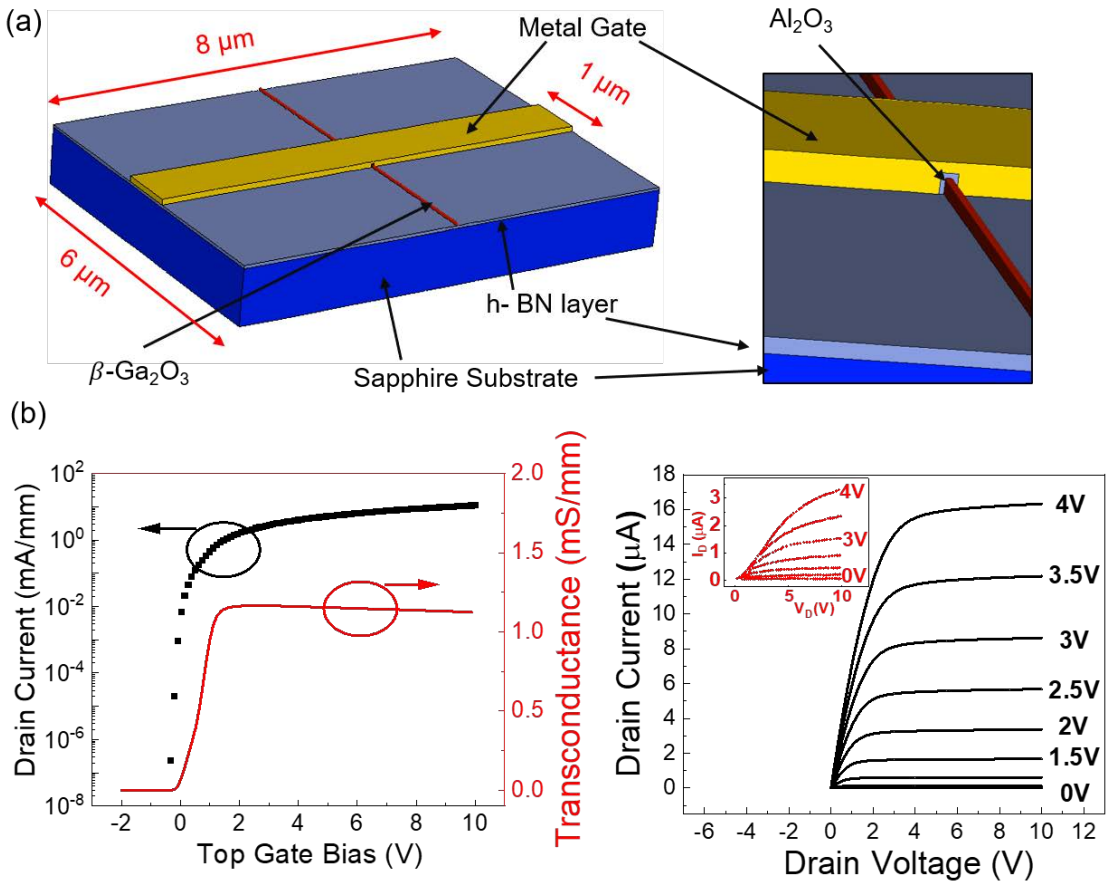


Figure 3.15. TCAD model of Enhancement mode wrap gate device on h-BN. (b) I_D-V_G of the β-Ga_2O_3 FET on h-BN coated Sapphire substrate, as obtained from TCAD simulation. (c). I_D-V_D data with β-Ga_2O_3 FET on h-BN coated Sapphire substrate, obtained from TCAD, which is about 500% more than the experimental data from [127], given in inset.

silicon wafer, the thermal resistance of β-Ga_2O_3 transistor can be reduced, as shown in Fig. 3.14, which improves the performance.

However, most of these devices are depletion-mode. If enhancement-mode devices are required, h-BN based FETs must use a surround-gate configuration, as shown in Fig. 3.15. The $I_D - V_G$ and transconductance curves are shown in Fig. 3.15 (b). The subthreshold slope has been determined to be 85 mV/dec. In TCAD, at least 500 % enhancement in I_{ON} has been observed for h-BN based FET Fig. 3.15 (b) compared to the existing FET (inset). Thus, if fabricated, this enhancement-mode h-BN/Sapphire β-Ga_2O_3 transistor will lead to a high current by dissipating the generated heat better.

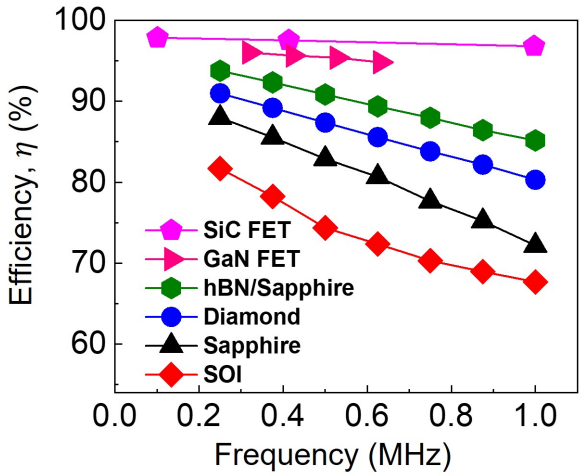


Figure 3.16. Efficiency of the boost converter circuit, with hBN/Sapphire configuration.

3.3.2 Circuit Simulations (HSPICE)

The device performance of β-Ga_2O_3 transistor using thermal shunt has improved. However, using h-BN/Silicon/β-Ga_2O_3 as a switch in the boost converter does not offer significant improvement. This is evident from the efficiency ($\eta = P_{out}/P_{in}$) plot in Fig. 3.16. Therefore, the key conclusion of this section is that despite the remarkable performance, the devices reported in the literature may still not be sufficiently efficient for practical power electronics applications.

3.3.3 Package Performance (COMSOL)

Now we can use the θ_{th} of the h-BN/Sapphire/β-Ga_2O_3 and simulate the Faraday Cage, and see the temperature rise. Faraday caging leads to reduced footprint, stacked inductor-transistor configuration. The temperature rise in h-BN/Sapphire/β-Ga_2O_3 is similar to that in GaN commercial packaging modules [172], as shown in Fig. 3.17.

3.4 Summary

Despite the promising experimental demonstrations of variety of power devices, we determine that the low-λ will hinder the commercial adoption of β-Ga_2O_3 FETs for power

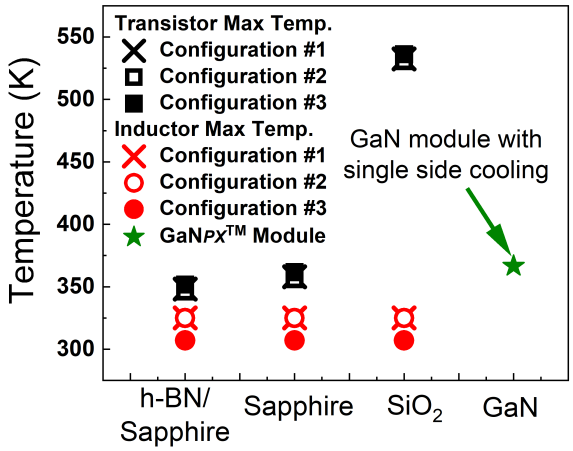


Figure 3.17. Transistor and inductor temperature comparison among various packaging strategies. GaN data taken from [172].

electronics applications. A holistic evaluation of performance from a device-circuit-system perspective is necessary before reaching any conclusion regarding the technological viability of β-Ga_2O_3. The findings of this chapter is summarized below:

(a). We develop a multi-physics and multi-scale model for a device-circuit-system analysis of β-Ga_2O_3 FETs. The framework allows us to explore the effectiveness of various device design strategies (e.g. thermal shunts) for mitigating the thermal chokepoints and compare the performance of improved β-Ga_2O_3 FETs against GaN and SiC systems.

(b). We highlight the limitations of the traditional figure of merits (FOM) to analyze the relative performance of the new generation of power transistors, whose structure incorporates stacked layers of materials with different thermal conductivity, like those of β-Ga_2O_3 FETs.

(c). We suggest device design strategies, such as wafer thinning, incorporating heat shunts, and improved channel mobility so that β-Ga_2O_3 FETs can compete commercially with GaN and SiC technologies.

(d). The device-circuit-system models presented in this chapter quantify the detrimental effect of severe self-heating, even in high-λ substrates like Sapphire and Diamond. The various device configurations currently existing in the literature do not provide much improvement.

(e). Based on the analysis presented in this chapter, we conclude only a combination of improved channel mobility, high thermal conductivity heat shunts, and wafer thinning will make β-Ga_2O_3 technology commercially competitive to GaN or SiC technologies. Together with the significantly lower substrate cost, the new device-circuit-package structure is likely to deliver the performance improvement originally promised by β-Ga_2O_3 FET.

4. REDISCOVERY OF THE UNIVERSAL SCALING OF HOT CARRIER DEGRADATION IN LDMOS TRANSISTORS

4.1 Introduction

In the previous chapter (chapter 3), we analyzed the electrothermal performance of β-Ga_2O_3 FETs, where we concluded that the thermal conductivity and the corresponding self-heating is the limiting factor, which was predicted by the i-SOA in Chapter 2. In chapter 2, we also presented the reliability-aware i-SOA, where we took an example of Silicon LDMOS and concluded that, as stress time increases, the interface trap (N_{it}) generation increases, and the i-SOA decreases. However, the physics behind the generation of defects and the degradation of current weren't discussed there. In this chapter[1] we will take a detailed look into the reliability of Silicon LDMOS transistors, as protypical power device. Among all electrical reliability phenomena, Hot Carrier Degradation (HCD) is the most common degradation phenomena in LDMOS, due to high drain bias.

Since the 1970s, HCD in classical long-channel MOSFETs has been studied extensively, and the key results are summarized as follows: (1) HCD degradation maximizes at $V_G \sim V_D/2$ and the maximum degradation is correlated to the peak of substrate current (I_B) [173]. (2) The generation of N_{it} is characterized by a single power-law behavior ($\Delta V_{th} = At^n$), with the time exponent n close to 0.5 [174]. (3) The interface damage, causing HCD, has been located close to the channel-drain edge where the electric field peaks [21]. (4) The degradation has been shown to scale to a single universal curve allowing reliable extrapolation [107].

Actually, the universal scaling has been shown to hold even for shorter channel transistors, with maximum degradation at $V_G \sim V_D$ and the degradation time-exponent n dependent on voltage, temperature, and device dimensions [2], [3], [107], [175]. This theory-agnostic universal degradation simply reflects the fact that degradation in a logic transistor can be described by the general form $\Delta N_{it} \sim f(t/\tau)$, where $\tau(V_G, V_D, T, G)$ is a characteristic function of voltage (V_G, V_D), temperature (T), and geometry (G). Therefore, when individual degradation curves ($\Delta I_{D,lin}(\%)$) at each bias are scaled along the timescale, it forms a single universal scaling function.

[1] ↑Most of the content of this chapter is based on Ref. [2] and [143]

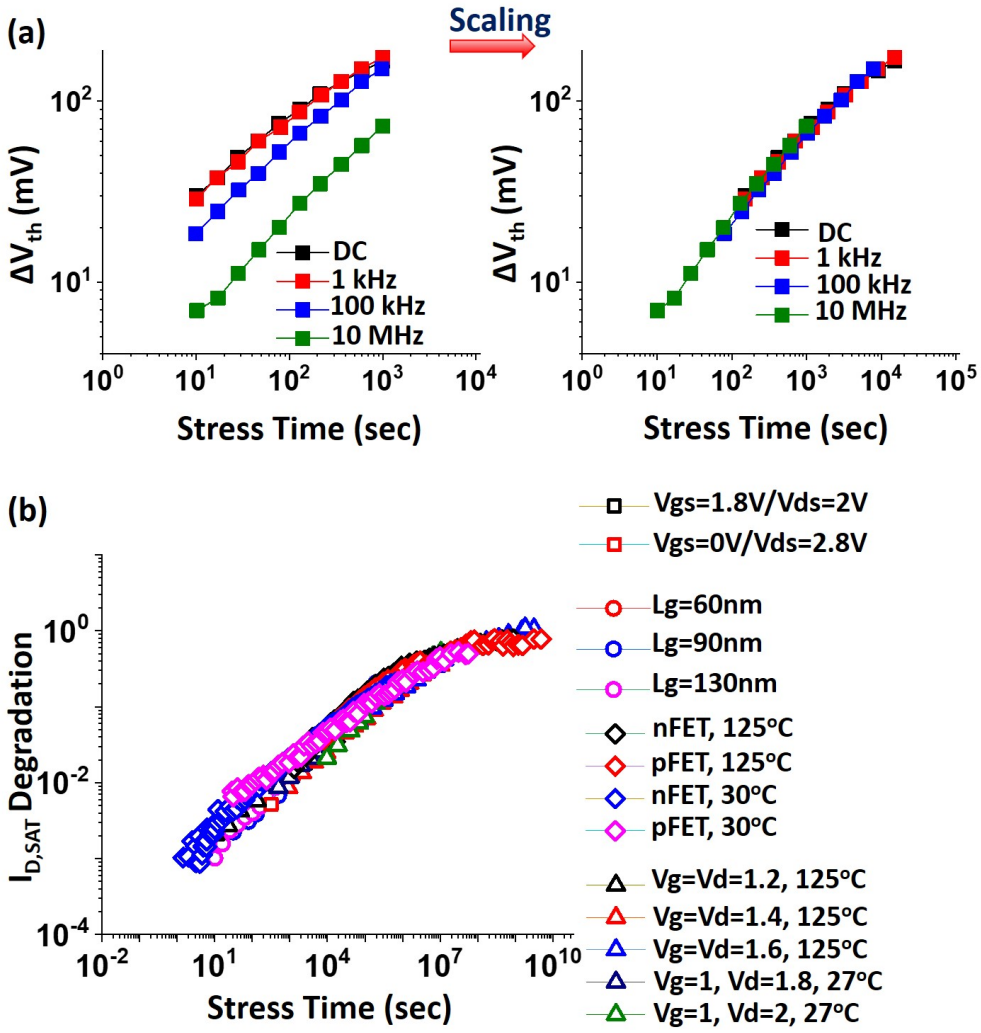


Figure 4.1. (a) Methodology of scaling the data to a universal curve, taken from [2]. (b) Universal scaling curve obtained from various technologies (DMOS, FinFETs), gate lengths, operating voltages, temperatures, suggesting that the underlying mechanism of HCD is universal [2].

Using the scaling function, $\tau(V_D, V_G, T_L,)$, one can project HCD degradation to an arbitrary combination of stress conditions. It should be noted that while the functional form has been derived variously using single particle, multiple particle, electron-electron, or bond-dispersion model, the scaling approach itself does not presume Arrhenius temperature activation, nor any specific form of voltage/field/time degradation [176]. Fundamentally, the scaling theory is borrowed from statistical physics of percolation and phase-transition, except

the spatial renormalization is replaced with time renormalization. An example of universal scaling for logic transistors is shown in Fig. 4.1.

Despite the long history, distinctive device topology, and operating conditions, HCD of power transistors (e.g., Laterally Diffused MOS (LDMOS)) has always been described by borrowed/adapted HCD theories of long-channel transistors (with questionable validity of the projected lifetime). Therefore, immediately after the discovery of universal scaling in logic transistors, researchers explored the possibility that the HCD in power transistors is likewise universal [177].

Fig. 4.2 shows a typical result of HCD degradation of a non-STI LDMOS transistor, with dimensions and doping optimized for breakdown voltage, $V_{bd} \sim$ 10 - 20 V. When the individual degradation curves in Fig. 4.2 (a) are scaled along the time axis, we find that unlike classical HCD in a logic transistor, the data does not fall onto a single universal curve, with prominent deviation from universality at the shorter time scale. Such a significant

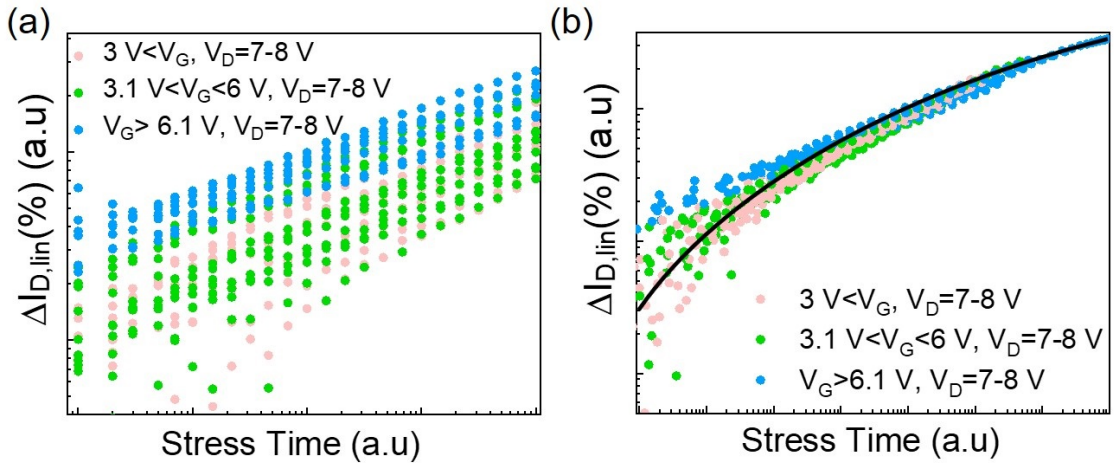


Figure 4.2. (a) HCD data of a silicon LDMOS transistor. (b) The data from (a) are scaled laterally to see if they form a universal degradation curve (black solid line). Clearly, the data cannot be described by a single universal curve.

deviation cannot be described by a single scaling function, $f(t/\tau)$, making it impossible to use the curve to determine the lifetime at a lower operating condition. Therefore, we need to review the existing specialized HCD models for power transistors (as opposed to logic

transistors) to see if it is possible to modify/adapt the scaling functions so that the paradox of the non-universal scaling of LDMOS transistors is resolved.

4.2 Existing Models of HCD for Power Transistors

Historically, the time-dependent degradation, $\Delta(t)$, of classical MOSFETs is modeled frequently using the Lucky Electron Model [21]:

$$\Delta(t) \sim Bt^n \tag{4.1}$$

with $B \equiv A\xi_n \equiv A\left(\frac{I_D}{W}\left(\frac{I_{sub}}{I_D}\right)^{\frac{\phi_{it}}{\phi_i}}\right)^n$, where A is a fitting parameter, I_D is the drain current, I_{sub} is the substrate current, W is the channel width, ϕ_{it} is the critical energy for N_{it} generation, ϕ_i is the critical energy for impact ionization, and n is the slope of the degradation. In practice, HCD in both logic and power transistors exhibit a saturating time-dependent degradation [107], which is not captured by the power-law model [177]. Instead, many groups have used the bond dispersion (BD) models [176], [178] or its approximation [179], given as:

$$\Delta I_{D,lin}(\%) = \frac{C_1 t^m}{1 + C_2 t^m} \tag{4.2}$$

to describe the saturating degradation of the power transistors. Here, the fitting parameters C_1,C_2, and m describe the voltage- and temperature-dependent rates of bond dissociation and the energy distribution of the bonds. Later, Dreesen et al. [180] combined Eqs. 4.1 and 4.2 to propose a degradation model for power transistors as:

$$\Delta I_{D,lin}(\%) = \frac{C_1^* \xi_m t^m}{1 + C_2^* \xi_m t^m} \tag{4.3}$$

where $\xi_m \equiv \left(\frac{I_D}{W}\left(\frac{I_{sub}}{I_D}\right)^{\frac{\phi_{it}}{\phi_i}}\right)^m$. Eq. 4.3 reasonably describes the HCD degradation of transistors with a single hotspot close to the drain. More importantly, the formulation allows a single-parameter universal scaling of all HCD degradation curves [107], [178]. Moens et al. [181] were among the first group of researchers to report that a single degradation term (single scaling function) cannot describe the HCD degradation in LDMOS transistors with thick

LOCOS (bird's beak) regions. Based on charge pumping (CP) measurements, they identified three regions of degradation and phenomenologically described the overall degradation (ΔR_{on} (%) or $\Delta I_{D,lin}$ (%)) as:

$$\Delta I_{D,lin}(\%) = \frac{C_1^* \xi_m t^m}{1 + C_2^* \xi_m t^m} + C_3^* \xi_n t^n \tag{4.4}$$

where C_1^* and C_3^* describe the degradation in n-well and bird's beak regions, respectively, and C_2^* accounts for saturating degradation in the n-well region. Here, although the channel region of the LOCOS LDMOS degrades, it does not contribute significantly to the overall $I_{D,lin}$ degradation.

Since Eq. 4.4 phenomenological, it is difficult to generalize it for other types of LDMOS with different geometry (e.g., non-LOCOS LDMOS, as in our case). In a non-LOCOS LDMOS, the electric field peaks both at the channel and the drift regions [144], suggesting the possibility that both regions might contribute to overall degradation. However, it is difficult to predict the channel's contribution in the absence of a non-LDMOS-specific LDMOS HCD model or a generalized HCD model for all LDMOS devices. A generalized, physics-based HCD model would require a careful re-examination of the voltage-partitioning between the channel vs. drift regions and should be valid for both low and high voltage stress. These considerations lead to the conclusion that a thorough re-evaluation of the degradation models of HCD in LDMOS is required before the models (or scaling functions) are adapted for constructing the universal degradation curve.

At first glance, one may conclude that, since the device structure of power transistors (LDMOS) are different, the HCD is also fundamentally different than a classical MOS. However, by using a simple '2 MOS model' (inspired by a similar model in LDD MOSFETs [179]), we will show that, although the device structure influences the overall degradation, an in-depth analysis of device operation allows us to describe the HCD in the entire V_G,V_D regime accurately and to restore the universality of HCD degradation in LDMOS transistors.

4.3 Experimental Details

4.3.1 Device Structure and Dimensions

All the experiments reported in this chapter are based on n-channel LDMOS transistors with no Shallow Trench Isolation (STI) or LOCOS. The gate covers both the channel and drift regions, and the device is optimized to eliminate most of the parasitic junction capacitances. The transistors are fabricated on Silicon wafers by Texas Instruments Inc., and the doping profiles are such that the breakdown voltage, V_{bd} is 10 - 20 V.

4.3.2 HCD Experiments

The n-channel non-LOCOS LDMOS transistors were subjected to electrical stress at different combinations of V_G and V_D biases at room temperature. The stress experiments and measurements were done by programming the Keysight B1500A Semiconductor Device Analyzer. The stress bias and the bias for $I_D - V_G$ sweeps were carried out using the Source Measurement Units (SMUs). The stress bias conditions were: V_D = 7 - 8 V and V_G = 2 - 9 V. The bias conditions for $I_D - V_G$ sweeps were: V_D = 0.1 V and V_G = 0 V to 5 V in steps of 0.05 V. The HCD relaxation was confirmed to be negligible.

4.3.3 TCAD Simulations

TCAD Simulations were carried out in Sentaurus TCAD (version: L-2016.03) [160] from Synopsis Inc. to calibrate the 2 MOS model and to gain insights into the physical parameters (electric field, impact ionization, etc.) of the LDMOS at various V_G and V_D biases. The transport and doping models were chosen carefully so that the TCAD model can self-consistently predict the device's performance. The carrier transport in LDMOS was solved using the first-order Spherical Harmonics Expansion of the Boltzmann Transport Equation. To model the impact ionization, the van Overstraeten – de Man Model was used [182]

4.4 '2 MOS Model' of an LDMOS

Designers working with power transistors have long understood that the complexity of geometry and doping profile requires the adoption of a multi-component compact model to capture the complexity of I-V characteristics of these devices [183]–[185]. In general, specialized operating conditions (e.g., high V_D) makes LDMOS HCD distinctly different from long channel MOSFET. The key to developing a physics-based HCD model and restoring the universality of HCD for LDMOS transistors is to recognize that the sub-components of the transistor degrade at different rates and must be scaled independently to describe the overall degradation process.

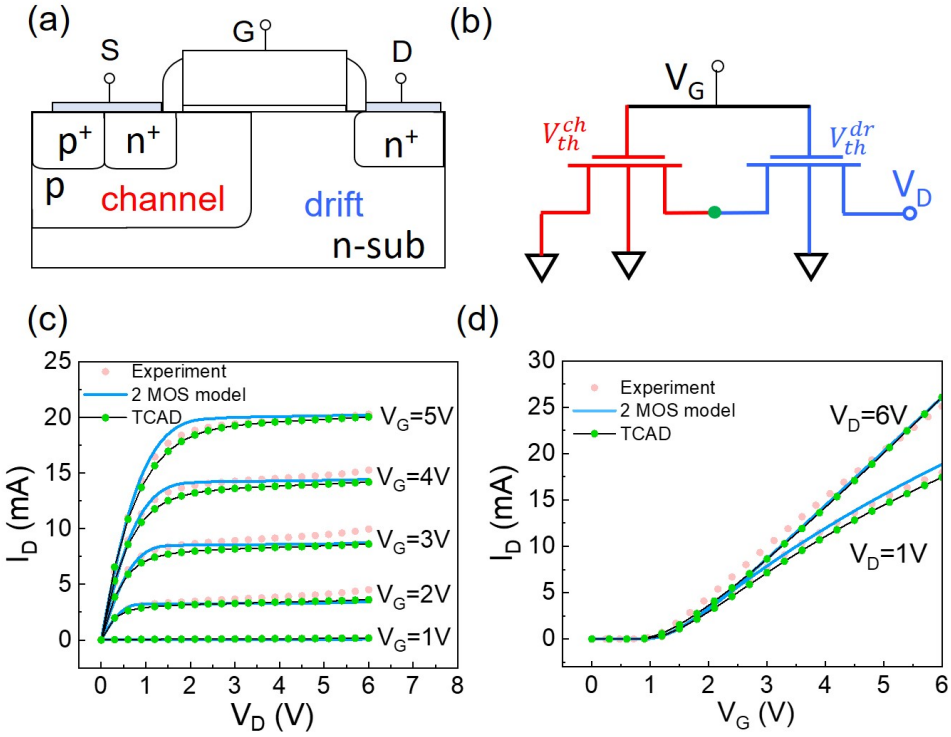


Figure 4.3. (a) Representative cross-section of a Silicon LDMOS device (b) 2 MOS model. S, G, D, V_{th}^{ch} and V_{th}^{dr} are the source, gate, drain, threshold voltage of channel MOSFET and drift MOSFET, respectively. The green dot is the metallurgical junction between the two MOS. Calibration of the model with TCAD and Experiments is shown in (c) and (d).

4.4.1 Calibration with Experiments and TCAD

LDMOS can be represented by two MOSFETs (BSIM6 compact model) connected in series with two different threshold voltages and geometric dimensions. Such a representation allows us to treat the degradations in the channel and drift regions independently. The '2 MOS' compact model has been validated by experiments and TCAD, as shown in Fig. 4.3.

Comprehensive calibrations of the 2 MOS model, TCAD, and HSPICE are documented in [144]. A key observation of the 2 MOS model is that depending on the applied voltage ($V_G < V_D/k$ or $V_G \geq V_D/k$), the maximum electric field switches from the drift to the channel region of the LDMOS (Fig. 4.4), accentuating the degradation in the respective regions of the device. In general, the degradation is concentrated in the drift region for $V_G < V_D/k$, once the $V_G \geq V_D/k$, the maximum electric field switches from drift to the channel region, and degradation occurs both in the channel and drift region. For this particular LDMOS, at room temperature, $k = 2$, the value of k is technology-, temperature-, and structure-dependent.

Representing the LDMOS as two MOSFETs enables direct extraction of region-specific mobility and threshold voltage degradation (ΔV_{th}) [144]. As explained in [144], ΔV_{th} doesn't impact $\Delta I_{D,lin}$ and therefore ΔV_{th} has been ignored in the following analytical model derived for $\Delta I_{D,lin}$.

4.4.2 Analytical Model of Two-region Degradation

To derive an analytical relation when the peak electric field is in channel ($V_G \geq V_D/2$), it is considered that the drift MOS have a resistor, R_{dr}. Assuming operation in the linear region, the current with the drift resistance R_{dr} is:

$$I_D = \frac{\beta_{ch}\left(V_G - V_{th}^{ch}\right)V_D}{\left[1 + \beta_{ch}\left(V_G - V_{th}^{ch}\right)R_{dr}\right]} \tag{4.5}$$

where β_{ch}=$\mu_{ch}C_{ox}W/L_{ch}$. Here μ_{ch}, L_{ch}, V_{th}^{ch} are the mobility, length, and threshold voltage of the channel, respectively. W is the device width. R_{dr} can be obtained as:

$$R_{dr} = \frac{1}{[\beta_{dr}(V_G - V_{th}^{dr})]} \tag{4.6}$$

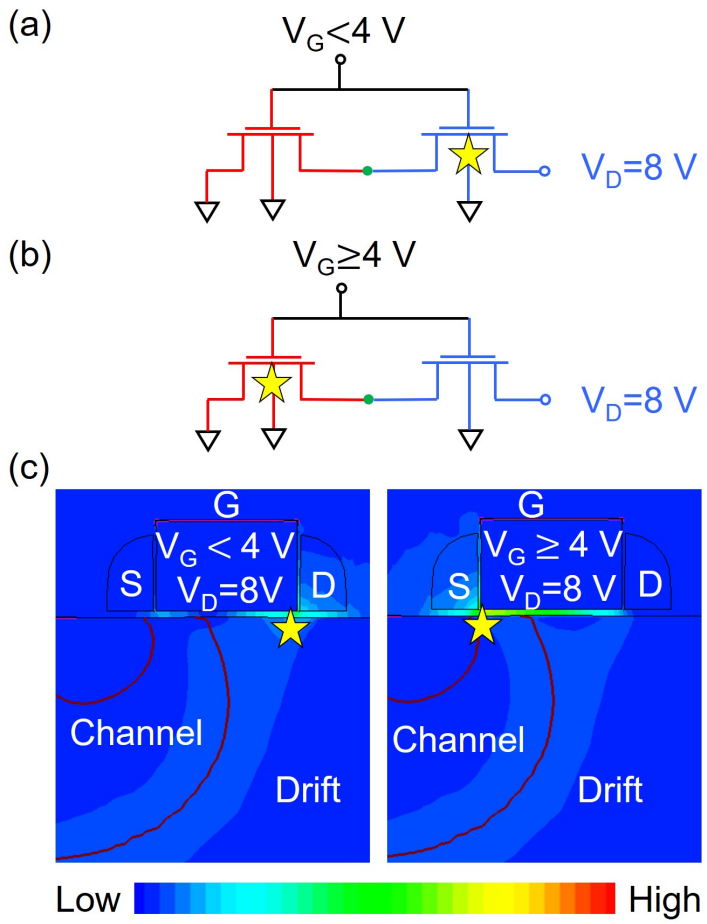


Figure 4.4. Position of peak electric field (represented by a star) is the drift MOS for (a) $V_G < V_D/2$ and in the channel MOS for (b) $V_G \geq V_D/2$. The corresponding electric field profiles are shown in (c).

where $\beta_{dr}=\mu_{ch}C_{ox}W/L_{dr}$. Here μ_{dr}, L_{dr}, V_{th}^{dr} are the mobility, length, and threshold voltage of the drift region respectively. W is the device width. The current without the drift region is given as:

$$I_D^* = \beta_{ch}(V_G - V_{th}^{ch})V_D \tag{4.7}$$

Using 4.7, 4.5 can be expressed as:

$$I_D = \frac{I_D^*}{[1 + K_0]} \tag{4.8}$$

where K_0 is the conductance ratio, which depends on length, width, mobility of the transistor and applied V_G, and is given as:

$$K_0 = \frac{\beta_{ch}(V_G - V_{th}^{ch})}{\beta_{dr}(V_G - V_{th}^{dr})} \tag{4.9}$$

Now let us consider the mobility parameters: M_{ch}, M_{dr} for the drift and the channel regions. Considering the value of $\Delta\mu_{ch}$ and $\Delta\mu_{dr}$ to be positive, it can be written as $M_{ch,dr}$ = 1-($\Delta\mu_{ch,dr}/\mu_{ch,dr}$) or ($\mu_{ch,dr}^{deg}$=$\mu_{ch,dr}$ $\times$ $M_{ch,dr}$). Therefore the degraded I_D, or I_D^{deg}, can be written as:

$$I_D^{deg} = \frac{M_{ch} I_D^*}{1 + (M_{ch} K_0 / M_{dr})} \tag{4.10}$$

For $\Delta I_{D,lin}(\%)$, we can use Eqs. 4.8 and 4.10 to write:

$$\Delta I_{D,lin} = \frac{I_D - I_D^{deg}}{I_D} = \alpha\,(1 - M_{ch}) + (1 - \alpha)\,(1 - M_{dr}) \tag{4.11}$$

where $\alpha = 1/(1+K_0 R)$ and $R \equiv M_{ch} M_{dr}$. If the channel degradation is negligible, $1-M_{ch}\sim 0$, so that $\Delta I_{D,lin} \sim (1 - M_{dr})$ as expected. The same is true if drift degradation is negligible. From Eq. 4.11, depending on the gate and drain voltages, the degradation in the channel and the drift proceeds at different rates such that $\Delta I_{D,lin} = \alpha f_1(t/\tau) + (1-\alpha) f_2(t/\tau)$,where $f_1(t/\tau)$ and $f_2(t/\tau)$ are scalable functions. The functional forms of $f_1(t/\tau)$ and $f_2(t/\tau)$ would arise naturally from experimental data, which can then be individually interpreted variously by bond-dispersion model, carrier-carrier excitation model, or multi-photon models. For example, in the bond-dispersion model [176], the fraction of activated defects, D, is often approximated as:

$$D = (1 - M) = f\left(\frac{t}{\tau}\right) \sim \frac{(t/\tau)^n}{1 + (t/\tau)^n} = \frac{A t^n}{1 + B t^n} \tag{4.12}$$

where A, B are voltage- and temperature-dependent functions, and $n \sim 0.3$ - 0.5 for classical MOS. For integrated degradation associated with the channel and the drift regions, from Eq. 4.12,

$$\Delta I_{D,lin} = \alpha \frac{A_{ch} t^m}{(1 + B_{ch} t^m)} + (1 - \alpha) \frac{A_{dr} t^n}{(1 + B_{dr} t^n)} \tag{4.13}$$

It is to be noted in Eq. 4.13, that at a very long timescale (t), $A_{ch,dr} \sim B_{ch,dr}$. Eq. 4.13 offers a physics-based generalization of Eq. 4.4 for the arbitrary gate and drain voltages, suggesting the need for universal scaling based on the voltage-dependent degradation rates of channel and drift region. This power-law approximation is not essential; the two-component scaling holds regardless of the specific theory used to describe the HCD. In essence, the model suggests that one must partition/deconvolve the degradation for the channel and drift regions after scaling to obtain the local degradation characteristics.

4.5 Separating Region-Specific Degradation

4.5.1 Voltage-Dependent Degradation

As explained in the previous section, one can stress below or above the transition voltage $V_G = V_D/k$ to spatially trigger the defects in the channel or drift region. The transition voltage factor, k (i.e., $V_G = V_D/k$), can be determined from TCAD simulations ($k \sim 1$ for logic transistors, $k = 2$, for this specific LDMOS transistor, at room temperature). For example, Fig. 4.5 shows the corresponding degradation results for the device stressed below (drift only, Fig. 4.5 (a)) and above (drift and channel regions, Fig. 4.5 (b)) the transition voltage. Since the HCD mechanism is similar in two regions, the time exponents should be identical ($n = m$). Using (Eq. 4.13), both region-resolved degradations (channel and drift) can be fitted with similar exponents (n,$m \sim 0.36$), reinforcing the fact that although the degradation rates are region-specific, the physics is universal. As seen in Fig. 4.5(b), the degradation and the saturation rates of channel and drift regions are different, which will be discussed in the following sub-section.

The impact ionization profiles obtained from TCAD simulations provide further confirmation that the channel degradation becomes prominent at high V_G. As shown in Fig. 4.6, when $V_G < V_D/k$, the impact ionization is concentrated in the drift region, while at increased V_G ($V_G \geq V_D/k$) a significant amount of impact ionization is present in the channel region also.

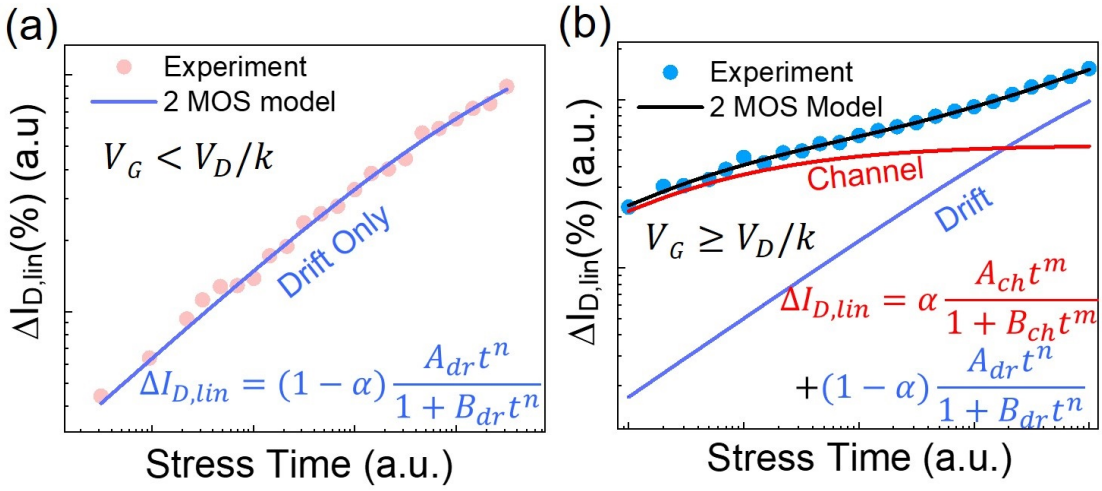


Figure 4.5. Two sets of data from Fig. 4.1, fitted with Eq. 4.13 at (a) $V_G < V_D/k$ and (b) $V_G \geq V_D/k$, where k=2, for the device in consideration. The same time exponent $n \sim m$ was assumed for the fitting. For both cases V_D is fixed at 8 V.

4.5.2 Saturation of the Channel and the Drift Region

The different saturation rates of the channel and the drift region can be understood by analyzing the degradation term, D, included in Eq. 4.12. The specific function of D can be derived as a function of ΔN_{it} (since $D = \Delta\mu/\mu_0 \equiv \gamma\Delta N_{it}/(1+\gamma\Delta N_{it})$, where γ is a device-specific fitting parameter [186]), by assuming that the Si-H and/or Si-O interface bonds are characterized by a Gaussian energy distribution [178] where E and E_{AV} are activation energy and mean activation energy, respectively. With the forward reaction (bond-dissociation) rate given by:

$$k(E) = k_0 \mathrm{e}^{-\frac{E-E_{AV}}{kT}} \tag{4.14}$$

We can write the respective degradation in the channel and the drift regions by integrating over the bonds dissociated in the respective hotspots (with widths L_{eff}^{dr} and L_{eff}^{ch}) as:

$$N_{it}^{dr}(t) = \int_0^{L_{eff}^{dr}} \int_{E_{AV}-m\sigma}^{E_{AV}+m\sigma} g(E,x)\left(1-\mathrm{e}^{-k_{dr}(E)t}\right) dEdx \tag{4.15}$$

$$N_{it}^{ch}(t) = \int_0^{L_{eff}^{ch}} \int_{E_{AV}-m\sigma}^{E_{AV}+m\sigma} g(E,x)\left(1-\mathrm{e}^{-k_{ch}(E)t}\right) dEdx \tag{4.16}$$

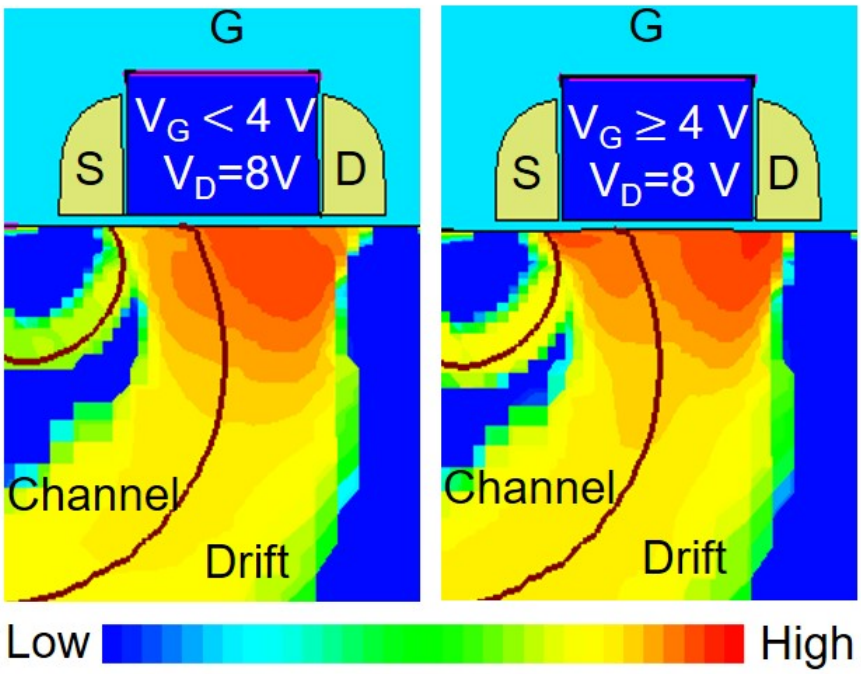


Figure 4.6. Impact ionization profiles for V_G<$V_D/2$ (left) and V_G≥$V_D/2$ (right). At high V_G, significant amount of impact ionization is present in the channel and the drift region.

where $m\sigma$ is the energy dispersion width, L_{eff}^{dr} and L_{eff}^{ch} are the effective width of the drift and channel hotspots, and $g(E, x)$ is position-dependent density of interfacial (Si-H or Si-O) bonds with binding energy E. It is to be noted that unlike traditional N_{it} (which is expressed in units of cm^2), here N_{it} is expressed in per unit length (cm) because the position integrated N_{it} affects mobility. The forward reaction rates of the drift and the channel region (k_{dr} and k_{ch} respectively) depend on the applied voltages across these specific regions. Assuming that the energy distribution of the bonds does not rely significantly on the location of the bonds (i.e., $g(E) \sim g(E, x)$), we can write:

$$N_{it}^{dr}(t) = L_{eff}^{dr} \int_{E_{AV}-m\sigma}^{E_{AV}+m\sigma} g(E) \left(1 - e^{-k_{dr}(E)t}\right) dE \tag{4.17}$$

$$N_{it}^{ch}(t) = L_{eff}^{ch} \int_{E_{AV}-m\sigma}^{E_{AV}+m\sigma} g(E) \left(1 - e^{-k_{ch}(E)t}\right) dE \tag{4.18}$$

From Fig. 4.6, it can be seen that the hotspot in the drift region is larger than the channel region even at high V_G,V_D and hence $L_{eff}^{dr} > L_{eff}^{ch}$. Therefore, the integrated channel degradation saturates faster than the drift degradation, as shown in Fig. 4.5(b).

Moreover, the electric field in the channel region is higher than the drift region of our device at high V_G,V_D (Fig. 4.4), and therefore, the forward reaction rate, $k(E)$, is higher in the channel (the electric field is proportional to the energy in $k(E)$), compared to the drift region. This leads to a higher degradation rate in the channel than the drift, leading to faster saturation.

We note that the contributions of the channel and the drift degradations to the overall device $\Delta I_{D,lin}$, is dependent on the parameter α. The longer the drift region in a device, the smaller the α, and hence smaller the contribution of the channel degradation. Therefore, the relative contributions of the two degradation components depend on the device geometry and doping concentration, as expected. Taking the example of devices with bird's beak, charge pumping experiments show that the defects can be located at the channel, the bird's beak, and the n-well region [181]. However, defects at all three positions have fundamentally different saturation rates. Therefore, the *principle* of multiple-component degradation is expected to hold for all power devices, but the specific features of the individual degradation and their integrated effect (universal scaling curve) depend on specific devices.

4.5.3 Universal Scaling of Degradation

The bond-dispersion model (Eqs. 4.17 and 4.18) described in the previous sub-section provides the theoretical basis of the universal scaling curve of degradation for the LDMOS. The analysis in the previous sections and Eqs. 4.17, 4.18 confirm that the channel and drift regions degrade with voltage-dependent region-specific degradation rates, and therefore all degradation curves must not be scaled to a single universal curve for the entire V_G, V_D regime. Instead, they should be grouped according to the voltage transition factor, k, ($k = 2$ for our devices). In addition, at high V_G, V_D, when both the degradations (channel and drift) are present, channel degradation is rapid and saturates faster than the drift degradation.

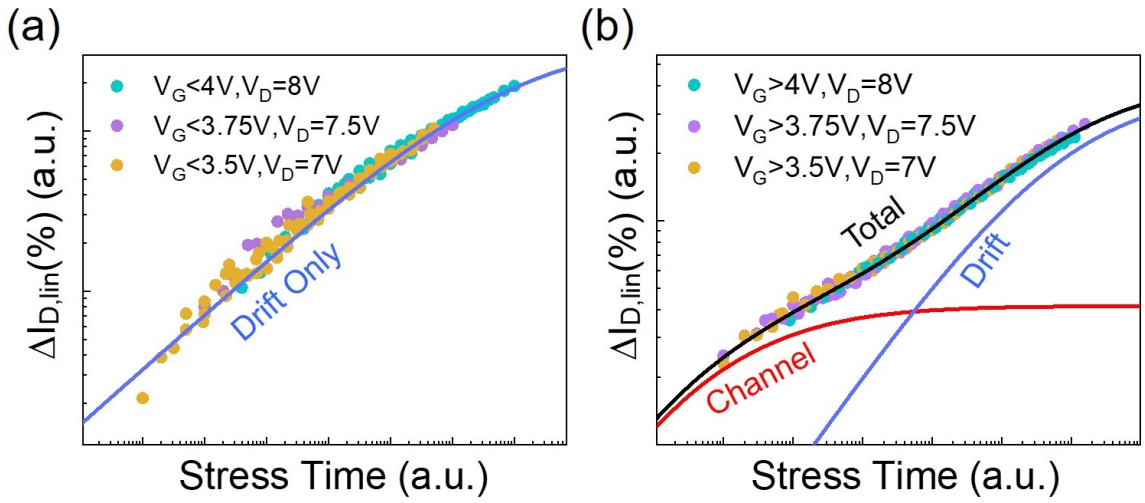


Figure 4.7. Data from Fig. 4.1, replotted by two-component universal scaling at (a) $V_G < V_D/k$ and (b) $V_G \geq V_D/k$, where $k = 2$.

Keeping these factors in mind, the universal scaling curve for the LDMOS is constructed by scaling each degradation curve with a scaling factor ($\tau(V_G, V_D)$), as shown in Fig. 4.6. When the degradation is dominated by the drift region ($V_G < V_D/2$), the degradation curves scale to a single universal curve (Fig.4.7(a)). For $V_G \geq V_D/2$, degradation is contributed by both the local degradations in the channel and drift regions, and the sum of the two universal curves defines the overall degradation (Fig. 4.7(b)). The relative contributions of the channel (solid red line) and the drift (solid blue line) regions to the universal curve can be determined by fitting (Eq. 4.13) to obtain the parameters (A_{ch}, B_{ch}, A_{dr}, B_{dr}) and exponents (n,m), as shown in Fig. 4.7. (b). Eqs. 4.17, 4.18 can be solved numerically to obtain the universal scaling curves in Fig. 4.7 by appropriately accounting for L_{eff}^{dr}, L_{eff}^{ch}, m, σ and the forward reaction rates.

The scaling factors, $\tau(V_G, V_D)$, used to construct the universal degradation curve are inversely proportional to the degradation rate. The scaling factors extracted from the shift of $\Delta I_{D,lin}$ (%) are shown in Figs. 4.8 (a) and (b). Using the scaling factors, $\tau(V_G,V_D)$, it is possible to rescale all experimental data to their original positions. An approximate power-law fit has been achieved for $V_G < V_D/2$ and $V_G \geq V_D/2$ as shown in Figs. 4.8 (a) and (b). We would like to highlight that the scaling factors used to construct the universal curve

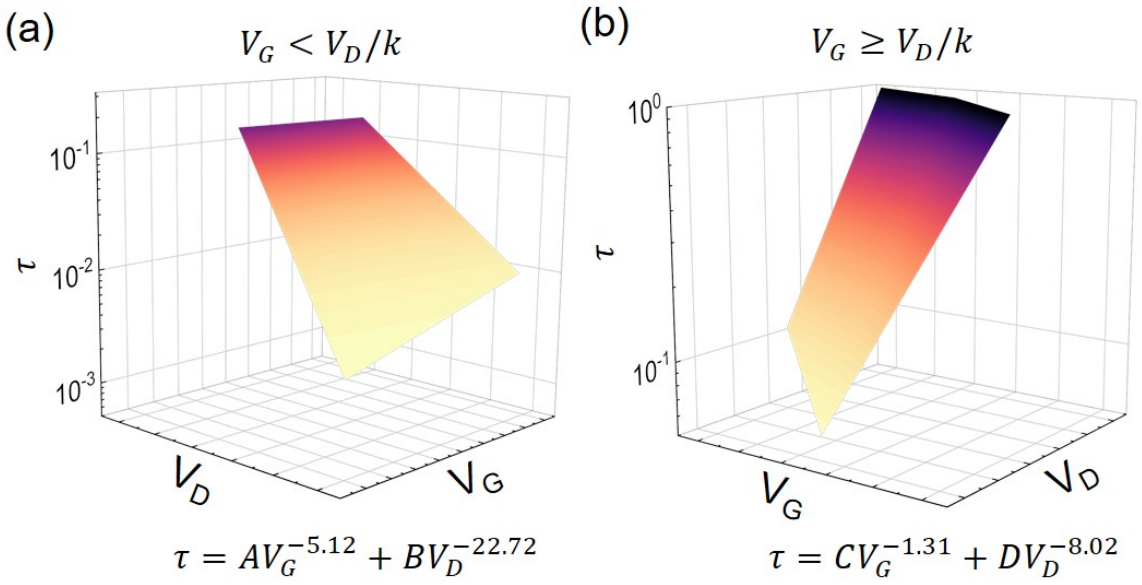


Figure 4.8. Voltage acceleration of the scaling factor, τ, for (a) $V_G < V_D/k$ and (b) $V_G \geq V_D/k$, where $k = 2$. The difference of the exponents reflects voltage partitioning between the channel and drift regions. A, B, C, and D are fitting parameters.

for $\Delta I_{D,lin}$ are obtained regardless of the location of degradation. For example, for all $V_G \geq V_D/2$, a single scaling factor is needed to construct the universal curve, although the overall degradation is contributed by degradations at both the channel and drain regions. This is because the degradation curves ($\Delta I_{D,lin}$ (%)) already includes the total contribution from both the channel and drift regions. Depending on the applied voltages, either the drift or the channel degradation becomes dominant and occupies either the leading part or lower part of the universal scaling curve. The relative contributions are obtained when the universal curve is interpreted by Eq. 4.13. Thus, the region-specific deconvolution of degradation using the '2 MOS model' restores the universality, thereby generalizing the theory of HCD for high and low power transistors.

4.6 Summary

We have shown here that Eq. 4.13 can be used to phenomenologically describe the HCD in LDMOS transistors at each V_G,V_D. Eq. 4.13, along with TCAD modeling, enables the

separation of region-specific degradations based on applied voltages. Once this information is available, the degradation curves can be grouped (into $V_G < V_D/2$ and $V_G \geq V_D/2$) for generating the universal curves. Afterward, the construction and interpretation of the universally scaled curve involve three logical steps:

(a). ***Scaling to form a Universal Curve***: In constructing the scaling curve, each $\Delta I_{D,lin}$ degradation curve was scaled by a scaling factor, $\tau(V_G,V_D)$, along the x-axis, for both voltage groups ($V_G < V_D/2$ and $V_G \geq V_D/2$), such that all the $\Delta I_{D,lin}$ degradation curves fall on the universal curve, as in Fig. 4.7.

(b). ***Interpreting the universal-curve in terms of location-specific degradation***: Once the scaling is complete and the universal curve constructed, we can then interpret the universal curve in terms of the relative contributions of the channel and the drift regions by fitting the parameters (A_{ch}, B_{ch}, A_{dr}, B_{dr}) and exponents (n,m) and of Eq. 4.13, as shown in Fig. 4.7 (b).

(c). ***Interpreting the physical origin of the degradation components***: Finally, Eqs. 4.17, 4.18 provide a physical interpretation of the overall degradation in terms of the bond-dispersion model.

Our key contributions here are:

(i) A direct and intuitive derivation of the linear current degradation in an LDMOS, based on the underlying compact '2 MOS' model,

(ii) Separating the respective contributions of various regions using a bias-voltage dependent deconvolution process.

(iii) Explicitly providing an opportunity to use I-V spectroscopy techniques [15], or position-resolved CP techniques [106], [187], [188], to independently determine the degradation.

(iv) Suggesting the possibility of assigning one degradation term of each hotspot in a multi-hotspot device (e.g., devices with bird's-beak usually show more than two hotspots, and therefore more than two degradation terms [177] would be needed to capture the safe operating area (SOA)) of the transistor, and

(v) Applying the insights related to region-specific degradation to restore the universal scaling principle of HCD degradation.

In short, although the HCD in power transistors appears to be fundamentally different than classical long-channel transistors, the physics of HCD, if correctly interpreted, is actually universal. The multi-component scaling principle would allow us to project lifetime to actual operating conditions.

5. TCAD SIMULATIONS OF HOT CARRIER DEGRADATION IN LDMOS

5.1 Introduction

Over the past few decades, LDMOS has become the most popular power transistor and is used in numerous applications, such as telecommunication, automotive, medical devices, space shuttles, etc., and can be easily implemented in smart power technologies. However, depending on the application, the geometry and applied biases can be dramatically different in an LDMOS. While the low voltage (Breakdown voltage, $V_{bd} \sim 10$ - 15 V) LDMOS usually have an oxide of thickness 10 - 20 nm, medium or high voltage LDMOS ($V_{bd} > 35$ V) features shallow trench isolation (STI) oxide of thickness $\sim$ 100 nm. However, current crowding around the STI-corners during device operation enhances the HCD. As a result, LDMOS with local oxidation of silicon (LOCOS) structures has been adapted, a few years ago [189].

Even though the initial studies of HCD in LDMOS date back a few decades ago, the physical mechanism of degradation is not fully understood, thus requiring device-specific, time-consuming and expensive qualification of every technology, even those with minor geographical or doping variation. Sharma et. al. [190] emphasized that the cold carriers must be considered in order to model the HCD accurately in n- and p-type LDMOS. Tallarico et. al., [189] investigated the HCD in both LOCOS and STI -LDMOS and highlighted the role of cold carriers in modeling HCD. According to their analyses, single hot electron collisions are the dominant mechanism of HCD in LOCOS LDMOS; in contrast, cold carriers play a significant role in the degradation of STI LDMOS at higher stress voltages. Reggiani et al. [191], also reaches a similar conclusion for STI LDMOS, using two different types of LDMOS (a short, low voltage and a long, high voltage LDMOS). In a different report by Tallarico et al. [192], single hot electron collisions have been shown to play a major role in the degradation of LDMOS featuring customized thick oxides (selective LOCOS). All these conclusions are drawn by calibrating parametric degradation (e.g., $\Delta I_{D,lin}$, ΔV_{th}) using TCAD-HCD models. However, the lack of a feasible experimental approach to extract $N_{it}(x)$ in LDMOS, made it challenging to verify the $N_{it}(x)$ obtained from the TCAD models, thus undermining the whole process. As a result, there is a longstanding interest in the power electronics indus-

try to understand the underlying mechanism in order to construct a predictive degradation model. In this chapter[1], we determine the physical mechanism of HCD in a non-LOCOS and LOCOS LDMOS using TCAD and demonstrate the capability of Super Single Pulse Charge Pumping (S^2PCP) technique to extract $N_{it}(x)$ at various points in the LDMOS. Using TCAD simulations and experiments, we try to understand how the device geometry impacts the degradation mechanism. This analysis establishes the robustness and identifies the limitations of TCAD modeling of HCD in LDMOS devices.

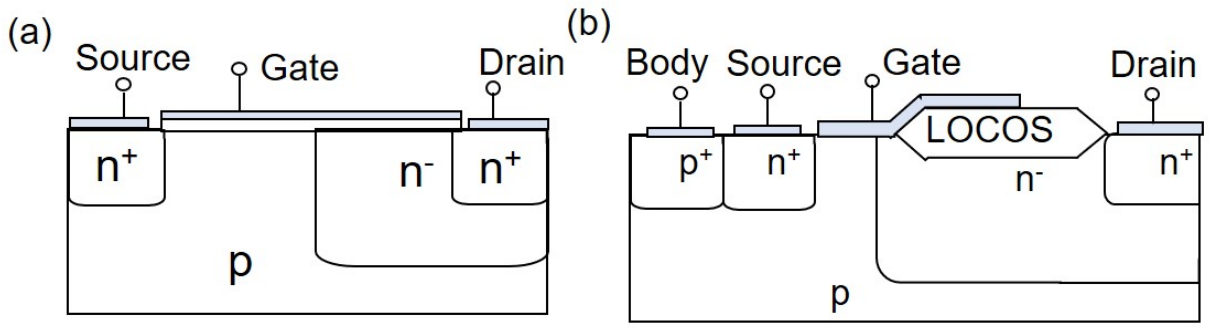


Figure 5.1. A schematic of (a) non-LOCOS LDMOS, and a (b) LOCOS LDMOS.

The non-LOCOS LDMOS usually operate at a relatively lower voltage (V_{bd} = 10 - 15 V) and have thinner oxides ($\sim$ 100 nm) than LOCOS LDMOS, and have applications in automotive parts (e.g., switches, airbag deployers), health-care equipment (e.g., implantable defibrillators, insulin pumps, glucose meters, neural stimulator), etc [144]. A schematic representing the two LDMOS is shown in Fig. 5.1.

5.2 Hot Carrier Degradation in High Voltage Transistors

It is well known that the dissociation of the Si-H bonds causes HCD at the silicon-insulator interface. Si-H bonds in the interface are formed in an annealing step following the dielectric deposition. The annealing step is essential to passivate the dangling Si bonds, which, if left unpassivated, can capture a charged carrier and degrade the device mobility.

One of the most popular models of HCD is the Lucky Electron Model, which states that under the influence of electric field, some electrons posseses high energy (hot electrons),

[1]↑Some of the content of this chapter is based on Ref. [106]

enough to surmount he Si-SiO_2 barrier, without losing energy or being scattered back to the channel, and then can depassivate these Si-H bonds by depositing its energy [193]. The energy of Si-H bonds is ∼1.5 eV [19], [194]; therefore, the energy of at least 1.5 eV is required to dissociate the bonds. Around the 1970s, when HCD was first reported, the supply voltage of the MOSFETs far exceeded the Si-H bond energy; therefore, HCD was a dominant degradation phenomenon. As supply voltage decreased, HCD decreased, only to re-emerge again at low voltages [19]. In a report in 1992 [195], HCD was found in a transistor, with supply voltage, less than 1 V. The concept of 'cold' carriers was then introduced to explain the phenomena.

These cold carriers depend on the scattering mechanisms (impact ionizations, electron-phonon, and electron-electron scattering, etc.) to exchange energy and populate the high energy tail of the electron distribution. In addition, due to multi-vibrational excitations (MVE), the Si-H bond disruption can be initiated by multiple cold carriers, instead of a single hot carrier. Thus, multiple-particle (MP) model was used to successfully explain the HCD for scaled devices with supply voltage less than 1 V. Pioneering work in this area has been done by Hess [176], [196], Bravaix [194], [197], [198], etc. The mechanism of HCD in power transistors, which are traditionally long-channel devices, was still believed to be caused by the single-particle (SP) mechanism. However, it was recently reported that even for power transistors, MP, or a combination of SP and MP, is responsible for HCD, depending on the applied bias and geometry. Therefore, modeling the physical mechanism in the power transistor depends on a sophisticated analysis of how the carrier ensemble is distributed over energy. This means that the carrier or electron energy distribution function (EEDF) is required to model HCD in transistors correctly. Fig. 5.2 provides the schematic representation of how a typical EEDF evolves as the electrons move from the source to drain in a MOSFET. When the electrons are near the source, they are in equilibrium and follow a Maxwellian distribution. As the electron ensemble moves towards the drain region, they become increasingly non-equilibrium; however, the average energy drops to the equilibrium value as the ensemble reaches the drain region.

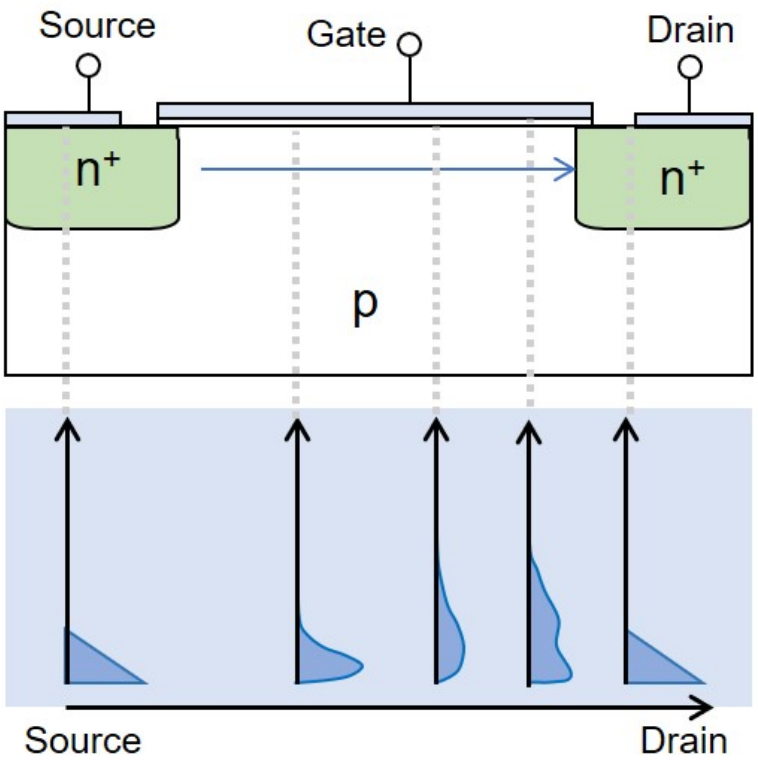


Figure 5.2. Schematic representation of EEDF evolution, from source to drain in a MOSFET.

5.2.1 Obtaining the Electron Distribution by Solving BTE numerically

The EEDF can be obtained as a solution of the Boltzmann Transport Equation (BTE). BTE is a semiclassical approach to describe the trajectory of a particle using Newtonian mechanics and probabilistic scattering rates. Solving the six-dimensional BTE is complicated, and statistical integration methods based on Monte Carlo techniques which were proposed for solving BTE in 1960s, are still relevant. Other approaches to solving BTE involves the scattering matrix method [199], [200], cellular automata methodologies [201], [202], spherical harmonics expansions [203]–[205], etc., which are implemented in device simulators (e.g., TCAD Sentaurus), or have their own dedicated solvers to obtain the EEDF (e.g. ViennaSHE [206]).

The moment-based approaches of solving BTE remains a popular methodology for modeling electron transport in device simulators. First proposed by Roosbroeck [207] in 1950s,

then demonstrated by Gummel for a practical device in 1960s [208], drift-diffusion is the most basic transport model for transistors. The drift-diffusion model can be derived by taking the first two moments of BTE and truncating them with some assumptions. The model is very well researched and implemented in all typical device simulators [209]. However, the drift-diffusion model cannot be used to describe the physics of hot electrons because it assumes that the electric field inside the device doesn't vary rapidly in the order of mean free path. To solve this, the hydrodynamic models (obtained by taking the first four moments of BTE) were developed [205]. These models are extensively implemented in device simulators and can calculate average energy, velocity, and electron density when solved along with the current continuity equations. However, there are persistent accuracy concerns with the hydrodynamic models [210].

One of the most commonly used deterministic approaches to solving BTE is that of the spherical harmonic expansion. This is based on the fact that the distribution of the electron momentum in equilibrium shows a spherical symmetry, and the distribution function can be represented with a zeroth-order expansion [203]. Although well known since 1960s, as evident from the reports of Baraff et al. [211], it was not widely adopted for device simulations until the analyses by Goldsman et al. [203] and Gnudi et. al [204] in 1990s. These early works represented the distribution as a perturbation of the equilibrium state, which is given as:

$$f(k^*) = f_0(E) + k^* g(E) cos\theta \tag{5.1}$$

where $f(k^*)$ is the distribution function in one of the first conduction valleys of k^* space, $f_0(E)$ is the coefficient of the first Legendre polynomial, $k^* g(E)$ is the coefficient of the second Legendre polynomial, and θ is the angle between the electron wave vector and the electric field in the starred space. Notable contributions to the development of the spherical harmonics expansion method for device simulation include: extension of the SHE method to arbitrary order by Hennacy et al. [212]; inclusion of full-band effects by Vecchi et al. [213]; approaches to handle hot electrons, impact ionization [214], etc. by researchers from the University of Bologna; discretization methods by Ringhofer [215] etc. Such consistent efforts made spherical harmonics expansion one of the most popular methods to model electron

transport and distribution in classical and emerging low and high voltage transistors. The TCAD analyses and degradation modeling presented in this chapter uses spherical harmonics expansion models.

5.2.2 Analytical Approaches to Obtain the Electron Distribution

Although deterministic BTE solvers are implemented in device simulators, they are sometimes computationally taxing and occasionally expensive. Therefore, there have been some attempts to represent the non-equilibrium distribution of electrons using analytical or numerical functions [216].

One of the most common approaches to represent the non-equilibrium carriers is by 'heated Maxwellian' distribution, which is given as [210]:

$$f_0(E) = A\mathrm{e}^{-\frac{E}{k_B T_\mathrm{e}}} \tag{5.2}$$

where k_B is the Boltzmann constant, T_e is the electron temperature, and A is a fitting parameter. However, the Monte Carlo simulations showed that the behavior of EEDF is not Maxwellian-like near the drain region of the MOSFET, and therefore will induce error in the HCD models. Cassi et al. [217], proposed a non-Maxwellian model, given as:

$$f_0(E) = A\mathrm{e}^{-\frac{\chi E^3}{\varepsilon^{1.5}}} \tag{5.3}$$

where $\chi = 0.1$, A is a fitting parameters, and ε is the local electric field. However, this model reportedly underestimates the EEDF and interface trap (N_{it}) in LDMOS devices. Some modifications of this model were reported in the literature to overcome the issues, for e.g., the Hasnat et al. [218], replaces the local electric field was replaced by a function of carrier temperature; however, still underestimating the reported N_{it} values. Reggiani et al. [219] proposed a model to represent the non-equilibrium EEDF for modeling HCD in LDMOS devices. The model is given as:

$$f_0(E, x, y) = \frac{1}{A(x, y)} \exp\left[-\alpha(x, y)\frac{\gamma(E)}{k_B T_\mathrm{e}(x, y)}\right] \tag{5.4}$$

where $A(x,y)$ and $\alpha(x,y)$ are fitting parameters, $\gamma(E)$ is the band-structure non-parabolicity which is given as:

$$\gamma(E) = \frac{E(1+\delta E)}{1+\beta E} \tag{5.5}$$

where δ and β are fitting parameters. To solve Eq. 5.4, the electron density, gradient of quasi-Fermi level, and electron mobility were obtained from TCAD as a function of the coordinate (x,y). The electron temperature was obtained following the relation:

$$T_{\mathrm{e}} = T_L + \frac{2q\tau\mu F^2}{3k_B} \tag{5.6}$$

where T_L is the lattice temperature, q is the absolute value of electron charge, τ is the energy relaxation time (∼0.35 ps for electrons and ∼0.4 ps for holes), and F is the gradient of quasi-Fermi level. The parameters $A(x,y)$ and $\alpha(x,y)$ are then obtained requiring that:

$$n(x,y) = \int_0^{E_{\max}} f_0(E,x,y)g(E)dE \tag{5.7}$$

$$T_{\mathrm{e}}(x,y) = \frac{2}{3k_B}\frac{\int_0^{E_{\max}} Ef_0(E,x,y)g(E)dE}{n(x,y)} \tag{5.8}$$

Eq. 5.4 can be numerically solved using Matlab, andthe EEDF of an LDMOS can be obtained at the channel and drift region. To improve the accuracy of the non-equilibrium distribution functions, Grasser et al. [220], proposed a model similar to that of Sonoda's [221], considering the contribution of both hot and equilibrium carriers. The model is given as:

$$f_0(E) = A\exp\left[-\left(\frac{E}{E_{ref}}\right)^b\right] + C\exp\left[-\frac{E}{k_B T_{\mathrm{e}}}\right] \tag{5.9}$$

and uses five parameters (A, E_{ref}, b, C and T_{e}) to describe the distribution function. Eq. 5.9 is solved similarly to Eq. 5.4 by obtaining the electron density, gradient of quasi-Fermi level, and electron mobility from a device simulator and then solving for the parameters. Eq. 5.9, shows good agreement with the EEDF obtained from the deterministic BTE solver based on spherical harmonics expansion, ViennaSHE [216].

While these approaches bypass the computational time and resources by modeling the distribution function analytically, they still require the location-dependent electron density, electric field, and electron mobility from a device simulator using drift-diffusion models, which may not be precise. Therefore, in this chapter, we use spherical harmonics expansion, integrated with TCAD Sentaurus, from Synopsis, for our analyses and modeling.

5.3 Calibration of the Simulation Deck

5.3.1 Calibration of the Transfer and Output Characteristics

All the experiments and simulations have been done on n-channel LDMOS devices fabricated on Silicon wafers by Texas Instruments. Inc. Two types of LDMOS devices are used in this chapter: non-LOCOS LDMOS and LDMOS, whose schematic was given in Fig. 5.1.

The breakdown voltage, V_{bd} for non-LOCOS LDMOS was ∼13 V and for LOCOS LDMOS, V_{bd} was 35 V. To facilitate high V_{bd}, the LOCOS LDMOS has a longer drift region (∼2.5 × longer than non-LOCOS LDMOS). LOCOS LDMOS also have visibly thicker oxide (∼5 ×thicker than non-LOCOS LDMOS) to achieve higher endurance to degradations. A field plate is present is present in LOCOS LDMOS to overcome the effects of high surface electric field. The gate fully covers both channel and drift regions in the two types of LDMOS.

2D simulations were carried out in TCAD Sentaurus by Synopsis, to investigate the device features in different operating conditions. A sample TCAD code for non-LOCOS LDMOS is given in Appendix. C. The carrier transport was solved using the first-order spherical harmonics expansion of the BTE. The thermal and impact ionization models were turned on to capture the device behavior. Experiments were carried out using the Keysight B1500A Semiconductor Device Analyzer and source measurement units (SMUs). As shown in Fig. 5.3, TCAD accurately reproduces both the transfer and output characteristics of the non-LOCOS and LOCOS LDMOS. The TCAD setup is now ready for further analysis.

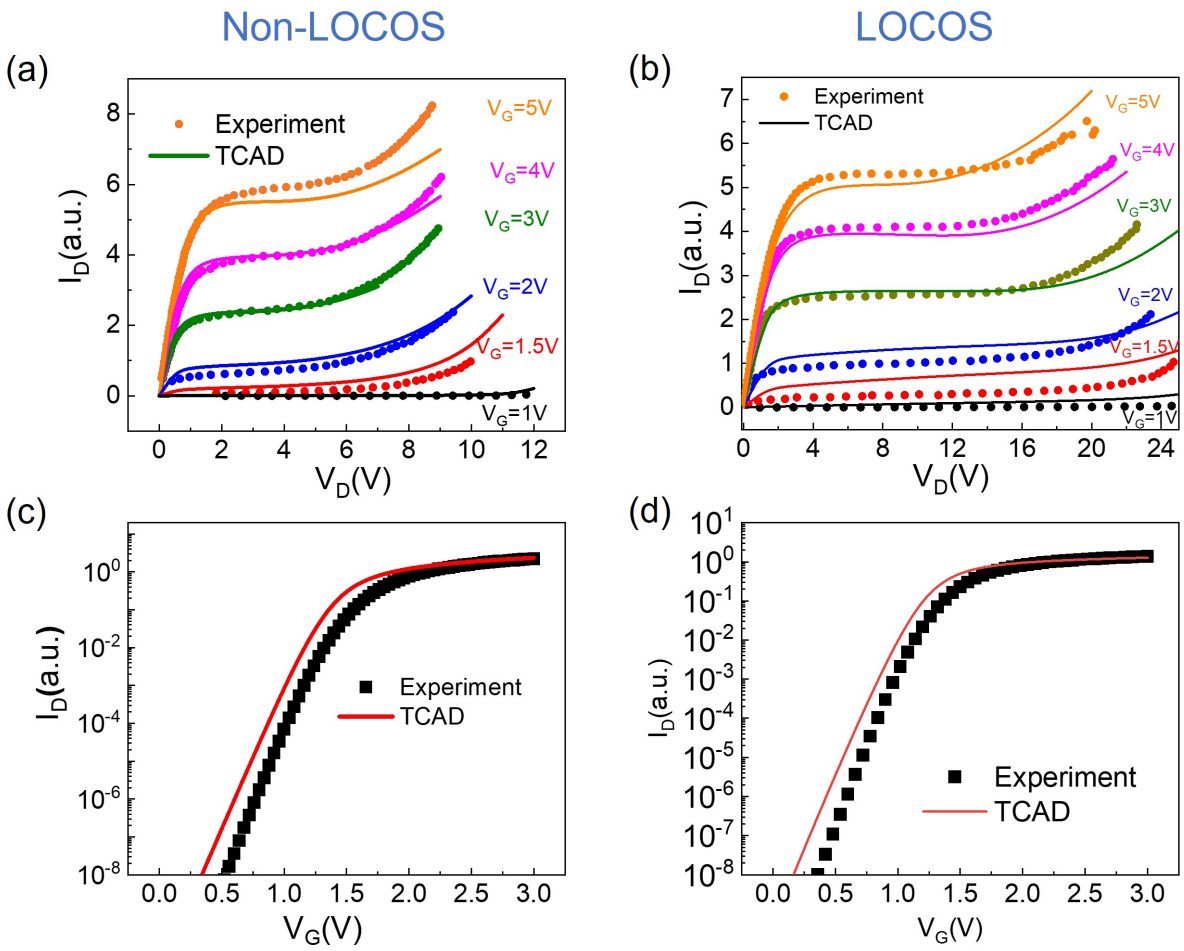


Figure 5.3. TCAD Calibration of the output and transfer characteristics of a non-LOCOS LDMOS ((a) & (c)), and a LOCOS LDMOS ((b) & (d)), respectively.

5.3.2 Device Characteristics from TCAD

Pristine device analysis by TCAD at different biases can provide insights into the 'hot spots' of degradation. For HCD, the electric field needs to be high, the electrons need to be 'hot', and there should be a high density of electrons. We, therefore, take a cutline along the Si/SiO_2 interface in a non-LOCOS and a LOCOS LDMOS to comprehend if HCD hotspots are present, as shown in Fig. 5.4.

For non-LOCOS LDMOS, the absolute electric field is higher at the drift region at low V_G ($V_D = 5$ V), and then starts redistributing in the channel and drift region at higher V_G [144].

This is because at low V_G, V_{GD} is higher, leading to a high electric field in the drift region. At high V_G, V_{GD} decreases while increasing the V_{GS}. This field redistribution depends on the device geometry and doping. At high V_D (10 V), the field increases in the drift region, which would lead to higher degradation, and hence positive voltage acceleration in HCD. The electron density, decreased slightly at a higher V_D, as seen from 5.4.

The electron temperature, calculated from the spherical harmonics expansion, peaks at the drift/drain corner at high V_D, marking the hotspot for HCD at high V_D. From TCAD 2D profiles, it was found that the maximum electron temperature at a certain V_G, V_D occurs slightly below the interface in bulk. From this analysis, two distinct hotspots for HCD was identified for a non-LOCOS LDMOS: one in the drift for low V_G, High V_D, and one in the channel region for high V_G, High V_D. Chapter 4 reached a similar conclusion in a non-LOCOS LDMOS, using a phenomenological approach.

The analysis of LOCOS LDMOS is much complicated than a non-LOCOS device, as shown in Fig 5.4. A longer drift region leads to a higher V_{bd}, but it also gives rise to additional complexity in the device characteristics. At low V_D (5 V), the LOCOS device, essentially behaves like a non-LOCOS device, with the peaks of electric field switching between the channel and the accumulation region depending on the V_G bias. However, when a high V_D (25 V) is applied, the electric field at the end of the LOCOS dominates and becomes the primary hotspot for HCD in the device. The electron density is orders of magnitude lower compared to the non-LOCOS device, because the inversion is formed much below the interface, into the bulk. The electron temperature follows the electric field profile, and a discernable peak is observed at the end of the LOCOS. An overall reduction in electric field, electron density is observed in non-LOCOS LDMOS, compared to LOCOS. However, at the same time strong localization of large electric fields are observed in LOCOS LDMOS, which may balance out the advantages of lower electric field. Interestingly, higher V_G gives rise to a higher peak in the electric field, electron density, and electron temperature, indicating a positive voltage acceleration of HCD. Therefore, although three different hotspots of degradation are identified in the LOCOS LDMOS, in practice, two hot spots (channel and accumulation (or at the beginning of LOCOS)) will be active at a low/high V_G, low V_D and only one hotspot (at the end of LOCOS) will dominate the device degradation at a low/high V_G, high V_D.

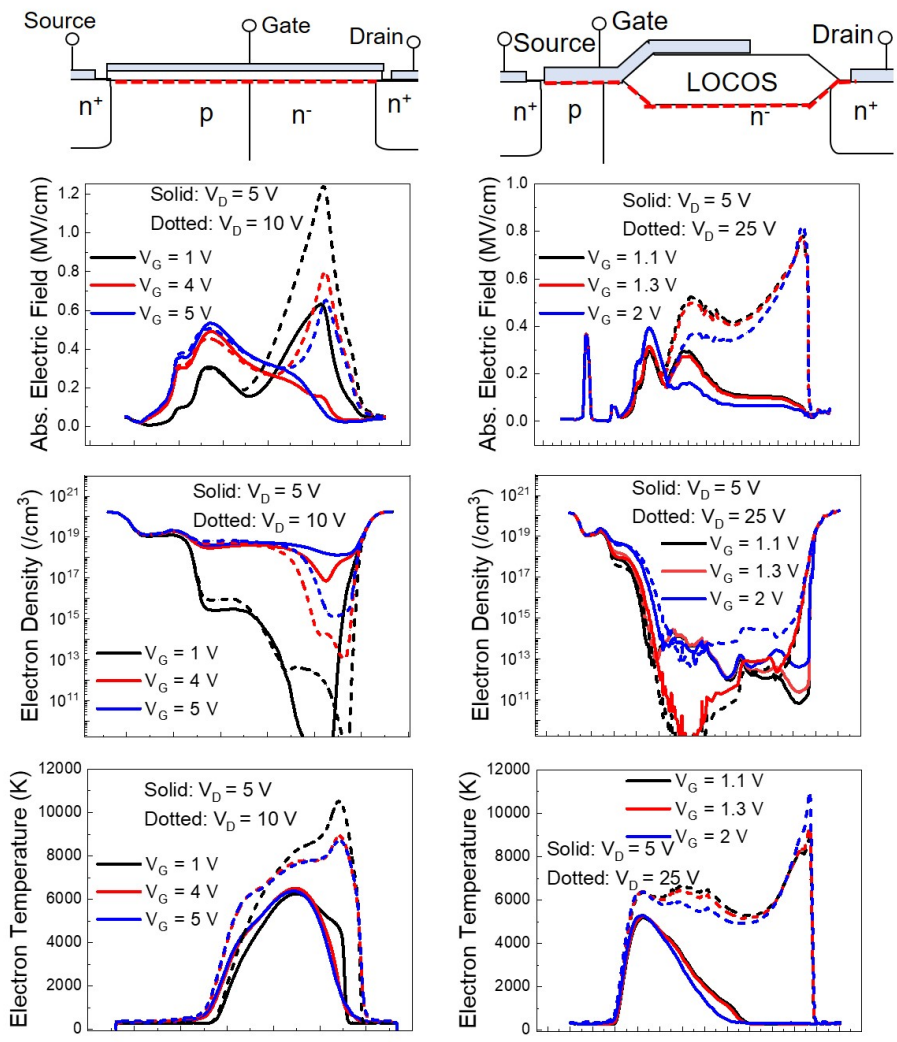


Figure 5.4. Cutline plots for absolute electric field (MV/cm), electron density (cm^{-3}), and electron temperature (K) at the Si-SiO_2 interface, obtained from TCAD for a non-LOCOS LDMOS and a LOCOS LDMOS.

The effect of these hotspots can be easily seen in the EEDF of the pristine devices. For non-LOCOS LDMOS, at low V_G, low V_D (5 V), the T_e for majority of the electrons in the channel region, calculated from the slope of EEDF, is slightly above 300K (Fig. 5.5 (a)), however at high V_G, low V_D the electrons start getting heated (Fig. 5.5 (c)). Fig. 5.5 (b) shows that the drift region has hotter electrons than the channel region due to a higher electric field. Although the electrons in the channel region are relatively insensitive to the

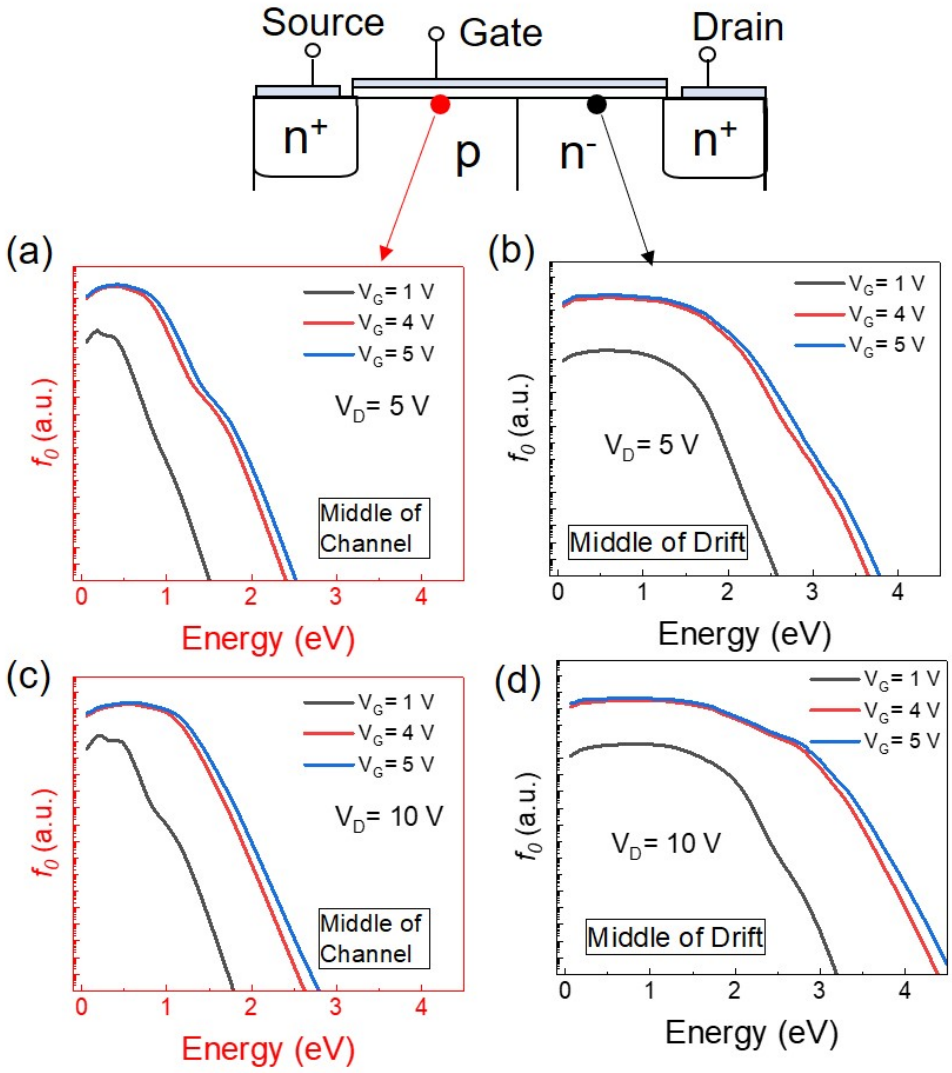


Figure 5.5. EEDF of the non-LOCOS LDMOS. EEDF of a selected point in the middle of the channel at (a)low V_D (5 V) and (c) high V_D (10 V). EEDF of a selected point in the middle of the drift at (b)low V_D (5 V) and (d) high V_D (10 V).

increases in V_D, a significant number of electrons in the drift region get very hot at high V_G, high V_D (Fig. 5.5 (d)).

The EEDF of various points in a LOCOS LDMOS is shown in Fig. 5.6. For low V_D (5 V), the electric field peak is in the accumulation region (or at the beginning of the LOCOS), as seen in Fig. 5.4. This gives rise to hot electrons in that region, as shown in Fig. 5.6. The electrons in all other points (middle of the channel, middle of LOCOS, and end of

LOCOS) are relatively colder with temperature, $T_e \sim 300$K, as calculated from the slopes of the EEDF. When a high V_D (25 V) is applied, the T_e remains similar for electrons in the channel and the accumulation region, but the electrons near the end of the LOCOS become dramatically hot, and dominates the degradation mechanism. Therefore the EEDF analyses take a deeper look into the electron ensemble characteristics as foreseen by the cutline profiles while providing a solid framework for the understanding of the physical mechanism of HCD in a non-LOCOS and LOCOS LDMOS.

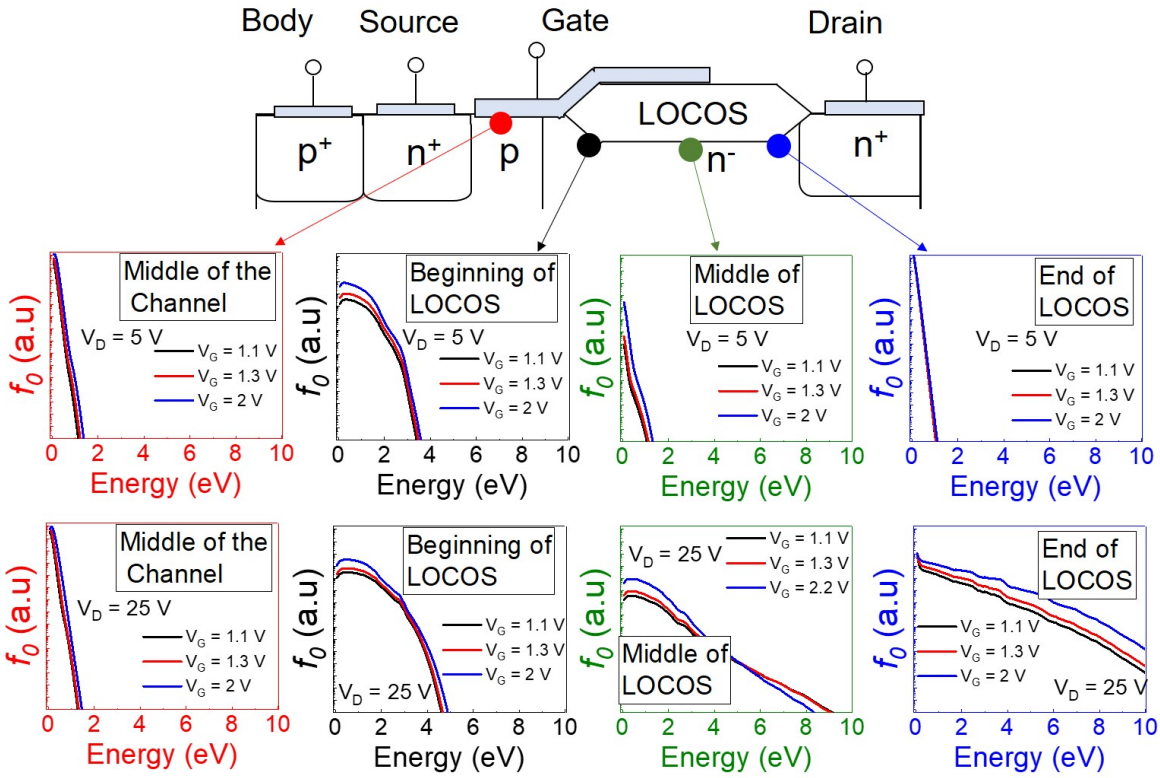


Figure 5.6. The EEDF profiles of various selected points of LOCOS LDMOS.

5.4 TCAD Modeling of Hot Carrier Degradation

HCD is attributed to the interface defects due to various applied bias. In the previous section, we have identified the driving forces behind defect formation. In this section, we will first subject the devices to HCD experiments, and then use TCAD to model the degradation to gain additional insights.

5.4.1 Hot Carrier Degradation Experiments

The electrical stress experiments for HCD were done by programming Keysight B1500A Semiconductor Device Analyzer for the non-LOCOS and LOCOS LDMOS. Source measurement units (SMUs) were used to perform the stress and the current-voltage sweeps. All the HCD experiments were carried out at room temperature and in a DC stress-measure-stress (SMS) pattern. In the I_D - V_G measurement phase, the drain bias V_D is set as 0.1 V while sweeping the gate bias, V_G. The linear drain current $I_{D,lin}$, is defined at $V_G = 5$ V. The stress V_D and V_G was selected depending on the device under test. The data collected was analyzed using Matlab and HCD parameters, such as $\Delta I_{D,lin}(\%)$, $\Delta V_{th}(\%)$ etc., were extracted.

5.4.2 Hot Carrier - Safe Operating Area

Doing the HCD experiments in a device is extremely time-consuming ($>$ 1000 seconds of stress for each device) and expensive. One has to measure multiple identical devices at various combinations of V_G and V_D , in order to predict the lifetime. While one of the most powerful approaches to avoid this labor-intensive work is to obtain the universal scaling of degradation as shown in Chapter 4, the other way is to construct the hot carrier-safe operating area (HC-SOA), from a series of stress experiments at various V_G and V_D. Another way to obtain HC-SOA is to do HCD in a few but wide variations of V_G and V_D, and then calibrate the experiments with a suitable degradation model in TCAD. Once calibrated at a wide range of V_G and V_D, the model becomes predictive and can be used to generate the degradations at desired combinations of V_G and V_D to acquire the HC-SOA. However, the TCAD approach has some challenges, which will be discussed in Sec. 5.4.5.

Generally, the SOA in LDMOS devices can be broadly classified into short-term SOA and long-term SOA [135]. The short-term SOA usually involves catastrophic device failure mechanisms [222] like impact ionization and thermal runaway, while HC-SOA [134] falls into the long-term SOA category. A common procedure to plot the HC-SOA is to measure degradation at various V_G and V_D and extrapolating to find the time taken for a predetermined amount of degradation (generally 10% of the pristine device [134]).

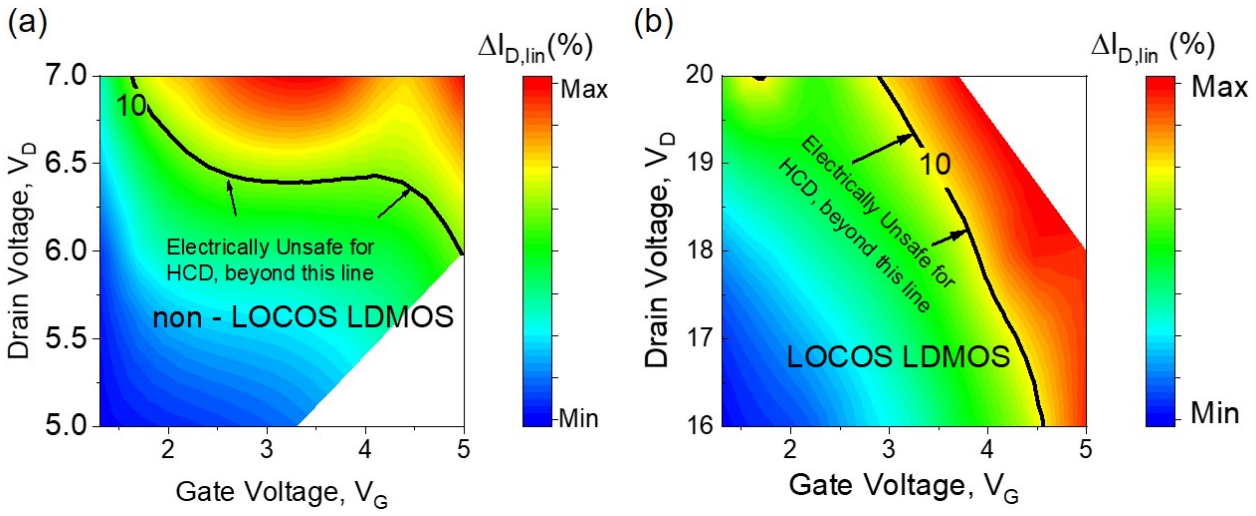


Figure 5.7. Experimentally measured HC-SOA, obtained by monitoring $\Delta I_{D,lin}(\%)$ for (a) non-LOCOS LDMOS and (b) LOCOS LDMOS, after stressing for an arbitrary time.

Here, we will monitor the $\Delta I_{D,lin}(\%)$ of non-LOCOS and LOCOS LDMOS for 10 (%) degradation, but refrain from any extrapolation because of the complicated interdependencies of the hotspots and applied biases, as described in the previous section. As seen from Fig. 5.7, the HC-SOA of non-LOCOS LDMOS exhibits a non-linear dependence on the V_G and V_D, whereas the LOCOS LDMOS demonstrates a monotonous dependence. This is because, in a non-LOCOS LDMOS, the electric field redistributes itself, and depending on the applied bias and stress time, either the channel or the drift region dominates the degradation, leading to a multi-hotspot feature in the HC-SOA. On the other hand, in a LOCOS LDMOS, at sufficiently high V_D, only one hotspot, located at the end of the LOCOS, dominates the degradation. Therefore, the HC-SOA experiments concur with the insights gained from the TCAD simulation of the pristine device. The TCAD will be used to model the HCD parameters as demonstrated in the next section.

5.4.3 TCAD Modeling

Although HCD has been researched over a few decades, the exact nature and role of hot electrons and holes, in the degradation of high voltage transistors is still being discussed.

This is partly due to the varying geometries and doping profiles of high voltage transistors depending on the applications and partly due to their inhomogeneous implantation in device simulators (e.g. TCAD Sentaurus). One of the most popular models of HCD, implemented on TCAD, is based on the solution of the reaction-drift-diffusion kinetic equation. The reaction model is based on Arrhenius approximation and empirically depends on electric field and hot electron/hole densities. With the implementation of the spherical harmonics expansion of the BTE [203] in TCAD, the reaction model can predict the degradation of STI LDMOS in various stress conditions. While attempts have been made to include the 'drift' part of the model in the degradation kinectics [223], it is currently not implemented in TCAD for robust LDMOS simulations. In this chapter, the reaction model, popularly known as the Hot Carrier Stress (HCS) degradation model, based on the research by Reggiani et al. [191], will be used for modeling, and the reservations will be discussed. The different mechanisms of bond breakage in this model is based on the works in Refs. [194], [224], [225].

From MOS degradation kinetics, the interface trap generation in a transistor is given as [226]:

$$\frac{dN_{it}}{dt} = k_f(N_0 - N_{it}) \tag{5.10}$$

where N_{it} is the interface trap concentration, N_0 is the total number of interface bonds available, t is the stress time, and k_f is the forward reaction rate. Solving the differential equation, we get:

$$N_{it} = N_0(1 - \mathrm{e}^{-k_f t}) \tag{5.11}$$

Eq. 5.11 gives the number of interface traps generated when a transistor is stressed for a certain time, t. The forward reaction rate, k_f depends on the bond energy, which was assumed to be discrete here. However, it was later determined that a continuous distribution characterizes the activation energies in a transistor [176]–[178], [227]. Therefore, both the interface traps and reaction rate becomes functions of bond energy. A distribution, $g_A\ (E)$, obtained by derivative of the Fermi functions, is given as [228]:

$$g_A(E) = \frac{N_0}{\sigma} \frac{\mathrm{e}^{-(E-E_{AV})/\sigma}}{(1 + \mathrm{e}^{-(E-E_{AV})/\sigma})^2} \tag{5.12}$$

where E_{AV} and σ are the mean and standard deviation of the energy distribution. The reaction rate is given as:

$$k_f(E) = k\mathrm{e}^{-\frac{E-E_{AV}}{k_B T_\mathrm{e}}} \tag{5.13}$$

The interface trap concentration then becomes:

$$N_{it} = N_0 \int_{E_{AV}-m\sigma}^{E_{AV}+m\sigma} g_A(E)\left(1-\mathrm{e}^{-k_f(E)t}\right)dE \tag{5.14}$$

The HCD has since been described as a resultant of two competing processes: single-particle (SP) and multiple-particles (MP). Individual contributions of SP and MP to the N_{it}, can be calculated using models described in [194], [225], [229]. The reaction rate for both the processes is given as:

$$k = \int_{E_{SP/MP}}^{\infty} f_0(E)g(E)u_g(E)\sigma(E)dE \tag{5.15}$$

where $f_0(E)$ is the EEDF, $g(E)$ is the density of states, $u_g(E)$ is the group velocity, and $\sigma(E)$ is the capture cross-sections for the SP and MP processes. A Keldish-like formulation was used to model the capture cross-section, which is given as [230]:

$$\sigma(E) = \sigma_0 \left(\frac{E-E_{SP/MP}}{k_B T}\right)^{p_{SP/MP}} \tag{5.16}$$

where $p_{SP/MP}$ is the exponent characterizing SP and MP and σ_0 is a fitting parameter. The total interface trap formation is therefore given as:

$$N_{it,total} = N_{it,SP} + N_{it,MP} + N_{it,TE} \tag{5.17}$$

where $N_{it,SP}$ is the N_{it} due to SP process, $N_{it,MP}$ is the N_{it} due to MP process, and $N_{it,TE}$ is the thermally generated N_{it}. This model is implemented in TCAD, with the parameters (probability of SP/MP process, capture cross-sections of SP/MP, etc.), subjected to fitting for a particular device.

5.4.4 TCAD Calibration

The Hot-carrier stress (HCS) degradation model was implemented in a 2D simulation deck for both non-LOCOS and LOCOS LDMOS. The transport models were kept similar to the initial calibration. The generated N_{it} was assumed to be acceptor-like. Although there are about 25 parameters are available to be calibrated, so that the model matches the experiments, only 8 parameters (maximum number of interface bonds N_0; activation energy for the SP and MP process, E_{SP}, E_{MP}; fitting parameter for SP and MP process, σ_{SP}, σ_{MP}; exponents characterizing the SP and MP process, p_{SP} and p_{MP}; and activation energy for the thermal process, $E_{TH,0}$) were found to have a significant effect. The calibration of the HCS degradation model with HCD experiments in non-LOCOS and LOCOS LDMOS should be done in a way so that a same set of parameters can be used to match the degradation in both of the devices. From the experimental $\Delta I_{D,lin}$ curves in Fig. 5.8, it was found power-law exponents varied from ∼0.7 to ∼0.1 and from ∼0.5 to ∼0.2 for the LOCOS and non-LOCOS LDMOS, respectively. Despite the different geometry, exponents, and range of applied bias, it was determined that the SP process is the dominant degradation mechanism in both the LDMOS devices, and the calibration can be achived by varying only two parameters (out of the 25!) in both the devices. A similar analysis by Tallarico. et al. [189], also found that SP process is the dominant physical mechanism of degradation in LOCOS LDMOS devices. The calibration is shown in Fig. 5.8.

Once the calibration is obtained at multiple voltages, as in Fig. 5.8, the underlying mechanisms can be studied. One can monitor the change in the electric field around the LOCOS edges, electron temperature, electron mobility, current density, etc. with increasing stress time at different V_G and V_D from TCAD [219].

Along with predictive modeling of degradation, perhaps the most crucial advantage that TCAD provides is the ability to monitor interface trap generation at any given coordinate, with stress time. This is shown in Fig. 5.9. In the non-LOCOS LDMOS, we monitor the N_{it} in the drift and the channel. The ΔN_{it} in the drift region is higher for both V_G and V_D combination in this case. This is because of the higher electric field, electron density, and electron temperature in the drift region, as shown in Fig. 5.4. The ΔN_{it} in the channel

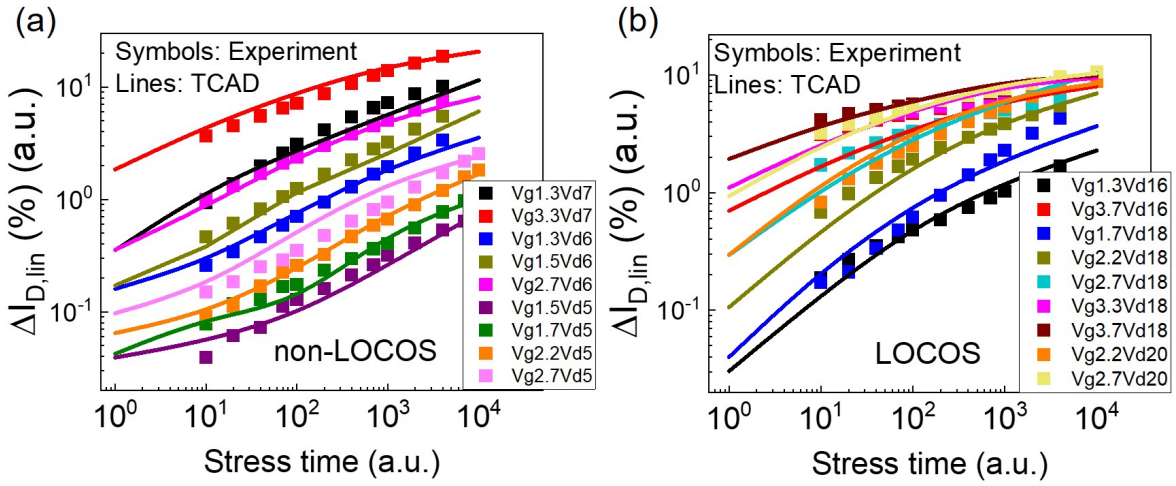


Figure 5.8. TCAD Calibration of $\Delta I_{D,lin}(\%)$ using HCS degradation model in TCAD, for (a) non-LOCOS LDMOS and (b) LOCOS LDMOS.

region is orders of magnitude smaller than that of the drift region at low V_G (1.5 V). However with increasing V_G, ΔN_{it} in the channel region also increases. This was phenomenologically determined in the previous chapter, using universal scaling curve.

For the LOCOS LDMOS, the ΔN_{it} in the beginning of the LOCOS region is much higher than at the end of the LOCOS at $V_G = 1.3$ V, and $V_D = 16$ V. However, as we increase the V_D to 20 V, dramatic change in the ΔN_{it} at the end of the LOCOS region is found. This was anticipated from the profiles of the electric field, electron density, electron temperature and EEDF earlier in this chapter, but now the evolution of ΔN_{it} with stress-time can be visualized, from the HCS degradation model.

5.4.5 Challenges Associated with TCAD Modeling of Hot Carrier Degradation

Some of the challenges and pitfalls associated with TCAD modeling of HCD are listed here, as follows:

(a) **Fitting parameters may not be unique**: One should proceed with caution while reporting ΔN_{it} of a specific location, because this procedure of determining ΔN_{it} at the interface is based on fitting, and the fitting parameters may not be unique for a device. While a specific combination of values of the model parameters was used to fit the experimental

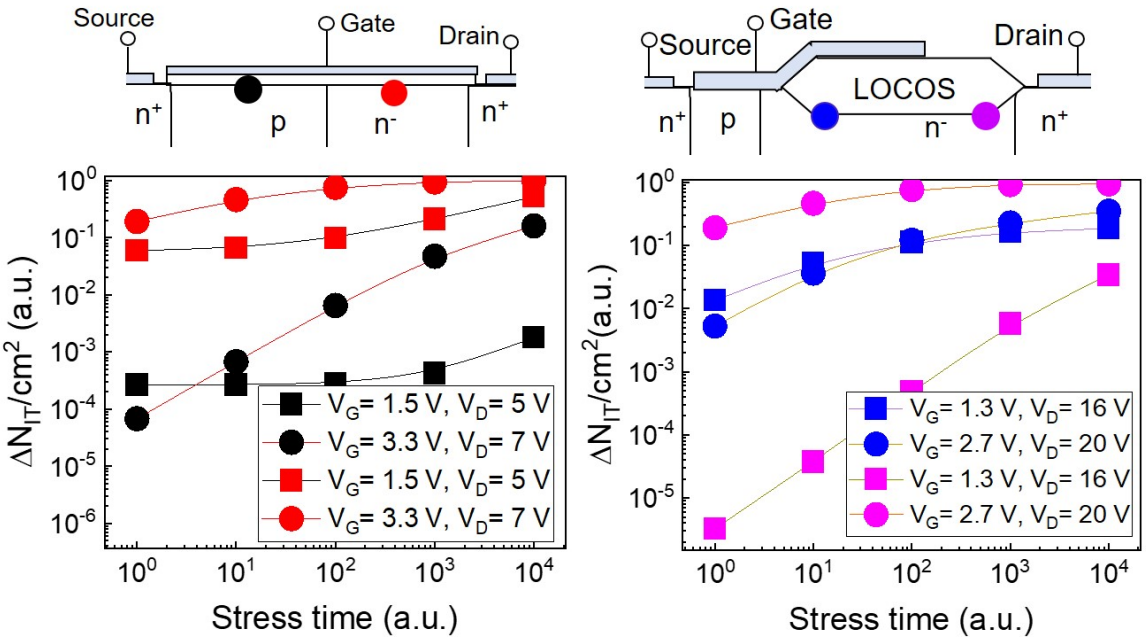


Figure 5.9. Interface trap determination, at various points in non-LOCOS and (b) LOCOS LDMOS.

curves in Fig. 5.8 (Fitting I), an entirely different, but close, set of combinations can also be used for fitting (Fitting II). It is possible that several other sets of parameters can be used to calibrate the data. It is entirely up to the user to determine the best fitting.

Fitting I and II is shown in Fig. 5.10. While both sets of values calibrate the experimental data quite well, the derived ΔN_{it} and other parameters which are determined by post-processing will be different. We monitor the ΔN_{it} at the beginning, the middle, and the end of the LOCOS, at simulated 10000 s of stress (Fig. 5.10 (c)). We find that the values of ΔN_{it} are different, but the overall trends are similar in both cases. Therefore, although TCAD can anticipate the pristine and stress device parameters and the trends of ΔN_{it} very well, the exact values of ΔN_{it} maybe derived differently by various users for the same device and will require additional experimental validation. One such approach of determining N_{it} experimentally, is known as charge pumping.

Despite a plethora of techniques in the literature (e.g., DCIV [231], charge-capacitance [232] etc.), the original charge pumping technique, demonstrated by Burgler and Jespers in 1969 [233], still remains one of the most powerful techniques for characterizing and spatially-

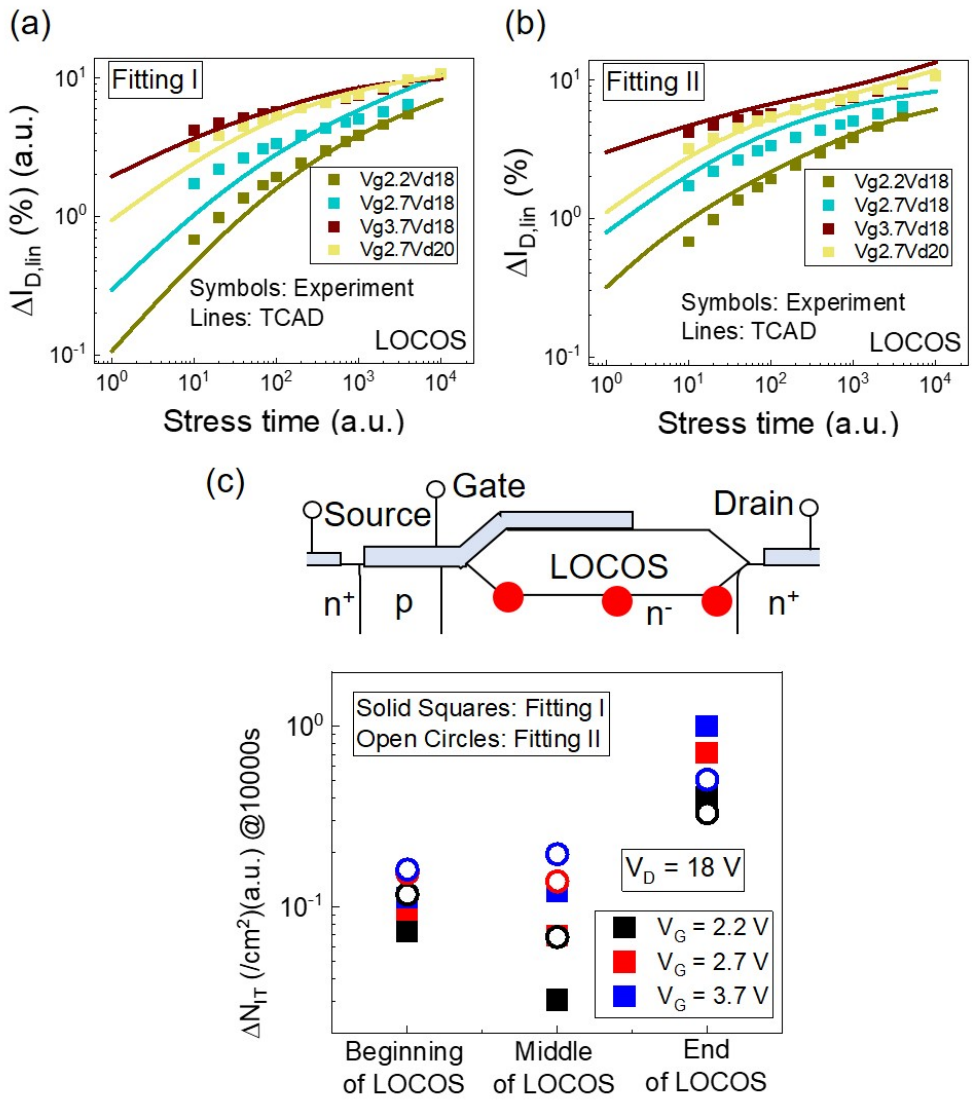


Figure 5.10. Fitting of the experimental degradation curves using two different sets of parameters (a & b). (c) The ΔN_{it} values determined from two fittings appear to vary, but with similar trends.

profiling N_{it} in a MOSFET. The charge pumping technique is based on the simple idea that when a periodic pulse is applied at the gate of a MOSFET (with the source and drain grounded), a DC substrate current (I_{CP}), proportional to N_{it}, gate area, and frequency, can be measured from either the source/drain or the body contact due to the recombination of majority and minority carriers at the device interface. The increase in I_{CP} of a stressed device can be used to quantify the time-evolution of N_{it}. For the LDMOS devices, charge pumping

technique faces two challenges: (a) This technique cannot be used if the body contact does not exist (as in floating body devices) or if the body contact is tied to source contacts. (b) The threshold voltage (V_{TH}) and flatband voltage (V_{FB}) needs to be determined precisely along the channel, to ensure that the applied gate pulse can pump sufficient majority and minority carriers. Unlike a classical MOSFET, V_{TH} and V_{FB} varies spatially from the channel (p-type) to drift (n-type) in an LDMOS [188]. Therefore, a novel CP technique, named Super Single Pulse CP (S^2PCP) Technique (not discussed in this thesis), has been developed to resolve N_{it} Independently in the channel and the drain region. As shown in Fig. 5.11, S^2PCP measurements in the non-LOCOS LDMOS confirms the fact that at low V_G, high V_D, the ΔN_{it} at the channel region is much lower than that of the drift region but at high V_G, high V_D, ΔN_{it} at the channel regions increase rapidly. It is to be noted that a direct point-by-point comparison of ΔN_{it} obtained TCAD and S^2PCP technique is not possible because S^2PCP can only determine the average ΔN_{it} of the specific region. Nonetheless, the TCAD simulations are experimentally validated with the S^2PCP technique, thus providing not only the physical mechanism responsible for HCD but also a method to determine how crucial parameters (ΔN_{it}, electron temperature, etc.) evolve temporally.

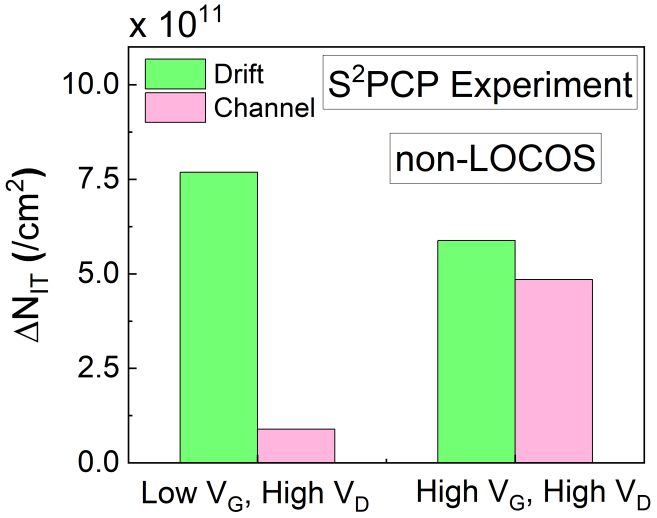


Figure 5.11. Determination of ΔN_{it} in the channel and the drift region, using S^2PCP Technique.

(b) **Limited validity of the model**: The second big challenge associated with TCAD is the bias range in which the degradation models are valid. The presence of ΔN_{it} in the channel has now been confirmed by both TCAD and S^{2}PCP experiments, but one wonders, if the ΔN_{it} in the channel can physically lead to HCD in the channel as well as the drift region. The previous chapter establishes the universal scaling in LDMOS by deconvolving the degradation in the channel and the drift region, but universal scaling is a theory of N_{it}, not of HCD specifically. Moreover, the electron temperature plots (not shown here) show only one peak, and it is in the drift region, even at high V_G,V_D. *So, there is a possibility that* ΔN_{it} *is generated due to mechanisms other than HCD.* Therefore, even though it might be possible to fit the parametric degradation curves ($\Delta I_{D,lin}(\%)$, $\Delta V_{th}(\%)$, etc.) using TCAD, it remains to be seen if it makes sense physically.

A couple of experiments were done to confirm the origin of N_{it} in the channel region of the non-LOCOS LDMOS, as shown in Fig. 5.12. Electrons can be injected into the SiO_2 at sufficiently high V_{GS}, and generate defects. This is known as the Fowler-Nordheim (FN) stress [234]. When FN Stress is applied, by setting V_{GS} to high, while grounding the drain contact, the ΔV_{th} degrades with stress time. The HCD degradation at the same V_{GS}, but high V_{DS} ($V_{DS} = V_{GS}$), is more than an order of magnitude higher, suggesting that the percentage of degradation in LDMOS, due to pure FN, in that applied bias, is modest. On the other hand, a reversal in gate current is detected at increasing V_D, suggesting the presence of an additional mechanism, other than pure HCD. If the electrons are able to tunnel through the oxide, they can drop down and initiate impact ionization in the poly-Si, producing high energy carriers to induce defect in the Si/SiO_2 interface. This phenomenon is known as Anode Hole Injection (AHI). [235]. Therefore, at high bias, the degradation in LDMOS might also have contributions from FN stress and AHI mechanisms [236]. These phenomena are not implemented along with the HCD degradation models in TCAD and hence will be impossible to detect. Therefore TCAD modeling is very helpful in predicting degradations at low V_G, high V_D, as shown in this chapter, but caution should be exercised when projecting the values to high V_G, V_D. This is why the HC-SOA, discussed in the previous section, may not be precise if determined by TCAD. The complete deconvolution of all the degradation

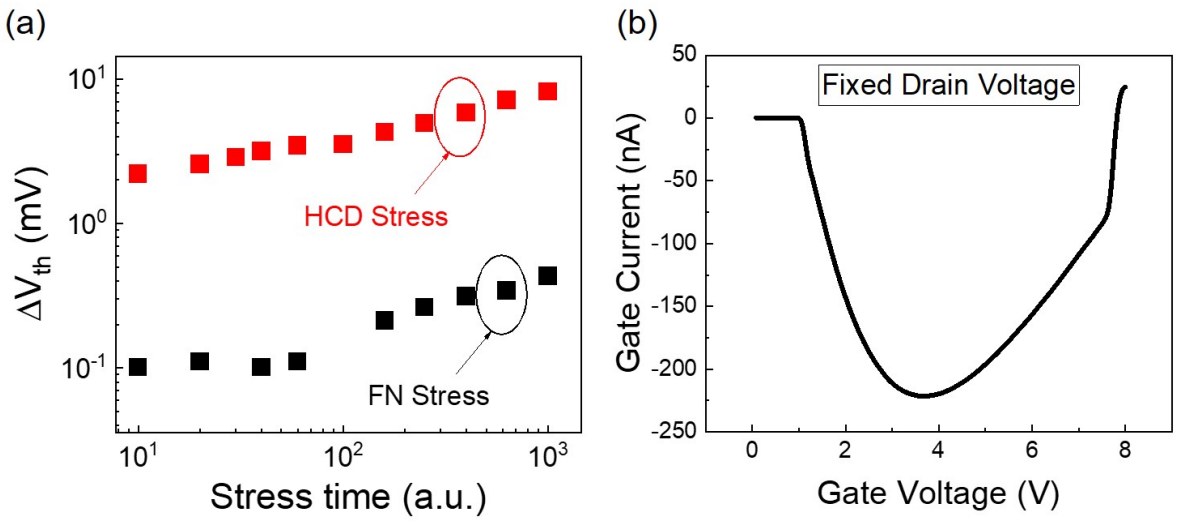


Figure 5.12. (a) Degradation due to FN stress and HCD stress in a non-LOCOS LDMOS. (b) Measured gate current at a fixed drain bias and varying gate bias.

phenomena in LDMOS at high biases, will require multiple experiments and modeling, which is beyond the scope of this thesis.

(c) **Convergence Issues**: Another challenge associated with TCAD modeling is that of convergence. Many times, this could be a numerical issue with the solver used. One can still follow the following approaches to converge TCAD simulations faster. The first approach is to change the mesh (fine or coarse) because the meshing controls the critical regions where the maximum fields are generated. A second suggestion is to switch off the temperature equations in the 'Solve' section, as the temperature may oscillate between very close values and give numerical issues to the solver. In addition, one can switch off the avalanche generation to improve the convergence. However, one must be careful and ensure that the effects like self-heating, or electron hole-pair generation, do not significantly influence the degradation before turning off the temperature and avalanche generation. One can also set the spherical harmonics expansion to a 'frozen' state so that the distribution is not updated at every point of the grid but needs to be cautious because errors can get introduced in the process. Therefore, in a nutshell, implementing TCAD to study the HCD and pristine characteristics

of a complicated device like LDMOS is very useful; however, one needs to be careful and be aware of the limitations of TCAD.

5.5 Summary

We have explored the physics behind the HCD mechanisms in non-LOCOS and LOCOS LDMOS using experiments and TCAD. The findings has been summarized below:

(a) Proper modeling of HCD requires monitoring the electron distribution as they travel from the source to the drain, under the influence of the electric field. Using spherical harmonics expansion in TCAD, the EEDF has been monitored at different locations in the both the LDMOS. Using TCAD, it was determined that non-LOCOS LDMOS has two hotspots (channel and drift) for HCD depending on the applied bias.

(b) While LOCOS LDMOS has three hotspots (channel, accumulation, and the end of LOCOS), the hotspots in the channel and accumulation are triggered at low V_G, low V_D, while the hotspot at the end of the LOCOS completely dominates the degradation at high V_G, high V_D. These characteristics of the hotspots also influence the HC-SOA.

(c) TCAD can also model the degradation at various V_G, V_D. By calibrating the experimental data, TCAD presents an opportunity to monitor various device parameters (e.g., N_{it}, electron temperature), which were otherwise difficult to comprehend. However, one must be careful with TCAD, because there are multiple fitting parameters with no unique set of solutions. Therefore, the post-parameters must be validated with experiments, if possible.

(d) Other challenges of TCAD include the possible deviation from pure HCD degradation to a combination of HCD, FN/PBTI, and AHI for LDMOS, which are not captured in TCAD. Therefore, although very helpful to determine the physical mechanisms behind the degradations, and predict degradations at arbitrary combinations of applied biases, the outcomes of TCAD, should be validated with experiments whenever possible.

Thus we have discussed all the advantages and pitfalls of modeling HCD using TCAD for LDMOS devices in this chapter.

6. CORRELATED EFFECTS OF RADIATION AND HOT CARRIER DEGRADATION ON LDMOS

6.1 Introduction

Commercial power transistors are ubiquitous in almost every automated process or application that controls and converts electric power in the industry (agriculture, automotive, etc.), home (refrigerator, microwave, etc.), or personally owned devices (e.g., cell phone charger). One of the most commonly used silicon-based power transistors is Lateral Double Diffused MOS (LDMOS). These transistors are often used in appliances or products, where they are subjected to high amounts of radiation (> 1 Mrad (Si) [85]), such as buck DC/DC converters for ATLAS detector at the Large Hadron Collider at CERN [237], space shuttles [238], and so on. The cumulative effects of such radiation exposure (i.e., Total Ionizing dose, TID) may lead to parametric degradation and functional failure [91]. Regarding TID, the most vulnerable part of a transistor is the insulator, where the electron-hole pairs are created as a consequence of the deposited radiation energy. It is presumed that under applied bias, the radiation-generated electrons are swept away quickly, but the holes linger in the oxide, owing to their low mobility, and hops towards the oxide/semiconductor interface. Some of the holes are trapped in the oxide as fixed charges, and the proton liberated during the transport may generate interface traps, which causes reliability issues. Fortunately, the oxide thickness in modern logic devices is below a couple of nm, leading to negligible TID effects [85], however, power transistors, such as the LDMOS, have thicker oxides (>10 nm) to sustain higher voltage bias. Naturally, these thick oxides remain vulnerable to TID.

Radiation is not the only concern for LDMOS. Due to it's operation at high bias, hot carrier degradation (HCD) is one of the most common reliability phenomena in LDMOS devices [2]. While several phenomenological [134], [239], and physics-based models [143], [183], [240] of HCD degradation of LDMOS have been proposed and validated over the years, the accuracy of those models in the presence of radiation has been rarely vetted. The generation of oxide traps and 'extra' ΔN_{it}, during radiation, could alleviate or exacerbate HCD degradation. This assessment is vital because, once the transistors are deployed in a high-radiation environment, it might be dangerous and sometimes impossible to replace

them. Therefore, we must modify the HCD models to explicitly account for radiation events and develop HCD-TID accelerated tests to prevent surprises and costly failures.

We can assess the combined degradation of an LDMOS in the presence of TID by quantifying the generation of oxide traps (ΔN_{ot}) and interface traps (ΔN_{it}) created during the radiation exposure. The trap concentration may be obtained by interpreting the time-dependent shifts of the I-V characteristics of the stressed devices. Other advanced techniques can be used as well. Although the original charge pumping (CP) technique developed by Burgler and Jespers [233] remains one of the most potent techniques for profiling $N_{it}(x)$ in a MOSFET, the complicated geometry of LDMOS requires that the technique be modified. Super Single Pulse Charge Pumping (S^2PCP) technique [106], [187] is a novel modification of the original CP technique, which can quantify N_{it} in the channel and drift region of an LDMOS. In this chapter, S^2PCP is employed to measure not only ΔN_{it} but also ΔN_{ot} after the radiation exposure.

The correlation between HCD and TID effects in a practical scenario is complicated: the LDMOS may be exposed to radiation throughout its lifetime but experience HCD when turned ON for a short time during circuit;operation, or the LDMOS may be ON the whole time, but receive intermittent radiation. To emulate these scenarios, two experimental setups (HCD followed by TID, $HCD \rightarrow TID$; and TID followed by HCD, $TID \rightarrow HCD$) were analyzed for both non-LOCOS and LOCOS LDMOS.

This chapter is arranged as follows: Sec. 6.2 describes the experiment setup. Sec. 6.3 investigates the width dependence of LDMOS on radiation through various device characteristics. This section also shows that the S^2PCP technique can be used to quantify the oxide traps and estimate the ΔV_{TH}. Sec. 6.4 demonstrates the correlation between HCD and TID. We analyze two sets of experiments ((a). TID followed by HCD; (b). HCD followed by TID) to study the correlation of TID and HCD. Sec. 6.5 attempts to obtain the universal scaling of HCD after the device exposure to TID. Overall, this chapter presents a generalized reliability framework to quantify the impact of radiation on LDMOS transistors by considering the correlation of defects created by electrical stress and radiation from extra-terrestrial sources.

6.2 Experimental Setup

Two types of n-channel LDMOS transistors (non-LOCOS and LOCOS) were subjected to electrical bias and stress at different combinations of V_G and V_D at room temperature. Schematic of non-LOCOS and LOCOS LDMOS is shown in Fig. 6.1. Several devices of widths 2 - 100 μm, were measured to study the device-width dependence of the impact of radiation. The electrical characteristics, stress experiments, and measurements were carried out using the Keysight B1500A Semiconductor Device Analyzer, where $I_D - V_G$ sweeps were carried out using the source measurement units (SMUs). The bias conditions for I_D–V_G

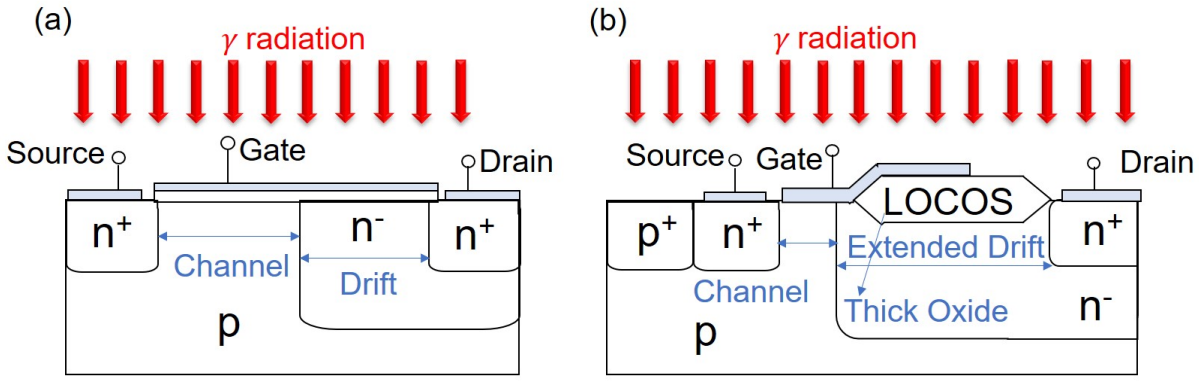


Figure 6.1. Schematic of (a) non-LOCOS and (b) LOCOS LDMOS, exposed to γ radiation.

sweeps were: V_D = 0.1 V and V_G = 0 – 5 V in steps of 50 mV. The LDMOS devices were subjected to gamma radiation using a Co-60 source at Purdue University, with a dose of 70 rad/min. The devices were exposed for several days to acquire a TID of 0.1, 0.5, 0.6, 1.2, and 1.8 Mrad (Si). All electrical properties were characterized immediately before and after the irradiation. To investigate the correlation of HCD and TID, two cases were considered: (i) TID followed by HCD ($TID \rightarrow HCD$), as in Fig. 6.2(a). (ii) HCD followed by TID ($HCD \rightarrow TID$), as in Fig. 6.2(b).

6.3 Impact of Radiation in LDMOS Device Geometry

To study the correlation between radiation and HCD in LDMOS transistors, it is important to explore the effect of radiation on a pristine transistor and see if there is any

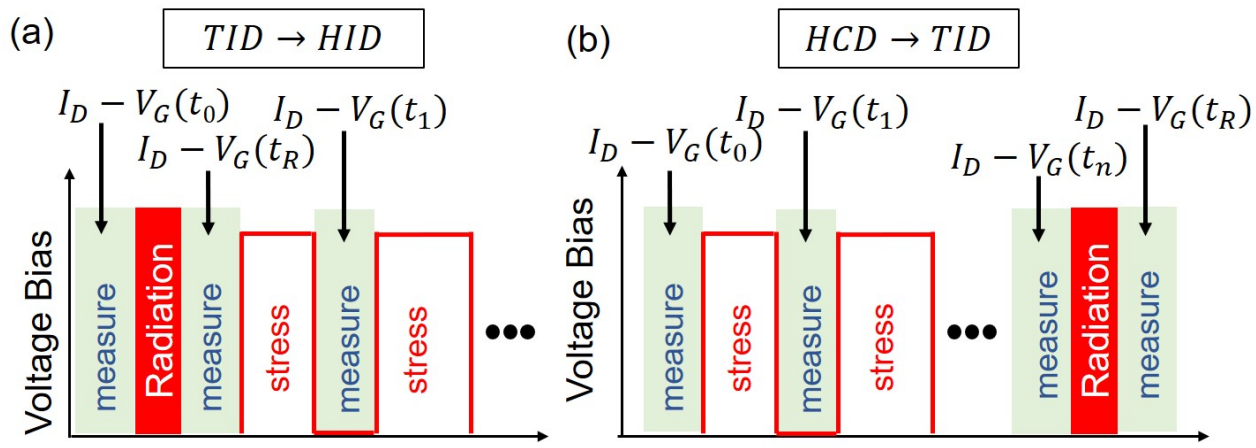


Figure 6.2. Experimental setups (a) TID followed by HCD (b) HCD followed by TID. $I_D - V_G(t_0)$, $I_D - V_G(t_R)$, and $I_D - V_G(t_n)$ is the pristine transfer characteristics, post-radiation transfer characteristics, and the final-time transfer characteristics of the device, respectively.

geometry dependence of transistor degradation related to radiation dose (after all, HCD depends sensitively on device geometry).

6.3.1 Impact of Radiation on Drain Current

Non-LOCOS LDMOS: Right after the exposure to various TID, the drain current is measured and found to increase, as shown in Fig. 6.3(a). The threshold voltage, V_{TH}, measured by the constant-current method decreases with increasing TID, as shown in the transfer characteristics in Fig. 6.3(b). The blown-up snapshot of the subthreshold region is shown in Fig. 6.3(c), indicating an almost parallel leftward shift of the I-V subthreshold characteristics. This parallel shift is easily interpreted as being related to trapped holes within the oxide of an n-type LDMOS. Here, ΔN_{ot} due to trapped charges enhances the electric field, and therefore, thus lowering the ΔV_{TH} ($\sim q(\Delta N_{ot}$ - $\Delta N_{it})/C_{ox}$), which was seen in Fig. 6.3 (a), (b), and (c) and increases the current at the same applied bias [241]. The leftward shift indicates that contribution from ΔN_{ot} is much larger than ΔN_{it}, because a higher ΔN_{it} would have moved V_{TH} to the right. To confirm this assertion, the change in subthreshold slope (ΔSS $\sim q\Delta N_{it}$) is extracted from Fig. 6.3 (b) and plotted w.r.t to TID

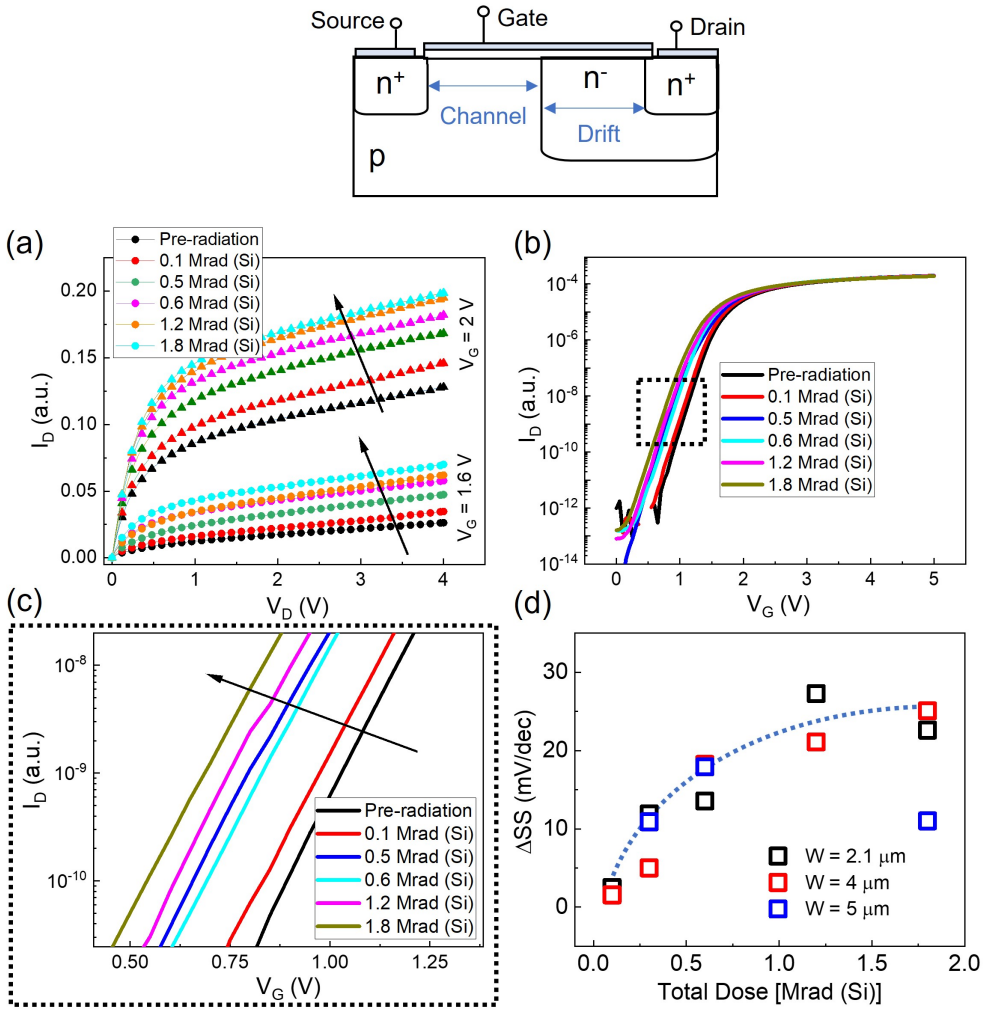


Figure 6.3. (a) I_D – V_D plot of non-LOCOS LDMOS transistors after exposure to different TID: 0.1, 0.5, 0.6, 1.2 and 1.8 Mrad (Si). (b) Dose-dependent I_D – V_G plot of LDMOS devices. (c) A blown-up snapshot of the I_D – V_G plot showing the impact of ΔN_{ot}. (d) Change in subthreshold slope (SS) of the LDMOS under different TID. An eye-guide (blue dotted lines) is added to visualize the saturation trend.

in Fig. 6.3(d). ΔSS of ∼25 mV/dec was found at high TID, indicating the slight increase in ΔN_{ot}. Moreover, ΔSS begins to saturate beyond 1 Mrad (Si), and several devices of different widths (2.1, 4, 5 μm) were measured to confirm the trend.

LOCOS LDMOS: Almost a similar trend is observed for LOCOS LDMOS devices, as shown in Fig. 6.4. The drain current increases with increases TID until the radiation, is high (TID: 1.8 Mrad (Si)) (Fig. 6.4 (a)). The leftward shift of the drain current indicates the

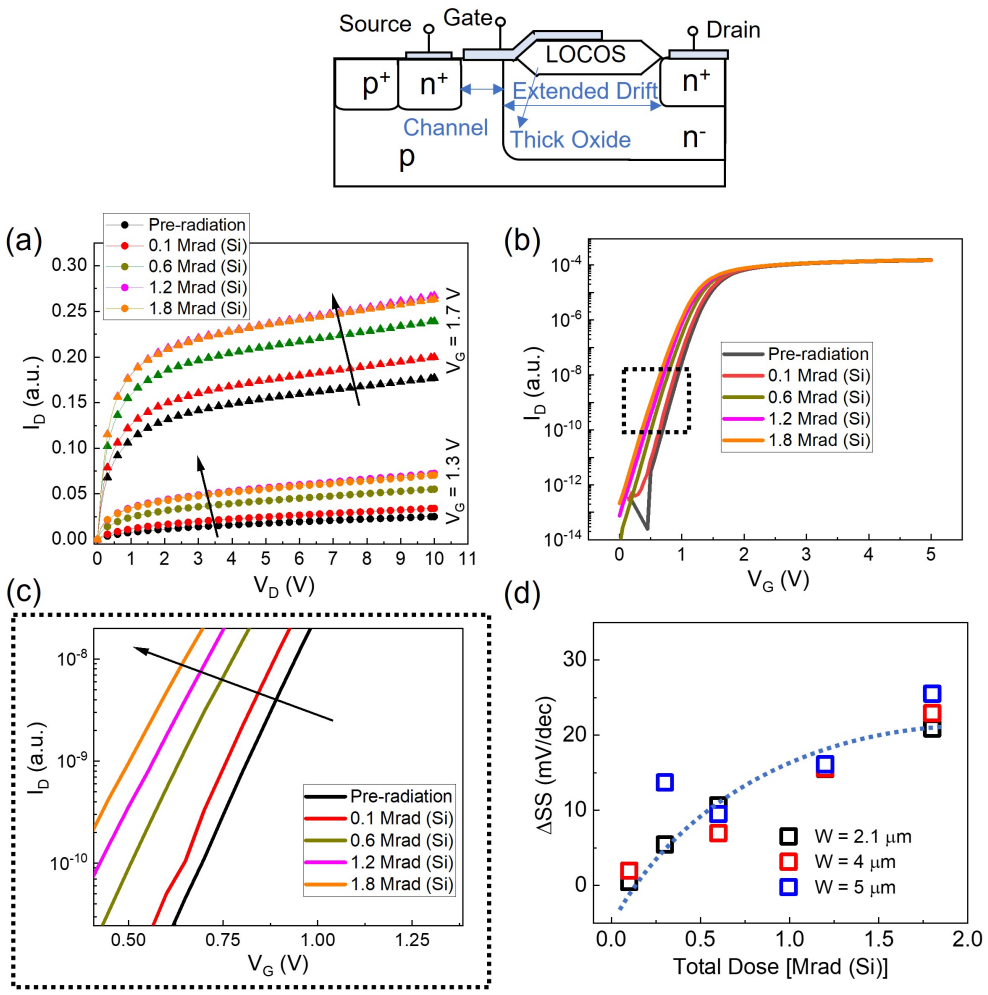


Figure 6.4. (a) I_D – V_D plot of LOCOS LDMOS transistors after exposure to different TID: 0.1, 0.6, 1.2 and 1.8 Mrad (Si). (b) Dose-dependent I_D – V_G plot of LDMOS devices. (c) A blown-up snapshot of the I_D – V_G plot showing the impact of ΔN_{ot}. (d) Change in subthreshold slope (SS) of the LDMOS under different TID. An eye-guide (blue dotted lines) is added to visualize the saturation trend.

contribution from ΔN_{ot} (Fig. 6.4(b) and (c)), while the unexpectedly lower drain current for 1.8 Mrad (Si) due to the increasing contribution of ΔN_{it}. The ΔSS of LOCOS LDMOS tends to saturate at higher TID, just like the non-LOCOS LDMOS.

6.3.2 Device Width Dependence

Non-LOCOS LDMOS: The trade-off between the breakdown voltage (V_{bd}) and the specific on-resistance ($R_{on,sp}$) is dictated by the drift region in an LDMOS transistor. While higher doping in the drift reduces the $R_{on,sp}$, the depletion width also reduces in reverse bias, leading to lower V_{bd} [93]. Instead of altering the doping, the device width is usually varied to meet the current requirements. Thus, it is essential to evaluate if there is any correlation between LDMOS device geometry and radiation dose. We already confirmed that ΔSS is device-width independent. Here, Fig. 6.5(a) shows that the change in current (ΔI_D (%)) is almost independent of device width except for the very narrow devices (< 5 μm). The possible reason behind this observation could be geometric edge effects, which

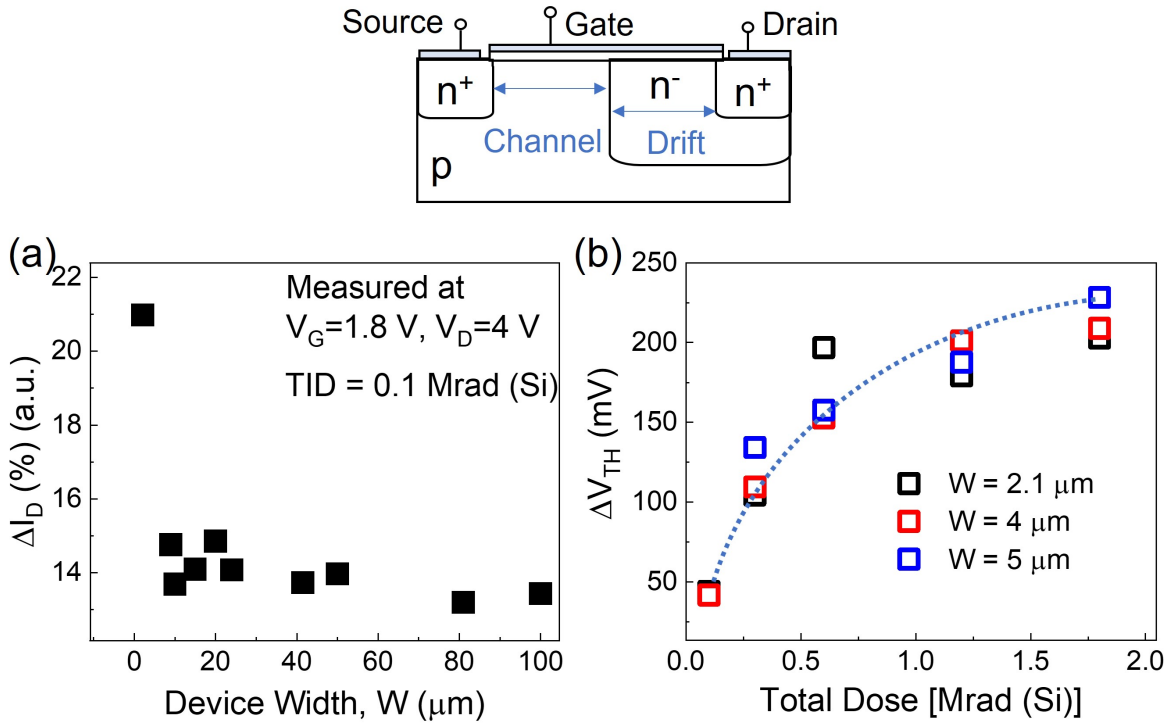


Figure 6.5. (a) Variation of I_D due to different channel width in case of non-LOCOS LDMOS devices. (b) Dose-dependent V_{TH} variation. An eye-guide (blue dotted lines) is added to visualize the saturation trend..

become prominent in narrow-channel devices [242]. ΔV_{TH} increases with increasing TID, as shown in Fig. 6.5(b); however, it tends to saturate with higher TID, similar to ΔSS (Fig

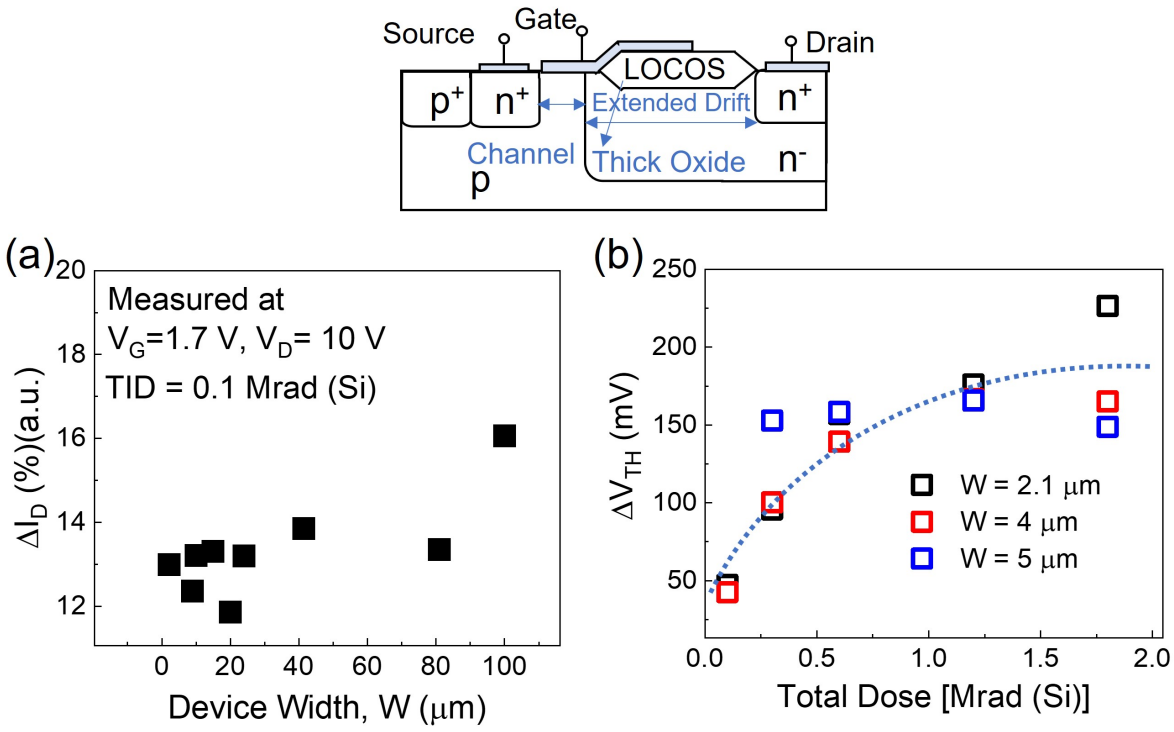


Figure 6.6. (a) Variation of I_D due to different channel width in case of LOCOS LDMOS devices. (b) Dose-dependent V_{TH} variation. An eye-guide (blue dotted lines) is added to visualize the saturation trend.

6.3(d)), so that ΔV_{TH}, $\Delta SS \propto TID/(1+TID)$. This is due to the 'rebound effect' where N_{it} generation starts competing with N_{ot} formation. A similar trend of ΔV_{TH} saturation has been observed when the devices were exposed to radiation of 1-6 Mrad [243], [244].

LOCOS LDMOS: For LOCOS LDMOS also, $\Delta I_D(\%)$ is independent of device width (Fig. 6.6 (a)), and ΔV_{TH} saturation tends to saturate (Fig. 6.6 (b)). To summarize, the impact of radiation in LDMOS (non-LOCOS and LOCOS) is device-width independent. Hence, all inferences drawn from this study are applicable for LDMOS with different widths and oxide thicknesses. The N_{it} due to TID can be quantified using a novel CP technique for both non-LOCOS and LDMOS LDMS, which is discussed in the following subsection.

6.3.3 Location Dependence of Radiation-Induced Defects

The Super Single Pulse Charge Pumping (S^2PCP) technique (not described in this thesis) was used to monitor ΔN_{it} in the channel and drift regions of LDMOS after various TID. The channel and drift regions in an LDMOS have different doping, oxide thickness, etc., and may potentially be impacted differently by the TID. The basic principle of the S^2PCP and the detailed physics, simulations, and experimental validation are described in Refs [106], [187]. A schematic of the measurement setup is shown in Fig. 6.7(a), and the obtained transient currents are shown in Fig. 6.7(b). ΔN_{it} can be calculated by comparing the extracted N_{it} before and after TID, as shown in Fig. 6.7(c). As expected, ΔN_{it} increases as TID increases for both the channel and the drift regions. However the ΔN_{it} generated in the channel region is higher than the ΔN_{it} generated in the drift region, at the same TID. The enhanced electric field in the oxide of the channel region (band diagram is shown in Fig. 6.7(c, inset)), leads to a quicker removal of the TID generated electrons from the oxide [241]. Thus fewer holes were eradicated due to recombination, which can hop towards the Si/SiO_2 interface, creating H^+ ions to form higher N_{it} in the channel region.

Following the same principle as the Oxide-Trap Charge Pumping (OTCP) technique [245], the S^2PCP technique can also estimate the N_{ot} generation. As more and more holes are generated due to higher TID, the electric field enhances, accelerating the recombination of the carriers. This leads to a temporal shift in the transient current with increasing TID, as shown in Fig. 6.7(b). This shift is compared to ΔV_{TH} calculated by the constant current method from I-V curves in Fig. 6.7 (d), since ΔV_{TH} of an LDMOS is primarily determined by the channel region alone [144], [246]. It is noteworthy that, for relatively low TID [<1 Mrad (Si)], ΔN_{ot} obtained from S^2PCP coincides with ΔV_{TH} from I-V curves. The deviation under higher TID may be due to the rapidly increasing ΔN_{it}, which saturates the ΔV_{TH} obtained from I_D - V_G curves. Therefore, the same S^2PCP technique can be used successfully to estimate both the ΔN_{it} and ΔN_{ot} in a non-LOCOS LDMOS transistor.

Designing pulses and biases for LOCOS LDMOS is way more complicated than the non-LOCOS device. This is because the extended drift region and unique geometry of the LOCOS oxide create a higher number of hotspots. Therefore, in addition to the channel and drift (or

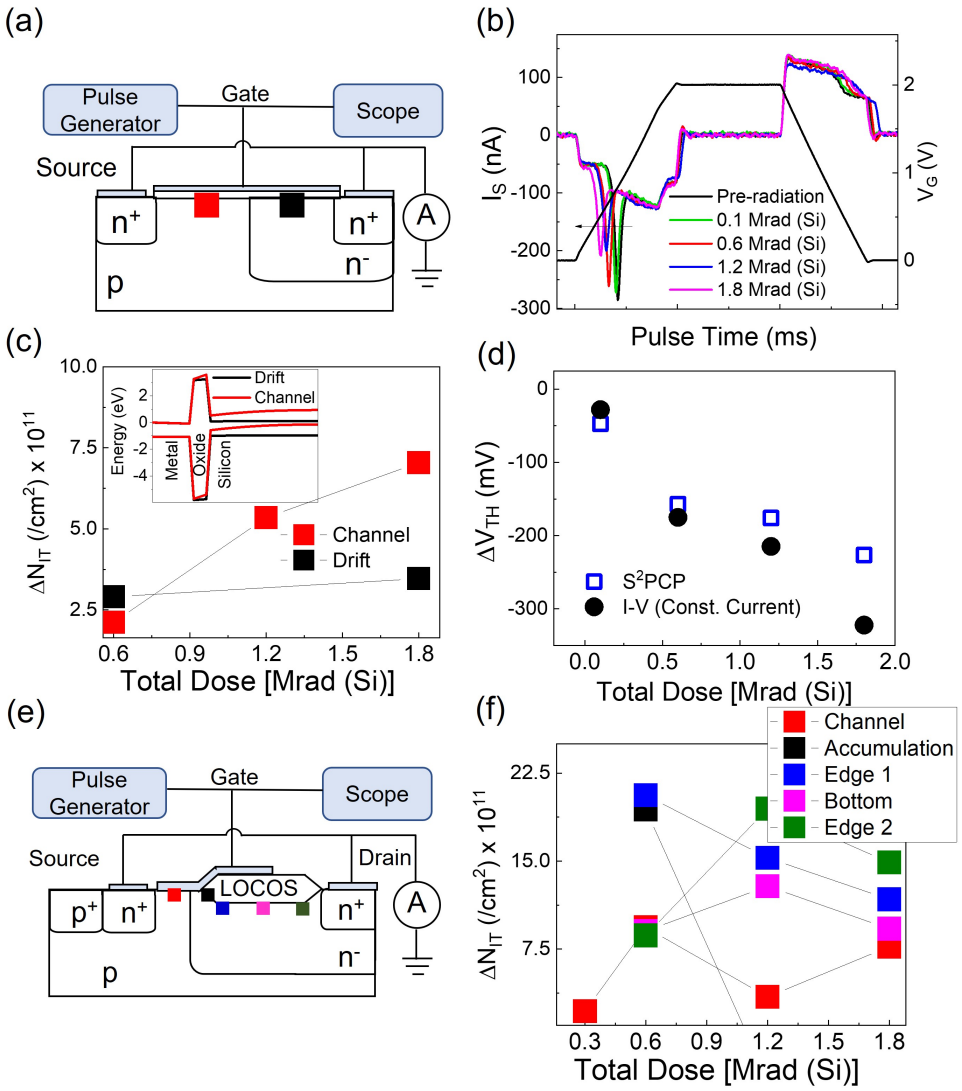


Figure 6.7. (a) A schematic of the connections of DUT for S^{2}PCP (Si). (b) The dose-dependent transient current, for floated source configuration. (c) Extraction of $N_{it}(x)$, using the transient current. (d) Threshold voltage shift measured from the transient currents.

accumulation) region, the edges of LOCOS (both at the beginning and in the end), and the middle of LOCOS in monitored in S^{2}PCP. The resulting ΔN_{it} due to TID at various points in the LOCOS LDMOS are shown in Fig. 6.7 (f). The detailed analysis and physics behind the evolution of N_{it} at each point in LOCOS LDMOS, is complicated due to the correlated effects of the electric field and LOCOS oxide thickness and is beyond the scope of this thesis. However, it is evident that the S^{2}PCP technique can be used to the defects generated due to

TID in a wide variety of LDMOS devices. With all these experiments on the pristine device and observations, we are now ready to explore the correlation between TID and HCD.

6.4 Correlated Hot Carrier Degradation and TID

6.4.1 TID followed by HCD: Threshold Voltage Shift

In the first set of experiments, radiation exposure is followed by HCD. The experiment was schematically represented as $TID \rightarrow HCD$, shown in Fig. 6.2(a). We have seen in the preceding section that V_{TH} decreases with increasing TID. However, when the hot carrier stress is applied to an already irradiated transistor (TID = 0.6 Mrad(Si) for example), V_{TH}

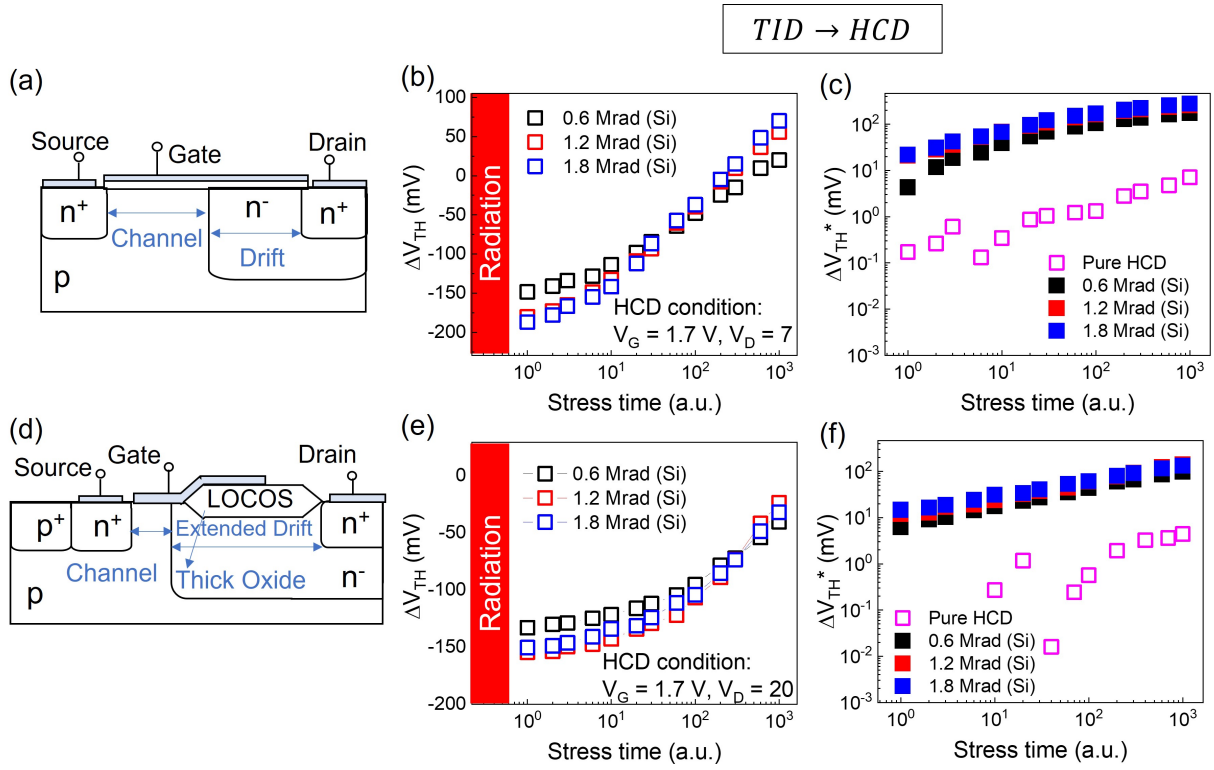


Figure 6.8. (a) A schematic of the non-LOCOS LDMOS. (b) Dose-dependent ΔV_{TH}, TID degradation due to HCD, preceded by TID, for a non-LOCOS LDMOS. (c) Extraction of ΔV_{TH}^{*}, after subtracting the initial shift due to TID. A pure HCD curve is also plotted for comparison. (d) A schematic of the LOCOS LDMOS. (e) Dose-dependent ΔV_{TH} degradation due to HCD, preceded by TID, for a LOCOS LDMOS. (f) Extraction of ΔV_{TH}^{*}, after subtracting the initial shift due to TID. A pure HCD curve is also plotted for comparison.

increases, as shown in Figs. 6.8 (b) and (c). This can be attributed to the hot carrier-induced generation of N_{it}, which counteracts the negative shift induced by N_{ot} generated due to TID. Fig. 6.8 (c) shows the time evolution of $\Delta V_{TH,TID\rightarrow HCD}$ under different TID. Initial TID shifts V_{TH} differently for the three cases, due to different N_{ot} generated by TID.

To further analyze the V_{TH} introduced by HCD, we define a term $\Delta V^{*}_{TH,TID\rightarrow HCD}$, which is expressed as:

$$\Delta V^{*}_{TH,TID\rightarrow HCD} = \Delta V_{TH,TID\rightarrow HCD} - \Delta V_{TH,R} \tag{6.1}$$

where $\Delta V_{TH,R}$ is the TID introduced ΔV_{TH}. *The key question here is: Does* $\Delta V_{TH,R}$ *impact* $\Delta V^{*}_{TH,TID\rightarrow HCD}$*, or in other words, are the degradations correlated?* The extracted ΔV^{*}_{TH} is plotted in Fig. 6.8(c). It is interesting to note that, for the same HCD stress conditions (i.e., same stress V_G,V_D), HCD induces more ΔV_{TH} if it exposed to higher TID beforehand, suggesting an obvious correlation. If ΔV^{*}_{TH} is fitted with a saturating power law, i.e.,

$$\Delta V^{*}_{TH,TID\rightarrow HCD} = \frac{A\left(V_G, V_D, T\right) t^m}{1 + B\left(V_G, V_D, T\right) t^m} \tag{6.2}$$

as it is done for to capture the time-kinetics of radiation-free HCD degradation [2], we find that the fitting parameters A and B are functions of V_G, and V_D as well as TID. The exponent, m, however, is independent of TID (m = 0.58) in Fig. 6.8(d). The correlated TID-dependence of HCD is easily understood: a higher TID enhances the effective electric field in the oxide, which accelerates the generation of ΔN_{it} due to HCD. The cumulative effect of ΔN_{it} due to radiation and enhanced ΔN_{it} due to HCD leads to a higher ΔV^{*}_{TH} degradation, compared to pure HCD, at the same applied bias (Fig. 6.8). To summarize, $\Delta V_{TH,TID\rightarrow HCD}$ is given as:

$$\Delta V_{TH,TID\rightarrow HCD} = \frac{A\left(V_G, V_D, TID\right) t^m}{1 + B\left(V_G, V_D, TID\right) t^m} + \Delta V_{TH,R} \tag{6.3}$$

When the LOCOS LDMOS is subjected to TID, after HCD, an observation similar to non-LOCOS LDMOS was recorded (Fig. 6.8 (e)). After subtracting the initial shift, when ΔV^{*}_{TH} is plotted with stress time, a power-law characteristic was observed, albeit with a different exponent (m ~0.45). As a result, the $\Delta V^{*}_{TH,TID\rightarrow HCD}$ for LOCOS LDMOS, shown in Fig. 6-

8 (f), can be fitted with Eq. 6.3. The enhanced HCD for LOCOS LDMOS can be interpreted similarly as the non-LOCOS LDMOS.

Therefore, in this subsection, we have established that for $TID \rightarrow HCD$, TID and HCD are correlated and enhances the HCD. In the following section, $HCD \rightarrow TID$, where TID is done after HCD stress, will be investigated.

6.4.2 HCD Followed by TID

The experimental setup for this set, is schematically represented in Fig. 6.2 (b), as $HCD \rightarrow TID$. As seen from Figs. 6.9 (b), while the HCD induces slight degradation (right shift of V_{TH} degradation, seen from the slight increase in ΔV_{TH}), TID counterbalances HCD with a significant negative shift in V_{TH}. This is due to competing ΔN_{ot} and ΔN_{it} [243]. Therefore the initial conclusion is that, for $HCD \rightarrow TID$, TID improves the HCD (ΔV_{TH}), while the leakage current is also enhanced.

In $HCD \rightarrow TID$ case, the HCD and TID appear to be correlated only at high TID. This is evident from Fig. 6.9 (c), where the ΔV_{TH} shift introduced by the ΔN_{ot} and ΔN_{it} due to radiation, is decreasing at high TID, in contrast to the saturation observed in the pristine devices (Fig. 6.5 (b) and 6.6 (b)). It is likely that the aggregate ΔN_{it} due to radiation and HCD compensate the impact of ΔN_{ot} generated due to radiation.

Almost a similar trend is observed for the LOCOS Devices, including the shift in ΔV_{TH}, post TID. While a direct comparison between non-LOCOS and LOCOS devices is not feasible due to different electric fields, resulting from different bias and oxide geometry, an important difference is identified in Fig. 6.9 (b)(zoomed image, right) and (d) (zoomed image, right), which may delineate the advanatges of a thick LOCOS. Despite having a similar shift in ΔV_{TH} due to TID of 0.6 and 1.2 Mrad (Si), the LOCOS LDMOS has a lower reduction at 1.8 Mrad (Si). One of the most plausible reasons is the that lesser N_{it} is generated in LOCOS LDMOS during TID, thus alleviating the compensation of the impact of ΔN_{ot}.

$\Delta V^{*}_{TH,HCD \rightarrow TID}$ can be given as:

$$\Delta V_{TH,HCD \rightarrow TID} = \frac{A\left(V_G, V_D\right) t^m}{1 + B\left(V_G, V_D\right) t^m} + V^{*} \tag{6.4}$$

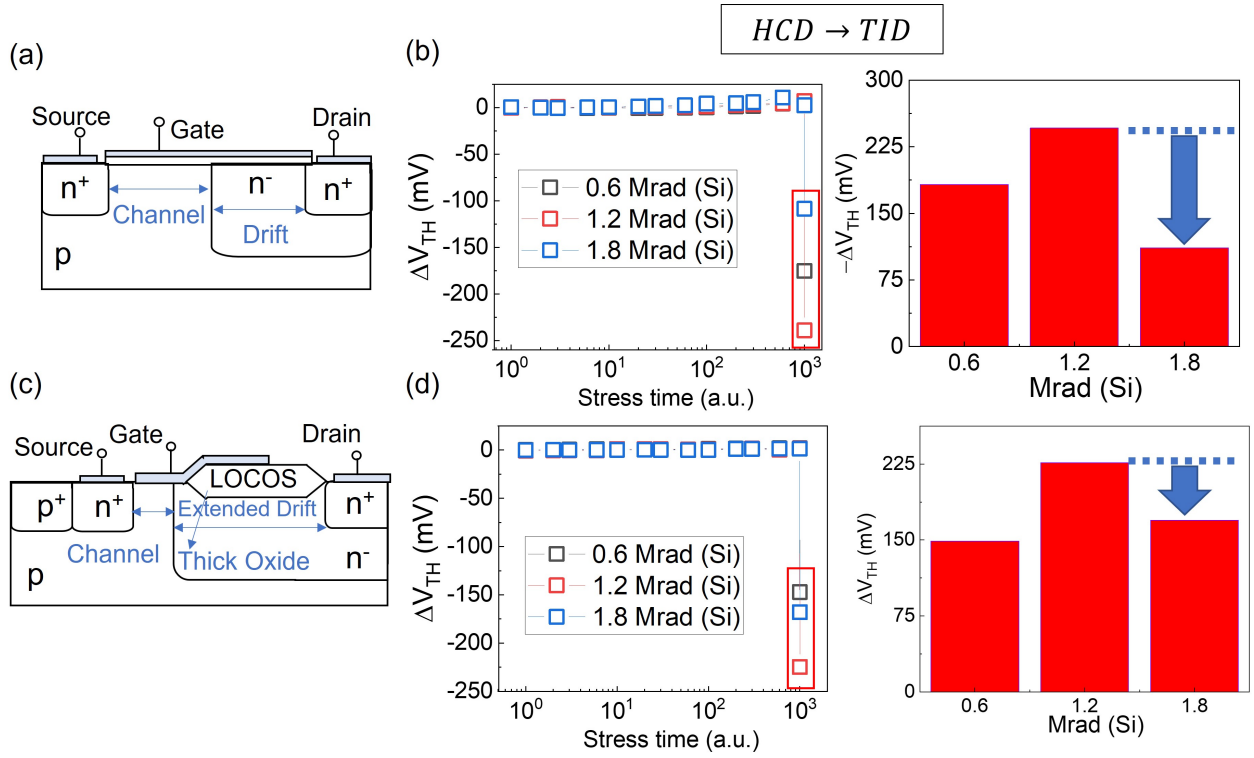


Figure 6.9. (a) Schematic of the non-LOCOS LDMOS (b) ΔV_{TH} degradation due to HCD, followed by TID. A zoomed in image of the decrease in ΔV_{TH} (or increase in -ΔV_{TH}) due to increased TID (right). (c) Schematic of the LOCOS LDMOS (d) ΔV_{TH} degradation due to HCD, followed by TID. A zoomed in image of the decrease in ΔV_{TH} (or increase in -ΔV_{TH} due to increased TID (right).

where V^* represents the decrease (or the increase) in $\Delta V_{TH,HCD \rightarrow TID}$ due to the correlated effects of TID and HCD. A and B here are bias dependent only. Therefore, while HCD is not as strongly correlated with TID for the $HCD \rightarrow TID$ case, however, high TID influences the HCD. Although phenomenological models to represent the correlation between the HCD and TID are proposed here, it is not entirely clear if TID alters the classical degradation kinetics of HCD or not. A straightforward way to verify this is by obtaining the universal scaling curve, which will be discussed in the next section.

6.5 Universal Scaling of HCD

The universal degradation of HCD is based on the principle that a general form, $N_{it} \sim f(t/\tau)$, can describe the degradation in logic or power transistors, where τ (V_G,V_D,G, etc.) is a characteristic function of voltage (V_G,V_D), geometry (G), etc., when individual degradation curves at each bias are scaled along the time-scale. Universal scaling curve is a characteristic of HCD and has been obtained for logic and power devices from different generations, operated at various biases and temperatures [2]. The basic principle and physics behind the universal scaling of HCD was described in Chapter 4.

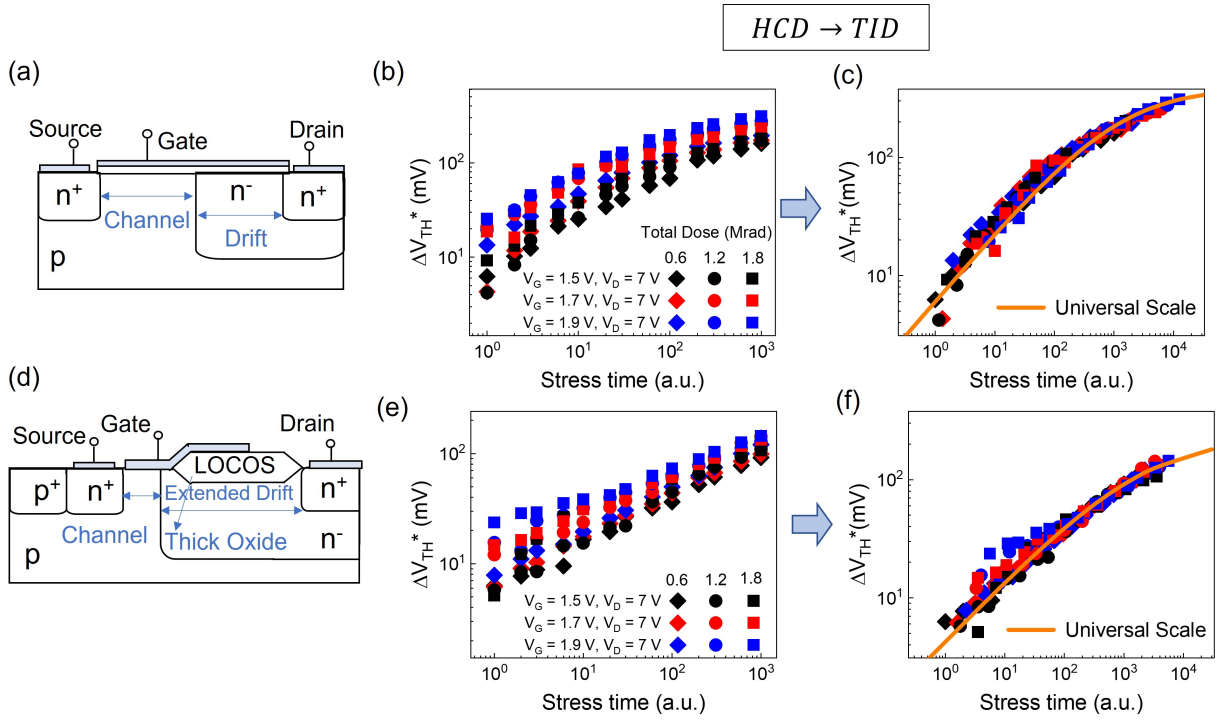


Figure 6.10. (a) Schematic of the non-LOCOS LDMOS (b) ΔV_{TH} degradations at different combinations of V_G,V_D due to HCD, followed by TID. (c) Universal Scaling of ΔV_{TH} degradations in the non-LOCOS LDMOS (d) Schematic of the LOCOS LDMOS (e) ΔV_{TH} degradations at different combinations of V_G,V_D due to HCD, followed by TID. (f) Universal Scaling of ΔV_{TH} degradations in the LOCOS LDMOS.

The extracted ΔV_{TH}^* curves at different biases and TID in $TID \rightarrow HCD$ are shown in Figs. 6.10(b) and (e). When we scale along the time-axis, the universal scaling curve of ΔV_{TH}^* for both non-LOCOS and LOCOS LDMOS can be obtained as shown in Figs. 6.10

(c) and (f). This is a significant result because the ΔV_{TH}^{*} curves are not pure HCD and affected by ΔN_{ot} or ΔN_{it} after TID. The universality holds simply because the TID leads to an effective shift in the internal stress voltage, but HCD universal scaling holds regardless the effective vs. actual gate stress voltage. The HCD component of $HCD \rightarrow TID$ is pure HCD and is expected to show this universal scaling, and hence not plotted here.

6.6 Summary

This chapter investigates the effect of TID on the performance and reliability of LDMOS devices. The results are summarized below:

(a). The effect of TID in LDMOS is independent of device width. Therefore, results obtained from test structures of a specific width can also be used to interpret/qualify LDMOS with other widths.

(b) Increasing TID leads to a decreasing ΔV_{TH}. This is due to the increasing number of ΔN_{ot} which enhances the electric field. However, this change in V_{TH} tends to saturate due to competing effects of N_{ot} and N_{it} generated in high TID. The same effect is observed for ΔSS.

(c) TID decreases V_{TH}, while HCD increases V_{TH}. This compensation may increase the parametric lifetime of power transistors. The optimistic conclusion is supported by a variety of experiments reported in this chapter.

(d) The HCD degradation in a pre-irradiated LDMOS depends on the TID dose, i.e., the degradations are correlated. The ΔV_{TH} due to TID acts as an excess internal V_G stress, thereby accelerating the degradation. Since degradation curves for various V_G stress of radiation-free LDMOS can be scaled to a universal curve, the same is true for HCD degradation under fixed HCD but exposed to different TID. The claim is supported by experiments involving both LDMOS and LOCOS-based transistors.

(e) If a device is irradiated after the HCD degradation, there is an overall improvement in V_{TH}. The degree of improvement depends on the radiation dose.

In conclusion, a counter-balancing ΔV_{TH} associated with the electrical and radiation of degradations various LDMOS transistors (non-LOCOS and LOCOS) shows that a carefully

designed system would function reliably even in a radiation-rich environment. This TID-specific conclusion needs to be generalized for other radiation effects, such as single-event upset (SEU) and total non-ionizing displacement damage (NIDD).

7. SUMMARY AND FUTURE WORK

7.1 Thesis Summary

In this thesis, we have holistically analyzed the reliability of power transistors by broadening the reliability physics framework originally developed for logic transistors. While we have used characterization techniques and simulation tools to interpret the evolution of interface defects in transistors, we have also developed analytical models to predict the long-term reliability of traditional and state-of-the-art power electronic devices.

The content in chapter 2 was driven by the realization that the emergence of several technology options and the ever-broadening range of applications for power electronic devices suggest both a need and an opportunity to develop unifying principles to guide the development of wide bandgap (WBG) semiconductors. Unfortunately, power electronic devices are typically evaluated with different elementary figure of merits (FOMs), which offer inconsistent and contradictory projections regarding the relative merits of emerging technologies. Therefore, one relies on the empirical (extrinsic) safe-operating area (SOA) of a packaged device to ultimately assess the performance potential of a technology option. Unfortunately, extrinsic SOA can only be calculated *a posteriori*, i.e., after precise measurement of the fabricated device parameters, making it suitable only for relatively mature technologies. Based on the insights of material-device-circuit-system performance analysis of a variety of idealized WBG power electronic devices (e.g., GaN HEMT, β-Ga_2O_3 MOSFET), in this thesis, we analytically derived a comprehensive, substrate-, self-heating-, and reliability-aware "intrinsic/limiting" safe operating area (SOA) that establishes *a priori*, i.e., before device fabrication, the optimum and self-consistent trade-off among breakdown voltage, power consumption, operating frequency, heat dissipation, and reliability. We established the relevance of the intrinsic-SOA by comparing its prediction with a broad range of experimental data available in the literature. The intrinsic SOA allows fundamental/intuitive re-evaluation of innate technology potential for power electronic devices and identifies specific performance bottlenecks and how to circumvent them.

In chapter 3, we take a closer look into individual power transistors to define the practical (rather than the intrinsic) performance and reliability limits. We start with the power tran-

sistor, which is making the most strides currently: a β-Ga_2O_3 based transistor. The β-Ga_2O_3 transistor came into prominence because it outperforms a GaN transistors in Baliga's FOM by 400% and Huang's chip area manufacturing figure of merit by 330%. The availability of large wafers of β-Ga_2O_3 is another factor, for which β-Ga_2O_3 is viewed as the material of choice for the next generation power transistors. However, its low thermal conductivity leads to extreme self-heating, which deteriorates the device performance during high voltage operation. Although our calculations for "intrinsic" SOA suggest that its low thermal conductivity will lead to a lower SOA than other wide bandgap devices (GaN, SiC, etc.), we decided to do a comprehensive evaluation of performance from a material-device-circuit perspective, so that we can calculate the switching response and mitigation strategies. We developed a multi-physics and multi-scale model for a material-device-circuit analysis of β-Ga_2O_3 transistors. The framework allows us to explore the effectiveness of various device design strategies (e.g., thermal shunts) for mitigating the thermal choke-points and compare the performance of improved β-Ga_2O_3 transistors against that of GaN and transistors. We highlight the limitations of traditional FOMs to analyze the relative performance of the new generation of power transistors whose structure incorporates stacked layers of materials with different thermal conductivity, like those of β-Ga_2O_3 transistors. We suggest device design strategies, such as wafer thinning, incorporating heat shunts, and improved channel mobility so that β-Ga_2O_3 transistors can compete commercially with GaN and SiC technologies. We also propose h-BN based FinFET that exceeds the I_{ON} of the existing β-Ga_2O_3 transistors by more than 500%; and develop a Faraday-cage type novel packaging strategy for effective heat dissipation and efficient system performance in β-Ga_2O_3 transistors.

After verifying our predictions of "intrinsic" SOA with an all-inclusive analysis of state-of-the-art β-Ga_2O_3 transistors, we turn our attention to one of the most popular power transistors that has been studied and used extensively over the last few decades: a Lateral Double Diffused MOSFET or LDMOS, in Chapter 4. LDMOS has numerous applications in almost all sections of the industry (automotive, photovoltaics, consumer electronics, agriculture machinery, medical instruments, etc.). However, hot carrier degradation (HCD) remains a persistent and vital design challenge for LDMOS transistors due to its high applied bias during operation. The first thing that we decided to check is how different is the

hot carrier degradation (HCD) in LDMOS transistors, compared to the classical MOSFETs. It is well-known that regardless of the voltage/temperature/device structure, the HCD of classical logic transistors scales onto a single universal curve, offering a theory-agnostic approach to predict long-term degradation based on short-term accelerated tests. Based on the experimental results, it has been suggested that the HCD in LDMOS is structurally and functionally so fundamentally different, that an analogous universal scaling cannot apply. In this thesis, we used a tandem FET (two MOS) model of an LDMOS to explore the physical origin of the anomalous HCD degradation in power transistors and establish the general principle needed to restore the universality of the degradation kinetics. By deconvolving the degradation in the drift and channel region, we found that the LDMOS follows the universal scaling of HCD, but in a unique way. Interestingly, the empirical models used to evaluate HCD degradation in power transistors emerge naturally as approximations of the generalized approach.

While the universal scaling approach establishes that the degradation kinetics of HCD in LDMOS is the same as in MOSFETs when deconvolved appropriately, it is a phenomenological approach and articulates little about the underlying physical mechanisms of degradation in LDMOS. Other profiling techniques also fail to reveal much information about the physical mechanisms of degradation (N_{it} generation), and therefore device-specific, time-consuming, and expensive qualification of every technology is required for devices, even those with minor geometrical or doping variation. TCAD proves to be an indispensable tool in such situations and provides the needed technology parameters like the electric field, electron temperature, mobility, etc., and the spherical harmonics expansion-based TCAD-HCD models presumably provide the required degradation kinetics for technology qualifications. The most popular TCAD-HCD model is that of the Hot Carrier Stress (HCS) model, which interprets the total degradation as the sum of single-particle, multiple particles, and thermal generation processes, with the device geometry and biases deciding the dominant degradation mechanism among them. Solving the carrier transport in TCAD using the first-order spherical harmonics expansion of the BTE, and using the HCS degradation model in Chapter 5 for HCD, we find that the single-particle excitation is the dominant mechanism in n-type non-LOCOS and LOCOS LDMOS devices. While the model reproduces the $I_{D,lin}$ degradation

over an extensive range of V_G/V_D voltages, unfortunately, the fitting parameters are not unique, with each combination leading to different but close values $N_{it}(x)$, suggesting a need to determine $N_{it}(x)$ experimentally. Experiments reveal that TCAD captures the essence of HCD in LDMOS, but one has to be careful before predicting the lifetime in the whole V_G,V_D regime, as additional mechanisms may be contributing towards the total degradation.

While HCD has been a persistant concern, power electronics devices have found applications in high energy physics, drones, space electronics, etc., over the last decade. It is well-known that the devices used in these applications are often subjected to high amounts of radiation, and unlike traditional applications, it is not possible to replace these power FETs (e.g., LDMOS) frequently. Therefore, it is essential to accurately predict the long-term degradation of these power FETs in the presence of radiation. In Chapter 6, we expose the LDMOS transistors to various Total Ionizing Dose (TID) of gamma (γ) radiation and characterized the degradation in terms of threshold voltage shift (ΔV_{TH}), linear drain current degradation ($\Delta I_{D,lin}$), subthreshold slope (SS). We also quantify the dose-dependent generation of interface traps (ΔN_{it}) and trapped charges (ΔN_{ot}), using a novel charge pumping technique. We introduce hot carrier degradation (HCD) models to explore the physical origin of the defects and their correlation with TID, establishing the universality of the degradation kinetics. Finally, we compare our findings with that of an LDMOS of varied geometry, dimension, and bias, illustrating that the model and inferences drawn from the conclusions of the chapter can be applied to other LDMOS devices of varied dimensions, power rating, breakdown voltage (V_{bd}), etc. as well.

Therefore in this thesis, we have taken a few steps towards developing a generalized reliability model for power transistors incorporating several sources of variation (electrical, thermal, and radiation) for long-term device operation; however, further experiments, modeling, and simulations need to be carrier out to achieve a truly 'end-to-end' predictive reliability model for a power electronic system.

7.2 Future Work

A few topics of research towards the ultimate goal of a comprehensive reliability model for power electronic systems are discussed here.

(a) ***Generalization of the "Instrinsic" Safe Operating Area of Power Transistors***: The analytical derivation of SOA in this thesis has been carried out by considering power dissipation due to conduction loss only. While the expressions derived here are robust for determining a transistor's lifetime, one may want to include the power dissipation during switching loss as well. Including the switching loss will provide a more realistic 'intrinsic' SOA for the power transistor's circuit operation in applications such as DC/DC converters. In addition, nowadays, state-of-art wide bandgap transistors include multiple layers to aid in fabrication, thermal management, etc. Therefore, it is crucial to determine the thermal resistance of such structures for determining the SOA. While one can always use COMSOL or any other finite element software to calculate the thermal resistance, an analytical expression is required to determine the 'intrinsic' SOA. Hence, another direction of research on this topic would be to obtain 3D closed-form analytical expressions for thermal resistance, which are easily scalable to multiple layers and can be solved without requiring complicated calculations.

(b) ***Thermal management of β-Ga_2O_3 transistors for future power electronics***: Besides the efficiency, the power electronics market is driven by the cost of the transistors. β-Ga_2O_3 is a promising material for power electronics because of the availability of potential low-cost substrates, however, thermal management of β-Ga_2O_3 transistors will become crucial in the competition with the already thriving GaN and SiC market. Although a few approaches for improving the thermal resistance of β-Ga_2O_3 transistors are proposed in this thesis, this field will require significant innovation if β-Ga_2O_3 transistors have to become a prevalent power transistor. Integrating high thermal conductivity materials with β-Ga_2O_3 transistors for lower thermal resistance, innovative packaging strategies to remove the heat from the transistors, engineering the transistor geometry for improved thermal management will receive significant thrust in the near future. Moreover, the search for exotic materials with desirable qualities for power electronics (high breakdown, high mobility, high thermal

conductivity, aligned with mature fabrication and processing technologies, etc.), would be an exciting research area.

(c) ***Compact models of emerging power transistors for circuit implementation***: One of the very interesting topics of research would be the implementation of compact models of various power transistors in HSPICE. The '2 MOS' model is a possibility, however, these transistors must be generalized by including relevant capacitances, before they are embedded into the simulator. The transport, impact ionization and reliability models needs to verified for the emerging wide bandgap semiconductors like β-Ga_2O_3, Diamond, hBN, etc., at elevated temperature and voltages, before implementing in the compact model. This would a significant effort, but would be a seminal contribution to the power electronics community.

(d) ***Extension of classicial theories of HCD for power transistors***: Universal scaling is a significant breakthrough in the area of HCD, not only because it establishes the pervasiveness of the physics of HCD, but it also substantially reduces the number of experiments required to determine the lifetime of a complicated power transistor. While the universal scaling of a non-LOCOS LDMOS device has been achieved here, one can attempt to understand the physics of a more complicated power transistor (e.g. LOCOS LDMOS) and try to obtain the universal scaling of HCD. In addition, efforts can be made to extend the classical theories of HCD and other reliability phenomena to other state-of-the-art power devices (β-Ga_2O_3, AlN, Diamond, etc.).

(e) ***Multi-hotspot model implementation in TCAD***: TCAD modeling of HCD in LDMOS is essential for understanding the physical mechanism of degradation. HCD has been physically described by the reaction, diffusion, and drift mechanisms. However, the models of HCD currently implemented in TCAD focus primarily on the 'reaction' part of the degradation and attempts to model the whole degradation. In addition, at high biases, several mechanisms other than HCD may also contribute to the total degradation, which is not currently implemented in TCAD. Therefore, there is an opportunity to include the drift mechanisms of degradation and other possible reliability phenomena (e.g., Anode Hole Injection) together in a comprehensive HCD model for LDMOS in TCAD.

(f) ***Effects of radiation on the performance of power transistors***: Radiation tolerance of state-of-the-art power transistors will be an essential topic of research in the

near future. While several studies focus on how the drive currents and pristine device characteristics of modern transistors (e.g., β-Ga_2O_3) are affected by radiation, few focus on the integrated electrical and radiation reliability. β-Ga_2O_3 and other wide bandgap transistors are inherently more radiation-tolerant than Silicon, and therefore extending the work on correlated effects of radiation and HCD on LDMOS to the upcoming power transistors for use in military and space applications will them help gain a few steps in the competitive power electronics market.

(g) ***Package reliability for power electronics***: The comprehensive reliability model of power electronics will be incomplete without research dedicated to improving the package reliability of power transistors. Packages are vulnerable to various environmental stresses like moisture ingress, thermal cycling, layer delamination, etc. The extreme operating regimes of power electronics (high voltage, high temperature, high radiation, etc.) sometimes accelerate these environmental stresses are accelerated and reduce the lifetime of the package and the device. Therefore, besides designing innovative packages for efficient thermal management, a generalized reliability model of the packaging should be developed that encompasses all sources of environmental variations.

Finally, as the power transistors become more efficient, wide bandgap gap semiconductor-based devices will become prevalent, and innovative packaging methodologies will drive the evolution of power electronics. The power electronics will have a massive role to play in the heralded 6G technologies, and wideband semiconductors like GaN is likely to become the *de facto* choice for RF power amplifiers. The number of connected devices will increases, and will support higher data capacity and the responses will have low latency. It is our hope that the analytical models, experiments, reliability framework, and insights provided in this thesis will motivate future power electronics innovations that will be instrumental in driving technologies like 6G and beyond, in the future.

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A. PARAMETERS USED IN CALCULATIONS

Various material parameters and device dimensions, used in this chapter for the calculation of on-resistance (R_{on}), breakdown voltage (V_{bd}), maximum current (I_{max}), and maximum power (P_{max}) and finally the i-SOA, and reliability aware- i-SOA is given in Table A.1 and A.2.

Table A.1. Device Parameters used in calculations.

Material	**Silicon**	**SiC**	**GaN**	β-Ga_2O_3	**Diamond**
Bandgap (eV)	1.1	3.25	3.4	4.85	5.47
Dielectric Constant	11.8	9.7	9	10	5.5
Thermal Conductivity (W/cmK)	1.5	4.9	2.3	0.2	20
Electron Mobility (cm^2/Vs)	1480	1000	1250	300	2000
Breakdown Field (MV/cm)	0.3	2.5	3.3	8	10
Specific Heat (J/K-g)	0.7	0.69	0.49	0.49	0.52
Density (g/cm^3)	2.33	3.1	6.15	5.95	3.52
C_{th}/W(J/K-cm) ($\times 10^{-5}$)	4.89	642	904	875	549

Table A.2. Device Dimensions used in calculations.

Layers	**Length**	**Width**	**Thickness**
Bulk Substrate	4 μm	50 μm	300 μm
Top Layer of Bilayer Substrate	4 μm	50 μm	5 μm
Bottom Layer of Bilayer Substrate	4 μm	50 μm	300 μm

B. DETERMINING THERMAL RESISTANCE OF A BILAYER STRUCTURE

The self-heating at the device level (i.e., $\Delta T = P_D \theta_{th}$) is determined by calculating the θ_{th} associated with the structure. While the formula and techniques of determining θ_{th} of a bulk substrate is well established, θ_{th} of a multi-layered device is more complicated due to the change in the heat spreading angle in different layers.

For a bulk substrate, the simplest approach of calculating θ_{th} is to assume that heat spreads at a constant angle, ω (consider $\omega \sim 45°$, for simplicity). For a disk-shaped heat source of radius, a, thermal conductivity, λ, on a substrate of thickness, ℓ, as shown in Fig. B.1(a), θ_{th} can be obtained as [247]:

$$\theta_{th,singlelayer} = \frac{1}{\lambda \pi a} \frac{\ell}{(a + \ell \times \tan \omega)} \tag{B.1}$$

Now, let us consider a bilayer substrate with the thickness of the top layer, l_1 and bottom layer, l_2 respectively. The heat spreading angle and the thermal conductivity of the top layer is given as ω_1 and λ_1 and correspondingly ω_2 and λ_2 for the bottom layer, as shown in Fig. B.1 (b). Let us also assume that $\lambda_1 < \lambda_2$, because a low thermal conductivity channel is placed on top of a high thermal conductivity substrate for high-performance power electronics devices [16]. To extend Eq. B.1 to a bilayer substrate, we consider a constant spreading angle α for both layers and rewrite Eq. B.1 as:

$$\theta_{th,\text{ bilayer}} = \frac{1}{\lambda_1 \pi a} \frac{\ell_1 + (\ell_2 \times \lambda_1/\lambda_2)}{(a + (\ell_1 + \ell_2) \tan \omega)} \tag{B.2}$$

Eq.B.2 provides a reasonable approximation of θ_{th} as confirmed by 3D COMSOL simulations, shown in Fig B.1 (d). Even though the range of λ_2 is much larger than λ_1, θ_{th} is accurately reproduced using Eq. B.2. It is to be noted that Eq. B.2 should only be used for back-of-the-hand approximations of θ_{th} and not as a replacement of bilayer θ_{th} determining closed-form formulas, numerical expressions, or TCAD.

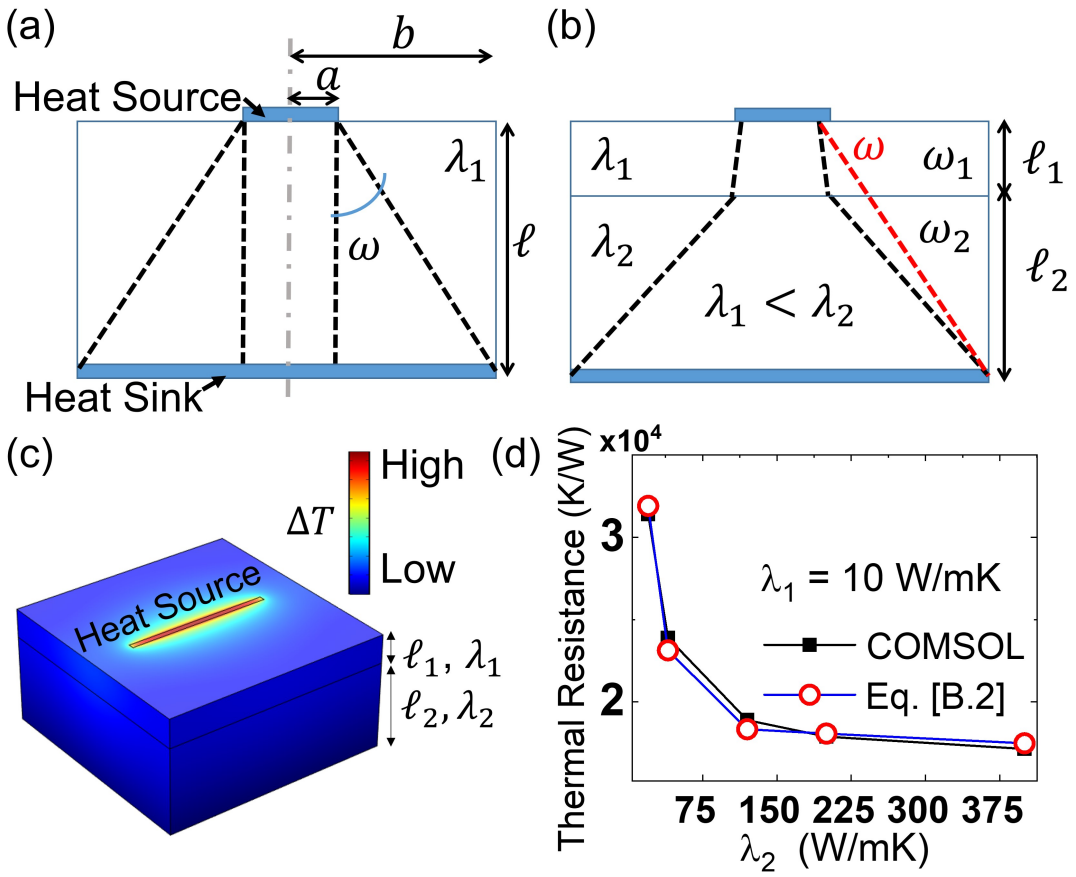

Figure B.1. (a) Schematic of a bulk substrate, with a spreading angle, ω and thermal conductivity, λ. (b) Schematic of a bilayer substrate, with a spreading angle, ω_1 and ω_2, thermal conductivity, λ_1 and λ_2 , and widths ℓ_1 and ℓ_2, for the top and bottom layers, respectively. (c) COMSOL simulation to obtain θ_{th} , of a bilayer structure. Here, Fourier Equation, $q = -\lambda \nabla T$, has been solved. Power of 1W has been applied of the structure and $\theta_{th} = \Delta\ T/P$ (d) Comparison of Eq. B.2, with 3D COMSOL simulation.

C. SENTAURUS TCAD CODE FOR A LDMOS

A sample TCAD code (sde, sdevice) for a generic LDMOS is given here. The 'sde' part generates the model, doping and meshing, whereas the 'sdevice' part includes the physics and solves for I_D - V_d of the LDMOS.

sde

```
; Reinitializing SDE
(sde:clear)
(sde:set-process-up-direction "+z")
(define Ltot 1.65) ;
(define Ly 1.65) ;
(define tox 0.010) ;
(define tch 1) ;
(define dl 0.25) ;
(define drift 0.3) ;
(define dftl 0.25) ;
(define sl 0.45) ;
(define sd 0.25) ;
(define sll 0.25) ;
(define c 0.005) ;
(define cs 0.125) ;
(define is 0.25) ;
(define i 0.235) ;
(define oxh 0.5) ;
; Overlap resolution: New replaces Old
(sdegeo:set-default-boolean "ABA")
; Creating the strcucture
(sdegeo:create-rectangle (position 0 0 0) (position Ltot Ly 0) "Silicon" "R.Substrate" )
(sdegeo:create-rectangle (position 0 0 0) (position tch tch 0) "Silicon" "R.channel" )
(sde:define-parameter "fillet-radius-ch" 0.5 0.0 0.0 )
```

(sdegeo:fillet-2d (find-vertex-id (position tch tch 0.0)) fillet-radius-ch)

(sdegeo:create-rectangle (position sl 0 0) (position (+ sl sll) sd 0) "Silicon" "R.source")

(sde:define-parameter "fillet-radius-s" 0.125 0.0 0.0)

(sdegeo:fillet-2d (find-vertex-id (position (+ sl sll) sd 0.0)) fillet-radius-s)

(sdegeo:fillet-2d (find-vertex-id (position sl sd 0.0)) fillet-radius-s)

(sdegeo:create-rectangle (position 0 0 0) (position sl sd 0) "Silicon" "R.body")

(sde:define-parameter "fillet-radius-b" 0.125 0.0 0.0)

(sdegeo:fillet-2d (find-vertex-id (position sl sd 0.0)) fillet-radius-b)

(sdegeo:create-rectangle (position 0 0 0) (position Ltot (* -1 oxh) 0) "SiO2" "R.Oxide")

(sdegeo:create-rectangle (position 0 0 0) (position (+ sl cs) (* -1 c) 0) "Gold" "Gold")

(sdegeo:create-rectangle (position (+ tch drift cs) 0 0) (position Ltot (* -1 c) 0) "Gold" "Gold")

(sdegeo:create-rectangle (position (+ sl cs) (* -1 is) 0) (position (+ tch drift cs) (* -1 (+ tox)) 0) "Nitride" "R.spacer")

(sdegeo:create-rectangle (position (+ sl sll) (* -1 is) 0) (position (+ tch drift) (* -1 (+ tox)) 0) "PolySilicon" "R.polygate")

(sde:define-parameter "fillet-radius-ls" 0.125 0.0 0.0)

(sdegeo:fillet-2d (find-vertex-id (position (+ sl cs) (* -1 is) 0.0)) fillet-radius-ls)

(sde:define-parameter "fillet-radius-rs" 0.125 0.0 0.0)

(sdegeo:fillet-2d (find-vertex-id (position (+ tch drift cs) (* -1 is) 0.0)) fillet-radius-rs)

(sdegeo:create-rectangle (position (+ sl sll) (* -1 (+ tox i c)) 0) (position (+ tch drift) (* -1 (+ tox i)) 0) "Gold" "Gold")

; Contact definitions

(sdegeo:set-contact (find-edge-id (position c (* -1 c) 0.0)) "4")

(sdegeo:set-contact (find-edge-id (position (+ sl sll c) (* -1 (+ tox i c)) 0.0)) "3")

(sdegeo:set-contact (find-edge-id (position (+ tch drift cs c) (* -1 c) 0.0)) "2")

(sdegeo:set-contact (find-edge-id (position (+ c) Ly 0.0)) "body")

; Doping Profiles:

; - Substrate (sdedr:define-constant-profile "Const.Substrate" "ArsenicActiveConcentration" 1e16)

(sedr:define-constant-profile-region ”PlaceCD.Substrate” ”Const.Substrate” ”R.Substrate”
)

(sedr:define-constant-profile ”Const.channel” ”BoronActiveConcentration” 1e17)

(sedr:define-constant-profile-region ”PlaceCD.channel” ”Const.channel” ”R.channel”)

(sedr:define-refeval-window ”BaseLine.drain” ”Line” (position 1.5 0.05 0.0) (position 1.8
0.05 0.0))

(sedr:define-gaussian-profile ”Gauss.drain” ”ArsenicActiveConcentration” ”PeakPos” 0.0
”PeakVal” 2.7e20 ”ValueAtDepth” 1e16 ”Depth” 0.25 ”Gauss” ”Factor” 1.2)

(sedr:define-analytical-profile-placement ”PlaceAP.drain” ”Gauss.drain” ”BaseLine.drain”
”Both” ”NoReplace” ”Eval”)

(sedr:define-refeval-window ”BaseLine.body” ”Line” (position -0.45 0.02 0.0) (position
0.2 0.02 0.0))

(sedr:define-gaussian-profile ”Gauss.body” ”BoronActiveConcentration” ”PeakPos” 0.0
”PeakVal”1.3e20 ”ValueAtDepth” 1e16 ”Depth” 0.6 ”Gauss” ”Factor” 0.9)

(sedr:define-analytical-profile-placement ”PlaceAP.body” ”Gauss.body” ”BaseLine.body”
”Both” ”NoReplace” ”Eval”)

(sedr:define-refeval-window ”BaseLine.source” ”Line” (position 0.505 0.05 0.0) (position
0.58 0.05 0.0))

(sedr:define-gaussian-profile ”Gauss.source” ”ArsenicActiveConcentration” ”PeakPos”
0.0 ”PeakVal” 2.7e20 ”ValueAtDepth” 1e15 ”Depth” 0.33 ”Gauss” ”Factor” 0.5)

(sedr:define-analytical-profile-placement ”PlaceAP.source” ”Gauss.source” ”BaseLine.source”
”Both” ”NoReplace” ”Eval”)

; - Poly (sedr:define-constant-profile ”Const.Gate” ”ArsenicActiveConcentration” 1e20
)

(sedr:define-constant-profile-region ”PlaceCD.Gate” ”Const.Gate” ”R.polygate”)

; Creating meshing:

(sedr:define-refeval-window ”RefWin.all” ”Rectangle” (position -0.2 -0.6 0) (position 2
6 0))

(sedr:define-refinement-size ”RefDef.all” 1 1 0.25 0.25)

(sedr:define-refinement-placement ”PlaceRF.all” ”RefDef.all” ”RefWin.all”)

(sedr:define-refinement-function ”RefDef.all” ”DopingConcentration” ”MaxTransDiff” 1)

(sedr:define-refinement-function ”RefDef.all” ”MaxLenInt” ”Silicon” ”Oxide” 0.001 1.5 ”DoubleSide”)

(sedr:define-refeval-window ”RefWin.drain” ”Rectangle” (position -0.01 -0.01 0) (position 1.7 1.3 0))

(sedr:define-refinement-size ”RefDef.drain” 1 1 0.005 0.005)

(sedr:define-refinement-placement ”PlaceRF.drain” ”RefDef.drain” ”RefWin.drain”)

(sedr:define-refinement-function ”RefDef.drain” ”DopingConcentration” ”MaxTransDiff” 1)

(sedr:define-refinement-function ”RefDef.drain” ”MaxLenInt” ”Silicon” ”Oxide” 0.0005 1.5 ”DoubleSide”)

(sedr:define-refinement-size ”Ref.sub” 1 1 0.05 0.05)

(sedr:define-refinement-function ”Ref.sub” ”DopingConcentration” ”MaxTransDiff” 1)

(sedr:define-refinement-region ”Placeref.sub” ”Ref.sub” ”R.Substrate”)

(sedr:define-refinement-function ”Ref.sub” ”MaxLenInt” ”R.Substrate” ”R.channel” 0.025 ”DoubleSide” ”UseRegionNames”)

(sde:build-mesh ”snmesh” ”-a -c boxmethod” ”n@node@msh”)

; Meshing the device structure ;(sde:build-mesh ”n@node@_LDMOS_msh”)

;(sde:save-model ”n@node@_LDMOS_sde”)

sdevice:

Input and Output Files

File { grid = ”@tdr@”

current = ”@plot@”

output = ”@log@”

plot = ”@tdrdat@”

parameter = ”@parameter@”

}

Electrical contacts

Electrode {

{ Name=”2” Voltage= 0.0 }

{ Name=”4” Voltage= 0.0 }

{ Name=”3” Voltage= 0.0 }

#{ Name=”body” Voltage= 0.0 }

}

For Thermal simulations

Thermode{

{ Name=”2” Temperature= @Tamb@ SurfaceResistance= 5e-4 }

{ Name=”4” Temperature= @Tamb@ SurfaceResistance= 5e-4 }

{ Name=”3” Temperature= @Tamb@ SurfaceResistance= 5e-4 }

}

Physics models

Physics {

AreaFactor= @AreaFactor@

Fermi

eSHEDistribution (-AdjustImpurityScattering FullBand)

}

Physics (Material= ”Silicon”) {

Mobility (

Enormal (IALMob(AutoOrientation))

HighFieldSaturation(EparallelToInterface)

)

Recombination(

SRH(DopingDependence TempDependence)

Avalanche

)

EffectiveIntrinsicDensity(OldSlotboom)

}

Plot{ eDensity hDensity

TotalCurrent/Vector eCurrent/Vector hCurrent/Vector

eMobility hMobility

eVelocity hVelocity

eQuasiFermi hQuasiFermi

Temperature

eTemperature hTemperature

ElectricField/Vector Potential SpaceCharge

Doping DonorConcentration AcceptorConcentration

SRH Auger Band2Band

AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

eGradQuasiFermi/Vector hGradQuasiFermi/Vector

eEparallel hEparallel eENormal hENormal

BandGapNarrowing ConductionBandEnergy ValanceBandEnergy

*–SHE Distribution

eBarrierTunneling hBarrierTunneling BarrierTunneling

eDirectTunnel hDirectTunnel eSHEDensity eSHEEnergy eSHEAvalancheGeneration

eSchenkTunnel hSchenkTunnel eSHECurrentDensity/Vector eSHEVelocity/Vector

eSHEDistribution/SpecialVector

hSHEDensity hSHEEnergy SHEAvalancheGeneration eSHEDistribution/SpecialVector

hSHECurrentDensity/Vector hSHEVelocity/Vector hSHEDistribution/SpecialVector

eTrappedCharge hTrappedCharge

```
eInterfaceTrappedCharge hInterfaceTrappedCharge
HotElectronInj
TotalInterfaceTrapConcentration
}
Math {
AvalDerivatives
Extrapolate
Notdamped= 50
Iterations= 120
Digits= 6
ErrRef(electron)= 1.0e10
ErrRef(hole)= 1.0e10
RHSmin=1e-20
SHECutoff=10
For Multi-threading
Number_of_threads= 4
ExitOnFailure
}
Solve {
coupled (iterations=100) { poisson }
coupled { poisson electron hole }
coupled { poisson electron hole temperature }
*- Vd sweep
Quasistationary(
InitialStep= 1e-4 MinStep= 1e-10 MaxStep= 1.0
Increment= 1.5 Decrement= 2.0
Goal { Name="3" Voltage= @Vg@ }
){ Coupled { Poisson Electron Hole Temperature } }
NewCurrentFile="IdVd"
*- Vg sweep
```

```
Quasistationary(
InitialStep= 1e-4 MinStep= 1e-10 MaxStep= 0.1
Increment= 1.5 Decrement= 2.0
Goal { Name="2" Voltage= @Vd@ }
)
{ Coupled { Poisson Electron Hole Temperature }
CurrentPlot( Time=(Range=(0 1) Intervals= 20 ) ) }
}
```

VITA

Bikram Kishore Mahajan was born in Agartala, Tripura, India in 1990. He received the B.Tech. and M.Tech. degrees in Electronics and Communication Engineering from National Institute of Technology, Agartala. In July 2016, he received M.S. degree in Mechanical Engineering from Missouri University of Science and Technology, Rolla at Missouri, USA. He has been with ALAM CEED Group since October 2017. He received Ph.D. degree in Electrical Engineering at Purdue University, West Lafayette, Indiana, USA in December 2021. His research focuses on electro- thermal and reliability modeling, and characterizations of advanced transistors (from thinfilm to power transistors). He is a recipient of Bilsland Dissertation Fellowship from Purdue University, and has authored and co-authored more than 25 journals and conference papers.