# RELIABILITY CHARACTERIZATIONS OF POWER TRANSISTORS: FROM SILICON TO OXIDE SEMICONDUCTORS

by

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This dissertation is dedicated to my wonderful parents with love,
who have raised me to be the person I am today.

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# ABSTRACT

Semiconductor power electronics find widespread use in miscellaneous applications, including power management in smart grids, electrical motors in self-driving cars, satellite power systems, and so on. In these high voltage systems, it is inevitable that the reliability issues at the transistor level, e.g., hot carrier degradation (HCD), bias temperature instability (BTI), and self-heating effect (SHE), would be prominent and must be carefully investigated. The geometrical and doping complexities of power transistors make their reliability issues very distinct from classical low-voltage logic transistors. Other than the classical material such as Si, commercialized wide bandgap (WBG) materials such as GaN and SiC, and emerging oxide semiconductors such as $\beta$-$Ga_2O_3$ and $In_2O_3$ have attracted researchers' attention. For example, $\beta$-$Ga_2O_3$'s ultra-wide bandgap (4.6 to 4.9 eV) makes it a promising candidate to compete with GaN and SiC. Amorphous $In_2O_3$, grown by atomic layer deposition (ALD), is demonstrated to possess high electron mobility (>100 $cm^2V^{-1}s^{-1}$). The reliability issues of the two emerging materials are worth exploring. As a result, this thesis can be divided into two major parts: silicon and oxide semiconductor. Our main contributions are new characterization techniques and reliability models, which are essential for integrated power systems.

In the first part of the thesis, the localized HCD in Si-based lateral diffused MOSFETs (LDMOSs) with different geometries and structures are explored by two new characterization methods. The first one is called "three-point I-V spectroscopy" and the other is called "Super Single Pulse Charge Pumping ($S^2$PCP)". The former technique extracts the mobility degradation percentage ($\Delta\mu$) in the channel and drift regions individually. The latter extracts the localized interface trap generation ($\Delta N_{it}$). $S^2$PCP is developed for the source-body-tied (SBT) LDMOS, in which the classical charge pumping techniques cannot function properly. The results from the two techniques compare well with each other, providing cross-validation of the techniques. For different types of LDMOS transistors under study, the channel region degradation is enhanced under higher $V_G$ bias. This channel degradation was then observed to be HCD-assisted anode hole injection (AHI) because of the stronger recovery, positive temperature activation, and negligible temperature dependence in gate leakage.

In the second part of the thesis, two emerging oxide semiconductors, β-$Ga_2O_3$ and $In_2O_3$ are studied. For β-$Ga_2O_3$, SHE is identified as a critical issue due to its low thermal conductivity. Therefore, the self-heating was included in circuit simulations, and indeed reveals a degradation in the efficiency of DC-DC boost conversion. The thermal resistance ($\theta_{th}$) of the bilayered structure is modeled, and its maximum current ($I_{max}$) and power ($P_{max}$) metrics are derived and estimated through analytical calculations. The choice of high-thermal-conductivity substrate, wafer thinning, etc, can help in mitigating SHE. However, extra effort is still vital to further improve β-$Ga_2O_3$ performance to outperform GaN and SiC. On the other hand, 1.2-nm-thick amorphous $In_2O_3$ thin-film transistors (TFTs) demonstrate promising electrical performances. Grown in a relatively low temperature (∼225 °C), it is recognized as a back-end-of-line (BEOL) compatible transistor. The reliability studies such as positive bias temperature stress (PBTS) and HCD are explored and modeled. Unlike traditional logic transistors, HCD is strongly correlated to PBTS, which is caused by the much stronger vertical field compared to the lateral field in the ultra-thin devices. Overall, the high-performance BEOL-TFTs are remarkably reliable, with a relatively small threshold voltage shift under PBTS/HCD stress conditions at room temperature.

# 1. INTRODUCTION

## 1.1 Background

Power electronic system has been widely used in aerospace, industrial automation, railway tractions, renewable energy conversion, wireless communication networks, etc. High efficiency, controllability, and durability are the most important concerns. Among various components that make an integrated system (e.g., inductors, capacitors, logic, and memory), the power transistor may often be the weakest link [1] because their continuous and high-voltage switching makes them susceptible to degradation and failure [2]. In recent years, therefore, there has been a worldwide effort to improve the long-term reliability of power transistors. To date, the common method to enhance the reliability of the power electronic system includes condition monitoring [3] and active thermal control [4]. The condition monitoring can be realized by having a real-time monitor on the characteristic quantities to prevent accidental shutdown. The active thermal control is implemented by reducing the excessive thermal stress to prolong the system lifetime. To quantify the rate of degradation at the operating conditions, one uses accelerated tests to determine the parameters necessary for lifetime projection [5]. It is sometimes possible to construct a universal curve based on the degradations measured at different voltages [6]. The required lifetimes for various applications are listed in Table 1.1. With a deeper understanding of the reliability of power devices, the power electronic system can achieve the requisite lifetime.

In terms of the applications and working principles of the power devices, they can be classified as power diode, silicon-controlled rectifier (SCR), thyristor, gate turn-off thyristor

**Table 1.1.** Typical power electronics lifetime requirements in various applications.

| **Application** | **Lifetime Requirement (years)** | **Ref.** |
|---|---|---|
| Electric Vehicle | 15-20 | [7] |
| String Inverter (Solar) | 5-10 | [8] |
| Micro Inverter (Solar) | 20-25 | [8] |
| Windmill | 20 | [9] |
| Industrial Converter | >10 | [10] |

(GTO), bipolar transistor, power MOSFET, insulated-gate bipolar transistor (IGBT). Their applications and operating voltages are shown in Fig. 1.1. Silicon power transistors allow inexpensive integration with logic and memory systems; however, the small-bandgap of Si limits their use in low-voltage applications. Wide bandgap (WBG) materials such as GaN, 4H-SiC, or β-$Ga_2O_3$, can be used for high-voltage applications (100 V to 10 kV) due to higher breakdown field ($E_{BD}$). Below the "Si limit", we will focus on lateral diffused MOS (LDMOS) as an illustrated example of Si power transistor; above the "Si limit", we will discuss the performance of β-$Ga_2O_3$ transistor. Regardless of the application, the high-voltage and high-frequency operations make hot carrier degradation (HCD) and self-heating effect (SHE) the most important reliability concerns. In this introductory chapter, we will briefly explain those reliability issues in the following subsection.

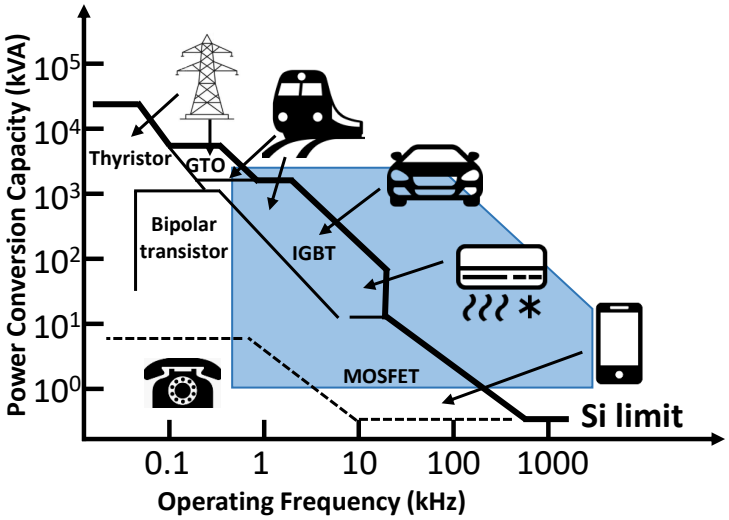



**Figure 1.1.** The classification of power devices and their application regimes. The thick line represents the Si limit. Our research focuses on the blue regions. Below the Si limit: LDMOS; above the Si limit: β-$Ga_2O_3$ transistor.

## 1.2 Hot Carrier Degradation (HCD)

HCD is caused by the accumulation of defects at or near the semiconductor/oxide interface. Those defects can be generated/trapped by the drain-field accelerated, high-energy

(hot) carriers bombarding the $Si/SiO_2$ interface [11], as depicted in Fig. 1.2. The hot carriers can cause impact ionization (II), generating electron-hole pairs. The secondary generated holes form the substrate current ($I_{SUB}$) and the electrons are injected into gate dielectric ($I_G$). Therefore, $I_{SUB}$ and $I_G$ can be used to measure the rate of HCD. The interface defects are measured by the interface trap density, $N_{it}$ (in the unit of $cm^{-2}$) or $D_{it}$ (in the unit of $eV^{-1}\,cm^{-2}$). Typically, the defects are spatially distributed in both position (along the channel) and energy (within the bandgap). These defects often lead to threshold voltage shift and transconductance degradation. The formation of defects outside the bandgap is normal but they do not affect electrical characteristics. In the following sections, we will introduce the HCD theory in both classical MOSFETs and non-classical power MOSFETs.

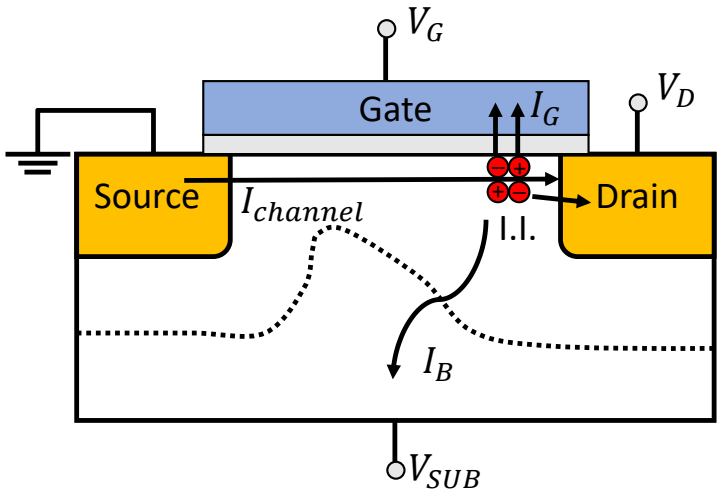



**Figure 1.2.** The schematic describes the hot carrier degradation (HCD) happens in a classical long-channel MOSFET.

### 1.2.1 HCD in Classical MOSFETs

Many theories have been proposed to describe HCD in terms of stress voltages and temperatures. One of the first successful physical models of long-channel MOSFET was the Lucky electron model (LEM) [12], [13], which predicted the probability of hot-electron (gaining high enough energy over the barrier) injection into the oxide in N-channel MOSFETs. As

described before, $I_{SUB}$ is caused by II, and $I_G$ is due to the electron injection. The general model is expressed as:

$$I_{SUB} = C_1 \cdot I_D \cdot e^{-\frac{\varphi_i}{q\lambda E_m}}, \tag{1.1}$$

$$I_G = C_2 \cdot I_D \cdot e^{-\frac{\varphi_b}{q\lambda E_m}}, \tag{1.2}$$

$$N_{it} = C_4 \left[ t \cdot \frac{I_D}{W} \cdot e^{-\frac{\varphi_i}{q\lambda E_m}} \right]^n. \tag{1.3}$$

Here, $E_m$ is the maximum electric field and $\lambda$ is the hot electron mean free path. $\varphi/qE_m$ is the required distance for an electron to travel to climb up the energy barrier $\varphi$. $\varphi_i$ is the barrier for impact ionization and $\varphi_{it}$ is the barrier for interface bond dissociation. Therefore, $e^{-\frac{\varphi}{q\lambda E_m}}$ describes the probability of an electron traveling a sufficient distance to gain sufficient energy without suffering a collision. Since $I_D$ is the rate of electron flow, multiplying with the current $I_D$ is the rate of supply of hot electrons.

Although the model must be generalized for short-channel devices, it is still widely used to interpret a variety of experiments. Later on, an empirical extension of LEM was proposed [14]. It suggests the degradation in power law ($\sim t^n$), which allows simple extrapolation of the acceleration tests. LEM defines the prefactors and the time exponent is usually independent of the stress condition and the temperature but changes with the dominant physical mechanism. In this formulation, the driving force of the HCD is the lateral peak electric field $E_m$, which governs the effective carrier temperature. On the other hand, another "energy-driven" paradigm was proposed afterward [15], [16], claiming that for a device smaller in scale with lower voltage bias, instead of the electric field, the high-energy electrons caused by electron-electron scattering (EES) should be the main driving force. The II rate and hot carrier lifetime are to the first order given by the energy dependences of the II scattering rate. In other words, the field-driven LEM, which is valid for long-channel and high-energy cases, is indeed a proxy of the energy-driven paradigm. In our hot carrier simulation in Technology Computer-Aided Design (TCAD), the energy-driven paradigm was always assumed.

In long-channel devices, the worst case of HCD is $V_G \sim V_D/2$ when the combination of carrier concentration and an electric field is high enough so that the impact ionization is

maximal. In this case, the interface trap generation is the root cause [18]. However, for short-channel devices, the worst case of HCD is $V_G \sim V_D$, where the charge injection into the oxide dominates [18], [20]. It is clear from Fig. 1.3(a) that when $V_G \sim V_D/2$, the higher field accelerates the electrons near the drain-side, making HCD more severe. Fig. 1.3(b) shows that the time exponent $n$ of $V_{th}$ shift changes from 0.6 to 0.1 with the increase of $V_G$, manifesting the domination of charge injection.

### 1.2.2 Non-Classical HCD in Power MOSFETs

The power MOSFETs evolve from logic transistors; therefore, it is not surprising that the early researchers followed the low-voltage HCD models to interpret the degradation of power MOSFETs. For example, laterally diffused MOSFET (LDMOS, as shown in Fig. 1.4(a)), the most widely used power device in RF power amplifier [21], has evolved from classical MOSFETs with a more complex doping structure to sustain higher drain bias (will be introduced more in detail later). The extended and lowly-doped N-type drift region enhances the breakdown voltage. In interpreting the HCD results in LDMOS, researchers found it necessary to use empirical forms that consist of two or several degradation terms to describe

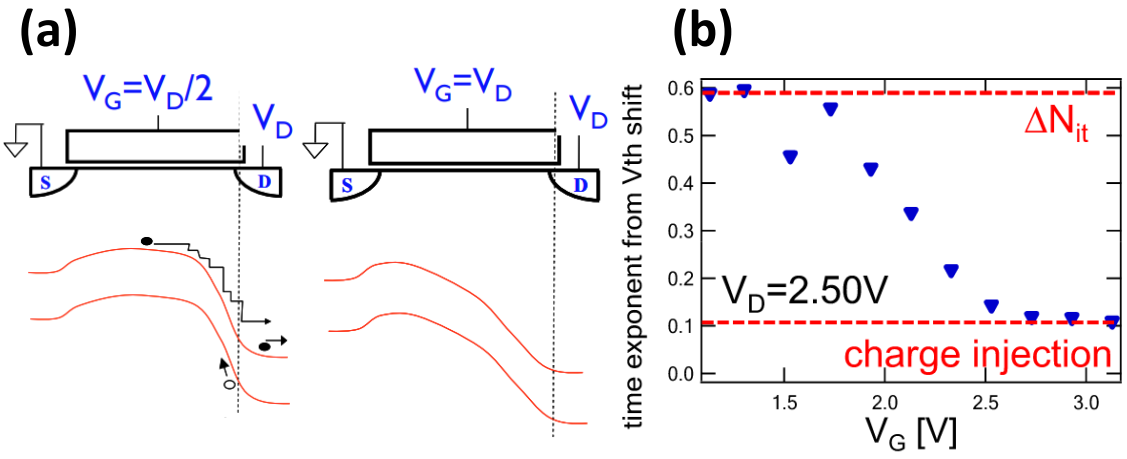



**Figure 1.3.** (a) The band diagram for two worse cases of HCD. The picture is taken from Ref. [17]. (b) The time exponents obtained by fitting $\Delta V_{th}$ with power law. The figure is taken from Ref. [18], which is done on devices with gate length of 250 nm.

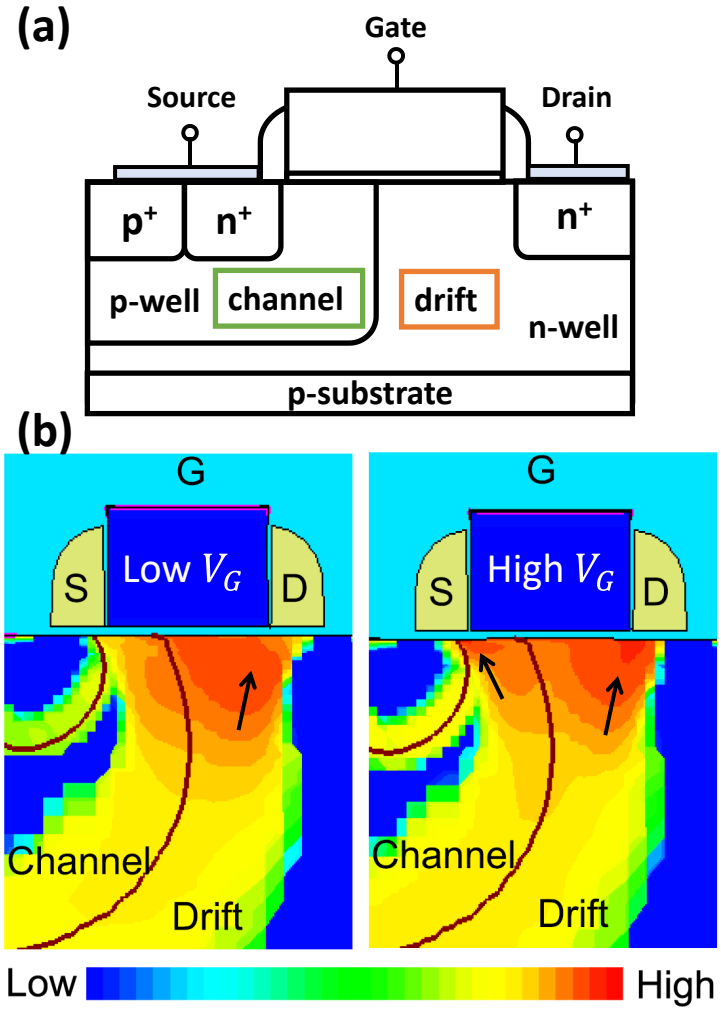



**Figure 1.4.** (a) The simplified schematic of the LDMOS transistor under study. (b) The TCAD simulation of an LDMOS under two different hot carrier stress conditions. The figure is taken from Ref. [19]. The arrows indicate the presence of hotspots.

the overall behavior [22], presumably because different regions of the LDMOS degrades with different time exponents and bias-dependent prefactors [21], [22]. As an example, Fig. 1.4(b) shows that, unlike the classical MOSFETs, at some stress conditions, II not only happens near the drain, but another "hotspot" appears in the channel region [19]. The main reason is its doping and structure complexity. However, the physical legitimacy of this hypothesis is still a concern, the degradations of individual regions have not been quantified, and a phys-

ically correct unified degradation model is missing. One of the difficulties toward a unified degradation model is due to the wide diversity of power device strictures. It is still not clear if the empirical model developed for one group of transistors (LDMOS) can be transferred to other groups of transistors (e.g., IGBT).

In this thesis, we will show that the complexity of HCD degradation leads to the spatial separation of the degradation associated with each local hotspot in a power transistor. In general, if a device is characterized by two or more hotspots, the extended power law model is often applied onto the individual region, and they are simply added up when they both contribute to the overall degradation [19], [23]. Taking the linear drain current degradation, $\Delta I_{D,lin}$ as an example,

$$\Delta I_{D,lin} = \frac{A_{ch} t^m}{1 + B_{ch} t^m} + \frac{A_{dr} t^n}{1 + B_{dr} t^n}. \tag{1.4}$$

The denominator term accounts for the saturation behavior, and the index "$ch$" and "$dr$" refer to two distinct regions.

In other words, after obtaining the device degradations from the experiments, one must deconvolve the degradation, develop measurement techniques, and compact models to characterize the exponents, and finally integrate them such that the HCD degradation can be predicted for arbitrary combinations of terminal voltages and operating temperature. This is the motivation of the new characterization methods developed in Chapters 3 and 4.

## 1.3 Self-Heating Effect (SHE)

### 1.3.1 The Evolution of Self-Heating Effect

SHE is another important issue for power electronic devices, and it can often be correlated to the inefficiency of heat dissipation especially for devices with new materials or new structures. The high lattice temperature $T_L$ will degrade the mobility (and hence the current) in the channel because of the participation of phonon scattering [24]. The lattice temperature $T_L = T_A + (P_D \times \theta_{th})$, where $T_A$ is the ambient temperature, $P_D$ is the power dissipated by a transistor, and $\theta_{th}$ is the thermal resistance. It indicates that the temperature will get higher for higher power and higher thermal resistance. In the early 1970s, Keyes was

the first to appreciate the importance of SHE as a performance limit of modern electronics. He showed that the thermal resistance $\theta_{th}$ depends on effective thermal conductivity, $\kappa$, and transistor-substrate shape-factor, $\beta$, as $\theta_{th} = \beta/(\kappa\sqrt{A})$. With transistor area $A$, the power density $P_0 = P_D/A$. Taken together: $T_L = T_A + P_0\sqrt{A}\ \beta/\ \kappa$ [25]. With the scaling of transistor area, the power density $P_0$ has increased from 1 to 100 W/cm$^2$ between 1985 and 2005 [26]. It shows that the self-heating issue will naturally be more and more detrimental. For modern MOSFETs with multi-gate or gate-all-around (GAA) topologies, the situation is getting worse due to the narrower gate geometry and smaller gate pitch [27], [28]. The evolution of $\theta_{th}$ is summarized in Fig. 1.5. In terms of power devices, their high-voltage capacities also make SHE a serious problem. To address this issue, one must increase the effective thermal conductivity, $\kappa$. For example, GaN-based high electron mobility transistors (HEMTs) can reduce SHE by adopting high thermally conductive substrates such as Si and diamond [29], [30], or adding a heat-spreading layer [31]. The focus of the thesis is to numerically and analytically estimate the intrinsic performance limitation of WBG power transistors, especially for $\beta$-$Ga_2O_3$.

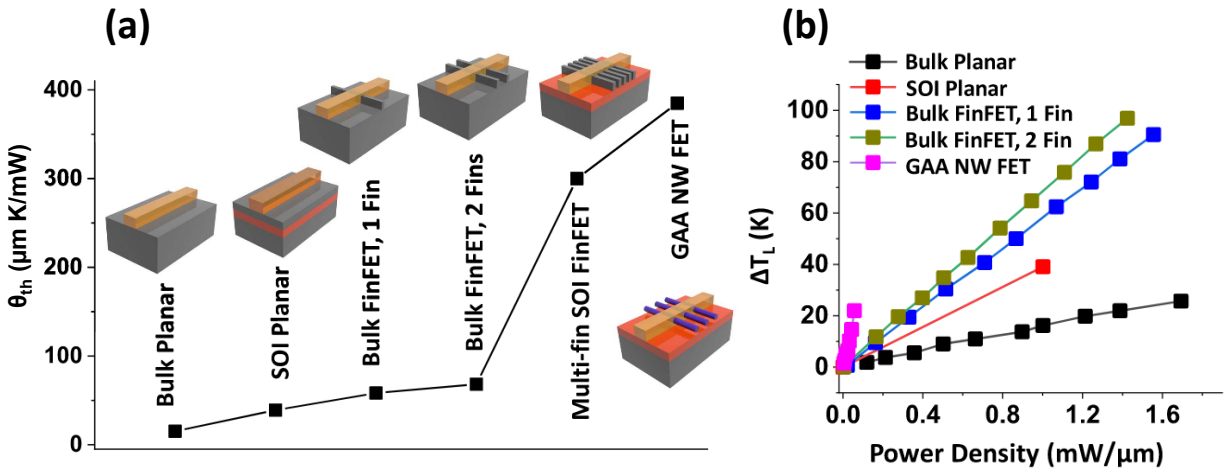



**Figure 1.5.** (a) Thermal resistance ($\theta_{th}$) of bulk, silicon-on-insulator (SOI) planar, and FinFETs. (b) Measured temperature rise ($\Delta T_L$) as a function of power density with various configurations.

### 1.3.2 Correlation of SHE and HCD

When both HCD and SHE are present, the rising temperature affects the HCD. Whether SHE mitigates or worsens HCD depends on the dimension of the transistors. The phenomenological theory of HCD can be written as:

$$\frac{dN_{it}(E_B, x, t)}{dt} = \sum_{E_B, x} k_f(E_B, T_e,\ T_L)\left(N_0(E_B, x) - N_{it}(E_B, x, t)\right). \tag{1.5}$$

$N_0(E_B, x)$ is the initial number of unbroken bonds with the binding energy $E_B$, located at a distance $x$ from the source. $N_{it}$ evolves with time so that the remaining Si-H and Si-O bonds, $N_0 - N_{it}$, and the forward reaction rate, $k_f$, determine the instantaneous dissociation rate. The temperature participates in the HCD process in the $k_f$ term since it is $T_L$-dependent (lattice temperature). It reflects that the cooling of energetic electrons at high temperature vs. the increase in the bond-dissociation probability at high temperature determines it is either positively or negatively temperature-activated. For long-channel high-voltage devices such as LDMOS, the first factor prevails, so that SHE can mitigate the HCD owing to the activation of optical phonons, which acquire the energy from hot carriers through electron-phonon scattering [32]. However, the story is quite different for scaled three-dimensional transistors such as FinFETs and GAA FETs. Biasing at lower voltages, EES [33] exclusively defines the high-energy tail of the energy distribution function (EDF) [34] (because impact ionization is absent). Moreover, since this EES-defined tail has energy lower than the bond-dissociation energy, the positive activation energy of bond-dissociation defines HCD.

Taking one step further, in the system perspective, actual system operating conditions may either improve or acerbate the reliability challenges. There are some debates on how to project the test results to the use conditions. Some reliability-aware circuit designs [35] can help to mitigate the reliability issues. Finally, SHE is not only important for the reliability of power transistors but also neighboring components in a packaged system. In a buck-boost converter, for example, the temperature-dependent shift of the integrated inductance can contribute to the distortion of the output characteristics. The consideration of SHE draws

an upper limit of the device driving current for reliable operations. This is an important topic especially for emerging materials under development.

## 1.4 Characterization of Interface Defects

The defects at semiconductor/oxide interface ($N_{it}$ or $D_{it}$), which formed by the dangling bonds, is crucial because it induces threshold voltage shift ($\Delta V_{th}$) and carrier mobility degradation ($\Delta\mu$). It can be either positively or negatively charged, depending on its type and whether it is occupied by an electron or not. The acceptor-like defect is negatively charged when filled with an electron, and neutral when it is empty. The donor-like defect is positively charged when empty, and neutral when it is filled by an electron, as depicted in Fig. 1.6. It is widely accepted that the defects above mid-gap are acceptor-like and donor-like below mid-gap [36]. The dynamic of the interface defect occupancy causes the stretch-out of the C-V curves, as shown in Fig. 1.7.

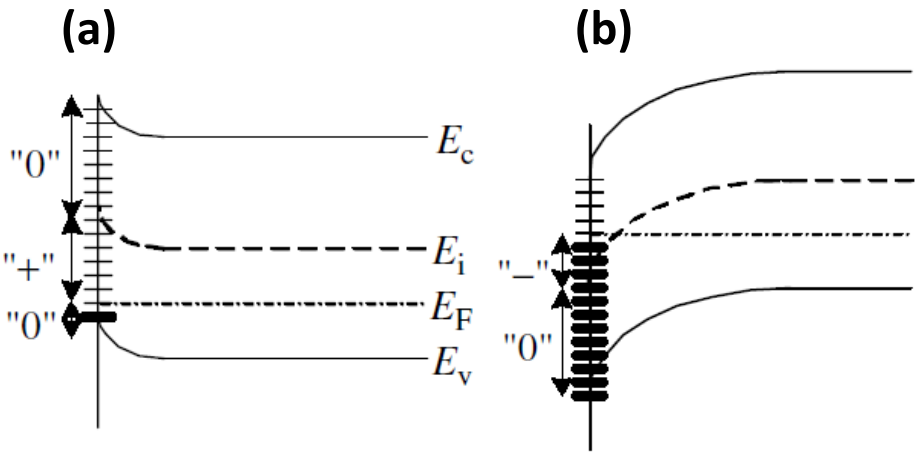



**Figure 1.6.** The position of the fermi level determines the sign of interface charge: (a) $V_G < 0$ and (b) $V_G > 0$.

Many techniques were developed to monitor the interface traps experimentally, including subthreshold current [37], high/low frequency [38], DCIV [39], AC conductance [40], deep-level transient spectroscopy (DLTS) [41], charge pumping (CP) [42], [43], etc. These techniques have their limitations and the detected energy range within the bandgap. With

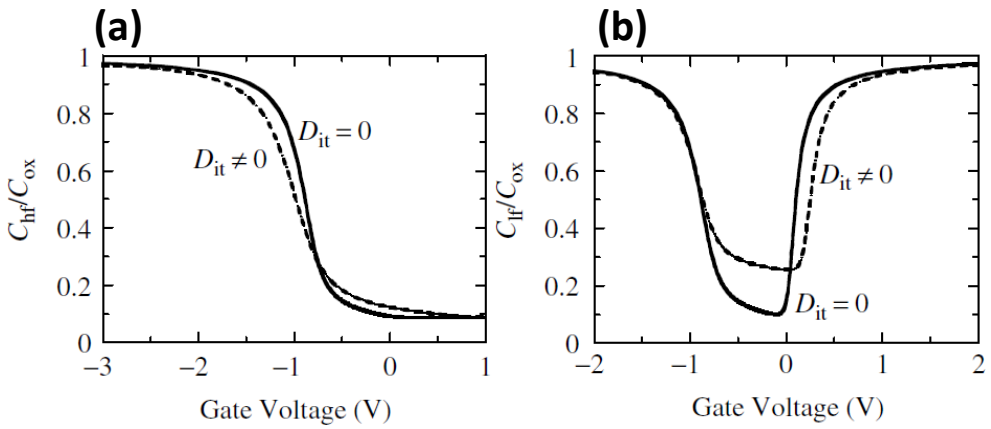



**Figure 1.7.** The change in C-V curve at (a) high frequency and (b) low frequency when considering $D_{it}$.

the stress applied on the devices, the interface defect density increases with stress time, which is reflected in current degradation with time. Therefore, it is important to quantify the evolution of $N_{it}(x,t)$ as a function of stress voltages. Different from classical MOSFET, LDMOS transistors have more complicated doping profiles and structures, hence the techniques may or may not work properly. In this thesis, we will develop new characterization methods to monitor the LDMOS transistor degradation under stress.

## 1.5 Outline of Thesis

The thesis consists of 8 chapters. Chapter 2 to 5 is the first part, focusing on the Si-based LDMOS transistors, the model, and characterization techniques developed based on LDMOS transistors. In Chapter 2, we develop the tandem-FET compact model for the LDMOS transistors. Based on the compact model, in Chapter 3, the three-point analytical equations are derived along with the I-V spectroscopy concept to deconvolve the regional degradations under hot carrier stress. Apart from that, in Chapter 4, a new charge pumping technique (Super Single Pulse Charge Pumping, $S^2$PCP) will be proposed to allow direct detection of $\Delta N_{it}$ under stress. It will be compared with the results obtained in Chapter 3. Chapter 5 investigates the root cause of the abnormal channel degradation in an LDMOS.

We will provide several aspects to demonstrate the involvement of Anode Hole Injection (AHI).

Chapter 6 and 7 focus on the reliability assessment of emerging WBG materials such as β-$Ga_2O_3$ and $In_2O_3$. In Chapter 6, the electrothermal limitation of β-$Ga_2O_3$ is explored by $\theta_{th}$ evaluations and circuit simulations. The derived maximum current and power ($I_{max}$ and $P_{max}$) metrics developed can be used to estimate the stand-alone device performance given the materials and dimensions. In Chapter 7, the reliability issues of the high-performance ultra-thin $In_2O_3$ thin-film transistors (TFTs) are scrutinized. Unlike classical MOSFET, its HCD and Positive Bias Temperature Instability (PBTI) are correlated. A unified model will be proposed and fitted to explain the three mechanisms involved. Finally, Chapter 8 will be the summary, future work, and concluding remarks.

# 2. LATERAL DIFFUSED MOS (LDMOS)

## 2.1 Introduction to LDMOS

Due to their compatibility with the standard CMOS manufacturing process and low on-resistance ($R_{on}$), Lateral Diffused MOS (LDMOS) transistors are widely used in medium- and high-voltage applications such as automotive, display drivers, digital audio, power management, etc. Unlike the logic devices which operate in lower voltages, LDMOS needs to sustain higher voltage over tens or even hundreds of volt. Design innovations such as field plates [44], either LOCal Oxidation of Silicon (LOCOS) or Shallow Trench Isolation (STI), and RESURF (REduced SURface Field) [45] are employed in LDMOS transistors to achieve high breakdown voltage ($V_{BD}$). Fig. 2.1 shows the evolution of the LDMOS from a classical MOSFET and a Drain-extended MOS (DEMOS). A long- and lowly-doped drift region can

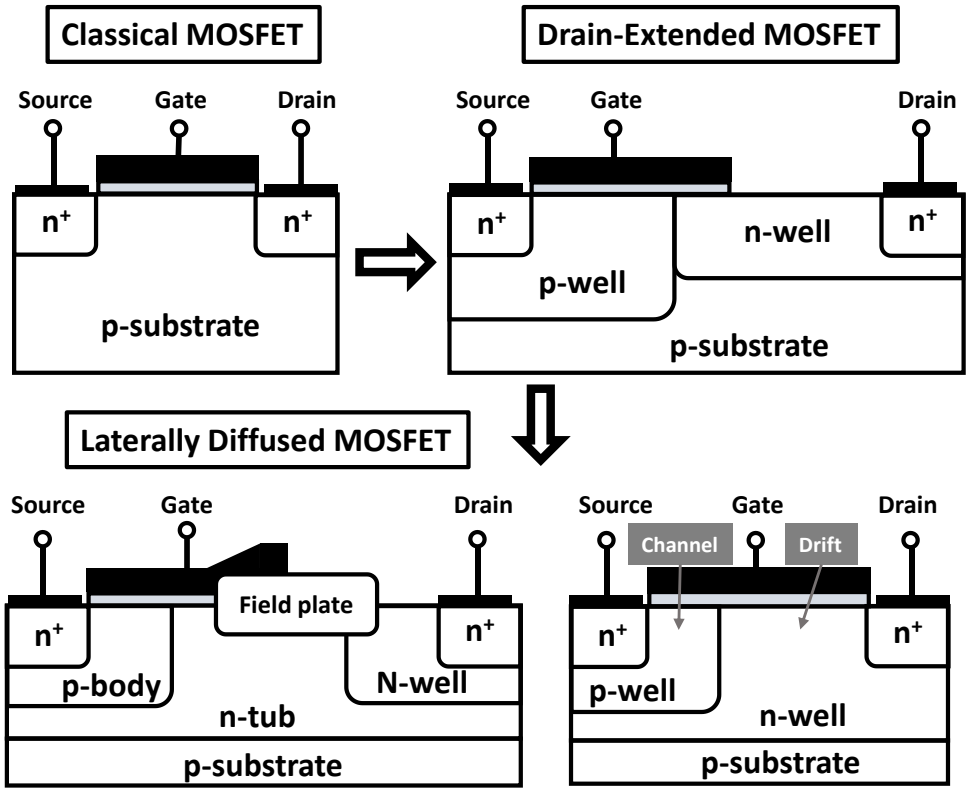



**Figure 2.1.** The evolution of LDMOS from classical MOSFET and Drain-Extended MOSFET (DEMOS).

be added into the fabrication process without extra process efforts and can help increase the breakdown voltage. DEMOS can thus be integrated for I/O applications. To further increase its breakdown voltage, a field plate (thick oxide) is often grown on the drift region. However, their higher operating voltage and temperature compared to traditional MOSFETs make them susceptible to a variety of reliability issues including HCD [25], [46]. As a result, the geometry and doping profiles of LDMOS transistors are tailored on a case-by-case basis to achieve application-specific targets for integration density, power-handling capability, and reliability.

In this thesis, we focus on two types of LDMOS: the low-to-medium-voltage one (bottom-right of Fig. 2.1) and medium-voltage (bottom-left of Fig. 2.1). In this chapter[1], we will review several ways people have adopted to construct LDMOS compact models. Afterward, the tandem-FET compact model will be proposed and validated by experiments.

## 2.2 The Literature Review of LDMOS Compact Models

The diversity of LDMOS geometry is reflected in the diversity of the compact models used to analyze the performance of LDMOS transistors. One approach is to use TCAD modeling. However, computational complexity makes the circuit implementation difficult. Instead, compact models offer a balance between accuracy and speed. The general compact modeling strategy involves splitting the LDMOS into an intrinsic MOSFET connected with a drift region. In this section, we will review some existing approaches to model an LDMOS transistor. One approach involves modeling the channel as a surface-potential-based bulk MOSFET compact model (PSP) and the second drift region with an R3 model [47], as indicated in Fig. 2.2 [48]. R3 is a nonlinear three-terminal compact model for JFETs. The depletion pinching formulation and empirical velocity saturation are critical in modeling quasi-saturation in LDMOS transistors. The effect of the drift region is included as a series resistance in the PSP model by modifying the effective mobility. The potential at the internal drain (DI) point is critical to be accurately modeled because it determines the impact ionization currents (the two current sources) for each region.

[1]↑The content of this chapter is taken from our publications [23]

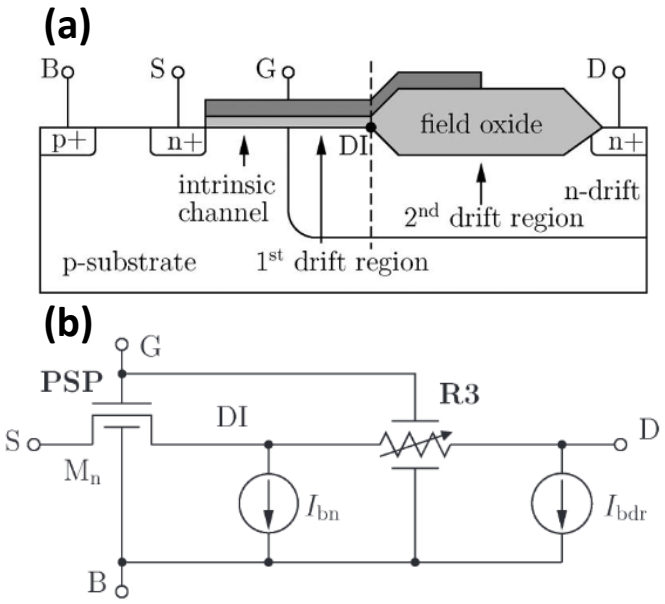



**Figure 2.2.** (a) The schematic of the LDMOS with a field oxide. (b) The equivalent circuit decomposing the device into two parts. Pictures are taken from Ref. [48].

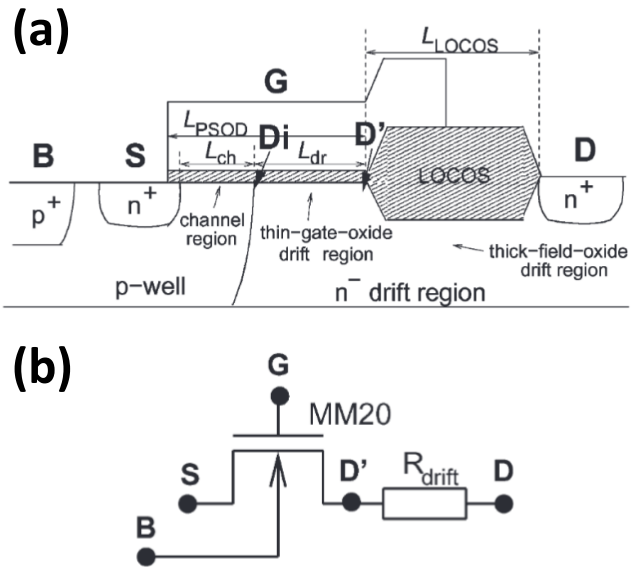



**Figure 2.3.** (a) The schematic of the LDMOS with LOCOS as the field oxide. (b) The equivalent circuit decomposing the device into two parts. Pictures are taken from Ref. [49].

Another approach people have developed is similar to the first one. Since the gate voltage can hardly influence the LOCOS region, the current spread out below the thick oxide. The LOCOS region is represented as a constant resistance $R_{drift}$, as shown in Fig. 2.3. The value of this resistance is:

$$R_{drift} = \frac{L_{LOCOS}}{W} R_{sheet}. \tag{2.1}$$

Here, $W$ and $L_{LOCOS}$ is the width of the device and the length of the LOCOS region. $R_{sheet}$ is the sheet resistance of the LOCOS drift region. The MOS Model 20 (MM20) was used to model the intrinsic MOS region.

To summarize, the LDMOS modeling is always divided into two building blocks. The intrinsic MOSFET part can be modeled by square-law model [50], PSP model [48], BSIM [51], or EKV model [52]. The drift region can be modeled by a non-linear resistance [49], R3 [48], distributed variable resistors [53], etc. The internal node is a key quantity to ensure its physical correctness.

## 2.3 Compact Modeling of LDMOS: Tandem-FET Model

### 2.3.1 Tandem-FET Model and I-V Matching

In Chapters 2 and 3, we will use the N-channel LDMOS transistors without field oxide, fabricated on silicon wafers by Texas Instruments as shown in Fig. 2.4(a). Dimensions and doping profiles have been optimized to achieve the breakdown voltage of 13 V, making it suitable for medium-voltage applications, such as automotive parts (e.g., switches, airbag deployers), health-care equipment (e.g., implantable defibrillators, insulin pumps, glucose meters, neural stimulator), etc. For this specific class of devices, the gate fully covers both the channel and drift regions, and the body and source contacts are tied together to eliminate the parasitic junction capacitances. Also, since the drift region is made of N-type silicon, it cannot be described by an R3 model (JFET-like resistor) [47], making it necessary to develop a new compact model for performance and reliability predictions.

In an intuitively simple approach, the drift region can be treated as a normally-on MOSFET, as shown in Fig. 2.4(b). In other words, the LDMOS can be represented by two

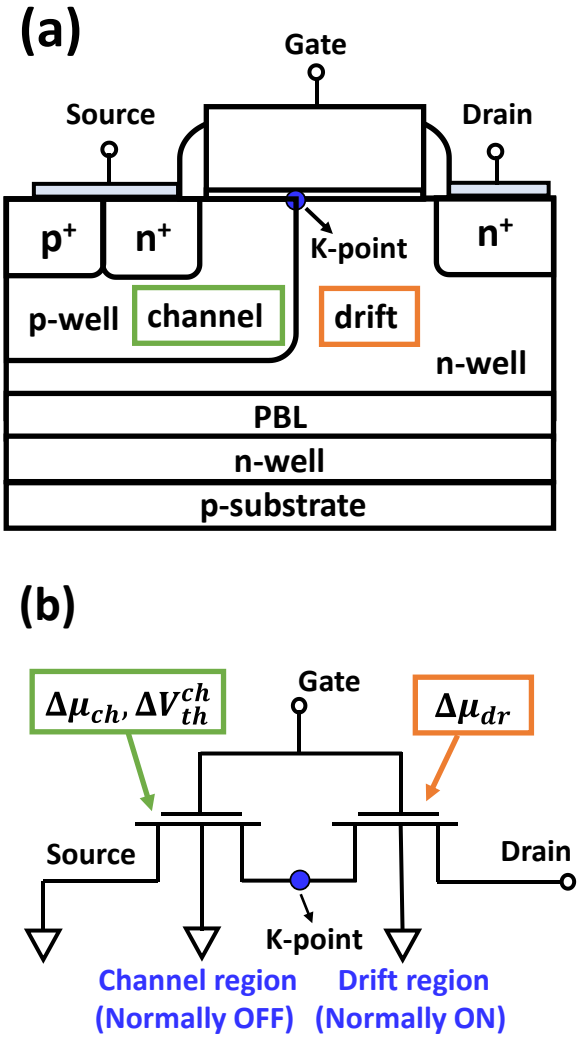



**Figure 2.4.** (a) The schematic of the LDMOS used in this study. PBL stands for P-buried layer. (b) The channel ($ch$) and the drift ($dr$) regions function individually as a MOSFET with different $V_{th}$ and dimensions. Three adjustable degradation parameters are $\Delta\mu_{ch}$, $\Delta V_{th}^{ch}$, and $\Delta\mu_{dr}$.

MOSFETs connected in series (tandem-FET) with two different threshold voltages and geometric dimensions. Compared to the approaches summarized in the previous section, this tandem-FET model is more straightforward, enabling the derivations of its analytical representation (Chapter 3). Each MOSFET is described by its BSIM6 representation [54] with the corresponding $V_{th}$, $\mu$, and geometric dimensions. This decomposition is particularly helpful because it allows the independent variations of the mobility ($\Delta\mu$) and threshold volt-

age ($\Delta V_{th}$) degradations in the channel and drift regions under HCD. Here, $\Delta\mu$ refers to the degradation of low-field mobility, assuming the field-dependent term of BSIM6 does not change after HCD. We will see in the next chapter that the characteristic features of the I-V characteristics are uniquely correlated to the mobility and threshold voltage degradations in the respective regions. Overall, the proposed tandem-FET compact model is convenient for reliability analyses.

To validate the tandem-FET compact model, the LDMOS is first numerically simulated by the TCAD Sentaurus simulator [55]. The transport and doping models were chosen carefully so that the TCAD model can self-consistently predict not only the device performance of the pristine device but also the device performance under stress.

Fig. 2.5 shows that the tandem-FET compact model accurately reproduces both the output ($I_D - V_D$) and the transfer ($I_D - V_G$) characteristics (both in linear and semi-log scale) obtained by experiments and Sentaurus TCAD simulations. The slight rise of $I_D$ at large $V_D$ reflects the impact ionization. The effect could have been implemented as a current source, as in Fig. 2.2. Since we will be using the model primarily in the normal operating region ($V_D < V_{BD}$), the current source would not play an significant role.

### 2.3.2 $V_K$ Matching

As mentioned before, the potential at the metallurgical junction is a key parameter. The transition voltage, $V_K$, at the metallurgical junction separating the channel and drift regions, as a function of the gate and drain voltages, are shown in Fig. 2.6. The accurate modeling of the transition voltage is crucially important for the hot carrier modeling of LDMOS because it determines the relative voltage drops across the channel and the drift region as a function of terminal bias conditions. The voltage drops, in turn, control the peak electric field, impact ionization, and hot carrier injection of the respective regions [48]. This transition is reflected in the saturation of $V_K$ as a function of $V_G$ in Fig. 2.6(a). These results demonstrate that our proposed tandem-FET compact model does capture the complexity of the internal voltage distribution of an LDMOS transistor. It shows that as the $V_G$ increases, $V_K$ increases and then decreases (or saturates). The reason is that at lower $V_G$, the channel resistance is

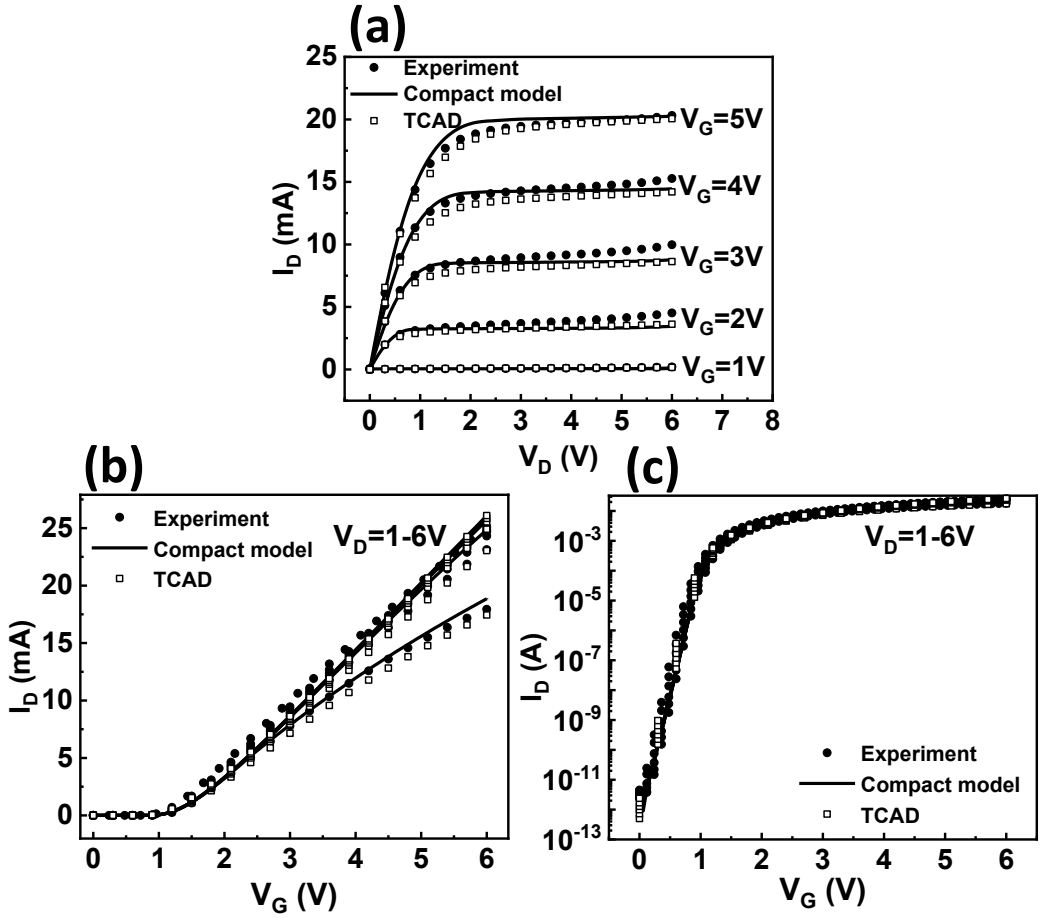



**Figure 2.5.** The comparison of the experimental I-V curves by the proposed tandem-FET compact model and calibrated TCAD simulations: (a) $I_D - V_D$; (b) linear $I_D - V_G$; (c) semi-log $I_D - V_G$. They coincide very well with each other. The HSPICE code is provided in Appendix A.1.

dominated over the drift region. As $V_G$ increases, the channel resistance starts to drop and reaches a peak or saturation point. At higher $V_G$, the drift resistance becomes higher than the channel resistance hence a large portion of $V_D$ drops on the drift region. A similar trend can be found in Fig. 2.6(b), $V_K$ vs. $V_D$ plot.

### 2.3.3 C-V Matching

Capacitance-voltage is another important electrical property to ensure an accurate modeling of a transistor, especially for AC transient simulations. Several capacitances such as

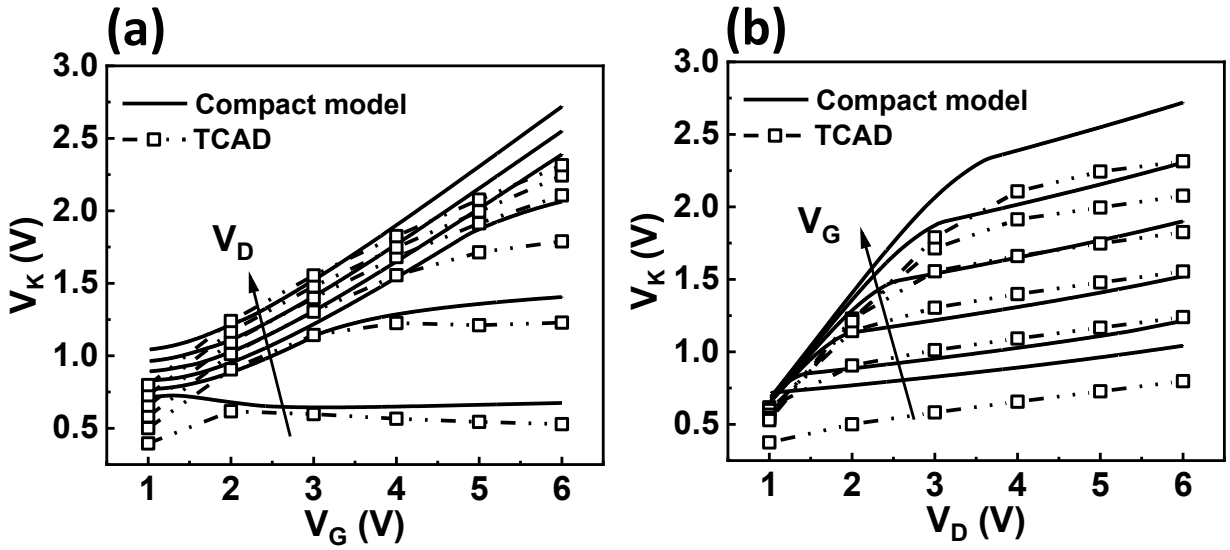



**Figure 2.6.** $V_K$ matching from the compact model (line) to the TCAD simulations (open square): (a) $V_K - V_G$ at fixed $V_D$; (b) $V_K - V_D$ at fixed $V_G$.

$C_{gg}$, $C_{gs}$, $C_{gd}$ were calibrated against experimental results by adjusting the parameters in BSIM6 for each region individually, as shown in Fig. 2.7. The C-V experiments were conducted with Agilent E4980A Precision LCR Meter, using an auto-balancing bridge under parallel mode. The small AC signal is with an amplitude of 50 mV and a frequency of 100 kHz. The differential capacitance described here,

$$C_{xy} = \partial Q_x / \partial V_y, \tag{2.2}$$

where the index $x$, $y$ can be either gate (g), drain (d), source (s), or body (b). $C_{gg}$ (also called input capacitance, as shown in Fig. 2.7(a)) is measured by connecting the gate terminal at the high-potential end and both the source and drain terminals at the low-potential end. It consists of $C_{gs}$, $C_{gd}$, and $C_{gb}$ in parallel. On the other hand, $C_{gs}$ ($C_{gd}$) is measured by connecting the gate terminal as the high-potential end and source (drain) terminal as the low-potential end while guarding the irrelevant terminal, drain (source) terminal to eliminate the stray capacitances. The matching of simulated C-V curves to the experimental results is shown in Fig. 2.7.

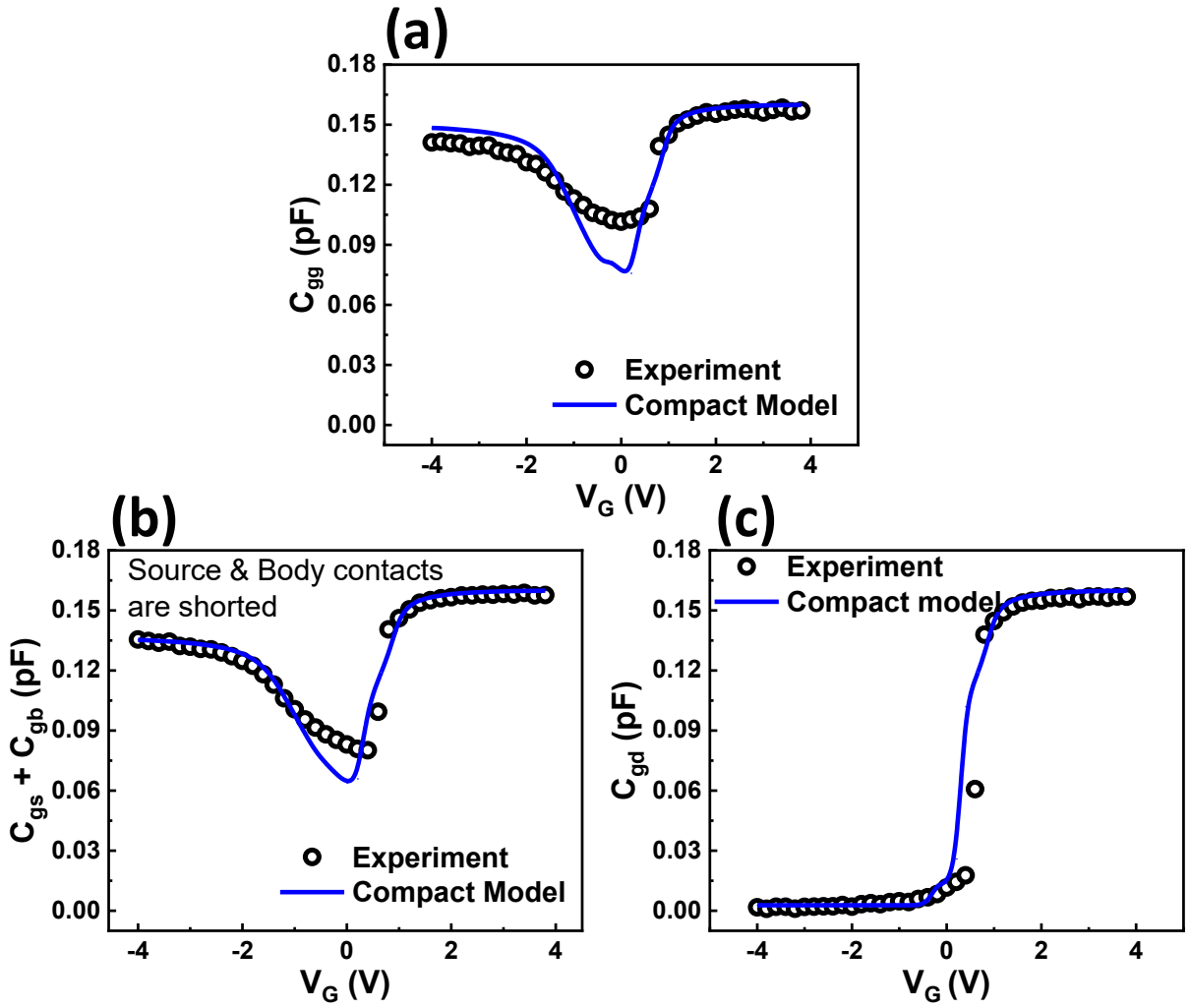



**Figure 2.7.** The capacitance matching from the compact modeling (line) to the experimental data (open circle): (a) $C_{gg}$ (b) $C_{gs}+C_{gb}$ (c) $C_{gd}$ vs. $V_G$. The HSPICE code is provided in Appendix A.2.

Note that because of the source-body-tied (SBT) configuration of the device under study, the measured $C_{gs}$ of this LDMOS transistor also consists of $C_{gb}$ of the channel intrinsic MOS. $C_{gb}$ mainly contributes to the capacitance of the negative $V_G$ branch, as shown in Fig. 2.7(b). The comparison demonstrates that the compact model catches the essence of device C-V fairly well. The slight underestimation in Fig. 2.7(b) may be due to the mismatch of $C_{gb}$, which is emulated by shorting the source and body contacts in the HSPICE simulation. One

the other hand, Fig. 2.7(c) shows a nearly perfect $C_{gd}$ matching. The rise of capacitance at $\sim$0 V confirms that the drift region can be treated as a normally-on NMOS with $V_{th} = 0$ V.

## 2.4 Conclusions

In this chapter, we propose a new LDMOS compact model based on BSIM6, which is convenient for the measurement phase in a reliability characterization. While most groups tend to model the drift region by a nonlinear model including velocity saturation, our approach allows direct mobility monitoring. Our innovative approach to model can also lead us to the simplified analytical form derived in Chapter 3. Since both its I-V (DC) and C-V (AC response) are well-calibrated, it is ready to be utilized to deconvolve the hot carrier damages in two separate regions.

# 3. THREE-POINT I-V SPECTROSCOPY DECONVOLVES REGIONAL DAMAGES

In Chapter 2, we have introduced a new way to construct the LDMOS compact model. In this chapter[1], we will use the concept to derive its simple analytical form to assist in obtaining the regional damages in mobility and shift in threshold voltage. Although other groups also developed equivalent circuits to separate the transistor into several parts and adjusted the corresponding parameters to mimic the localized degradation [57], [58], the distinctive feature of the analytical model proposed here allows direct extraction of the critical transistor parameters from the characteristic points of the degradation spectrum. Remarkably, the compact model and its analytical form are proved to deliver comparable results. Before utilizing the compact model to fit the experimental data, we need to introduce a new concept 'I-V spectroscopy' to help analyze the regional damage in an LDMOS transistor.

## 3.1 Hot Carrier Stress and I-V Spectroscopy

The schematic of N-channel LDMOS transistors, fabricated on Silicon wafers, is shown in Fig. 3.1(a). The HCD tests are conducted by applying a constant voltage stress ($V_{D(s)}$, $V_{G(s)}$) to generate interface defects and the consecutive $I_D - V_G$ measurements ($V_{D(m)}$, $V_{G(m)}$) to quantify the defects generated. This stress-measure-stress sequence is shown on the right-hand side of Fig. 3.1(a). For the illustrative example shown in Fig. 3.1, the stress conditions are $V_{D(s)} = 8$ V, $V_{G(s)} = 2, 4, 8$ V. During the measurement phases, $V_{D(m)}$ is kept at 0.1 V so that the measured current, sweeping of $V_{G(m)}$ from 0 V to 5 V is the linear current (Fig. 3.1(b)). From each $I_D - V_G$ sweep, one can obtain $\Delta I_{D,lin}(t)$ and $\Delta V_{th}(t)$ after stress time $t$ (all $I_D$ in this chapter are obtained in the measurement phase). Here, $I_{D,lin}$ is defined at $V_{G(m)} = 5$ V, $V_{D(m)} = 0.1$ V and $\Delta V_{th}(t)$ is evaluated by determining the shift in $V_{G(m)}$ needed to keep the constant current at 10 µA (i.e., the constant current method [59]) because $\Delta V_{th}(t)$ calculated using the maximum transconductance method is found to be contaminated by severe mobility degradation [23].

[1]↑The content of this chapter is taken from our publications [56]

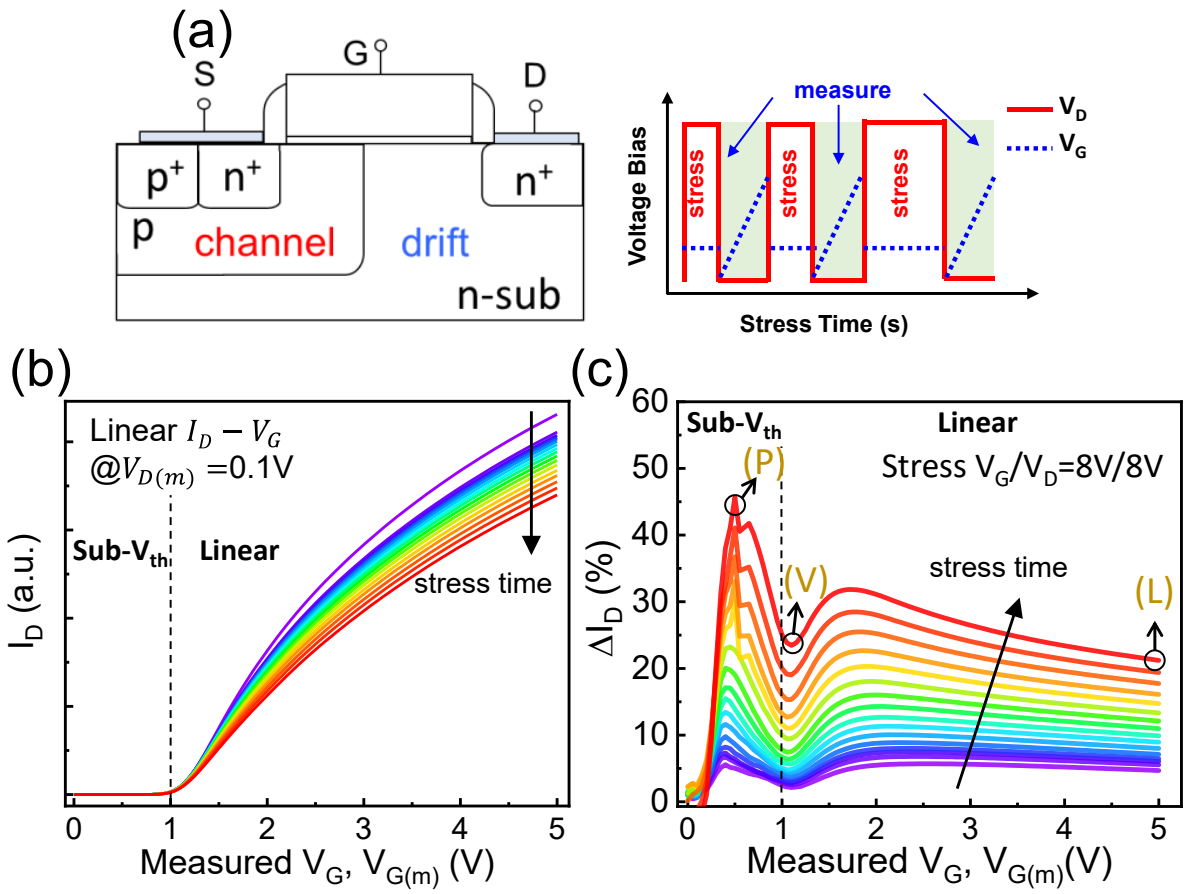



**Figure 3.1.** (a) The simple schematic of the LDMOS in the study and its HCD test illustration. (b) The degradation of $I_D - V_G$ curves in measurement phases (indicated by (m)) after consecutive stress phases (indicated by (s)). (c) The degradation spectrum is obtained from the data in (b). Three important $V_{G(m)}$ points: P (peak), V (valley), L (linear) are labeled.

After obtaining a series of $I_D - V_{G(m)}$ curves at successive intervals during stress, the full degradation $\Delta I_D - V_{G(m)}$ spectrum is calculated and plotted as a function of stress time $t$, see Fig. 3.1(c). Here, the degradation percentage is calculated at each $V_{G(m)}$ point:

$$\Delta I_D\left(V_{G(m)}, t\right) \equiv \frac{I_D\left(V_{G(m)}, t=0\right) - I_D\left(V_{G(m)}, t>0\right)}{I_D\left(V_{G(m)}, t=0\right)}. \tag{3.1}$$

In other words, each degraded I-V curve ($t > 0$) is turned into the degradation ratio (in %) by point-by-point subtractions from their primitive current levels ($t = 0$). These characteristics

behave like a degradation spectrum over $V_{G(m)}$ from the subthreshold region ($V_{G(m)} < 1$ V) to linear region ($V_{G(m)} > 1$ V). Interestingly, it shows a double-peak behavior, corresponding to the subthreshold and linear regions, respectively. The three critical $V_{G(m)}$ points (P, V, L in Fig. 3.1(c)) will serve as important points to solve the three key quantities $\Delta\mu_{ch}$, $\Delta\mu_{dr}$, and $\Delta V_{th}^{ch}$ (as discussed in the compact model in Fig. 2.4) analytically in Section 3.2.

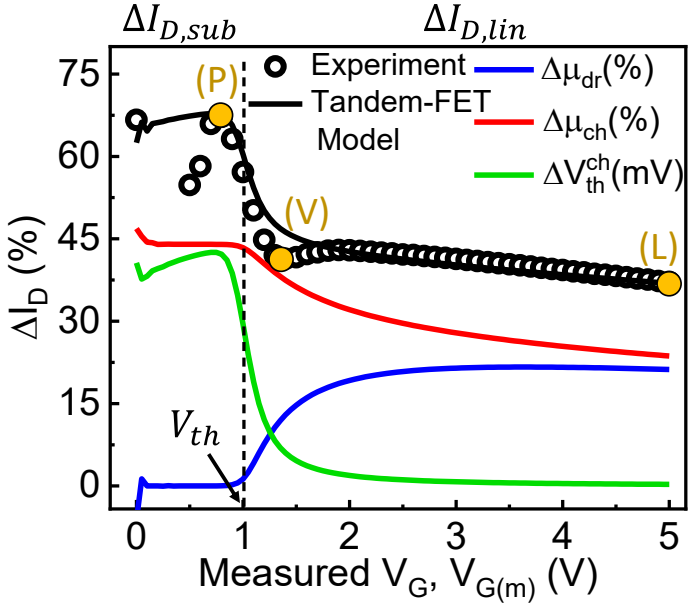



**Figure 3.2.** An example of an I-V degradation spectrum (black circle, under a specific stress condition and after a particular stress time) can be fitted through the tandem-FET model (solid black line). After fitting, the individual impact of the three degradation components on the overall spectrum can be decomposed.

Fig. 3.2 shows how a typical measured I-V degradation data (black circle) can be fitted by adjusting $\Delta\mu_{ch}$, $\Delta V_{th}^{ch}$, and $\Delta\mu_{dr}$ in the compact model (solid black line). Once calibrated, one can depict the individual contribution to $\Delta I_D$ by setting the other two parameters to zero. For example, by setting $\Delta V_{th}^{ch}$ and $\Delta\mu_{dr}$ to zero, the pure $\Delta I_D$ from $\Delta\mu_{ch}$ along with the measured $V_G$ (solid red line) can be plotted. Similar curves can be obtained for the other two components. Interestingly, it shows that a positive shift of $\Delta V_{th}^{ch}$ (in mV) only causes $\Delta I_D$ in the subthreshold region (solid green line). This decomposition explains the reasons for the double peaks. The first peak in the subthreshold region ($V_{G(m)} < V_{th}$) is

due to the exponential dependence on $V_{th}$, which drops dramatically (solid green line) and is taken over by the mobility degradations after $V_{G(m)} > V_{th}$, hence the second peak appears with a valley in the middle. Furthermore, the traditional HCD metric, $\Delta I_{D,lin}$, adds up their impacts (with weighting factors) of mobility degradation in both regions. Furthermore, the subthreshold region ($\Delta I_{D,sub}$) reveals critical information about channel degradation (which is a combination of $\Delta\mu_{ch}$ and $\Delta V_{th}^{ch}$). The decreasing trend of $\Delta I_D$ along measured $V_G$ arises from the feature of $\Delta\mu_{ch}$ (red line in Fig. 3.2). In essence, the tandem-FET model can be used to fit the degraded I-V characteristics to extract the corresponding $\Delta\mu_{ch}(\%)$, $\Delta\mu_{dr}(\%)$, and $\Delta V_{th}^{ch}(\mathrm{V})$ at any stress time $t$. The investigation of the subthreshold region allows us to deconvolve the three components (namely $\Delta\mu_{ch}$, $\Delta V_{th}^{ch}$, and $\Delta\mu_{dr}$).

The benefits of matching the degradation spectrum instead of the original I-V curves are a) the device-to-device pre-stress I-V variation is not a concern because one obtains $\Delta\mu(\%)$ directly from $\Delta I_D(\%)$; b) It provides the holistic view from off- to on-state in the linear scale (semi-log scale for sub- or near-subthreshold matchings is no longer required).

### 3.2 Three-Point Analytical Model

The need to adapt the full degradation spectrum at each measurement period is time-consuming, and the fitting of the tandem-FET model by HSPICE simulation requires expertise in compact modeling. Furthermore, the BSIM6 compact model itself is complicated, and its use obscures the essential physics of the degradation process. Therefore, based on the insights of the BSIM6 model, we will now derive a three-point analytical model to overcome these shortcomings. $\Delta I_D(\%)$ at three critical $V_{G(m)}$ points ($\Delta I_D^{(P)}(t)$, $\Delta I_D^{(V)}(t)$, and $\Delta I_D^{(L)}(t)$ in Fig. 3.1(c) or Fig. 3.2) allow us to determine the three key quantities $\Delta\mu_{ch}$, $\Delta\mu_{dr}$, and $\Delta V_{th}^{ch}$ (as discussed in the compact model in the previous chapter) by solving three analytical equations (to be derived below) corresponding to the P, V, L points. Although *any* three points may be used, the judicious choice of the points simplifies the extraction of the parameters. Specifically, we chose these three points so that three different regimes for an $I_D - V_G$ curve are considered: sub-threshold, near-threshold, and above-threshold.

Assuming linear on-state (measured $V_{G(m)} \gg V_{th}^{ch}$, small $V_D$), the analytical model for the tandem-FET can be derived by interpreting the drift region as a resistor $R_{dr}$. In the linear region, the drain current with the drift resistance $R_{dr}$ is given by:

$$I_D = \frac{\beta_{ch}\left(V_G - V_{th}^{ch}\right)V_D}{1+\beta_{ch}\left(V_G - V_{th}^{ch}\right)R_{dr}} = \frac{I_D^*}{1+K_0}. \tag{3.2}$$

Here, $\beta_{ch} = \mu_{ch}C_{ox}W/L_{ch}$ and $\mu_{ch}$,$W$, $L_{ch}$ are respectively the mobility, width, and length of the channel. $C_{ox}$ is the oxide capacitance. Since the drift region is another MOSFET, the drift resistance is given by $R_{dr} = 1/\left(\beta_{dr}(V_G - V_{th}^{dr})\right)$. By definition, $I_D^* \equiv \beta_{ch}(V_G - V_{th}^{ch})V_D$ and $K_0 \equiv \frac{\beta_{ch}(V_G - V_{th}^{ch})}{\beta_{dr}(V_G - V_{th}^{dr})}$. Both terms change after degradations ($K_0'$ is defined as degraded $K_0$). We can introduce four degradation parameters: $M_{ch}$, $M_{dr}$, $\Delta V_{th}^{ch}$, $\Delta V_{th}^{dr}$ to include the mobility degradation multiplier ($M_{(ch,dr)} = \mu_{(ch,dr)}^{deg}/\mu_{(ch,dr)}^{0} < 1$) and threshold voltage shift ($\Delta V_{th}^{(ch,dr)}$ in mV) after degradation. Therefore, the general form of the degraded $I_D$ can be written as:

$$I_D^{deg} = \frac{M_{ch}\beta_{ch}\left(V_G - V_{th}^{ch} - \Delta \mathrm{V}_{th}^{ch}\right)}{1+\frac{M_{ch}\beta_{ch}\left(V_G - V_{th}^{ch} - \Delta \mathrm{V}_{th}^{ch}\right)}{M_{dr}\beta_{dr}\left(V_G - V_{th}^{dr} - \Delta V_{th}^{dr}\right)}} = \frac{M_{ch}\beta_{ch}\left(V_G - V_{th}^{ch} - \Delta \mathrm{V}_{th}^{ch}\right)}{1+K_0'}. \tag{3.3}$$

Eq. (3.3) can be further simplified for linear (L) and valley (V) points individually. First, let us start with **linear point (L)** (on-state). Here, $V_G - V_{th}^{(ch,dr)} \gg \Delta V_{th}^{(ch,dr)}$, so that all $\Delta V_{th}^{(ch,dr)}$ terms in Eq. (3.3) are negligible, indicating that *degradation depends primarily on the mobility degradation of the two regions* ($M_{ch}$ and $M_{dr}$), but not on $\Delta V_{th}^{(ch,dr)}$, as verified in Fig. 3.2. With Eqs. (3.2) and (3.3):

$$\Delta I_D^{(L)}\,(\%) \equiv \frac{I_D - I_D^{deg}}{I_D} = \frac{M_{dr}\left(1-M_{ch}\right) + K_0 M_{ch}\left(1-M_{dr}\right)}{M_{dr} + K_0 M_{ch}}. \tag{3.4}$$

It is worth mentioning that $K_0$ is an essential parameter for device customization because $K_0 \propto \beta_{ch}/\beta_{dr} \propto L_{dr}/L_{ch}$. For a device with a longer drift region than this specific LDMOS, $K_0$ will be larger, and $\Delta\mu_{dr}$ will become more pronounced in $\Delta I_D$ compared to $\Delta\mu_{ch}$.

The second point to be considered is the **valley point (V)**, as shown in Fig. 3.2, which occurs slightly (0.1 V is used here) above $V_{th}$. Since $V_G - V_{th}^{ch} = V_D = 0.1, I_D^*$ needs to be corrected with a factor of 2 since the second term $(V_D^2/2)$ cannot be neglected,

$$\beta_{ch}\left[\left(V_G - V_{th}^{ch}\right)V_D - V_D^2/2\right] = \frac{\beta_{ch}}{2}\left(V_G - V_{th}^{ch}\right)V_D. \tag{3.5}$$

The parameter $K_0'$ defined in Eq. (3.3) now becomes:

$$K_0' = \frac{M_{ch}\beta_{ch}/2}{M_{dr}\beta_{dr}}\frac{(0.1 - \Delta V_{th}^{ch})}{(1.1 - \Delta V_{th}^{dr})} \approx \frac{M_{ch}}{M_{dr}}\frac{\beta_{ch}}{\beta_{dr}}\frac{(0.1 - \Delta V_{th}^{ch})}{2.2}. \tag{3.6}$$

Revised Eq. (3.3) gives $I_D^{deg} = \frac{M_{ch}I_D^*/2}{1+K_0'}$. Near $V_{th}$, $K_0 \ll 1$ and hence $I_D \approx I_D^*/2$. $\Delta I_D^{(V)}(\%)$ can therefore be written as:

$$\Delta I_D^{(V)}(\%) \equiv \frac{I_D - I_D^{deg}}{I_D} = 1 - \frac{M_{ch}}{1 + K_0'}. \tag{3.7}$$

We may further simplify it because $K_0'$ is less than 0.1. By applying $(1 + K_0')^{-1} \approx 1 - K_0'$, we can write:

$$\Delta I_D^{(V)}(\%) \approx 1 - M_{ch}(1 - K_0') = (1 - M_{ch}) + \frac{M_{ch}^2}{M_{dr}}\frac{\beta_{ch}}{\beta_{dr}}\frac{(0.1 - \Delta V_{th}^{ch})}{2.2} \approx 1 - M_{ch}. \tag{3.8}$$

One can either choose to adopt Eq. (3.7) as an exact form or use Eq. (3.8) for a quick estimate.

Finally, let us consider the **peak point (P)** in the subthreshold region. At this point, the subthreshold current $I_{D,sub} = I_S exp(\frac{q(V_G - V_{th})}{mkT})$, where $I_S(\propto \mu)$ is a constant at fixed $V_D$, $kT/q$ is the thermal voltage at ambient temperature, and m is the body coefficient. The degradation of the channel mobility degrades $I_S$ while $\Delta V_{th}$ degrades $I_{D,sub}$ exponentially. Therefore,

$$\Delta I_D^{(P)}(\%) \equiv \frac{I_D - I_D^{deg}}{I_D} = 1 - M_{ch} exp\left(\frac{-\Delta V_{th}^{ch}}{mkT/q}\right). \tag{3.9}$$

For the case $\frac{\Delta V_{th}^{ch}}{mkT/q} \ll 1$, Eq. (3.9) can be further simplified with Taylor's expansion of the exponential term ($e^{-x} \approx 1 - x$),

$$\Delta I_D^{(P)}(\%) \approx (1 - M_{ch}) + M_{ch}\frac{\Delta V_{th}^{ch}}{mkT/q}. \tag{3.10}$$

Since $mkT/q \sim 52$ mV at room temperature, Eq. (3.10) works well for relatively small $\Delta V_{th}^{ch}$. As predicted in Fig. 3.2, both the channel mobility and threshold voltage degradation could contribute to $\Delta I_{D,sub}$. Given these three unique points (i.e., P, V, L), Eqs. (3.4), (3.7), (3.8), (3.9), (3.10) allow us to directly and intuitively calculate the three unknowns, $\Delta\mu_{ch}$, $\Delta\mu_{dr}$, $\Delta V_{th}^{ch}$.

### 3.3 Comparison Between Compact Model and Analytical Model

Fig. 3.3 shows some examples of the I-V spectroscopy fitting from the compact model. It shows that the tandem-FET compact model can reasonably match the experimental I-V spectroscopy from off-state ($V_{G(m)} < 1$ V) to on-state (high $V_{G(m)} > 1$ V). Each line (certain stress time) determines a set of parameters ($\Delta\mu_{ch}$, $\Delta\mu_{dr}$, $\Delta V_{th}^{ch}$). Fig. 3.4(a) shows that this Peak-Valley-Linear (PVL) algorithm (symbols) reproduces $\Delta\mu_{ch,dr}$ obtained by fitting the full degradation spectrum with the BSIM6-based tandem-FET compact model (lines). It is noteworthy that when $\Delta\mu < 1$ %, the compact model cannot be fitted precisely due to the weak/noisy $\Delta I_D$ peak. In this regime, the analytical forms, Eqs. (3.4)-(3.10), offer a more accurate and much faster calculation of mobility degradation. For higher degradation ($\Delta\mu < 1\%$), the three-point analytical technique and tandem-FET compact model give comparable results, as expected. Note that, the linear relationship in a log-log plot implies that $\Delta\mu_{ch,dr}$ follows a power-law degradation.

Fig. 3.4(b) shows $\Delta I_D^{(P)}(\%)$ vs. $\Delta V_{th}^{ch}$ (mV) from experiments, where its linear behavior is suggested by Eq. (3.10). It deviates from the linear curve at higher $\Delta V_{th}^{ch}$ as expected (works well when $\Delta V_{th}^{ch} < 15$ mV). The smaller slope of $V_{G(s)}/V_{D(s)} = 4$ V/ 8 V case is due to the higher calculated $\Delta\mu_{ch}(\%)$ (smaller $M_{ch}$). In both cases, channel degradation is minor, $M_{ch} \approx 1$, so that the offset term in Eq. (3.10), $1 - M_{ch} \approx 0$. Here, the coefficient, $m \approx 2$, justifies the derivations.

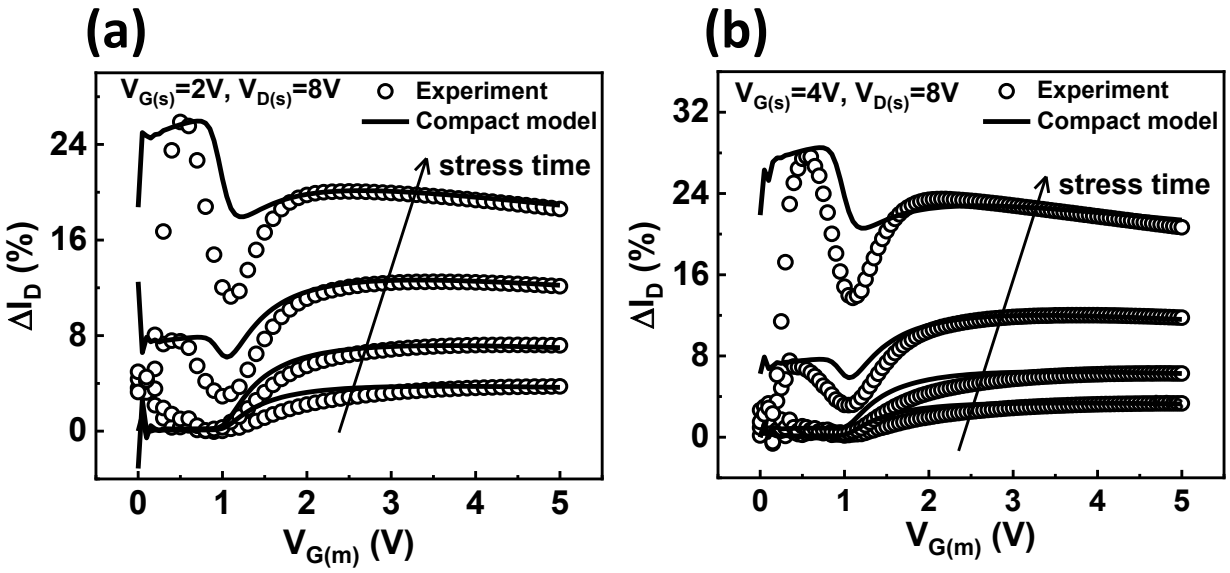



**Figure 3.3.** The examples of I-V spectroscopy matching with the proposed tandem-FET compact model by parameterizing $\Delta\mu_{ch}$, $\Delta\mu_{dr}$ and $\Delta V_{th}^{ch}$ with stress conditions $V_{G(s)}/V_{D(s)}$ = (a) 2 V/8 V; (b) 4 V/8 V, as examples.

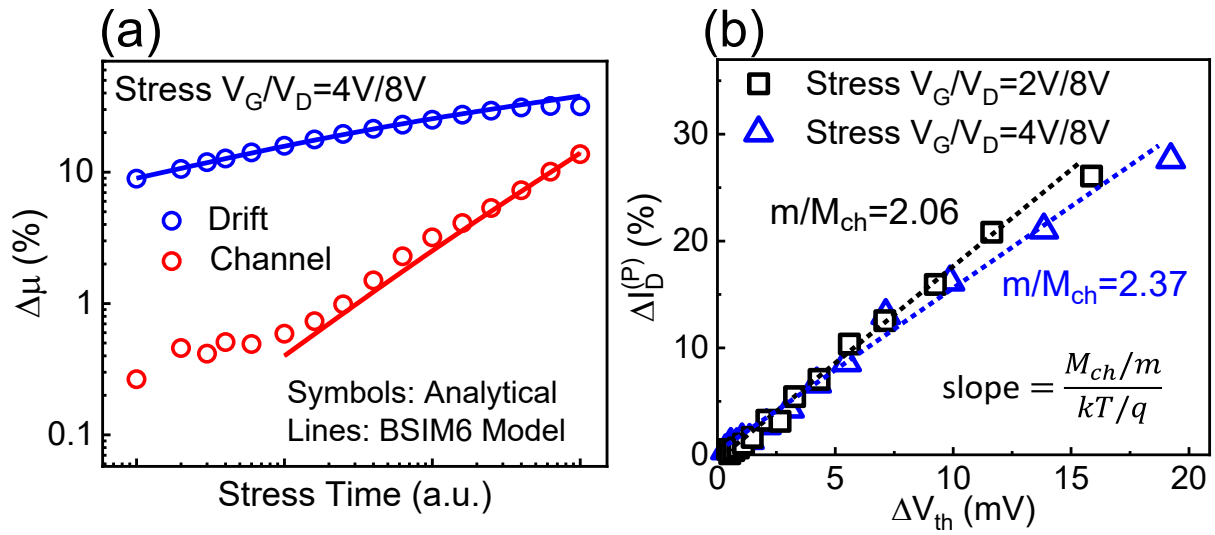



**Figure 3.4.** (a) The comparison of $\Delta\mu(t)$ results between the analytical model (symbols) and compact model (lines). The stress condition is $V_G/V_D$ = 4 V/ 8 V, as an example. (b) Verification of the relation of $\Delta I_D^{(P)}$ and channel $\Delta V_{th}$ from Eq. (3.10).

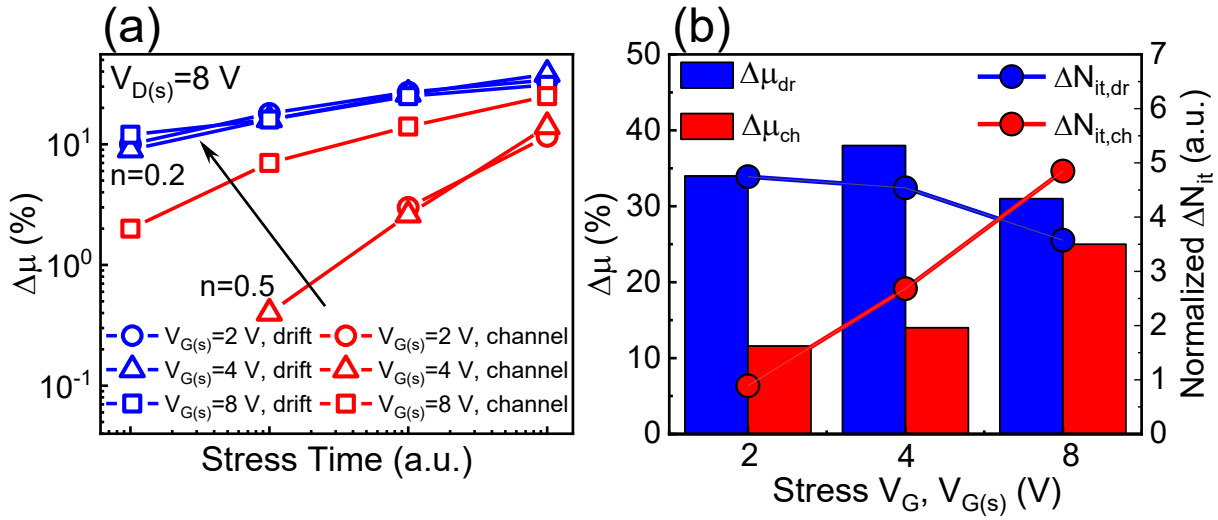



**Figure 3.5.** (a) The extracted channel and drift $\Delta\mu(t)$ at various stress conditions. (b) The comparison of extracted $\Delta\mu$ to $\Delta N_{it}$ by the charge pumping technique [60] at the final stress time.

### 3.4 HCD in Channel and Drift Regions

Finally, the time kinetics of deconvoluted $\Delta\mu_{ch}$ and $\Delta\mu_{dr}$ under different stress conditions are compared. Fig. 3.5(a) shows an increasing $\Delta\mu_{ch}$ and decreasing time exponent (0.5 to 0.2), whereas $\Delta\mu_{dr}$ does not vary for different stress $V_{G(s)}$, with a smaller time exponent around 0.1. Similar results have been reported in other papers [22], [61]. Fig. 3.5(b) replots the data in Fig. 3.5(a) to compare the degradations at the final stress time. The results agree well with the generation of interface traps ($\Delta N_{it}$) extracted through CP-related technique [60]. LDMOS transistors for different applications can have distinct structures, geometries, doping levels. For example, an LDMOS with field oxide, depending on the stress condition, may have three hotspots, and only two of them contribute to overall $\Delta I_D$ [62]. Therefore, although the concept of 'three-point I-V spectroscopy' was demonstrated on one specific structure in this paper as a prototype, it holds for LDMOS transistors with different drift lengths and doping configurations. The general principle proposed (i.e., representing a transistor into a set of sub-transistors, determining the critical points on the $I_D - V_G$ curve that localizes the degradation associated with individual sub-transistors, and extracting the

degradation parameters related to the critical points) can be a versatile approach for the degradation characterization of other configurations of the LDMOS transistor as well. Although in most of the LDMOS devices, the features of the I-V spectroscopy (first peak in subthreshold, then a valley near the threshold, and a peak again after the threshold) are similar, this model should also be applicable in devices where the peak and the valley may not be easily distinguishable. In those cases, any point in the subthreshold region can be chosen as (P), and any point close to the threshold can be chosen as (V) to perform the analysis. However, the closer the V-point to the device $V_{th}$, the more accurate the analytical model can be, as discussed in Appendix A.3.

### 3.5 Conclusions

In conclusion, using an N-channel LDMOS as an example, the 'three-point I-V spectroscopy technique' is proposed as a powerful HCD characterization approach. It unveils the degradation components without conducting detailed and time-consuming characterization of multiple degraded spots using the charge pumping technique. The physics underneath its double-peak feature is fully explored through the proposed tandem-FET model. Those deconvoluted degradation parameters ($\Delta\mu_{ch}$, $\Delta\mu_{dr}$, $\Delta V_{th}^{ch}$) can be obtained either by fitting the BSIM6-based compact model or solving the derived three-point analytical model (results are comparable). The general principle of using a physics-based compact model to derive a device-specific characterization protocol should generalize to other power transistors as well. Given any LDMOS with two degradation spots, the proposed technique can be used.

# 4. SUPER SINGLE PULSE CHARGE PUMPING ($S^2PCP$)

## 4.1 Introduction

Among other factors, the performance and the reliability of a traditional MOSFET are defined by the density of broken bonds at the interface between the channel and the gate dielectric, i.e., $N_{it}$. There are many techniques to measure $N_{it}$, such as high/low frequency [63], DCIV [64], AC conductance [65], deep–level transient spectroscopy (DLTS) [41], Terman method [66], etc. One of the most widely used techniques is the charge pumping (CP) method, which was originally developed by Burgler and Jespers in 1969 [42] and then later put on a firm theoretical foundation by Groeseneken *et al.* in 1984 [43]. The original CP technique was subsequently generalized to include spatially-resolved CP based on local $V_{fb}(x)$ and $V_{th}(x)$ [67] and multi-frequency charge pumping (MFCP) to probe the bulk traps within high-$\kappa$ gate dielectric stack [68]. Even today, CP and its variants remain versatile techniques for characterizing $N_{it}$ in four-terminal bulk MOSFET. With independently accessible contacts, a periodic gate pulse fills the interface traps by electrons from the source-drain contacts and then empties the trapped charges by electron-hole recombination through the substrate contact. Averaged over millions of cycles, the corresponding DC charge pumping current ($I_{CP}$) provides a direct measure of $N_{it}$. The classical CP technique is widely used to track the time evolution of interface traps of bulk MOSFETs due to various degradation mechanisms [69], that is, $N_{it}\,(t) \propto I_{CP}(t)$.

Unfortunately, classical CP cannot be used for many technologically important three-terminal (3T) logic and power transistors such as SOI-FinFETs, back-gated thin-film FET, HEMTs, etc. Without body contact, $I_{CP}$ cannot be measured. The SPCP technique addresses this challenge by measuring the incoming and outgoing transient fluxes from the same terminal. A single square pulse with a high temporal resolution is applied to the gate and the source-drain transient current ($I_{SD}$) is measured [70]–[72]. Once the capture and emission fluxes are separated, $N_{it}$ is then calculated by subtracting the charge accumulated during ramp-up and ramp-down phases of the gate pulse. In this way, $N_{it}$ of the 3T devices can be calculated by SPCP technique [73]–[75]. While SPCP determines spatially averaged $N_{it}$, it is difficult to profile the defects along the interface. This is particularly important for

lightly-doped drain (LDD) or LDMOS devices where understanding the spatial distribution plays an important role in lifetime predictions and failure analyses. The generalization is particularly difficult when the body contact is present but shorted to the source because of the complex partitioning of the capture and emission fluxes among the contact [60]. The goal of this chapter[1] is to develop a new SPCP technique that offers the intuitive generalization of the SPCP technique. It will be utilized to measure the generated HCD-induced $N_{it}$ in LDMOS transistors. Understanding the basic mechanisms behind CP and SPCP techniques is very essential for our proposed Super SPCP ($S^2$PCP) method.

### 4.1.1 Charge Pumping (CP) Technique

Usually, to conduct CP measurements, the source and drain terminals are shorted, and they are slightly reverse biased to the substrate to improve the accuracy by reducing the geometric component [43]. Taking an N-channel MOSFET as an example, the gate bias pulse is designed to drive the channel surface from accumulation (full of holes) to inversion (full of electrons) periodically. The experimental setup is illustrated in Fig. 4.1(a), where the DC charge pumping current ($I_{CP}$) can be measured at the substrate terminal due to the recombination of the electrons and holes. Fig. 4.1(b) describes the mechanisms in more detail. As $V_G$ is ramped up from accumulation, the holes are forced to be detrapped from the interface traps. However, due to the high frequency of the pulse, the holes cannot be completely detrapped from the trap, especially for those near the midgap (far away from the conduction band and valence band, more time is required). Those residual holes will be recombined by the incoming electrons, giving rise to $I_{CP,SD}$ (measurable from source and drain). On the other hand, as $V_G$ ramps down, the incoming hole recombines the residue electrons instead, again producing $I_{CP,SUB}$ (measurable from the substrate). Ideally, the two $I_{CP}$ should be identical, and substrate current is classical and more common. Multiple papers of source/drain $I_{CP}$ can also be found [77], [78]. $I_{CP}$ can be formulated as [43],

$$I_{CP} = f\ A_G\ q^2\ \bar{D_{it}}\ \Delta\psi_s, \tag{4.1}$$

[1]↑The content of this chapter is partially taken from our publications [60], [76]

where $f$ is the frequency of the pulse, $A_G$ is the gate area, $\bar{D_{it}}$ is the average surface state density per energy, and $\Delta\psi_s$ is the energy range within the bandgap.

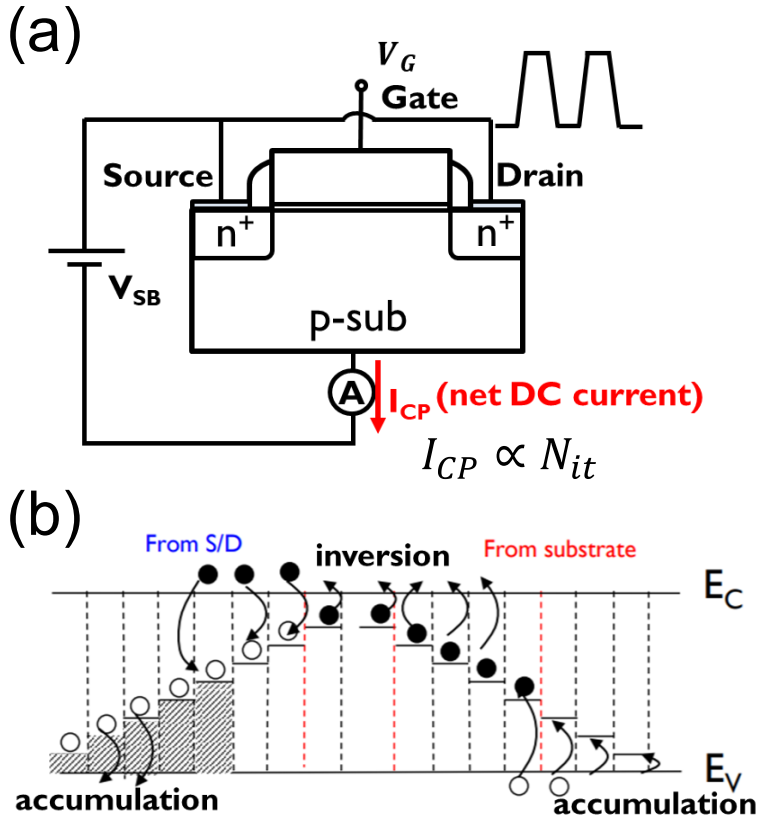



**Figure 4.1.** (a) The experimental setup of the charge pumping (CP) method for a MOSFET. (b) The schematic illustrates the movements of electron and hole carriers during the pulse from accumulation to inversion. The picture is taken from Ref. [17].

### 4.1.2 Single Pulse Charge Pumping (SPCP) Technique

As shown in Fig. 4.2, similar to CP, single pulse charge pumping (SPCP) utilizes the mechanism of injecting the carriers and emptying them from the interface defects. The main differences are 1) a single pulse is applied instead of a periodic pulse; 2) Transient current (displacement current), $I_{SD}$, is measured through the shorted source/drain contact. Starting from the accumulation region ($V_G = V_L$), as $V_G$ is ramped up, electrons flow from the

source/drain will recombine with the residual holes in interface defects, causing a 'recombination peak' on top of the displacement component. As $V_G$ is ramped down, on the other hand, only the displacement component presents, usually with a tail due to the slower detrapping process. The subtraction of the two components provides the total charge proportional to $N_{it}$. The formulation of SPCP can be expressed as [73]–[75],

$$N_{it} = \left( \int I_{SD,\uparrow}(t)dt - \int I_{SD,\downarrow}(t)dt \right) / qLW, \tag{4.2}$$

where the $I_{SD,\uparrow}$ and $I_{SD,\downarrow}$ are the transient current during the ramp-up and -down phase. The limit of integration is the rising/falling edges. $q$ is the elementary charge, $L$ and $W$ are the length and width of the region activated by the pulse.

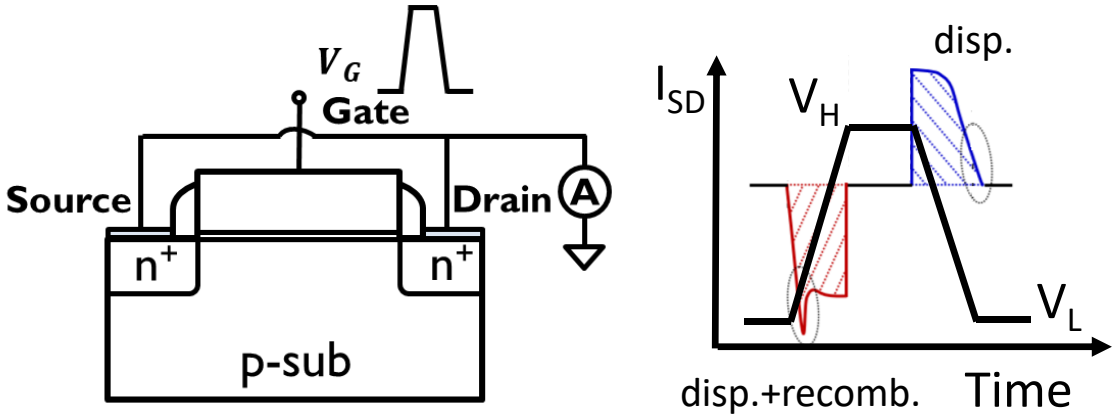



**Figure 4.2.** The experimental setup of the SPCP and the common response in source/drain transient current ($I_{SD}$). The recombination peak and detrapping tail are highlighted by the dashed circles. $V_L$ and $V_H$ are the low and high levels of the pulse.

Compared to CP, SPCP allows a faster surface defect characterization, which addresses the issue of relaxation after stress such as negative-bias temperature instability (NBTI). However, since the magnitude of the transient current can be expressed as

$$I_{disp} = C_G \frac{dV}{dt}, \tag{4.3}$$

a primary constraint of the SPCP technique is that it requires a larger gate capacitance or higher pulse ramp rate to obtain a clean result ($I_{disp} \gg 1$ nA). This constraint persists in the proposed new charge pumping technique, which will be discussed in the next section.

## 4.2 Super Single Pulse Charge Pumping (S²PCP) Development

### 4.2.1 Limitations of CP/SPCP

Fig. 4.3(a) shows a source-body-tied (SBT) LDMOS, identical to the one shown in the previous chapters. The device is selected as an illustrative example of an important class of devices that requires a generalization of the conventional CP/SPCP technique. In this

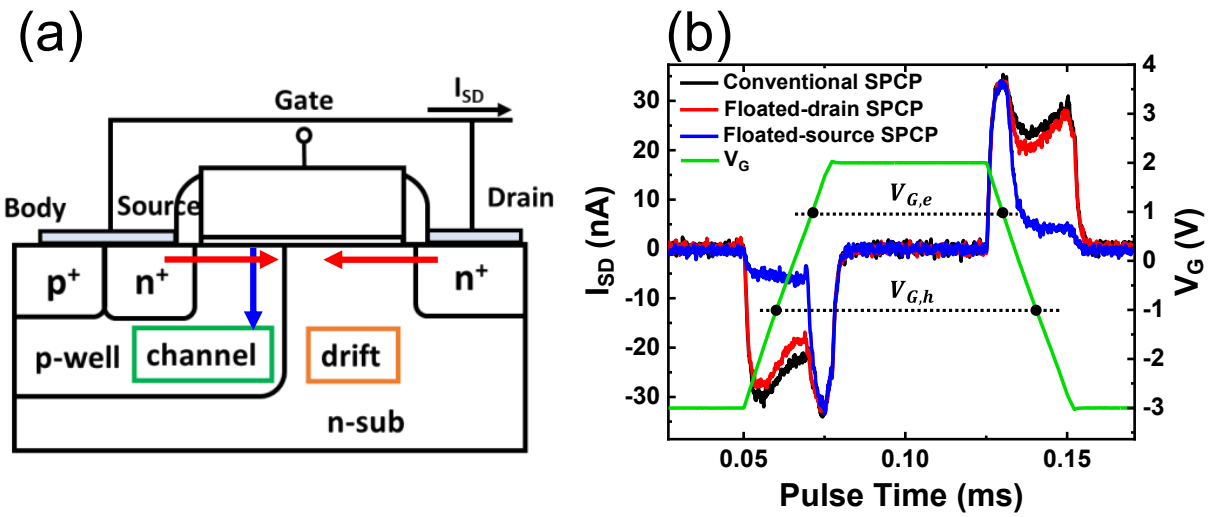



**Figure 4.3.** Challenge in applying CP/SPCP technique: (a) A 3T device with a source-body-tied (SBT) structure. The body hole current ($I_B$, blue) mixes with source-drain electron current ($I_{SD}$, red). (b) The comparison among different SPCP measurement setups. $V_{G,e}$ and $V_{G,h}$ are the level corresponds to $10^{14}$ cm$^{-3}$ of electron and hole concentration for the channel region.

SBT scheme, the body hole current $I_B$ (blue arrow) mixes with source/drain electron current (red arrow) as the measured $I_{SD}$, which complicates the analysis. Moreover, the localized $N_{it}$ extraction in the channel and the drift region are of great interest so that CP/SPCP techniques cannot be used to profile the defects. Fig. 4.3(b) shows the experimental result of SPCP on the SBT LDMOS. The "anomalous" double-peaked feature observed in the SPCP experiment (black) cannot be understood based on the classical theory of CP/SPCP and yet this feature contains the seed of the S$^2$PCP measurement. The mechanisms behind this can be explored by floating either the source or the drain terminal. Interestingly, the onset of the peak corresponds to a higher $V_G$ (= 1 V, noted as $V_{G,e}$) always presents for either drain- or source-floated SPCP. This should be attributed to channel inversion, supported by the tandem-FET model in the last chapter. Before the onset of the channel inversion, floating the source or the drain terminal can help isolate the channel (red) and drift (blue) current. This can be confirmed because their sum is close to the classical SPCP (black). The insights from Fig. 4.3 pave the way to design the super SPCP. The mixture of the electron and hole current will be addressed in the following section.

### 4.2.2 Pulse Design of S$^2$PCP

To design the pulse, the two levels ($V_{G,e}$ and $V_{G,h}$ to reach the electron/hole concentration of $10^{14}$ cm$^{-3}$) along the current path from source to drain is required. Due to the complexity of the doping profile, the TCAD model can assist in estimating the carrier concentration at a certain $V_G$ bias. Apart from the LDMOS structure discussed in Fig. 4.3(a), the LDMOS with field oxide is also of interest. As shown in Fig. 4.4, $V_{G,e}$ and $V_{G,h}$ for the two types of LDMOS are obtained. Here, LOCal Oxidation of Silicon (LOCOS) is used as field oxide in one of the devices under study. The dashed line is drawn along the surface of both types of LDMOS. It is worth noting that due to the thick field oxide, it usually requires more negative $V_G$ to generate sufficient holes at the interface. Moreover, it can be classified into three regions: channel region (P-well), accumulation region (N-well, outside the LOCOS region), LOCOS region (N-well, under thicker oxide). It is commonly observed that under HCD, the damage usually occurs at the edge of the LOCOS [61], [79]. Therefore, we will

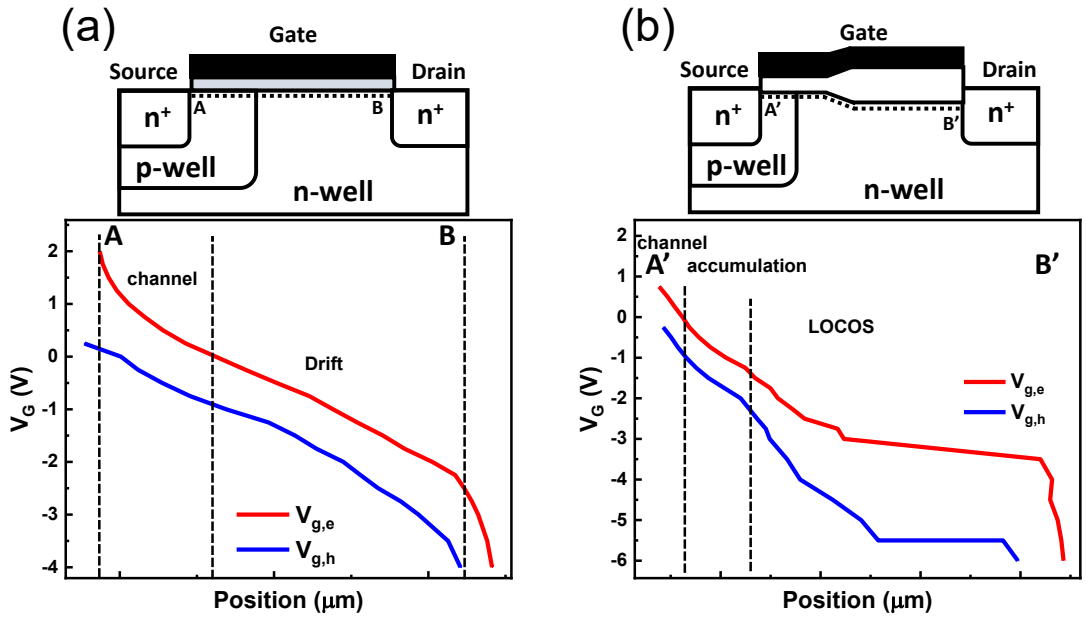



**Figure 4.4.** Two types of LDMOS under study: (a) low-voltage application (b) higher-voltage application with a thick field oxide (LOCOS). The two important levels ($V_{G,e}$ and $V_{G,h}$) along the current path (dashed line) are obtained by the TCAD model.

design the gate pulse to probe $N_{it}$ at the two edges and the bottom of the LOCOS. In the following sections, we define the LOCOS edge near to the source as edge 1, and the one near to drain as edge 2.

Fig. 4.5 illustrates the concept of the proposed S$^2$PCP. To separate the electron and hole components, the 'double-step pulse' is implemented when probing the channel region (Fig. 4.5(a)). The plateau introduced in the midgap allows the decoupling of the hole (blue) and electron current (red), which is an essential step so that Eq. (4.2) is still valid. On the other hand, to probe the drift region (either with or without LOCOS), the source terminal needs to be floated, and the pulse design is similar to the classical SPCP because there is no hole component to be isolated. Therefore, it is operated like the single-terminal SPCP, as shown in Fig. 4.5(b). We also hold $V_G$ at $V_L$ for 1 second because of the relatively slow thermal generation rate for holes [80], [81]. The pulse generation code is provided in Appendix B.

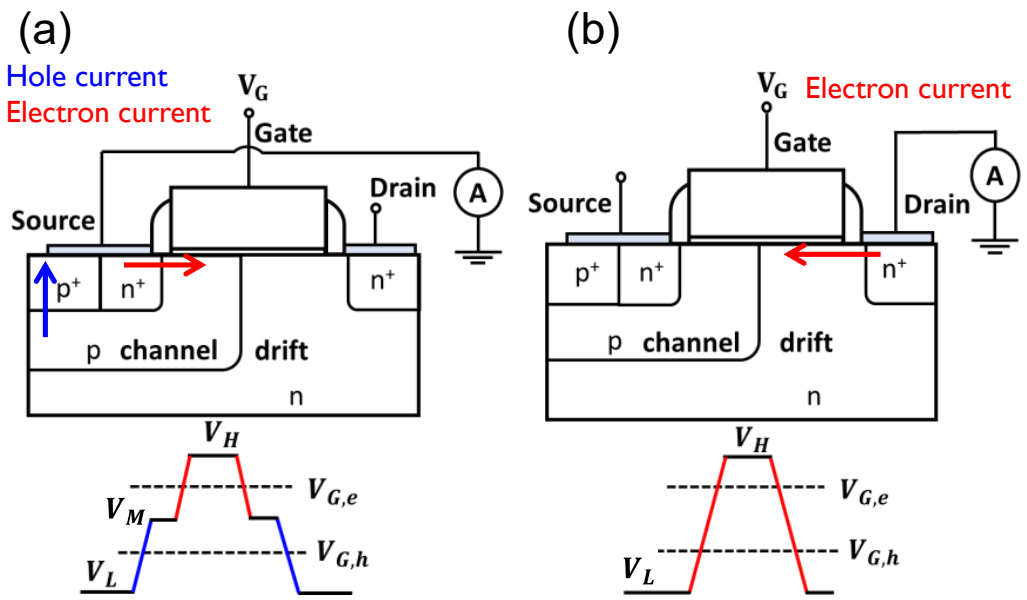



**Figure 4.5.** Simple description of the measurement setup and pulse design of (a) floated drain S$^2$PCP to probe the channel $N_{it}$ and (b) floated source S$^2$PCP to probe the drift $N_{it}$. $V_L$, $V_M$, and $V_H$ are the low-, mid- and high-level of the pulse.

## 4.3 Experimental Validations of S$^2$PCP Technique

Keysight B1500A Semiconductor Device Analyzer with waveform generator/fast measurement units (WGFMUs) are used for pulse generations and high-speed current/voltage measurements. Either the source or drain contact is floated and the current ($I_{S/D}$) is measured by an ammeter. The square pulse (with $t_{rise} = t_{fall} = 20\,\mu$A, from $V_L$ to $V_H$) is applied to the gate contact to drive the transistor between accumulation and inversion. The pulse ramp rate and the gate geometries determine the transient current level by Eq. (4.3), and $I_{S/D}$ needs to be well above the measurement limit ($\sim$1 nA) to ensure reliable measurements. The rise and fall time of the gate pulse ($t_{rise}$ and $t_{fall}$) determine the time window available for capture and emission of trapped charges [43]. In this section, we will validate the S$^2$PCP technique with various effective widths and ramp rates to understand the limitation and the optimized parameters.

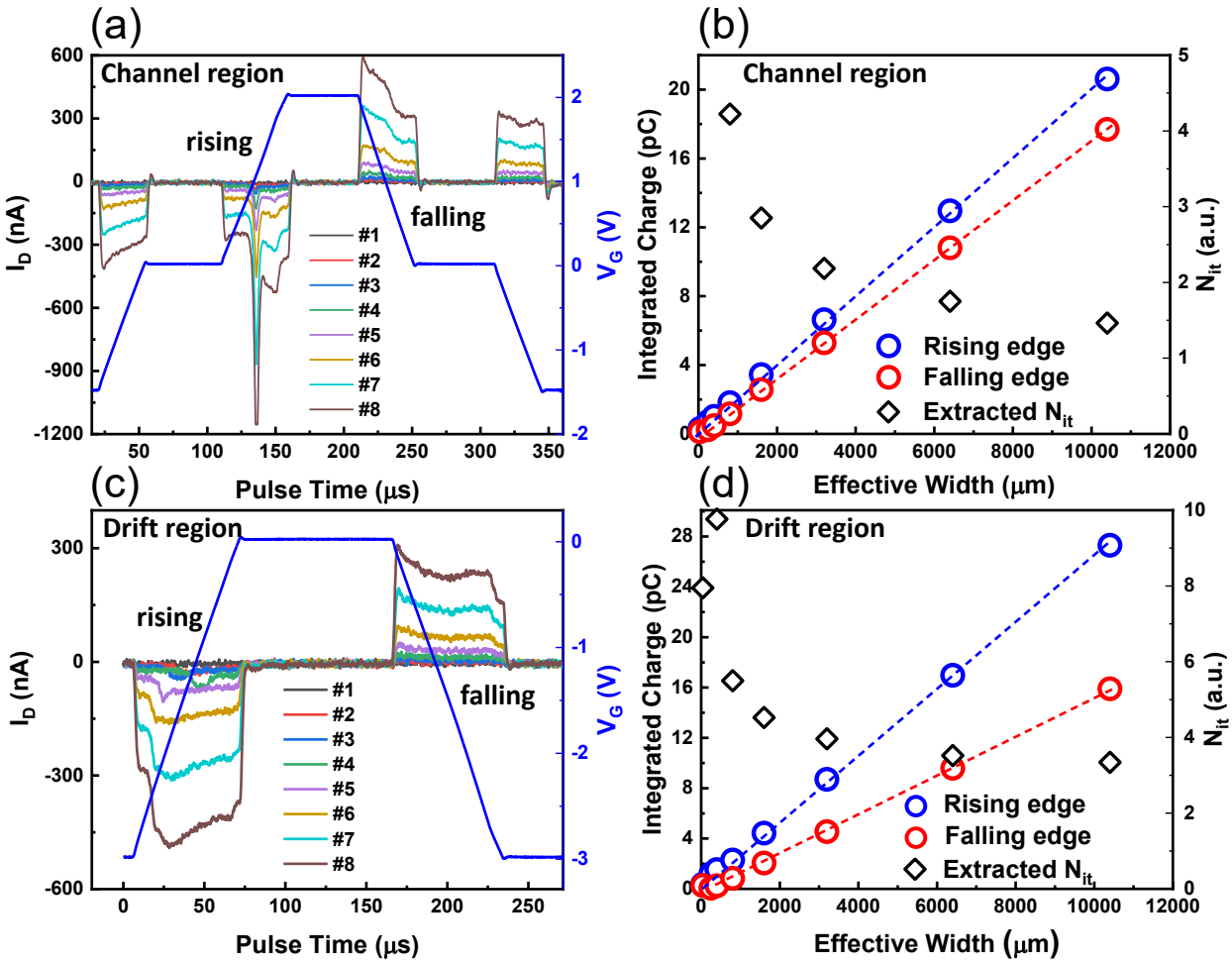



**Figure 4.6.** The proposed S$^2$PCP Technique technique to probe LDMOS with various device widths (#1-#8). The transient current, integrated charge, and $N_{it}$ are plotted for (a)(b) channel region and (c)(d) drift region.

We examine the proposed S$^2$PCP on the non-LOCOS LDMOS with the same geometries but with various effective widths, ranges from 41.5 μm to 10400 μm, which are labeled as #1 to #8. Figs. 4.6(a) and 4.6(b) are the data from floated drain S$^2$PCP, targeting at channel region. Figs. 4.6(c) and 4.6(d) are the data from floated source S$^2$PCP, targeting the drift region. The integrated charge at both rising and falling edges increases linearly with the effective width. The obtained interface trap density ($N_{it}$) from devices with distinct widths varies. There are two reasons: 1) the device-to-device variation. 2) Inaccuracy for narrower devices owing to the weaker displacement current and hence the contamination due to the noises. As suggested by the results, a wider device is preferred for $N_{it}$. For both regions

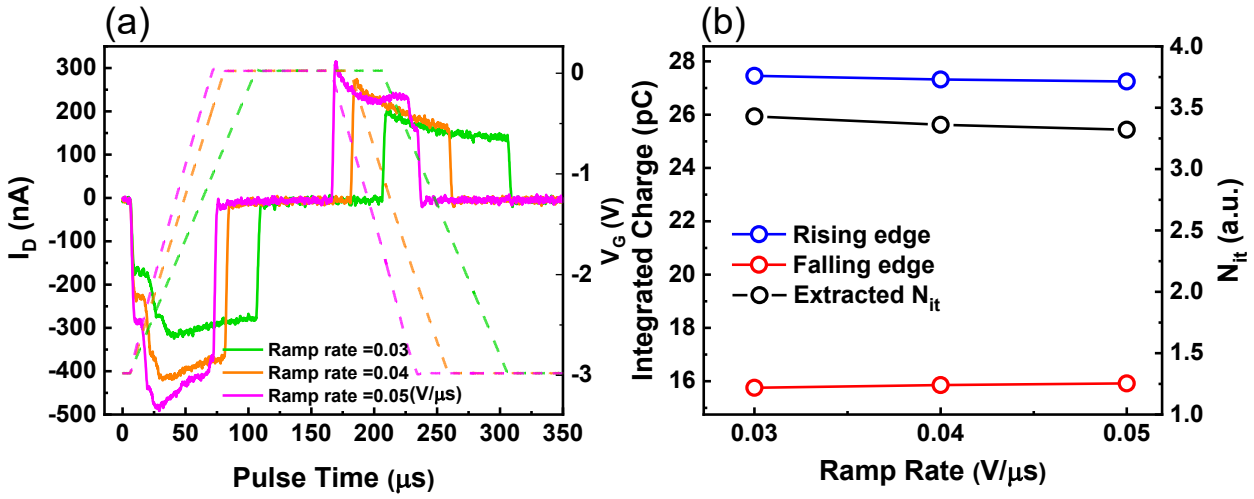



**Figure 4.7.** The pulse rise/fall time adjustment during the S$^2$PCP measurements. Three ramp rates are chosen: 0.03, 0.04, 0.05 V/μs. (a) The measured transient current. (b) The integrated total charge and $N_{it}$.

in this specific device, the device width should be larger than 1000 μm to ensure a reliable extraction (for the oxide capacitance of $\sim$ 1.8 fF/μm$^2$ and ramp rate of 0.04 V/μs).

To examine the frequency dependence, three different pulse rise/fall times are tested here. It is observed that the shorter the rise/fall time (higher the ramp rate), the higher the transient current levels. However, the integrated charge does not change dramatically, as shown in Fig. 4.7. Therefore, there might not be a strong limitation of the rise/fall time. On the other hand, if the device is quite small in the gate area, one might choose the higher ramp rate to acquire more stable and reliable current data. Another way to eliminate the noise is to have a series of pulses and take an average. Fig. 4.8 shows a sequence of 10 pulses on a small device with an effective area of $\sim$20 μm$^2$. Although there is $\sim$5% cycle-by-cycle variation, an increase of integrated charge increases after certain hot carrier stress can still be observed and calculated. Up to now, the tunable parameters in S$^2$PCP have been discussed. In the next section, we will start to conduct S$^2$PCP after each hot carrier stress period to extract the damage status. The goal is to obtain the regional $\Delta N_{it}$ as a function of stress time.

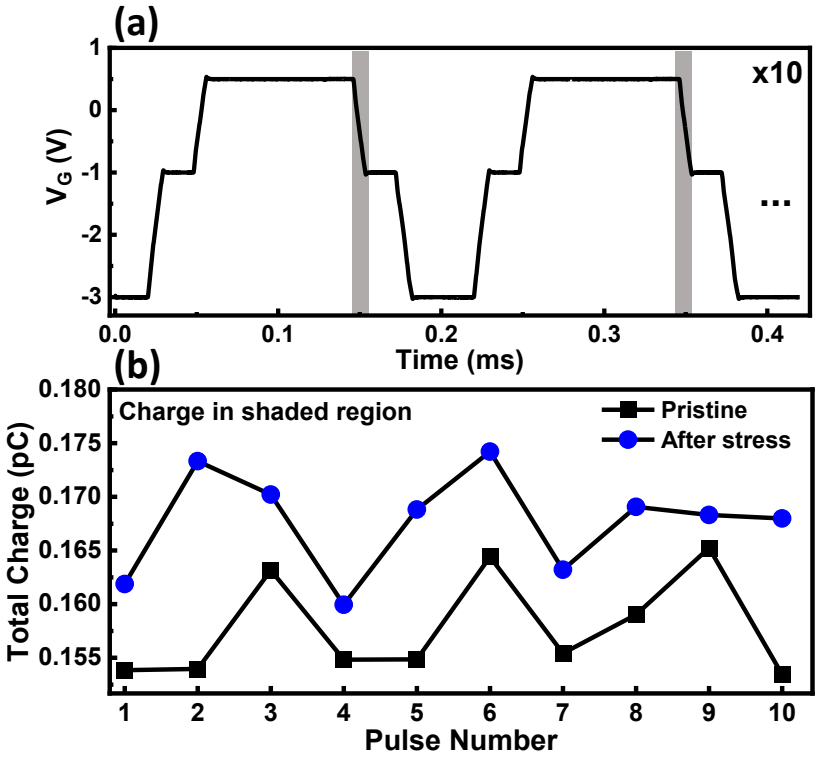



**Figure 4.8.** (a) A series of 10 repetitive pulses are applied. (b) The comparison of the integrated charge during the ramp (grey regions in (a)) in each cycle.

## 4.4 S²PCP-HCD Test on LDMOS Transistors

In this section, two types of LDMOS transistors (as illustrated in Fig. 4.4) are stressed under hot carrier stress and constantly interrupted in logarithmic time with a complete measurement of S²PCP (floated drain and floated source, with a series of 10 pulses for each case) given the negligible recovery of HCD.

### 4.4.1 Non-LOCOS LDMOS Transistors

An example of S²PCP measurement under hot carrier stress is plotted in Fig. 4.9. In both regions, the integrating charge at the rising edge increases while the falling edge remains nearly unchanged, referring to $\Delta N_{it}$ with stress time. The extracted channel and drift $\Delta N_{it}$ are shown in Fig. 4.10. It reveals that the drift region is still the main degradation spot

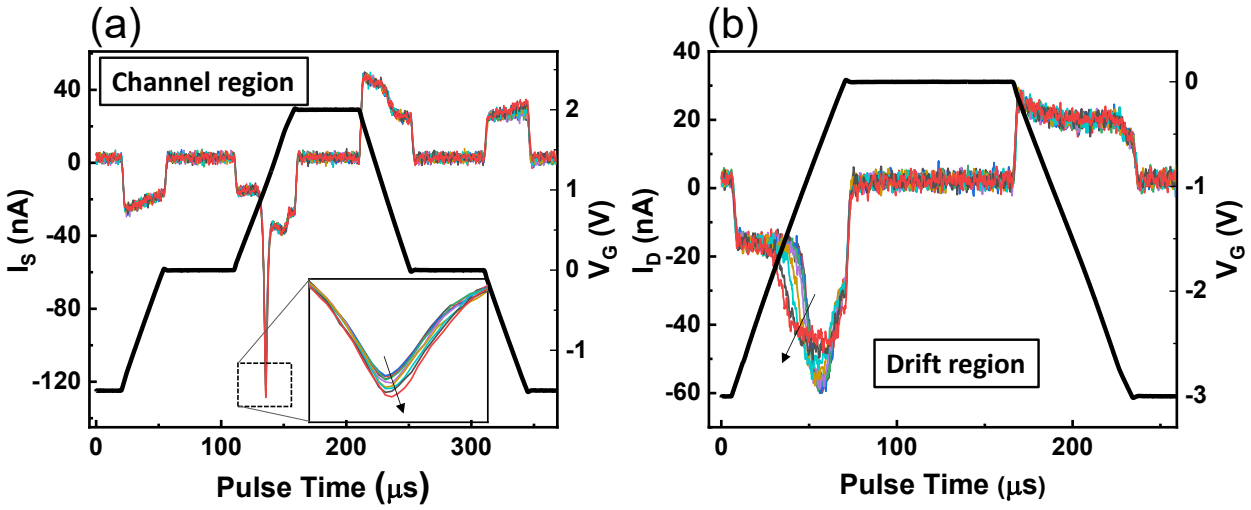



**Figure 4.9.** The evolution of S$^2$PCP current under hot carrier stress of $V_G$ =1.7 V, $V_D$ =7 V in (a) channel region with inset focuses at the peak, and (b) drift region. The arrow indicates the direction it changes over stress time.

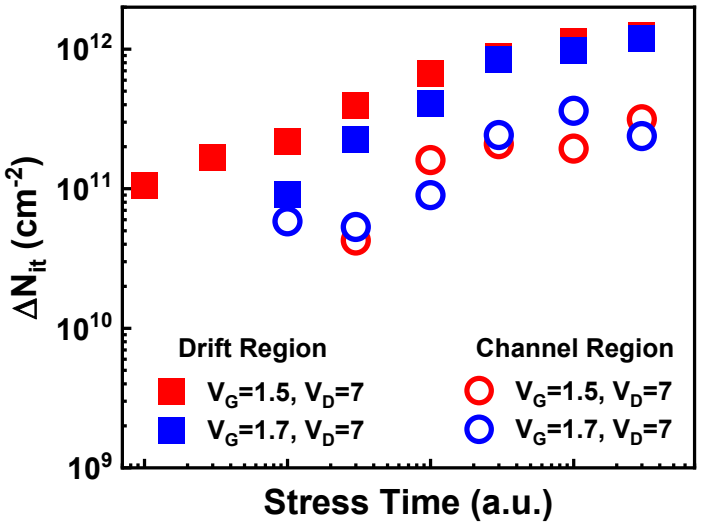



**Figure 4.10.** $N_{it}$ generation as a function of stress time. The drift region degrades much more than the channel region. The stress conditions are $V_G$ =1.5/1.7 V, $V_D$ =7 V.

under the stress conditions of $V_G$ = 1.5, 1.7 V, and $V_D$ = 7 V. The overall trend follows a power law, with the time exponent ranging from 0.3 to 0.5.

To validate the measured $\Delta N_{it}$, we compare it in two ways. Firstly, the channel $\Delta N_{it}$ is linearly proportional to the device $\Delta V_{th}$ because $\Delta V_{th} \sim qN_{it}/C_{ox}$, as shown in Fig. 4.11(a). Secondly, the mobility degradation is more severe at higher $\Delta N_{it}$, described by [82], [83],

$$\mu_{deg} = \frac{\mu_0}{1 + \alpha N_{it}}, \tag{4.4}$$

where $\mu_{deg}$ is the degraded mobility, $\mu_0$ is the prestress mobility, $\alpha$ is a coefficient in the order of $10^{-12}$. Therefore, after some approximations, the mobility degradation percentage is proportional to $\Delta N_{it}$, $\Delta\mu/\mu_0 \sim \alpha\Delta N_{it}$. In other words, the proposed technique 'I-V spectroscopy' (in Chapter 3) can be utilized here to verify the results. Both plots show a linear correlation reasonably well, justifies the extracted $\Delta N_{it}$ in both regions. It is interesting to note that the channel and drift region share the similar $\alpha = 1.23 \times 10^{-13}$.

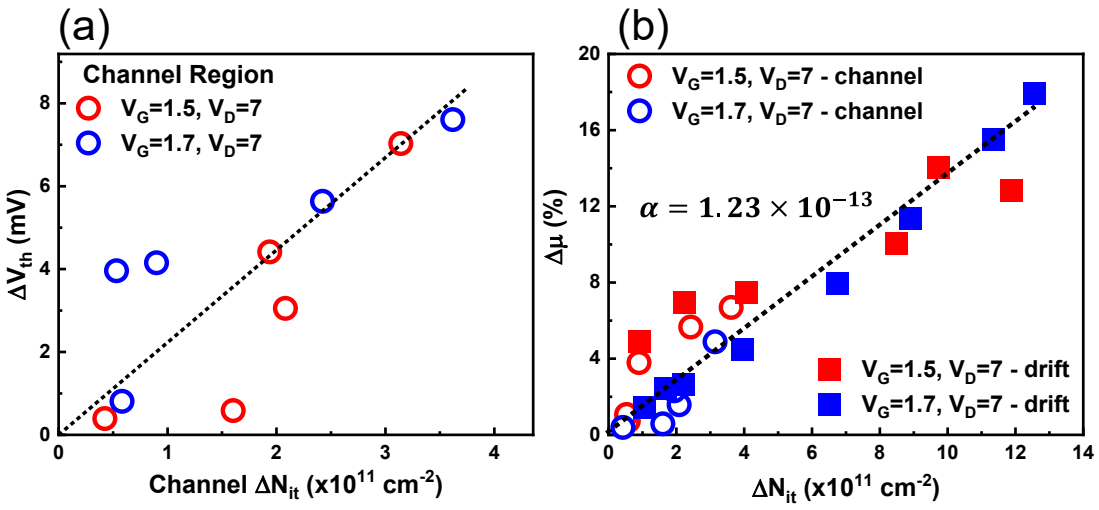



**Figure 4.11.** (a) Extracted channel $\Delta N_{it}$ vs. $\Delta V_{th}$. (b) $\Delta\mu$ obtained from I-V spectroscopy vs. $\Delta N_{it}$. Both the channel and drift regions demonstrate the same $\alpha = 1.23 \times 10^{-13}$.

### 4.4.2 LOCOS-Based LDMOS Transistors

Similarly, the pulse can be customized to detect the specific position in an LDMOS with LOCOS. 5 different regions are of interest: channel region, accumulation region, LOCOS edge 1, LOCOS bottom, LOCOS edge 2, as illustrated in Fig. 4.12(a). The evolution of the $S^2$PCP transient current (under the stress condition of $V_G$ =1.5 V, $V_D$=20 V, as an example) is plotted in Fig. 4.12. Generally, all regions, except accumulation, show increasing $N_{it}$ as the stress time evolves. This decreasing $N_{it}$ in the accumulation region may be caused by the hole trapping. The calculated $\Delta N_{it}$ vs. stress time for all regions are plotted in Fig. 4.13. By comparing $\Delta I_{D,lin}$ with several regional $\Delta N_{it}$ in the log-log plot, it can be observed that the LOCOS edge 1 (closer to the source-side) is the dominant component that contributes to the overall $\Delta I_{D,lin}$, which is also supported by references [62]. Many papers [61], [84], [85] also suggest that the impact ionization happens at the edges of the field oxide (LOCOS or STI) owing to the localized field peak at the two edges. This phenomenon can also be observed in Fig. 4.13.

Finally, we can compare the regional $\Delta N_{it}$ at several different stress conditions, as shown in Fig. 4.14. Considering that the main damage is at the two edges, it will be helpful to compare $\Delta N_{it}(t)$ at the two edges for several different stress conditions. The increasing trend of $\Delta N_{it}(t)$ does not vary when increasing the stress conditions. Overall, the Nit is higher when increasing the stress $V_G$. Again, the LOCOS edge 1 has much more impact in causing the device $\Delta I_{D,lin}$.

## 4.5 $S^2$PCP to Detect Oxide Charge Trapping

Except for detecting $\Delta N_{it}$, similar to the traditional charge pumping, it can also be used to detect oxide trapping, $\Delta N_{ot}$. Here, gamma ray radiation (Cobalt-60 as the source) is utilized to create oxide traps. The incident gamma ray creates electron-hole pairs in the oxide. A big portion of the electrons can be quickly swept out through contact due to higher mobility. However, the holes, due to lower mobility, linger in the oxide, and transport to the location near the oxide/semiconductor interface. Part of the holes are trapped near the interface, the others could generate $N_{it}$ when they transport to the interface [86]. Both $\Delta N_{it}$

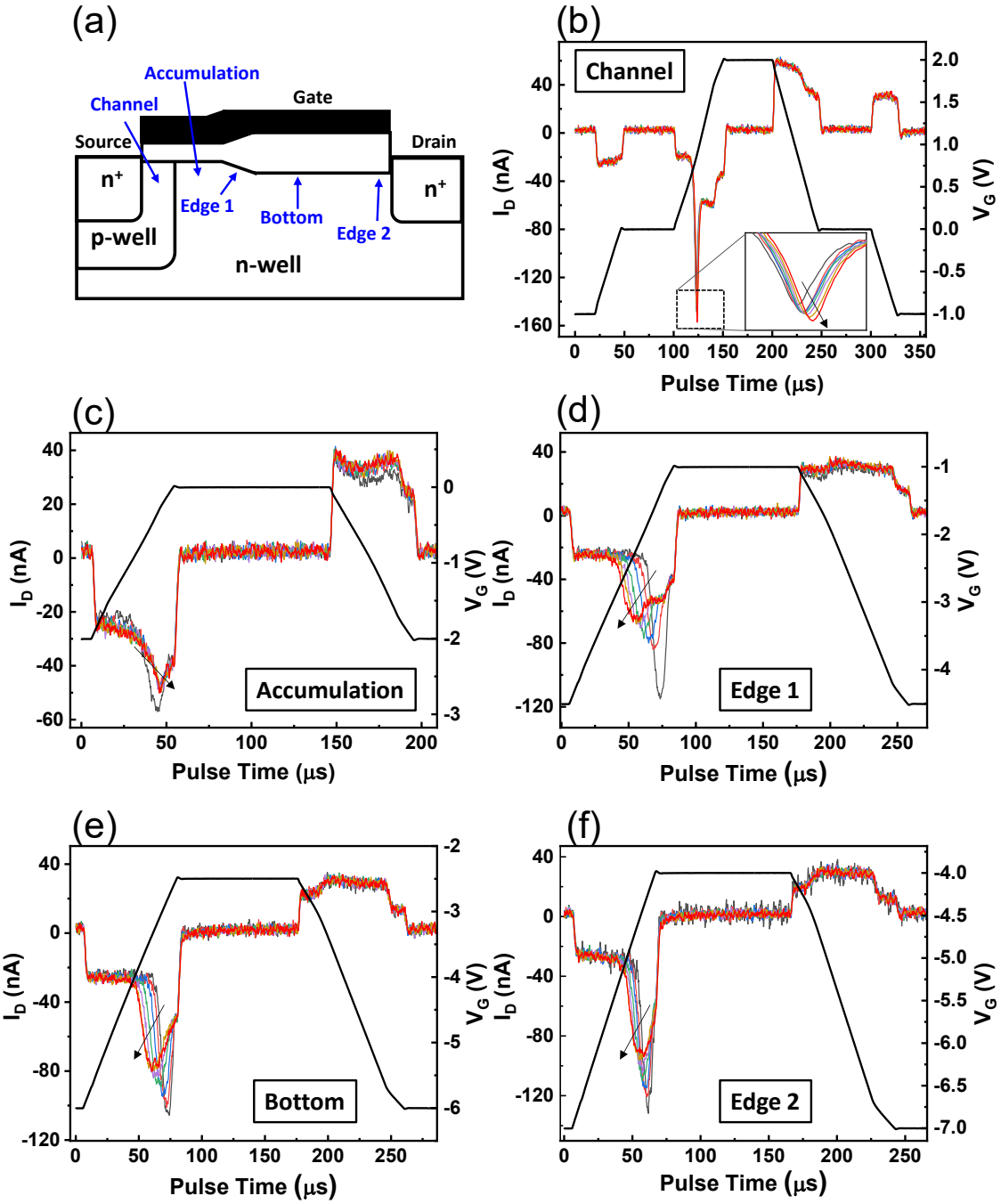



**Figure 4.12.** (a) The schematic of the LDMOS with several regions. The evolution of S$^2$PCP current under hot carrier stress of $V_G$ = 1.5 V, $V_D$ = 20 V in (b) channel region with inset focuses at the peak, (c) accumulation region, (d) LOCOS edge 1, (e) LOCOS bottom (f) LOCOS edge 2. The arrow indicates the direction it changes over stress time.

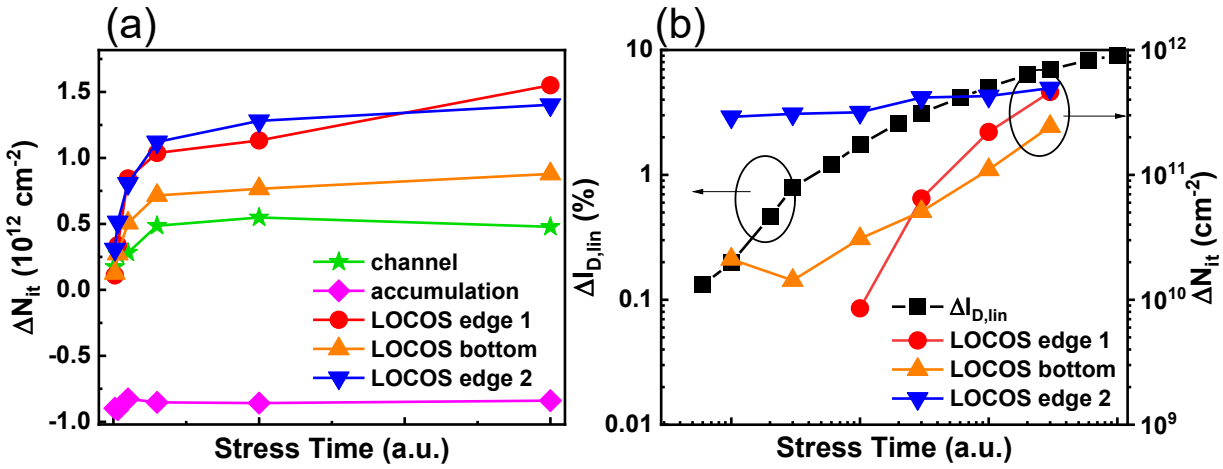



**Figure 4.13.** (a) The calculated $\Delta N_{it}$ vs. stress time, stressed at $V_G = 1.5$ V, $V_D = 20$ V. (b) The comparison between device $\Delta I_{D,lin}$ and several regional $\Delta N_{it}$.

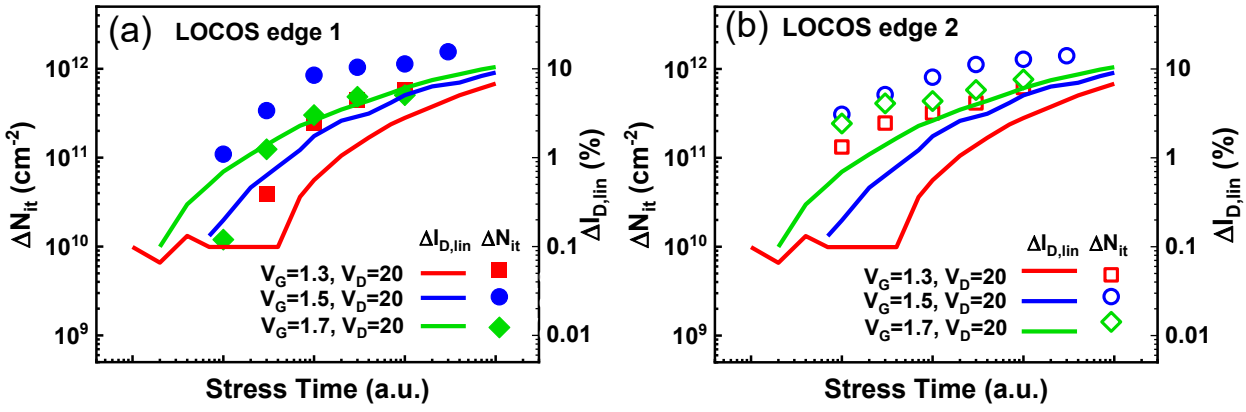



**Figure 4.14.** $\Delta N_{it}(t)$ at three different stress conditions, in comparison to device $\Delta I_{D,lin}$ in (a) edge 1 and (b) edge 2.

and $\Delta N_{ot}$ cause $\Delta V_{th}$ but in an opposite direction. $\Delta N_{ot}$ by hole trapping causes a negative shift of $\Delta V_{th}$ while $\Delta N_{it}$ (acceptor-like is assumed in general) causes a positive shift of $\Delta V_{th}$.

The non-LOCOS LDMOS devices are placed in the radiation chamber under gamma rays from 1 day to 18 days long for different devices. The total ionizing dose (TID) experiment is carried out with an accumulation of total doses of 0.1, 0.6, 1.2, and 1.8 Mrad (Si) by controlling the radiation time duration under a constant dose rate of 0.1 Mrad (Si)/day. Under radiation, a negative $\Delta V_{th}$ was observed and it increases at higher doses. After exposure to the radiation, I-V characteristics and S$^2$PCP measurements on the channel region are done, as shown in Fig. 4.15. Fig. 4.15(a) shows that the recombination peak shift to lower $V_G$, which is not observed during HCD tests. This confirms that HCD only generate $\Delta N_{it}$ but not $\Delta N_{ot}$, whereas TID generate mainly $\Delta N_{ot}$ (and minor $\Delta N_{it}$) because the integrated charge does not increase significantly after radiation. Fig. 4.15(b) compares $\Delta V_{th}$ extracted from linear $I_D - V_G$ curves and S$^2$PCP. It shows consistent results from the two methods, however, at extremely high dose $>$ 1 Mrad (Si), the two methods deviate more, which might be due to the increased $\Delta N_{it}$ [87], [88], inducing the increased subthreshold slope, or possible damage on other locations.

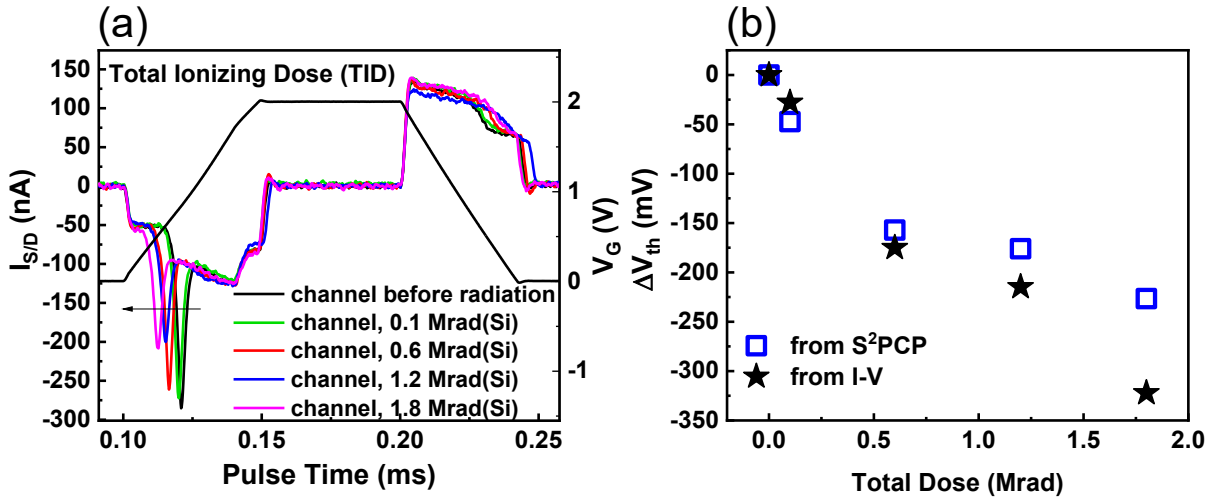



**Figure 4.15.** (a) S$^2$PCP measurements for channel region after different dose of gamma ray. (b) The comparison of $\Delta V_{th}$ measured from the shift of recombination peaks and the ones from linear $I_D - V_G$ curves.

## 4.6 Conclusions

In this chapter, a new type of charge pumping method (Super Single Pulse Charge Pumping, $S^2$PCP) is proposed to address the limitation on SBT and multi-region transistors. SBT configuration, inducing the mixture of electron and hole current, can be solved by introducing the double-step pulse. And the region-specific $\Delta N_{it}$ can be measured by floating either the source or the drain terminal. Since it originates from SPCP, the limitation of the device area persists. Therefore, it should be used when the detected area is sufficiently large ($> 100$ µm$^2$ for the oxide capacitance of $\sim 1.8$ fF/µm$^2$ and ramp rate of 0.04 V/µs). If the device is not in the SBT schematic, the double-step pulse is not required.

For non-LOCOS LDMOS transistors, the results show a good correlation with $\Delta\mu$ extracted from I-V spectroscopy (Chapter 3), cross-validating the two characterization techniques. For LOCOS-based LDMOS transistors, the damage at the LOCOS edge near the source dominates the overall $I_{D,lin}$ degradation. Compared to the non-LOCOS devices, most of the damage occurs in the LOCOS region with less $\Delta V_{th}$. Finally, another useful feature of $S^2$PCP was explored by TID experiments with gamma rays, showing that the oxide charge trapping can also be detected from the lateral shift of the recombination peaks. To sum up, the newly proposed $S^2$PCP technique successfully extends the conventional CP/SPCP techniques into the power transistor field. It is a versatile technique that allows $N_{it}$ extractions in SBT multi-region transistors.

# 5. HCD-INDUCED ANODE HOLE INJECTION

## 5.1 Introduction

Unlike logic transistors, the characterization results show that the TCAD prediction in Fig. 1.4 is indeed correct. Namely, if stressed at high enough $V_G$, the hot carrier damage occurs not only near the drain but also near the source, which gives rise to rapid degradation in $V_{th}$. TCAD simulation can be utilized to investigate this multi-hotspot phenomenon, as shown in Fig. 5.1(a). We found that the gradient quasi-Fermi level at the channel region starts to rise rapidly when $V_G > V_D/k$, where $k$ is a device-specific parameter (= 2 for our devices) to determine the onset of channel degradation [19]. In other words, when stressed at $V_D = 8$ V, the transition point occurs at $V_G = 4$ V. The peak of gradient quasi-Fermi level in the source region indicates the possible damage. The goal of this chapter is to explore the mechanisms causing the channel degradation at high $V_G$ stress from the experimental evidence.

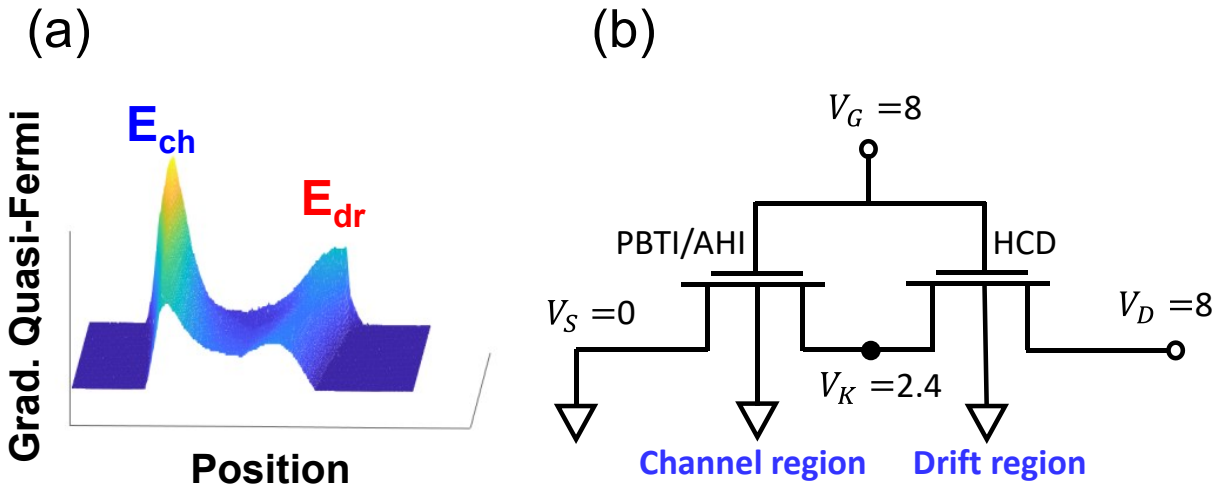



**Figure 5.1.** (a) The corresponding TCAD simulation indicates the possible presence of the two hotspots in terms of the gradient quasi-Fermi level. (b) The tandem-FET model to analyze two regions separately. At $V_G = 8$ V and $V_D = 8$ V, $V_K = 2.4$ V can be obtained from the TCAD simulations.

The previously proposed tandem-FET compact model in Chapter 2 can guide us in understanding this topic. The potential at the metallurgical junction, $V_K$, can be treated as the drain bias for the intrinsic MOSFET. Also, as depicted in Fig. 2.6, $V_K$ changes with different $V_D$ and $V_G$ bias. For an extreme stress condition of $V_G/V_D$ = 8 V/8 V, according to TCAD simulations, $V_K$ = 2.4 V. It means that the voltage drops on the two MOSFETs (channel and drift regions) are 2.4 V and 5.6 V individually, as depicted in Fig. 5.1(b). This seems to indicate that instead of HCD, the channel region is more likely to experience a positive-bias temperature instability (PBTI) or anode hole injection (AHI) [89] because effectively it has $V_G > V_D$. Indeed, these two mechanisms may even be correlated.

To unveil the fundamental mechanisms of channel degradation, many features of channel degradation will be characterized and analyzed in this chapter, including the recovery, temperature-dependence degradation, temperature-dependence gate leakage. All of them indicate a conclusion that the channel degradation is due to anode hole injection (AHI) while the drift degradation is due to classical HCD.

## 5.2 Puzzle: The Root Cause of Channel Degradation

### 5.2.1 Temperature-Dependent HCD

For starters, the HCD at different temperatures are performed and inspected. To compare the channel and drift region, two different stress conditions are compared here: $V_G/V_D$ = 2 V/8 V and 8 V/8 V. Since $V_G/V_D$ = 8 V/8 V induces channel degradation while 2 V/8 V does not, it is expected that the two conditions will demonstrate different properties. In an LDMOS, HCD generally decrease at higher temperatures [22], therefore, one should expect decreasing $\Delta I_{D,lin}$ and $\Delta V_{th}$ at elevated temperatures.

The experimental data are plotted in Fig. 5.2. First, both $\Delta I_{D,lin}$ decrease at higher temperatures as shown in Figs. 5.2(a) and 5.2(b), following the general trend for an LDMOS. Interestingly, $\Delta V_{th}$, from Figs. 5.2(c) and 5.2(d), shows the opposite temperature trend for low and high $V_G$ stress.

To further understand it, the I-V spectroscopy introduced in Chapter 3 is used to decompose the channel and drift degradation components given that $\Delta I_{D,lin}$ is composed of

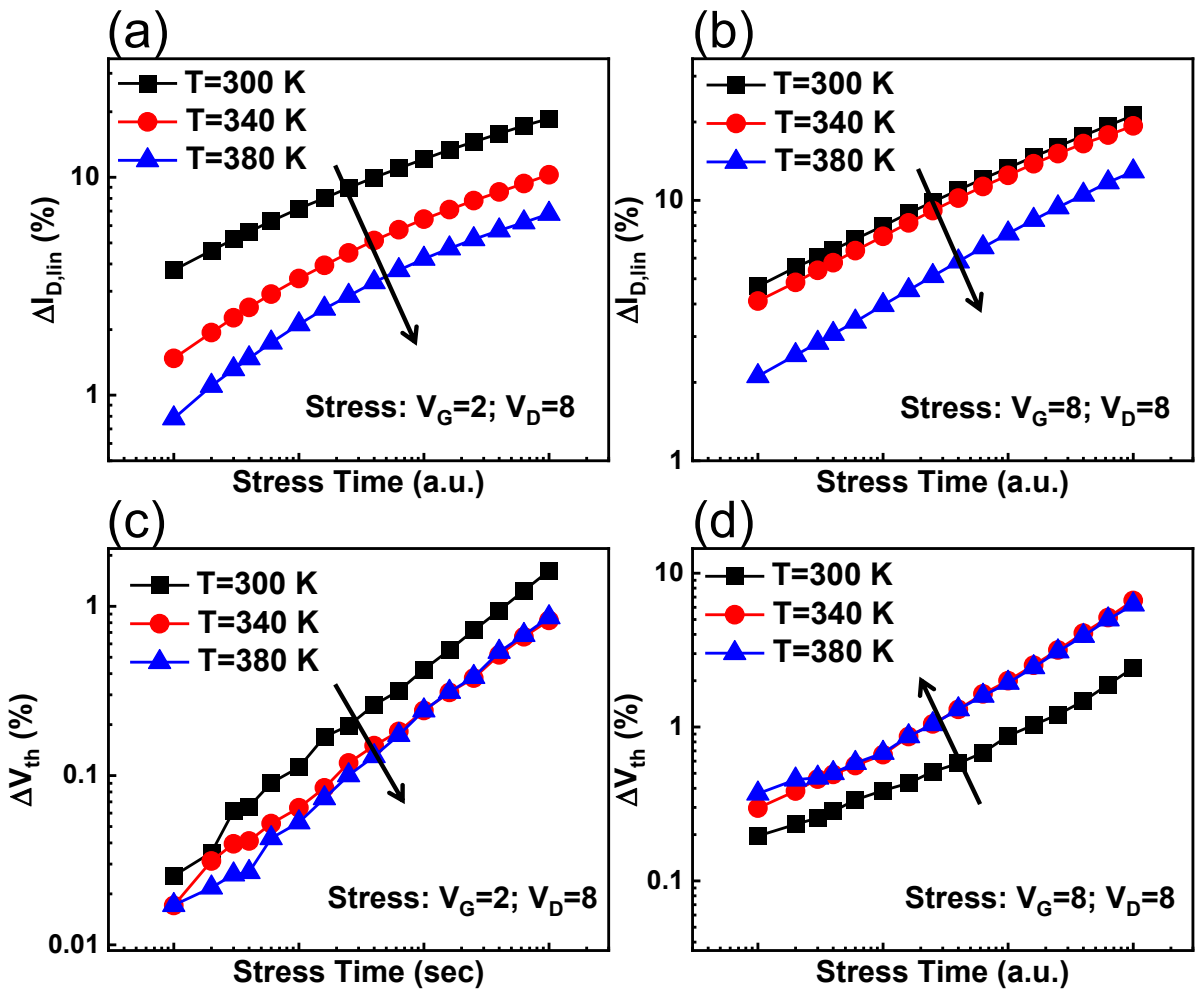



**Figure 5.2.** Temperature-dependence HCD measurements: $\Delta I_{D,lin}$ decreases at higher temperatures for (a) $V_G/V_D$ = 2 V/8 V and (b) $V_G/V_D$ = 8 V/8 V. However, $\Delta V_{th}$ decreases at higher temperatures for (c) $V_G/V_D$ = 2 V/8 V and increases at higher temperatures for (d) $V_G/V_D$ = 8 V/8 V. The arrows indicate the direction with increasing temperature.

$\Delta\mu_{ch}$ and $\Delta\mu_{dr}$. The decomposition results are plotted in Fig. 5.3. Overall, both $\Delta\mu_{ch}$ and $\Delta\mu_{dr}$ decrease with temperature, indicating that $\Delta N_{it}$ is diminished due to carriers with less energy. However, $\Delta V_{th}$ shows a turn-over when stressed at $V_G/V_D$ =4 V/8 V when increasing the temperature, manifesting two competing mechanisms with similar strength.

We speculate the second mechanism is AHI because it generally increases with temperature [90], which is opposite to HCD. Plus, as pointed out by Mahapatra *et al.* [91], AHI is a common stress scenario in creating $N_{it}$. At a high enough temperature (380 K here), HCD

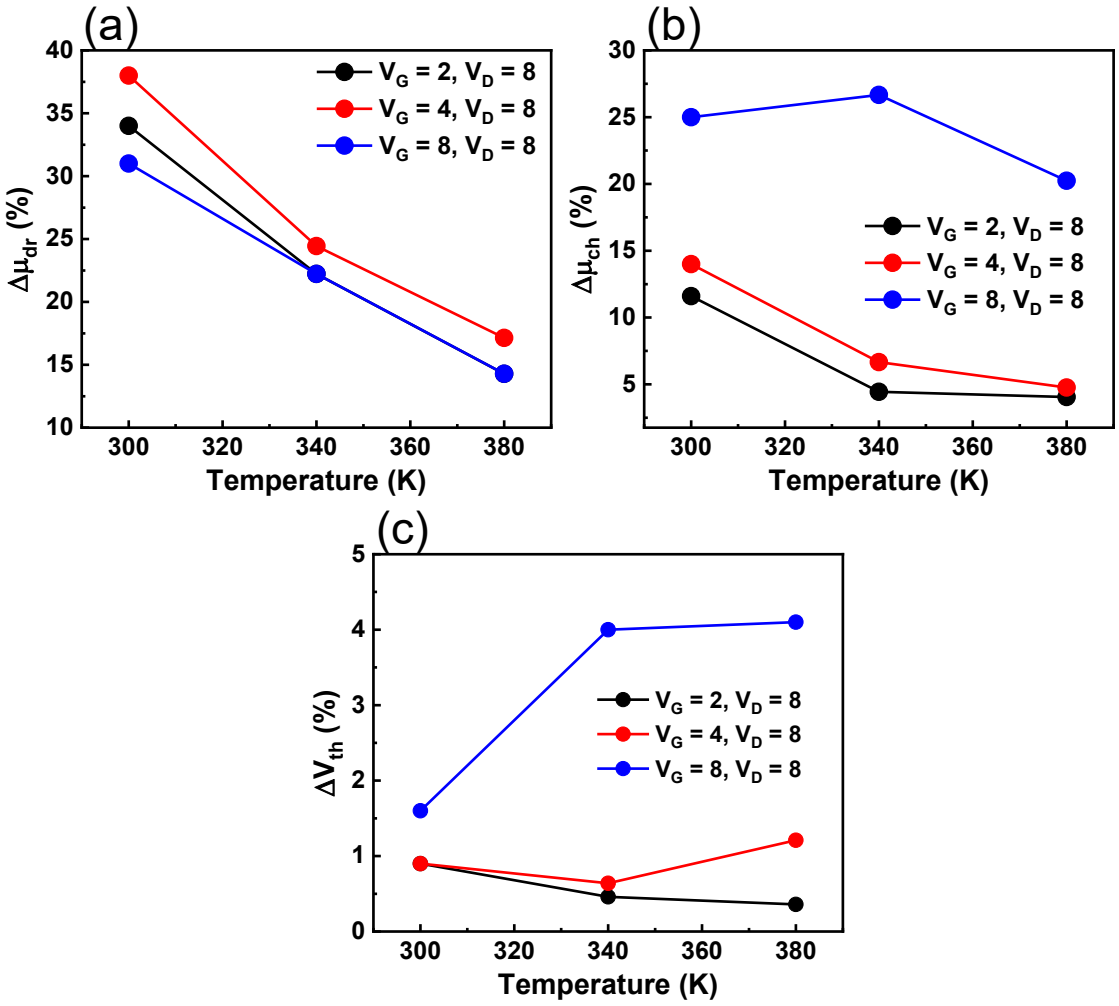



**Figure 5.3.** The decomposition of regional HCD in terms of (a) $\Delta\mu_{dr}$, (b) $\Delta\mu_{ch}$, and (c) $\Delta V_{th}$ at increasing temperature at different stress conditions.

becomes weaker while AHI is intensified, hence it becomes the primary cause of $\Delta V_{th}$. At the stress condition of $V_G/V_D$ =8 V/8 V, AHI-induced oxide defect is dominant in measured $\Delta V_{th}$, rendering the positive temperature acceleration.

Moreover, the universal scaling of HCD in an LDMOS is very distinct from the one found in classical logic transistors [25], [92]–[94]. Classically, it can be expressed as $\Delta N_{it} \sim f(t/\tau)$, where $\tau(V_G, V_D, T, G)$ is a characteristic function of voltage $(V_G, V_D)$, temperature $(T)$, and geometry $(G)$. Therefore, when individual degradation curves $(I_{D,lin}(\%))$ at each bias are scaled along with the timescale, it forms a single universal degradation function. Using

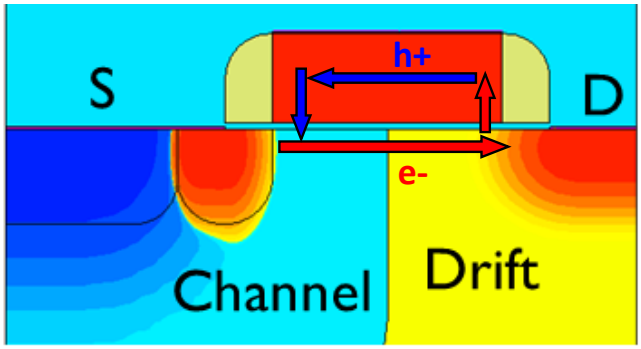



**Figure 5.4.** The schematic shows the proposed AHI-HCD theory. The HCD induced by electrons (red) and the AHI induced by holes (blue) correlate through the holes generated by the impact ionization.

the scaling function, one can project the degradation to an arbitrary combination of stress conditions. In contrast, in an LDMOS, our previous publication [19] found that the HCD universal curve should be constructed by two separate HCD degradation curves of the channel and drift regions, as shown in Fig. 5.5. The key observation is that the channel region degrades earlier than the drift region. This can serve as a probe to unravel the degradation in the two regions. In the following subsections, we will scrutinize this problem through several points of view.

### 5.2.2 HCD Recovery

HCD recovery could be an effective property to investigate because HCD involves the Si-O bond breakage (does not recover over time) or Si-H bonds at the drain corner (hydrogen released from Si-H bonds can hardly diffuse back and passivate the broken bonds at the drain corner [95]). On the other hand, NBTI/PBTI/AHI generally recovers more because of the uniform damage along the interface [17]. Again, the HCD conditions of $V_G/V_D$ = 2 V/8 V and 8 V/8 V are compared here. The experiment is designed with two cycles of stress/recovery (1000 seconds each), as shown in Fig. 5.6, where the recovery condition is at zero bias. It is not surprising that $V_G = 2$ shows a weak recovery during the recovery phase because the main mechanism is HCD in the drift region. On the other hand, $V_G = 8$ shows larger $\Delta V_{th}$ as also indicated by $\Delta I_{D,lin}$ in Fig. 5.2. Interestingly, it recovers 6 to 8% at each

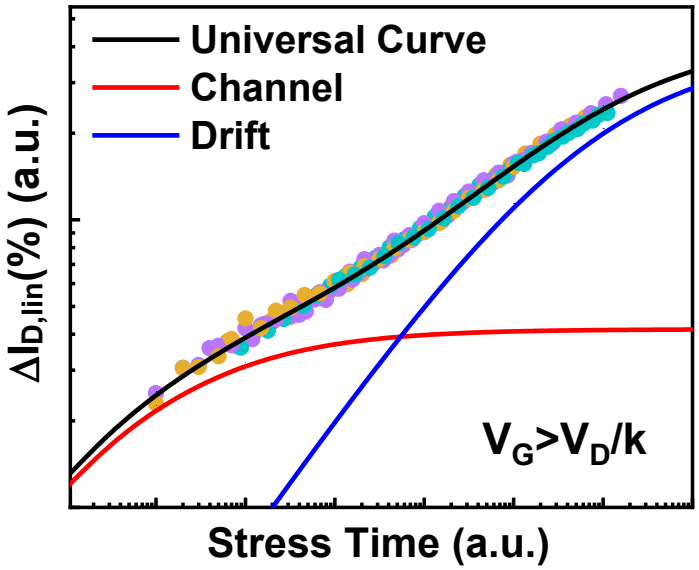



**Figure 5.5.** The decomposition of the universals scaling curve of HCD in an LDMOS. The figure is taken from [19].

recovery phase. The reason for the stronger recovery under $V_G = 8$ stress indicates that the channel region experiences other mechanisms other than HCD.

The recovery tests at different stressing moments (stressed at $V_G/V_D = 8$ V/8 V) are also investigated, as shown in Fig. 5.7. In this experiment, the recovery phase of 1000 seconds is subsequent to various stress times of 100, 1000, and 6300 seconds. The measured $\Delta V_{th}$ is normalized to its maximum for each case to visualize the recovery percentage. $\Delta V_{th}$ recovers 12.5%, 9.4%, and 3.1% after 100, 1000, 6300 seconds of stress. The stronger recovery at the earlier stage coincides with the universal scaling theory for LDMOS mentioned in Fig. 5.5. It again indicates that the channel tends to recovery while the drift does not.

### 5.2.3 Gate Leakage to Distinguish HCD and AHI

If the AHI-HCD theory illustrated in Fig. 5.4 is veracious, the temperature-dependent gate leakage current may offer us a clue. It should be pointed out that both HCD and AHI can induce the leakage current but in the opposite sign. Fig. 5.8(a) shows that the two stress voltages show an opposite sign of leakage current ($I_G$). Furthermore, they have very distinct

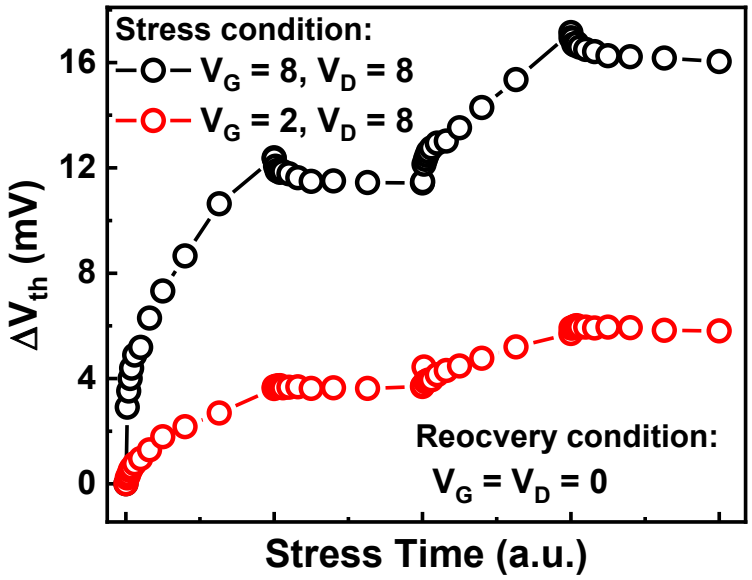



**Figure 5.6.** The comparison of threshold voltage shift under two different stress conditions with two cycles of stress/recovery processes.

temperature dependence: $I_G$ at low $V_G$ stress decreases at elevated temperatures (indicates the dominance of HCD), while $I_G$ at high $V_G$ stress is insensitive to the temperature. This, again, elucidates two completely different degradation mechanisms that dominate at the two stress conditions. At low $V_G$ stress, the strong decrease in $I_G$ is related to the weaker impact ionization. At high $V_G$ stress, if AHI is the primary cause, the holes tunnel from the poly-Si/metal side to the semiconductor and partly get recombined with the tunneling electrons, causing defect generations in the oxide. The weak temperature dependence should be attributed to the temperature insensitivity of the tunneling current. The band diagram simulations by the TCAD model are given in Figs. 5.8(c) and 5.8(d), which clearly explain the opposite sign of $I_G$. The negative electric field in the drift region at low $V_G$ stress causes the negative $I_G$. On the other hand, at high $V_G$ stress, both regions experience a positive electric field (channel > drift).

To understand more about the transition point ($V_G = V_D/k$), the measurements of $I_G$ for different $V_G$, $V_D$, and temperature is plotted in Fig. 5.8(b). It is observed that at a fixed $V_D$ bias, $I_G$ dramatically increases at higher $V_G$, referring to a higher magnitude of HCD. As

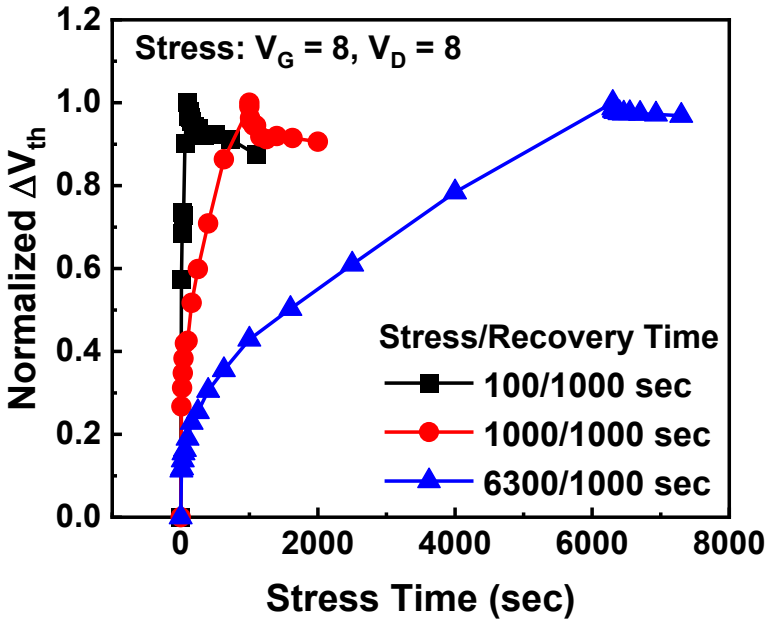



**Figure 5.7.** The normalized $\Delta V_{th}$ recovery after various stress times (to their maximum), showing the decreasing recovery percentage after a longer stress time.

$V_G$ increases to a certain point, $I_G$ gradually turns into positive (due to AHI), behaving like a V-shape. We can define the valley points as the transition points, where the AHI starts to get involved. Remarkably, given a $V_D$ bias, the turning point is approximately $V_D/2$. Also, the tunneling current is becoming visibly high when $V_D \geq 6$ V, indicating a massive increase in HCD. As mentioned previously, the negative $I_G$ shows a strong temperature dependence in the entire V-shape region, which is a characteristic of HCD. All of the observations above strongly suggest AHI as the main cause of channel degradations.

## 5.3 Correlation Between HCD and AHI

Up to now, we have experimentally proved that HCD and AHI have distinct recovery, temperature dependence, and gate leakage direction. Furthermore, we also found that AHI may be strongly accelerated by HCD. In Fig. 5.9, $\Delta V_{th}$ induced by HCD (circle) and PBTI (square) are compared. If AHI and HCD are uncorrelated and AHI in the channel region is the major reason for the dramatic increase in $V_{th}$, one should observe similarly $\Delta V_{th}$ for

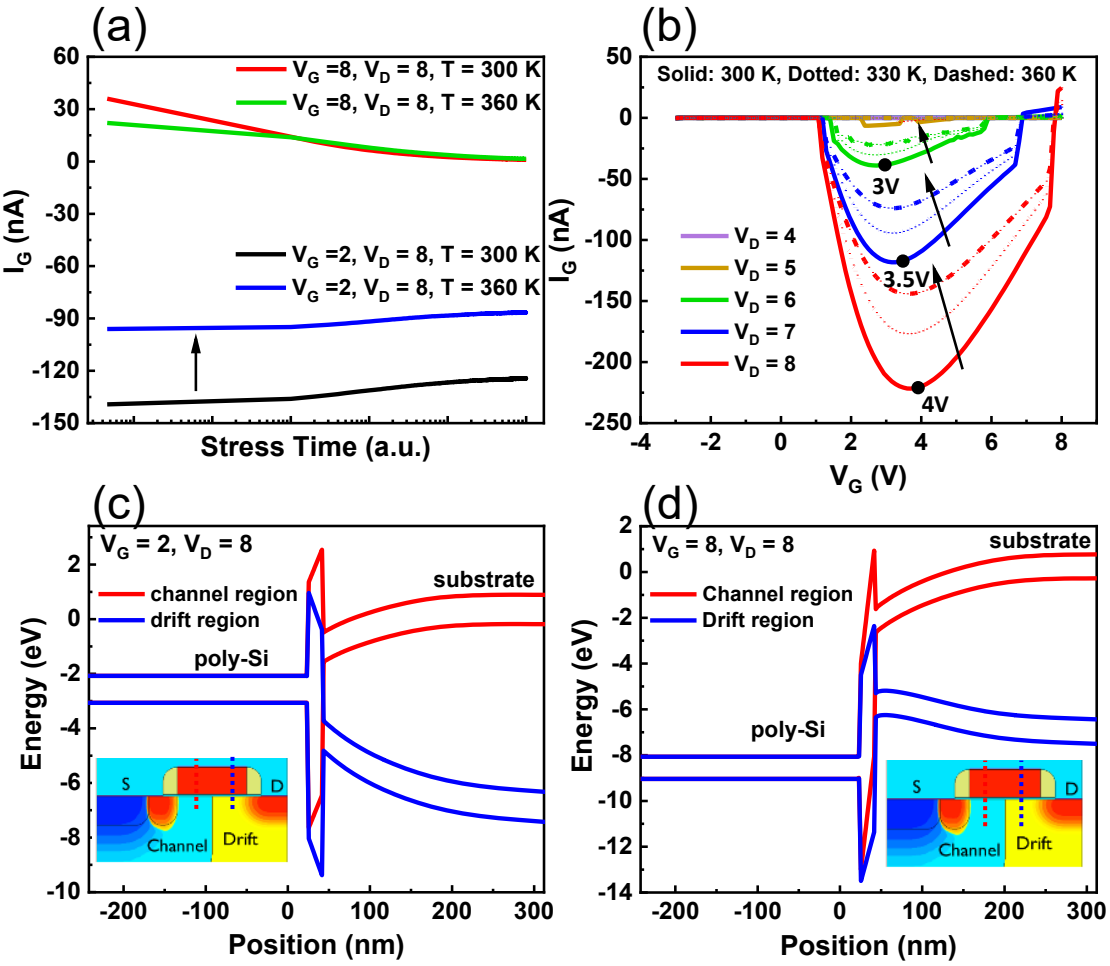



**Figure 5.8.** (a) $I_G$ vs. stress time for two stress conditions at two temperatures. (b) The full sweep of $I_G$ as a function of $V_G$, $V_D$, and temperature. The valley can be viewed as the transition point. (c)(d) The band diagram along the vertical direction at two different stress conditions for the channel and drift regions.

HCD and PBTI. However, $\Delta V_{th}$ under pure PBTI ($V_G$ = 8 V, $V_D$ = 0 V) at either low or high temperatures show a much lower $\Delta V_{th}$. In other words, PBTI alone (even with self-heating) cannot contribute to the huge $\Delta V_{th}$, the channel AHI should be assisted by another mechanism, preferably drift HCD. Therefore, we claim that *AHI and HCD are correlated*. To be more specific, AHI is accelerated by HCD. As the hot electrons are injected into the poly-Si at the drain side, the impact ionization generates electron-hole pairs (strong temperature dependence). The holes generated can then contribute to channel AHI and cause $\Delta V_{th}$.

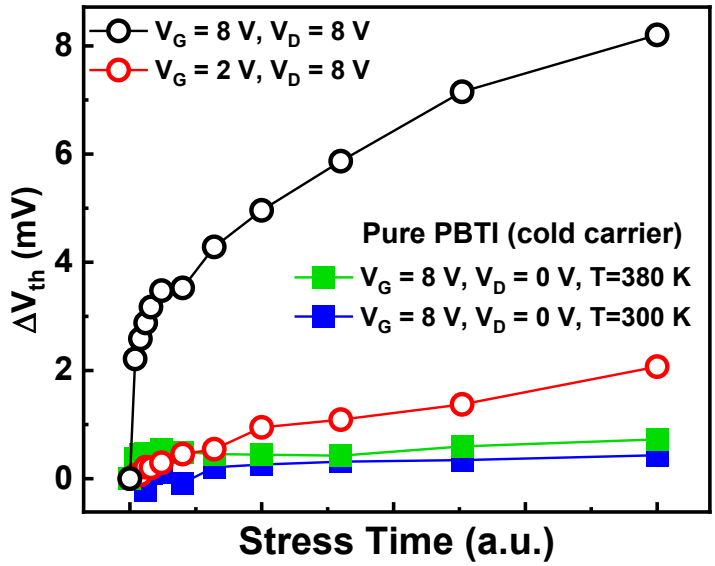



**Figure 5.9.** Comparison of $\Delta V_{th}$ between HCD and PBTI at low and high temperature. It proves that PBTI alone cannot cause sufficiently high damage.

## 5.4 Conclusions

In this chapter, we explore the origin of the channel degradation discussed in Chapters 2-4, which only occurs at high $V_G$ stress. Unlike the classical HCD observed in the drift region, the channel degradation (proposed to be AHI) has very distinct properties. The channel AHI shows a more significant recovery, positive temperature activation in $\Delta V_{th}$, and negligible temperature-dependence in $I_G$. At a fixed $V_D$ stress, the dominant mechanism gradually switches from HCD to AHI at increasing $V_G$ stress, confirmed by $\Delta V_{th}$ and $I_G$. Finally, the correlation between drift HCD and channel AHI is linked by the holes generated from the impact ionization. HCD in the drift region is still the driving force of channel degradations caused by AHI. In summary, we propose the root cause of channel degradation in the LDMOS to be HCD-assisted AHI, as validated and explained by the experimental evidence from several perspectives.

# 6. OXIDE ELECTRONICS: β-GALLIUM OXIDE

## 6.1 Introduction to Oxide Semiconductors

Oxide semiconductors are broadly researched for various purposes, including dielectrics, ferroelectrics, magnetics, piezoelectric, and high-temperature superconductors. One important point making it different from prevalent semiconductors such as Si is that oxide semiconductor is usually N-type. This can be attributed to its special chemical bonding nature. For oxide semiconductors, the conduction band edge is primarily composed of the s-orbital of the metal ions, while the valence band edge is mainly from the p-orbital of the oxygen ions. The strong electro-negative nature of the oxygen ions makes the valence band edge so deep in the band diagram, and hence difficult to dope with holes [96]. Given the rarity of its P-type forms, its applications in circuits were restricted until some P-type oxide semiconductors are demonstrated, such as $CuAlO_2$ in 1996 [97].

In the beginning, the polycrystalline oxide semiconductors are the main focus, such as ZnO and $SnO_2$. However, the polycrystalline oxide semiconductors are electrically unstable due to the nature of surfaces and grain boundaries [98], [99]. This issue was resolved by the adoption of an amorphous oxide semiconductor (AOS), starting from late 2004 [100]. AOS has no grain boundaries and has great advantages in large-area fabrications, which is strongly suitable for display applications, e.g., amorphous In-Ga-Zn-O (a-IGZO). Another advantage of oxide semiconductors is the relatively large bandgap. For example, bulk β-$Ga_2O_3$ has a wide bandgap of 4.6 to 4.9 eV [101] so that it is a promising candidate in the field of power electronics. In Chapters 6 and 7, we will focus on two types of oxide semiconductors: β-$Ga_2O_3$ and $In_2O_3$, and their potential reliability issues for future adoptions. In this chapter[1], β-$Ga_2O_3$ is targeted at power electronics. While in the next chapter, $In_2O_3$ is mainly investigated as back-end-of-line (BEOL) compatible thin-film transistors (TFTs).

[1]↑The content of this chapter is taken from our publications [102], [103]

## 6.2 Device and Material Properties of β-$Ga_2O_3$

### 6.2.1 Material Properties

Gallium oxide ($Ga_2O_3$) is an emerging material that has great potential to be the next-generation power device material. There are five different polymorphs of $Ga_2O_3$, namely, the monoclinic (β-$Ga_2O_3$), rhombohedral (α), defective spinel (γ), cubic (δ), or orthorhombic (ε) structures [104]. Among them, β-$Ga_2O_3$ is the most widely studied one because of its stability in the normal condition of temperature and pressure.

The unit cell of the stable phase, β-$Ga_2O_3$ (shown in Fig. 6.1), contains two crystallographically different Ga atoms in the asymmetric unit, one with tetrahedral and the other with octahedral coordination geometry [105]. Therefore, there is a strong anisotropy in its physical properties. For example, the electron mobilities in β-$Ga_2O_3$ Schottky barrier diodes (SBDs) shows an anisotropy. The $(\bar{2}\,0\,1)$ SBD has 2 times higher mobility than that of $(0\,1\,0)$ SBD [106]. The electron effective mass was calculated as $0.34m_0$ ($m_0$ is the free electron mass) [105] and a very large hole effective mass because of the relatively flat valence band. Sometimes they are reported to be not free to move but form localized polarons [107]. The bandgap ($E_g$) of β-$Ga_2O_3$ is reported to be 4.6-4.9 eV, which is higher than Si (1.1 eV), 4H-SiC (3.25 eV), and GaN (3.4 eV). In terms of critical field ($E_c$), it is 2 to 3 times higher than SiC and GaN. Hence, it is expected that β-$Ga_2O_3$ can offer higher breakdown voltage ($V_{BD}$). Table 6.1 lists some important properties of common materials including β-$Ga_2O_3$.

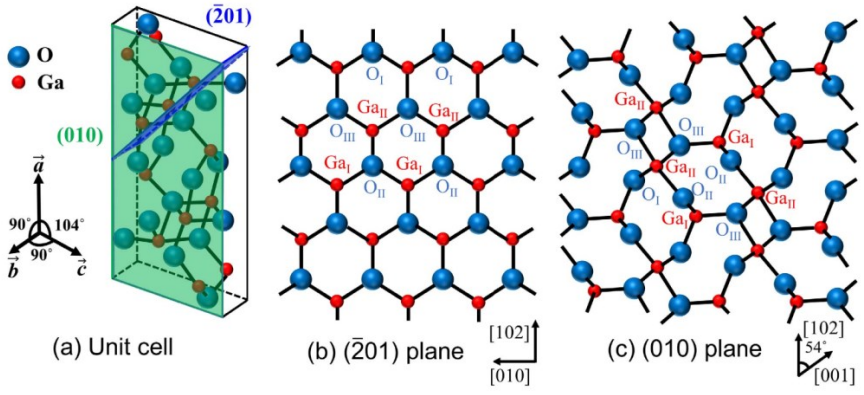



**Figure 6.1.** (a) β-$Ga_2O_3$ unit cell. (b) $(\bar{2}\,0\,1)$ plane, and (c) $(0\,1\,0)$ plane. The picture is taken from Ref. [106].

**Table 6.1.** Physical properties of commonly used materials including β-$Ga_2O_3$. The Figure of Merits (FOMs, in bold) are the relative values compared to Si [107].

| **Material Parameters** | **Si** | **4H-SiC** | **GaN** | **β-$Ga_2O_3$** | **Diamond** |
|---|---|---|---|---|---|
| Bandgap, $E_g$ (eV) | 1.1 | 3.25 | 3.4 | 4.85 | 5.5 |
| Breakdown Field, $E_c$ (MV/cm) | 0.3 | 2.5 | 3.3 | 8 | 10 |
| Electron Mobility, $\mu$ ($cm^2V^{-1}s^{-1}$) | 1480 | 1000 | 1250 | 300 | 2000 |
| Dielectric Constant, $\varepsilon$ | 11.8 | 9.7 | 9.0 | 5.5 | 10 |
| Thermal Conductivity, $\lambda$ ($Wcm^{-1}K^{-1}$) | 1.5 | 4.9 | 2.3 | 0.1-0.3 | 20 |
| **Baliga FOM** | 1 | 317 | 846 | 3214 | 24660 |
| **Keyes' FOM** | 1 | 3.6 | 1.8 | 0.2 | 41.5 |
| **Baliga High Frequency FOM** | 1 | 46.3 | 100.8 | 142.2 | 1501 |
| **Johnson FOM** | 1 | 278 | 1089 | 2844 | 1110 |
| **Huang's Chip Area FOM** | 1 | 48 | 85 | 279 | 619 |

### 6.2.2 Figure of Merits

There are several figure-of-merits (FOMs) that are widely used: 1) Baliga's FOM (BFOM $= \varepsilon\mu E_c^3$) [108] is derived from DC condition. It also shows the trade-off between the specific on-resistance $R_{on,sp}$ and $V_{BD}$. The $R_{on,sp} - V_{BD}$ relation for different materials is shown in Fig. 6.2. We can see the potential of β-$Ga_2O_3$ over SiC and GaN. 2) Baliga high-frequency FOM (BHFFOM $= \mu E_c^2$) [109] is more practical because the transistors usually operate in AC conditions. 3) Johnson figure of merit (JFOM $= E_c^2 V_s^2/4\pi^2$) [110] represents the power-frequency product for RF amplification. 4) Huang's Chip Area FOM (HCAFOM $= \varepsilon\sqrt{\mu}E_c^2$) [111] accounts for the manufacturability and cost value. 5) Keyes' FOM (KFOM $= \lambda\sqrt{cV_s/(4\pi\varepsilon)}$) [112] measures the thermal capability for minimum delay time. From Table 6.1, we can notice that all FOMs except Keyes' FOM anticipate β-$Ga_2O_3$ to be more superior than GaN and SiC because only Keyes takes thermal conductivity into account. In other words, the most serious problem of β-$Ga_2O_3$ may be its low thermal conductivity.

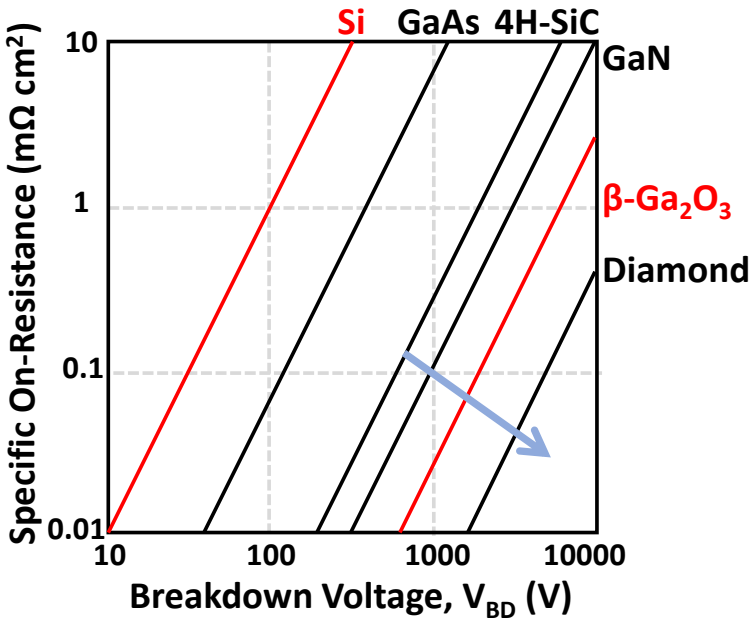



**Figure 6.2.** Theoretical $R_{on,sp} - V_{BD}$ relation for various materials. The arrow points to the desired direction with higher performance.

### 6.2.3 Challenges of β-$Ga_2O_3$ FETs

The fabrications of β-$Ga_2O_3$ FETs also have difficulties: 1) Ohmic contact between the electrode and the channel layer is hard to achieve because wide-bandgap typically has a large barrier height [113]. The insertion of an intermediate layer or a heavily doped semiconductor layer under the metal is necessary. Without good ohmic contacts, poor contact resistance will undermine the performance. 2) Enhancement-mode (E-mode) is relatively rare to be reported but better than depletion-mode (D-mode) devices for practical use. The reason is the absence of p-type β-$Ga_2O_3$ to form a bipolar junction [114]. 3) The holes in β-$Ga_2O_3$ are self-trapped so that it limits the β-$Ga_2O_3$ FET to be unipolar [107]. 4) The thermal management approach is required to compensate for the low thermal conductivity of β-$Ga_2O_3$ and its substrates [102]. In the following sections, we will investigate β-$Ga_2O_3$ FET on various substrates: Sapphire, $SiO_2$/Si, and Diamond. The experimental data and simulations can provide us with strategies for thermal management. This self-heating effect sets an upper limit to the transistor driving current ($I_{max}$) and output power ($P_{max}$) to ensure reliable and safe operations, which will be the main goal of this chapter. The analyses will be done through simulations and analytical derivations.

## 6.3 Substrate-Aware β-$Ga_2O_3$ FET Performances

The β-$Ga_2O_3$ FET under study is shown in Fig. 6.3. There are three types of β-$Ga_2O_3$ FETs with different substrates, that is, $SiO_2$/Si, Sapphire, and Diamond. Fig. 6.3(b) shows the side view of the one on $SiO_2$/Si substrate. All the dimensions are kept the same when the substrate is replaced by another. To investigate their physical properties and the circuit performances, the TCAD and compact model (written in Verilog-A) have been developed and calibrated to match the experimental I-V curves, as shown in Fig. 6.4. For the compact model, the MIT Virtual Source GaNFET-RF HSPICE model [115] is adopted with correct dimensions, mobility $\mu$, thermal resistance $\theta_{th}$, thermal capacitance $C_{th}$ to ensure a reasonable electro-thermal behavior. Usually, power circuits such as boost/buck converter require much wider devices to support the high current, in the range of millimeters [116], [117]. Therefore, the $\theta_{th}$ simulated from the TCAD simulations need to be adjusted accord-

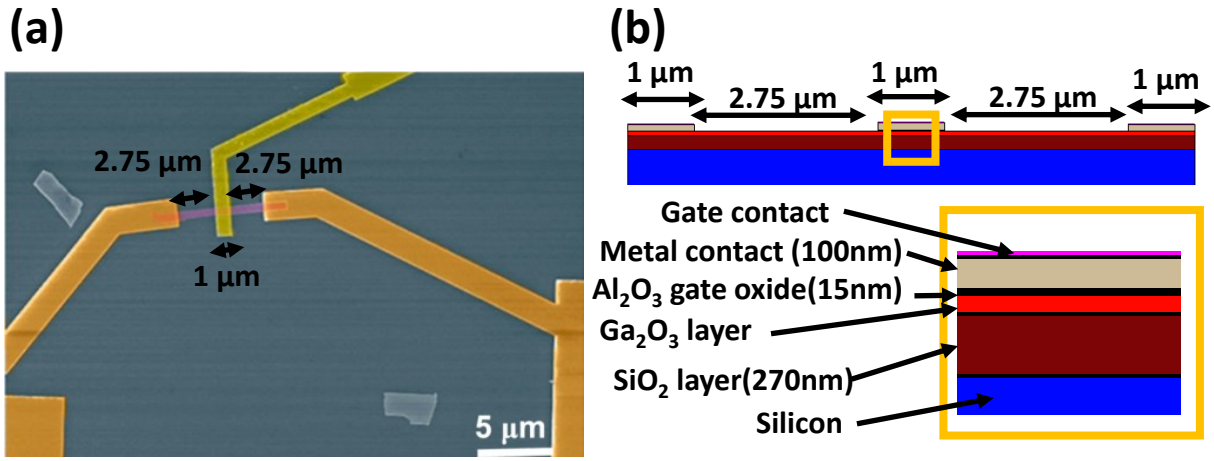



**Figure 6.3.** (a) The front view of the β-$Ga_2O_3$ FET. (b) The side view of the β-$Ga_2O_3$ FET on $SiO_2$/Si (SOI) substrate.

ingly for accurate circuit simulations. Since the TCAD simulation for wider devices is not efficient, COMSOL is used instead for large-scale $\theta_{th}$ simulation. The COMSOL simulations are carried out in 2D under the premise of being uniform in the $z$-direction (width, $W$) as the width is much larger than the length of the device ($W \gg L$). The width of the devices is set to be 0.5 mm, the heat source (∼1 µm long) is set to be under the gate terminal and the heat sink is set at the bottom of the substrate. The thermal conductivity and the thickness of each layer are listed in Table 6.2(a). With the parameters given, the simulated $\theta_{th}$ of the β-$Ga_2O_3$ FET on the three substrates are shown in Table 6.2(b). Clearly, the substrate with high thermal conductivity can dramatically reduce the effective $\theta_{th}$. That explains why the β-$Ga_2O_3$ FET on Diamond shows the best performance. Those $\theta_{th}$ will be used further in the circuit simulations in the following section.

## 6.4 Substrate-Aware β-$Ga_2O_3$ Circuit Performances

The boost converter circuit simulations were carried out to estimate their practical performances. Since the β-$Ga_2O_3$ FET needs to be turned off and on periodically, we chose our driving clock to have a lower limit of −10 V and the higher limit of 0 V, keeping the

**Table 6.2.** (a) The thermal conductivity and the thickness used in COMSOL simulations. (b) The simulated $\theta_{th}$ of the β-$Ga_2O_3$ FETs on Diamond, Sapphire, and $SiO_2$/Si (SOI) substrates.

**(a)**

| **Material** | **λ (W cm$^{-1}$K$^{-1}$)** | **Thickness** |
|---|---|---|
| β-$Ga_2O_3$ | 0.1 | 50 nm |
| Diamond | 10 | 50 nm |
| Sapphire | 0.4 | 50 µm |
| Silicon | 0.8 | 270 nm |
| $SiO_2$ | 0.025 | 50 µm |

**(b)**

| **Structure** | **$\theta_{th}$ (K/W)** |
|---|---|
| β-$Ga_2O_3$/Diamond | 47 |
| β-$Ga_2O_3$/Sapphire | 233 |
| β-$Ga_2O_3$/$SiO_2$/Si | 458 |

chosen $V_{th}$ well within the operating voltage limits and giving the FETs a reasonably good operating range. To have both high enough efficiency and conversion ratio, a duty cycle of 30% was chosen for all the simulations. Other circuit parameters are summarized in the caption of Fig. 6.5. The results demonstrate that the self-heating effect caused by the high thermal resistance can degrade the efficiency of the boost converter severely. The power conversion efficiency ($= P_{out}/P_{in}$) is also simulated as a function of the clock frequency, as shown in Fig. 6.6. It is worth noting that by adopting the Diamond structure, β-$Ga_2O_3$ FET can achieve a power efficiency of 85-91%, which is closer to the more matured GaN HEMT with an efficiency of 96% [118]. To address this self-heating issue, we need strategies to reduce self-heating. Some solutions have been proposed such as inserting an intermediate layer with high thermal conductivity, i.e., h-BN [119], to assist the heat spreading. However, to the best of our knowledge, there is no analytical thermal transport model developed for a multi-layered system like β-$Ga_2O_3$ FET. In the following sections, we will develop the first simple analytical model for the multilayered structures.

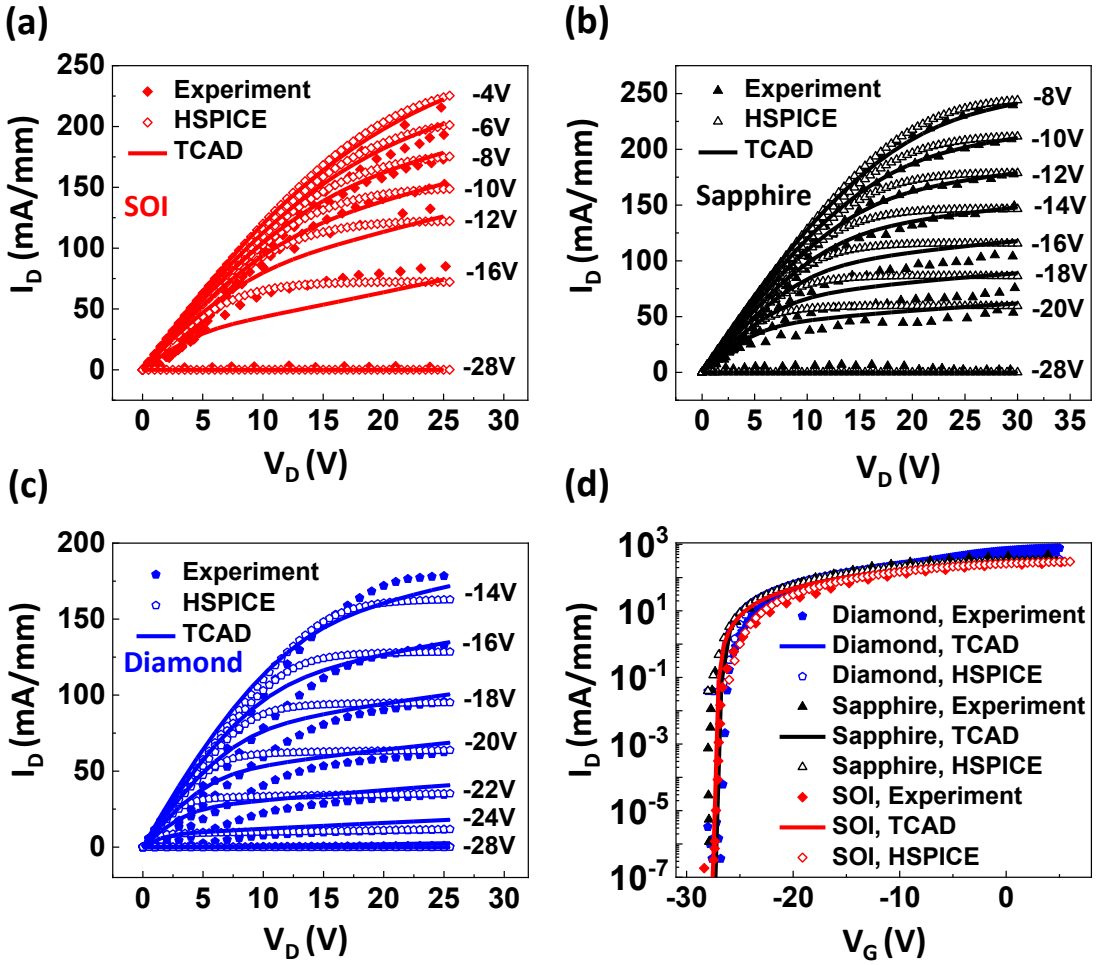



**Figure 6.4.** Output characteristics obtained from experiments, TCAD and HSPICE compact model for (a) $SiO_2$/Si (SOI) (b) Sapphire (c) Diamond substrates. (d) Transfer characteristics of β-$Ga_2O_3$ FETs on the three substrates. The TCAD and HSPICE model reproduces the experimental data accurately.

## 6.5 Analytical Thermal Resistance Model: Bilayered Structures

The analytical form of $\theta_{th}$ for bilayered structures has been reported in Ref. [120], based on multi-finger AlGaN-GaN High Electron Mobility Transistors (HEMTs). The 3D thermal transport from the channel (heat source) to the bottom of the substrate (heat sink) acts as a spheroid, as described in Fig. 6.7. The total thermal resistance $\theta_{total}$ can be split into three parts: 1) The uniform 2D cylindrical propagation between two planes. 2) The prolate spheroid propagation. 3) The elliptic cylindrical propagation. They can be added up as

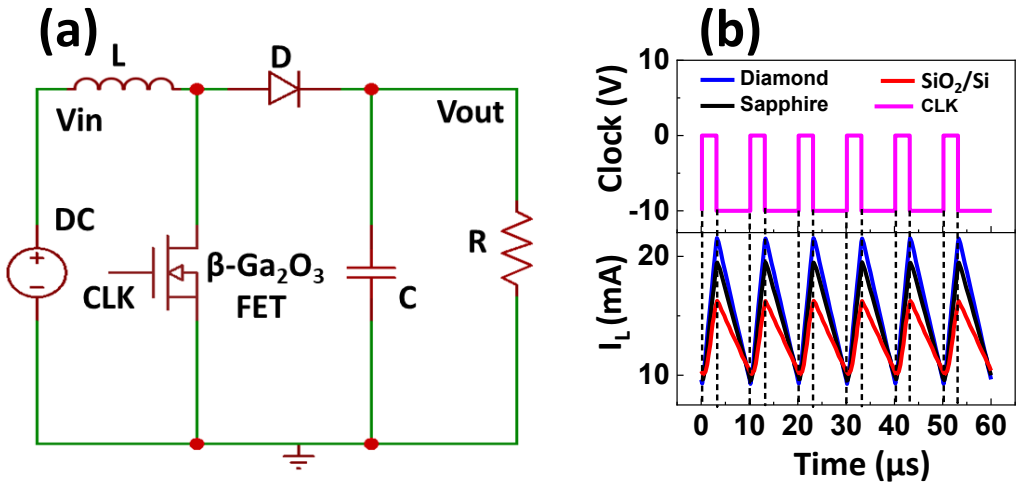



**Figure 6.5.** (a) The boost converter circuit used in our analysis. Circuit parameters: inductor, L = 3 mH, FET = β-$Ga_2O_3$ on SOI/Sapphire/Diamond; output capacitance, C = 50 μF; Schottky diode, D; load resistance, R = 2 kΩ; input voltage, $V_{in}$; output voltage, $V_{out}$. The Schottky diode, SBR3U100LP with forward voltage drop, $V_F$ = 0.79 V, and total capacitance, $C_T$ = 800 pF was used. (b) The transient inductor currents with β-$Ga_2O_3$ FETs on three different substrates. The HSPICE simulation code is provided in Appendix C.

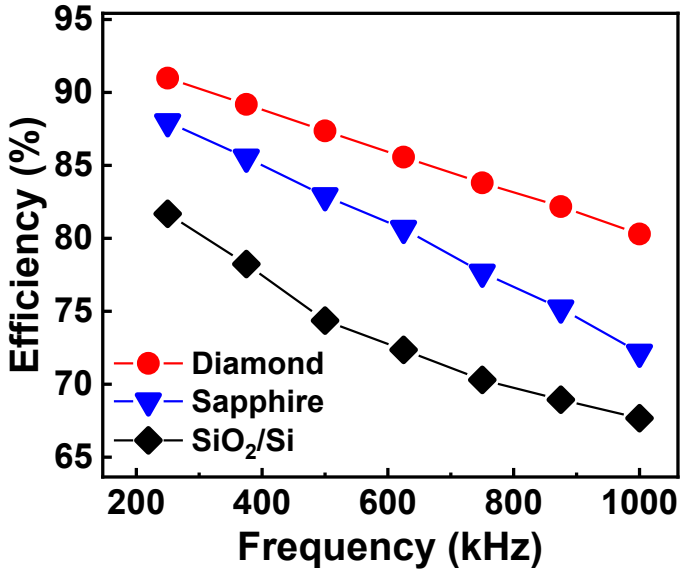



**Figure 6.6.** Efficiency of the boost converter circuits with β-$Ga_2O_3$ FET on Diamond (500 μm), Sapphire (500 μm), and $SiO_2$/Si (270 nm/500 μm).

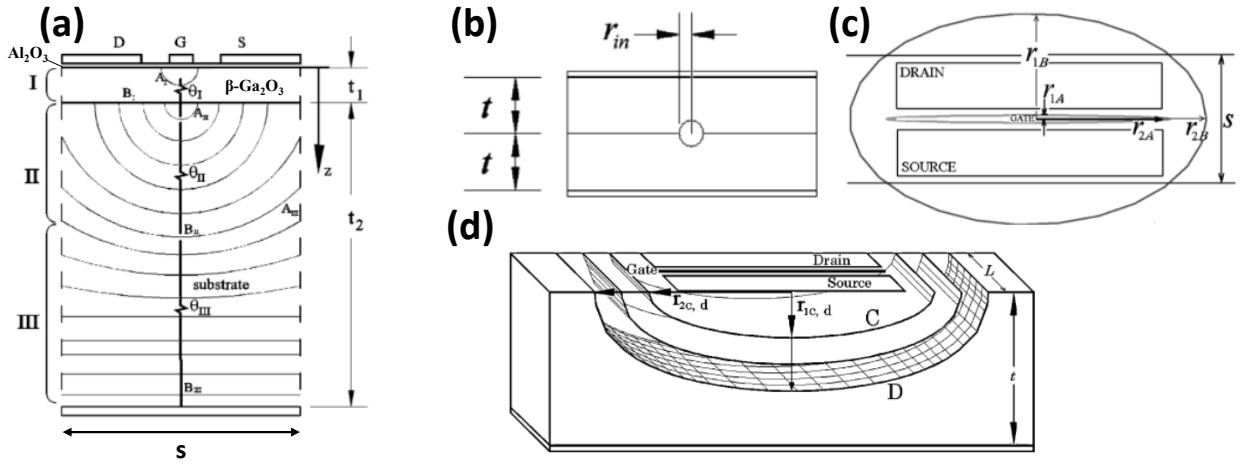



**Figure 6.7.** (a) The side view of the HEMT structure. (b) Region I: uniform 2D cylindrical. (c) Region II: prolate spheroid. (d) Region III: elliptic cylindrical. Region II and III represent the heat spreading in the substrate. The index 1 stands for the channel material and 2 for the substrate material.substrates. The figures are taken from Ref. [120].

$\theta_{total} = \theta_I + \theta_{II} + \theta_{III}$. The model was constructed assuming $W_g \gg L_g$, and it has the multi-parallel finger with the periodic length s. The individual $\theta$ can be derived as follows:

$$\theta_I = \frac{1}{\pi W_g \lambda_1} \ln\left(\frac{4t_1}{\pi L_g}\right). \tag{6.1}$$

$$\theta_{II} = \frac{1}{2\pi\lambda_{sub} R}\left[\ln\left(\tanh\left(\frac{\varphi_B}{2}\right)\right) - \ln\left(\tanh\left(\frac{\varphi_A}{2}\right)\right)\right] \quad \text{with} \quad \varphi_A = \frac{1}{2}\ln\left(\frac{r_{2A}+r_{1A}}{r_{2A}-r_{1A}}\right), \varphi_B = \frac{1}{2}\ln\left(\frac{r_{2B}+r_{1B}}{r_{2B}-r_{1B}}\right). \tag{6.2}$$

$$\theta_{III} = \frac{1}{2\pi s\lambda_{sub}}\left[ln\left(\frac{R_{2B}+R_{1B}}{R_{2B}-R_{1B}}\right) - ln\left(\frac{R_{2A}+R_{1A}}{R_{2A}-R_{1A}}\right)\right]. \tag{6.3}$$

To distinguish between regions II and III, the notation '$r$' is used in region II and '$R$' in region III. To facilitate simpler calculations and explicit physical concepts, we will further simplify the expression of $\theta_{II}$ and $\theta_{III}$ and verify with the COMSOL simulations. For a few micrometers depth in the substrate (region II), we have $r_{2A} = \frac{W_g}{2}, r_{1A} = \frac{4k_1}{\pi^2\lambda_{sub}}t_1, r_{1B} = \frac{s}{\sqrt{2}}, r_{2B} = \sqrt{R^2 + r_{1B}^2}$ due to $R = \sqrt{r_{2A}^2 - r_{1A}^2} = \sqrt{r_{2B}^2 - r_{1B}^2}$. It is worth noting that $r_{1A}$ is proportional to the relative thermal conductivity of the layer on top of the substrate. If there

is an interlayer before the substrate, simply replace $r_{1A}$ as $\frac{4\lambda_{int}}{\pi^2\lambda_{sub}}t_{int}$. By putting reasonable numbers in, we will notice that for a wide enough device, $r_{2A} \gg r_{1A}$, meaning $R \approx \frac{W_g}{2}$. Also, if the length of the device $s$ is short compared to $R$, which is valid most of the time, we have $r_{2B} \gg r_{1B}$. We may define new parameters: $r_A^{II} = \frac{r_{2A}}{r_{1A}} = \frac{\pi^2 W_g}{8t_1}\frac{\lambda_{sub}}{\lambda_1}$, $r_B^{II} = \frac{r_{2B}}{r_{1B}} \approx \frac{W_g}{\sqrt{2}s}$ Therefore, Eq. (6.2) can be further simplified as

$$\theta_{II} = \frac{1}{\pi\lambda_{sub}W_g}\ln\left[\frac{r_A^{II}-1}{r_B^{II}-1}\right]. \tag{6.4}$$

Here we can notice that $r_A^{II}$ is proportional to the substrate-to-channel thermal conductivity ratio while $r_B^{II}$ is proportional to the width-to-length dimension ratio. $\theta_{II}$ suggests that the material-wise strategy is to enhance the channel thermal conductivity, and the dimension-wise is to make it wider or longer.

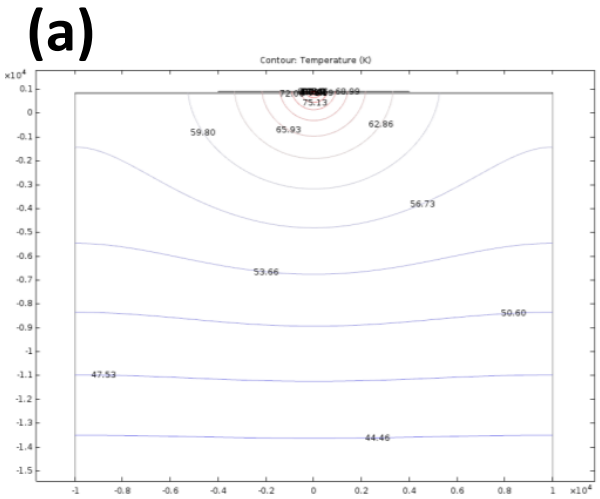
In terms of Region III, we have, $R_{1A} = \frac{s}{\sqrt{2}}, R_{2A} = \sqrt{R^2 + r_{1A}^2}, R_{1B} = \frac{\pi}{2}(t_1 + t_2), R_{2B} = \sqrt{R^2 + r_{2B}^2}$. Again, new parameters can be defined: $r_A^{III} = \frac{R_{2A}}{R_{1A}} \approx \frac{\frac{W_g}{2}}{\frac{s}{\sqrt{2}}}$, $r_B^{III} = \frac{R_{2B}}{R_{1B}} \approx \frac{\sqrt{\left(\frac{W_g}{2}\right)^2 + \left(\frac{\pi}{2}t_2\right)^2}}{\frac{\pi}{2}t_2} \approx \frac{W_g}{\pi t_2}$. If the length of the device $s$ is short compared to $R$, $r_A^{III}$ can be neglected, that is,

$$\theta_{III} = \frac{1}{2\pi s\lambda_{sub}}\ln\left[\frac{r_B^{III}+1}{r_B^{III}-1}\right]. \tag{6.5}$$

Here we can notice that $r_B^{III}$ is proportional to the ratio of gate width and substrate thickness. The thinner substrate makes larger $r_B^{III}$ but smaller $\theta_{III}$. It suggests that wafer thinning can be another possible remedy for reducing total thermal resistance. In summary, the simplified analytical model can be expressed as,

$$\theta_{total} = \frac{1}{\pi W_g\lambda_1}\ln\left(\frac{4t_1}{\pi L_g}\right) + \frac{1}{\pi\lambda_{sub}W_g}\ln\left[\frac{\frac{\pi^2 W_g}{8t_1}\frac{\lambda_{sub}}{\lambda_1}-1}{\frac{W_g}{\sqrt{2}s}-1}\right] + \frac{1}{2\pi s\lambda_{sub}}\ln\left[\frac{\frac{W_g}{\pi t_2}+1}{\frac{W_g}{\pi t_2}-1}\right]. \tag{6.6}$$

This model can also be applied to the cases with a high $\lambda$ interlayer, simply by replacing $\lambda_1$ and $t_1$ with $\lambda_{int}$ and $t_{int}$ because the interlayer has negligible contribution to the total thermal resistance but helps to reduce $\theta_{II}$. We will examine how the simplified analytical model performs comparing to 2D COMSOL simulation on the multilayered structure with β-$Ga_2O_3$ (50 nm)/h-BN (50 nm)/Si (50 µm). As shown in Fig. 6.8(b), the analytical model works well




(b)

| Material | 2D COMSOL $\theta_{th}$(K/W) | 3D Analytical $\theta_{th}$(K/W) |
|---|---|---|
| $Ga_2O_3$ | 37 | 30.75 |
| h-BN | 2 | 0.51 |
| Si (10μm) | 33 | 36.06 |
| Si (40μm) | 50 | 50.26 |
| Total $R_{th}$ | 122 | 117.58 |

**Figure 6.8.** (a) The isothermal line in the COMSOL simulation. (b) The comparison of the simulated (COMSOL) $\theta_{th}$ and calculated (Eq. (6.6)) $\theta_{th}$.

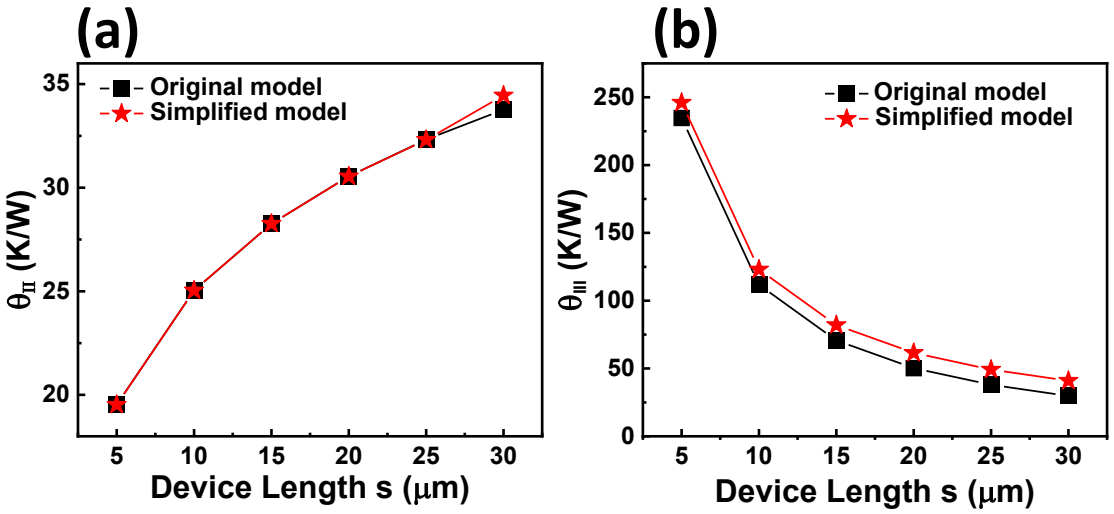



**Figure 6.9.** Comparison of the original [120] and simplified analytical model for (a) $\theta_{II}$ (b) $\theta_{III}$ with respect to the device length.

on reproducing the results from the COMSOL simulations (Fig. 6.8(a)). Furthermore, we should also examine how good our approximations of the preexisting 3D analytical model are. In Fig. 6.9, as mentioned before, although the approximation might be less and less accurate when the length of the device s becomes larger, the simplification still works reasonably well.

All those comparisons confirm that our new simplified analytical model can predict $\theta_{th}$ of the multilayered structure very well. After putting values in Eq. (6.6), we conclude that inserting an interlayer between the channel material and the substrate can help to reduce the total $\theta_{th}$. In the next section, we will investigate the self-heating problem from another angle: the maximum performance (current and power) given a maximum allowable temperature.

## 6.6 $I_{max}$ and $P_{max}$ Limits for Lateral Transistors

### 6.6.1 Analytical Form of $I_{max}$ Limit (DC)

Since the device mobility degrades with increasing temperature, the device junction temperature is required to be well below the maximum junction temperature ($T_{j,max}$) to maintain proper functionality. In other words, for a given material, geometry, structure, and package (i.e., given $\theta_{th}$), the maximum allowable power dissipation ($P_{max}$) can be represented as,

$$P_{max} = \frac{\Delta T_{max}}{\theta_{th,j-c} + \theta_{th,c-a}}, \tag{6.7}$$

where $\Delta T_{max}$ is the maximum temperature rise, ($\Delta T_{max} = T_{j,max} - T_{amb}$), $T_{amb}$ is the ambient temperature, $\theta_{th,j-c}$ and $\theta_{th,c-a}$ are junction-to-case and case-to-ambient thermal resistances. $P_{max}$ can be directly linked to the maximum current rating ($I_{max}$) if only the conduction loss is considered. To determine $I_{max}$ for a device, $T_{j,max}$ is fixed. To determine the intrinsic limiting performance, we neglect $\theta_{th,c-a}$ (can vary with different package configurations) and switching loss (may vary with different gate drive circuits and switching conditions [111]). Therefore, the maximum allowable current density can be written as,

$$I_{max} = \sqrt{\frac{\Delta T_{max}}{\theta_{th,j-c} R_{on}(T_{j,max})}}, \tag{6.8}$$

where $I_{max}$ is the maximum allowable current in a device at $\Delta T_{max}$. Let us assume $\theta_{th,j-c} = (W \lambda_{sub} S)^{-1}$, where $W$ is the device width, $\lambda_{sub}$ is the substrate thermal conductivity, and $S$ is the shape factor [121], $R_{on}(T_{j,max})$ is the on-resistance at $T_{j,max}$. In practice, one can easily obtain the shape factor for a technology from thermal modeling and/or experimental

measurements [122], [123]. Note that effective $\theta_{th,j-c}$ (for the packaged chip) can change with duty cycle and frequency. For a lateral device, the normalized $I_{max}$ can be written as,

$$\frac{I_{max}}{W} = \sqrt{D_{dr}}\sqrt{\frac{\lambda_{sub} S \Delta T_{max}}{R_{on,sp}(T_{j,max})}}, \tag{6.9}$$

where $R_{on}$ is replaced with $R_{on} = R_{on,sp}/(W D_{dr})$ so that Baliga's FOM (BFOM) [108] can be used. $D_{dr}$ is the drift region thickness. It can be easily adapted for vertical devices by interchanging $D_{dr}$ with the gate length. Substituting the $R_{on,sp}(T_{j,max})$ to account for mobility degradation $(T_{j,max}/300)^{\gamma}$ and possible dopant ionization rate $\xi$ as derived in Ref. [103], so as to obtain a metric to compare the maximum current for various WBG semiconductors:

$$\frac{I_{max}}{W} \propto \sqrt{\frac{\varepsilon \mu_n E_c \lambda_{sub} S \Delta T_{max}}{\frac{\xi(T_{off})}{\xi(T_{j,max})}\left(\frac{T_{j,max}}{300}\right)^{\gamma}}}. \tag{6.10}$$

$\varepsilon$ (dielectric constanct), $\mu_n$ (electron mobility), $E_c$ (breakdown field) are the fundamental parameters of the channel material. The material-dependent factor, $\gamma$, describes how mobility decreases with elevated temperatures. The corresponding generalization of $I_{max}$ (Eq. (6.10)) provides a new limit that explicitly accounts for the first time, the effect of temperature-dependent mobility, shape factor, and incomplete ionization.

The effect of SH is more severe in lateral devices compared to vertical devices, and hence lateral devices are compared for demonstration in various WBG materials. The device dimensions and basic parameters used for calculations are tabulated in Table 6.3. $\theta_{th}$ is calculated considering 3D thermal spreading (Eq. (6.6)). By alternating the corresponding $\lambda$ for channel and substrate material, the $I_{max}$ FOM at fixed $\Delta T_{max}$ (150 K here) for various WBG materials can be easily calculated as Fig. 6.10(a). It shows the calculated values

**Table 6.3.** Device dimensions used in analytical calculations.

| | **Length (µm)** | **Width (µm)** | **Thickness (µm)** |
|---|---|---|---|
| Single Layer | 4 | 50 | 300 |
| Bilayer(Top) | 4 | 50 | 5 |
| Bilayer(Bottom) | 4 | 50 | 300 |

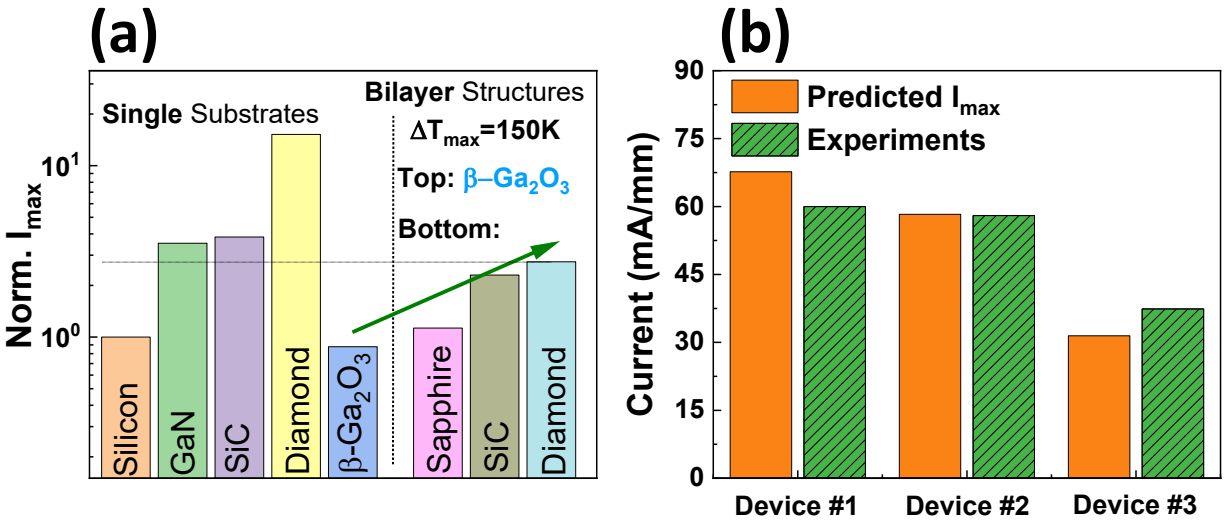



**Figure 6.10.** (a) (Left) Normalized $I_{max}$ metric for WBG materials at $\Delta T_{max}$ =150 K. (Right) β-$Ga_2O_3$ channel layer on various substrates (Sapphire, SiC, Diamond). The performance (e.g., $I_{max}$) can be improved by depositing β-$Ga_2O_3$ on substrates with higher thermal conductivity. The arrow indicates increasing performance of β-$Ga_2O_3$ FETs. (b) Comparison of $I_{max}$ predicted by the analytical form with the data from the literature: device #1 [124], #2 [125], #3 [126].

normalized to the value of Si, including the bulk material (left half). For bulk materials, at the same $\Delta T_{max}$, GaN and SiC outperform Si about 3.5 to 3.8 times in $I_{max}$. Bulk β-$Ga_2O_3$, however, performs worse than GaN and SiC. As shown in Fig. 6.10(b), the $I_{max}$ values predicted by Eq. (6.10) reproduces the experimentally obtained current for β-$Ga_2O_3$ in Ref. [124]–[126] for completely different geometric configurations. The prediction of Device #3 is slightly lower compared to the experimental data, which could be due to the uncertainty (10% to 20% [127]) in the Raman Thermography technique used to obtain the peak channel temperature. It is worth emphasizing that the $I_{max}$ metric considers stand-alone device performance under DC operation, which is different from the circuit performance shown in Fig. 6.6.

To improve $I_{max}$ (right half, Fig. 6.10(a)), we consider β-$Ga_2O_3$ on various substrates with higher thermal conductivity. The device dimensions of the bilayer structure (β-$Ga_2O_3$ on various substrates) are also tabulated in Table 6.3. The $I_{max}$ metric assigns β-$Ga_2O_3$ a

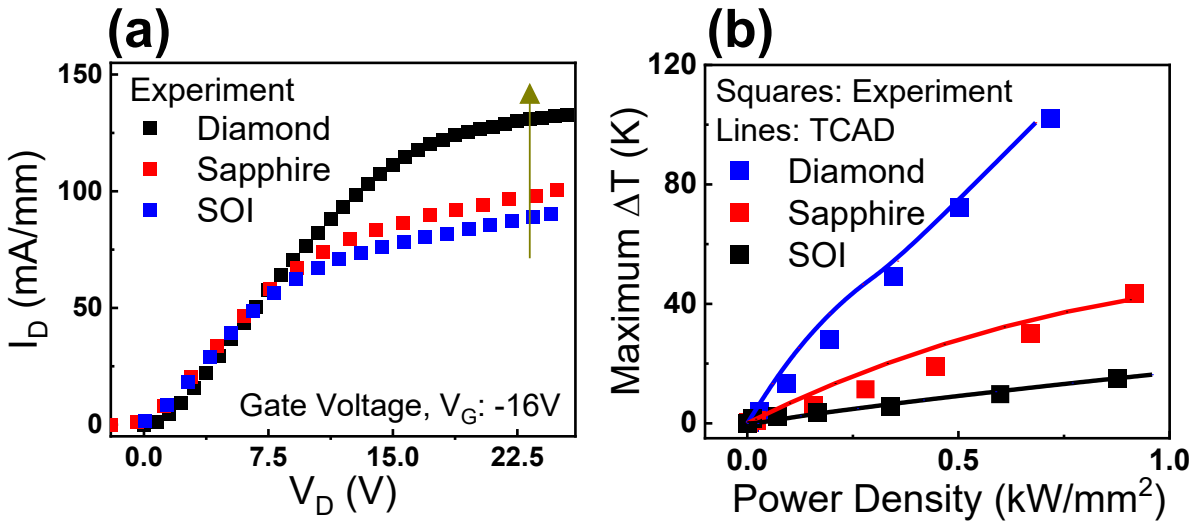



**Figure 6.11.** β-$Ga_2O_3$ FETs on various substrates: (a) Increased current in β-$Ga_2O_3$ FETs as predicted by $I_{max}$ equation (Eq. (6.10)) [102]. (b) Decreased junction temperature, resulting from the use of higher thermal conductivity substrates.

lower rank than other WBG materials due to its low thermal conductivity. The bottleneck of the low thermal conductivity can be alleviated by stacking β-$Ga_2O_3$ on high thermal conductivity substrates. This is achieved by fabricating β-$Ga_2O_3$ FETs on Sapphire and Diamond as shown in Fig. 6.11(a). *As predicted by $I_{max}$, high current is observed at the same gate overdrive for β-$Ga_2O_3$ FETs on Sapphire and Diamond.* This is because of the reduction in junction temperature, as revealed by Thermoreflectance measurements and TCAD validation (Fig. 6.11(b)) [102]. It can be noticed that β-$Ga_2O_3$ on Diamond is predicted to have ∼1.3 times smaller $I_{max}$ compared to GaN and SiC, which is a much more optimistic prediction compared to Keyes' FOM [112]. Therefore, β-$Ga_2O_3$ could be a material of choice for power electronics if appropriate thermal shunts or other cooling systems are employed.

### 6.6.2 Analytical Form of $P_{max}$ Limit (AC)

In a realistic power circuit, power transistors are constantly switching on and off. Fortunately, the substrate- and self-heating-aware expressions obtained in the previous section

can still be used by introducing the transient thermal impedance $Z_m$. At $T_{amb} = 300$ K, by setting $T_{j,max} = 450$ K, $P_{max}$ can be determined using the following relation:

$$P_{max} = \frac{T_{j,max} - T_{amb}}{\theta_{th} \times Z_m(t_{on})} = I_D \times V_D. \tag{6.11}$$

$\theta_{th}$ is the DC thermal resistance, $Z_m(t_{on}) < 1$, is the normalized transient thermal impedance, $t_{on}$ is the pulse duration ($t_{on} = D\ \zeta$, $\zeta$ is the period, $D$ is the duty cycle). If multiple stages of equivalent RC-time constants are considered due to package, submounts, heat sink, PCB, etc., one can write [123], [128]:

$$\begin{aligned} Z_m\left(t_{on}\right) &= D + (1-D)\sum_i \frac{\theta_{th,i}}{\theta_{th,tot}} C_i\left(D,\zeta\right) Z_{0,i}\left(t_{on}\right) \\ \text{with } C_i(D,\zeta) &= \frac{1 - exp\Big(-\frac{(1-D)\zeta}{\tau_{thi}}\Big)}{1 - exp\Big(-\frac{\zeta}{\tau_{thi}}\Big)}. \end{aligned} \tag{6.12}$$

The index $i$ stands for a certain stage of the RC circuit ($i$ =1 is the chip itself), $C_i(D,\ \zeta)$ is a correction function that depends on $\tau_{th}$ of each stage. $Z_{0,i}$ is the transient thermal impedance for a single pulse, expressed as $[1 - exp(-t_{on}/\tau_{th})]$, where $\tau_{th}$ ($\tau_{th} = \theta_{th}C_{th}$) can be calculated by the parameters given in Table 6.4. This is the first closed-form analytical expression for arbitrary complex package structure subjected to pulses of arbitrary duty cycle, which considerably simplifies the calculation of $P_{max}$. In a similar fashion of Fig. 6.10(a), Eqs. (6.11) and (6.12) can be utilized to estimate $P_{max}$ (Fig. 6.12) considering the thermal transient response. Here, $t_{on}$ =10 ms and $D = 0.5$ for a stand-alone device ($i$ =1) are assumed with the same device geometries listed in Table 6.3. As expected, Diamond outperforms others, whereas β-$Ga_2O_3$ FETs still need to be improved to catch up with their GaN and SiC counterparts. For high-frequency operations in hundreds of kilohertz, $Z_{0,i} \sim 0$ for all materials. Therefore, from Eq. (6.12), $Z_m \sim D$. It is worth mentioning that a holistic performance assessment can be made with safe operating area (SOA) [103], which considers $R_{on}$, $I_{max}$, $P_{max}$, and $V_{BD}$.

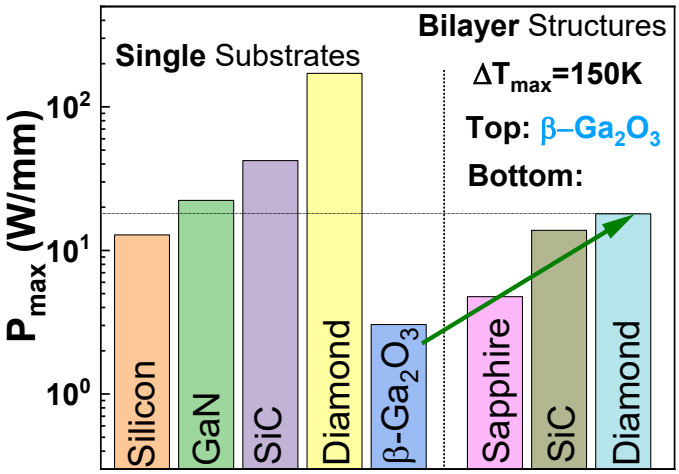



**Figure 6.12.** (a) (Left) $P_{max}$ for WBG materials at $\Delta T_{max}$ =150 K. (Right) β-$Ga_2O_3$ channel layer on various substrates (Sapphire, SiC, Diamond). The performance (e.g., $P_{max}$) can be improved by depositing β-$Ga_2O_3$ on higher thermal conductivity substrates. The arrow indicates increasing performance of β-$Ga_2O_3$ FETs. $t_{on}$ =10 ms and $D = 0.5$ are assumed.

**Table 6.4.** Physical properties of commonly used materials for transient thermal calculations.

| **Material Parameters** | **Si** | **4H-SiC** | **GaN** | **β-$Ga_2O_3$** | **Diamond** |
|---|---|---|---|---|---|
| Specific Heat (J/K g) | 0.7 | 0.69 | 0.49 | 0.49 | 0.52 |
| Density (g/cm$^3$) | 2.33 | 3.1 | 6.15 | 5.95 | 3.52 |
| $C_{th}/W$ (J/K cm $\times 10^{-5}$) | 4.89 | 642 | 904 | 875 | 549 |

## 6.7 Conclusions

In this chapter, we have discussed the importance of the self-heating effect on emerging power electronics. Through the well-calibrated compact model, the performance of the boost converter is limited and not as competitive as SiC and GaN counterparts despite the superior material properties of β-$Ga_2O_3$. By developing a simplified 3D analytical model, the overall thermal resistance of a β-$Ga_2O_3$ FET can be easily estimated and it coincides with the results from COMSOL simulations. From the analytical model, some strategies can be suggested such as the insertion of an interlayer and wafer thinning. This simpler thermal resistance

model can be easily adopted in the new performance metrics of a multilayered structure like β-$Ga_2O_3$ FETs. Finally, the analytical form of $I_{max}$ and $P_{max}$ is obtained and can be used to compare the upper limit of stand-alone device performance (given a maximum temperature) among various materials and bilayered structures. It again confirms that β-$Ga_2O_3$ is still inferior (1.3 times lower) to GaN and SiC in terms of maximum performance even with Diamond substrate to assist the heat dissipation. However, β-$Ga_2O_3$ does have an advantage of lower-cost large-scale epitaxial growth compared to GaN and SiC technologies. Taken together, one anticipates the use of β-$Ga_2O_3$ in niche power-electronics applications.

# 7. OXIDE ELECTRONICS: INDIUM OXIDE

## 7.1 Introduction

There has been a surging interest in integrating thin-film transistors (TFTs), resistors, and memory elements within the metal-insulator back-end-of-line (BEOL) stack for applications in traditional and in-memory computing such as 3D DRAM [129], 3D one transistor-one resistor (1T-1R) RRAM array [130], 3D field-programmable gate array (FPGA) [131]. Another well-known application of TFTs is pixel control in a display, where amorphous-Si (a-Si, with mobility ~1 $cm^2V^{-1}s^{-1}$) and low-temperature polysilicon (LTPS, with mobility ~100 $cm^2V^{-1}s^{-1}$) have been widely used for a long period. Although the low mobility for a-Si, it has advantages in large-area growth for cheaper display. LTPS, fabricated by melting a-Si through Excimer laser annealing (ELA) [132], on the other hand, needs a process temperature of ~550 °C [133], hence it is not a BEOL-compatible transistor. Later on, amorphous oxide semiconductor (AOS) TFTs are of great interest for advanced display applications because of their transparency, higher mobility, and steeper subthreshold slope (SS) compared to amorphous a-Si TFTs [134]. Among those AOSs, amorphous In-Ga-Zn-O (a-IGZO) TFTs, which can be deposited by sputtering [135] or atomic layer deposition (ALD) [136], are widely used in display circuits. The use of compositionally simpler $In_2O_3$ TFTs was hindered by the unstable electrical properties of the films deposited by sputtering (because it forms poly-crystalline films) and the difficulty in operating the transistor in enhancement mode (because oxygen-deficiency makes the film intrinsically n-type) [96].

Fortunately, these persistent challenges have recently been addressed by Si *et al.* with ALD-grown amorphous $In_2O_3$ TFT with the channel thickness of 1.5 to 0.7 nm and the channel length scaled down to 40 nm [137]. These ALD-grown TFTs (process temperature ~225 °C [99]) demonstrate excellent mobility (>100 $cm^2V^{-1}s^{-1}$) [138], low subthreshold slope (65 mV/dec) [139], and tunable threshold voltage ($V_{th}$) between −4 and 5 V [99]. As an enhancement mode TFT, the record high current density of 2.2 A/mm at $V_{DS}$ of 0.7 V was reported [139]. These performance metrics establish $In_2O_3$ TFT as a promising technology for BEOL integration. It remains to be seen, however, if the technology is sufficiently reliable to make this integration practical.

In this chapter[1], we characterize the $V_{th}$ instability of the ultra-thin $In_2O_3$ TFTs with channel thickness of 1.2 nm under positive bias temperature stress (PBTS) and hot carrier degradation (HCD). This specific thickness was chosen due to its fairly good consistency during the reliability test. Other thicknesses may also be worth exploring since their electronic properties might differ. It is well known that PBTS and HCD are the two dominant reliability challenges of this class of thin-film transistors, where negative bias temperature stress (NBTS) should be negligible for N-channel FETs. Given its sub-nm ultra-thin channel, we expect the degradation physics to be substantially different compared to traditional front-end logic transistors (e.g., FinFET) or other thin-film technologies (e.g., a-IGZO TFTs).

## 7.2 Electrical Properties of $In_2O_3$ TFTs

Fig. 7.1(a) shows the schematic of the device under test. It has $Al_2O_3$ (1 nm) and $HfO_2$ (10 nm) as the gate dielectric and 1.2-nm-thick $In_2O_3$ as the channel material. The channel width ($W$) is 11.1 µm, and the channel length ($L_{ch}$) ranges from 10 µm to 2 µm are examined. The fabrication details can be found in Ref. [99]. All the stress/I-V experiments are conducted by Keysight B1500A semiconductor device parameter analyzer. The pre-stress $I_D - V_G$ is confirmed to have a subthreshold slope (SS) of ∼115 mV/dec (at $V_{DS}$ = 1 V), field-effect mobility ($\mu_{FE}$) of 10 $cm^2V^{-1}s^{-1}$ (at $V_{DS}$ = 0.05 V), and $V_{th}$ of ∼2 V (at both $V_{DS}$ = 0.05 V and 1 V, by extrapolation from the linear region of the $I_D - V_G$ curve). The negligible hysteresis in double-sweep mode confirms reliable measurements. The transfer characteristics are provided in Fig. 7.2 for various $L_{ch}$ and at various chuck temperatures ($T$ = 20 to 80 °C at fixed $L_{ch}$ = 10 µm, as an example). It shows that $V_{th}$ decreases as $L_{ch}$ is shortened. On the other hand, the temperature dependence is similar to the classical Si transistors, where both $V_{th}$ and on-current decrease at higher temperatures.

The stress voltages range from $V_G$ = 4 to 6 V, and $V_D$ = 8 to 9 V, for a temperature range of 20 to 80 °C, a typical range of temperatures in self-heated BEOL interconnects [141]. PBTS tests are conducted with source and drain grounded, and the gate contact is biased. The PBTS (HCD) stress is intermittently interrupted by $I_D - V_G$ sweeps at $V_{DS}$ =

[1]↑The content of this chapter is taken from our publication [140].

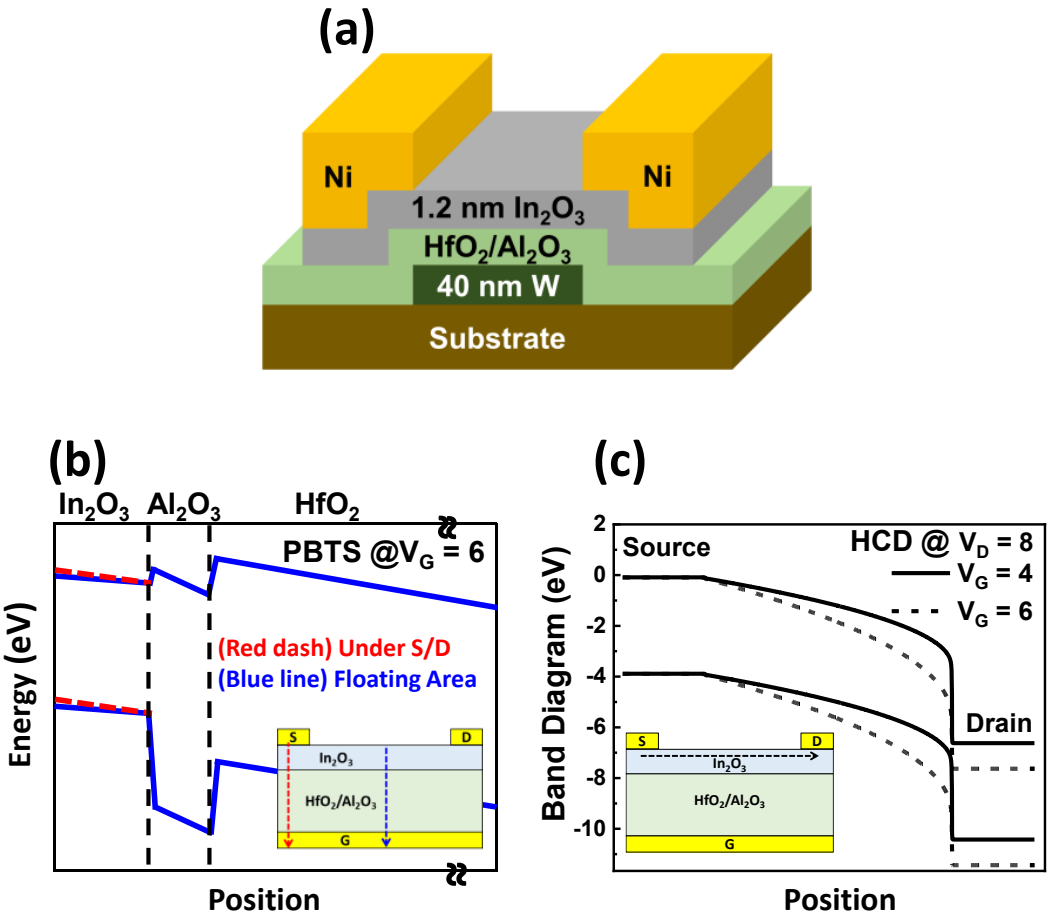



**Figure 7.1.** (a) The schematic of the bottom-gate $In_2O_3$ TFT under study. (b) Band diagram in vertical direction under PBTS along two paths. (c) Band diagram in horizontal direction under HCD tests.

0.05 V (1 V). $V_{th}$ shift ($\Delta V_{th}(t)$) is obtained by the constant current method at 1 nA $\times(W/L)$ in this study. The band diagram under PBTS and HCD, perpendicular and parallel to the channel, are calculated by TCAD simulator Sentaurus$^{TM}$ individually, as shown in Figs. 7.1(b) and 7.1(c). We will see later that the band diagrams are essential to interpret the physical mechanisms related to PBTS and HCD degradation.

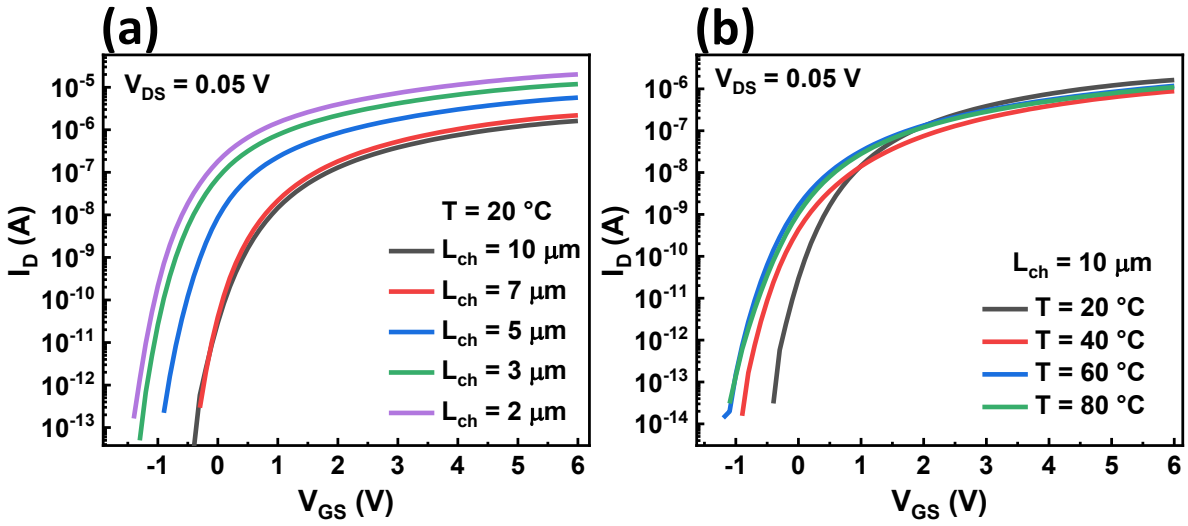



**Figure 7.2.** The pre-stress $I_D - V_G$ curves measured at $V_{DS} = 0.05$ V (a) for various channel lengths and (b) at elevated temperatures.

## 7.3 Reliability Measurements of $In_2O_3$ TFTs

### 7.3.1 Experimental Observations

Fig. 7.3 summarizes $\Delta V_{th}$ results of temperature and field-dependent PBTS (first row, Fig. 7.3(a-b)) and HCD (second row, Fig 7.3(c-d)) on devices with $L_{ch} = 10$ µm. It is noteworthy that, in traditional silicon transistors, $\Delta V_{th}$ due to PBTS is always positive due to electron trapping [142]. However, Fig. 7.3(a) shows that the low-stress degradation ($V_G = 4$, 5 V) in our TFTs are characterized by an anomalous negative-to-positive turn-over in $\Delta V_{th}$, while the high-stress case ($V_G = 6$ V) shows a fast positive shift in the threshold voltage characterized by a logarithmic time-dependent degradation. A similar trend has been reported for a-IGZO TFTs [143]. For a given stress voltage (e.g., $V_G = 6$ V), the temperature-dependent PBTS shown in Fig. 7.3(b) are also characterized by an anomalous positive-to-negative shift in $V_{th}$. Therefore, PBTS-induced $\Delta V_{th}$ in $In_2O_3$ TFTs can be characterized by a two-stage (negative to positive or positive to negative) degradation. This two-stage degradation has also been reported for other TFTs [143]–[146].

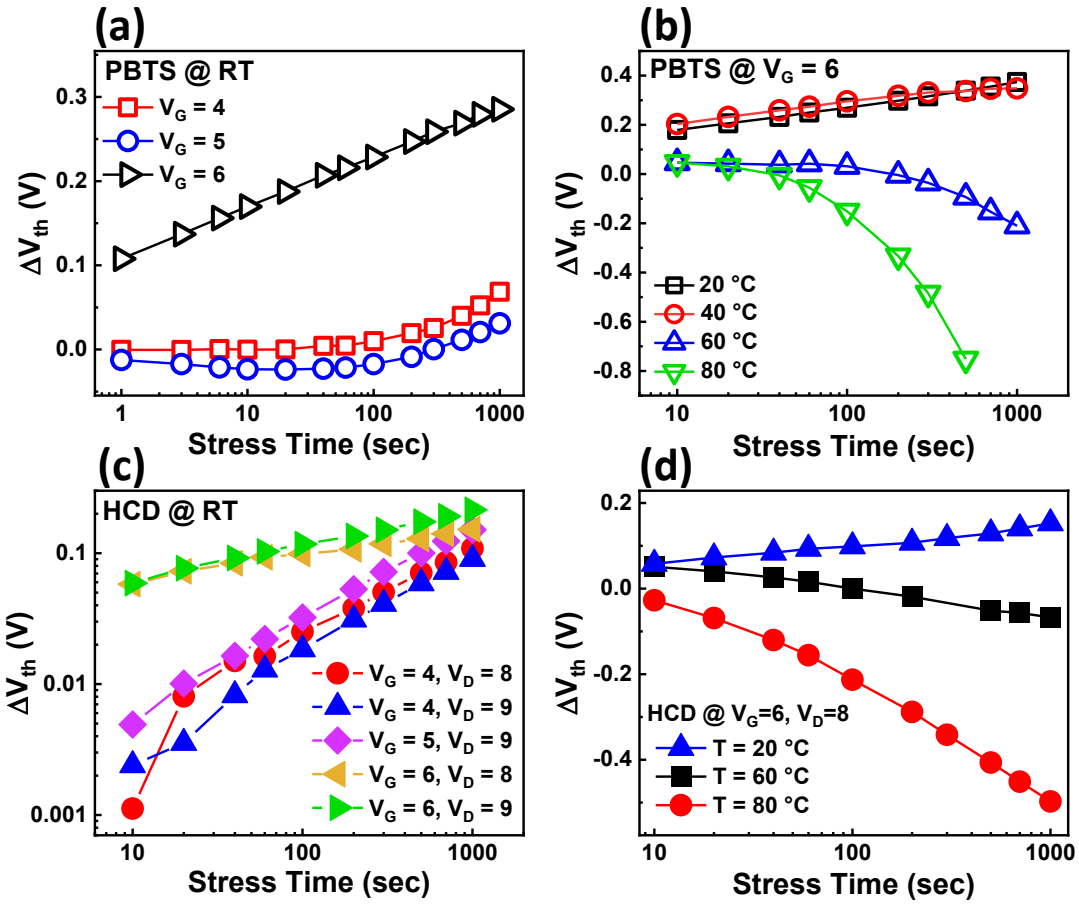



**Figure 7.3.** $\Delta V_{th}(t)$ under various PBTS conditions in semi-log scale at (a) RT and (b) elevated temperatures. $\Delta V_{th}(t)$ under various HCD conditions in log-log scale at (c) room temperature (RT) and (d) elevated temperatures. All results are from devices with $L_{ch} = 10$ µm.

Fig. 7.3(c) shows the corresponding curves for HCD degradation as the TFTs are stressed with different $V_G/V_D$ combinations. Higher $V_G$ stress (6 V) shows a distinct behavior with a higher degradation level at an early stage compared to lower $V_G$ stress (4 and 5 V). This abrupt transition at higher voltage is similar to the PBTS transition at similar gate voltage, as in Fig. 7.3(a). Fig. 7.3(d) reveals that temperature-dependent HCD shows a positive to negative $\Delta V_{th}$ with increasing temperature, similar to that of PBTS. As an aside, this is the first report of the HCD degradation and its correlation to PBTS degradation in BEOL-integrated transistors. The alikeness of the PBTS and HCD voltage and temperature dependence suggests that identical mechanisms may be driving this phenomenon.

### 7.3.2 Theory and Proposed Model

It has been suggested that the two-stage degradation of a-IGZO TFTs may be interpreted by two-component degradation: a positive $\Delta V_{th}$ is attributed to electron trapping at the channel/oxide interface ($N_{it}$) and/or into oxide ($N_{ot}$) [147], [148], and a negative $\Delta V_{th}$ variously correlated to accumulation of positive ions at the semiconductor/oxide interface [149], or formation of the donor-like defect states through the interaction with hydrogen (H) [144], [145], oxygen ($O_2$) [150], or water ($H_2O$) molecule [143], [146]. Our analysis below, however, shows that consistent interpretation of the dataset in Fig. 7.3 is only possible if $\Delta V_{th}$ involves a correlated sum of *three components*, i.e.,

$$\begin{aligned}\Delta V_{th}(t) &\equiv V_{it}^{+}(t) + V_{tr}^{+}(t) - V_{dt}^{-}(t) \\ &= \left[A_{it}t^{n} + B_{tr}\log(\frac{t}{\tau_{tr}})\right] - C_{dt}\left(1 - \mathrm{e}^{-\left(\frac{t}{\tau_{dt}}\right)^{\beta}}\right).\end{aligned} \tag{7.1}$$

where $A_{it}$, $B_{tr}$, $C_{dt}$ are voltage- and temperature-dependent prefactors of interface trap generation, oxide electron trapping, and donor-trap generation, respectively. The corresponding characteristic time-scale factors, $\tau_{tr}$ and $\tau_{dt}$, also depend on voltage and temperature, but power exponent $n$ and $\beta$ are not. The stretched exponential functional form for donor-trap formation is empirical, but the general form and the exponent $\beta$ can be justified physically. We exclude $O_2$ or $H_2O$ as potential sources of degradation because both passivated and unpassivated samples show similar degradations. As proposed in Ref. [144], hydrogen can be released from ALD-grown $Al_2O_3$ [151] and react with react with $O^{2-}$ (in $In_2O_3$ channel), producing $OH^-$ and $e^-$, and creating shallow donor levels at the oxide/semiconductor interface. This negative shift associated with donor traps fully recovers within 24 hours at room temperature (RT), see Fig. 7.4.

Next, we use Eq. (7.1) to fit the experimental data shown in Fig. 7.3 to decouple the components due to interface trap generation, electron-trapping in existing states, and donor-trap formation. Fig. 7.5(a) shows that for high-voltage PBTS ($V_G$ = 6 V) at 40 °C, $\Delta V_{th}(t, \text{high}) \sim V_{tr}^{+}(t) - V_{dt}^{-}(t)$. Here, $V_{tr}^{+} \equiv B_{tr}\log\left(\frac{t}{\tau_{tr}}\right)$, increases rapidly as the increasing vertical electric field exponentially increases the (weakly temperature-dependent) tunneling

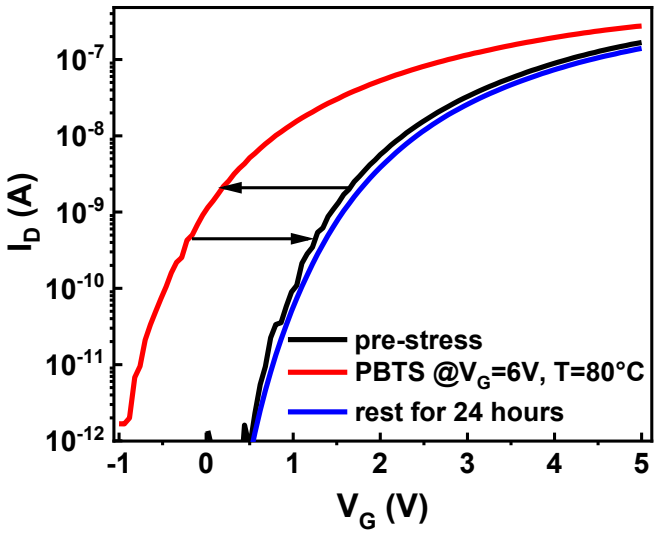



**Figure 7.4.** Pre-stress, post-stress (PBTS: $V_G$ = 6 V, $T$ = 80 °C), and post-recovery $I_D$-$V_G$ curves in atmosphere and room temperature.

current into the oxide. Similar results have been reported in Ref. [147] for a-IGZO TFTs. The negative (donor-trap) contribution, $V_{dt}^{-}(t)$, is relatively small at RT (Fig. 7.5(a), dashed line), but it enhances rapidly (Figs. 7.5(b) and 7.5(c), dashed line) as the temperature rises from 40 to 80 °C. This indicates a *strong field and temperature activation in the donor-trap formation*. It follows the Arrhenius relationship, i.e., $\tau_{dt}(T) = \tau_0 \exp(E_\tau/kT)$ [148], see Fig. 7.6(a), where $E_\tau$ is the average effective energy barrier, and $\ln(\tau_{dt})$ vs. $1/kT$ is plotted. From its linear relationship, $\tau_0$ = 47.2 μs and $E_\tau$ = 0.48 eV are determined, which is close to 0.52 and 0.63 eV reported in Ref. [145]. The coefficient $C_{dt}$ is also found to increase with temperature, which is plotted in Fig. 7.6(b). Arrhenius relationship is again assumed to fit it. One possible reason for the intensified $V_{dt}^{-}$ is the enhanced release of hydrogen atoms from $Al_2O_3$ at a higher $V_G$, given the high hydrogen concentration in low-temperature ALD-grown $Al_2O_3$ [151]. And the elevated temperature accelerates the chemical reaction of creating shallow donor levels. At lower stress voltage ($V_G$ = 4, 5 V), however, reduced vertical field exponentially suppresses $V_{tr}^{+}(t)$, and the interface trap generation $V_{it}^{+}(t)$ dominates long-term degradation. In other words, $\Delta V_{th}(t;\text{low}) \sim V_{it}^{+}(t) - V_{dt}^{-}(t)$.

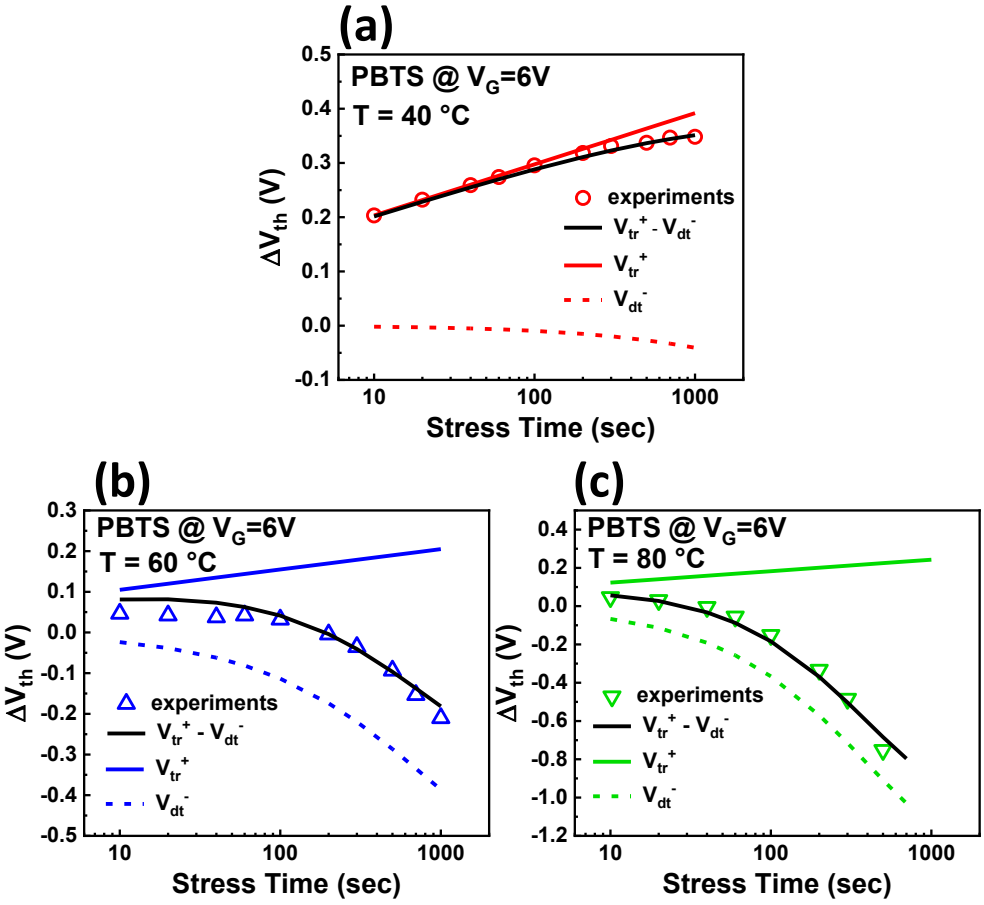



**Figure 7.5.** $\Delta V_{th}$ under PBTS at the temperature of (a) 40 °C (b) 60 °C (c) 80 °C are fitted with the two components shown separately.

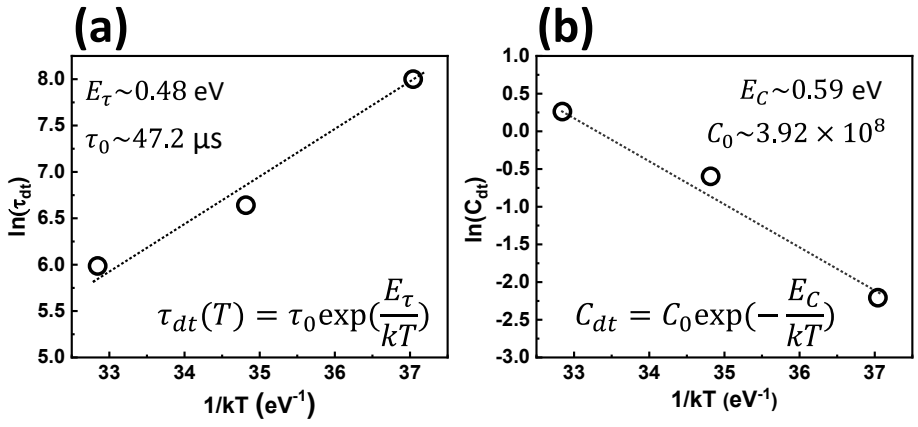



**Figure 7.6.** Arrhenius plots of the extracted parameters: (a) $\tau_{dt}$ and (b) $C_{dt}$.

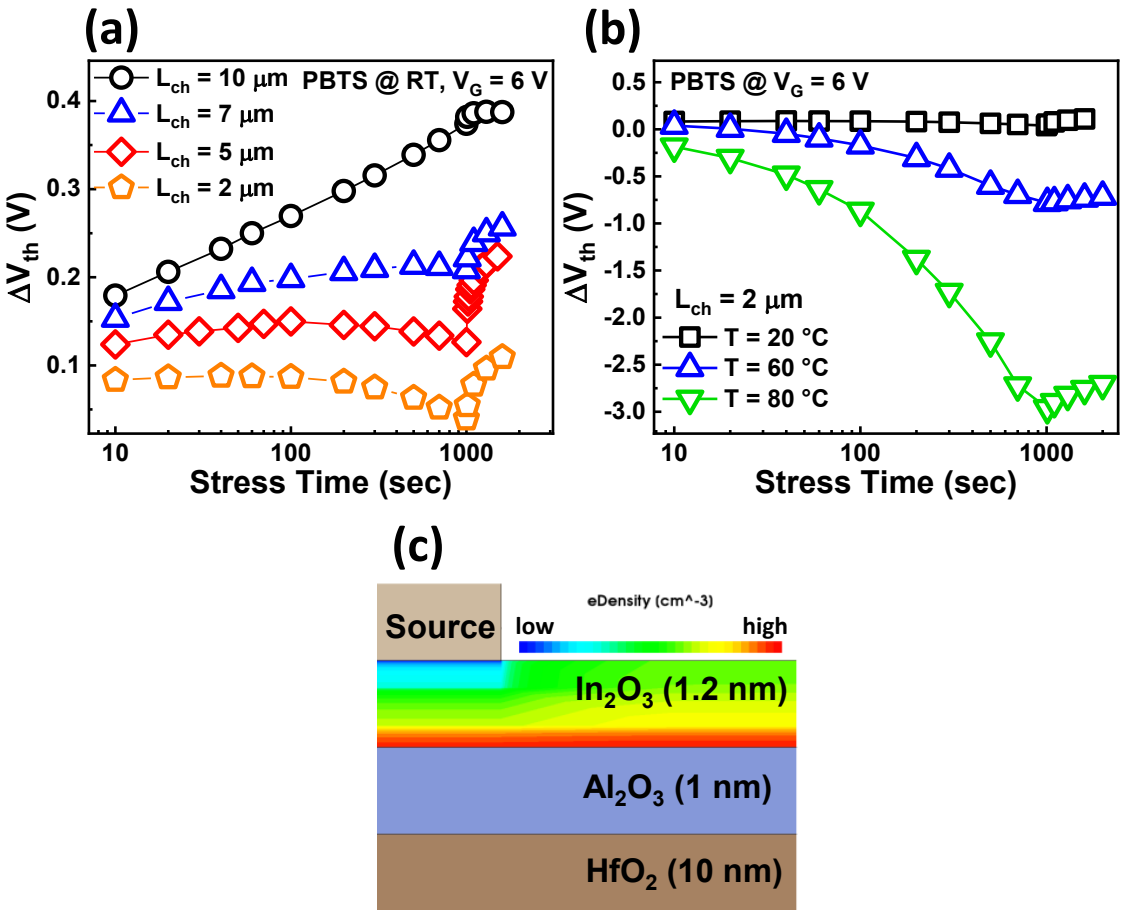



**Figure 7.7.** (a) Channel length ($L_{ch}$)-dependence of $\Delta V_{th}$ under PBTS. (b) PBTS in devices with $L_{ch} = 2$ µm. (c) The electron concentration (eDensity) profile simulated by Sentaurus TCAD.

$In_2O_3$ TFTs with several different channel lengths ($L_{ch}$) are stressed with the same PBTS condition as shown in Fig. 7.7(a). Surprisingly, $V_{dt}^{-}(t)$ term is also enhanced in shorter $L_{ch}$ devices, with enhanced recovery (biased at $V_G = 0$ V) at RT. Moreover, the temperature-activated $V_{dt}^{-}(t)$ in shorter $L_{ch}$ (2 µm was chosen here), as shown in Fig. 7.7(b), is aggravated compared to longer $L_{ch}$. This may be explained by the competition between electron trapping (which may dominate in the floating channel area) and donor-trap formation (under source/drain contact). TCAD simulations are carefully calibrated and are used for further justifications, as shown in Fig. 7.7(c). The source/drain area may have weaker electron trapping due to electron depletion by the grounded source/drain contact; also, the higher

vertical field there induces a more substantial negative shift. On the other hand, the floating channel area has more substantial electron trapping and weaker donor-trap formation; therefore, positive $\Delta V_{th}$ dominates. The area ratio of the source/drain area to the floating channel area determines the overall PBTS degradation behavior. It also explains why there is a stronger negative shift at elevated temperatures and enhanced recovery for shorter $L_{ch}$.

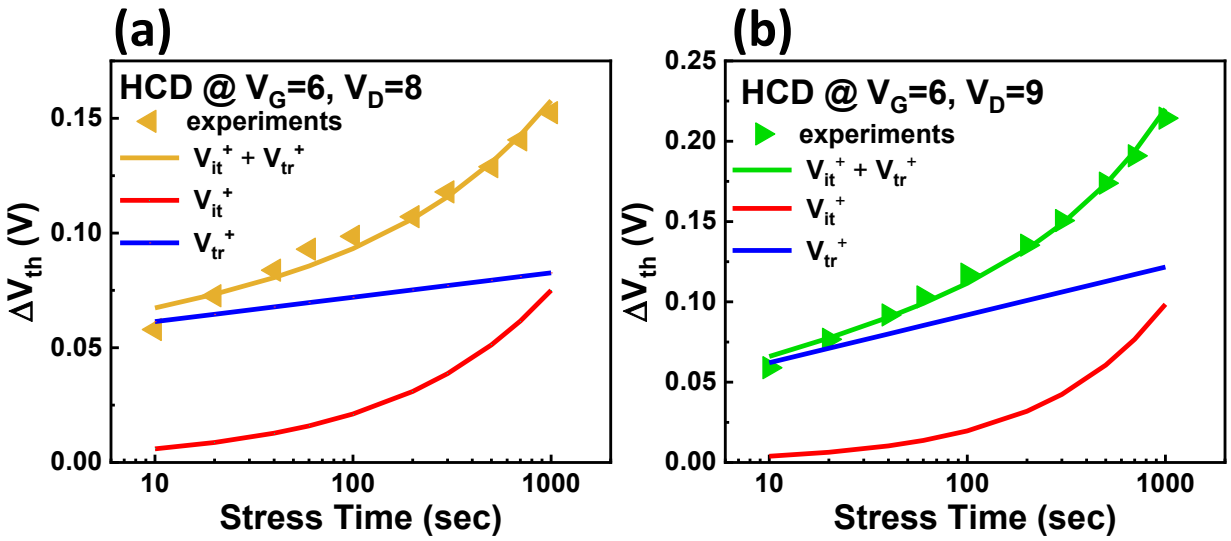



**Figure 7.8.** $\Delta V_{th}(t)$ of HCD at RT with (a) $V_G = 6$, $V_D = 8$ and (b) $V_G = 6$, $V_D = 9$, showing the dominance of PBTS during HCD at RT.

HCD at various $V_G/V_D$ combinations can likewise be interpreted in terms of Eq. (7.1), as shown in Fig. 7.8. Specifically, $\Delta V_{th}(t, \text{high}) \sim V_{it}^{+}(t) + V_{tr}^{+}(t)$ as is typical for traditional MOSFETs [25]. Indeed, at high enough stress $V_G$, PBTS-assisted $V_{tr}^{+}(t)$ dominates. The $V_{dt}^{-}(t)$ component must also exist due to the PBTS-like stress, but is overwhelmed by $V_{it}^{+}(t)$ and $V_{tr}^{+}(t)$ components at RT. In brief, the decompositions demonstrate that Eq. (7.1) describes both PBTS and HCD as various combinations of the three degradation components.

Fig. 7.9(a) shows that the interface trap generation ($\Delta N_{it}$) calculated from decomposed $V_{it}^{+}$ terms ($V_{it}^{+} = q\Delta N_{it}/C_{ox}$) can be characterized by a voltage- and temperature-*independent* time exponent, $n$~0.7. The universality of the time-exponent suggests that although the magnitude of the contribution ($A_{it}$) may be differently accelerated by PBTS vs. HCD, $\Delta N_{it}$ is governed by the same physical mechanism. Equally remarkable, $V_{dt}^{-}(t)$ component is likewise given by a universal function, characterized by the voltage- and temperature-

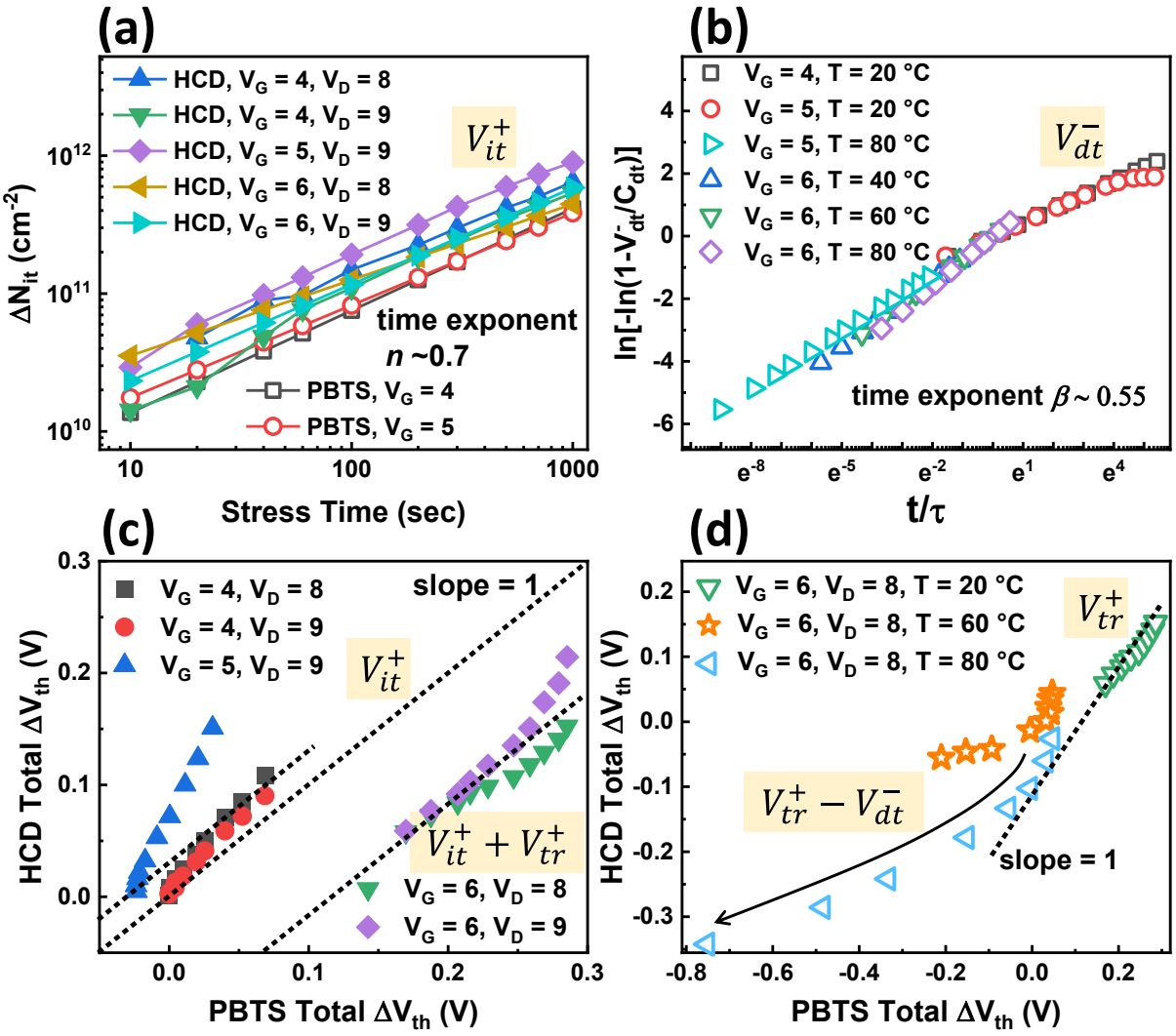



**Figure 7.9.** (a) $\Delta N_{it}$ calculated from decoupled $V_{it}^{+}$ components from both PBTS and HCD tests. (b) Decoupled $V_{dt}^{-}$ components in the Weibull plot. The comparison of total $\Delta V_{th}$ under PBTS and HCD at (c) RT and (d) elevated temperatures. The corresponding components are annotated.

independent exponent ($\beta \sim 0.55$), as demonstrated by the Weibull plot in Fig. 7.9(b). In other words, the mechanics of donor-trap formations, regardless of the microscopic detail, are also universal. Interestingly, other types of TFTs fabricated with very different processes (e.g., sputtering vs. ALD, and top-gate vs. bottom-gate) are also characterized by $\beta = 0.44$ [143], $\beta = 0.66$ [144], and, $\beta = 0.59$ [146] suggesting a common mechanism.

Despite the similarity of the underlying mechanisms, $V_{it}^{+}$, $V_{tr}^{+}$, and $V_{dt}^{-}$ contribute differently to PBTS and HCD. By comparing HCD and PBTS degradation at RT in Fig. 7.9(c), we find that at low voltage and RT, $\Delta V_{th}^{\mathrm{HCD}} \gg \Delta V_{th}^{\mathrm{PBTS}}$. However, at higher $V_G$, the dominance electron-trapping erases the gap, i.e., $\Delta V_{th}^{\mathrm{HCD}} \sim \Delta V_{th}^{\mathrm{PBTS}}$. Consequently, it defines the upper limit of the accelerated HCD test for these TFTs. Finally, Fig. 7.9(d) shows a similar plot at higher temperatures, with a strong non-classical negative shift for both HCD and PBTS. Interestingly, PBTS induces a significantly more negative shift compared to HCD, making it deviate from the line of slope = 1. This is attributed to the higher and uniform vertical field ($E_y \gg E_x$) by strong PBTS, stemming from the *ultra-thin channel relatively to its length: a critical distinction to the classical devices*. From another point of view, the degradation percentage of linear drain current ($I_{D,lin}$, defined at sense $V_G = 4$ V) is plotted with $\Delta V_{th}$ at each data point as Fig. 7.10. At lower $V_G$ stress (= 4 and 5 V), the linear relationship passing the origin means that negligible oxide trapping presents. The degradation is dominated by $\Delta N_{it}$ and channel mobility. However, for $V_G = 6$ V, a finite extrapolated $y$-intercept reveals a fast oxide trapping followed by a larger slope (presumably, $\Delta N_{it}$, but not $\Delta N_{ot}$, causes $\Delta I_{D,lin}$). This coincides with the PBTS behavior mentioned in Fig. 7.3(a).

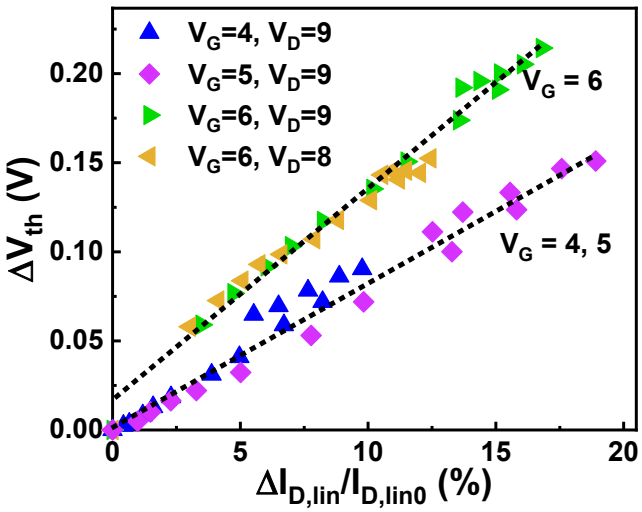



**Figure 7.10.** $\Delta V_{th}$ vs. linear drain current degradation at different stress conditions.

## 7.4 Conclusions

In conclusion, we have examined the reliability of 1.2-nm-thick ALD-grown $In_2O_3$ TFT as a promising BEOL-integrated transistor. We find that, like other AOS TFTs, the two-stage PBTS and HCD degradation can be described by various combinations of three-component degradation (interface trap generation, oxide trapping, and donor-trap formation), as in Eq. (7.1). Also, the time-evolution of the same degradation functions are essentially identical, defined by power exponents ($n$ ~0.7, $\beta$ ~0.55). Compared to other alternatives [143]–[145], [152], our TFTs demonstrate an excellent $V_{th}$ stability at RT under PBTS ( $\Delta V_{th} < 0.4$ V) and HCD ($\Delta V_{th} < 0.3$ V) after 1000 seconds of stress. Their strong/anomalous temperature-dependent $\Delta V_{th}$, related to the donor-trap formation, is an important concern, especially when integrated with traditional transistors with substantial self-heating. Depending on the interconnect level, the temperature difference will reflect a rapid $V_{th}$ divergence. Overcoming the temperature sensitivity by suppressing the hydrogen-assisted donor-trap formation is the key challenge for the wide adoption of BEOL-integrated oxide transistors in modern integrated circuits.

# 8. SUMMARY AND FUTURE WORK

## 8.1 Summary of the Thesis

In this thesis, we look into the reliability issues (HCD, SHE, and PBTI (PBTS)) in several nonclassical power transistors and thin-film transistors, which are made of Si or oxide semiconductors. The underlying mechanisms causing the degradation under stress depend on its materials, doping profiles, and geometries. A big part of the thesis discusses HCD in Si LDMOS transistors with multiple degradation hotspots. The proposed tandem-FET model serves as a critical concept to isolate the degradation in the channel and drift regions. It allows the compact model to be reliability-compatible, which is distinct from the traditional way of LDMOS modeling. Two new characterization techniques: I-V spectroscopy and $S^2$PCP, are implemented and validated through a series of experiments and modeling.

### 8.1.1 Developed New Characterization Tools for Multi-Hotspot Theory

The proposal of I-V spectroscopy demonstrates the fact that the HCD could induce the degradations not only near the drain, as the classical HCD in a MOSFET, but also in the channel region under high gate bias. And the additional degradation spot could also degrade the device driving current, $I_{D,lin}$. In other words, the preexisting approach of data analysis cannot identify the components from the two hotspots. By plotting a series of $I_D - V_G$ curves into the degradation spectrum, the two-peak behavior: one in the subthreshold region and the other one in the super-threshold region, can provide useful information about the degree of each degradation even before starting analyzing it. Those deconvoluted degradation parameters ($\Delta\mu_{ch}$, $\Delta\mu_{dr}$, $\Delta V_{th}^{ch}$) can be obtained either by fitting with the BSIM6-based compact model (more exact) or by solving the derived three-point analytical model (comparable results but much faster). Remarkably, the simple MOSFET equation with square law can represent the more complicated charge-based model like BSIM6 with excellent accuracy. Furthermore, since the two-peak property is confirmed to be universal for various kinds of LDMOS transistors, the three-point analytical model can be easily implemented on other LDMOS given the device geometries and regional mobilities.

Charge pumping is also a widely-used method to extract $N_{it}$ in a classical MOSFET. It was also adopted to probe the spatially-resolved $N_{it}$ with specially designed pulses. However, for a source-body-tied (SBT) transistor, it was never a feasible choice. We first explain the issue of mixed electron and hole current due to the SBT schematic and prove that the common shorted-source-drain connection can induce a double-peak in transient current in classical SPCP measurement. Then, we propose the first charge pumping technique for the SBT-LDMOS called Super Single Pulse Charge Pumping ($S^2$PCP). By floating either the source or the drain terminal with a designed pulse to prevent the inversion of the other region, the region-specific $N_{it}$ can be obtained without the involvement of the other region. This new technique is adopted to characterize the multi-hotspot problem and cross-validates the three-point analytical model. Despite the limitation of the gate size to have a large enough transient current, it can be resolved by averaging a few pulses to ensure a more reliable measurement provided the degradation is hardly recoverable. Moreover, it is also demonstrated in LOCOS-based LDMOS transistors, confirming that the LOCOS region suffers from the highest degree of damage. The edge close to the source side is the root cause of the $\Delta I_{D,lin}$. Finally, the shift of the recombination peak attests that $S^2$PCP is capable of detecting $N_{ot}$ along with $N_{it}$. With the exposure to gamma ray, the controllable amount of $N_{ot}$ can be created and it demonstrates a good correlation between the recombination peak shift and $\Delta V_{th}$. In sum, $S^2$PCP is validated to be a versatile alternative for classical CP and SPCP.

### 8.1.2 AHI-HCD Governs the Multi-Hotspot Theory

Although the channel degradation can be evaluated by the above-mentioned two techniques, the underlying mechanisms are still unknown. To explore the root cause of the hotspot in the channel region, we try to investigate the properties of the channel degradation by its recovery, temperature activation, and gate leakage. We postulate the channel degradation to be HCD-assisted AHI given the faster recovery, negative temperature activation, and insensitivity to temperature in gate leakage. The holes created by the drift HCD may be the driving force of AHI in the channel region owing to the large vertical field in the

channel region. This can also be comprehended by the tandem-FET model under the stress condition of $V_G > V_D/2$. It is the first time to observe that the AHI is correlated with HCD in an LDMOS transistor.

### 8.1.3 β-$Ga_2O_3$ Needs to Overcome Thermal Management Challenges

Apart from Si power transistors, WBG material is the future trend and is still under development. As a fourth-generation semiconductor, β-$Ga_2O_3$ was proposed to be a promising candidate to outperform GaN and SiC due to its high bandgap. However, its practical adoption is hindered by its self-heating effect due to low thermal conductivity. The calibrated compact model reproduces the experimental I-V characteristics well and can be used to estimate its circuit performances such as DC-DC converter, with power efficiency as a deterministic factor. With the $\theta_{th}$ values simulated by COMSOL as inputs, it is observed that as the substrate changes from $SiO_2$/Si, Sapphire, to Diamond, the simulated power efficiency increases up to 85 to 91%. It reveals that there is still a gap for β-$Ga_2O_3$ to compete with GaN and SiC (with an efficiency of 98 to 99%). To have more insights into reducing $\theta_{th}$, we have simplified the 3D $\theta_{th}$ analytical model for multi-layered structures. The model suggests that a heat-spreading layer (e.g., h-BN) between the channel and the substrate, wafter thinning, and a wider device can help to reduce $\theta_{th}$. It can be easily adapted for a fast estimate of $\theta_{th}$ given a structure and a material combination before fabrications. Beyond $\theta_{th}$, we also derived $I_{max}$ and $P_{max}$ so that a stand-alone transistor's performance can also be predicted analytically. By including the $\theta_{th}$ model, temperature-dependent $R_{on}$, and transient thermal impedance $Z$, the performance limit, $I_{max}$ and $P_{max}$ at a maximum allowed temperature, can be calculated. To make a fair comparison, $I_{max}$ and $P_{max}$ are compared among different materials and β-$Ga_2O_3$ on various substrates. As expected, even with a Diamond substrate, β-$Ga_2O_3$ is still inferior to GaN and SiC. This again necessitates the demand to further reduce its $\theta_{th}$ with new techniques or cooling systems.

### 8.1.4 Ultra-Thin $In_2O_3$ TFTs Have Correlated HCD/AHI Reliability Concerns

Another class of oxide semiconductor, a-IGZO, is a famous and commercialized material for TFTs due to its capability of large-area growth and its higher mobility than a-Si. We examine the reliability issues (PBTS and HCD) of the a-$In_2O_3$ TFTs as thin as 1.2 nm grown by ALD. Unlike the classical Si MOSFETs, PBTS and HCD are observed to be correlated when the applied $V_G$ is high. The reason is that it is much smaller in device thickness (∼few nm) compared to its channel length (∼few µm), rendering a much higher vertical field compared to the lateral field. The threshold voltage shift for both PBTS and HCD can hence be modeled by the summation of three terms: interface trap generation ($V_{it}^{+}$), oxide trapping ($V_{tr}^{+}$), and donor-trap formation ($V_{dt}^{-}$). The first two terms increase $V_{th}$ while the third term decreases $V_{th}$. Interestingly, $V_{dt}^{-}$ can be strongly accelerated by high temperature and high gate voltage, which may be stemmed from the reaction of hydrogen (which immigrates from $Al_2O_3$) and $O^{2-}$ (in $In_2O_3$), producing $OH^-$ and $e^-$ and creating shallow donor levels at the oxide/semiconductor interface. This strong negative shift was also reported by other a-IGZO TFTs and could also be caused by $H_2O$ and $O_2$. Therefore, to ensure proper operations of this $In_2O_3$ TFT, the careful passivation and elimination of residual hydrogen in the oxide are crucial in maintaining a relatively small $V_{th}$ variation. Also, this high-performance BEOL-transistor is examined to be very reliable with a relatively small threshold voltage shift under PBTS/HCD stress conditions at room temperature, possibly thanks to its much thinner oxide (higher effective oxide thickness, EOT). Other than a-$In_2O_3$ TFTs, many groups have been exploring the reliability of two-dimensional (2D) materials such as $MOS_2$ transistors [153]–[155]. These next-generation electronics may share similar reliability properties due to the similar geometries.

## 8.2 Future Directions and Recommendations

### 8.2.1 HCD Model of LDMOS Transistors

In terms of HCD in an LDMOS, since there is a great variety of device dimensions and structures, it is hard to develop a unified theory that works for every LDMOS. For

example, we found that an LDMOS with LOCOS is less prone to have huge degradations in the channel region during normal operations, whereas an LDMOS without LOCOS (the devices we investigated in Chapter 2 to 3) tends to have large channel degradations ($\Delta V_{th}$). This may be due to the existence of thick field oxide that decreases the channel field and mitigates the field crowding in the drift region. However, even for the similar structures of LDMOS devices, different technologies, doping profiles employed may also change the field profiles significantly, making it difficult to have precise lifetime estimation. To the best of our knowledge, a real unified and widely recognized HCD model is still absent. Almost all the existing works are phenomenologically developed from the combination of experiments and TCAD simulations. Therefore, it will be a remedy if one can develop a multi-hotspot HCD model, verify it with many different types of LDMOS devices, and embed the model in TCAD simulations.

### 8.2.2 The Need for Innovative Characterization Techniques

$S^2$PCP developed in this thesis is designed for source-body-tied LDMOS. It would be very useful if one can further verify this technique with the same but source-body-opened LDMOS by applying the normal CP technique. Moreover, the energy profiling within the bandgap may also be developed by adjusting the rise/fall time of the pulse. Finally, the multi-frequency charge pumping (MFCP) [68] for oxide bulk traps may also be developed for $S^2$PCP . In this way, $S^2$PCP may become a more mature and standard $N_{it}$ profiling technique.

### 8.2.3 Resolve the Thermal Issues of β-$Ga_2O_3$ FETs

Other than the self-heating issue we discussed in Chapter 6, to reach higher electrical performance, the fabrication process of β-$Ga_2O_3$ FETs requires to be advanced. For example, the contact resistances should be optimized so that the total on-resistance can be further reduced, hence improving the power efficiency of the power circuits. To make it even more competitive to its GaN/SiC counterparts, the fabrication yield should also be improved and should be made as an enhancement mode. Finally, the self-heating issue we addressed in this

thesis should be incorporated into practical circuit/system design. Although Diamond may be the most effective substrate to address the self-heating problem, it is not an affordable solution for mass productions. One should consider a more affordable substrate such as Sapphire along with other cooling systems.

### 8.2.4 Nanometer-Thick $In_2O_3$ TFTs and 2D Electronics

Since we have identified the problem of a strong negative shift of $V_{th}$, the next would be how to mitigate it. One could optimize the fabrication process to reduce the residual hydrogen in the ALD-grown $Al_2O_3$. Also, because of the nm-thick channel, $V_{th}$ can be easily changed by $O_2$ and $H_2O$ adhesion. For a reliable practical operation, it is required to study how to effectively passivate the channel so that less gas adhesion happens to induce $\Delta V_{th}$. Moreover, we studied the reliability issue of TFTs with channel length primarily of 10 µm. Things might be a bit different if channel length shrinks to as short as 40 nm, where the lateral field may not be too small compared to the vertical field. It would be interesting to study the case when the strength of PBTS and HCD are comparable.

Because the transistors made of 2D materials such as $MOS_2$ shares similar dimensions as our ultra-thin $In_2O_3$ TFTs. It would be interesting to investigate if the mixture of HCD/PBTI and the anomalous two-stage degradation are common issues at elevated temperatures. It would be a crucial reliability concern for future next-generation electronics.

## 8.3 Concluding Remarks

In this thesis, we have discussed the reliability issues from Si to emerging WBG materials such as β-$Ga_2O_3$ and $In_2O_3$. The electrical characterizations were carried out, analyzed, and modeled. For the non-classical power transistors like LDMOSs, β-$Ga_2O_3$, and ultra-thin TFTs, their reliability issues need to be reevaluated. The characterization methods proposed in Chapters 2-4 provide different perspectives to address the problem. The HCD-assisted AHI discussed in Chapter 5 brings new insights to understand the multi-hotspot theory. The $I_{max}$ and $P_{max}$ metrics developed in Chapter 6 allow reasonably good performance predictions when designing new structures and materials for WBG transistors. Lastly, the

correlation between HCD and PBTS discussed in Chapter 7 is a unique behavior for nm-thin BEOL-transistors. The conclusion and the modeling method could also lay a foundation for the reliability of emerging 2D transistors. For an integrated system (especially the power electronics components and BEOL transistors), the findings/techniques/theories proposed in this thesis can pave the way for emerging transistor development and solve its potential reliability issues down the road.

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# A. TANDEM-FET LDMOS COMPACT MODEL

The BSIM 6 was downloaded from the website: http://bsim.berkeley.edu/models/bsimbulk/. The version is BSIM-BULK 106.2.0. The predictive technology model (PTM) model card was downloaded from the website: http://ptm.asu.edu/modelcard/2006/130nm_bulk.pm. They were used as inputs to the following HSPICE codes.

## A.1 LDMOS Compact Model: I-V Curve

```
*Tandem-FET Compact Model I-V Measurement
.option abstol=1e-6 reltol=1e-6 post ingold
.hdl "bsimbulk.va" *This is BSIM-bulk file
.include "modelcard.nmos130" *This is the modelcard

* --- parameters ---

.param U0_dr = 50e-3
.param U0_ch = 25e-3
.param Vt_deg = 0e-3

* --- Voltage Sources ---
vds supply  0 dc=0
vgs gate  0 dc=0
vss gnd 0 0

* --- MOS1 ---channel
X1 key gate gnd gnd t1 nmos130 L=0.2e-6 W=35e-6 TOXE=20e-9 CIT=2e
   -4 SHMOD=1 U0=U0_ch VSAT=7e4 RDSW=50 ALPHA0=10 BETA0=29 DELVTO
   =Vt_deg
+ NDEP=1.5E23 IDS0MULT=0.9
* --- MOS2 ---drift
```

```
X2 supply gate key gnd t2 nmos130 L=0.25e-6 W=35e-6 TOXE=20e-9
   CIT=2e-4 SHMOD=1 U0=U0_dr VSAT=6e4 RDSW=100 ALPHA0=10 BETA0=29
    DELVTO=-1
+ NDEP=1E23 IDS0MULT=0.7

* --- DC Analysis ---
.dc vgs 0 6 0.06 sweep vds 1 5 1
.probe dc par'-i(vds)'
*.probe dc par'v(key)'

.end
```

## A.2 LDMOS Compact Model: C-V Curve

```
*Tandem-FET Compact Model Cgg-Vg Measurement
.option abstol=1e-6 reltol=1e-6 post ingold
.hdl "bsimbulk.va"
.include "modelcard.nmos130"

* --- parameters ---

.param U0_ch = 250e-4
.param U0_dr = 500e-4
.param Vt_deg = 0
.param Vac = 0.05

* --- Voltage Sources ---
vds supply 0 dc=0
vgs gate 0 DC= pdcin AC Vac 0
```

```
vss source 0 0

* --- MOS1 ---channel
X1 key gate source source t1 nmos130 L=0.3e-6 W=9.5e-6 TOXE=20e-9
    SHMOD=1 CIT=2e-4 U0=U0_ch VSAT=9e4 RDSW=10 ALPHA0=10 BETA0=29
    NDEP=1e23 DELVTO=Vt_deg IDS0MULT=5.1 VFB=-0.95 ETA0=1e-6

* --- MOS2 ---drift
X2 supply gate key source t2 nmos130 L=0.6e-6 W=10e-6 TOXE=20e-9
   SHMOD=1 CIT=2e-4 U0=U0_dr VSAT=10e4 RDSW=0 ALPHA0=10 BETA0=29
   DELVTO=-0.8
+ NDEP=1E23 IDS0MULT=8.5

.ac lin 2 10k 100k sweep pdcin -4 3.8 0.2
.measure ac cgg find par( '-1 * ii(vgs)/(Vac*hertz*2*3.1415926)'
   ) AT=10000hertz

* --- DC Analysis ---
.dc vgs 0 6 0.06 sweep vds 1 6 1
.probe dc par'-i(vds)'
.print dc par'v(key)'

.end
```

### A.3 The Choice of Peak Point and Valley Point

In most of the LDMOS transistors (with or without the field oxide) discussed in the literature, the peak (P) and the valley (V) points are always present in the I-V spectroscopy. In the subthreshold region, $\Delta I_D$ is contributed by the channel region (both $\Delta\mu_{ch}$ and $\Delta V_{th}^{ch}$).

When the chosen $V_G$ becomes closer to $V_{th}^{ch}$(= 1 V, in this case), the subthreshold current equation that we assumed in the derivation may not be as accurate, and the unwanted component ($\Delta\mu_{dr}$) starts to rise. The P point will be the suitable choice since it stands well below $V_{th}$ and is also easy to identify. The V point is also always present because it is the crossover point of $\Delta\mu_{ch}$ (blue) and $\Delta V_{th}^{ch}$ (green) (See Fig. 3.2). We pick V point to be 0.1 V above $\Delta V_{th}^{ch}$ so that $V_G - V_{th}^{ch} = V_D = 0.1$, which is the minimum $V_G$ where both regions will be in the linear region, and the derived model is valid. Fig. A.1 shows that as the chosen valley moves farther from 1.1 V, the extracted values deviate more from the compact model results.

However, it may be true that there may not be a need to fix P at the peak and V in the valley. If in some devices, the P and the V points are not easily distinguishable, any point in the subthreshold region can serve as P, and any point close to $V_{th}^{ch}$ can be chosen as the V point to perform the analysis (but closer to $V_{th}^{ch}$, better the results, as shown in Fig. A.1). The V point of 1.1 V will have the most accurate results compared to BSIM6.

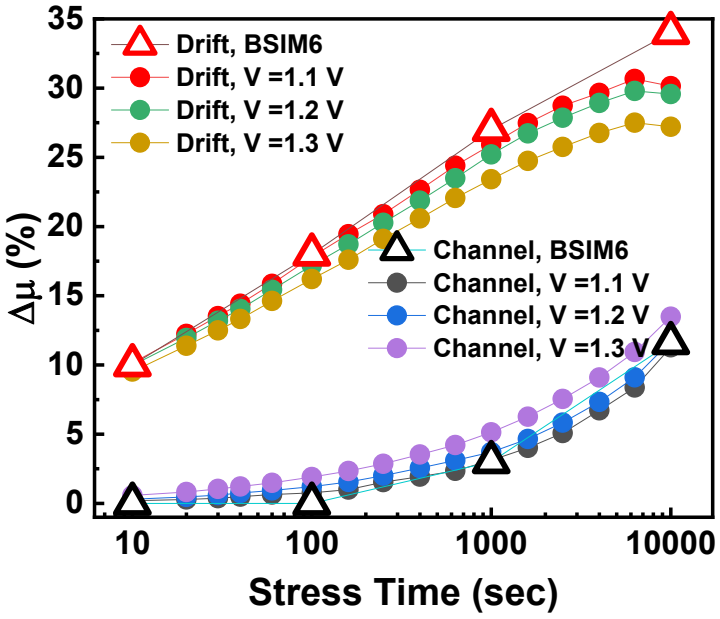


**Figure A.1.** The impact of the choice of valley point (solid circle) on the accuracy of the simplified analytical model (stress $V_G/V_D$ = 2 V/8 V, as an example). The results from BSIM6 (hollow triangle) are also shown for comparisons.

# B. S$^2$PCP MEASUREMENTS

The Matlab code as an input to B1500A Semiconductor Device Parameter Analyzer was provided here for the double-step and single-step pulse generations.

## B.1 Double-Step Pulse Generation: Matlab Code

```
clc; clear all;
points = 2001;  % trise=1us, points = 8001; others use 2001;
VL = -1;
VM = 0;
VH = 2;
ramp_rate = 0.05*1e6; % in unit: V/s

resol = 0.2*1e-6;  % trise=1us, resol = 0.025*1e-6, others resol
   =0.1*1e-6
t_delay = 100*resol;
t_middle = 300*resol;
t_total = 2000*resol;

% Some important parameters that can be adjusted
t_rise = (VH-VL)/ramp_rate;
t_fall = t_rise;
t_on = 300*resol;
t_off = t_total - t_rise -t_fall - t_on - t_delay - 2*t_middle;

M = (VM-VL)/(VH-VL);  % it indicate where is the middle step
% Start filling the vector
Time_Volt = zeros(points,2);
% Fill in time
```

```
for i=1:points
    Time_Volt(i,1) = (i-1)*resol;
end
% Fill in voltage:VL
for i=1:1+t_delay/resol
    Time_Volt(i,2) = VL;
end
% Fill in voltage:VL to -1V
k=1;
for i=2+t_delay/resol:1+t_delay/resol+M*t_rise/resol
    Time_Volt(i,2) = VL+k*resol*ramp_rate;
    k=k+1;
end
% Fill in voltage:keep -1V
for i=int32(2+t_delay/resol+M*t_rise/resol):1+t_delay/resol+M*
   t_rise/resol+t_middle/resol
    Time_Volt(i,2) = VM;
end
% Fill in voltage:-1V to VH
k=1;
for i=2+t_delay/resol+M*t_rise/resol+t_middle/resol:1+t_delay/
   resol+t_rise/resol+t_middle/resol
    Time_Volt(i,2) = VM+k*resol*ramp_rate;
    k=k+1;
end
% Fill in voltage:keep VH
for i=int32(2+(t_delay+t_rise+t_middle)/resol):int32(1+(t_delay+
   t_rise+t_middle+t_on)/resol)
    Time_Volt(i,2) = VH;
```

```
end
% Fill in voltage:VH to -1V
k=1;
for i=int32(2+(t_delay+t_rise+t_middle+t_on)/resol):int32(1+(
   t_delay+t_rise+t_middle+t_on+(1-M)*t_fall)/resol)
    Time_Volt(i,2) = VH-k*resol*ramp_rate;
    k=k+1;
end
% Fill in voltage:keep -1V
for i=int32(2+(t_delay+t_rise+t_middle+t_on+(1-M)*t_fall)/resol):
   int32(1+(t_delay+t_rise+t_middle+t_on+(1-M)*t_fall+t_middle)/
   resol)
    Time_Volt(i,2) = VM;
end
% Fill in voltage:-1 to VL
k=1;
for i=int32(2+(t_delay+t_rise+t_middle+t_on+(1-M)*t_fall+t_middle
   )/resol):int32(1+(t_delay+t_rise+t_middle+t_on+t_fall+t_middle
   )/resol)
    Time_Volt(i,2) = VM-k*resol*ramp_rate;
    k=k+1;
end
% Fill in voltage:keep VL
for i=int32(2+(t_delay+t_rise+t_fall+2*t_middle+t_on)/resol):
   points
    Time_Volt(i,2) = VL;
end
```

## B.2 Single-Step Pulse Generation: Matlab Code

```
clc; clear all;
points = 2001;
VL = -4.5;
VH = -1;
ramp_rate = 0.05*1e6; % in unit: V/s

resol = 0.2*1e-6;  % 0.2us
t_total = 2000*resol;

t_delay = 30*resol;
% Some important parameters that can be adjusted
t_rise = (VH-VL)/ramp_rate;
t_fall = t_rise;
t_on = 500*resol;
t_off = t_total - t_rise -t_fall - t_on - t_delay;


% Start filling the vector
Time_Volt = zeros(points,2);
k=1;
for i=1:points
    Time_Volt(i+1,1) = (i-1)*resol+1; %+1 is to keep VL for 1 sec
end
for i=1:1+t_delay/resol
    Time_Volt(i,2) = VL;
end
for i=2+t_delay/resol:1+t_delay/resol+t_rise/resol
    Time_Volt(i,2) = VL+k*resol*ramp_rate;
```

```
    k=k+1;
end
for i=int32(2+t_delay/resol+t_rise/resol):int32(1+t_delay/resol+
   t_rise/resol+t_on/resol)
    Time_Volt(i,2) = VH;
end
k=1;
for i=2+t_delay/resol+t_rise/resol+t_on/resol:1+t_delay/resol+
   t_rise/resol+t_on/resol+t_fall/resol
    Time_Volt(i,2) = VH-k*resol*ramp_rate;
    k=k+1;
end
for i=2+t_delay/resol+t_rise/resol+t_on/resol+t_fall/resol:points
   +1
    Time_Volt(i,2) = VL;
end
```

# C. BOOST CONVERTER WITH β-GALLIUM OXIDE FETS: HSPICE SIMULATIONS

The MIT Virtual Source GaN HEMT-High Voltage (MVSG-HV) was downloaded from the website and used here as an input: https://nanohub.org/publications/73/1. The boost converter HSPICE code is provided here.

```
.option abstol=1e-6 reltol=1e-6 post ingold
.HDL "MVSGHV_1_0_0.va" *Include MIT Virtual Source GaN HEMT-High
   Voltage (MVSG-HV) code

* --- Voltage Sources ---
V2 3 0 PULSE(-10 5 0 0 0 4u 10u)
V1 1 0 DC=15V

* --- Transistor ---
X1 2 3 0 0 mvsg l=1 lgs=2.75 lgd=2.75 w=3k vto=-4 cg=2e-3 mu0=3e
   -3 ss=0.47
+rcs=4e-2 rcd=4e-2 rsh=200 rth=1000

* --- circuit ---
L1 1 2 400u
R1 4 0 1k
D1 2 4 diode1
C2 4 0 10u

.param Ro=0.5k

.model diode1 D level=1 IS=1e-14 CJO=1e-12 M=.5 TT=3e-11 VJ=.783

```

```
* --- Transient Analysis ---
.Tran   1u  40m
.probe tran Pout=par'v(4)*v(4)/Ro'
.probe tran Pin=par'v(1)*i(L1)'

.probe tran par'i(L1)-i(D1)'
.probe tran par'i(L1)'
.probe tran par'i(C2)'
.probe tran par'i(R1)'
.probe tran par'i(D1)'
.print tran X1:tsh

.end
```

# VITA

Yen-Pu Chen was born in Chiayi city, Taiwan in 1991. He received the B.S. degree in electrophysics from National Chiao Tung University, Hsinchu (NCTU), Taiwan, in 2013, and the M.S. degree in electronic engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2015. He started pursuing his Ph.D. degree in Electrical and Computer Engineering (ECE) at Purdue University, West Lafayette, Indiana, USA and officially joined the research group led by Professor Muhammad Ashraful Alam (Alam CEED group) in January 2017. He is expected to earn his Ph.D. degree in December 2021. His research topics are mainly on electrical characterizations, reliability tests, and device/circuit modeling for logic, thin-film, and power transistors. The reliability issues he has been working on are hot carrier degradation (HCD), self-heating effect (SHE), time-dependent dielectric breakdown (TDDB), and positive bias temperature instability (PBTI).