SELF-HEATING EFFECT ALLEVIATION FOR POST-MOORE ERA CHANNEL MATERIALS

by

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Dedicated to Meng-Ling and my parents

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SYMBOLS

A_s	Surface area
C_{ox}	Oxide capacitance per unit area
C_p	Specific heat
D	Diameter
F	Outward heat flux
g_m, G	Transconductance
h	Heat transfer coefficient
I_{BC}	Breakdown current
I_D, I_{DS}, I_{ds}	Drain current
I_G	Gate leakage current
I_{max}	Maximum current
I_{on}	On current
I_{off}	Off current
κ	Thermal conductivity
k	Dielectric constant
L_{ch}	Channel length
μ_e	Effective mobility in linear regime
μ_0	Intrinsic mobility
μ_{FE}	Field-effect mobility
R_C	Contact resistance
ρ	Mass density
R_{sh}	Sheet resistance
R_{total}	Total resistance
t_{delay}	Delaying time
t_{fall}	Falling time
t_{meas}	Measuring time
t_{pulse}	Pulse width
t_{rise}	Rising time
T	Period

T_a	Ambient temperature
τ	Time constant
T(t)	Temperature at time *t*
T_{ch}	Channel thickness
θ	Mobility attenuation coefficient
θ_c	Mobility attenuation factor from the contact
θ_{ch}	Mobility attenuation factor from the channel
V	Volume
V_{BG}	Back-gate-to-source bias voltage
V_D, V_{DS}, V_{ds}	Drain-to-source bias voltage
$V_{D,\,max}$	Maximum drain-to-source bias voltage
V_G, V_{GS}, V_g	Gate-to-source bias voltage
V_{max}	Maximum voltage
V_T, V_{th}	Threshold voltage
W_{ch}	Channel width

ABBREVIATIONS

1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
AFM	Atomic force microscope
ALD	Atomic layer deposition
BEOL	Back-end-of-line
BG	Back-gate
BN	Boron nitride
BNNT	Boron nitride nanotube
BOE	Buffered oxide etchant
BP	Black phosphorus
CNT	Carbon nanotube
CVD	Chemical vapor deposition
DC	Direct current
DFT	Density functional theory
DI	De-ionized
EBL	Electron-beam lithography
EDS, EDX	Energy-dispersive X-ray spectroscopy
FET	Field-effect transistor
FFT	Fast Fourier transform
GVT	Growth vapor trapping
HAADF	High-angle annular dark-field
h-BN	Hexagonal boron nitride
HOPG	Highly oriented pyrolytic graphite
HRTEM	High-resolution transmission electron microscope
IC	Integrated circuit
ID	Inner diameter
LPE	Liquid-phase exfoliation
MIS	Metal-insulator-semiconductor

MS	Metal-semiconductor
MWCNT	Multi-walled carbon nanotube
NW	Nanowire
PLD	Pulsed laser deposition
PMMA	Polymethyl methacrylate
PVP	Polyvinylpyrrolidone
PVT	Physical vapor transport
RTA	Rapid thermal annealing
SAED	Selected area electron diffraction
SEM	Scanning electron microscope
SHE	Self-heating effect
SS	Subthreshold swing
STEM	Scanning transmission electron microscope
SWCNT	Single-walled carbon nanotube
TDMAHf	Tetrakis(dimethylamido)hafnium(IV)
TEM	Transmission electron microscope
TG	Top-gate
TLM	Transfer length method
TMD	Transition metal dichalcogenide
TMIn	Trimethylindium
TR	Thermo-reflectance
vdW	van der Waals
vdWE	van der Waals epitaxy
YFM	Y-function method

NOMENCLATURE

$[(CH_3)_2N]_4Hf$	Tetrakis(dimethylamido)hafnium(IV)
Al_2O_3	Aluminum oxide
Ar	Argon
Au	Gold
B	Boron
BN	Boron nitride
CdS	Cadmium sulfide
CdTe	Cadmium telluride
$CuInP_2S_6$	Copper indium thiophosphate
FeO	Iron(II) oxide
GaN	Gallium nitride
Ge	Germanium
HfO_2	Hafnium oxide
I_2	Iodine
$In(CH_3)_3$	Trimethylindium
In_2O_3	Indium oxide
In_2Se_3	Indium selenide
InAs	Indium arsenide
InP	Indium phosphide
MgO	Magnesium oxide
$MgCl_2$	Magnesium chloride
Mo	Molybdenum
MoS_2	Molybdenum disulfide
$MoSe_2$	Molybdenum diselenide
$MoTe_2$	Molybdenum ditelluride
N_2H_4	Hydrazine hydrate
Na_2TeO_3	Sodium tellurite
NaOH	Sodium hydroxide
NH_3	Ammonia

Ni	Nickel
$NiGe_2$	Nickel germanide
PbSe	Lead selenide
S	Sulfur
Se	Selenium
SF_6	Sulfur hexafluoride
Si	Silicon
SiO_2	Silicon dioxide
SnO_2	Tin(IV) oxide
$TaSe_3$	Tantalum triselenide
Te	Tellurium
W	Tungsten
WS_2	Tungsten disulfide
WSe_2	Tungsten diselenide
ZnO	Zinc oxide
$ZrTe_3$	Zirconium tritelluride

ABSTRACT

As the miniaturization of the transistors in integrated circuits approaches the atomic scale limit, novel materials with exceptional performance are desired. Moreover, to conduct enough current with an ultrathin and small-scale body, high drain current density is preferably required. Nevertheless, devices may suffer seriously from self-heating effect (SHE) with high drain bias and current if the generated heat cannot be dissipated efficiently. In this thesis, we introduce two material systems and several techniques to accomplish the demand without SHE. Tellurium, as a van der Waals material composed by atomic helical chains, is able to realize its one-dimensional structure. We illustrate that the cross-sectional current density of 150 MA/cm^2 is achieved through boron nitride nanotube (BNNT) encapsulation without SHE due to the superior thermal conductivity of BN. With the nanotube encapsulation technique applied, one-dimensional tellurium nanowire transistors with diameter down to 2 nm are realized as well, and single tellurium atomic chain is isolated. Furthermore, atomic-layer-deposited indium oxide (In_2O_3) as thin-film transistors exhibit even better current carrying capacity. Through co-optimization of their electrical and thermal performance, drain current up to 4.3 mA/μm is achieved with a 1.9-nm-thick body without SHE. The alleviation of SHE is due to a) the high thermal conductivity of the substrate assisting on efficiently dissipating the generated thermal energy, b) SHE avoidance with short-pulse measurement, and c) interface engineering between the channel stack and the substrate. These two material systems may be the solid solution to the desire of high current density transistors in the post-Moore era.

1. INTRODUCTION

1.1 Overview

1.1.1 Motivations

Transistors are the working unit on an integrated circuit (IC) which is the operational center and one of the most important components of our cellphones and laptops. To make these electronic devices achieve better performance and more efficient task processing capability, more transistors are required to be integrated together per unit area. That is to say, efforts are made to increase the transistor density by miniaturizing their physical size as the well-known Moore's Law [1] predicted. In the recent years, the leading semiconductor corporations dedicate themselves to developing 7-nm, 5-nm, even 3-nm technology nodes. However, this trend cannot be eternal since not only it is approaching the atomic scale limit but we are losing electrostatic control so that the transistors can hardly be turned off. Moreover, as we downsize the transistor dimension, it requires higher current density to conduct enough current. Therefore, material candidates which can plausibly be considered in the post-silicon era beyond Moore's Law are widely investigated.

In this chapter, some of these potential materials including graphene, transition metal dichalcogenide (TMD), black phosphorus (BP), tellurium (Te), and indium oxide (In_2O_3) will be discussed. More details will be covered with the last two since they are more comprising in many aspects. At the last part of this chapter, self-heating effect (SHE) will be introduced as a challenge of employing In_2O_3 as the channel material in high-current transistor applications.

1.1.2 Graphene

Graphene is few layers or even one layer of graphite possessing a layered structure where has van der Waals interaction between layers and sp^2-hybrized covalent bonds within a single layer. Mechanical exfoliation method can be applied as the van der Waals interaction is much weaker than covalent bonds, and it turns out that graphene became the first 2D material that realized single layer structure.

Since the discovery of graphene in 2004, global attention has been attracted due to its superb properties [2]–[5]. Monolayer graphene, as a semi-metallic 2D material, exhibits extremely

high mobility of 2.5×10^5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature [6]. The electric transport of graphene is governed by Dirac's relativistic equation since its charge carriers are massless Dirac fermions [7]. On the other hand, despite of the excellent physical properties of graphene, the lack of bandgap appears as a crucial fundamental challenge in its electronic applications. Without a bandgap, graphene has poor electrostatic control. Consequently, more attention was attracted by another layered 2D material family, TMDs, to overcome the downside and further explore the transistor technology.

1.1.3 Transition Metal Dichalcogenides

The TMD family, including molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), molybdenum ditelluride ($MoTe_2$), tungsten disulfide (WS_2), tungsten diselenide (WSe_2), and more, is a group of materials which share similar chemical formula of MX_2 where M represents transition metal such as molybdenum (Mo), tungsten (W) and X stands for chalcogen such as sulfur (S), selenium (Se), and tellurium (Te). Typically, a single layer of TMD consists of one layer of transition metal atoms sandwiched and covalently bonded by two layers of chalcogen atoms. As alternative layered 2D materials, they are widely studied after graphene especially on their electrical properties and applications [8]–[12].

The first realization of transistors based on TMDs can be tracked back to 2007 where molybdenum disulfide (MoS_2) was employed [8]. MoS_2 has an indirect bandgap of 1.2 eV in the bulk form and a direct bandgap of 1.8 eV in monolayers [13]. The existence of bandgap makes the TMD material system fundamentally different from graphene and able to be applied to a variety of fields including field-effect transistors, integrated circuits, and photonic detectors [10], [12], [14]–[16]. Decent device performance of MoS_2 transistors was accordingly reported: drain current being as high as several hundred mA/mm, ON–OFF current ratio being up to over 8 orders of magnitude, and subthreshold swing (SS) down to 74 mV/dec [9], [17], [18].

Nevertheless, a serious drawback of TMDs is that the carrier mobility is reasonably low mainly due to the large effective mass of carriers, which restrains this material system on competitiveness with some other 2D material possessing at least one order higher of mobility such as black phosphorus (BP) and tellurium.

1.1.4 Black Phosphorus

Black phosphorus (BP) is an elemental material with layered 2D structure similar to graphene and TMDs. The realization of single layer BP and its transport behavior was reported in 2014 through mechanical exfoliation technique [19], [20]. BP has a narrower bandgap (0.3 eV in bulk form) and reveals much higher hole mobility up to approximately 300 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [19].

In spite of the excellent transport properties and application potentials of BP, the instability of phosphorene (few-layer BP) turns out to be a significant drawback in terms of realistic applications. It was reported that the electrical performance of BP field-effect transistor (FET) starts to degrade in tens of minutes upon exposure in ambient environment due to its strong affinity for moisture [21]. In order to further explore new electronic materials for beyond Moore's law device applications, researchers are looking for other novel material systems which master all the aforementioned downsides.

1.2 Tellurium

1.2.1 Introduction to Tellurium

Tellurium (Te) is a chalcogen group-VI element and well known as low-dimensional and anisotropic elemental semiconductor materials. It presents attracting properties including piezoelectricity [22]–[24], photoconductivity [25], and thermoelectricity [26], [27]. Besides, Te has a small band gap (0.35 eV in bulk form) under room temperature and performs exceptionally high field-effect mobility (around 10^3 $cm^2 \cdot V^{-1} \cdot s^{-1}$) [28], which makes it more intriguing for electronic applications. Moreover, unlike graphene which has zero bandgap, TMDs which show relatively low carrier mobilities, and BP which is unstable in ambient environment, Te is free of these drawbacks and therefore becoming a more promising nanomaterials showing strong potential in electric applications.

Despite of the outstanding physical properties, synthesis method of high-quality thin films and nanowires are rarely reported. In recent years, we proposed a solution-based and substrate-free strategy of growing 2D Te (tellurene) [28] and a physical vapor transport method with nanotube encapsulation of synthesizing controllable number of atomic Te chains [29]. These steady synthetic methods of tellurene and Te nanowires (NWs) provide reliable access to the

materials and broaden the way to studying its intrinsic physical properties and developing technological applications. More details will be introduced in chapter 2.

In the atomic structure of crystalline, Te as a chalcogen has a one-dimensional (1D) spiral chain structure. Figure 1.1(a) and 1.1(b) show the atomic structure of the top-view and side-view of Te lattice, respectively. Each tellurium atom is covalently bonded with the two nearest adjacent atoms along the *c*-axis forming helical chain structure, and different chains stack with each other by van der Waals force forming a hexagonal crystal structure on the projection of basal plane.

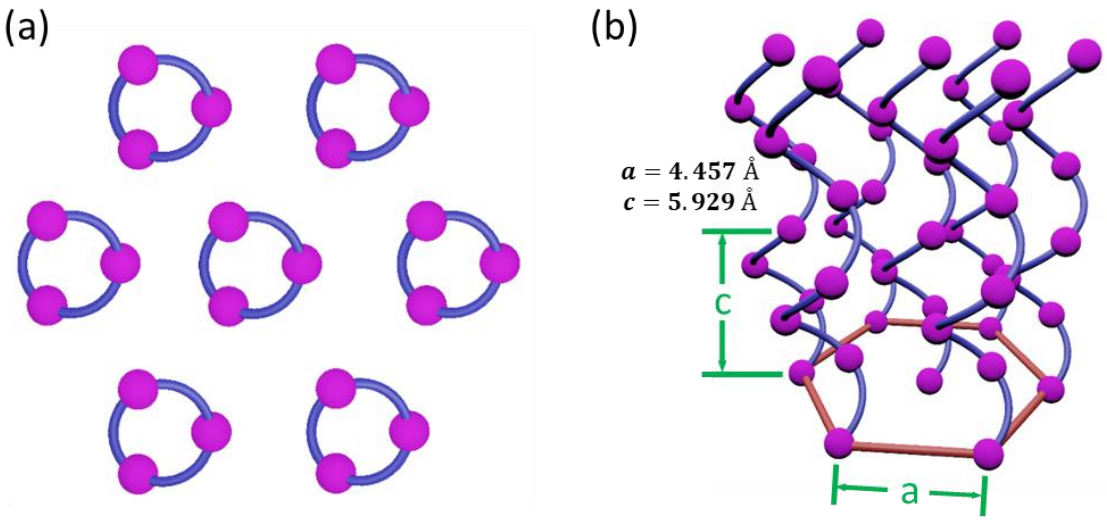

Figure 1.1. Schematic illustration of the atomic structure of tellurium. (a) Top view and (b) side view of a hexagonal crystal structure.

As a powerful nondestructive characterization tool, Raman spectroscopy has been widely used to investigate material properties and layer-to-layer even chain-to-chain interactions, through lattice vibrations [30]. Figure 1.2(a) illustrates the vibration pattern of Raman modes. The A_1 mode is caused by the chain expansion where each atom moves in the basal plane, whereas the E_1 and E_2 modes represent the bond-bending and bond-stretching with larger admixture, respectively [31]. Figure 1.2(b) exhibits a typical Raman spectroscopy of bulk Te crystal with three first-order Raman active modes E_1, A_1, and E_2 located at 92 cm^{-1}, 123 cm^{-1} and 140 cm^{-1}, respectively, which experimental results are in great agreement with theoretical analysis [31], [32].

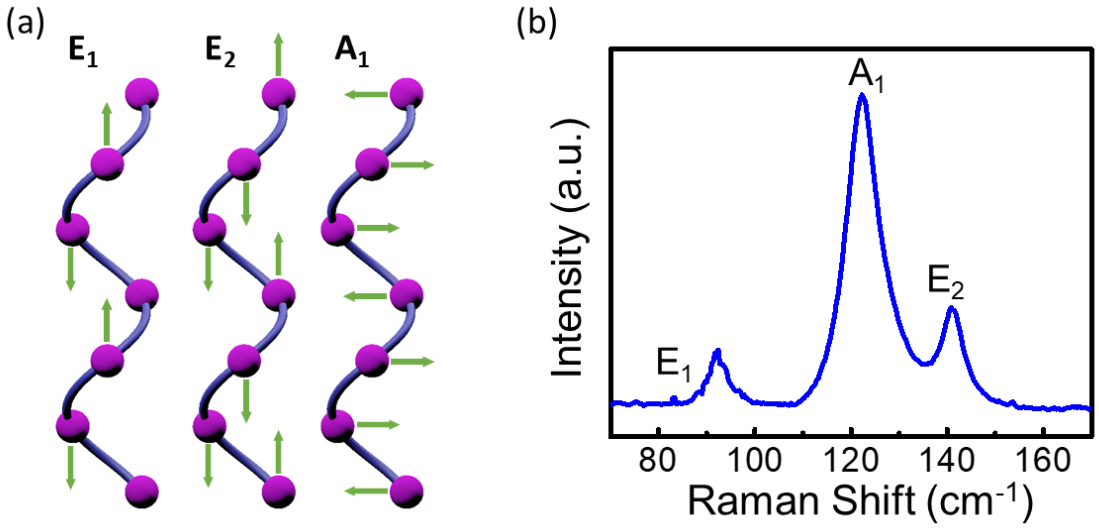

Figure 1.2. Typical Raman spectroscopy of bulk Te samples. (a) Schematic illustration and (b) an experimental Raman response showing 3 first-order Raman active modes.

1.2.2 Synthesis Methods

There are many different synthesizing strategies reported to grow 2D Te with advantages and disadvantages. In this section, we will introduce several methods either in literature or proposed by ourselves.

Pulsed Laser Deposition

A significant challenge for the growth of Te thin film is scalability. Being applicable for mass productivity, synthesis methods providing large-area growth of 2D thin films are more preferable in a variety of realistic applications. Pulsed laser deposition (PLD) was reported to achieve centimeter-scalability of 2D Te deposition with thickness ranging from 2.7 to 6 nm on single crystalline magnesium oxide (MgO) substrate under room temperature and vacuum environment [33]. The thickness of the deposited Te films could be controlled by tuning the number of pulses applied. MgO was considered as a satisfactory growth substrate due to its affordability and chemical inertness. It is further shown that Te could grow vertically with the *c*-axis perpendicular to the MgO (100) surface through another scalable approach, magnetron sputtering [34], which will be discussed in the next sub-section.

Since the intra-chain covalent bonds between adjacent Te atoms along *c*-axis are much stronger than the inter-chain vdW interactions along *a*-axis, the surface free energy of basal plane is three times higher than other planes in the growth intermediate [35]. As a result, large-area Te thin film deposition tends to establish thicker flakes rather than ultrathin films. In PLD method, 248 nm laser was utilized to provide high kinetic energy to the Te source, and the atoms and ions in the plasma plume deposited on the lying substrate. PLD therefore is able to provide a growth route for tellurene with thickness as thin as 2.7 nm.

Physical Vapor Deposition

Although PLD technique indicates a scalable approach of depositing large-area Te thin films, ultrathin films are desirable as 2D materials usually manifest intriguing physical properties such as monolayer graphene [27]. PVD delivers an alternative procedure to grow thinner 2D Te films down to 0.85 nm, corresponding to three layers of Te atoms [33]. A two-zone furnace was used to provide temperature gradient during the process: Te source was placed at the hot end at 650 ^{o}C and silicon with 300 nm silicon oxide (SiO_2/Si) substrate was positioned at the cold end (room temperature) and downstream. Argon with 15 % hydrogen was chosen as the carrying gas to deliver tellurium vapor from the source to the substrate. The dimension of the flakes is typically around 10–100 μm.

SiO_2/Si is a widely used substrate due to its high commercial availability and affordability. However, the surface cleanness and the lack of dangling bonds make it a challenge to be applied as an outstanding template for tellurene growth. Crystal nucleus are required for the formation of ultrathin 2D Te films in PVD method, which brings uncertainties to the synthetic strategy.

On the other hand, the aforementioned attributes conduct some advantages in some situations. Van der Waals epitaxy (vdWE), a novel growing strategy, makes use of chemically inert substrates such as fluorophlogopite mica [36] to synthesize a variety of materials including graphene [37], indium selenide (In_2Se_3) [38], and TMD flakes [39]. This method with mica as the growth substrate was applied to synthesize hexagonal 2D Te films [40] as it not only tolerates larger lattice mismatch but also eases the relocation of Te adatoms along the substrate surface. In this method, Te source and mechanically cleaved fluorophlogopite mica sheets were placed in a sealed quartz tube which was evacuated to provide oxygen-free environments. A horizontal furnace was utilized to carry out the reaction by heating the source side at 750 ^{o}C and the cooling

side at 500 ^{o}C for 1 hour. The resulting tellurene flakes on mica appear in hexagonal shapes with typical lateral length in micrometer range and thickness being 30–80 nm. With mica as a mechanically flexible growth substrate, vdWE reveals great application potential in wearable devices.

Magnetron Sputtering

With its chain-based crystal structure, Te is an anisotropic elemental material. Therefore, the controllability of orientation becomes an interesting topic in material growth and property measurement. It was described that the orientation of Te atomic chains could be managed in a magneton sputtering method through selecting variant substrates as growing templates [34]. Besides, the sputtering is scalable in centimeter range, and the thickness of 2D Te films is down to 2.5–20 nm. This novel sputtering approach widens the avenues for the study of orientation controllability of this material system.

In this method, a home-built external electromagnet (magnetic field up to 500 G perpendicular to the substrate surface) was employed to grow 2D Te films on highly oriented pyrolytic graphite (HOPG), MgO (100), and hexagonal boron nitride (h-BN) substrate. The Te source was sputtered by Ar with a power of 14 W. The sputtered Te thin films express contrasting orientation on the substrates: HOPG and h-BN have the *c*-axis parallel to the surface whereas MgO has it perpendicular to the surface. The directionality of the standing Te helical chains on MgO surface is relatively rare to be reported.

Liquid Phase Exfoliation

Due to the relatively weak vdW interactions between adjacent atomic layers in layered 2D material systems, mechanical exfoliation is widely used as a simple technique to obtain thinner 2D flakes [41]–[44]. Liquid-phase exfoliation (LPE), on the other hand, utilizes organic solvent such as IPA to break the vdW interactions and exfoliate the materials into smaller pieces and is applied to a variety of material systems [45]–[48]. Tellurene flakes obtained by LPE was reported as well [49]. In this method, bulk Te powder was ground with IPA for 30 minutes to squash the larger particles into smaller ones, and the materials along with the solvent were treated sequentially with probe sonication in Ar environments for 5 hours, bath sonication for 8 hours, centrifugation under 1000 g and 6000 g for 30 minutes each, and dried in a vacuum oven at room temperature for 6

hours. The thickness and the lateral length of the obtained 2D Te flakes were 5.1–6.4 nm and 41.5–177.5 nm, respectively.

Thermal Evaporation

The report of Te transistors based on evaporation can be tracked back to 1961 which grows Te thin films down to 50 nm with Hall mobility being around 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [50]. After more than half century, high-performance FETs with great switching characteristics based on evaporated Te thin films were achieved [51]. With the substrate temperature down to –80 ^oC by cooled nitrogen gas flow, the average domain area of the polycrystalline Te thin films on the substrate becomes as large as around 25 μm^2. The average grain size of the thin films increases as the substrate temperature decreases from room temperature and saturates at around –80 ^oC. Polarized light microscopy was manipulated to exhibit the domains due to the absorption dependence of the angle between the light polarization and Te helical chains. The thickness of the thin films was controllable and can be down to 4 nm.

Solution-Based Growth

In order to gain insights on electrical device technology, the following attributes are desirable for tellurene synthesis methods: large scalability, high reproducibility, substrate independence, thinner films achievability, and excellent electric transport performance. In 2018, we proposed a solution-based, substrate-free method that satisfies these properties [28], which provides a reliable production of tellurene flakes down to monolayer for the exploration of 2D material technology. In this method, hydrazine hydrate (N_2H_4) was used to reduce sodium tellurite (Na_2TeO_3), with polyvinylpyrrolidone (PVP) as crystal-face-blocking ligands, in alkaline solution under 160–200 ^oC. The resultant 2D Te flakes in the solution are typically around 50-100 μm in lateral dimension and transferrable through a Langmuir-Blodgett process [52] or an ink-jet printing method [53].

The mole ratio of Na_2TeO_3 to PVP plays a significant role in the synthesis of tellurene. The productivity increases as reaction time passes and gradually saturates after a period of 30 hours. By detailed observations on the relationships between the mole ratio and productivity growing curves, it is distinguishable that it takes a longer time for the tellurene flakes to appear when the ratio of PVP is larger. On the other hand, smaller mole ratios of PVP develop lower ultimate

productivity. Regardless of PVP concentration, the preliminary products are dominant by tellurium nanowires. The intermediate between 1D and 2D form emerges after a period of time, and tellurene flakes show up as final products. On account of the growing mechanism, this synthesis method provides reliable routes to not only 2D tellurene flakes but also 1D Te nanowires. The diameter of the nanowires can be down to 6 nm or thinner [28]. FET based on its 1D NWs will be exhibited in chapter 2.

Moreover, tellurene flakes from monolayer to 10 nm thickness are derivable by a solvent-assisted post-growth thinning process as follows: a certain ratio of tellurene solution, sodium hydroxide (NaOH) solution, and acetone were mixed and placed in ambience under room temperature for 2–10 hours, followed by a centrifugation process at 5000 rpm for 5 minutes. Thinner telllurene flakes could be obtained for a longer period of time. Due to the absence of PVP shielding, the alkaline solution reacts with the tellurene flakes.

Physical Vapor Transport

Polycrystalline materials, composed by many crystal grains with different orientation, are used in a variety of applications since they are more economically efficient and easier to be grown into large area. For instance, most of the current commercially available solar panels, due to these advantages, are utilizing thin film polycrystalline materials including silicon [54], cadmium sulfide [55], cadmium telluride [56], copper indium gallium selenide [57], and more.

Similar to layered two-dimensional (2D) materials which can be mechanically exfoliated by scotch-tape method to obtain thinner flakes, thin films of Te with 2D atomic structure can be realized through the same methodology. Even though Te has exhibited many attracting capabilities in a variety of fields and many methods of growing single crystalline Te have widely been reported [28], [58]–[60], the synthesis and property exploration of polycrystalline thin films are relatively deficient [61]–[63]. We synthesized mm-scale hexagonal polycrystalline Te thin film by PVT under high-vacuumed environment (10^{-5} torr). Interestingly, the material forms in hexagonal shapes even being polycrystalline microscopically. The Raman response, surface roughness, and electrical transport properties of its thin films with variant thickness are studied. Polycrystalline Te shows little thickness-dependence compared to single crystal. Moreover, both electrical transport measurement and phonon response show strong isotropy in polycrystalline Te which is

very different from single crystal. On the other hand, polycrystalline Te performs clear thickness dependence on mobility and ON–OFF ratio measurements, where the latter is similar to single crystal but the former is lower. The 2D Te thin films can be mechanically exfoliated to achieve sub 10-nm thickness, and the surface roughness of the resultant Te flakes is almost the same as layered 2D materials such as graphene.

We demonstrate the synthesis of high quality polycrystalline Te in mm scale, as Figure 1.3(a) shows, by PVT method. 144 mg of Te powder (Sigma-Aldrich, 99.99 %) and a 6 mm by 20 mm silicon substrate with 300 nm SiO_2 were placed in separate regions and sealed under high vacuum (10^{-5} mbar) in a quartz ampoule. The whole system was then heated rapidly at a rate of 10 °C/min to 900 °C (source) / 800 °C (sink) and kept for 24 hours. Tellurium atoms were vaporized in the high temperature environment and moving around in the sealed quartz ampoule. Due to the temperature gradient, they tend to crystallize at the other end of the ampoule. Consequently, hexagonal polycrystalline Te films in mm scale were grown on both sidewalls of substrate and inner wall of the sealed ampoule after the furnace is cooled naturally back to room temperature. Figure 1.3(b) which was taken by optical microscopy shows that a hexagonal shape can be clearly observed even though it is grown on the sidewall of the SiO_2/Si substrate.

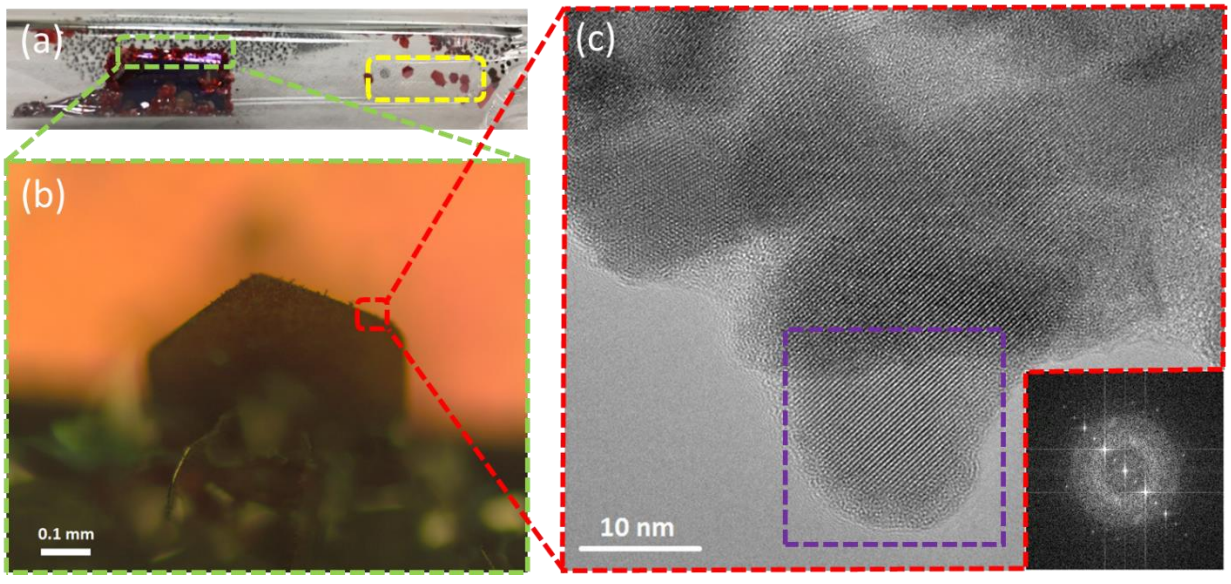

Figure 1.3. As-grown 2D tellurium through PVT. (a) Hexagonal van der Waals 2D Te flakes grown on the inner wall of the sealed ampoule and (b) sidewalls on the SiO_2/Si substrate (c) TEM image and the inset shows the corresponding FFT image of the area squared by the purple dashed lines.

As a powerful tool to realize the material structure in atomic scale, high resolution transmission electron microscopy (HRTEM) was utilized to confirm the atomic structure of the synthesized polycrystalline Te. Sample preparation of HRTEM was realized by a wet-transfer method: As grown polycrystalline Te films were mechanically exfoliated by scotch-tape method and transferred onto SiO_2/Si substrate. PMMA was spin-coated onto the substrate with 2500 rpm, followed by baking at 180 °C for 2 minutes. The substrate with exfoliated Te flakes and PMMA was soaked in buffered oxide etchant (BOE) for 6 hours to thoroughly etch silicon dioxide, and the thin film of PMMA with materials was separated with the substrate and floated on BOE. A copper grid with lacey carbon support film (Agar Scientific) was utilized to fish up the floating PMMA film. The grid with the film was cleaned by DI water, baked dry at 150 °C, soaked in acetone for 15 minutes to dissolve PMMA, and baked dry again at 150 °C for 30 minutes.

HRTEM was performed with FEI Talos F200x operated at 200 kV of electron acceleration voltage. The images of the materials are shown in Figure 1.3(c), and the inset of each TEM is the fast Fourier transform (FFT) pattern of the area squared by purple dashed lines. We can clearly observe single grains on the edge and in the middle of the Te films.

1.2.3 Physical Properties

Optical Properties

Due to the non-destructive property, Raman spectroscopy has been widely utilized to explore the structure of materials through lattice vibration and deformation. As grown polycrystalline Te films were mechanically exfoliated by scotch-tape method and transferred onto SiO_2/Si substrate. Raman measurements were performed using a Horiba LabRAM HR800 Raman spectrometer with a He-Ne excitation laser of 633 nm wavelength. In order to investigate the thickness dependence, mechanically exfoliated Te flakes with variant thickness were obtained by scotch-tape method and transferred onto SiO_2/Si substrate for Raman spectroscopy characterization. Figure 1.4 shows a representative flake with thickness of 25.1 nm confirmed by atomic force microscope (AFM). The thickness dependence and anisotropy of Raman spectrum of single crystal Te synthesized by a substrate-free solution process have been studied and reported [28]. Nevertheless, we found both of these characteristics to be obviously different in polycrystalline Te as shown in Figure 1.5(a). The E_1-TO peaks at around 94 cm^{-1} disappear

regardless of thickness here. Furthermore, the pick shift caused by thickness variance of polycrystal Te is much more immune than single crystal films. For instance, the blueshift in A_1 mode from thickness of ~25 nm to ~6 nm is 9.4 cm^{-1} in single crystal but only 3.7 cm^{-1} for polycrystal. We further studied the isotropy of the flake by Raman spectroscopy with different incidental polarization. The phonon response was collected every 30 degrees, and the 12 resultant patterns, as Figure 1.5(b) shows, almost perfectly coincide with each other throughout the whole measured range. The representative peak value of A_1 of the curves were extracted and plotted into a circular system in Figure 1.5(c). The difference between the maximum and minimum is less than 5 % for all of the obtained data.

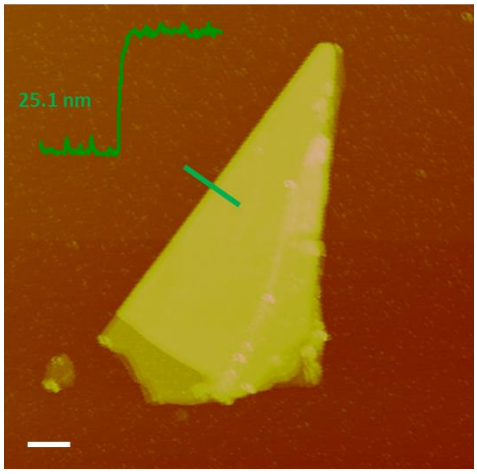

Figure 1.4. AFM image of a typical 2D Te flake with a thickness of 25.1 nm grown by PVT. The scale bar is 1 μm.

Electrical Properties

In order to study the electric transport properties, angle-resolved two-terminal devices with 1 μm channel length on a silicon wafer with 300 nm thermally grown SiO_2 as the gate dielectric were fabricated. Metal electrodes of source and drain regions were patterned by electron beam lithography (EBL) and grown by electron beam evaporation of 20 nm Ni and 50 nm Au, followed by a lift-off process. The devices were measured with a probe station connected to semiconductor characterization system (4200SCS, Keithley) at room temperature. The metal electrodes were designed to be Ni/Au with thickness of 20/50 nm.

The designed device structure is visualized in Figure 1.6(a). To further confirm the isotropy of the polycrystalline material, angle-resolved DC conductance measurements were performed by patterning metal electrodes with variant angles on the same flake with the same channel length of 3 μm. The values of on-state current were extracted and arranged to Figure 1.6(b), and the inset is a false-colored SEM image of a representative device. It is clear that regardless of the orientation of measurement, the on-state current value consistently falls in a small range, confirming the isotropy in electric transport properties.

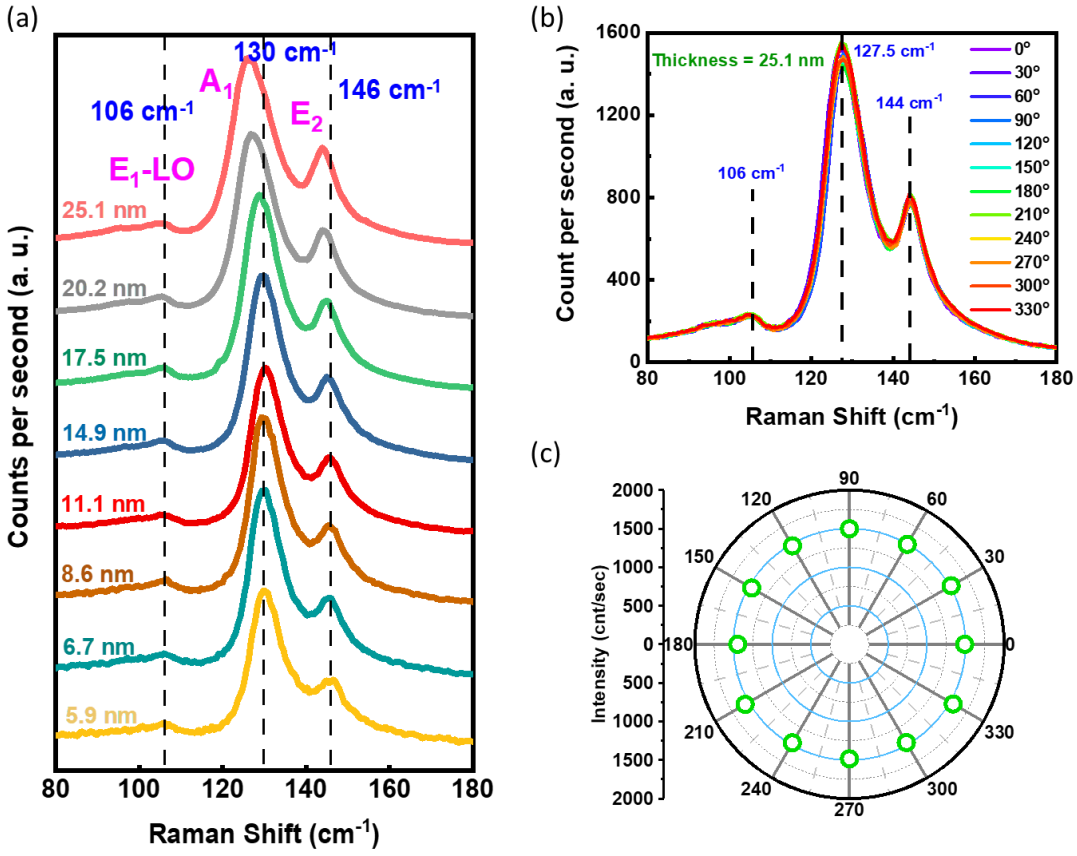

Figure 1.5. Raman spectroscopy of polycrystalline Te thin film. (a) Thickness dependence of Raman spectroscopy on 2D Te flakes and (b, c) angle-resolved (between crystal orientation and incident laser polarization) Raman spectra for the 2D Te flake.

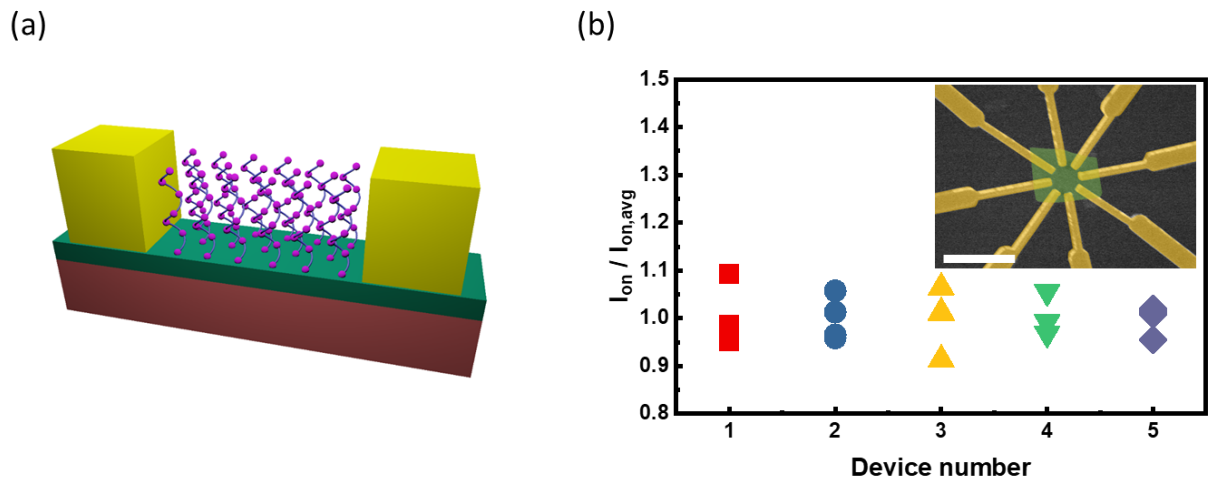

Figure 1.6. (a) Visualization of the designed device structure and (b) the isotropy of electric transport performance. The inset is the a false-colored SEM image of a measured device with the scale bar to be 3 μm.

To further study the transport performance, we designed short channel devices with 300 nm channel length and 300 nm SiO_2 as the gate dielectric. Figure 1.7(a) and (b) show the output and transfer characteristic of a polycrystalline Te device, respectively. The on-state current reaches approximately 10 mA/mm at V_{DS} = 1 V.

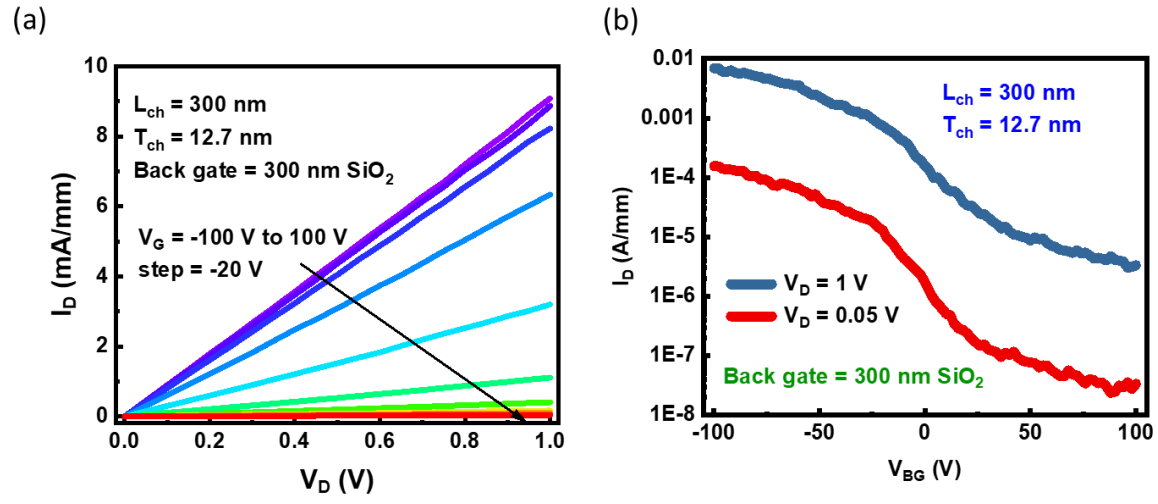

Figure 1.7. Electrical measurement of 2D Te short channel devices. (a) Output characteristic and (b) transfer characteristic of a device with 300 nm channel length and 12.7 nm channel thickness.

We investigated more than 20 devices with different thickness of the films, extracted the ON–OFF ratio and intrinsic mobility, and plotted the results in Figure 1.8(a). As a small-bandgap semiconductor material, the ON–OFF ratio is as expected and consistent with single crystal Te grown by solution-based method [28]. On the other hand, the measured hole mobility is lower than single crystal Te since a single flake of polycrystalline Te is composed of small grains. Both the variant orientation of the grains and junctions between the grains of the polycrystal contributed to the low mobility of the device performance. Besides, the trade-off of two key parameters, on-state current and ON–OFF ratio, was statistically arranged into Fig. 1.8(b). Clear dependence which is consistent with expectations of negative slope is observed.

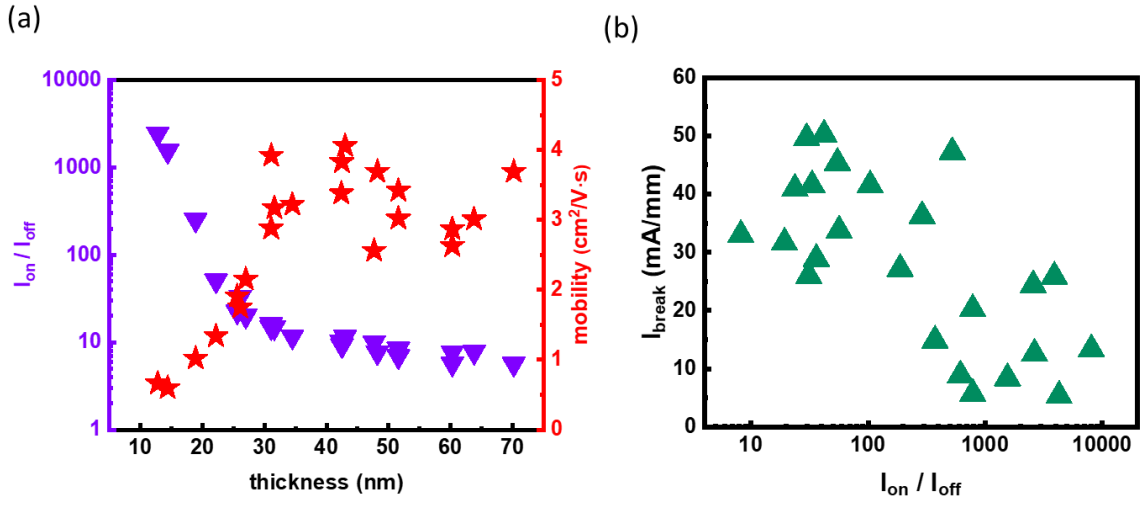

Figure 1.8. Statistical plot of (a) relation between on-current and ON–OFF ratio and (b) relation between ON-current and ON–OFF ratio.

1.3 Indium Oxide

1.3.1 Introduction to Indium Oxide

Being widely applied as channel materials for thin-film transistors (TFT) and potentially for back-end-of-line (BEOL) compatible monolithic three-dimensional (3D) integration, oxide semiconductors have received extensive attention and been broadly explored in the past years [64]–[72]. Among them, indium oxide (In_2O_3) [64]–[66] and doped indium oxides [67]–[70] are

even of great interests because of their exceptional properties including high growth scalability and reproducibility to enable mass production, atomically smooth roughness to guarantee the surface quality, ambient stability to achieve little material degradation in air, and low thermal budget to be well suited with BEOL technologies.

Given its roughly 2.7 eV bandgap [72], In_2O_3 as an oxide semiconductor has attracted revived attention as a promising channel material. Especially, the conformal growth of the atomic-layer-deposited (ALD) In_2O_3 enables it to form on uneven surfaces including side walls and deep trenches, which dramatically benefits the monolithic 3D integration [64], [65], [73]–[76]. Moreover, as the physical size of transistors in integrated circuits becomes smaller according to Moore's law, it requires higher current density for a single device to conduct enough current. It has been reported that scaled back-gate (BG) In_2O_3 transistors accomplish channel thickness (T_{ch}) down to 0.7 nm [64] and drain current (I_D) up to 2.2 A/mm in enhancement mode as 1.5-nm-thick In_2O_3 acts as the channel [66], [77].

Nevertheless, the investigations of the In_2O_3 devices mostly focus on BG structure [64]–[66]. Top gate (TG) In_2O_3 transistors are rarely explored, even though TG devices are particularly demanded in many practical integration applications. The challenges for top-gate devices are due to a) the performance degradation of In_2O_3 channel after the growth of the high-κ oxide gate dielectric and b) the drastic self-heating effect (SHE) as the current density becomes higher under high voltage biases. For the former, it is proposed that the oxygen atoms in the In_2O_3 layer are lost and taken away as the ALD hafnium oxide (HfO_2) is formed, which intensely generates more oxygen vacancies in the In_2O_3 channel and increases the OFF-state current value [78]. Fortunately, this is resolvable by lowering the growth temperature of HfO_2 from 200 ^oC to 120 ^oC followed by a low-temperature RTA treatment in O_2 environment. However, the latter remains as a bottleneck for its TG transistor applications. In order to address the thermal issues, several techniques will be discussed and demonstrated in great details in chapter 3 to chapter 5.

1.3.2 Thin-Film Growth through Atomic Layer Deposition

Atomic layer deposition (ALD) is a significant and useful thin-film deposition technique which will be employed to grow In_2O_3 as the ultra-thin semiconducting channel and hafnium oxide (HfO_2) as the high-*k* dielectric layer (where *k* represents dielectric constant) in chapter 3 to 6.

In a typical process of ALD, the chamber is vacuumed and maintained at a certain growth temperature (generally lower than 250–300 ^{o}C) where the substrate surface is exposed. After the pressure and temperature of the environment is stabilized, gaseous precursors flow into the chamber in a sequential and alternative manner. The precursor bottles are kept at a desired and stable temperature as well so that the vapor pressure is well controlled, and the precursor reactants are skillfully chosen or designed to adsorb on the substrate surface, react but self-limit to only leave a layer of the target element atoms on the surface. An exposure of both precursors (or more in relatively few cases) is regarded as one ALD cycle, and the more cycles are executed, the thicker the resultant film is. Therefore, by appropriately choosing the number of ALD cycle, the thickness of the synthesized thin-film can be precisely controlled even down to angstrom order with a stable ALD system. The In_2O_3 thin films in this dissertation are all grown by ALD, and more details will be covered in the following chapters.

2. TELLURIUM NANOWIRE WITH HIGH CURRENT DENSITY

2.1 Introduction to Tellurium Nanowire

Given the chain-based crystal structure, Te is a one-dimensional (1D) van der Waals (vdW) material. Naturally, a Te atom covalently bonds with its two neighboring atoms and forms a helical atomic chain parallel to the [0001] direction (*c*-axis), and the atomic chains pack with each other by van der Waals (vdW) interactions to form a hexagonal lattice structure.

Even though 2D thin films of them are stable in ambience, it is relatively difficult to realize 1D free-standing chains. In order to study the physical properties of its 1D form, nanotube encapsulation is helpful for isolating Te helical chains [29], [79], [80]. Te atomic chains can be isolated through the encapsulation of carbon nanotubes (CNTs) and boron nitride nanotubes (BNNTs). Due to the spatial confinement of the cavities of nanotubes, the number of atomic chains accommodated in the hosting tubes are tunable. It was reported that the formation of crystal structure of Te is not preferable when the inner diameter (ID) of the nanotube is less than 1.7-2.0 nm [79]. Instead, free standing atomic chains are filled inside. The atomic structure of single Te chain was clearly observed through high resolution transmission electronic microscopy (HR-TEM) and scanning transmission electronic microscopy (STEM), and the optical and electric transport responses of the atomic chains in BNNTs down to 2 nm limit were characterized and reported as well [29].

We reported the synthesis of Te NWs down to a single atomic chain and few-chain limit by filling the cavities of CNTs and BNNTs, respectively, using a physical vapor transport (PVT) technique. By controlling the inner diameter (ID) of CNTs, few-chain and single-chain Te NWs are isolated. We find that the frequency of Raman peaks of the samples varies monotonically with the number of Te atomic chains. Due to the excellent transport properties of Te and high thermal conductivity of BNNTs, the current-carrying capacity of BNNT-shielded Te NWs exceeds that of most semiconductor nanowires, reaching up to 1.5×10^8 A/cm^2, which is only slightly smaller than the semiconducting SWCNTs value of 4.3×10^8 A/cm^2 [85, 86] Due to the shielding and isolation provided by the BNNTs, Te NW at the few-chain limit could stably exist in ambient, and the short-channel Te NW FETs exhibit decent electrical performance even with a diameter of only 2 nm.

2.2 Tellurium Nanowire in Carbon Nanotube

Since the discovery of carbon nanotubes (CNTs) in 1991 [83], this novel 1D material has contributed to the development in the fundamental investigations and research fields [84]–[88]. Beside applied as a conducting or semiconducting 1D materials, CNTs are utilized as a growth templates to have other nano-materials coated outside [89], [90]. Moreover, CNTs being a hollow 1D structure are employed as a natural growing shell for controllable 1D material synthesis as well [79], [91]–[93]. Therefore, Te with a 1D chain-based vdW structure is suitable for this growing strategy [29], [79]. Because of the physical confinement and limited accommodation in the cavities of CNTs, the number of Te helical chains can be accordingly controlled by choosing CNTs with appropriate diameters.

2.2.1 Synthesis Method

Physical vapor transport (PVT) is an important material synthesis technique which is utilized here to grow 1D tellurium. In a typical process of PVT, a precursor is put in an ampoule which is employed as a reacting chamber. In amount of cases, a transport agent such as iodine (I_2) is mixed with the precursor to assist on vapor transportation. After locating the precursors in the ampoule, the ampoule will be vacuumed (usually lower than 1 mTorr) and sealed by a propane-oxygen or acetylene-oxygen torch so that the precursor is in a vacuumed, enclosed environment. Next, the sealed ampoule will be put into a furnace which provides the desired growing temperature and the temperature gradient along the ampoule. The precursor will be vaporized under high temperature, and the vapor will be restricted in space of the vacuumed ampoule. Due to the designed temperature gradient, the precursor will gradually grow on the other end of the ampoule and/or somewhere in between.

A variety of CNTs with different inner diameters were purchased from Sigma-Aldrich. Before filling, 26 mg of CNTs were heated at 420 ºC for 1h in ambient to open the ends of tubes. Cap-opened CNTs and 70 mg of Te (Sigma-Aldrich, 99.8% trace metals) were sealed under vacuum (10^{-5} mbar) in a quartz tube and heated at 439 °C for 4 days. Under such pressure and temperature, tellurium is vaporized and transporting within the space of the sealed ampoule. Chances are that they can possibly fill into the cavity of the cap-opened CNTs and form crystallized

or free-standing atomic chains there. After the growth, as-prepared Te-CNTs were dispersed ultrasonically into methanol for subsequent characterization.

2.2.2 TEM Characterization

A variety of CNTs with different ID were taken as templates, and in a given batch more than 90% of the SWCNTs are successfully filled with Te atomic as shown in Figure 2.1. The High-angle annular dark-field scanning TEM (HAADF-STEM) and high-resolution TEM (HRTEM) images demonstrate that a single Te atomic chain can exist in ambient using a 0.8 nm SWCNT as a container, where the individual Te atoms can also be distinctively resolved with a clear 3-fold-symmetry helical structure (Figure 2.2). The successful realization of a single atomic chain is ascribed to the unique 1D vdW nature of Te. Since a single Te atom tends to covalently bond only with its two neighboring atoms in a chain, a single atomic chain of Te can be isolated through the spatial confinement from a SWCNT.

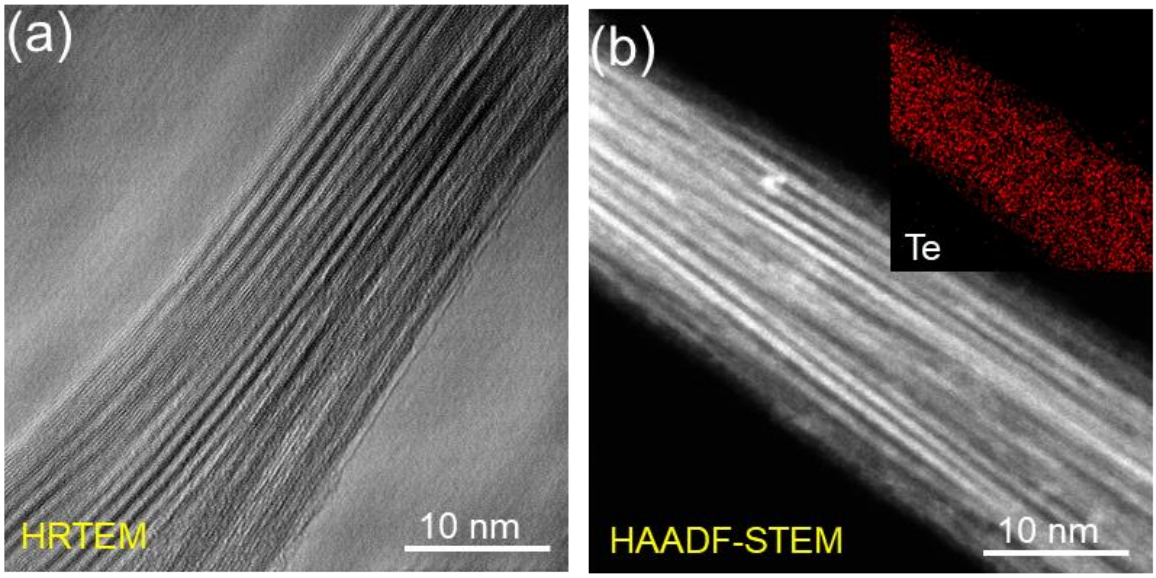

Figure 2.1. TEM characterization of Te chains in SWCNTs. (a) HRTEM image and (b) HAADF-STEM image. Inset shows the corresponding EDX mapping image.

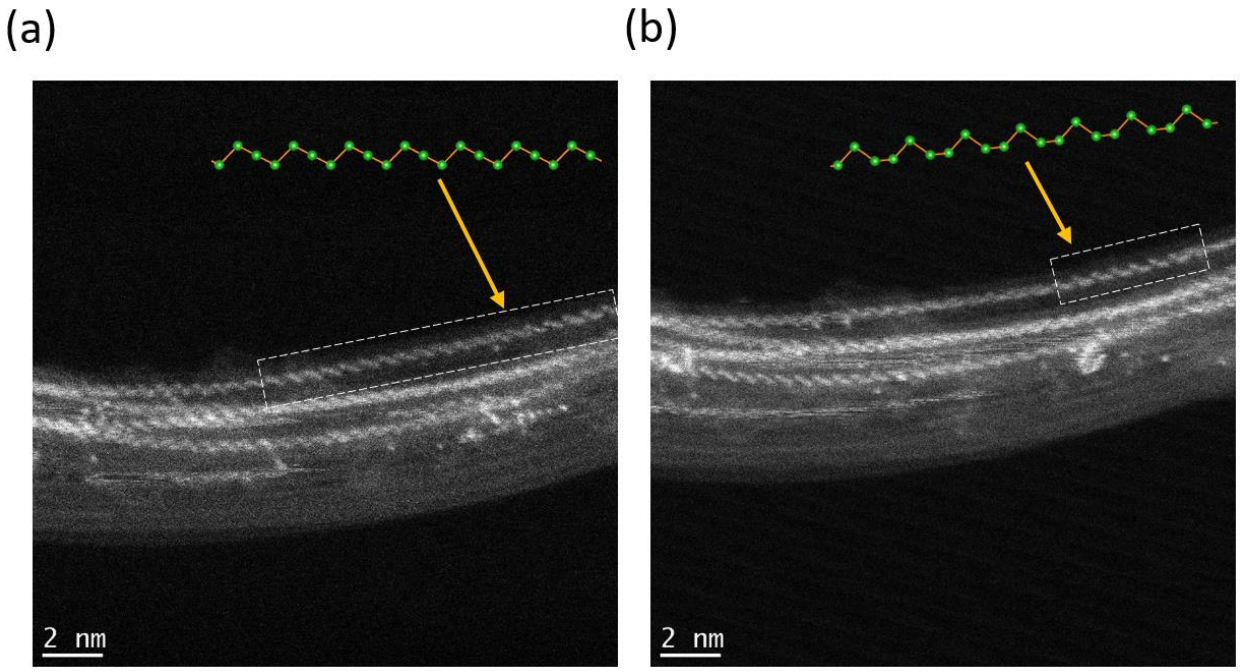

Figure 2.2. Single Te atomic chain in CNTs with ID of 0.8 nm exhibiting 3-fold structure.

SWCNTs with an inner diameter of 1.2 and 1.5 nm increase the number of confined Te atomic chains to 2 and 3, respectively, and a larger-diameter multi-wall CNT (MWCNT) of 2.3 nm results in a wider Te NW with ~19 Te atomic chains (Figure 2.3). The results suggest that by carefully selecting the inner diameter of CNTs, controlled growth of ultra-narrow Te NWs with few-number of atomic chains can be realized.

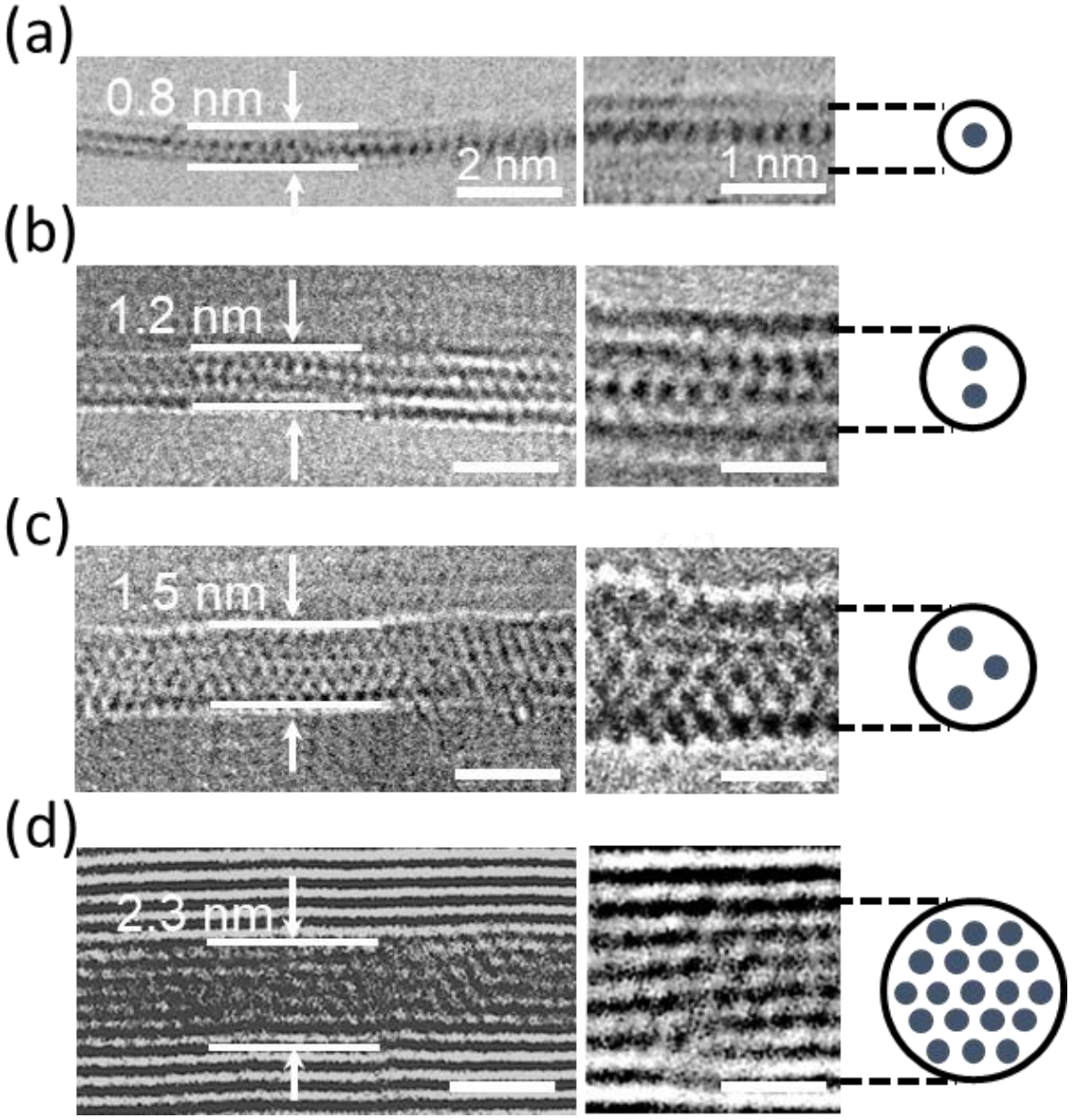

Figure 2.3. HRTEM images of the (a) single, (b) double, (c) triple, and (d) 19 chains of Te shielded by CNTs. Inset: schematic structure diagrams.

2.2.3 Raman Response

As illustrated in Figure 2.4, free-standing single atomic Te chain was fully relaxed to obtain its photon energies [94]–[96]. DFT-relaxed structures give the frequency of E_1, E_2 and A_1 modes to be 68, 178 and 192 cm^{-1}, respectively. With the increase of chains, both the A_1 and E_2 would move toward the low-frequency direction, while the E_1 mode shows the opposite tendency, which are well matched with experiments. The DFT results suggest that vdW interaction between the Te chain and CNT is very weak and the CNT encapsulation keeps the free-standing structure of Te atomic chain.

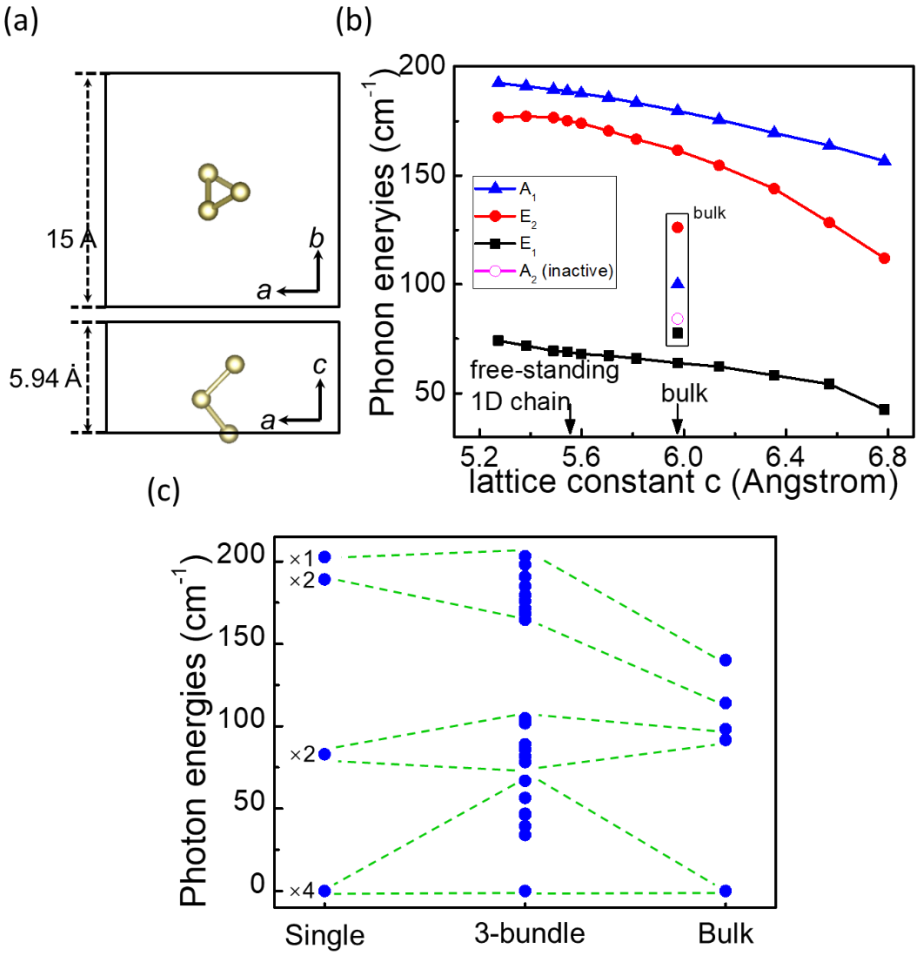

Figure 2.4. The photon energy calculation of Te atomic chains. (a) Atomistic structure of the Te atomic chain. (b) Phonon energies of a single atomic Te chain with dependence of lattice constant. (c) Phonon energies for a single Te atomic chain and bulk Te. In 3-bundle case, the interaction between chains would split the Raman vibration modes and result into the increase of modes, while these modes are degenerated in single chain case or in bulk form

In 2D materials, the Raman frequency is very sensitive to the number of layers, since the vdW interaction can strongly affect the electron-phonon coupling resulting in changed phonon modes [39]. Therefore, the Raman technique can also be used to evaluate the vdW interaction in Te NW crystal and identify the number of atomic chains. For a single Te atomic chain confined in a 0.8 nm SWCNT, the A_1 mode exhibits a large shift towards higher frequency at 196 cm^{-1}, while the E_1 and E_2 modes are too weak to be detected. This result is in good agreement with our theoretical calculations for the free-standing single Te chain. This suggests that the vdW interaction between the single Te atomic chain and the SWCNT inner wall is very weak and the Te chain could be fully relaxed in the SWCNT and exist stably in the form of a 3-fold-symmetry helical coil.

Figure 2.5(a) and (b) present the evolution of Raman peak frequency with the diameter of Te NWs. As the number of Te atomic chains increases from two toward bulk (ID of CNT increases from 1.3 nm to >10 nm), clear redshifts of the A_1 and E_2 modes can be observed. For example, the A_1 peak is significantly shifted from 148 cm^{-1} for 1.3 nm to 123.1 cm^{-1} for bulk.

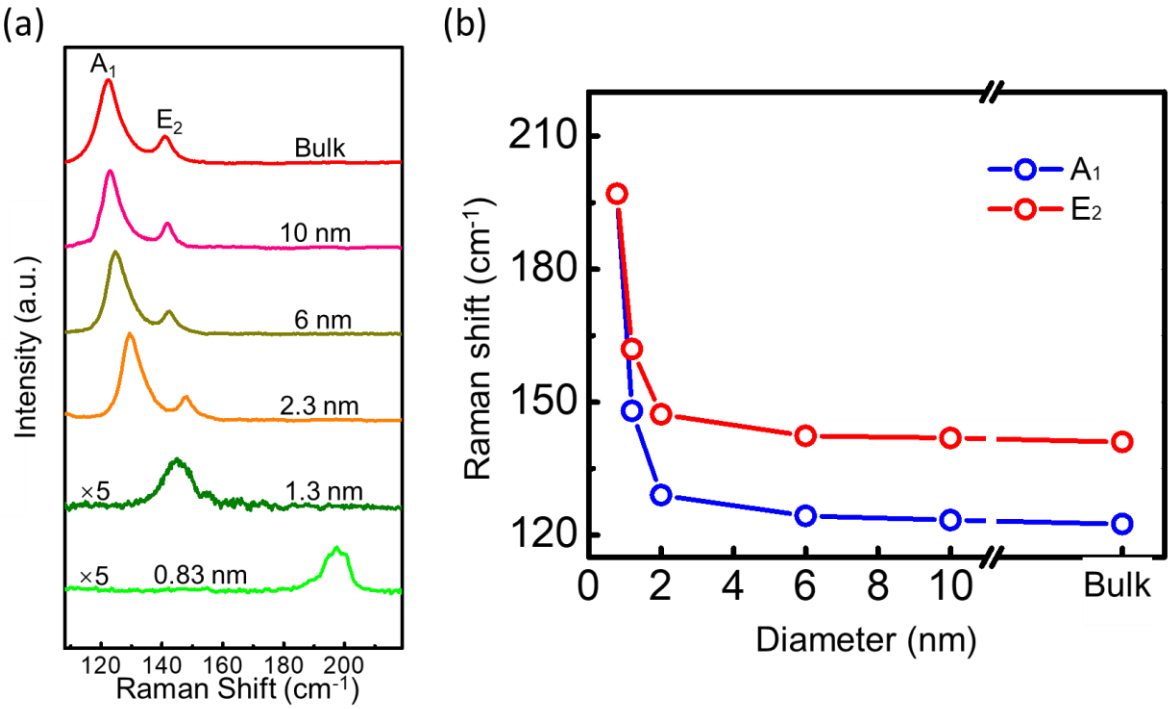

Figure 2.5. (a) Raman spectrum evolution of Te NWs with CNTs of different ID. (b) Dependence of the shifts in Raman peak frequency on CNT ID.

Similar to the previously reported results on few-layer tellurene [28], the unique chiral structure of Te causes the weakening of intra-chain covalent atomic bonding and the enhancement of inter-chain vdW interactions as the number of layers increases. Therefore, Te atoms could more easily restore back in bulk form, resulting in Raman frequency reduction of the A_1 vibration mode. On the contrary, long-range Coulomb interactions dominate the vibration mode of individual Te atomic chains in few-chain samples and lead to the hardening of intra-chain E vibration modes [97].

2.3 Tellurium Nanowire in Boron Nitride Nanotube

Although few-chain Te NWs could be well protected from ambient degradation by CNT encapsulation, the dominant electrical conductivity of CNTs prevents direct electrical measurements of the shielded Te NWs. BNNTs are electrically insulating with the same hollow structure as CNTs, and are also the promising 1D nanoscale containers for guest species such as metals, metal halides and molecules [98]–[100]. We demonstrated that BNNTs grown by a chemical vapor deposition (CVD) process are an ideal template to encapsulate few-chain Te NWs using the same PVT technique as with CNTs. Since BNNTs are electrically insulating, this property makes it possible to perform direct electrical measurements on Te NWs down to the few-chain limit [101], [102]. Furthermore, the ultrahigh thermal conductivity of BN helps on heat dissipation as large current conducts through countable Te atomic chains, assisting the Te-BNNT devices to avoid SHE.

2.3.1 Synthesis Method

BNNTs are obtained using chemical vapor deposition (CVD) combined with growth vapor trapping (GVT) approach [101] as illustrated in Figure 2.6. In the beginning, clean Si substrate was uniformly covered by 10 nm $MgCl_2$ films deposited by pulsed laser deposition (PLD) technique, and it was then placed upside down on the top of Al_2O_3 boat with B, $MgCl_2$, and FeO precursors (molar ratio of 4:1:1) and loaded at the end of a quartz tube. The quartz tube was placed in the center of a horizontal tube furnace with the holding temperature of 1200 ^oC for 30 min, and the ammonia flow was set to be 200 sccm. The GVT is realized since the substrate is placed at the end of quartz tube, and the growth process cannot be affected by the flow of the ammonia gas.

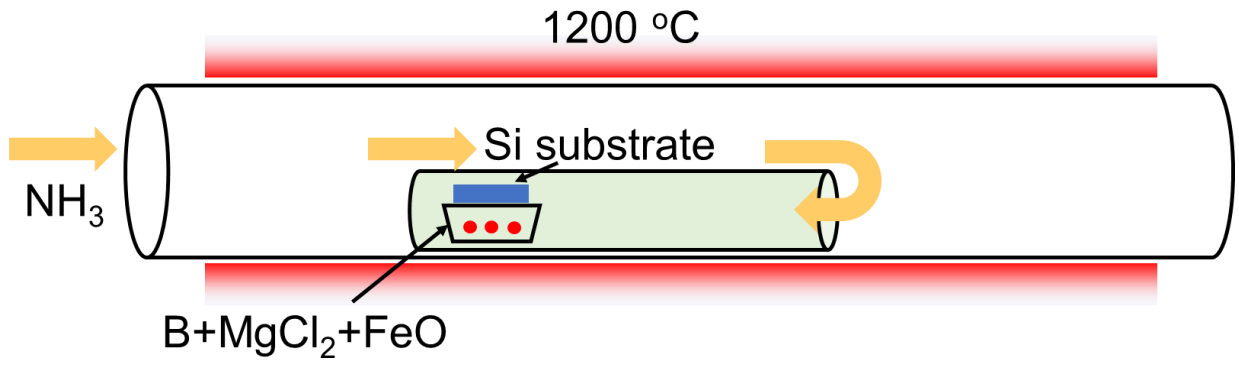

Figure 2.6. Experimental setup for the CVD growth of BNNTs.

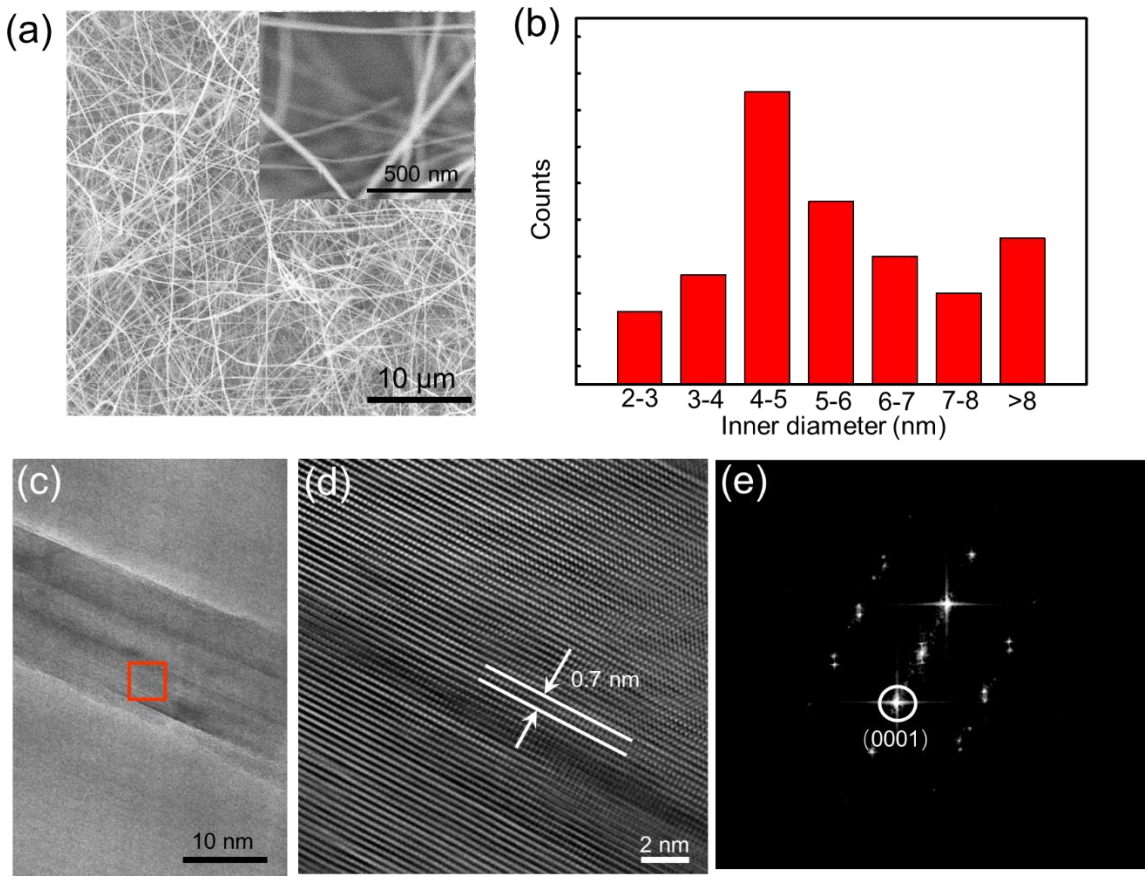

Figure 2.7. Materials characterization of BNNTs. (a) SEM image of as-grown BNNTs on Si substrate. Inset image shows the enlarged SEM image. (b) Statistics of the inner diameter of BNNTs. (c) TEM of an individual BNNT showing nano-tubular structures of BNNTs with amorphous-free sidewalls. (d) HRTEM of a BNNT with the interlayer distance to be 0.35 nm. (e) Corresponding SAED pattern of BNNT.

Figure 2.7 shows the scanning electron microscopy (SEM) image of the as-grown BNNTs on Si substrate, where clean and long BNNTs can be clearly observed, and the length is estimated to be longer than 10 μm. Transmission electron microscopy (TEM) indicates that these BNNTs exhibit a high-order tubular structure with uniform inner diameter along the axial direction (Figure 2.7(c)). High-resolution TEM (Figure 2.7(d)) demonstrates that the as-grown BNNTs are well crystallized almost without amorphous BN coatings on the surface of the sidewalls. Consist with previous results, the interlayer spacing of the BNNT walls is estimated as ~0.35 nm, suggesting the BNNT tends to crystalline with the (0001) faces along the radical direction. According to the distribution of inner diameter of BNNTs, we can confirm that these BNNTs have an average inner diameter of 5 nm (Figure 2.7(b)).

Before filling, the caps of the BNNTs were removed by ultrasonicating in 10% ammonium hydroxide solution for 4h, followed by thermal treatment at 800 ºC in air for 1h. Cap-opened CNTs/BNNTs and 70 mg of Te (Sigma-Aldrich, 99.8% trace metals) were sealed under vacuum (10^{-5} mbar) in a quartz tube and heated at 439 °C for 7 days. As-prepared Te-BNNTs were dispersed ultrasonically into methanol for subsequent characterization.

2.3.2 TEM Characterization

Figure 2.8(a) and (b) are schematic illustrations of an ultra-narrow Te NW shielded by a BNNT (Te-BNNT). Before filling, the caps of nanotubes were first removed by ammonium hydroxide etching. Figure 2.8(c) and Figure 2.9 show a representative TEM image and STEM images of individual Te NWs inside BNNTs, respectively, where the Te-filled section exhibits a clearly different contrast in the BNNT cavity. Combined with the X-ray energy dispersive spectroscopy (EDS) elemental mapping shown in Figure 2.8(g), we confirm that elemental Te NWs can be successfully confined inside the cavity of a BNNT.

HRTEM images show that Te NWs confined in BNNTs crystallize homogeneously in the form of a single crystal, where distinctive lattice fringes belonging to the Te NW can be clearly observed, suggesting that the Te NW is well crystallized with high quality (Figure 2.8(d) and Figure 2.10). Note that the filling length of Te NWs in BNNT usually less than 400 nm, which is much shorter than that in CNTs. This is attributed to the polarity of interatomic B-N bonding and delocalization of π electrons in BNNTs, which leads to strong interface interactions between the inner BNNT surface and the filled Te atoms, restricting high aspect ratio filling [98]. In our

experiments, the narrowest diameter of Te NW achieved was 2 nm, corresponding to about 19 individual Te atomic chains inside a BNNT cavity (Figure 2.8(e) and (f)).

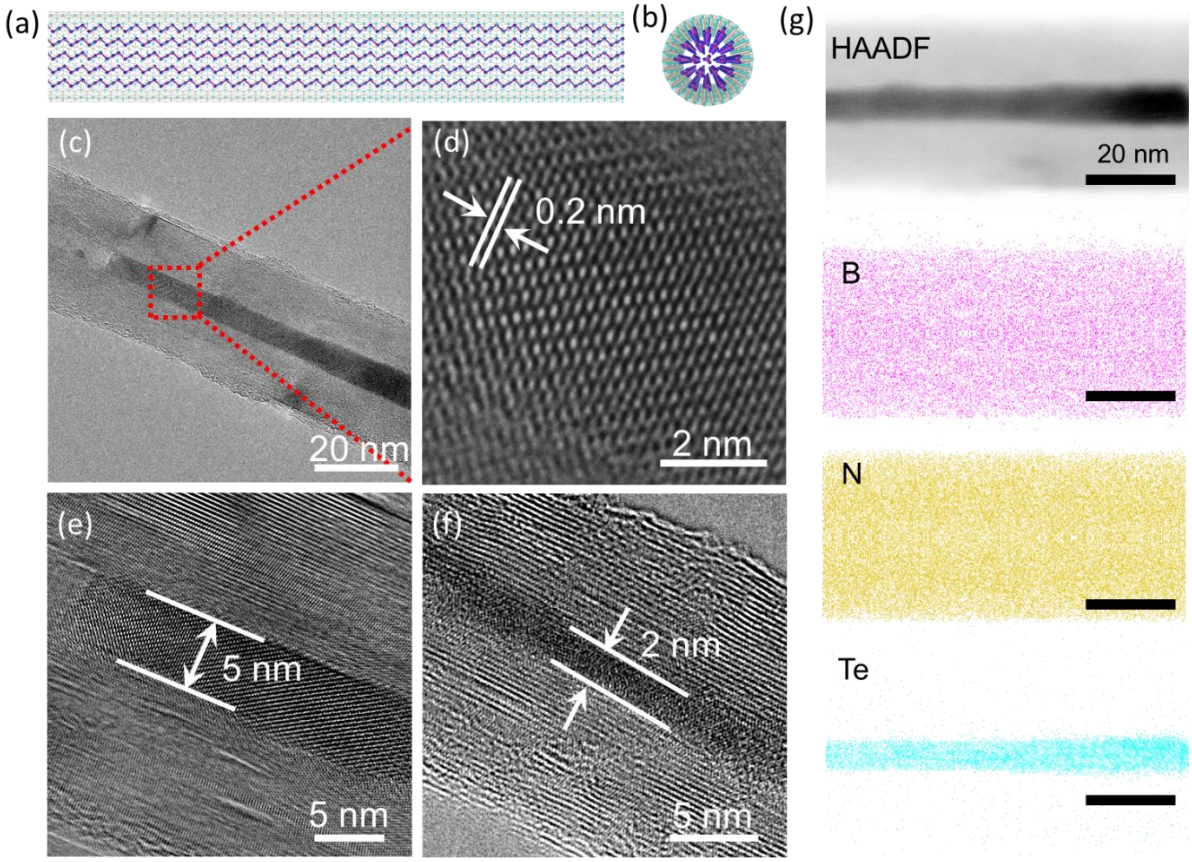

Figure 2.8. Characterization of few-chain Te NWs shielded by BNNTs. (a) Side view and (b) top view of schematic illustration of a Te-BNNT. (c) TEM image of a 5 nm Te NWs in a BNNT. (d) Enlarged HRTEM image of red rectangular region marked in (c). (e, f) HRTEM images of BNNT filled with 5 nm and 2 nm Te NWs, respectively. (g) HAADF-STEM image and EDS maps showing the chemical composition of the filling material.

2.3.3 Raman Response

As was previously done for CNTs, Raman frequency shifts are used to determine the diameters of Te NWs encapsulated by the BNNTs. The A_1 mode of a Te-BNNT with 5 nm inner diameter exhibits a blue shift of 2.4 cm^{-1} compared with bulk form (about 121.2 cm^{-1}), and the vibration frequency continues to shift up to 129.2 cm^{-1} as the diameter of the Te NW is reduced down to 2 nm (Figure 2.11(a)). Thus, we applied Raman spectroscopy to determine the diameter

of Te NWs filled in BNNTs and located the samples for device fabrication after they were transferred onto a SiO_2/Si substrate.

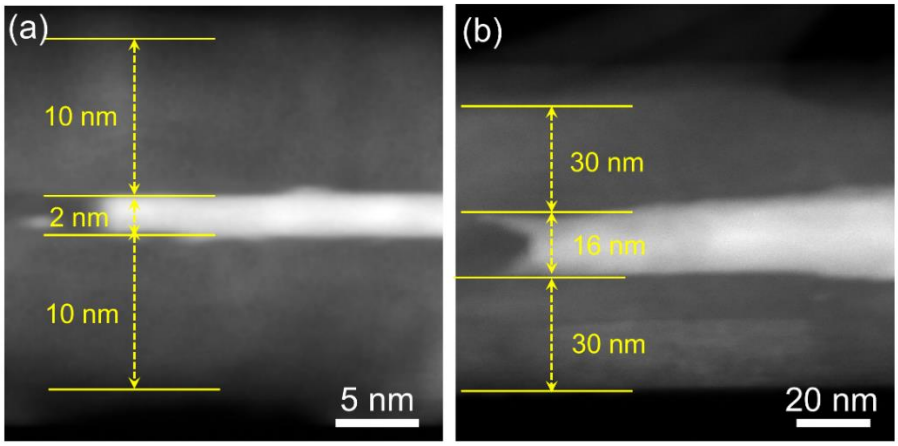

Figure 2.9. STEM images of Te filled BNNTs showing obvious contrast with (a) 2 nm and (b) 16 nm ID.

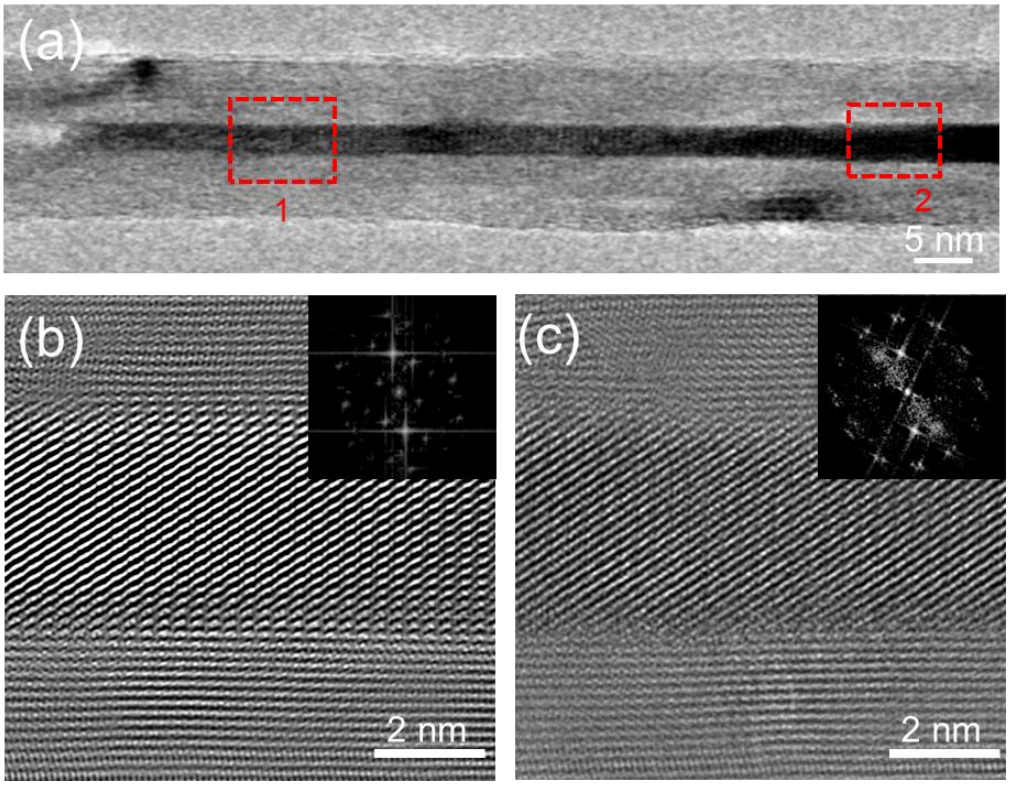

Figure 2.10. TEM characterization of Te-BNNT. (a) low-magnificent TEM image of an individual Te NW encapsulated by BNNT. (b, c) HRTEM images collected from the areas marked with rectangular in (a). Inset image shows the corresponding SEAD patterns of single crystalline Te NW.

In-situ temperature-dependent Raman spectroscopy was conducted to investigate the thermal stability of Te-BNNTs and bare Te NWs. The Raman signals were collected after the samples annealed for 5 min in ambient environment. As shown in Figure 2.11(b)–(d), bare Te NWs are easily degraded and damaged at 250 ºC, which is much lower than that for those shielded by BNNTs (400 ºC). The shift of Raman peaks can be attributed to the non-crystalizing phase change induced by high temperatures.

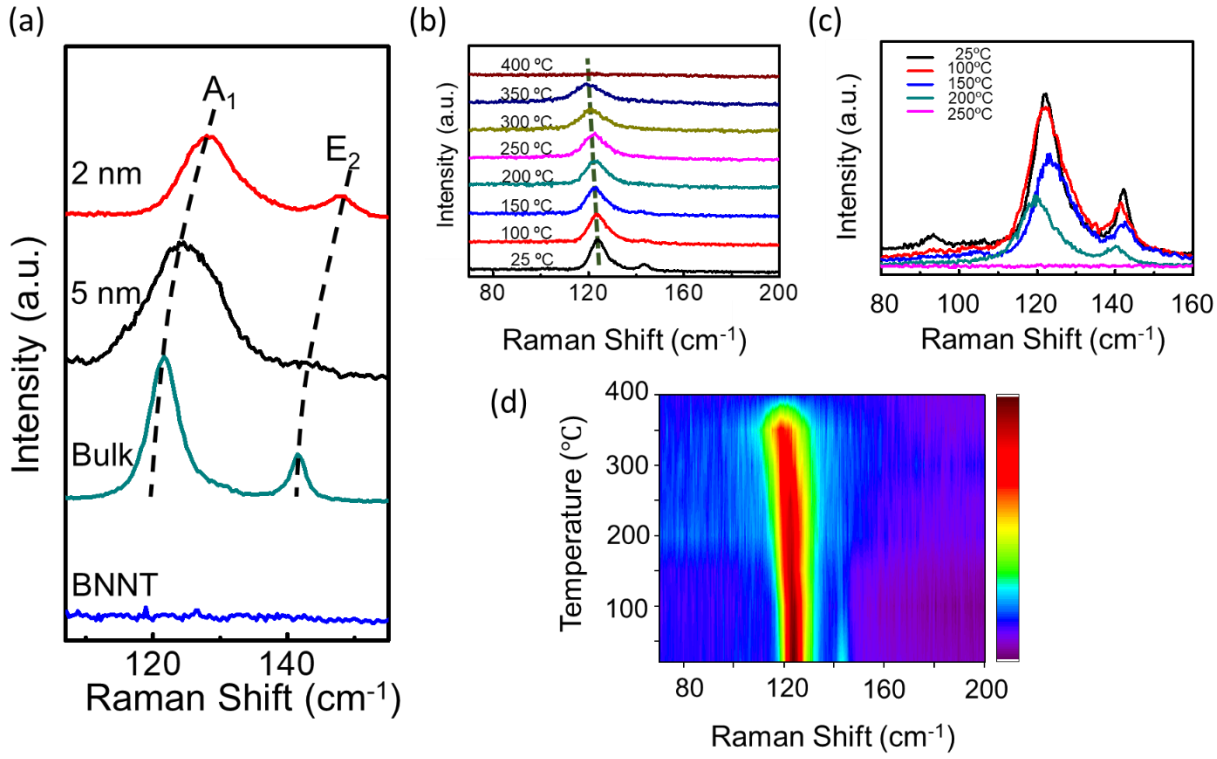

Figure 2.11. Raman response of Te-BNNTs. (a) Raman spectrum comparison of Te NWs in BNNTs with different diameters. (b–d) *In-situ* temperature-dependent Raman spectra of (b, d) Te-BNNTs and (c) bare Te NWs.

2.3.4 Electrical Performance

Large Current Breakdown

In order to investigate the electrical properties of few-chain Te NWs, we first fabricated two-terminal devices with an isolated Te-BNNT as the channel material on a Si substrate with 90 nm SiO_2 as the gate dielectric. Ni/Au (30/100nm) electrodes were patterned using electron-beam lithography (EBL) followed by electron beam evaporation of metals and lift-off process. Short-

channel (100 nm) devices were fabricated to ensure the channel region was fully filled by the Te NW. Empty BNNT devices were also tested for comparison.

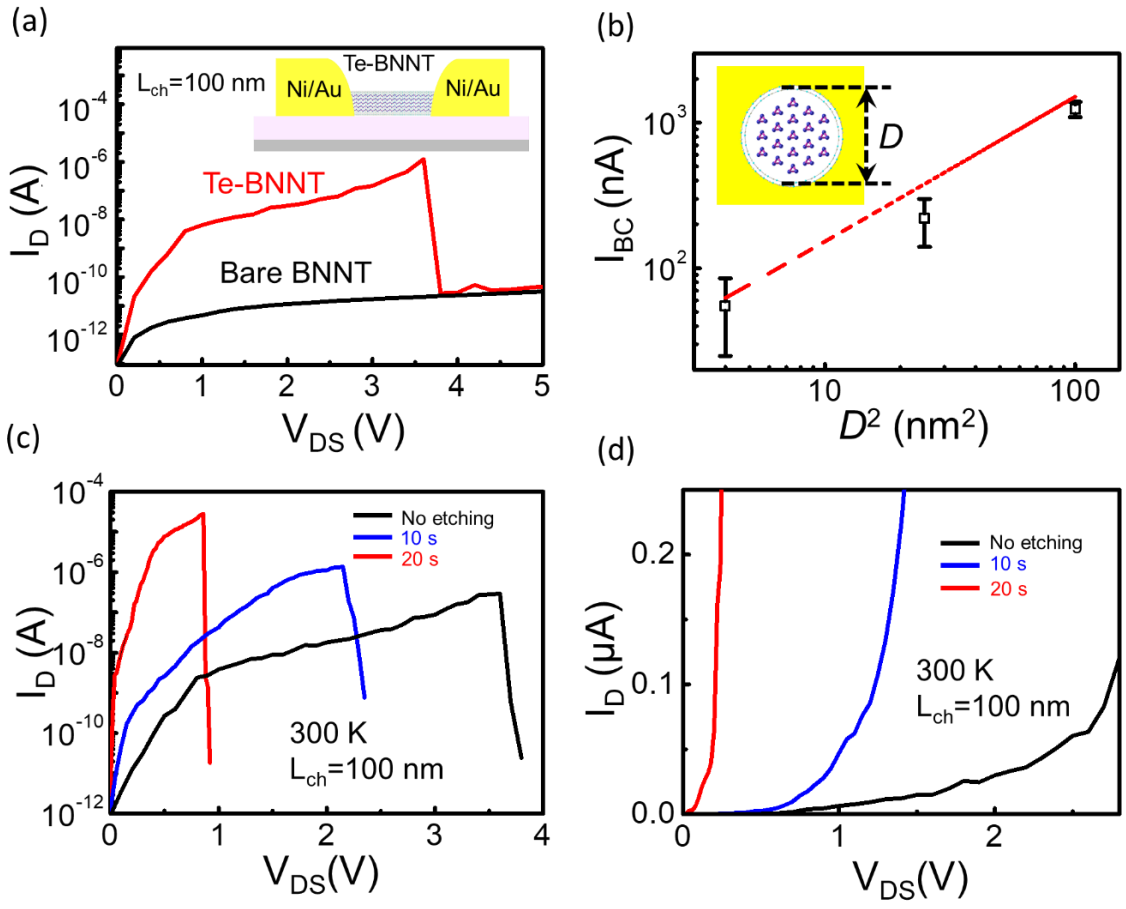

Figure 2.12. Current-carrying capability of Te NWs encapsulated in BNNTs. (a) I-V curves up to breakdown of a Te-BNNT device with a 100 nm channel length and an empty BNNT device. (b) Breakdown current (BC) versus D^2 with all channel lengths of 100 nm. (c) Logarithmic scale and (d) linear scale plot of I-V characteristics in Te-BNNT devices with different etching time.

As the I-V characteristics show in Figure 2.12(a), the current of a Te-BNNT device with a diameter of 10 nm has about four orders of magnitude higher current carrying capacity than that of the empty BNNT device with the same configuration, which confirms that the Te NW is responsible for the channel conduction instead of the BNNT. The device could sustain a large V_{ds}, and the current does not show any saturation until device breakdown at V_{max}=3.6 V and I_{max}=1.2 μA. The diameter-dependent breakdown current of ultra-narrow Te NWs was also measured based on devices with 100 nm channel lengths. Although the encapsulated Te NWs have varying diameters, BNNTs with different diameters usually have similar thickness (> 10 nm) as observed

by HRTEM images, so the breakdown current is mainly determined by the intrinsic properties of the inner Te NWs. For devices with D^2 of 100 nm^2, the average breakdown current is determined to be about 1.2 μA. The reduction of D^2 leads to the scaling down of current carrying capacity of Te, and smallest average current measured is 62 nA for devices filled with 2 nm Te NWs. The values of ampacity in different devices are fitted linearly with D^2 as plotted in Figure 2.12(b). The realization of electrical measurement of few-chain Te NWs is attributed the efficient dissipation of Joule heating by BNNT encapsulation [103].

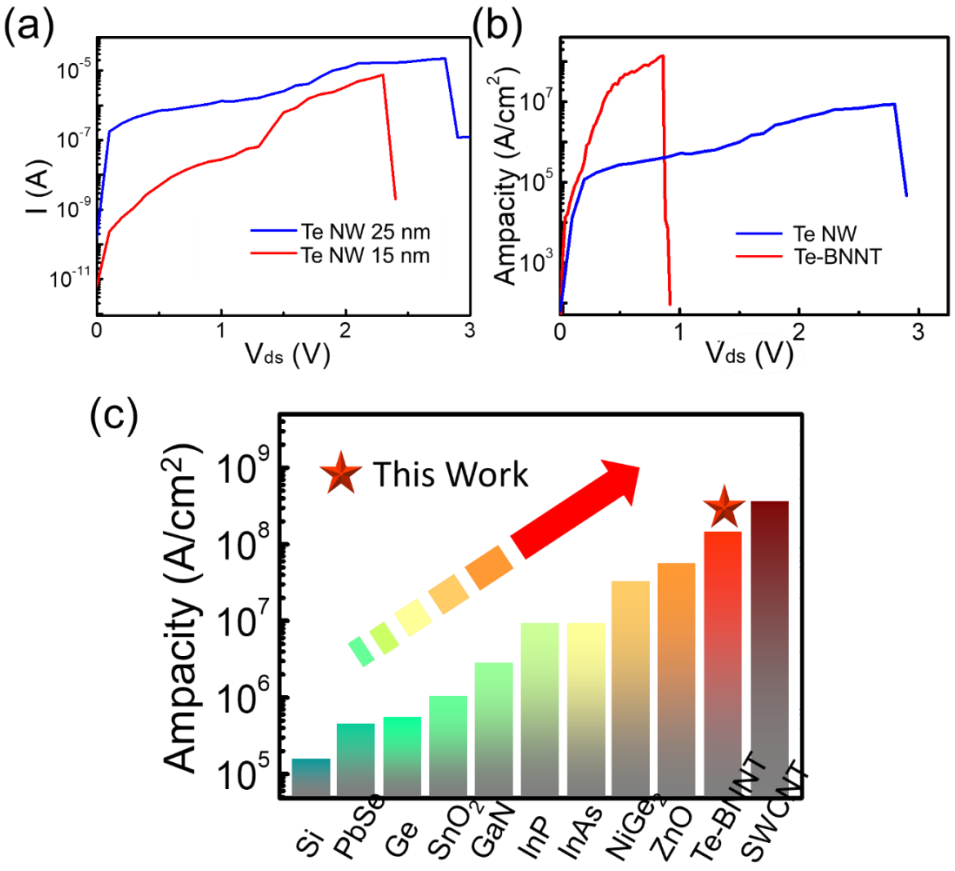

Figure 2.13. (a, b) I-V curves up to breakdown of (a) Te NW devices with different diameters and (b) Te NW and Te-BNNT devices with the same diameter. (c) Comparison of the ampacity of Te-BNNTs and other semiconductor NWs.

The BN encapsulation protects the few-chain Te NW from damage during the measurements, but it also introduces a large electrical contact resistance, resulting in reduced channel current. Considering this, an accurate and selective BN etching process was developed to directly control the thinning of the BNNT insulator layer. Figure 2.12(c) and (d) show the I-V

curves of typical devices as a function of etching time. Notably, the breakdown current is greatly enhanced up to 29 μA after 20 s of etching, almost 100 times larger than the un-etched reference devices. Total resistance of the device after 20 s of etching is calculated to be 1.6 kΩ·μm, which is one order of magnitude smaller than that of devices without etching (about 21 kΩ·μm).

The value of current capacity for the Te-BNNT devices reaches up to 1.5×10^{8} A cm^{-2}, almost two orders of magnitude larger than that in bare Te NW devices of 7.4×10^{6} A cm^{-2} (Figure 2.13(a) and (b)). This value exceeds most of the reported semiconductor NWs [104]–[111] (Figure 2.13(c) and Table 2.1), and it is also higher than those from the high-ampacity $TaSe_3$ and $ZrTe_3$ quasi-1D metallic nanowires [112], [113]. Indeed, it is only slightly smaller than the semiconducting SWCNTs with similar configuration (about $3.0\sim8.8\times10^{8}$ A cm^{-2}) [81], [82]. Such dramatic enhancement of ampacity can be attributed to the high mobility of Te NWs, extremely high thermal conductivity of BN (about 360 W/m·K), and low electrical and thermal resistance at the BN/Te interface [114]. The excellent current carrying capacity of Te-BNNT strongly suggests that this nanomaterial system has its potential for future electronics applications, especially high-performance FETs with ultra-short channels.

Table 2.1. Comparison of ampacity of devices based on semiconducting nanowires.

Semiconductor	L_{ch} (μm)	D (nm)	I_{max} (μA)	Ampacity (MA/cm²)
Si	5.06	180	170	0.1
PbSe	3	80	10	0.5
Ge	3	20	0.7	0.56
SnO_2	2.2	50	25	1
GaN	3.2	400	3200	3
InP	2	100	1000	10
InAs	1.5	33	96	10
$NiGe_2$	1.6	50	850	35
ZnO	3	228	1000	63
SWCNT	0.02	1.2	10	880
SWCNT	0.3	1.2	3~6	264~528
Te-BNNT	**0.1**	**5**	**29**	**150**

Field-Effect Transistor

After determining the diameter of Te NWs encapsulated in BNNT by Raman spectroscopy, source/drain regions were patterned by EBL, followed by electron beam evaporation of 30 nm Ni and 100 nm Au as metal contacts. The devices were measured with a probe station connected to a semiconductor characterization system (4200SCS, Keithley) at room temperature. For thinning of BN at the contact areas, Ar/SF_6 plasma with power of 75 W and pressure of 50 Pa was used with different irradiation times at room temperature. The schematic illustration is exhibited in Figure 2.14.

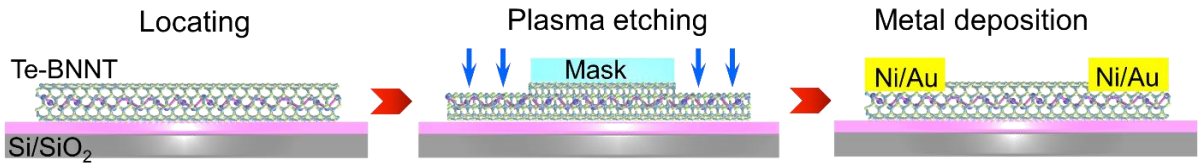

Figure 2.14. Schematic illustration of the BN thinning process and contact formation.

The electrical characteristics of FETs based on Te NWs were also systematically studied. Note that the diameter of ultra-narrow Te NWs shielded by BNNTs is restricted to less than 10 nm due to the inner diameter limitation of BNNTs, whereas Te NWs with larger diameters can be well achieved using a substrate-free solution process as introduced in section 2.2.6. Thus, two types of Te NWs were systematically investigated: ultra-narrow Te NWs in BNNTs with diameters of 2–10 nm and solution-grown Te NWs with diameters of 6–40 nm. Figure 2.15(a) shows the typical schematics of FET device based on Te-BNNT, where an Al_2O_3 capping layer grown by low-temperature atomic layer deposition (ALD) can dope the channel and change the FET characteristics from p-type to n-type. Figure 2.15(b) shows a false-colored scanning electron microscope (SEM) image of some short-channel devices, where the outer diameter of the Te-BNNT was measured to be 24 nm by AFM (Figure 2.15(c)).

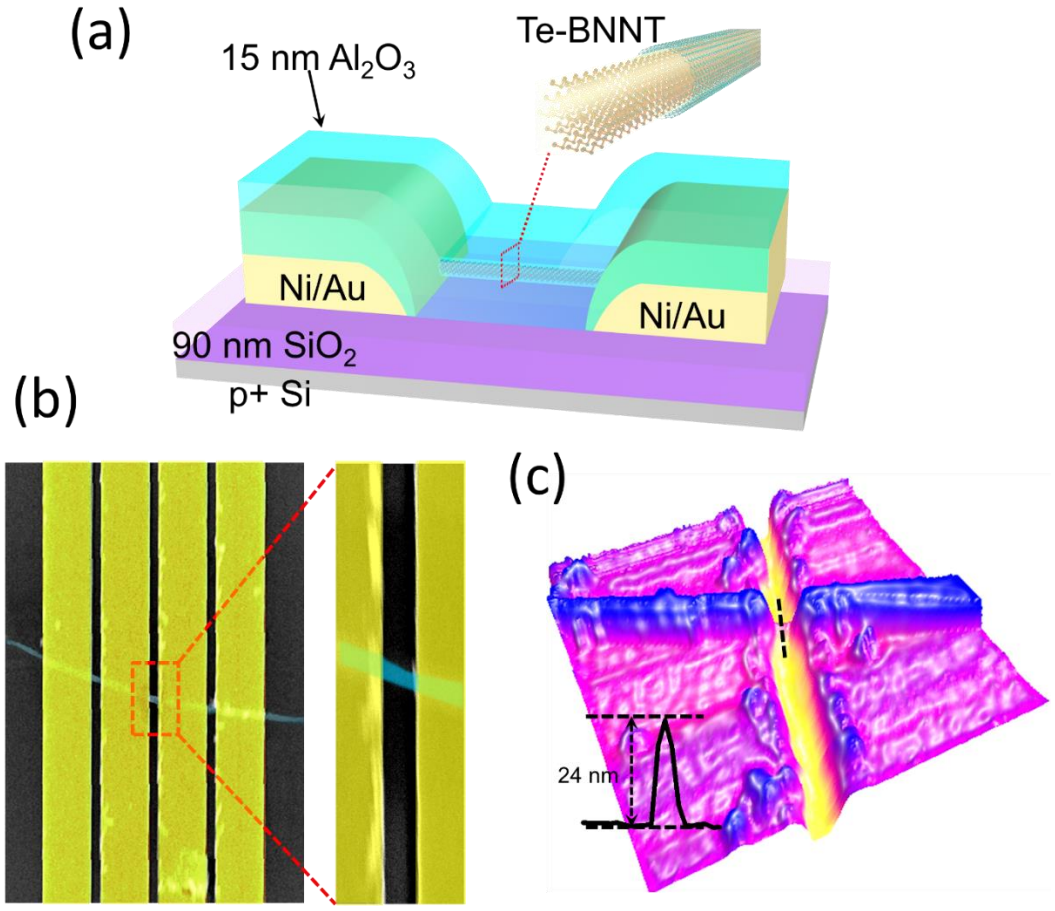

Figure 2.15. (a) Schematic of an individual Te-BNNT FET. (b, c) False-colored SEM image (b) and AFM height profile (c) of a representative FET device before Al_2O_3 capping.

Figure 2.16(a) and (b) present the electrical performance of a Te NW FET with a diameter of 13 nm measured at room temperature. The device exhibits the typical p-type characteristics with ON–OFF ratio on the order of ~1×10^4 at a small V_{ds} of 0.05 V, with on-state drain current up to 700 mA/mm at V_g=−40 V normalized by the diameter. Short-channel (100 nm) devices were also fabricated for comparison (Figure 2.16(c) and (d)). The diameter dependence of the ON–OFF ratio and maximum drain current based on long-channel devices was also systematically studied, with data elucidated from more than thirty devices (Figure 2.16(e)). Due to the enhanced gate electrostatic control in narrow NWs, the ON–OFF ratio increases sharply from ~1×10^2 to ~1×10^5 as the diameter decreases from 40 to 6 nm. However, the current density exhibits the opposite trend in narrower samples since they are more susceptible to surface oxidization and defects. Indeed, FETs on ultra-narrow bare Te NWs less than 6 nm in diameter start to lose electrical

conductance and gate control since the crystalline structure of Te at this scale cannot be well preserved in ambient for a long-time during device fabrication and measurement.

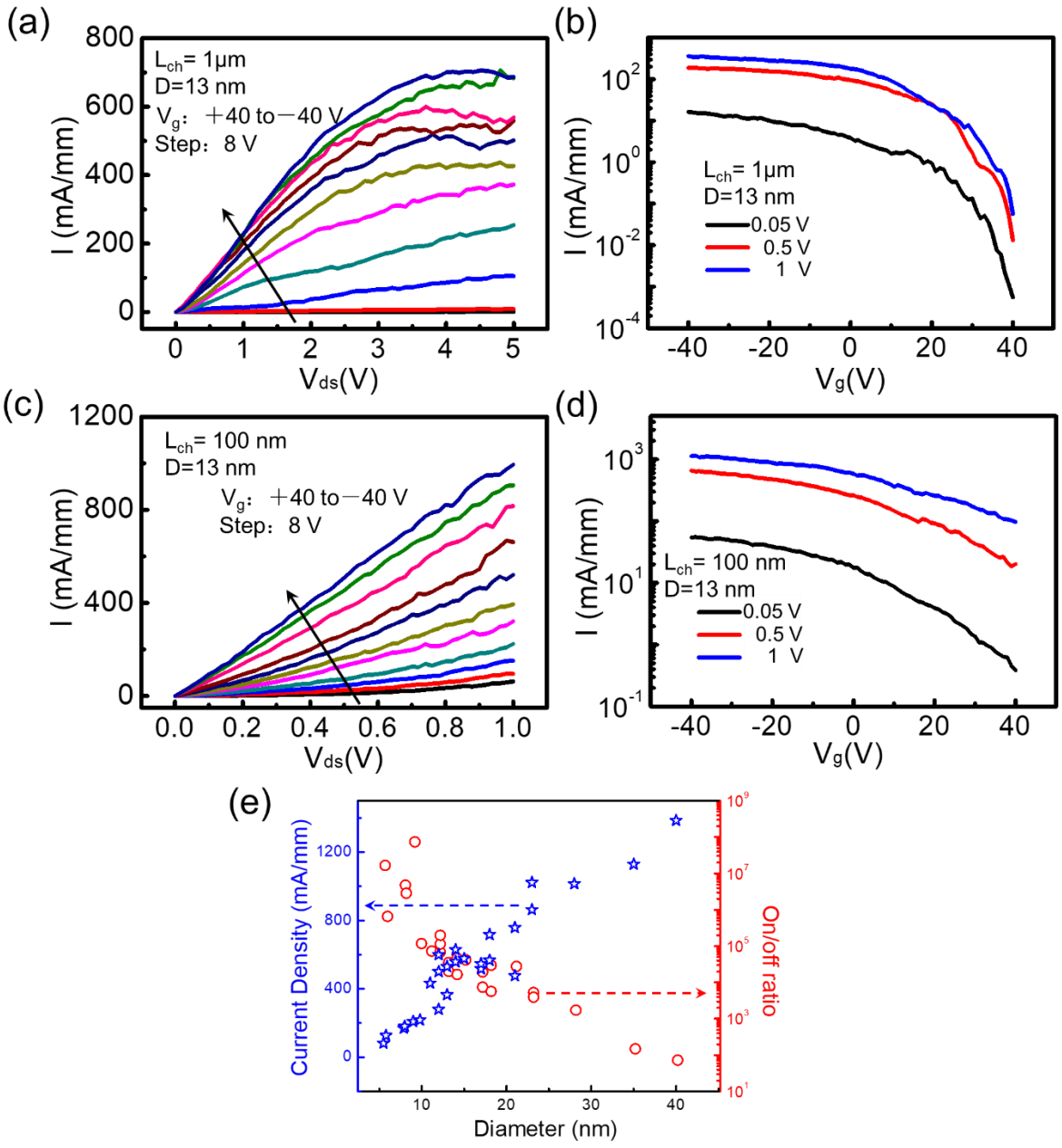

Figure 2.16. Electrical performance of a Te NW transistor. (a) Output characteristics of a typical p-type Te NW transistor with a diameter of 13 nm. (b) Corresponding transfer curves of the same device. (c) Output curves and (d) transfer curves of the device with a short channel of 100 nm.

For Te-BNNT devices with typical metal-semiconductor (MS) or metal-insulator-semiconductor (MIS) contacts, the current of channel is mainly limited by the contact resistance, determined by two factors: Schottky barrier height/width and the tunneling resistance of the inserted ultrathin insulator [115]. Although Ni has a relatively high work function which is close to the Fermi level of unintentionally *p*-doped bulk Te, direct contact at an MS interface results in a high Schottky barrier height for ultra-narrow Te NWs due to an enhanced bandgap by the quantum confinement [116]. A large Schottky barrier height leads to a large contact resistance at the Ni/Te contact. Few-layer BNNT in the contact region after selective dry etching could provide a perfect insulating layer for the inner Te NW from the process damage. Therefore, the thickness of BN layer needs to be optimized to realize the maximum current carrying capacity in devices. The shielding of BNNT enables Te-BNNT devices to electrically functionalize with Te NWs having diameters as small as 2 nm. More interestingly, the transport characteristics of Te-BNNT FETs show n-type behavior after Al_2O_3 capping, indicating that the classical Fermi-level pinning issue doesn't exist on Te-BNNTs [117]. The 2 nm device possesses a large on-state current reaching up to 50 mA/mm at V_{ds}=1 V (Figure 2.17(a)). Such high current is comparable to that in monolayer MoS_2 transistors with the same short channel length (I_{max}=42 mA/mm, V_{ds}=0.8 V, L_{ch}=100 nm) [118]. Note that the output curves showing non-ideal characteristics at low V_{ds} are due to the insulating BN layer sandwiched at the Ni/Te interface. Figure 2.17(b) presents the transfer characteristics of the same device at V_{ds}=0.6 V and 0.8 V, showing decent ON–OFF current ratio (>10^2), comparable to that of BP transistors with 100 nm channel length [119]. Low-temperature ALD Al_2O_3 has a large amount of positive fixed charges in the dielectric and can be used as an n-type dielectric doping layer for p-type 2D Te film [120], [121]. The situation here is even more interesting: The Al_2O_3 capping layer serves as a low work-function material to lift up the Fermi-level in the Te NW and make it an n-type FET. The large drain current obtained on n-type Te-BNNT FET reflects the fact that electron mobility of Te is as high as hole mobility in Te [121].

It is essential to evaluate the channel mobility (μ_{ch}) of Te atomic chains. However, the large contact resistance due to the tunneling resistance of BN layer and general difficult to contact NWs would underestimate the intrinsic mobility (μ) of Te atomic chains. Thus, we need to eliminate the influence of contact resistance (R_c). For FET devices, two techniques can be employed to correct μ. The transfer length measurement (TLM) requires multiple devices of varied L, thus it is only

plausible for large-area samples. On the contrary, the Y-function method (YFM) can be conducted based on individual devices, which is much more suitable for Te-BNNT FETs with short channel [121], [122].

The I_{ds} in linear region could be described as following (Equation 2-1):

$$I_{ds} = \frac{W}{L} C_{ox} \mu_e \left(V_{gs} - V_{th}\right) V_{ds} = \frac{W}{L} C_{ox} \frac{\mu_0}{1+\theta(V_{gs}-V_{th})} \left(V_{gs} - V_{th}\right) V_{ds} \qquad 2\text{-}1$$

The μ_e, μ_0, C_{ox}, V_{th}, W, L, and θ represents the effective mobility in linear regime, the intrinsic mobility, the capacitance between the channel and the gate per unit area, the threshold voltage, the channel width, the channel length, and the mobility attenuation coefficient, respectively, and the Y-function can be defined as Equation 2-2

$$Y - Function = \frac{I_{ds}}{\sqrt{G}} = \sqrt{\frac{W C_{ox} V_{ds} \mu_0}{L}} \cdot \left(V_{gs} - V_{th}\right) \qquad 2\text{-}2$$

where the transconductance G could be described by Equation 2-3

$$G = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{W C_{ox} V_{ds} \mu_0}{L} \frac{1}{\left[1+\theta(V_{gs}-V_{th})\right]^2} \qquad 2\text{-}3$$

Based on the transfer curve at V_{ds}= 0.8 V, we can linear fit the derived quantity Y-function in the sublinear regime of on state (Figure 2.17(d)). From the slope of Y-function, we can extrapolate μ_0 value at V_{ds}=0.8V, which is independent of the attenuating factors, as 1.85 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (Figure 2.17(e)). The mobility attenuation factor θ can be described as Equation 3-4

$$\theta = \theta_{ch} + \theta_c = \theta_{ch} + \mu_0 C_{ox} R_c \frac{W}{L} \qquad 2\text{-}4$$

where θ_{ch}, θ_c, and R_c denote the mobility attenuation factor from the channel, mobility attenuation factor from the contact and the contact resistance, respectively. Assuming that θ_{ch} is negligible, the value of θ is estimated to be 0.007. The corresponding gate-dependent resistance is plotted in Figure 2.17(f), $2R_c$ at high V_g was estimated to be 12 kΩ·μm. This value is much higher than widely studied metal/2D systems, which is supposed to be introduced by the inserted BN layer.

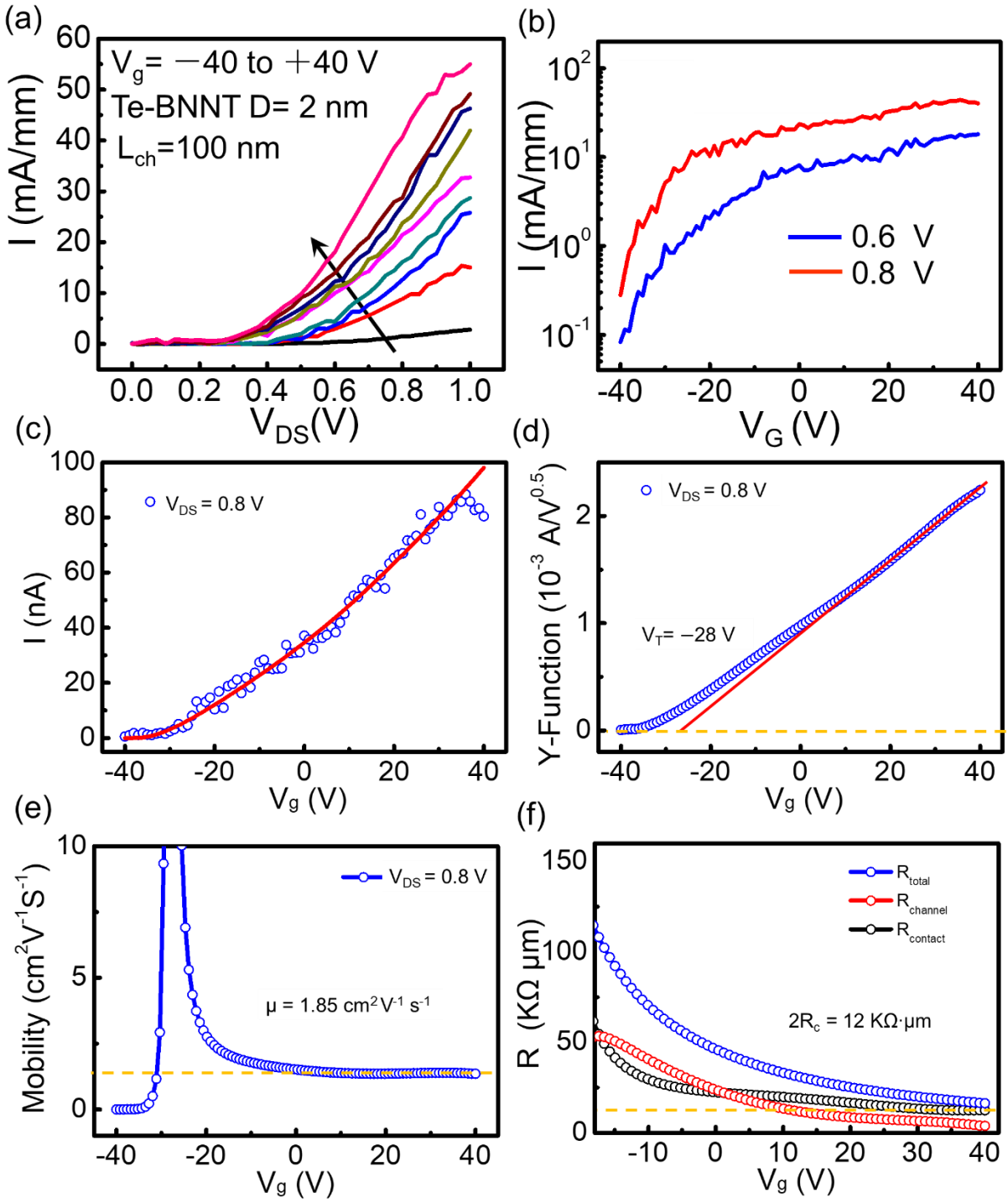

Figure 2.17. Electrical performance of a 2 nm Te-BNNT transistor. (a) Output and (b) transfer curves of the same device. (c) Linear scale of the transfer curve at V_{DS}=0.8 V. (d) Y-function plots of the device. (e) The calculated intrinsic carrier mobility of the Te atomic chains. (f) The gate dependent resistance of the device.

Figure 2.18(a) and (b) illustrate that Te-BNNT devices enable us to extend the electrical performance to 2 nm Te NWs compared to bare Te NW devices where the diameter is limited to 6 nm. As summarized in Figure 2.18(c), Te NWs exhibit excellent carrier mobility larger than ~600 $cm^2 \cdot V^{-1} \cdot s^{-1}$ with a diameter of 25 nm. The reduction of mobility in narrower samples can be ascribed to surface oxidation and defects with a significant increase in surface to volume ratio. The carrier mobility decreases with smaller diameter Te NWs and the average carrier mobility for the smallest 2 nm Te NW is around 1.85 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

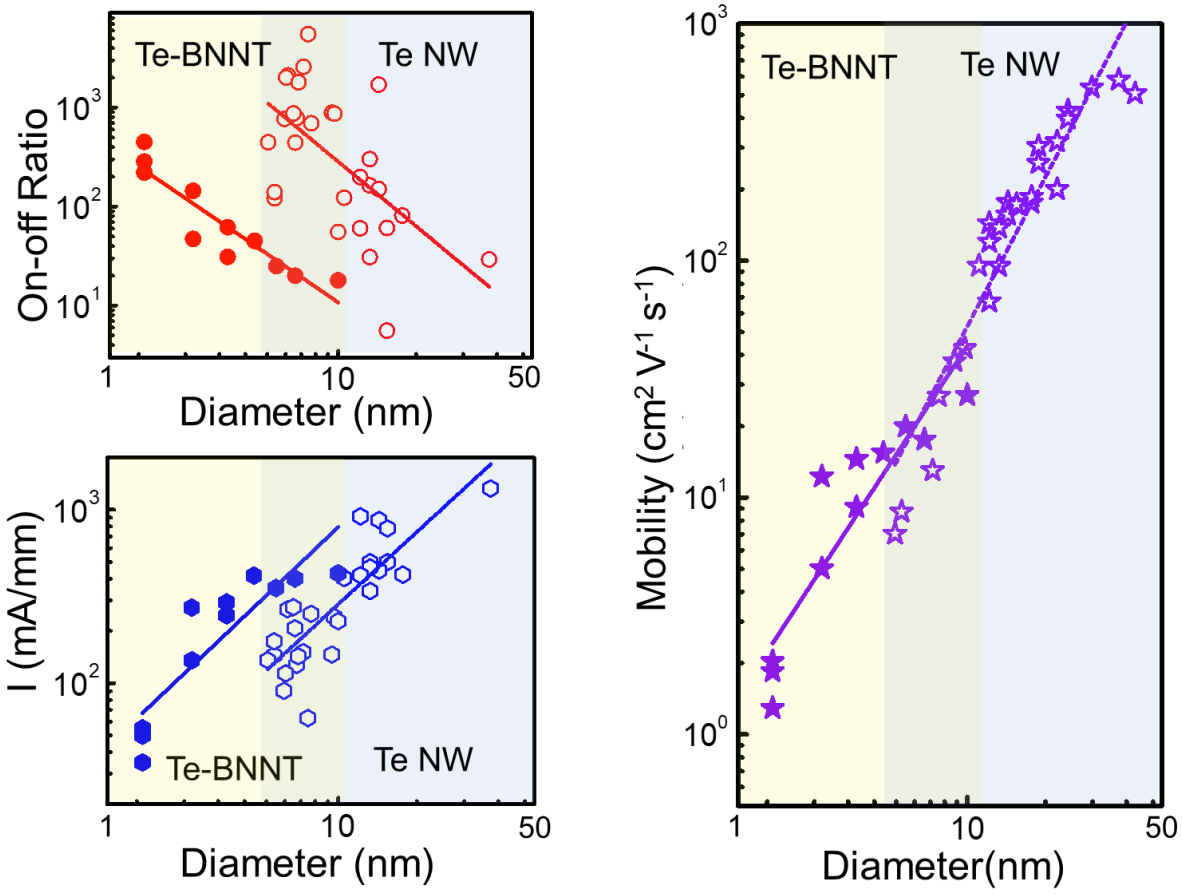

Figure 2.18. Comparison of electrical performance between Te-BNNT and bare Te NW FETs. (a) ON–OFF ratio (b) current density at V_{ds}=1 V and (c) carrier mobility of Te-BNNTs and Te NWs short-channel FETs. The solid signs represent Te-BNNT NW devices and the empty signs represent bare Te NW devices.

3. SELF-HEATING EFFECT ALLEVIATION ON ALD INDIUM OXIDE THROUGH SUBSTRATE SUBSTITUTION

3.1 Introduction to ALD In_2O_3 Transistors

There are several advantages of employing ALD In_2O_3 as the channel material. The followings are some of the important ones. The first is that the fabrication can be back-end-of-line compatible, meaning that the overall thermal budget is low. We will see that it can be as low as around 250–275 ^oC in the following sections. The second is that ALD In_2O_3 transistors have excellent conformality. Figure 3.1 shows that ALD In_2O_3 and HfO_2 can grow on uneven surfaces such as deep trenches and side walls, and the elemental mapping sub-figures show the excellent conformality. The third advantage is that ALD In_2O_3 has precise thickness control. Figure 3.2(a) shows a correspondence between the ALD cycle numbers and resultant In_2O_3 thickness. The thicknesses are confirmed by TEM and AFM. By choosing an appropriate number of ALD cycles, the corresponding thickness of In_2O_3 can be obtained, and the preciseness can be even down to angstrom scale. The fourth is the ultrahigh drain current In_2O_3 transistors can conduct. Figure 3.2(b) shows that the maximum drain current can be up to 2.5 mA/μm at only 0.7 V of drain bias with a back-gate structure.

Nevertheless, although TG devices are particularly desired for practical applications, the explorations of In_2O_3 FETs mostly focus on back-gated structure due to the challenges of defect induction during the formation of the high-k TG dielectric and severe SHE with high power density (PD). The former fortunately can be partly resolved by low temperature ALD of the TG dielectric followed by a rapid thermal annealing (RTA) treatment in O_2 environment while the latter remains as a bottleneck.

For the former, it is reported that by lowering the growth temperature of the ALD HfO_2 dielectric stack from 200 ^oC to 120 ^oC and annealing the devices in O_2 environment, the switching behavior can be recovered [78]. As shown in Figure 3.3(a), with 200 ^oC growth temperature, it is not recoverable despite of the annealing conditions. On the other hand, with 120 ^oC growth environment, great switching behaviors can be performed with an O_2 annealing treatment as indicated in Figure 3.3(b). It is proposed [78] that the formation of HfO_2 likely fetches oxygen not only from the H_2O precursor but also from the In_2O_3 layer, generating huge amount of oxygen defects at the interface. By lowering the growth temperature, the interaction between HfO_2 and

In_2O_3 is minimized, and an annealing treatment in O_2 atmosphere also assists to eliminate the oxygen vacancies. Therefore, this strategy is able to partially address the issue.

For the latter, SHE happens when the power density of the device is too high. As larger V_{DS} is applied, the I_D increase accordingly. Nevertheless, huge amount of thermal energy is generated with the increased power, which is calculated as the product of I_D and V_{DS}. If the heat can be transferred or dissipated efficiently enough, the temperature at the In_2O_3 channel will elevate drastically. The local high temperature will then damage the channel material itself, the dielectric layer above it, and even their interface. This phenomenon is consequently called self-heating effect. In addition, the high channel temperature might even result in the damage of the gate dielectric and the diminish of the long-term reliability [124], [125]. To address it, thermal engineering which has been applied to other materials [126]–[128] might be a solid solution. Therefore, thermal management will be utilized and discussed in this chapter. Besides, more methods and techniques will be applied to help on heat transfer or self-heating avoidance in the following chapters.

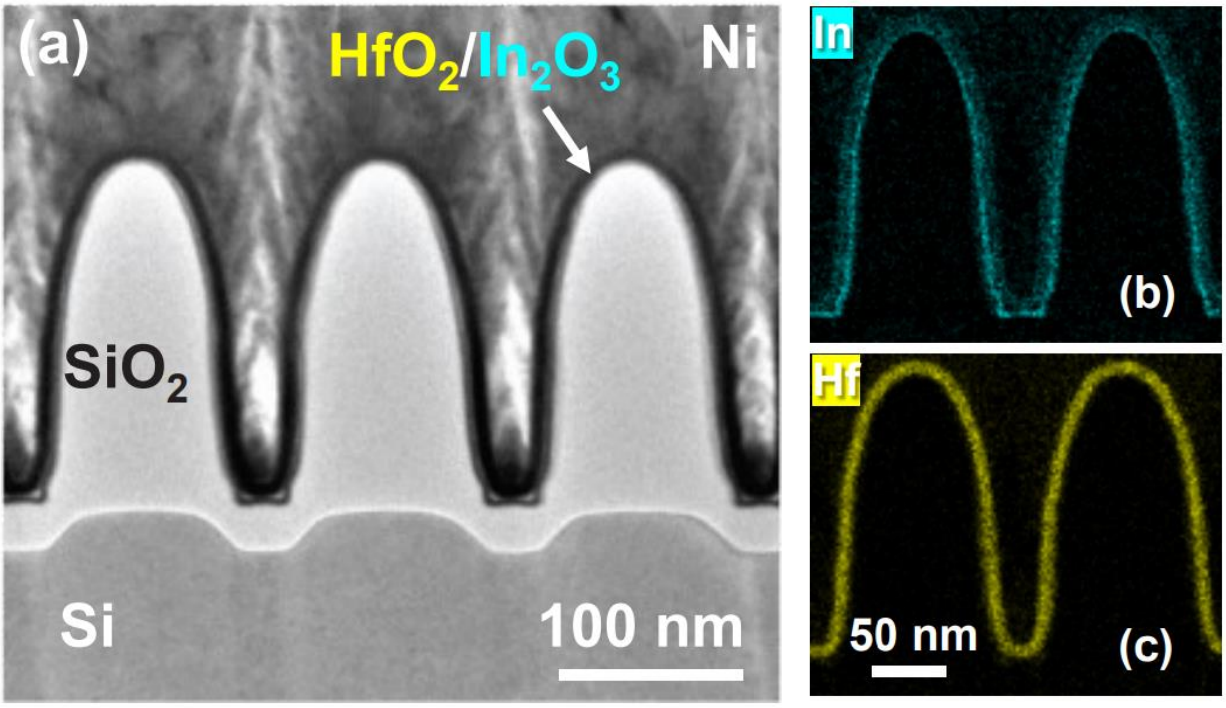

Figure 3.1. (a) A TEM image demonstrating ALD In_2O_3 and HfO_2 grown on uneven surfaces. (b, c) EDX mapping of In and Hf with HAADF STEM, showing conformal growth by ALD.

We first begin with ultrathin In_2O_3 thickness of 1.3 nm, and relatively thicker devices will be covered in the following chapters. Here, we realized ALD-based TG In_2O_3 transistors achieving ID as high as 2 A/mm by employing highly resistive silicon substrate to minimize SHE. In the previous exploration [64]–[66], silicon dioxide on silicon (SiO_2/Si) is usually chosen as the substrate due to its insulating property and vast commercial availability. Nevertheless, the thermal conductivity of silicon (κ = 142 $W \cdot m^{-1} \cdot K^{-1}$) [129] is approximately 100 times higher than SiO_2 (κ = 1.1 $W \cdot m^{-1} \cdot K^{-1}$) [130], implying that the generated heat can be dissipated much more efficiently from the bottom as silicon serves as the substrate. In this case, we utilize highly resistive silicon (resistivity ~ 10^5 $\Omega \cdot$cm) to block the leakage current through the substrate. Additionally, to estimate and compare the rough temperature of the channel with different substrates as certain amount of current flows through, we measure the regression of the transconductance (g_m) of In_2O_3 TG transistors from room temperature to 160 ^oC as an approximate channel thermometer [131]–[133]. It is revealed that the In_2O_3 on SiO_2 is already heated up to 140 ^oC locally when the silicon devices are still under 40 ^oC. The enormous thermal conductivity difference benefits the realization of scaled TG In_2O_3 transistors with high current carrying capacity up to a maximum I_D of 2 A/mm.

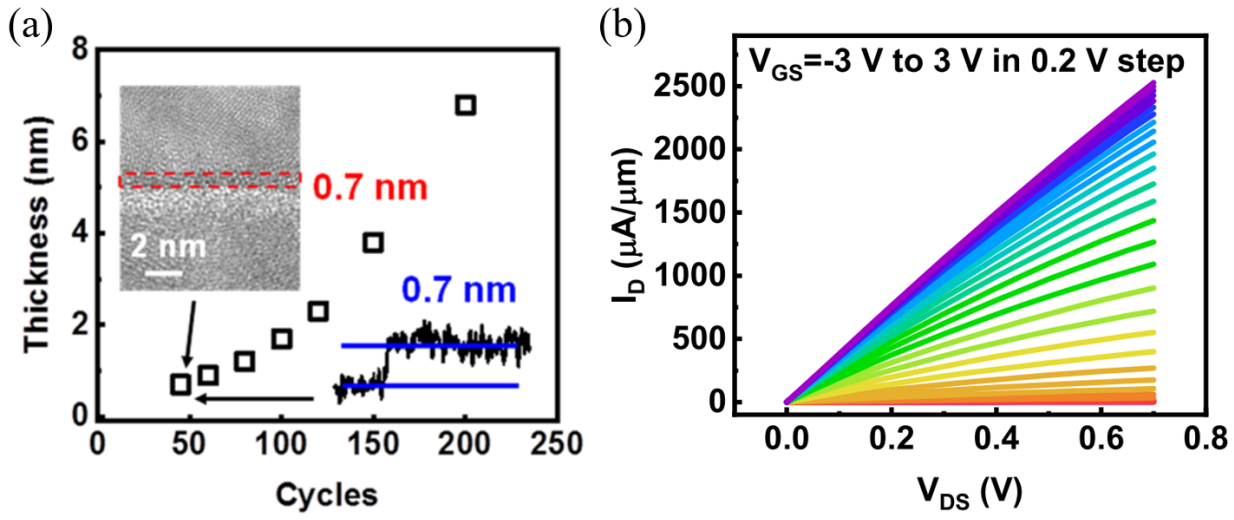

Figure 3.2. (a) Correspondence between ALD cycle numbers and the resultant In_2O_3 thickness, showing precise thickness control down to angstrom scale. (b) High current of 2.5 mA/μm conducting through ALD In_2O_3 transistors with back-gate structures at V_{DS} of 0.7 V.

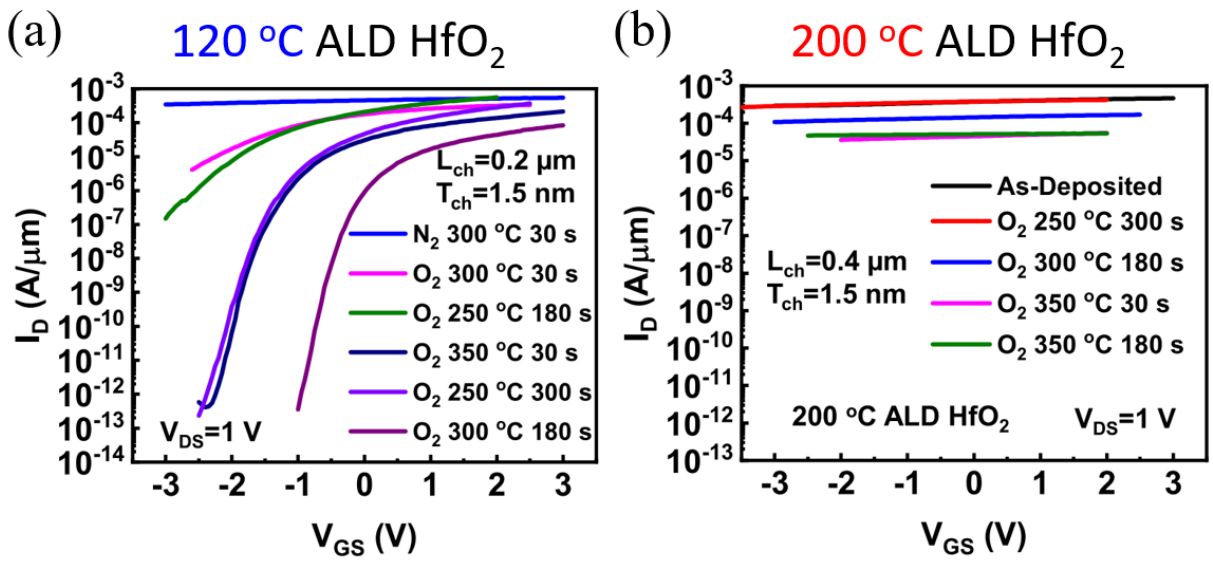

Figure 3.3. Switching behaviors recovery in TG In_2O_3 transistors through low temperature ALD HfO_2 growth followed by an annealing treatment in O_2 environment. (a) Recoverable with 120 °C ALD HfO_2 and (b) Unrecoverable with 200 °C ALD HfO_2.

3.2 Device Fabrication

Figure 3.4 illustrates the schematic view of a TG In_2O_3 transistor and the workflow of the fabrication. From bottom to top, the stacks are substrate (either 90-nm thermally grown SiO_2 on silicon or highly resistive silicon), isolated In_2O_3 channel with thickness of 1.3 nm, 45-nm Ni serving as source and drain metal contacts, 6-nm HfO_2 of gate dielectric, and 50-nm Ni acting as top gate metal electrode.

Standard solvent cleaning steps are followed before the substrates are used in the device fabrication process. 1.3 nm of In_2O_3 thin film is deposited by ALD at 225 °C with trimethylindium (TMIn) and H_2O as the In and O precursors, respectively, on the pre-cleaned substrates. The as-deposited In_2O_3 thin film is isolated through a dry-etch process with Ar/SF_6 plasma under room temperature. Then, 45-nm Ni as source and drain contacts are defined with variant L_{ch} by e-beam lithography, e-beam evaporation, and a lift-off process. On top of them, 6-nm HfO_2 is conformally formed by ALD at 120 °C with $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as the Hf and O precursors, respectively. The relatively low-temperature is chosen to minimize the interaction between In_2O_3 and the growth of HfO_2 to preserve the intrinsic properties of the channel semiconducting material

[78], and dedicated ALD chambers are employed in order to prevent cross-contamination of In_2O_3 and HfO_2 deposition. 50-nm Ni served as top gate electrode is formed in the same way as source and drain contacts. Last, the devices are treated with rapid thermal annealing (RTA) under O_2 environment at 200 ^oC for 2 minutes to reduce the oxygen vacancies in the In_2O_3 channel induced by the ALD growth process of HfO_2 [78]. The whole fabrication process requires thermal budget as low as 225 ^oC which is for the formation of atomic-layer-thin In_2O_3 channel.

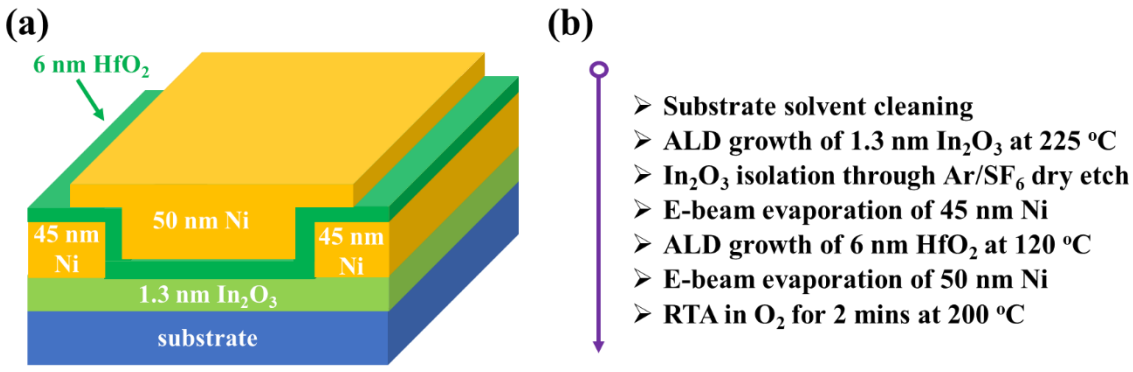

Figure 3.4. (a) Schematic illustration and (b) workflow of the fabrication process of a TG In_2O_3 transistor. The substrate is either 90-nm thermally grown SiO_2 on silicon or highly resistive silicon (resistivity ~ 10^5 Ω·cm).

3.3 High Current Density and Low Contact Resistance

Figure 3.5(a) exhibits the output characteristics of a representative TG In_2O_3 transistor with L_{ch} of 600 nm, T_{ch} of 1.3 nm, W_{ch} of 2 μm, 6-nm HfO_2 as the top gate dielectric, SiO_2/Si as the substrate, and annealed at 200 ^oC in O_2 environment. It exhibits decent current saturation and gate modulation. Figure 3.5(b) illustrates the output behavior of a transistor with L_{ch} of 40 nm. The top gate voltage (V_G) sweeps from -4 V to 4 V with a 0.5 V step, and the maximum I_D achieves 991 mA/mm at V_G of 4 V and drain voltage (V_D) of 1 V, which surpasses the highest reported value of 570 mA/mm for TG In_2O_3 transistors [128] to the best of our knowledge. For the devices with L_{ch} of 60 and 40 nm, the maximum I_D of them are 405 and 660 mA/mm, respectively, at V_G of 4 V and V_D of 1 V (Figure 3.5(c) and (d)).

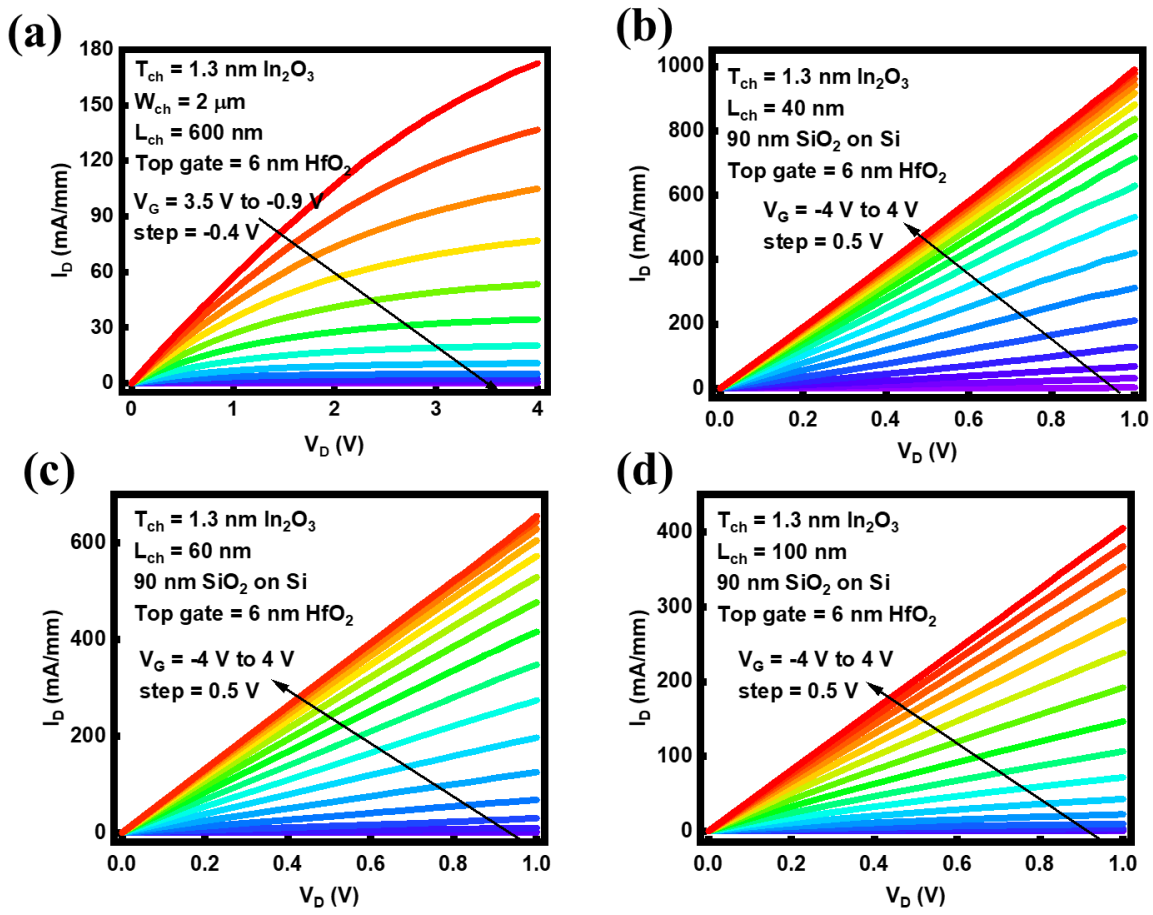

Figure 3.5. Output characteristic of TG In_2O_3 transistors with L_{ch} of (a) 600 nm, (b) 40 nm, (c) 60 nm, and (d) 100 nm.

Figure 3.6(a) and (b) presents the transfer characteristics, showing ON–OFF ratio of almost 4 to more than 6 orders with variant L_{ch} from 100 nm down to 40 nm in logarithmic and linear scale, respectively. The gate leakage current is illustrated and much smaller than the drain current. Some key parameters are extracted as follows, threshold voltage (V_T) being -1.1, -1.8, and -2.5 V, subthreshold swing being 344, 433, and 577 mV/dec for L_{ch} of 100, 60, and 40 nm, respectively, and field-effect mobility (μ_{FE}) being 4.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

It is noticeable that the I_D of the transistors at V_G of 4 V and VD of 1 V is roughly proportional to the inverse of the L_{ch}, indicating that a) the semiconducting In_2O_3 channel can be nicely scaled and b) most of the resistance is contributed by the channel, that is, contact resistance (R_C) is reasonably low. To further explore the R_C of TG In_2O_3 devices at on-state, the total resistances (R_{total}) with different L_{ch} and V_G from 4 V to 1 V are extracted and arranged into Figure 3.6(c) where R_{total} is consist of a) $2R_C$ designated to the contacts between the semiconducting channel and source/drain metal and b) sheet resistance (R_{sh}) contributed by the channel material and proportional to the L_{ch}. In each case of V_G, the extracted data points are in superb linear fashion, and therefore, the R_C is accordingly obtained by extrapolation with a traditional transfer length method (TLM) method [134]. The y-axis intersection with the extrapolated regression line is regarded as $2R_C$. Figure 3.6(d) illustrates the acquired R_C under different V_G with a largest value of 0.24 Ω·mm at V_G of 4 V, which is still lower than the reported value of 0.36 Ω·mm [30] with a BG structure. The low RC value implies that the In_2O_3 channel and the Ni source/drain are of good contact in the TG structure.

Even though TG In_2O_3 devices with SiO_2/Si substrates manifest I_D of roughly 1 A/mm, it is not able to achieve even higher as the BG transistors showing up to 2.2 A/mm [66]. Figure 3.7(a) reveals the difficulties as a larger V_D is applied. Noticeably, the curves of I_D start to saturate and then degrade while V_D of 1.25 V is kept applied with variant V_G swept, which is mostly ascribed to the SHE. As manifested in Figure 3.7(b), large amount of heat could be generated when large current passes through the ultrathin In_2O_3 channel. Nevertheless, the device is not capable to dissipate the created thermal energy efficiently when SiO_2/Si serves as the substrate, causing dramatical elevation of the local temperature and the damage of the In_2O_3 channel. Under certain condition, the transistors no longer behave well and are even unrecoverable.

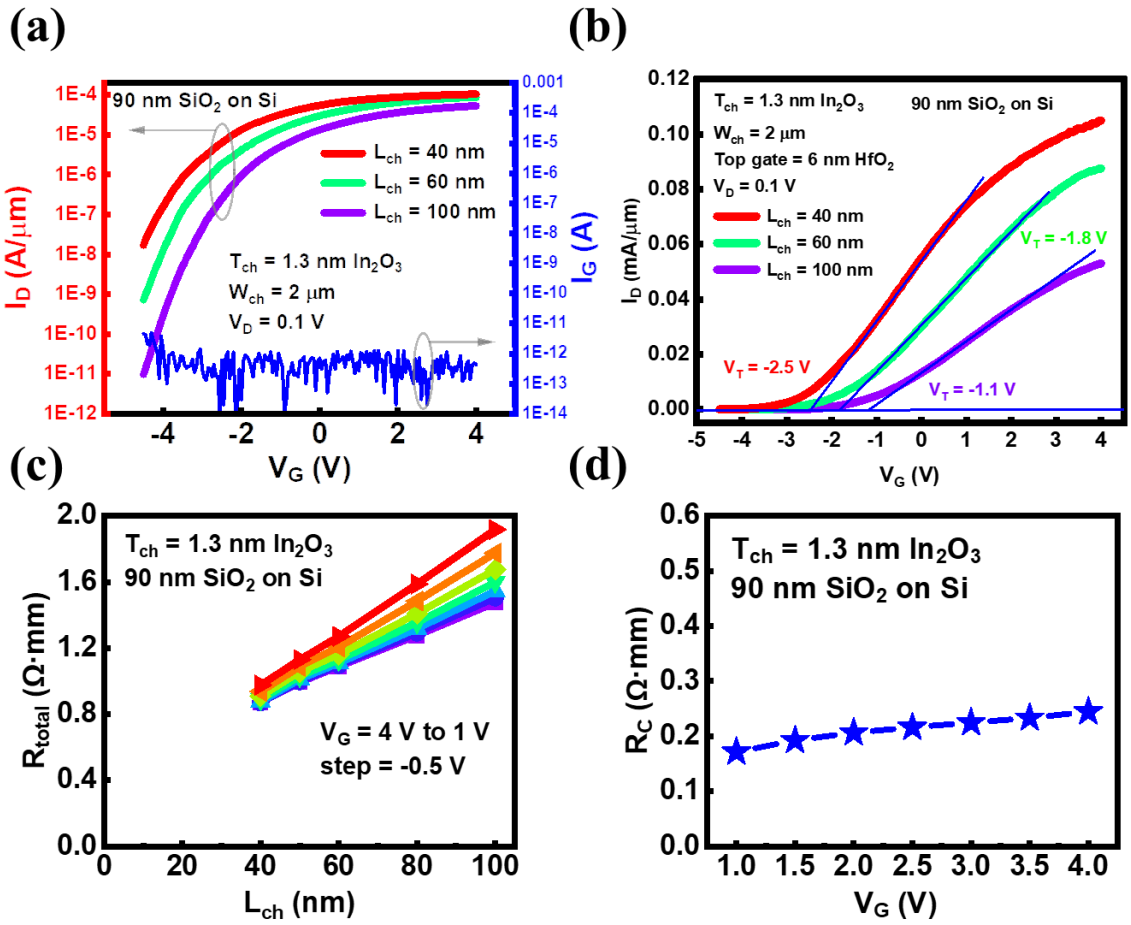

Figure 3.6. (a, b) Output characteristics of a TG In_2O_3 transistor with SiO_2/Si substrate and L_{ch} of 40 nm in (a) logarithmic and (b) linear scale. (c) The total resistance of the devices with variant L_{ch} at on-state for TLM extraction. (d) The extracted R_C values from (c) showing great contact between the In_2O_3 channel and the source/drain contacts.

To further investigate the SHE, larger V_D of 1.8 V is applied to 2 devices with one sweeping the V_G from low to high and the other one from high to low as exhibited in Figure 3.7(c) and (d), respectively. The 2 situations reveal completely different results. Observably, in Figure 3.7(c), the current degradation becomes more and more critical over the sweeps of larger V_G. The curves are entirely in unexpected situation, and the behavior becomes extremely unstable due to the severe SHE. The red color is chosen and utilized to illustrate the high-temperature condition. On the other hand, in Figure 3.7(d), even the first curve already reveals poor performance with V_G of 4 V applied first. After the first measurement and thermal stress, the device is degraded significantly

or partly damaged. All the following measurements show the underscored performance. The limited capability of heat dissipation of the devices restricts themselves from broader applications.

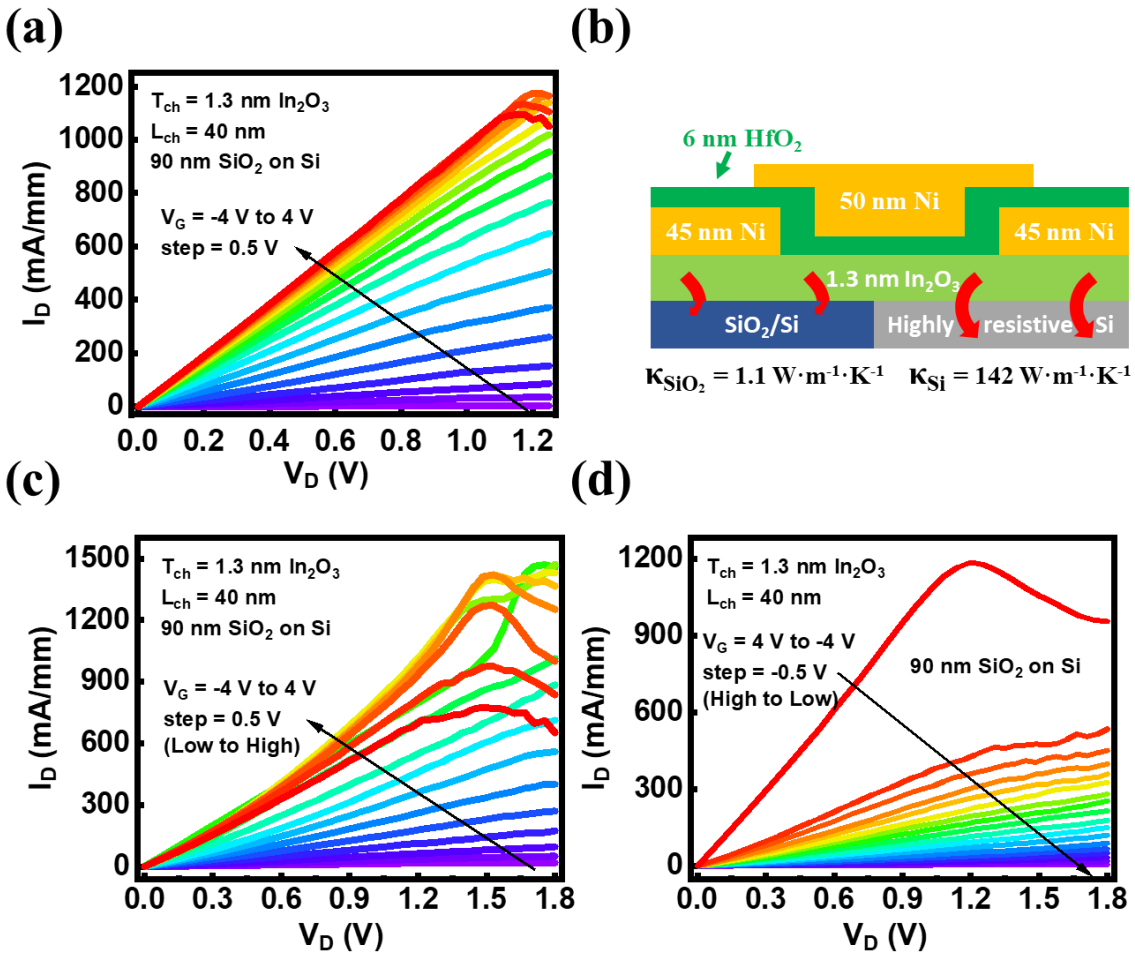

Figure 3.7. (a) Degraded I_D curves of a TG In_2O_3 transistor with SiO_2/Si substrate and a large V_D up to 1.25 V, revealing the SHE. (b) Cross-sectional exhibition of the heat dissipation of In_2O_3 devices with different substrates. Silicon with around 100 times higher thermal conductivity is able to passivate the generated thermal energy much more efficiently. Drastically degenerated and extremely chaotic I_D–V_D curves with VG sweeping (c) from low to high and (d) from high to low. The totally different behaviors imply that SHE is dominating over the transport performance.

3.4 Thermal Engineering with Highly Resistive Silicon Substrate

To address this thermal issue, a thermal management method is adopted. Highly resistive silicon (resistivity ~ 10^5 Ω·cm) is used to replace the SiO_2/Si substrate to assist dissipating the generated thermal energy as large current is conducted. Silicon is chosen because of its much higher thermal conductivity of 142 $W \cdot m^{-1} \cdot K^{-1}$ [129] compared with that of SiO_2 (1.1 $W \cdot m^{-1} \cdot K^{-1}$ [130]), the widely commercial availability, and the great affordability. Figure 3.8(a) illustrates the output characteristics of a TG In_2O_3 device with highly resistive silicon as the substrate, the same L_{ch} of 40 nm, T_{ch} of 1.3 nm, 6-nm of HfO_2 as the top gate dielectric, and 200 ^oC RTA in O_2 environment. The only difference is the different substrate in operation. Even with V_D of 2 V applied, the created heat can be majorly dissipated ascribed to the high thermal conductivity of silicon. Consequently, the critical SHE is considerably mitigated, and the device achieves a much higher I_D of 2 A/mm at V_D of 2 V and V_G of 4 V. The 2 A/mm value is around 100 % higher than that of 0.99 A/mm with SiO_2/Si substrate.

Figure 3.8(b) exhibits the transfer characteristics of the device. It performs roughly 3 orders of ON–OFF ratio, which is similar to that of SiO_2/Si in Figure 3.4(a). To compare the SHE in the two cases, alike Figure 3.7(c) and (d), V_D of 1.8 V is applied to two In_2O_3 transistors with one sweeping the V_G from low to high and the other one from high to low. In Figure 3.8(c), decent output curves are behaved. Unlike Figure 3.7(c) exhibiting the dramatical current descent, Figure 3.8(c) shows much healed SHE only with the upmost two curves being close. Similarly, in Figure 3.8(d), even though the difference between the topmost 2 curves is a little larger, the severe SHE is greatly eliminated compared with Figure 3.7(d) whose I_D degrades drastically within and after the 1st curve. With the huge discrepancies between Figure 3.8(c) and (d) and Figure 3.7(c) and (d), it is a direct and unambiguous evidence that substituting the SiO_2/Si substrate with highly resistive silicon in TG In_2O_3 transistors largely reduces the SHE and observably benefits its transport performance.

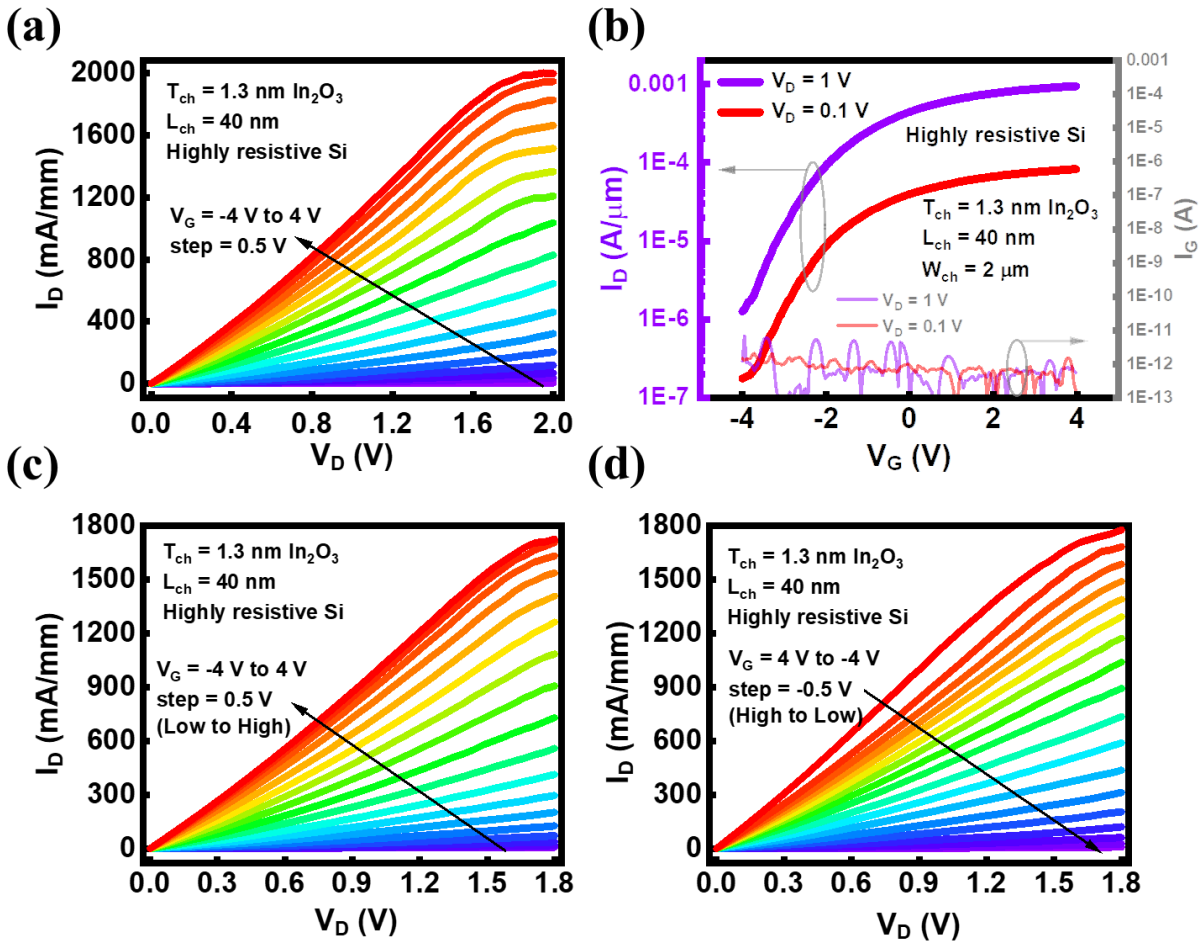

Figure 3.8. (a) Output and (b) transfer characteristics of TG In_2O_3 transistors with highly resistive silicon substrate and L_{ch} of 40 nm. Cured I_D–V_D curves with V_G sweeping (c) from low to high and (d) from high to low.

In order to further quantitatively explore the SHE on the TG In_2O_3 device behavior, the current conducted through the transistors at on-state with the two different substrates are measured 10 times in a row. Because of the SHE, the local temperature at the In_2O_3 channel will increase after each measurement and degrade the channel mobility and contacts, which leads to the performance degradation in the following measurements. The same dimensional parameters of 40-nm L_{ch}, 1.3-nm T_{ch}, and 6-nm HfO_2 are employed, and V_G of 4 V is chosen to ensure the entire experimental setup to be the same. Figure 3.9(a)–(d) illustrates the 10 collections of I_D curves with SiO_2/Si substrate and variant V_D applied where individual transistors with the same structure are employed in each subfigure. The V_D in Figure 3.9(a) is only 0.5 V, and all the 10 curves overlap with each other, meaning that no SHE takes place. The V_D in Figure 3.9(b) is elevated to 0.8 V,

and the curves start to decrease one time after another with around 9 % reduction in the 10^{th} test compared to the 1^{st}. The VD applied in Figure 3.9(c) is further enlarged to 1.0 V, and the distinctions between the curves become more obvious, indicating that SHE is deteriorating the electric behavior. The V_D in Figure 3.9(d) is up to 1.8 V, and the curve in the 1^{st} collection is already awful, specifying the acute SHE. Moreover, the current degrades radically in the following measurements, and the I_D is decreased by approximately 77 % compared the 1^{st} collection with the 10^{th}.

It is observable that the few topmost curves in this figure are principally similar to the ones in Figure 3.7(d), implying that the SHE partly damages the device permanently as large V_G is applied first. Besides, it also verifies the reproducibility of the experiments and the consistency of the setup and devices. In great contrast to Figure 3.9(d) and (e) illustrates V_D of 1.8 V with silicon as the substrate. Observably, the SHE is mostly cured, and only a little degradation is remained. The current deterioration between the 1^{st} and the 10^{th} measurement is only 7.5 % which is even better than the case of V_D of 0.8 V with SiO_2/Si. The comparison of the degeneration over the 10 collections between the two different substrates is arranged to Figure 3.9(f), and the descending rate of highly resistive silicon substrate devices is less than 10 % of the SiO_2/Si ones. The satisfactory capacity of heat dissipation of silicon considerably alleviates the serious SHE suffering SiO_2 and profits the exceptional I_D of 2 A/mm for TG In_2O_3 devices.

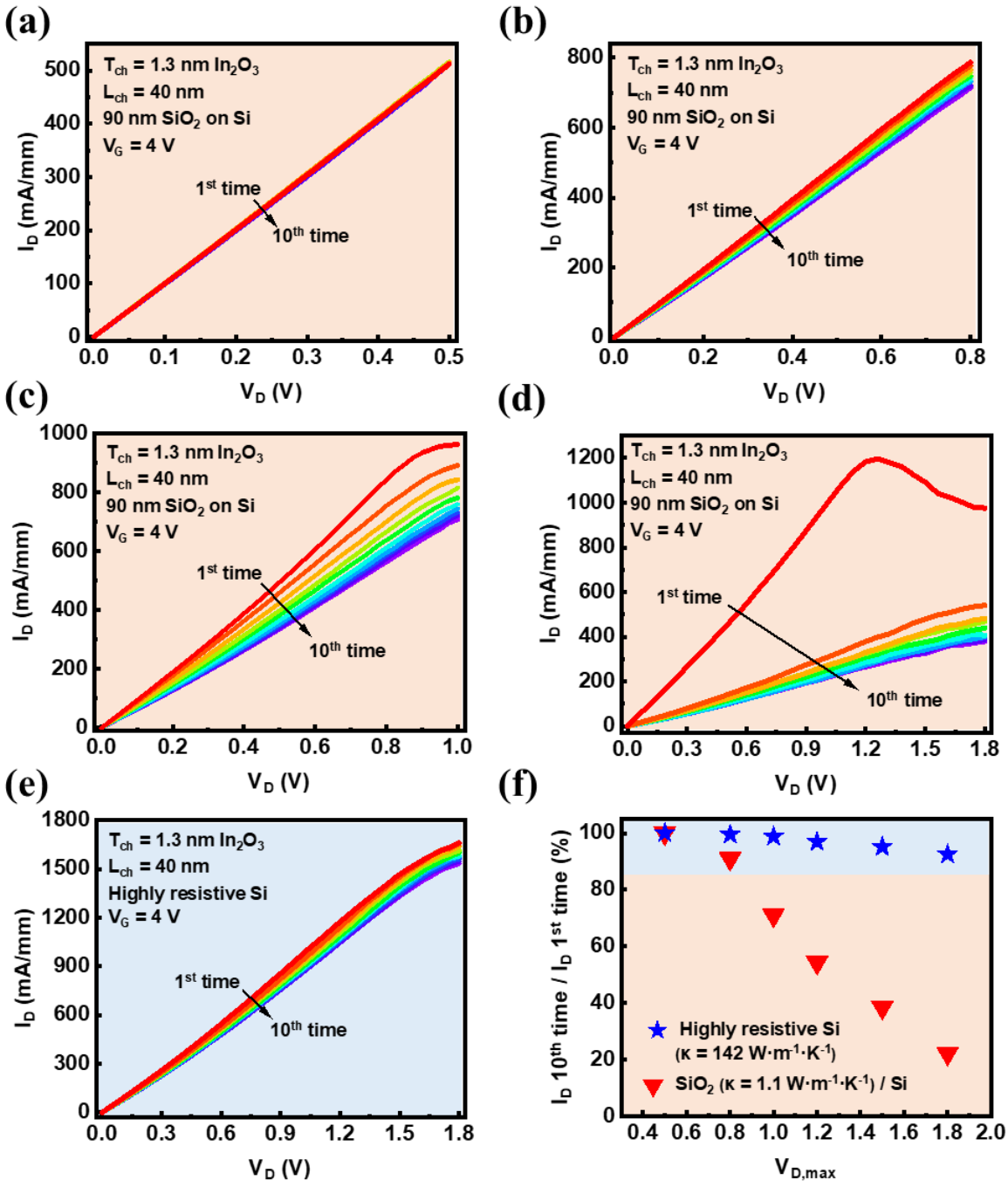

Figure 3.9. I_D–V_D measurement of TG In_2O_3 transistors with (a) V_D up to 0.5 V and SiO_2/Si substrate, (b) V_D up to 0.8 V and SiO_2/Si substrate, (c) V_D up to 1 V and SiO_2/Si substrate, (d) V_D up to 1.8 V and SiO_2/Si substrate, and (e) V_D up to 1.8 V and highly resistive silicon substrate 10 times in a row. (f) The I_D preservation percentage between the 1st and 10th measurement with different V_D and substrates.

Besides, to roughly estimate the local temperature of the In_2O_3 channel as operating at on-state in a quantitative way, the changes of the transconductance (g_m) under variant chuck temperature up to 160 ^oC are statistically investigated with SiO_2/Si serving as the substrate [131]–[133]. The gm values here are extracted from I_D–V_G measurements at V_G around 4 V. A long L_{ch} of 1 μm and a low V_D of 50 mV are chosen to minimize the produced heat by the devices during the measurements. It is shown previously in Figure 3.9(a) and discussed above that the SHE at V_D of 500 mV is already negligible and causes no degradation in the experiments. Therefore, V_D of 50 mV is more than safe to be utilized in the g_m measurements. In Figure 3.10, each data point is calculated from at least 5 devices through dividing the average gm with the certain chuck temperature by the g_m at that of 20 ^oC, and a minimum of 5 minutes are allowed after the environmental temperature becomes stable to ensure the preciseness. The error bars indicate 95 % confidence interval. Noticeably, the gm of the TG In_2O_3 transistors degrades relatively slowly before 80 ^oC, and 90 % or more of the g_m is preserved within this range. On the other hand, it decreases substantially after 100 ^oC, and only 35 % is left at 160 ^oC. Applying this effect as a rough channel thermometer, the local temperature at the channel is less than 40 ^oC at 1.8-volt-measurements at V_G of 4 V on silicon substrate as shown in Figure 3.8(e) and based on the estimation of Figure 3.9; while it reduces to roughly 1 A/mm (I_D at V_D=1.8V of the first measurement in Figure 3.9(d)) from 1.8 A/mm (I_D at V_D=1.8V on silicon in Figure 3.7(d)). 45% reduction in g_m and I_D refers 140 ^oC device temperature from Figure 3.10, which is significant. The evidential contrast specifies that the thermal engineering methodology does benefit the improved performance of the In_2O_3 TG transistors.

For high power density devices in general, substrates with even higher thermal conductivity might be desired. For instance, it is revealed that diamond (κ = 2,000–2,200 $W \cdot m^{-1} \cdot K^{-1}$ [128, 135]) as a substrate is capable of further profiting the performance of β-Ga_2O_3-based power devices [128]. Nevertheless, the transparent body of diamond upraises the fabrication difficulties to a great extent, and its narrower commercial availability and much poorer affordability compared with a wide variety of silicon restrict it from mass production. With moderate power density, TG In_2O_3 transistors with highly resistive silicon substrate are sufficient enough for dissipating the produced heat efficiently to avoid self-heating as previously presented and discussed, which makes it much more competitive in the realistic implementation and qualifies it in practical applications. For

BEOL-compatible monolithic 3D integration, high thermal conductive interlayer material is obviously desired for addressing thermal management issues.

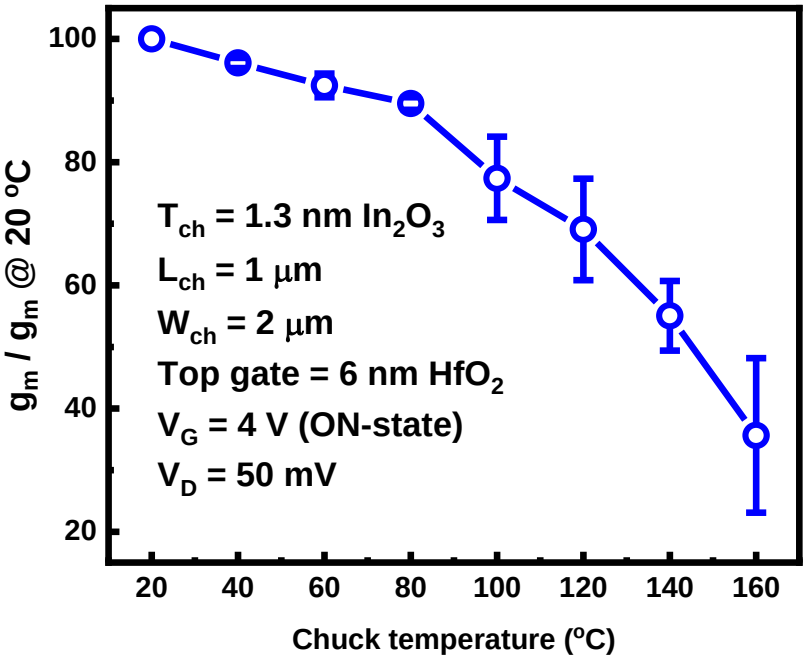

Figure 3.10. g_m regression of TG In_2O_3 devices with long channels of 1 μm, low V_D of 50 mV, and ascending temperature up to 160 °C as an approximate channel thermometer.

4. SELF-HEATING EFFECT VISUALIZATION THROUGH THERMO-REFLECTANCE IMAGING TECHNIQUE

4.1 Motivations

In chapter 3, self-heating effect mitigation through substrate substitution is introduced. By utilizing highly resistive silicon as the substrate to replace the original SiO_2/Si substrate, the temperature increase is largely decreased. Through measuring the transconductance under variant temperature environment and observing the transconductance reduction of the devices as they are self-heating, the temperature increase at the channel can be roughly estimated.

However, this quantitative estimation is in some degree too rough and not intuitive. Moreover, the transconductance reduction may depend many factors such as channel thickness, channel length, *etc*. This greatly limits the universality of its use. Besides, we can only have a rough estimation of the temperature at the channel instead of observing the temperature distribution across the whole area by this method. Therefore, a technique which can be more universally applied and utilized to demonstrate the temperature change distribution of the devices when self-heating effect happens is much more desired.

Accordingly, in this chapter, we are going to introduce a thermo-reflectance (TR) equipment with high spatial resolution, which fulfills the aforementioned requirements, to visualize the SHE of TG In_2O_3 transistors. Moreover, to verify its accuracy, we will also perform heat transfer simulation which adopts a finite-element method. The TR experimental results and the simulation outcomes are in excellent agreement and support each other. Greater details are shown in the following sections.

4.2 Equipment Setup and Mechanism

To quantitively investigate and address the SHE, a high-resolution TR measurement system is introduced with the setup illustrated in Figure 4.1. In this figure, the lower right part shows the device under test which is a TG ALD In2O3 transistor. During the measurement, V_{DS} pulses are applied to the device as shown in the green square at the bottom left part. There is another supplier which provides constant gate-to-source (V_{GS}) bias to the device. Besides, a high-speed LED pulses illuminate the device as shown at the upper right part. The reflectance signals, which contains its

temperature information, will be captured by a charge coupled (CCD) camera. The CCD camera is synchronized with the VDS pulses by a center control.

Figure 4.2 shows its working mechanism in time domain. The lower green curve presents the V_{DS} pulse that is applied to the device. The brown curve above it shows the surface reflectance change with time. This signal is directly related with its temperature. Therefore, at the start of the V_{DS} pulse, the device is turned ON and therefore self-heat-up due to the SHE. After a short period of time, the steady-state is reached. We will then capture an image as an active image as shown in the red curve. And then, after the V_{DS} pulses ends, the device is turned OFF and therefore naturally cool-down. Similarly, after a short period of time, the steady-state that is the ambient temperature is reached. Then we will capture another image which is a passive image as shown in the blue curve. Then, the difference between the active and passive images will be calculated. This process will be repeated numerous times, and the difference image will be averaged accordingly to maximize the signal-to-noise (STN) ratio. The averaged difference image includes the reflectance difference with the green LED. Therefore, it is then transformed into a final delta T image through dividing by the thermal coefficient of the surface material ($C_{TH} = -5\times10^{-5}\ K^{-1}$) and calibration to obtain the final thermal image [136].

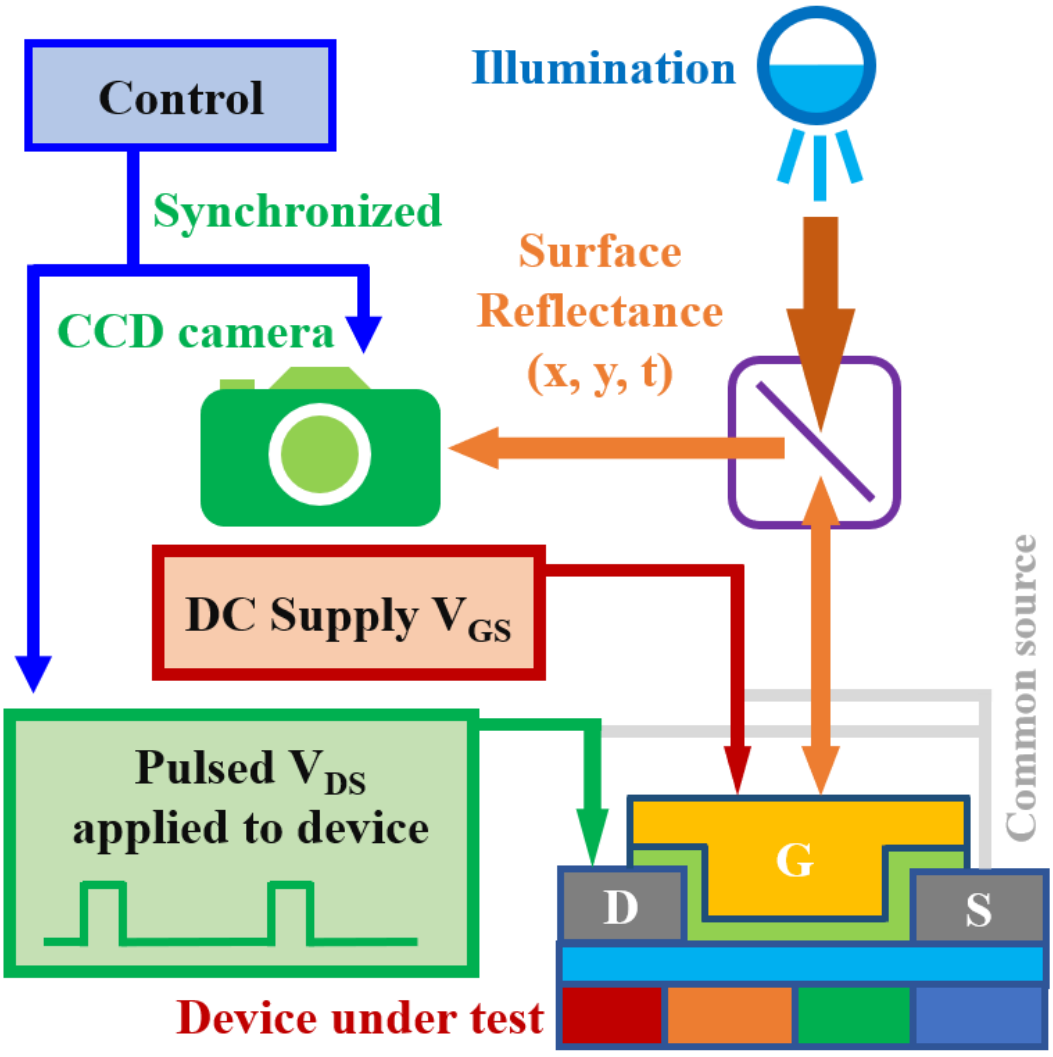

Figure 4.1. Schematic illustration of the high-resolution thermo-reflectance (TR) imaging system setup.

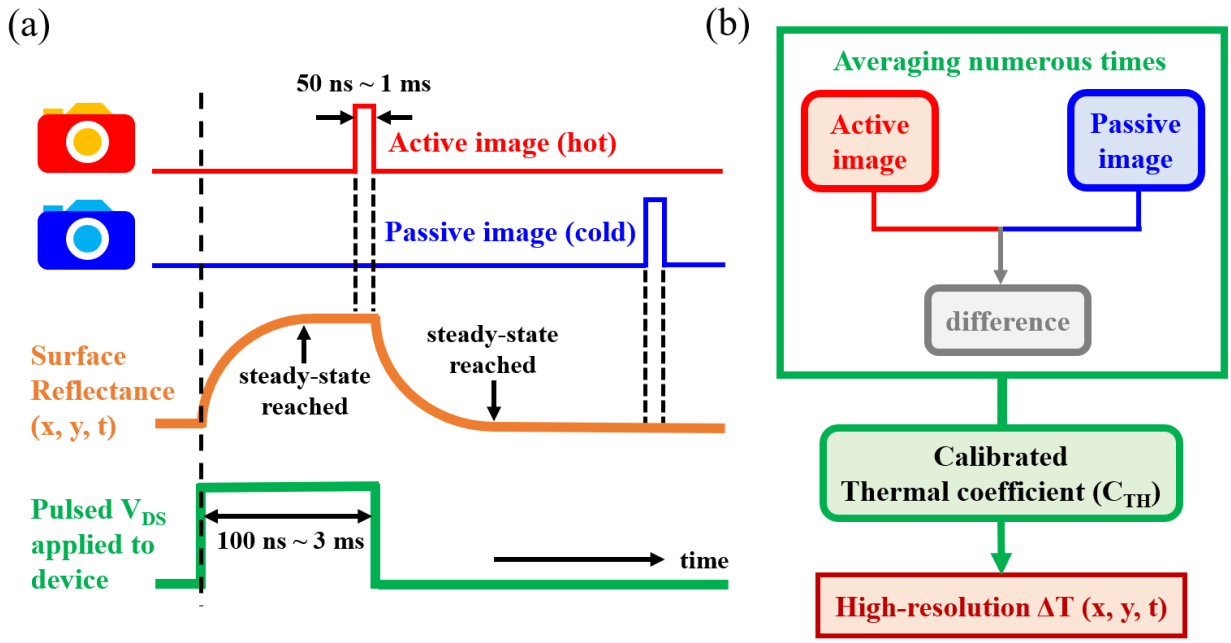

Figure 4.2. (a) Working mechanism of the high-resolution TR imaging equipment in time domain. (b) Transformation from TR signal to a temperature scale.

4.3 Thermo-Reflectance Measurement

Beside SiO_2/Si and HR Si substrate, in this chapter a third kind of substrate of sapphire is utilized as well to have a clearer comparison. Sapphire has a thermal conductivity of 40 $W \cdot m^{-1} \cdot K^{-1}$, which is in between the SiO2 and Si. All the devices under test have the same L_{ch} of 400 nm and W_{ch} of 2 µm, and the only difference between them is the substrate underneath.

Figure 4.3(a)–(c) manifest the channel region of steady-state ΔT of TG In_2O_3 devices with SiO_2/Si substrate at power density of 2.44 kW/mm^2, sapphire substrate at 2.65 kW/mm^2, and HR Si substrate at 3.00 kW/mm^2, respectively. The In_2O_3 transistors have the same structure except for the different substrates in use as mentioned, and the power density is calculated by 4-1:

$$Power\ density\ (PD) = \frac{I_D \times V_{DS}}{W_{ch} \times L_{ch}} \qquad 4\text{-}1$$

The results show a clear correlation between increasing thermal conductivity of the substrate material and decreasing ΔT (κ_{SiO_2} / κ_{sap} / κ_{Si} = 1.1 / 40 / 142 $W \cdot m^{-1} \cdot K^{-1}$ [129, 130, 137]). In Figure 4.3(a), devices with PD of 2.44 kW/mm^2 on a SiO_2/Si substrate perform maximum ΔT up to 50 K. In contrast, Figure 4.3(b) illustrates that devices on a sapphire substrate show much lower ΔT of

around 20 K even with slight larger PD of 2.65 kW/mm^2. Furthermore, with a HR Si substrate as demonstrated in Figure 4.3 (c), the devices exhibit even lower ΔT of roughly 10 K with even larger PD of 3.00 kW/mm^2. The reason is that a substrate material with better thermal conduction is able to dissipate the generated heat more efficiently. The cross-sections of Figure 4.3(a)–(c) are normalized by power density and plotted in Figure 4.3(d) for a clear comparison. The ΔT/P values for sapphire and HR Si substrates are roughly 2.7 and 6.0 times smaller than that for SiO_2/Si, indicating that the SHE can be mostly eliminated by utilizing HR Si as the substrate.

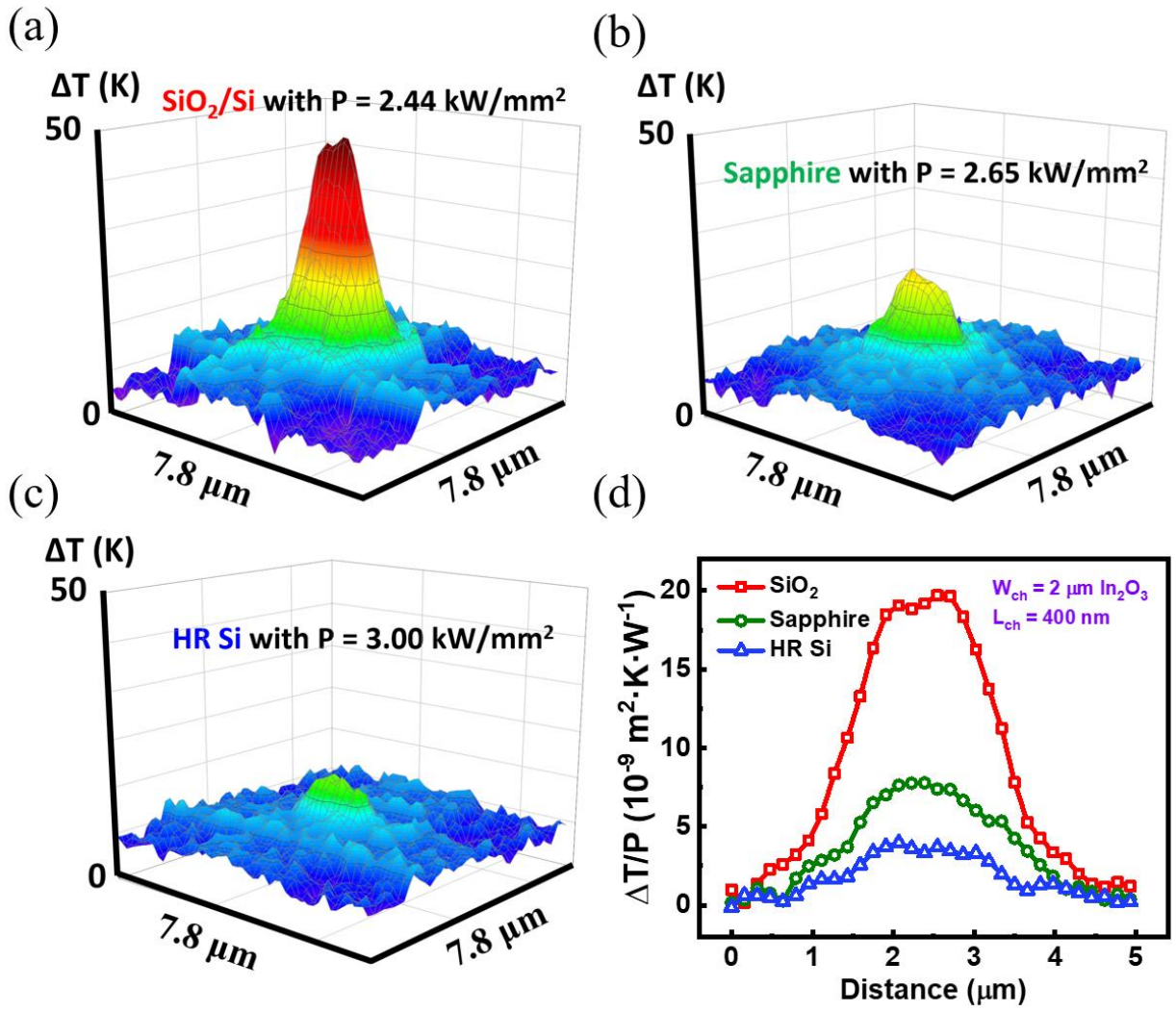

Figure 4.3. Temperature increase of a TG In_2O_3 transistor with (a) SiO_2/Si, (b) sapphire, and (c) HR Si substrate and power density of (a) 2.44, (b) 2.65, and (c) 3.00 kW/mm^2.

Through the thermo-reflectance measurement, the SHE of TG In_2O_3 transistors is visualized can explored quantitatively. Furthermore, this technique is applicable to devices with different parameters such as channel length or channel thickness, even to different material systems.

4.4 Heat Transfer Simulation

To verify the TR measurement results, thermal simulation with a finite-element method is carried out through COMSOL. The model design, which is similar to the discussed In_2O_3 TG transistors, and its mesh build-up are illustrated in Figure 4.4. The red square in Figure 4.4 denotes the area of interest, and Figure 4.5(a) reveals the simulated result with SiO_2/Si substrate and power density of 2.44 kW/mm^2 (same conditions as Figure 4.3(a)). To compare the simulation results with the TR measurements, the area of interest in Figure 4.3(a) is shown in Figure 4.5(b) in a similar fashion to Figure 4.5(a), and their cross-sections are plotted in Figure 4.5(c). It can be seen in Figure 4.5(a)–(c) that the simulation and experimental results are in excellent agreement.

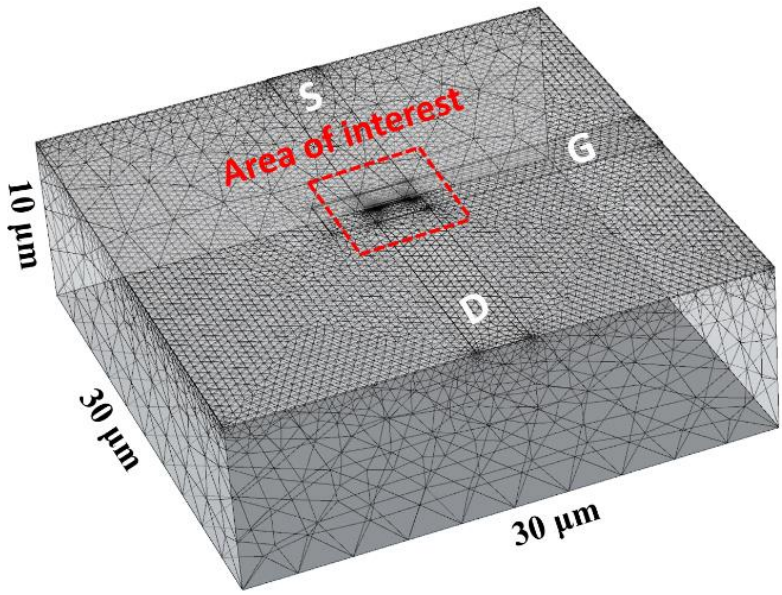

Figure 4.4. Model design and mesh build-up of a TG In_2O_3 device for thermal simulation with a finite-element method.

A false-color image of the corresponding area of a fabricated device is illustrated in Figure 4.5(d) for better SHE visualization. The ΔT values of TG In_2O_3 transistors with the three different substrates at various power conditions are plotted in Figure 4.6, showing a linear relation. The slope of each line is the thermal resistance (RT) for that corresponding case. The extracted RT values for SiO_2/Si, sapphire, and HR Si substrates are approximately 19.6, 7.4, and 3.2 $mm^2 \cdot K/kW$, respectively.

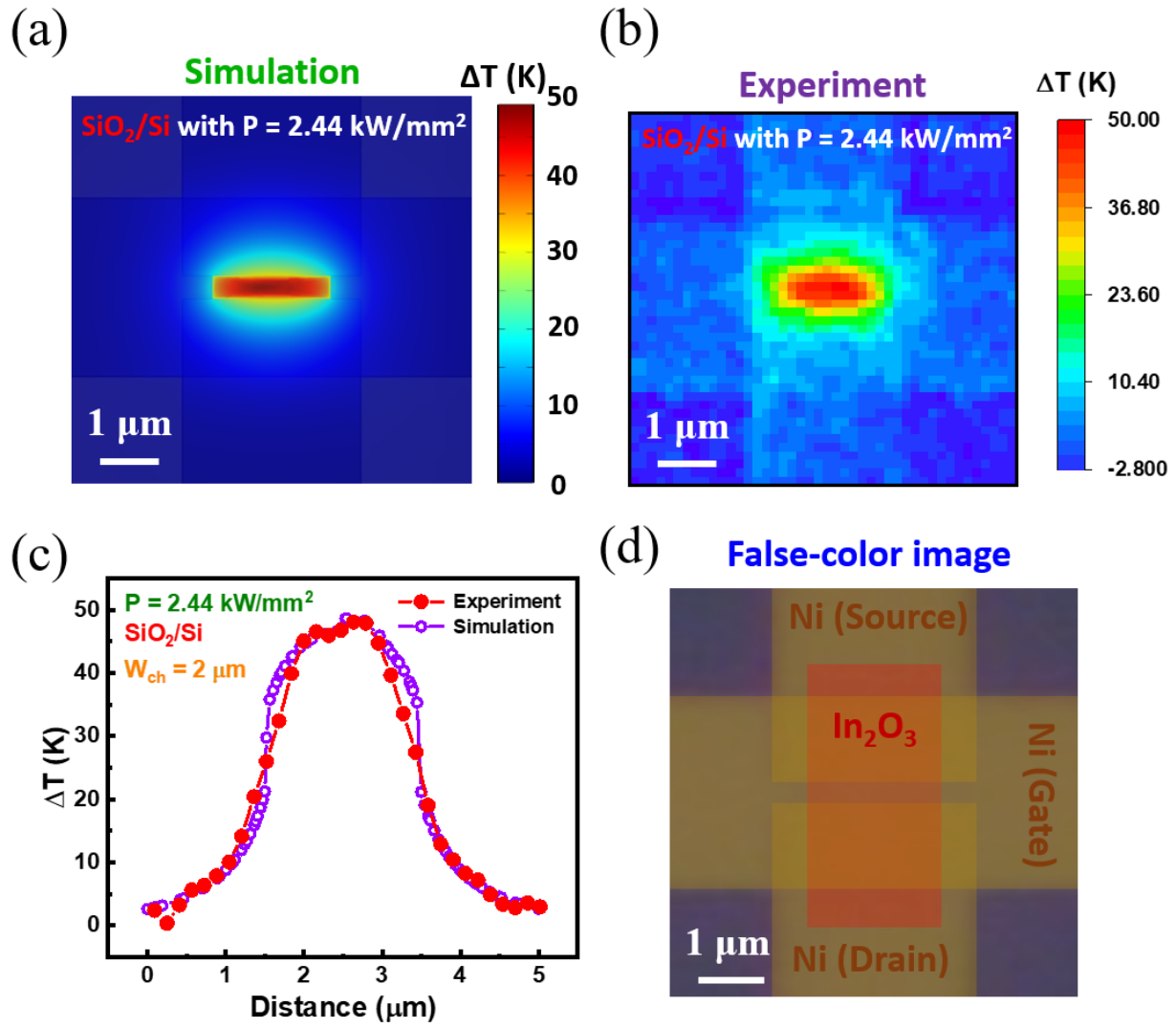

Figure 4.5. (a) Simulation result and (b) TR measurement of a TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm. (c) Cross-sections of the simulated and experimental results of temperature increase. (d) A dales-color image of a fabricated TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm.

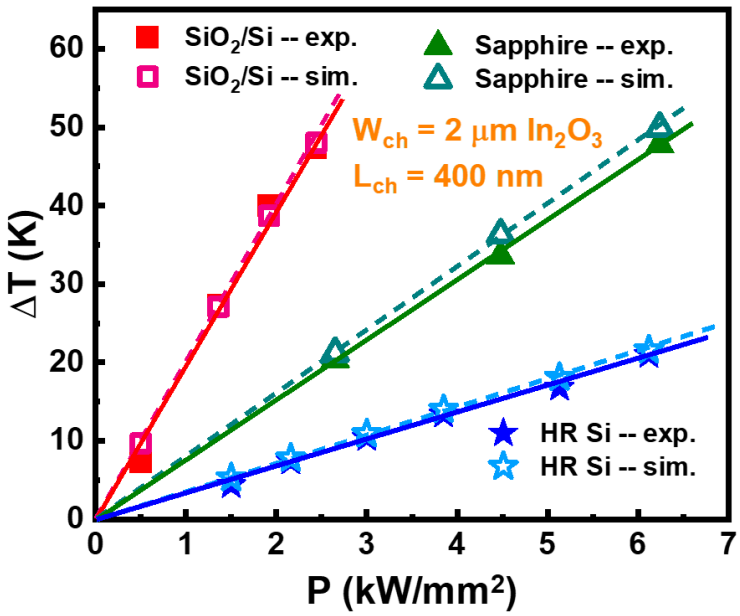

Figure 4.6. Temperature increase of TG In_2O_3 device with different substrates and power density.

4.5 Contact Resistance Engineering

With the ΔT being 6 times lower, HR Si is employed as the substrate to suppress the SHE and boost the ON-state performance of TG In_2O_3 devices. Moreover, contact resistance (R_C) can be further reduced by designing the contact regions of In_2O_3 in between the S/D and TG stacks as shown in Figure 4.7. The carrier concentration at the contacts, and therefore R_C, can be modulated by V_{GS}. With a positive increase of V_{GS}, R_C is decreased down to a minimum of 0.13 Ω·mm, which is lower than the previous report of 0.24 Ω·mm without the V_{GS} modulation as shown in chapter 3. Figure 4.8 illustrates the transfer and output characteristics of a TG In_2O_3 transistor with T_{ch} of 1.8 nm, L_{ch} of 80 nm, and HR Si substrate after O_2 annealing at 235 °C, showing an ON–OFF ratio of 3 orders and a maximum I_D up to 2.65 mA/μm. Even with such high power, the generated heat can be mostly dissipated due to the high thermal conductivity (142 $W \cdot m^{-1} \cdot K^{-1}$) of HR Si. Therefore, with the low R_C and the considerably mitigated SHE, an extremely high maximum I_D of 2.65 mA/μm is accomplished with a 1.8-nm In_2O_3 TG transistor.

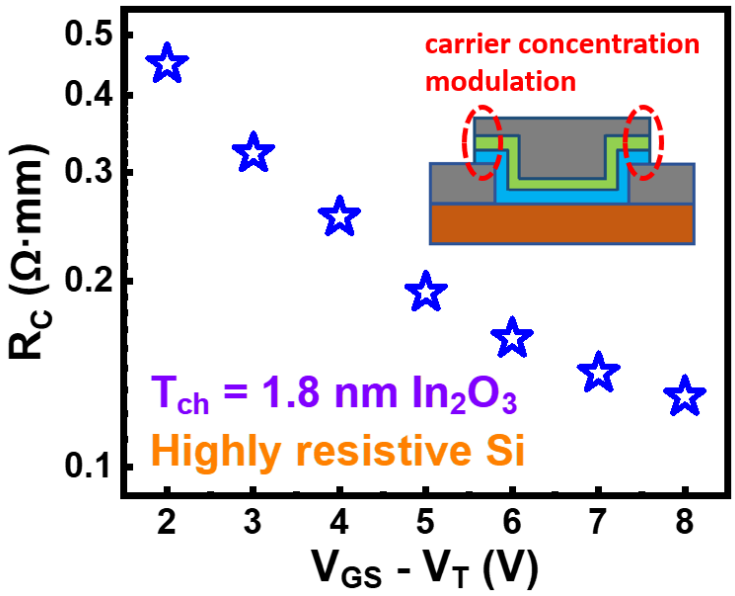

Figure 4.7. Contact resistance decrease with increasing V_{GS}–V_T due to carrier concentration modulation.

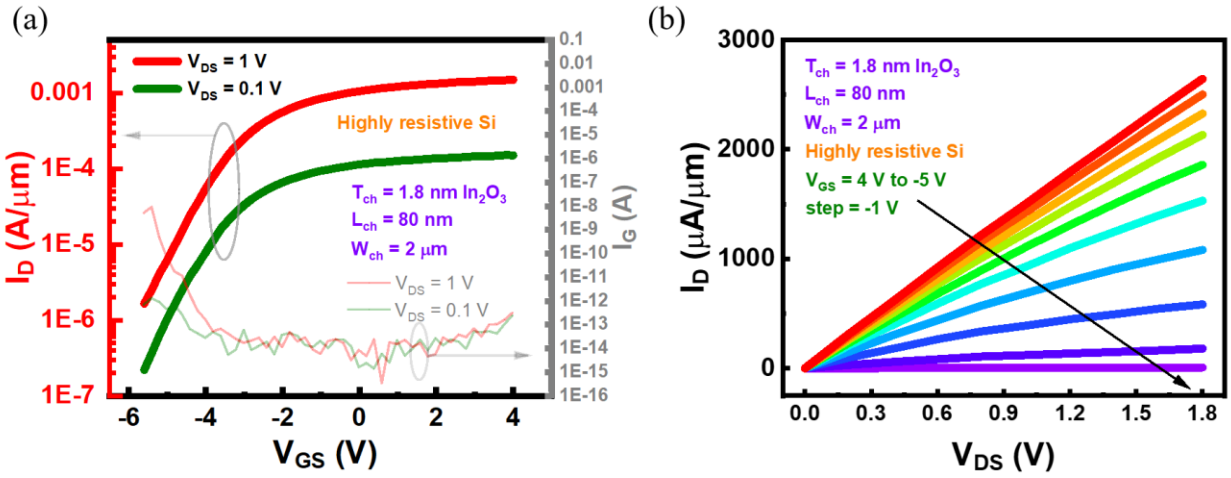

Figure 4.8. (a) Transfer and (b) output characteristics of a TG In_2O_3 transistor with T_{ch} of 1.8 nm, L_{ch} of 80 nm, and HR Si substrate after O_2 annealing at 235 °C achieving maximum I_D of 2.65 mA/μm.

5. TRANSIENT THERMAL AND ELECTRICAL CO-OPTIMIZATION OF ALD INDIUM OXIDE TRANSISTORS

5.1 Motivations

In chapter 4, self-heating effect is visualized through thermo-reflectance measurement. In addition, heat transfer simulation with a finite-element method provides verification and outputs consistent results on the temperature change distribution. It is demonstrated that by utilizing sapphire (40 $W \cdot m^{-1} \cdot K^{-1}$) and HR Si (142 $W \cdot m^{-1} \cdot K^{-1}$) as the thermally conductive substrate, the self-heating induced temperature elevation is reduced by a factor of 2.6 and 6.0, respectively.

On the other hand, the exploration only focused on their steady-state thermal behaviors. To acquire a comprehensive understanding and co-optimize the electrical performance of TG In_2O_3 transistors with their thermal characteristics, transient thermal characterization plays an important role here. Therefore, in this chapter, we employ the TR equipment to investigate the transient thermal behaviors of TG In_2O_3 transistors as they self-heat-up and cool-down. With the understanding, we utilize pulse measurement to optimize the electrical behaviors of the devices. This way, self-heating effect is avoided from the root as the devices under test are only turned on for short periods of time so that they are turned OFF before the SHE degrades the device performance. Accordingly, extremely high drain current of 4.3 mA/μm is achieved at high drain bias of 3.2 V with TG In2O3 transistors with T_{ch} of 1.9 nm, L_{ch} of 80 nm, and W_{ch} of 2 μm. Even with this high power, no SHE is observed, and the transport behaviors are well characterized and optimized.

Besides, even though diamond is economically unaffordable for mass production, its thermal conductivity (2200 $W \cdot m^{-1} \cdot K^{-1}$) is the highest. In this chapter, we also studied the SHE of TG In_2O_3 FETs on diamond substrates as a reference to understand the maximum benefits that can be obtained by substrate substitution.

5.2 Substrate Substitution with Variant Thermally Conductive Substrates

In this chapter, the TG In_2O_3 devices used for thermal investigations have the same channel length of 400 nm and channel width of 2 μm as the previous chapter. On the other hand, beside SiO_2/Si, sapphire, and HR Si, a fourth kind of diamond which has the highest thermal conductivity

of 2200 $W \cdot m^{-1} \cdot K^{-1}$ serves as a thermally conductive substrate. Moreover, 20/30 nm of Ni/Au is used as the top-gate metal instead of plain Ni as shown in Figure 5.1. This way, Au, which has 5x larger thermal coefficient ($C_{TH} = -2.5 \times 10^{-4}\ K^{-1}$ [127], [138], [139]) with green light LED than Ni, is the serving as the surface material, delivering 5x better signal-to-noise ratio in the TR measurement. Therefore, we will see that the TR imaging results are much more ideal than what were observed in the previous chapter.

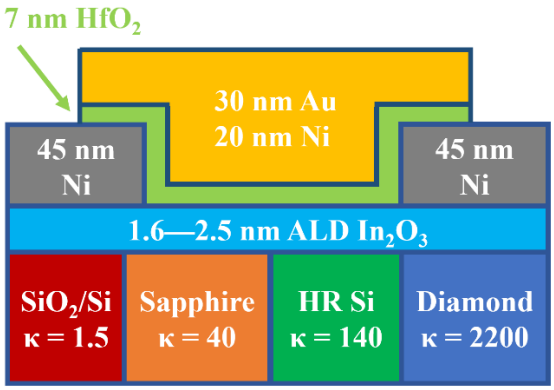

Figure 5.1. Device schematic of a TG ALD In_2O_3 FET with various thermally conductive substrates. The unit of thermal conductivity (κ) is $W \cdot m^{-1} \cdot K^{-1}$.

As a quick reminder and comparison figure for later, Figure 2 presents the electrical characteristics of TG ALD In_2O_3 FETs and the severe SHE. Figure 2(a) and (b) exhibits the transfer and output behaviors of a TG ALD In_2O_3 device with channel length (L_{ch}) of 600 nm and thin channel thickness (T_{ch}) of 1.6 nm on SiO_2/Si substrate operated at enhancement-mode (E-mode). The extracted threshold voltage (V_T) and subthreshold swing (SS) are 0.08 V and 150 mV/dec, respectively. ON–OFF ratio of 12 orders of magnitude is obtained due to the 3.0 eV wide bandgap of In_2O_3. Figure 2(c) shows the I_D–V_{DS} curves of a similar device with a shorter L_{ch} of 80 nm, exhibiting a maximum I_D of 1 mA/μm at V_{DS} of 1 V. However, as the applied V_{DS} increases to 1.6 V as shown in Figure 2(d), serious SHE happens due to low-κ of SiO_2, and the device becomes unstable. This is the thermal bottleneck for high I_D In_2O_3 FETs.

Figure 5.3 presents the observed ΔT distribution of the TG In_2O_3 transistors with identical structure and dimensions but different substrates around the channel region. Clearly, the one on SiO_2/Si substrate is the most self-heated while the one on diamond substrate is the least. The cross-sections of the ΔT along the channel width (W_{ch}) direction normalized by PD is demonstrated in

Figure 5.4(a) where the PD is calculated by ($I_D \times V_{DS}$) / ($L_{ch} \times W_{ch}$). The maximum ΔT of the devices with individual substrate and different PD is plotted in Figure 5.4(b) where a linear relationship is obtained despite of the substrate. The inversed slopes of the regression lines indicate the capability of the substrate to dissipate the generated Joule heat in the channel. As implied in Figure 5.4(c), the higher κ of the substrate is, the lower the maximum normalized ΔT will be. Sapphire, HR Si, and diamond substrates have ΔT reduction by factors of 2.6, 6, and 13, respectively, compared with SiO_2/Si substrate with thick SiO_2.

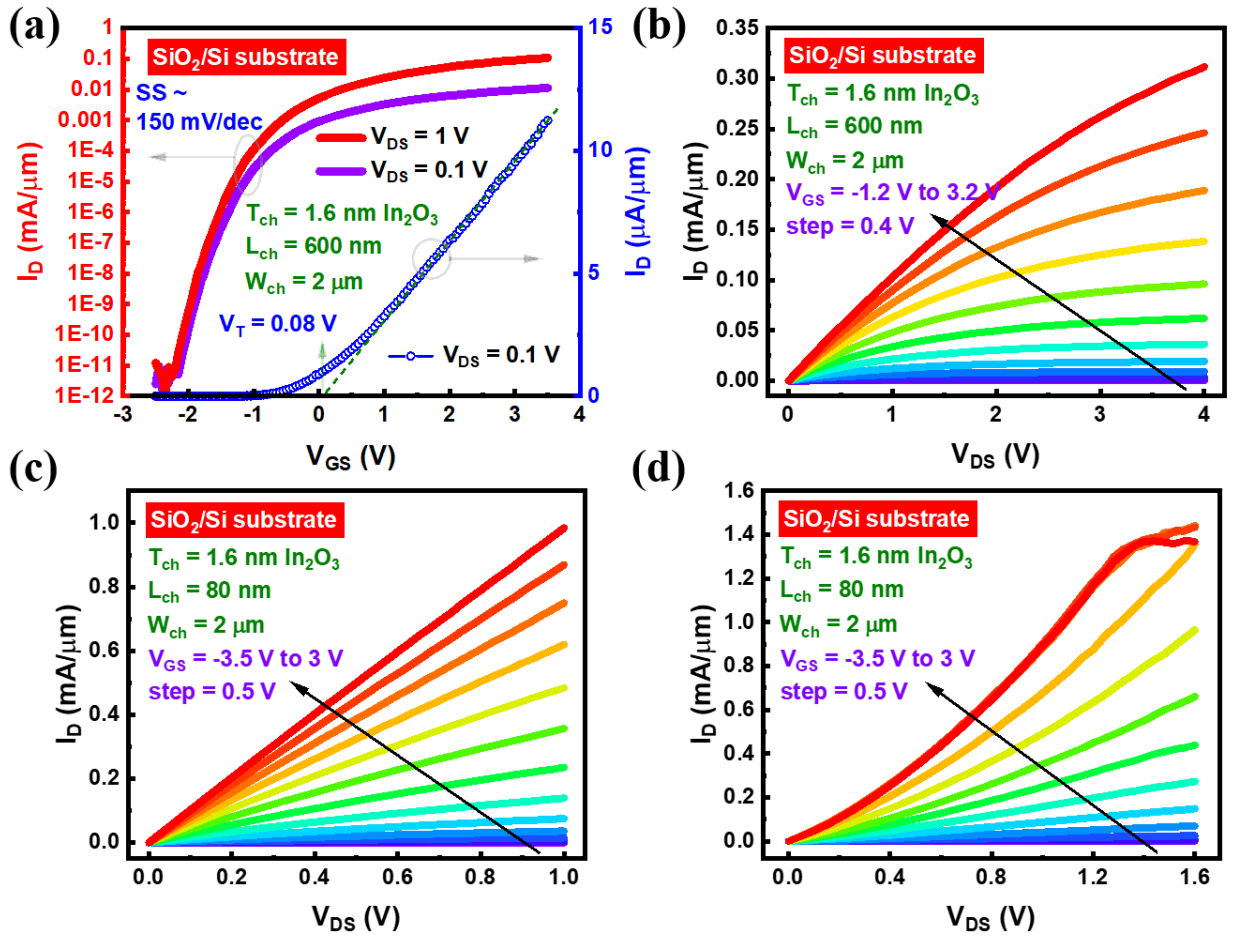

Figure 5.2. (a) Transfer and (b) output characteristics of a TG In_2O_3 transistor with T_{ch} of 1.6 nm and long L_{ch} of 600 nm on a SiO_2/Si substrate operated at enhancement-mode (E-mode). (c) Output characteristics of a TG ALD In_2O_3 FET with short L_{ch} of 80 nm on a SiO_2/Si substrate. (d) Severe SHE deteriorates the device performance of a TG ALD In_2O_3 FET with high power density.

Thermal studies motivate to build up an In_2O_3 transistor with T_{ch} of 2.5 nm and L_{ch} of 100 nm on diamond substrate to alleviate SHE. Figure 5.5 presents its DC output and transfer characteristics where an ultrahigh I_D of 3.7 mA/μm is realized at V_{DS} of 1.4V without observable SHE even with high PD, in great contrast to Figure 5.2(d). The extracted field-effect mobility (μ_{FE}) and SS are 55.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 185 mV/dec, respectively.

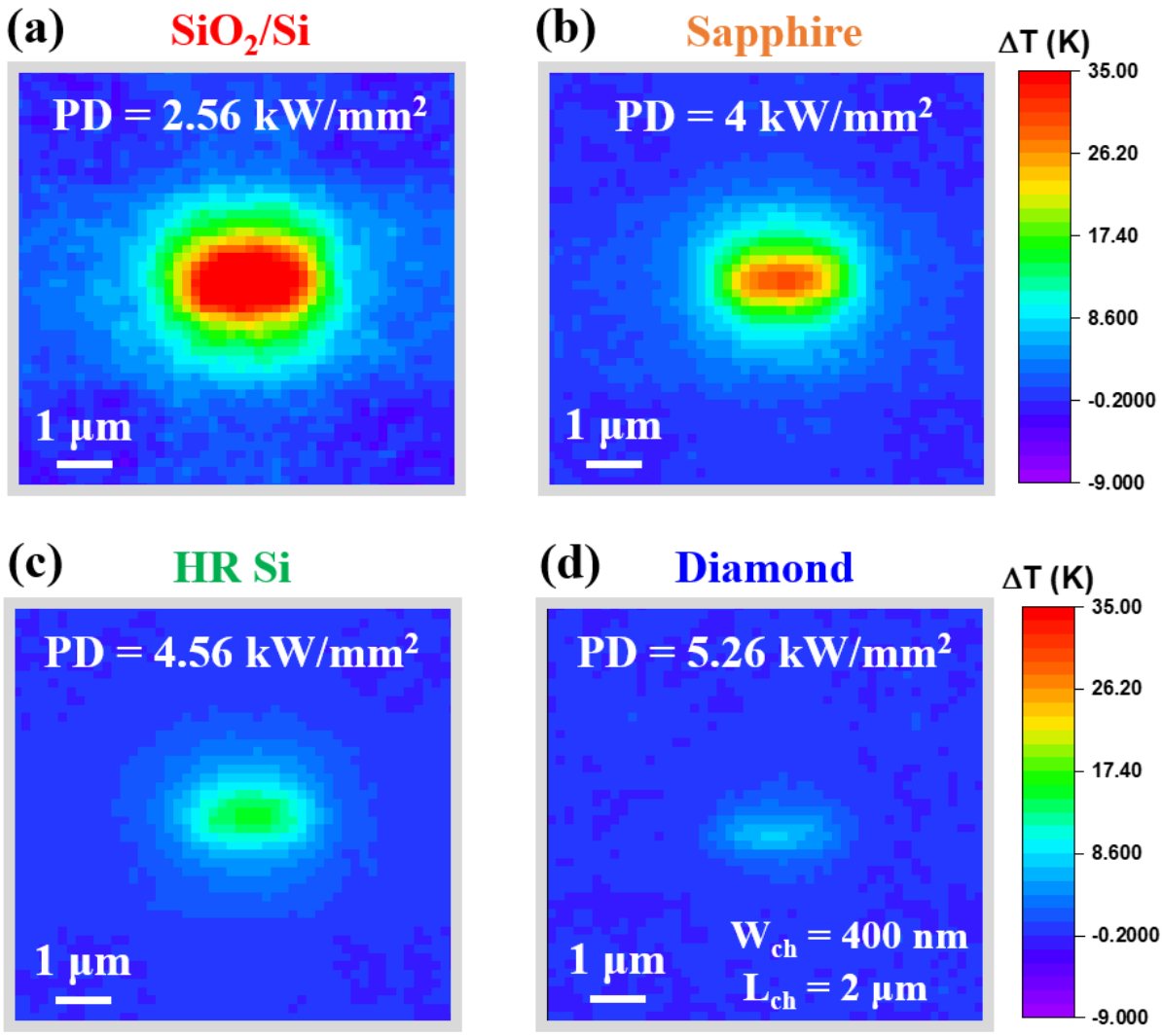

Figure 5.3. SHE visualization of In_2O_3 FETs in experiments with substrates of (a) SiO_2/Si, (b) sapphire, (c) highly resistive silicon, and (d) diamond substrate with various power density.

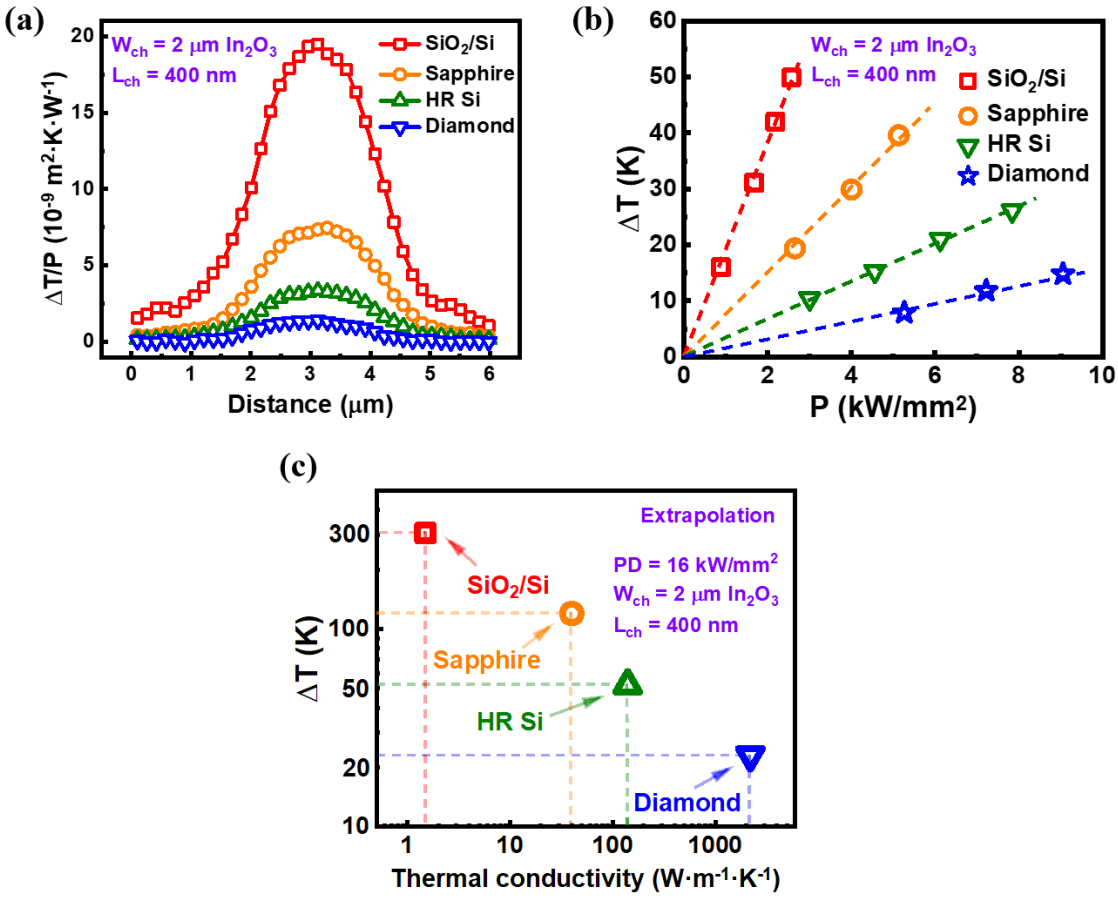

Figure 5.4. (a) Cross-sections of PD-normalized temperature increase distribution and (b) Temperature increase extraction of TG ALD In_2O_3 FETs with different substrates. (c) Comparison of the extrapolated temperature increase with different substrates given a constant PD.

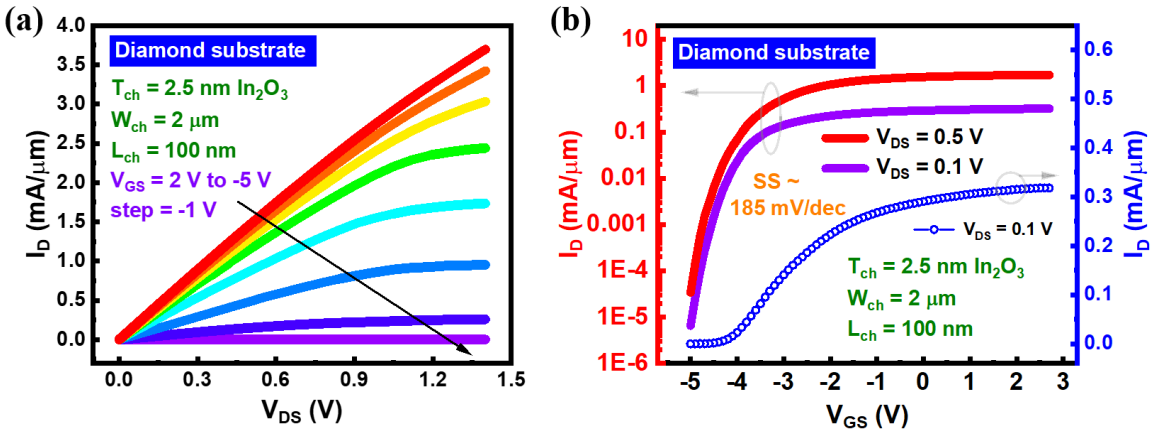

Figure 5.5. Output and transfer characteristics of an In_2O_3 FET with L_{ch} of 100 nm and T_{ch} of 2.5 nm on a diamond substrate, performing ultrahigh I_D of 3.7 mA/μm under DC condition.

5.3 Transient Thermal Property Exploration

5.3.1 Equipment Setup and Mechanism

Although diamond with ultrahigh κ is an excellent heat sinker, it is not economically affordable for mass production. TG transistors on Si substrate are much more practical. To further mitigate the SHE on Si substrate, detailed transient thermal characteristics are studied.

As introduced in chapter 4, an ultrafast high-resolution TR imaging equipment is employed to systematically investigate and resolve the SHE. Its setup is shown in Figure 4.1. As a recall, the device under test is applied by periodic V_{DS} pulses, high-speed LED pulses, and a constant V_{GS} bias during the measurement. Besides, a synchronized charge coupled device (CCD) camera is equipped to capture the surface reflectance. Figure 4.2(a) demonstrates its working mechanism for steady-state exploration. As V_{DS} pulses start/end, the device is turned ON/OFF and accordingly self-heat-up/cool-down, and TR signals are captured as active/passive images after the steady-state is reached. This process is repeated numerous times, and the difference between the active and passive images is averaged consequently and transformed into a temperature scale through dividing by the calibrated thermal coefficient of the surface material ($C_{TH} = -2.5\times10^{-4}$ K^{-1} [127], [138], [139]) to obtain the final HR ΔT distribution image at the steady-state as shown in Figure 4.3(b).

Figure 5.6 illustrates the working mechanism for transient thermal characteristics. Similar to steady-state measurements, an active and a passive image are captured by the synchronized CCD camera in each period. By setting the active image to be captured at a specific timing, the ΔT distribution of that moment can be obtained through the same process shown in Figure 4.2(c). Here, the capture time window is set down to 50 ns to maximize the time-resolution.

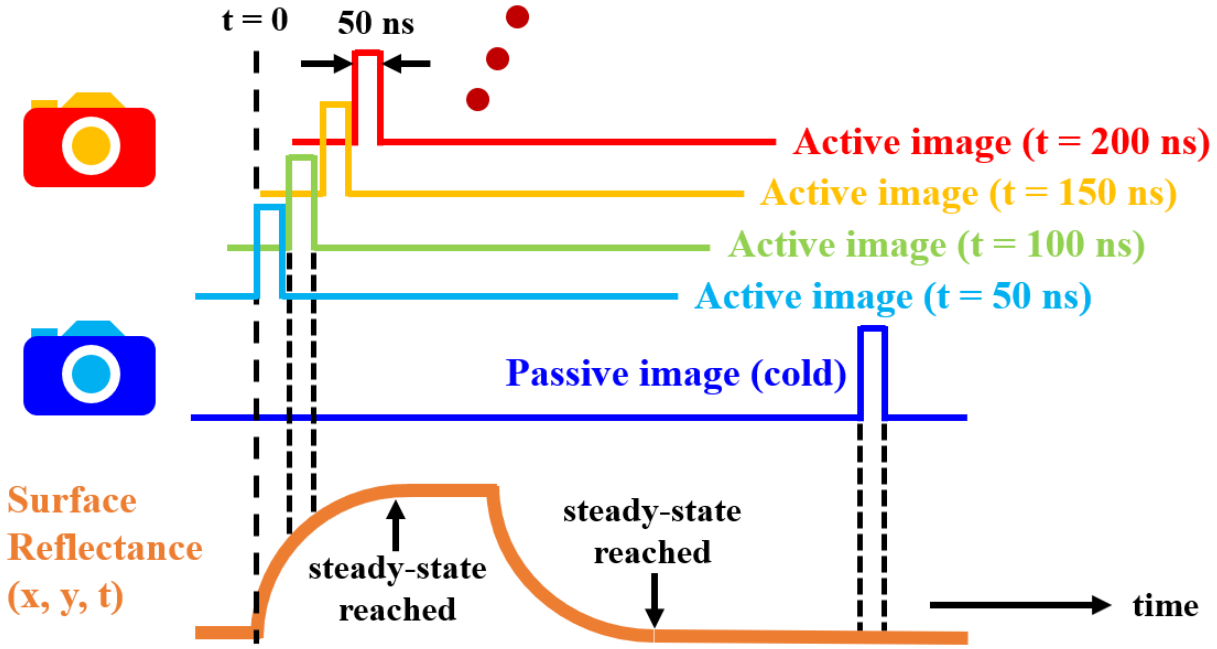

Figure 5.6. Working mechanism of transient thermal property study with an ultrafast high-resolution TR imaging system.

5.3.2 Transient Thermal Behaviors of TG ALD In_2O_3 Transistors

To experimentally observe the time-resolved self-heat-up and cool-down processes, the V_{DS} pulses are set to start at 0 ns and end at 600 ns. From 0 ns to 1200 ns, TR images are taken every 50 ns as presented in Figure 5.7 and Figure 5.8. The maximum ΔT of each moment of the devices with SiO_2/Si and HR Si substrates are summarized in Figure 5.8. It takes roughly 350 and 300 ns to reach steady-states for heat-up and cool-down, independent on the substrate. The maximum ΔT of each measurement is extracted and arranged into Figure 5.9.

The thermal energy transferred from a body to the ambient at a given time period is proportional to the temperature difference between the body and the ambient as expressed as follows [140]:

$$F = hA_s(T(t) - T_a) = -\rho c_p V \frac{dT}{dt} \quad 5\text{-}1$$

where F is the outward heat flux from the body, h is the heat transfer coefficient, A_s is the surface area, $T(t)$ is the body temperature at time t, T_a is the constant ambient temperature, ρ is the mass density of the body, c_p is the specific heat of the body, and V is the volume of the body. Let

$$\tau = \frac{-\rho c_p V}{h A_s} \quad 5\text{-}2$$

then we have

$$\frac{dT}{dt} + \frac{1}{\tau} T = \frac{1}{\tau} T_a \quad 5\text{-}3$$

By defining

$$\Delta T \equiv T - T_a \quad 5\text{-}4$$

we have

$$\frac{d\Delta T}{dt} + \frac{1}{\tau} \Delta T = 0 \quad 5\text{-}5$$

Solving the differential equation, we obtain

$$\Delta T(t) = c \times e^{-\frac{t}{\tau}} \quad 5\text{-}6$$

For the cool-down process, the initial condition is

$$\Delta T(0) = c \times e^{-\frac{0}{\tau}} = c = \Delta T_{st} \quad 5\text{-}7$$

where ΔT_{st} is the steady-state temperature difference, and then we have

$$\Delta T(t) = \Delta T_{st} \times e^{-\frac{t}{\tau}} \quad 5\text{-}8$$

Therefore, we have

$$\frac{t}{\tau} = -\ln\left(\frac{\Delta T(t)}{\Delta T_{st}}\right) \quad 5\text{-}9$$

For the heat-up process, similar derivation can be followed and the following equation can be obtained

$$\frac{t}{\tau} = -\ln\left(1 - \frac{\Delta T(t)}{\Delta T_{st}}\right) \quad 5\text{-}10$$

By plugging in the experimental data point in Figure 5.9 into equation 5-9 and 5-10, The heat-up and cool-down time constant can be obtained. Figure 5.10 exhibits the time constant extraction where 137 and 109 ns are acquired for heat-up (τ_h) and cool-down (τ_c), respectively. τ_h and τ_c are related to intrinsic thermal properties of In_2O_3.

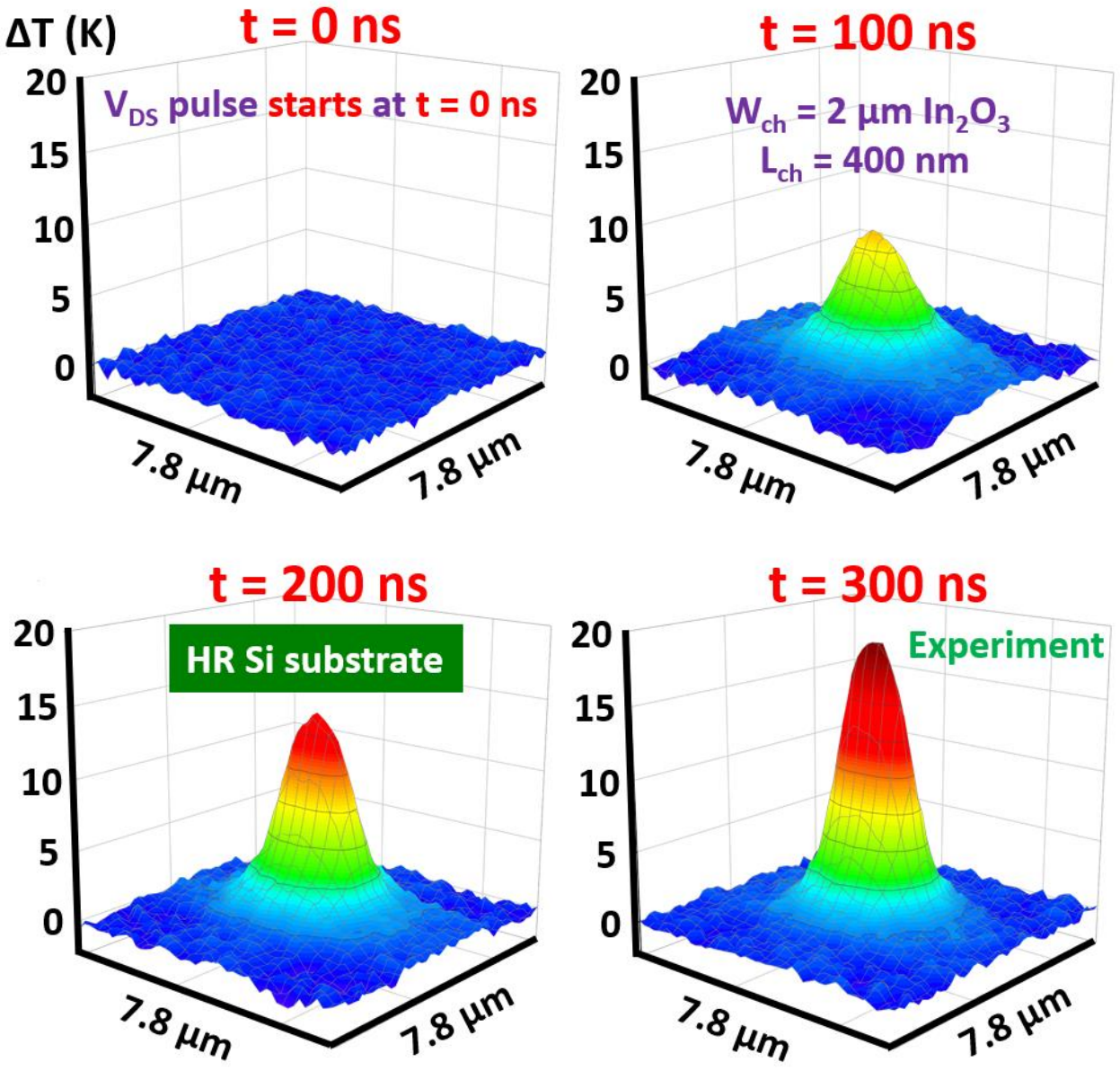

Figure 5.7. Transient TR characterization of the heat-up process of a TG ALD In_2O_3 FET on HR Si substrate. The device was self-heated-up by applying a V_{DS} pulse starting at 0 ns.

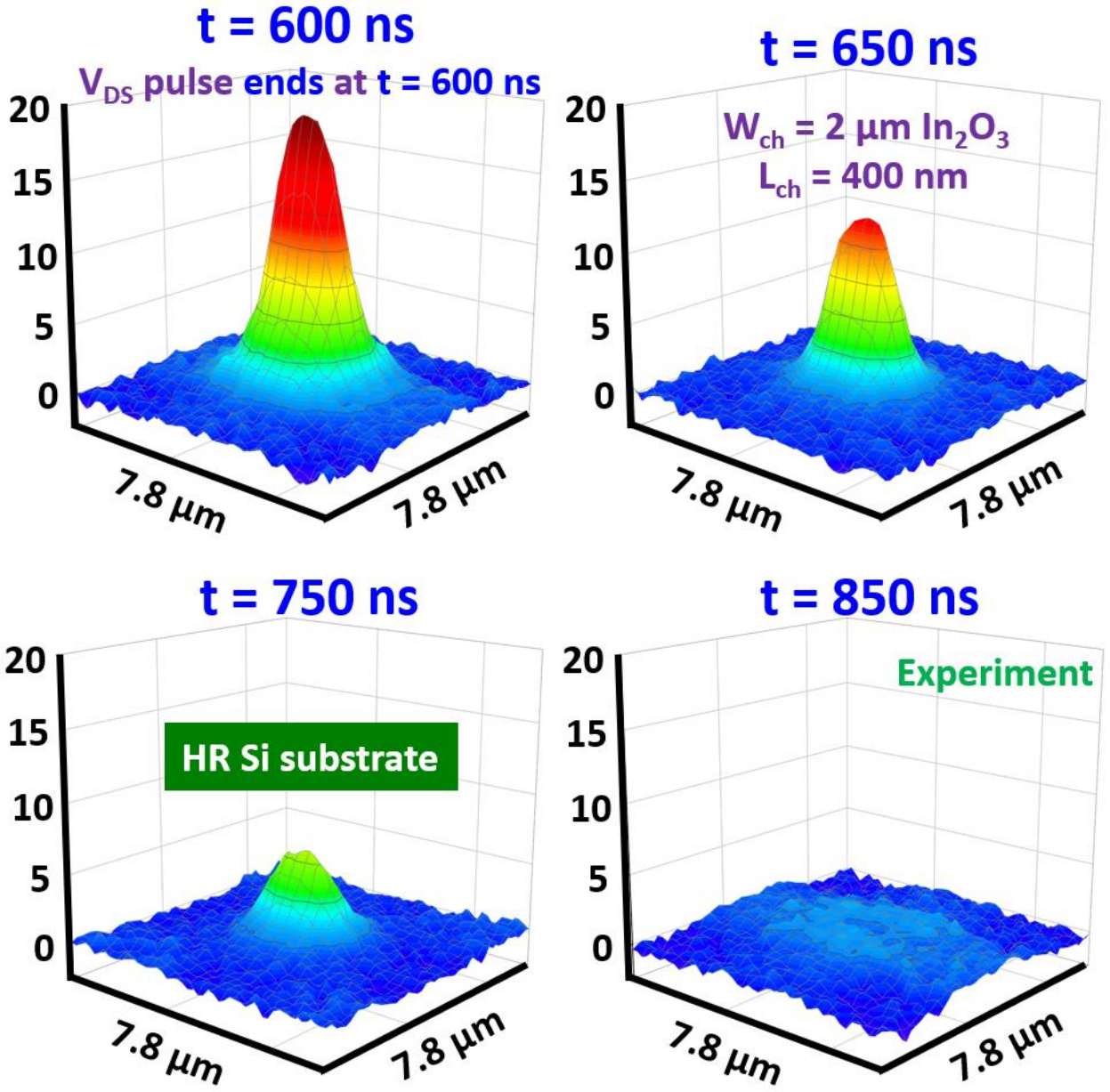

Figure 5.8. Transient TR characterization of the cool-down process of a TG ALD In_2O_3 FET on HR Si substrate. The device started to cool-down at 600 ns.

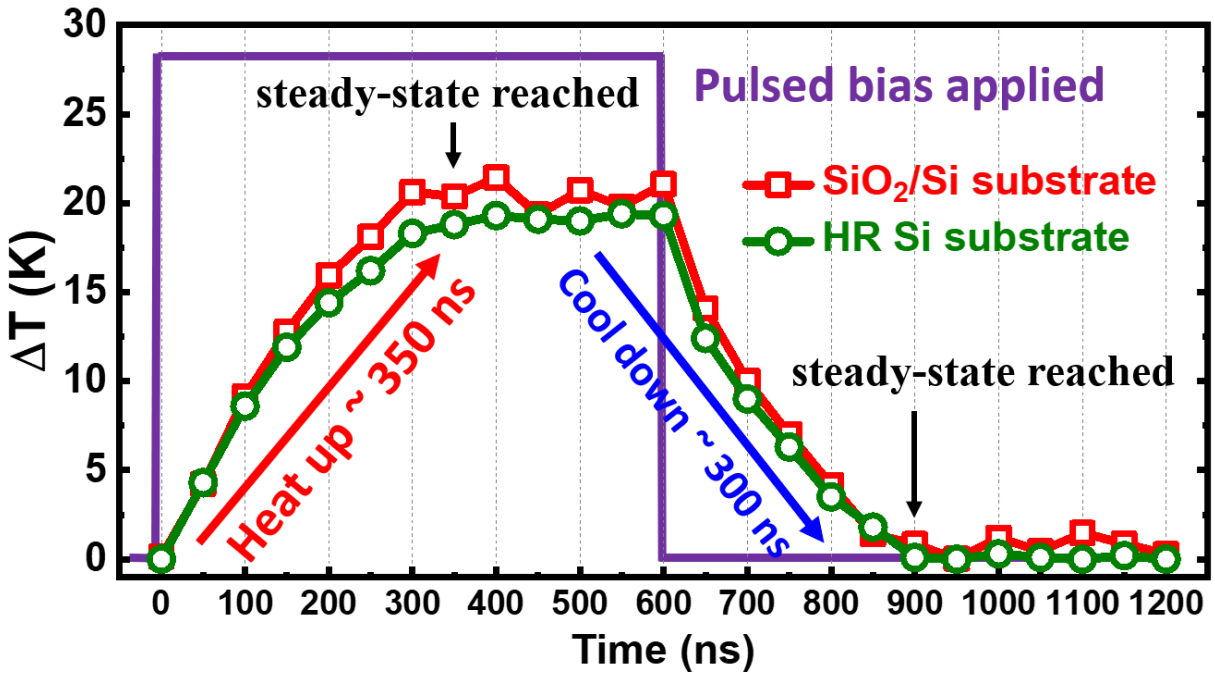

Figure 5.9. Transient temperature elevation results and comparison with different substrates. Roughly 325 ns is needed to reach steady-state in both cases.

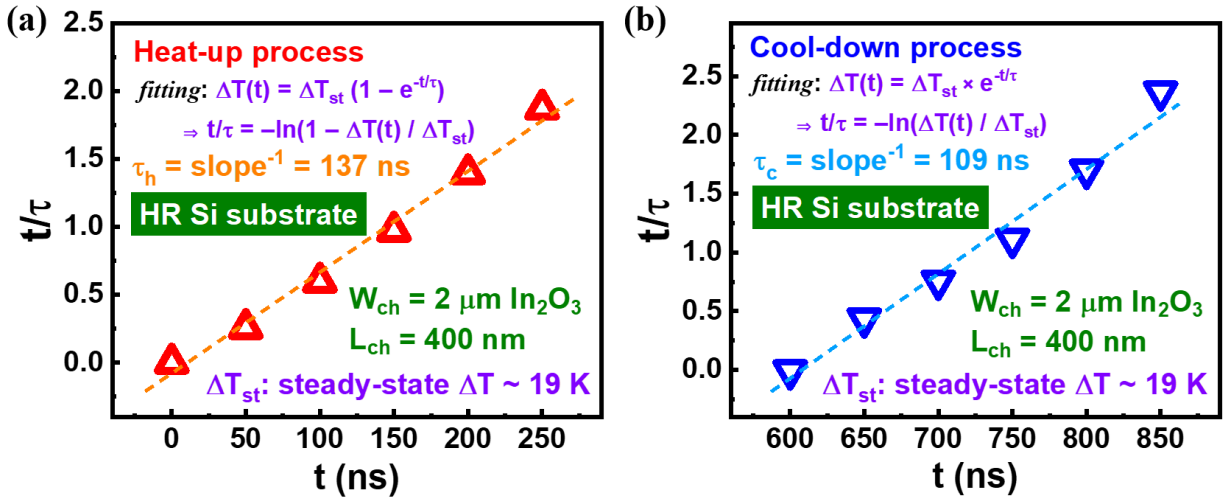

Figure 5.10. Time constant extraction of (a) heat-up and (b) cool-down processes from the transient ΔT measurement results with HR Si substrate of Fig. 20. The t/τ values are obtained by plugging the measured individual ΔT(t) values into the indicated formulas.

5.4 Self-Heating Effect Avoidance with Short-Pulse Measurement

With the understanding of its transient thermal characteristics, short-pulse electrical co-optimization is proposed to alleviate SHE. During the DC measurement, the extremely large current density flows through the semiconducting ultra-thin channel for a long time. The generated thermal energy exceeds the capability of heat dissipation of silicon substrate at some point, resulting in an upper bound of current density even though it's much higher than employing SiO_2. To further address this issue, pulse measurement is introduced to minimize the time window of on state, which greatly lowers the power rate and benefits even higher current density. Figure 5.11 illustrates the working principle of pulse measurement where t_{rise}, t_{pulse}, t_{fall}, t_{delay}, $t_{average}$, and T represent rising time, pulse width, falling time, delaying time, measuring and averaging time, and period, respectively. During the collection of the measurement results, an amount of short pulses, instead of DC, of V_D and V_G are applied to the device. In each period, it takes t_{rise} of time to set to the desired bias, keeps t_{pulse} of time at that bias, and takes t_{fall} to be back to the unbiased state. During the t_{pulse} time window, the first t_{delay} of time is utilized to wait for the bias to become stable, and collection of data happens in the following $t_{average}$ of time. By applying pulse measurement, the power rate of the device reduces to a ratio of t_{pulse} to T which is defined as duty cycle. Accordingly, the SHE can be alleviated even better through designing an appropriate duty cycle such as 0.01 %.

Figure 5.12 exhibits the I_D–V_{DS} curves of a TG In_2O_3 FET with T_{ch} of 1.9 nm and L_{ch} of 80 nm on HR Si substrate. The empty and solid symbols represent DC and pulse measurement results, and an ultrahigh I_D of 4.3 mA/μm is achieved at high V_{DS} of 3.2 V. In great contrast to Fig. 4, even with such high PD on atomically thin channel, there is no observable SHE since the t_{pulse} of 120 ns is even shorter than τ_h. The key fact is that the electrical response is much faster than the thermal response. As τ_h and τ_c are independent of the heating amplitude [141], ΔT over time during the pulse measurement can be calculated. Figure 5.13 illustrates the transient ΔT of the device under the highest PD of DC and pulse measurement in Figure 5.12. The maximum ΔT of pulse measurement (blue curve) is lower than 120 K even though its steady-state is higher than 200 K. Short-pulse electrical measurement can significantly reduce SHE and probe the potential of the material and device performance.

As a short summary, transient thermal and electrical properties of TG ALD In_2O_3 FETs on various thermally conductive substrates are co-optimized employing an ultrafast HR TR imaging

technique to unveil the problematic SHE. By using HR Si substrate and electrical short-pulse measurement, ultra-high I_D of 4.3 mA/μm is achieved on atomically thin In_2O_3 devices without observable SHE. This work demonstrates that the understanding of both thermal and electrical transient dynamics is of importance to resolve thermal bottleneck on atomically thin oxide semiconductor devices.

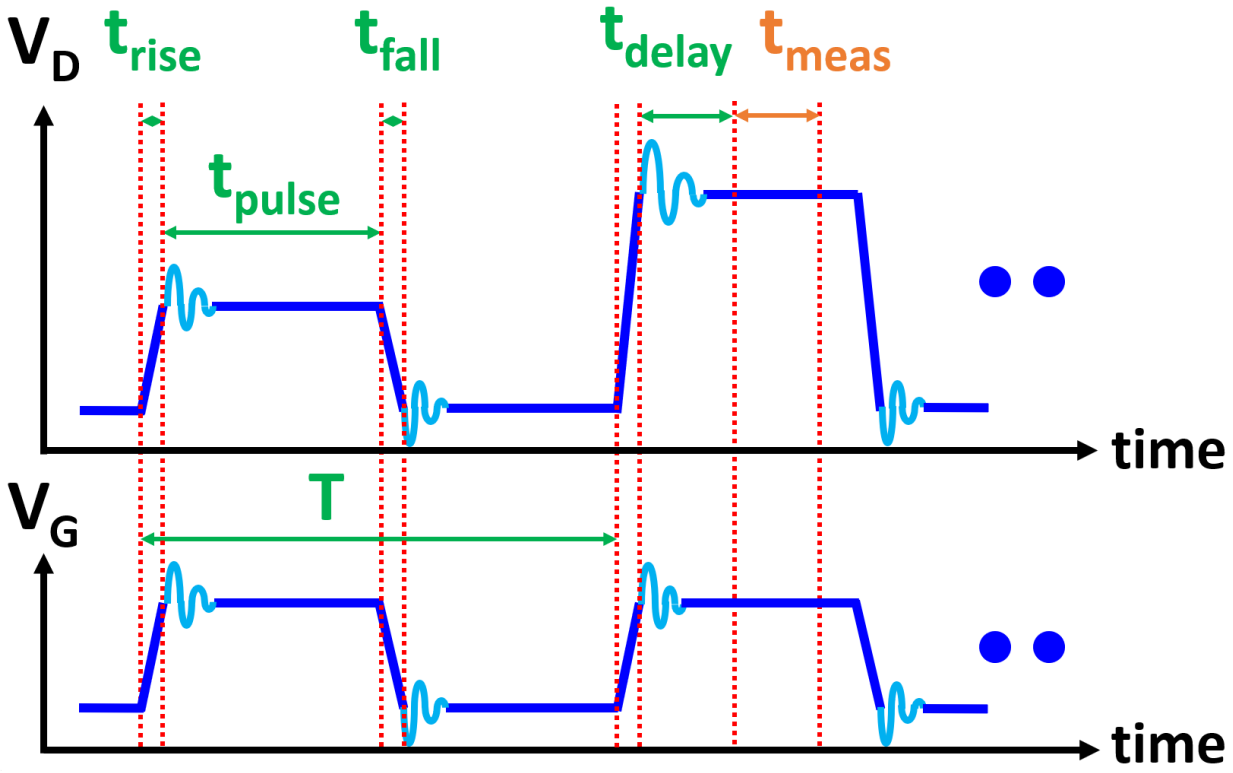

Figure 5.11. Diagram sketch of pulse measurement setup in time domain. The light blue damping illustrates the bias stabilization process after being set to desired values.

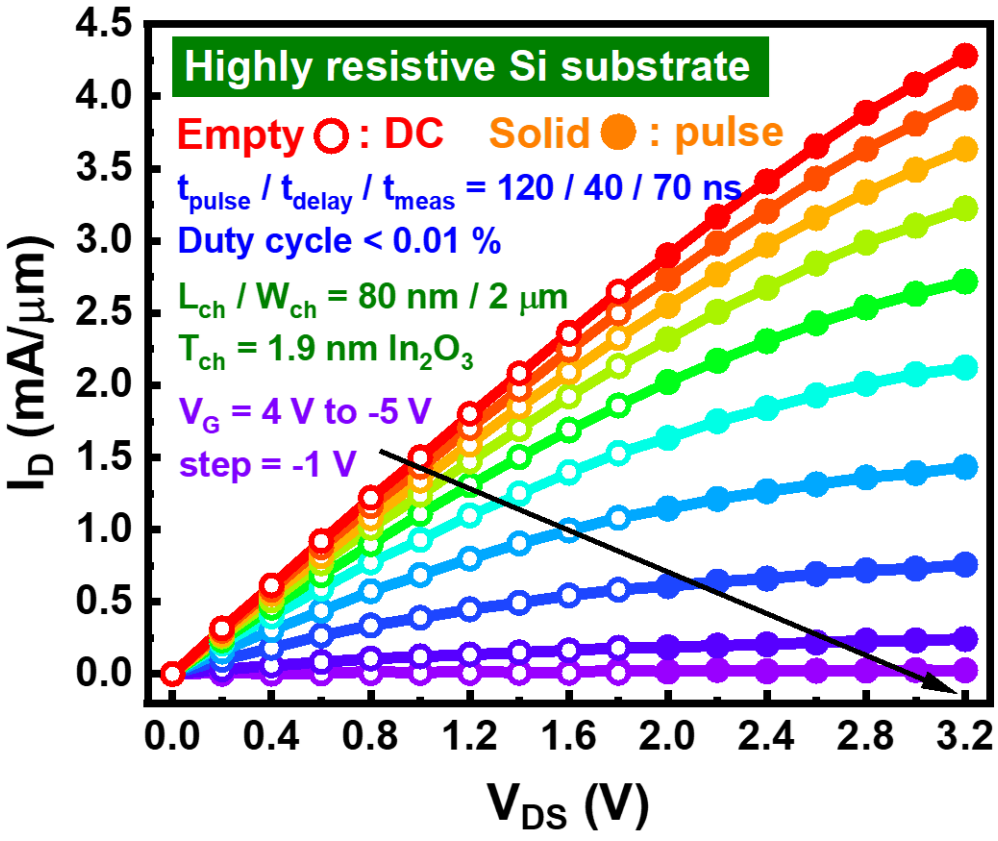

Figure 5.12. Output characteristics of a TG ALD In_2O_3 FET with short L_{ch} of 80 nm and T_{ch} of 1.9 nm on HR Si substrate achieving extremely high I_D up to 4.3 mA/μm.

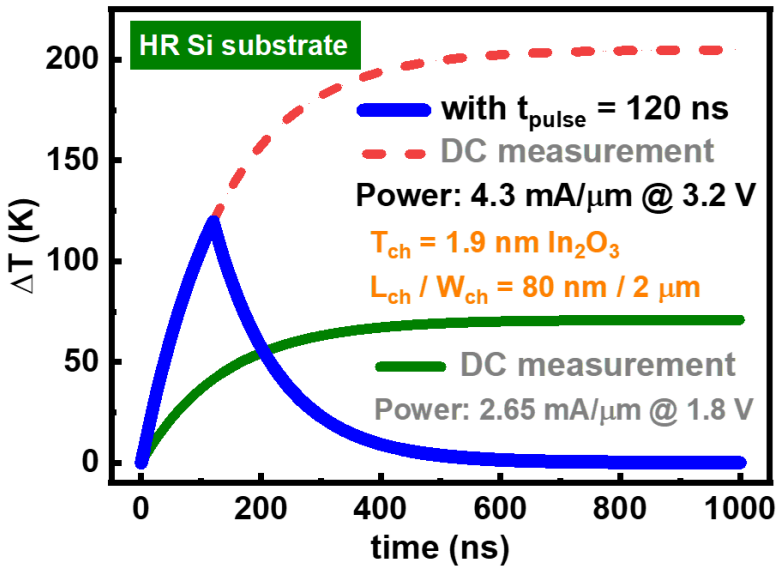

Figure 5.13. Transient ΔT calculation of DC and pulse measurements under respective highest PD in Figure 5.12.

6. SELF-HEATING EFFECT ALLEVIATION ON ALD INDIUM OXIDE THROUGH INTRERFACE ENGINEERING

6.1 Motivations

In chapter 4, sapphire is introduced as a thermally conductive substrate with thermal conductivity of 40 $W \cdot m^{-1} \cdot K^{-1}$ to assist heat transfer in TG In_2O_3 transistors, and it is demonstrated through TR measurement that the self-heating induced temperature increase is suppressed by a factor of 2.6, compared to that with a SiO_2/Si substrate.

Indeed, the higher κ of sapphire implies preferable heat dissipation potential. Nonetheless, it is found that the thermal boundary conductance (TBC) at the In_2O_3/sapphire interface is far from ideal, limiting the benefits of SHE reduction that sapphire can conduct. Moreover, TBC between wide bandgap semiconductors and high thermal conductivity substrates has been a concern for FET applications in other materials [142]–[145]. Therefore, even though thermal management has been applied to In_2O_3 and other material systems where substrates with higher κ such as sapphire are utilized to assist transferring thermal energy to deal with SHE, additional explorations to thermally improve the interface between the In_2O_3 channel and the substrate are still desired [139].

It is reported that a thermal adhesion layer as thin as 1 nm is sufficient to increase the TBC by more than a factor of 4 at the Au/sapphire interface [146]. In this chapter, a thin stack of h-BN or HfO_2 is similarly introduced as a thermal adhesion layer between the In_2O_3 channel and the sapphire substrate. To experimentally demonstrate the difference between devices with and without the presence of an interlayer, a thermo-reflectance (TR) measurement system with high spatial resolution is employed to observe the temperature increase (ΔT) caused by SHE. The ΔT of TG In_2O_3 transistors with the h-BN (HfO_2) adhesion layer induced by SHE is shown to drop by 9 (27) %, compared to that with no interlayer. Through heat transfer simulation and phonon density of state (PDOS) calculation, it is revealed that the TBC at the interface is improved by a factor of 2 (7), and this is due to the higher value of the intersection over union (IOU) ratio in the PDOS acoustic region of In_2O_3 with h-BN (HfO_2) than that with sapphire by a factor of 3 (11). Consequently, TG In_2O_3 transistors achieving extremely high I_D of 2.4 mA/μm are realized with T_{ch} of 2.1 nm, L_{ch} of 80 nm, and W_{ch} of 2 μm on a sapphire substrate with a thin HfO_2 thermal adhesion layer. Even with such high PD, there is no observable performance degradation due to the SHE which is much alleviated.

6.2 Device Structure and Fabrication

The TG In_2O_3 devices are similar to that introduced in the previous chapters but with a thin thermal adhesion layer between the indium oxide channel stack and the substrate. Figure 6.1 (a) and (b) illustrate the schematic diagram and fabrication flow of TG In_2O_3 transistors. The substrate was either p+ silicon with 90 nm thermally grown silicon dioxide (SiO_2/Si) or sapphire. At first, standard solvent cleaning process was applied to the substrates to ensure the surface cleanness. There was no interlayer as SiO_2/Si served as the substrate while two layers (2L) of hexagonal boron nitride (h-BN) or 4 nm of HfO_2 as sapphire served as the substrate. The 2L h-BN was formed by chemical vapor deposition (CVD) while the 4 nm HfO_2 was grown by ALD at 200 °C with $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as the Hf and O precursors, respectively. Standard solvent cleaning steps were followed again at this point before the deposition of the channel stack.

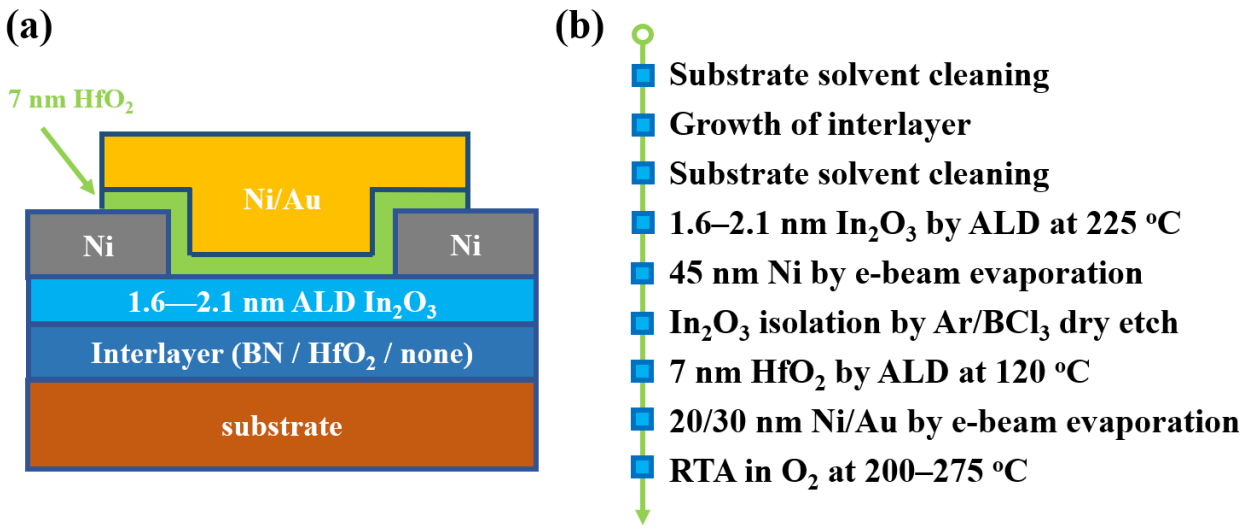

Figure 6.1. Cross-sectional illustration of device structure and (b) fabrication flow of TG In_2O_3 transistors with a thermal adhesion interlayer.

1.6–2.1 nm of In_2O_3 ultrathin film was conformally grown by ALD at 225 °C with trimethylindium (TMIn) and H2O as the In and O precursors, respectively, on the well-cleaned substrates with or without an interlayer, followed by an Ar/BCl_3 plasma dry-etch step for channel region isolation. Next, 45 nm of Ni as source and drain (S/D) contacts with variant L_{ch} was formed by e-beam lithography (EBL), e-beam deposition, and a lift-off process. At the step of EBL patterning, diluted ZEP 520A served as the e-beam resist. With a sapphire substrate, DisCharge

H_2O was applied as an anti-charging agent on top of the e-beam resist because of the electrical insulation property of sapphire. The anti-charging agent was removed by 2-propanol (isopropyl alcohol, IPA) before development. Then, 7 nm HfO_2 as TG dielectric layer was deposited by ALD at 120 ^oC where the relatively low temperature was for the minimization of the interaction between the HfO_2 and In_2O_3 layers as mentioned. On the top, a Ni/Au of 20/30 nm metal stack as the gate contact was defined by the identical process as the S/D contacts. The whole fabrication flow ended with an RTA treatment at 200–275 ^oC for 2 minutes in an O_2 environment to annihilate the oxygen vacancies. Dedicated ALD chambers for HfO_2 and In_2O_3 growth were utilized to circumvent cross-contamination throughout the steps, and the thickness of HfO_2 and In_2O_3 films were measured by Gaertner L116A ellipsometer calibrated by transmission electron microscopy (TEM) and atomic force microscopy (AFM) as presented and introduced in chapter 3.

6.3 Self-Heating Effect Comparison

6.3.1 Thermo-Reflectance Imaging Observation

Because of its inferior thermal boundary conductance (TBC) with the In_2O_3 stack, the heat transfer capability of sapphire is restricted to some degree. Therefore, a thermal adhesion layer of h-BN or HfO_2 is inserted in between to enhance the effective TBC. Figure 6.2(a) and (b) exhibit the ΔT distribution around the channel region of a TG In_2O_3 transistor on a sapphire substrate with L_{ch} of 400 nm, W_{ch} of 2 μm, and no interlayer at power density (PD) of approximately 5 kW/mm^2 in a 3D plot and a heat map, respectively. Likewise, Figure 6.2(c)–(f) present the devices with identical structure and dimensions but an inserted layer of h-BN or HfO_2 at similar PD in the same way. In all 3 cases, the ΔT distributes in bell-like shapes with high plateaus in the middle descending to their proximity. It is noticeable that the device without a thermal adhesion layer shows the highest ΔT while the one with a HfO_2 interlayer exhibits the lowest.

For a clearer comparison, the cross-sections of Figure 6.2(b), (d), and (f) along the direction of channel width are plotted into Figure 6.3(a). With identical dimensions and similar PD, the TG In_2O_3 devices without a thermal adhesion layer, with 2L h-BN, and with 4 nm HfO_2 demonstrate maximum ΔT of 38.2, 35.0, and 28.1 K, respectively. This suggests that a 9 (27) % of ΔT reduction is obtained by inserting a thin thermal adhesion layer of h-BN (HfO_2) between the In_2O_3 channel

and the sapphire substrate. Besides, the maximum ΔT with cases of different substrates and interlayers at variant PD is arranged into Figure 6.3(b) where the error bars indicate 95 % confidence intervals. Observably, the maximum ΔT of a certain device is roughly proportional to the PD in all cases. Moreover, at the same PD, the ΔT decreases by a factor of 2.5 through replacing the SiO_2/Si substrate with sapphire and by a factor of 2.8 (3.7) through replacing that with BN/sapphire (HfO_2/sapphire). This specifies the diminishment of SHE in TG In_2O_3 transistors.

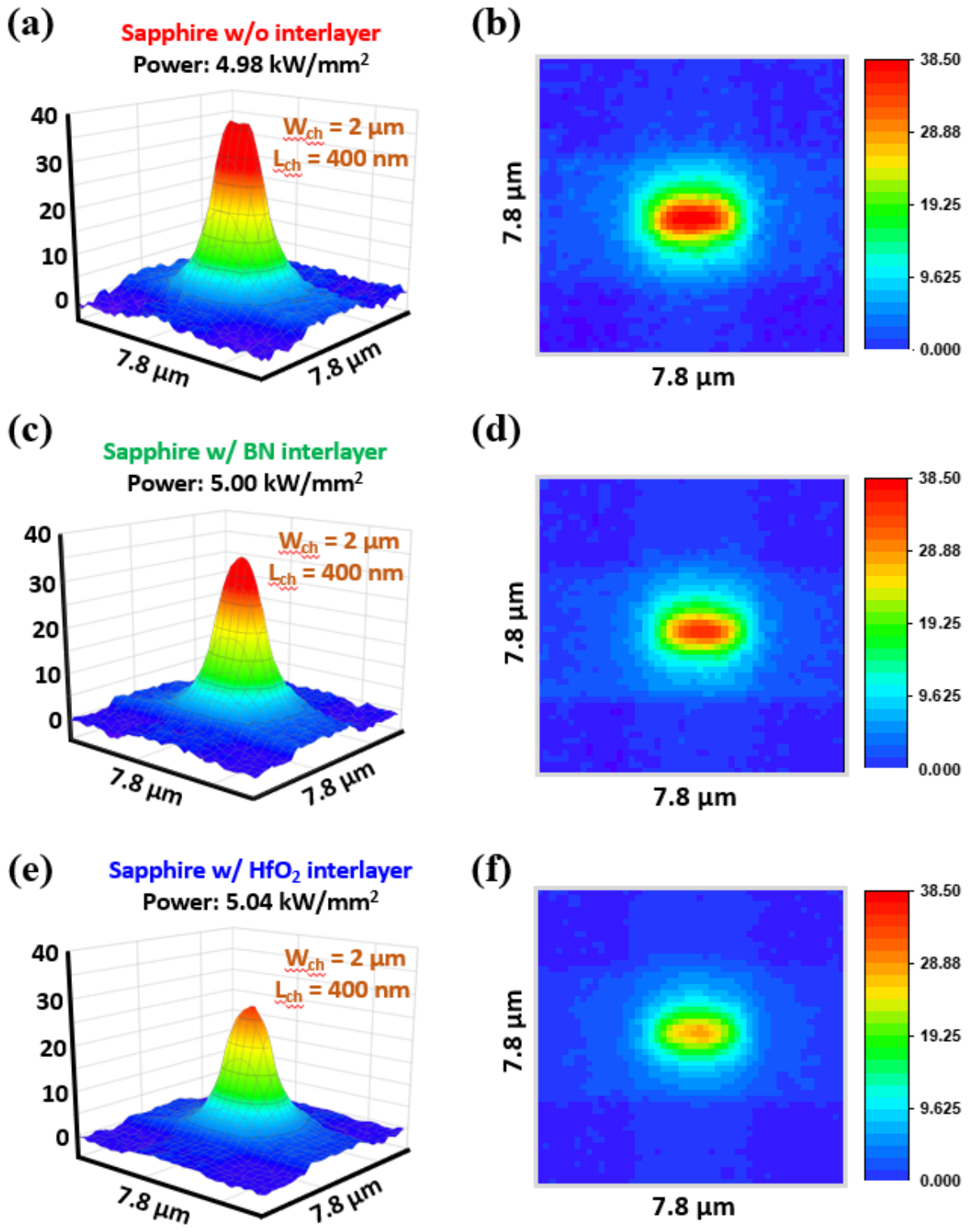

Figure 6.2. A ΔT (a) 3D plot and (b) heat map of a TG In_2O_3 transistor with W_{ch} of 2 µm, L_{ch} of 400 nm, no interlayer on a sapphire substrate at PD of roughly 5 kW/mm^2 imaged by the TR measurement system. The corresponding plots of the devices with the same structure, dimensions, but a thermal adhesion layer of (c, d) 2L h-BN and (e, f) 4 nm HfO_2 at similar PD.

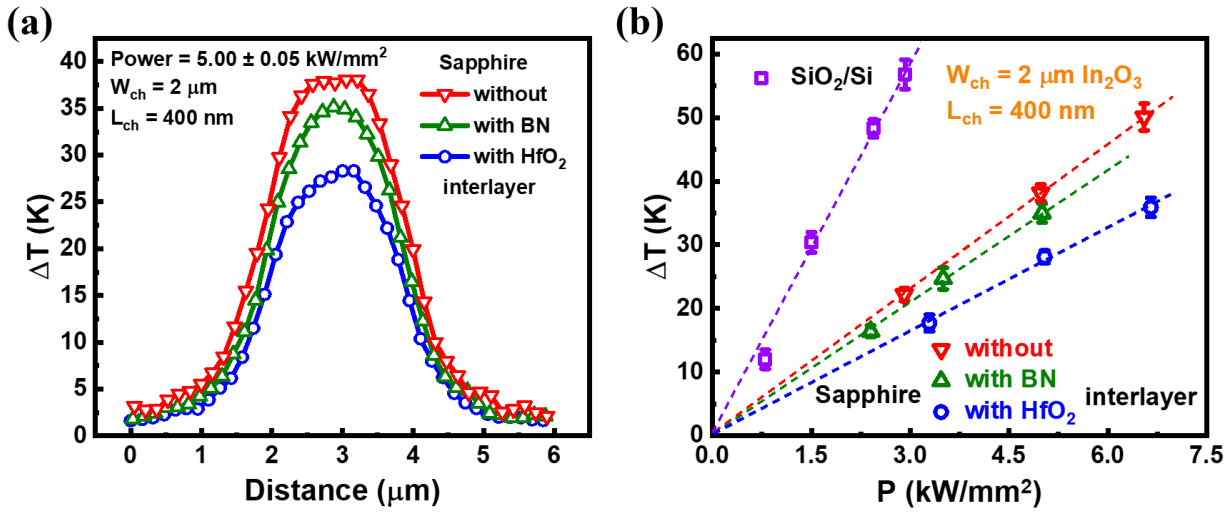

Figure 6.3. (a) Cross-sections of the three ΔT plots along the direction of channel width, showing 9 or 27 % alleviation of the SHE by inserting a thermal adhesion layer of h-BN or HfO_2, respectively. (b) Comparison between devices with different substrates and interlayers and variant PD. Great linearity is agreed in all cases.

6.3.2 Thermal Boundary Conductance Extraction

Although h-BN has much higher thermal conductivity (390 $W \cdot m^{-1} \cdot K^{-1}$ [147]) than HfO_2 (1.2 $W \cdot m^{-1} \cdot K^{-1}$ [148]), devices with HfO_2 interlayer performs 3x larger ΔT reduction. This suggests that the thermal interfacial conductance is significant here. The insertion of the thermal adhesion layer eliminates the interface of In_2O_3/sapphire but brings in another two interfaces of In_2O_3/interlayer and interlayer/sapphire. By the TR imaging and maximum ΔT comparison discussed, it is observable that the effective TBC of the devices with a h-BN or HfO_2 interlayer is larger than the TBC of the devices without one. In order to quantify the improvement, a steady-state thermal diffusion model with a finite-element method is combined with the TR imaging results to extract the effective TBC values. It is verified in literature that this method of TBC extraction is consistent with experimentally measured TBC values [139], [149].

The steady-state thermal simulation is carried out through COMSOL Multiphysics which adopts a finite-element method. Mesh build-up of the model which is designed to have identical structures and dimensions (L_{ch} of 400 nm and W_{ch} of 2 μm) with the devices used in Figure 6.1(a) and similar to Figure 4.4. The PD is set to be around 5 kW/mm^2 which is the same as the scenarios

in Figure 6.1(a) as well, and the square indicated by the red dashed lines denotes the area of interest which includes the channel region and its proximity. By giving variant effective TBC values of the introduced interfaces, different values of maximum ΔT are obtained as shown in Figure 6.4(b). Considering the experimental ΔT values with the error ranges, the corresponding TBC implied by the steady-state simulation for the devices without an interlayer is extracted to be 11 +4/-4 MW/(m^2·K). Similarly, the effective TBC of the devices with a thermal adhesion layer of h-BN or HfO_2 is extracted to be 21 +6/-5 MW/(m^2·K) or 75 +45/-19 MW/(m^2·K), which is 2 or 7 times larger than the original value, respectively. The huge improvement of effective TBC suggests that the interlayer of h-BN or HfO_2 enhances the heat dissipation that sapphire is capable of, benefiting the SHE alleviation in TG In_2O_3 transistors.

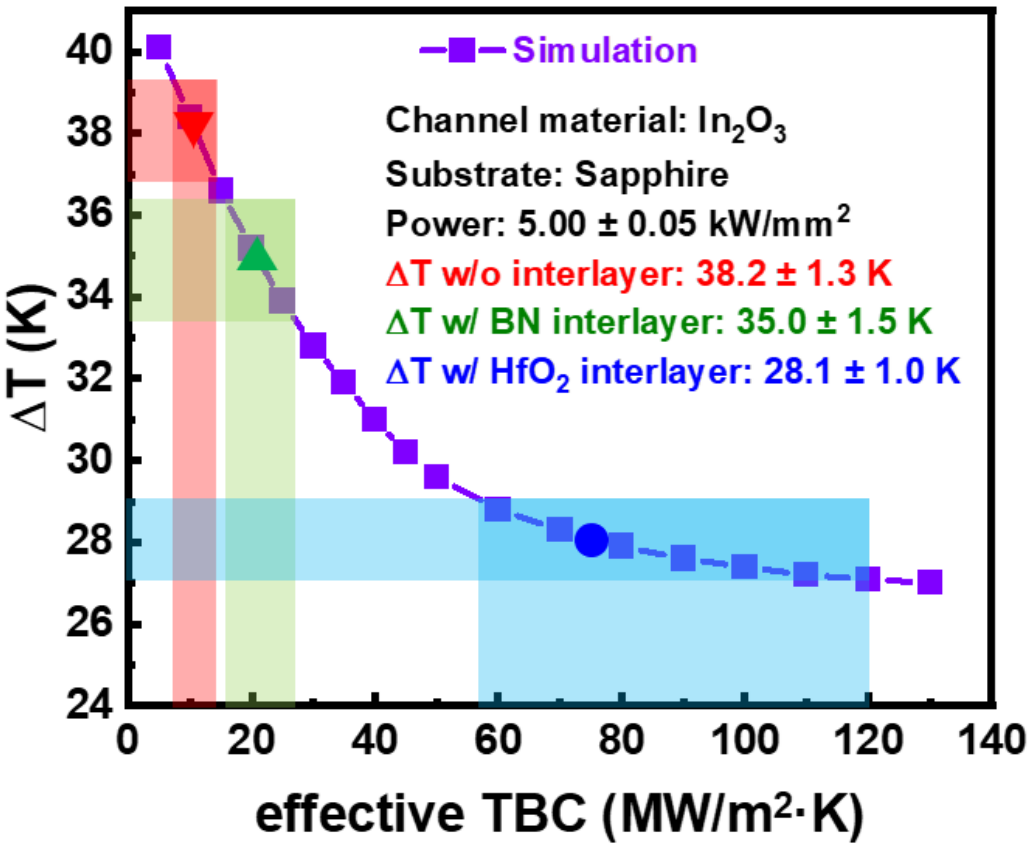

Figure 6.4. Maximum ΔT at the steady-state extracted by setting variant effective TBC. Considering the experimental ΔT error ranges, ranges of effective TBCs are corresponded accordingly.

The obtained effective TBC, including contributions from both the introduced interfaces and the interlayer itself, equals to the inverse of the sum of the inversed thermal conductance of the three contributions. The thermal conductance of the interlayer itself is defined as the thermal conductivity divided by the thickness. It is revealed that thermal conductivity of a thin film is more dependent on its thickness as the thickness is down to the same order of magnitude of the energy carriers' mean free path [150], [151]. Considering the thin-film thermal conductivity of the 4 nm HfO_2 (0.5–1.0 $W \cdot m^{-1} \cdot K^{-1}$ [152]) or 2L h-BN (out-of-plane thermal conductivity 2.3–3.5 $W \cdot m^{-1} \cdot K^{-1}$ [153]) thermal adhesion layer, the TBC contribution from the interlayer itself is roughly 125–250 $MW/(m^2 \cdot K)$ or 1900–3500 $MW/(m^2 \cdot K)$, respectively. The TBC contributions are larger than their individual effective TBC values, indicating that the interlayer itself may not be a critical thermal bottleneck for the effective TBC in either case.

Beside the interlayer itself, there are two introduced interfaces by the insertion of the interlayer, namely, interlayer/sapphire and In_2O_3/interlayer. For the former, the experimentally demonstrated TBC of HfO_2/sapphire interface by time-domain thermo-reflectance (TDTR) is around 227–327 $MW/(m^2 \cdot K)$ [144], which is much larger than the effective TBC of 75 $MW/(m^2 \cdot K)$. Besides, the TBC of h-BN/sapphire is reported to be 980 $MW/(m^2 \cdot K)$ [154] which is also even higher than the effective TBC of 21 $MW/(m^2 \cdot K)$. Consequently, the TBC contribution from the interlayer/sapphire interface is not a main concern in each case, either.

6.4 Phonon Density of States

6.4.1 Calculations

Therefore, the bottleneck of the effective TBC could be the In_2O_3/interlayer interface. Here, phonons as the energy carriers play a significant role. Especially, phonons at lower frequency, called acoustic phonons, are attributed to most of the heat transport behaviors [155]. To investigate the behaviors, the phonon density of states (PDOS) distributions of HfO_2 and sapphire were obtained from literature [139], [156], and the PDOS distribution calculations of h-BN and In_2O_3 were performed by density functional theory (DFT) as implemented in Vienna Ab initio Simulation Package (VASP) [157], [158]. The two calculations on h-BN and In_2O_3 followed different pathways due to the differences in their material properties. A bilayer h-BN with vacuum above and below was constructed to replicate the 2L interlayers in the device. The projector

augmented wave (PAW) [159] method was adopted along with optB86-vdW [160] functional due to the presence of van der Waals forces based on previous work [161]. An energy cut-off of 600 eV was involved together with a 9x9x3 Monkhorst-Pack k-point mesh for structure optimization of the 4-atom bilayer unit cell. Density functional perturbation theory (DFPT) was applied for calculating the second-order force constants on a 6x6x1 supercell with a 3x3x2 k-point grid. The required PDOS were acquired using an open source package Phonopy [162]. The calculated phonon dispersion of 2L h-BN is revealed in Fig. 7(a), and its resultant PDOS distribution is demonstrated in Fig. 7(b). For In_2O_3, the PAW method was used alongside LDA functional with a cut-off of 520 eV. The 40-atom cubic unit cell was optimized utilizing a 4x4x4 Monkhorst-Pack k-point mesh. A supercell of 2x2x2 was constructed with a 2x2x2 k-point mesh for the second-order force constants calculations. However, DFPT is not applicable for In_2O_3 due to the large computational expense of the method for this complicated structure. Hence, the finite differences method for force constants calculation was adopted instead. Similar to h-BN, Phonopy was employed for post-processing and obtaining the PDOS of In_2O_3. The calculated phonon dispersion of In_2O_3 is shown in Fig. 7(c), and its resultant PDOS distribution is demonstrated in Fig. 7(d).

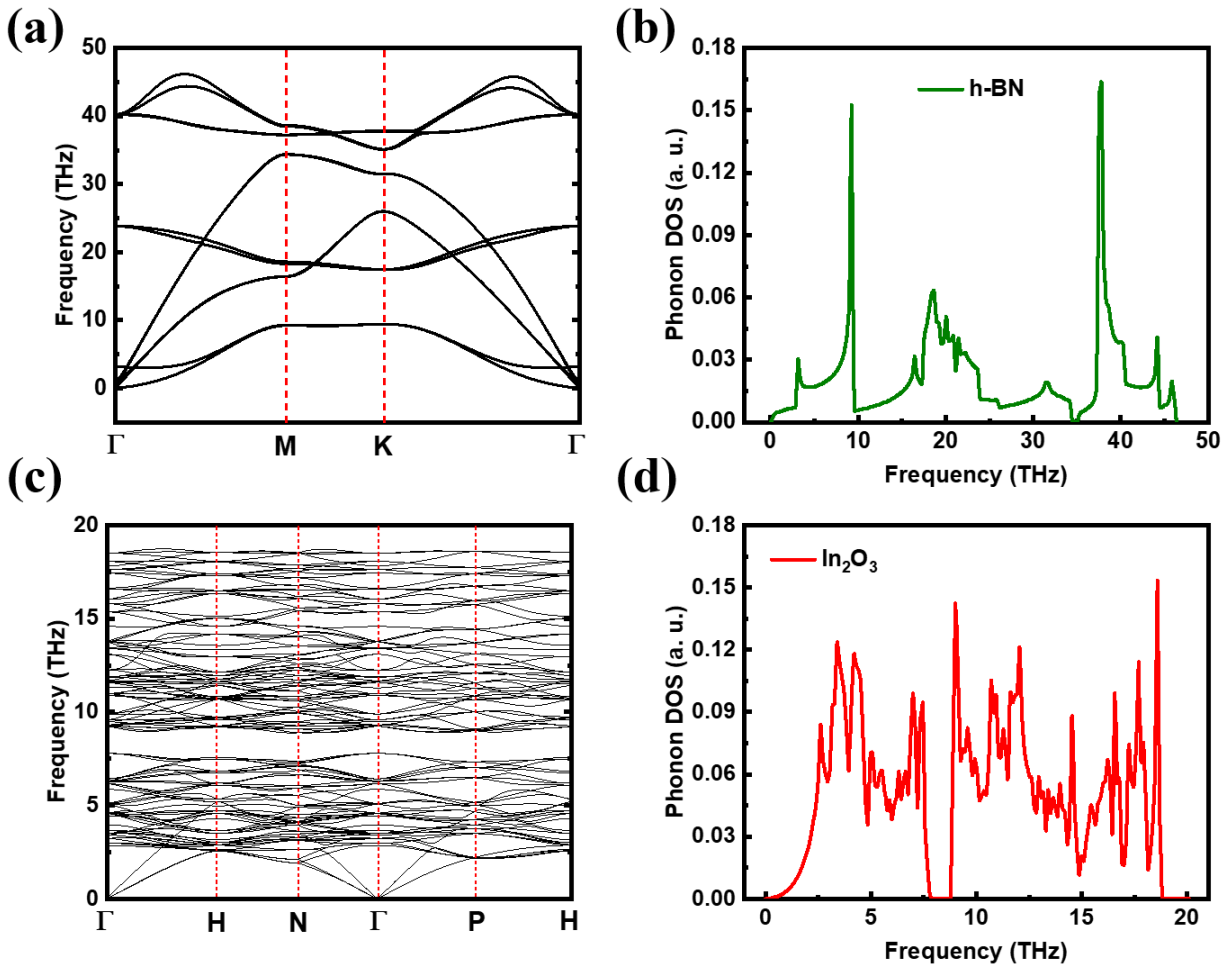

Figure 6.5. Phonon dispersion of (a) h-BN and (c) In_2O_3 performed by first principle calculation and (b, d) the resultant PDOS distributions of them.

6.4.2 Analysis

Figure 6.6 exhibits the PDOS distributions of sapphire, h-BN, and HfO_2 with that of In_2O_3 where fig. 8(a), (c), and (e) show the comparisons of the whole distributions while Figure 6.6(b), (d), and (f) illustrate the acoustic region magnification (frequency lower than 5 THz). All the distributions are normalized by setting the integration area to be one (1). Intersection over union (IOU) ratio is here used to evaluate how well two distributions match with each other and defined as the ratio of their intersection area and their union area. As demonstrated in Figure 6.6(b), the IOU ratio between PDOS of sapphire and In_2O_3 in the acoustic phonon region is only 6.2 %, explaining the low TBC of 11 +4/-4 $MW/(m^2 \cdot K)$. On the other hand, Figure 6.6(d) and (f) indicate

that the IOU ratios in the acoustic phonon region with h-BN and HfO_2 employed are improved to 21.5 and 69.5 %, which are 3 and 11 times larger than 6.2 %, respectively. Due to the much larger IOU ratios in the acoustic phonon region of the PDOS distributions, heat transfer is much more efficient with the presence of the h-BN or HfO_2 interlayer in TG In_2O_3 devices with a sapphire substrate, especially HfO_2. Accordingly, the effective TBC of a) In_2O_3/interlayer interface, b) thin h-BN or HfO_2 stack, and c) interlayer/sapphire interface as a whole is considered satisfactory and improved from the structure without the thermal adhesion layer, which is responsible for the 9 or 27 % of the SHE alleviation observed by the TR imaging, respectively.

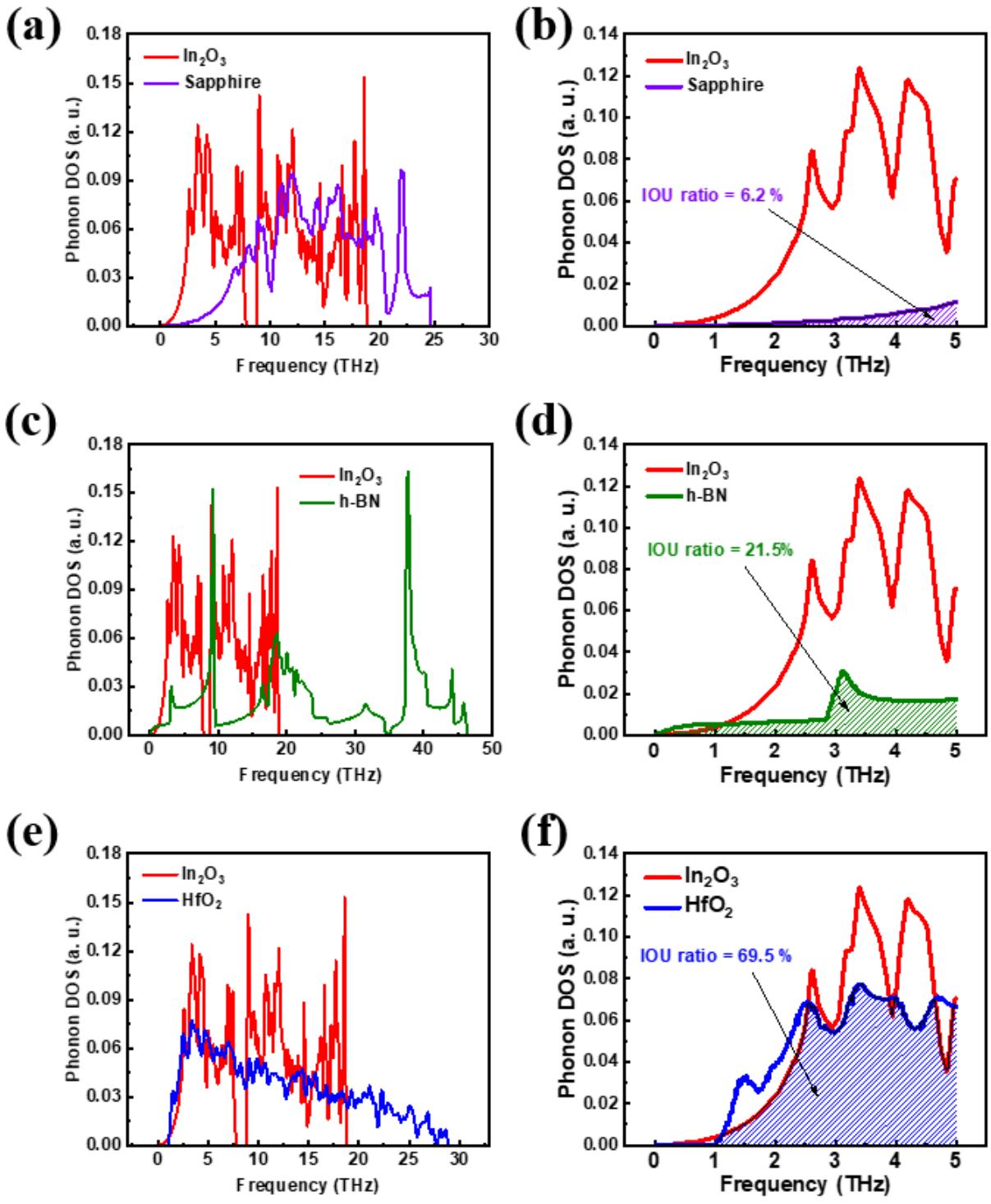

Figure 6.6. PDOS distribution comparison between In_2O_3 and (a) sapphire, (c) h-BN, and (e) HfO_2 and (b, d and f) their acoustic phonon region magnification (frequency lower than 5 THz). The intersection over union (IOU) ratio between PDOS distributions of sapphire, h-BN, and HfO_2 and that of In_2O_3 in the acoustic phonon region are 6.2, 21.5, 69.5 %, respectively

With the extracted effective TBC, the steady-state ΔT distribution is demonstrated in Figure 6.7(a) where the case with HfO_2 interlayer at PD of around 5.04 kW/mm^2 is simulated. For clearer comparison, the TR image of Fig. 4(f) is re-plotted with a modified rainbow-color scale into Figure 6.7(b) where the device with HfO_2 interlayer at PD of 5.04 kW/mm^2 is measured. Figure 6.7(a) and (b) are in excellent agreement, specifying that the experiments and simulation lead to extremely consistent results and support each other. The cross-sections of Figure 6.7(a) and (b) along the direction of channel width are revealed in Figure 6.7(c). The 2 curves are alike and only off a little near the edge of the channel where the experimental curve is smoother while the simulation curve is sharper. On the other hand, Figure 6.7(d) exhibits a false-color image of a TG In_2O_3 transistor with the same structure and dimensions. By comparing Figure 6.7(a), (b), and (d), it is clear that the heat comes from the channel region of the device and transfers to its proximity in all directions, and the SHE is better visualized.

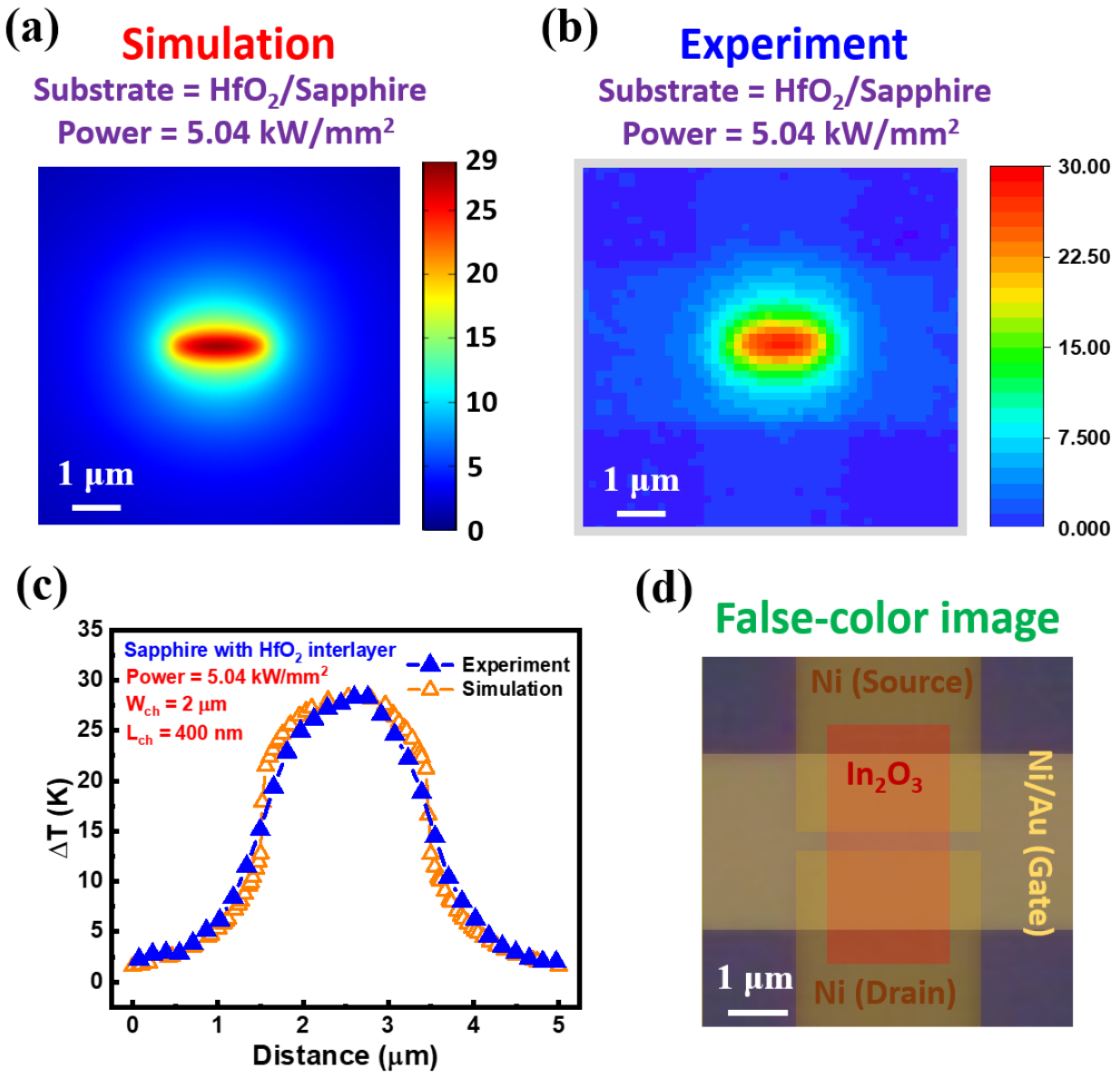

Figure 6.7. (a) A simulated ΔT distribution around the channel region of a TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 µm on a sapphire substrate with HfO_2 interlayer at PD of 5 kW/mm^2. (b) An experimental ΔT distribution of the same region of a transistor with identical structure and dimensions at the same PD imaged by the high-resolution TR equipment. (c) Cross-section comparison along the channel width direction of the experimental and simulation results. (d) A false-color image of a TG In_2O_3 transistor with the same structure and dimensions for better visualization of the SHE

Therefore, by growing a HfO_2 interfacial layer on a sapphire substrate for thermal adhesion, the SHE of TG In_2O_3 devices is much diminished. Figure 6.8(a) exhibits the output characteristics of a TG In_2O_3 transistor with T_{ch} of 2.1 nm, L_{ch} of 80 nm, W_{ch} of 2 μm on a HfO_2/sapphire substrate where extremely high I_D of 2.4 mA/μm is demonstrated. The I_D–V_{DS} curves are well-performed with some saturation behaviors at low V_{GS}, and the SHE is negligible. Figure 6.8(b) reveals the corresponding transfer characteristics where an ON–OFF ratio larger than 3 orders of magnitude is behaved even though the device is in depletion mode. The solid curves are in logarithmic scale, and the empty symbols represent the identical curve in linear scale.

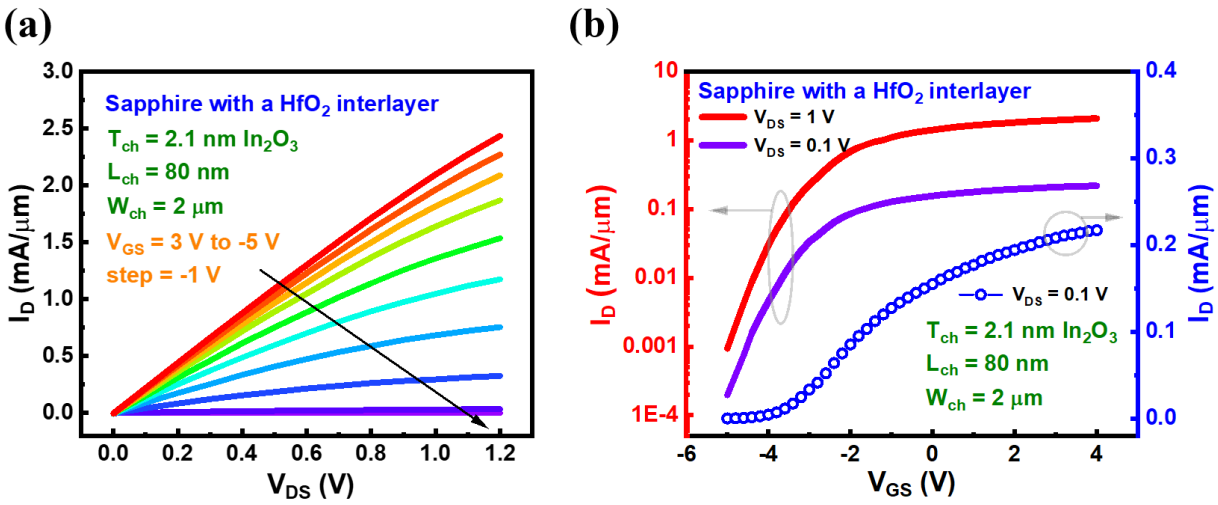

Figure 6.8. (a) Output and (b) transfer characteristics of a 2.1-nm-thick TG In_2O_3 transistor with L_{ch} of 80 nm and W_{ch} of 2 μm on a sapphire substrate with a HfO_2 thermal adhesion layer. Due to the great heat transfer properties of the substrate, SHE is negligible, and maximum I_D of 2.4 mA/μm is achieved at V_{DS} of 1.2 V. The ON–OFF ratio is roughly 4 orders of magnitude

Although substrate materials with even higher thermal conductivity such as silicon carbide (SiC, 387 $W \cdot m^{-1} \cdot K^{-1}$) [163] and diamond (2200 $W \cdot m^{-1} \cdot K^{-1}$) [134] normally have substandard affordability and relatively limited commercial availability, they are generally advantageous against others for power device applications. Nevertheless, thermal interfacial issues at the channel/substrate interface may also restrict the benefit they can conduct to some degree. This work provides a route to potentially resolve this challenge and maximize the profits that those substrates with high thermal conductivity can bring to relieve SHE.

As a chapter summary, heat dissipation of TG ultrathin In_2O_3 transistors on a sapphire substrate with 2L h-BN, 4 nm HfO_2, or no interlayer is explored to assist alleviating SHE. A high spatial resolution TR measurement system is introduced to visualize the ΔT distribution as the devices are self-heating. With the thermal adhesion layer of h-BN or HfO_2 to improve the interfacial heat transfer between the In_2O_3 channel and the sapphire substrate, the observed maximum ΔT of the devices is reduced by 9 or 27 %, respectively. A steady-state thermal diffusion model with a finite-element method is integrated with the TR imaging results to extract the effective TBC values in each case to quantify the improvement of the interfacial heat transfer. The effective TBC is enhanced by a factor of 2 or 7 with the insertion of the h-BN or HfO_2 interlayer. The huge amelioration of the effective TBC is likely due to the better match of the PDOS distribution in the acoustic region where the IOU ratio of In_2O_3 with h-BN or HfO_2 is 3 or 11 times larger than that with sapphire. Because of the cured SHE, extremely high I_D of 2.4 mA/μm is realized in TG In_2O_3 transistors with ultrathin T_{ch} of 2.1 nm, L_{ch} of 80 nm, and W_{ch} of 2 μm on a HfO_2/sapphire substrate. This thermal management method can be potentially applied to In_2O_3 devices with other substrates such as diamond or even devices with other channel materials for further investigations to alleviate SHE.

7. SUMMARY AND OUTLOOK

Two novel channel material systems with ultrahigh drain current density, tellurium (Te) and ALD indium oxide (In_2O_3), for post-Moore era were discussed in this thesis. Especially, a variety of techniques to alleviate the self-heating effect (SHE), caused by the high drain current and high device power density, were systematically investigated and introduced.

In chapter 1, the potential materials which once attracted much attention including graphene, transition metal dichalcogenides (TMDs), and black phosphorus (BP) were briefly reviewed. Besides, the individual drawbacks of these materials as potential candidates for post-Moore era electronics were also introduced.

Chapter 2 focused on employing one-dimensional Te encapsulated in boron nitride nanotube (BNNT) as field-effect transistors (FETs). FETs with diameter down to 2 nm and large current density up to 150 MA/cm^2 were demonstrated. Due to the superior thermal conductivity of boron nitride, it turns out that SHE is not a concern. Nevertheless, the lack of a reliable synthesis method to grow wafer-scale single crystalline Te restricts the applications in mass production.

From chapter 3 to chapter 6, ALD In_2O_3 which overcomes all the downsides of the previous candidate materials was introduced. Graphene as a semi-metal has no bandgap while In_2O_3 has a proper bandgap of 2.9 eV; TMDs perform relatively low carrier mobility (generally lower than 20 $cm^2 \cdot V^{-1} \cdot s^{-1}$) while In_2O_3 has shown mobility up to 113 $cm^2 \cdot V^{-1} \cdot s^{-1}$; BP is not air-stable while In_2O_3 as an oxide material stays extremely stable in ambience; there is no reliable growth method reported for wafer-scale single crystalline for Te while ALD provides wafer-scale conformal growth for In_2O_3. However, ALD In_2O_3 transistors with high power density encounter serious SHE which not only restricts its applicability but also harms its long-term reliability. To address the thermal issues, several techniques were proposed and demonstrate from chapter 3 to chapter 6.

In chapter 3, substrate substitution is utilized to diminish the SHE. Highly resistive silicon (HR Si), which has approximately 100 times higher thermal conductivity than SiO_2, was introduced to assist transferring the generated heat at the channel. Through transconductance degradation measurement, the difference between employing the HR Si and SiO_2/Si substrates was demonstrated. Nonetheless, this method was not able to directly measure the temperature of the devices as they self-heat.

Therefore, in chapter 4, an ultrafast high-resolution thermo-reflectance (TR) imaging equipment was introduced. Moreover, for comprehensive comparisons between substrates with different thermal conductivity, sapphire (chapter 4) and diamond (chapter 5) also served as substrates. Through the TR measurement, the temperature increase (ΔT) due to the SHE was experimentally observed, and it was demonstrated that the ΔT of the devices with sapphire, HR Si, and diamond substrates performed SHE reduction by factors of 2.6, 6, and 13, respectively.

Chapter 5 focused on the exploration of the time-resolved self-heating process and the corresponding resolution to avoid SHE. The TR imaging equipment was used to study the transient thermodynamics by setting a series of timing for capturing the active images. With the understanding of the transient self-heating characteristics, short-pulse measurement with pulse width shorter than a heat-up time constant (τ_h) was designed to measure the electrical transport characteristics and avoid the SHE from the root at the same time. Accordingly, extremely high drain current up to 4.3 mA/μm at large drain bias of 3.2 V was achieved with 1.9-nm-thick ALD TG In_2O_3 FETs without observable SHE.

In chapter 6, a study to resolve the interfacial thermal issues was demonstrated. Due to the low thermal boundary conductance (TBC) between In_2O_3 channel and sapphire substrate, the capability of sapphire as a thermally conductive substrate was restricted to some degree. Consequently, a 2L h-BN or 4 nm HfO_2 was introduced as a thermal adhesion layer. It was revealed that the effective TBC was improved by a factor of 2 or 7 with the presence of the BN or HfO_2 interlayer, which was due to the better phonon density of state (PDOS) distribution. Through PDOS calculation, it was shown that the intersection over union (IOU) ratio at the h-BN/In_2O_3 or HfO_2/In_2O_3 interface was 3 or 11 times larger than the sapphire/In_2O_3 interface.

Looking forward, there are still remaining topics to study to further understand and resolve the SHE in TG ALD In_2O_3 transistors. A few instances are described below.

One of the advantages of ALD In_2O_3 is that the fabrication process is back-end-of-line (BEOL) compatible, which makes it a promising material towards monolithic 3D integration. However, some of the thermally conductive substrates presented in this thesis, such as sapphire and diamond, are not BEOL compatible. To maintain the compatibility and simultaneously employing a thermally conductive substrate, aluminum nitride (AlN) can be a potential candidate. AlN can be deposited by ALD under relatively low temperature and has a high thermal conductivity of roughly 170 $W \cdot m^{-1} \cdot K^{-1}$.

Another direction which can follow this work is to understand the transient thermodynamics of the self-heating process from a physical angle of view. The work focused on observing the effect phenomenon-wise and utilized the observations to address the SHE. More explorations to understand the relationships between SHE and, for example, carrier transport, are still open for investigations.

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VITA

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PUBLICATIONS

(† Equal contribution)

[1] **P.-Y. Liao**, M. Si, Z. Zhang, Z. Lin, and P. D. Ye, "Realization of maximum 2 A/mm drain current on top-gate atomic-layer-thin indium oxide transistors by thermal engineering," *IEEE Trans. Electron Device*, vol.69, pp. 147–151, 2021.

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